National Semiconductor

400035

National Data Acquisition Databook

Data Acquisition Systems
Analog-to-Digital Converters
Digital-to-Analog Converters
Voltage Reference
Temperature Sensors
Sample and Hold
Active Filters
Analog Switches/Multiplexers

DATA ACQUISITION
DATABOOK

1995 Edition

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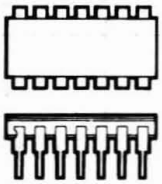
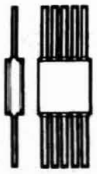
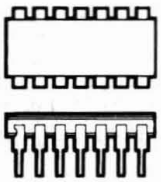
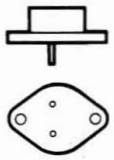
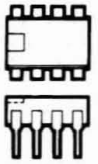
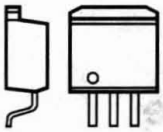
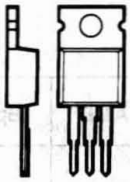
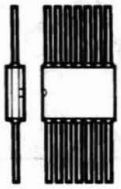
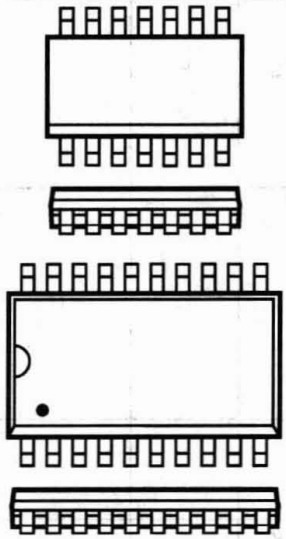
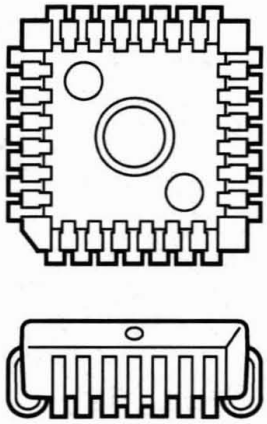
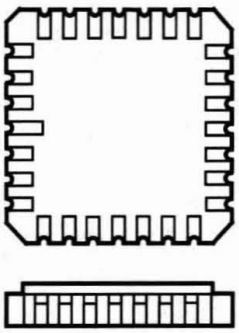
National Semiconductor

Industry Package Cross-Reference Guide

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
 4/16 Lead Glass/Metal DIP	D	D	I	L		D	R
 Glass/Metal Flat Pack	F	F	Q	F	F, S	F	
TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	H	
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J	D	H
 TO-3 (Steel)	K			KS			
TO-3 (Aluminum)	KC	K	DA	K	K		
 8-, 14- and 16-Lead Plastic DIP	N	T, P	N, V	P	P, N	P	A, B, M

		NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
	TO-263 3- & 5-Lead	S						
	TO-220 3- & 5-Lead	T	U	U		KC		
	TO-220 11-, 15- & 23-Lead	T						
	Low Temperature Glass Hermetic Flat Pack	W	F		F	W	F	
	TO-92 (Plastic)	Z	W	S	P	LP		
	SO (Narrow Body)	M	S	S, D	D	D		L
	(Wide Body)	WM				DW		LW
	SOT-23 5-Lead	M5						

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
 PCC	V	Q	A	FN	FN	L	EP
 LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	L	EK

Section 1

Data Acquisition Systems

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Data Acquisition Systems Definition of Terms

Throughput Time: The time it takes from addressing the analog input channels till valid data is read on the output. In the case of systems such as the LM12454/8 family, this includes reading the sequencer instruction, selecting the proper multiplexer input channels and waiting for them to settle, the conversion time of the A/D, storing the results in the FIFO, sending a data request, and one clock cycle for the read to occur.

Throughput Rate: The inverse of the Throughput Time.

Watchdog Mode: This mode of operation is used to monitor an analog input's amplitude to two preset (and programmable) limits. An interrupt signal can be generated if the input signal is above or below either of the two limits. As the preset limits are fed into the successive approximation A/D's internal D/A, and then compared to the input signal, the watchdog mode can provide a quick and accurate assessment of a possible alarm condition.

Part No.	I/O Type	Mode/Res' (Bits)	Accuracy (Max)	Conversion Time (Max)	S/H	# MUX Inputs	On-Board Reference	Supply Voltage	Temp Range	Power (mW Max)	Packages	Comments
ADC0851B	Serial	8 W	±½ LSB	18 μs 2 μs	N	2	N	+5V	I, M	50 mW	N, V	
ADC0851C	Serial	8 W	±1 LSB	18 μs	N	2	N	+5V	I, M	50 mW	N, V	
ADC0858B	Serial	8 W	±½ LSB	18 μs	N	8	N	+5V	I, M	50 mW	N, V	
ADC0858C	Serial	8 W	±1 LSB	18 μs	N	8	N	+5V	I, M	50 mW	N, V	
LM12454	Parallel/ Byte-Wide	12 + Sign 8 + Sign W	±1 LSB	8.8 μs 4.2 μs	Y	4	Y	+5V	I	30 mW	V	On-Board Timer, FIFO, Sequencer
LM12458	Parallel/ Byte-Wide	12 + Sign 8 + Sign W	±1 LSB	8.8 μs 4.2 μs	Y	8	Y	+5V	I, M	30 mW	V, VF, EL	On-Board Timer, FIFO, Sequencer
LM12H454	Parallel/ Byte-Wide	12 + Sign 8 + Sign W	±1 LSB	5.5 μs 2.6 μs	Y	4	Y	+5V	I	34 mW	V	On-Board Timer, FIFO, Sequencer
LM12H458	Parallel/ Byte-Wide	12 + Sign 8 + Sign W	±1 LSB	5.5 μs 2.6 μs	Y	8	Y	+5V	I, M	34 mW	V, VF, EL	On-Board Timer, FIFO, Sequencer
LM12L458	Parallel/ Byte-Wide	12 + Sign 8 + Sign W	±1 LSB	7.3 μs 3.5 μs	Y	8	Y	+5V	I, M	15 mW	V, VF, EL	3V Operation
LM12L454	Parallel/ Byte-Wide	12 + Sign 8 + Sign W	±1 LSB	7.3 μs 3.5 μs	Y	4	Y	+5V	I, M	15 mW	V, VF, EL	3V Operation
LM12434	Serial	12 + Sign 8 + Sign W	±1 LSB	5.5 μs 2.6 μs	Y	4	N	+5V	I	45 mW	V, M	On-Board Timer, FIFO, Sequencer
LM12438	Serial	12 + Sign 8 + Sign W	±1 LSB	5.5 μs 2.6 μs	Y	8	N	+5V	I	45 mW	V, M	On-Board Timer, FIFO, Sequencer
LM12L438	Serial	12 + Sign 8 + Sign W	±1 LSB	7.3 μs 3.5 μs	Y	8	N	+5V	I	20 mW	V, M	3V Operation

Resolution: W Watchdog Comparison Mode *(See datasheets for details)*

Package Codes:
- N Plastic DIP
- M Small Outline
- V PLCC
- VF PQFP
- EL CLCC

Temperatures:
- C 0°C to +70°C
- I −25°C to +85°C or −40°C to +85°C
- M −55°C to +125°C

National Semiconductor

Data Acquisition Systems Selection Guide

National Semiconductor

ADC0851 and ADC0858 8-Bit Analog Data Acquisition and Monitoring Systems

General Description

The ADC0851 and ADC0858 are 2 and 8 input analog data acquisition systems. They can function as conventional multiple input A/D converters, automatic scanning A/D converters or programmable analog "watchdog" systems. In "watchdog" mode they monitor analog inputs and determine whether these inputs are inside or outside user programmed window limits. This monitoring process takes place independent of the host processor. When any input falls outside of its programmed window limits, an interrupt is automatically generated which flags the processor; the chip can then be interrogated as to exactly which channels crossed which limits.

The advantage of this approach is that its frees the processor from having to frequently monitor analog variables. It can consequently save having to insert many A/D subroutine calls throughout real time application code. In control systems where many variables are continually being monitored this can significantly free up the processor, especially if the variables are DC or slow varying signals.

The Auto A/D conversion feature allows the device to scan through selected input channels, performing an A/D conversion on each channel without the need to select a new channel after each conversion.

Key Specifications

- Resolution — 8 Bits
- Total error — ±½ LSB or ± 1 LSB
- Low power — 50 mW
- Conversion time — 18 μs/Channel
- Limit comparison time — 2 μs/Limit

Features

- Watchdog operation signals processor when any channel is outside user programmed window limits
- Frees microprocessor from continually monitoring analog signals and simplifies applications software
- 2 (ADC0851) or 8 (ADC0858) analog input channels
- Single ended or differential input pairs
- COM input for DC offsetting of input voltage
- 4 (ADC0851) and 16 (ADC0858), 8-bit programmable limits
- NSC MICROWIRE™ interface
- Power fail detection
- Auto A/D conversion feature
- Single 5V supply
- Window limits are user programmable via serial interface

Applications

- Instrumentation monitoring and process control
- Digitizing automotive sensor signals
- Embedded diagnostics

Simplified Block Diagram

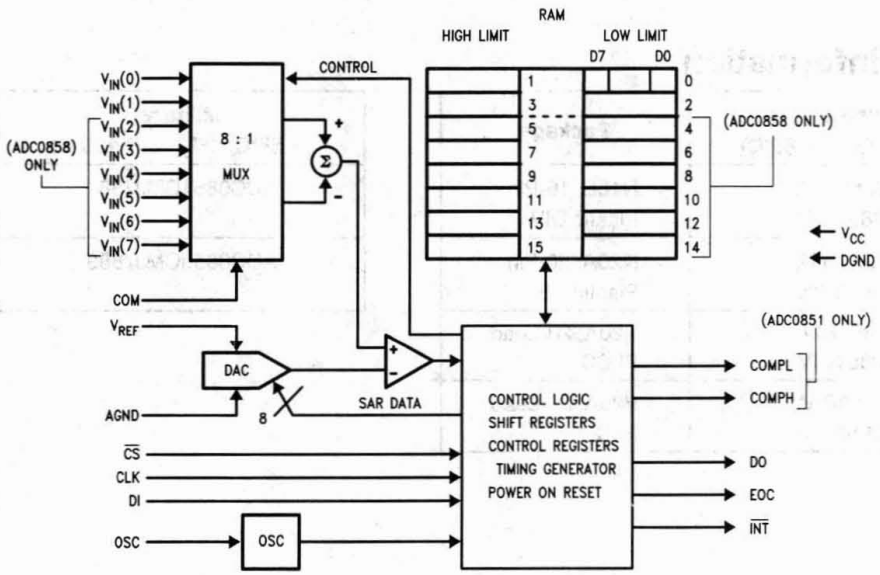

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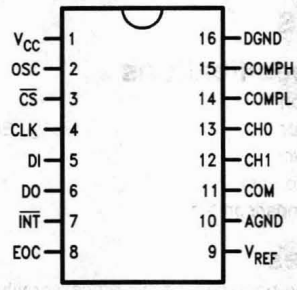
FIGURE 1

Connection Diagrams

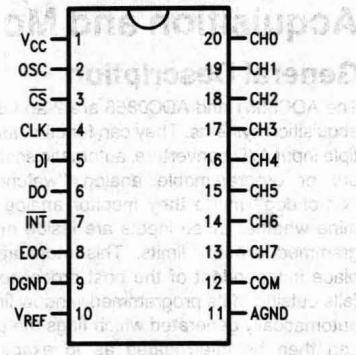
ADC0851
2-Channel MUX
Dual-In-Line Package



TL/H/11021–1

Top View

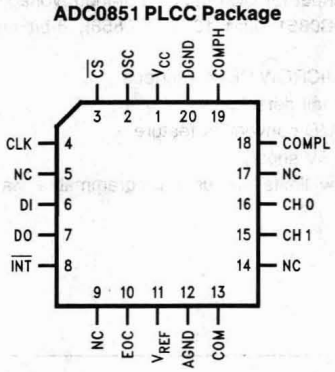
ADC0858
8-Channel MUX
Dual-In-Line Package



TL/H/11021–2

Top View

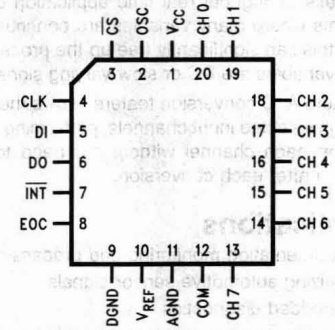
ADC0851 PLCC Package



TL/H/11021–3

Top View

ADC0858 PLCC Package



TL/H/11021–4

Top View

Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC0851BIN, ADC0851CIN	N16E, 16-Pin Plastic DIP
ADC0858BIN, ADC0858CIN	N20A, 20-Pin Plastic DIP
ADC0851BIV, ADC0851CIV	V20A, 20-Lead PLCC
ADC0858BIV, ADC0858CIV	V20A, 20-Lead PLCC

Military ($-55°C \leq T_A \leq +125°C$)	Package
ADC0851CMJ/883	J16A, 16-Pin Ceramic DIP
ADC0858CMJ/883	J20A, 20-Pin Ceramic DIP

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	6.5V
Voltage at Logic and Analog Inputs (Note 3)	−0.3V to V_{CC} + 0.3V
Input Current per Pin	±5 mA
Input Current per Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = +25°C (Board Mount)	500 mW 800 mW
Lead Temperature (Soldering, 10 Sec.)	
Dual-In-Line (Plastic)	+260°C
Dual-In-Line (Ceramic)	+300°C
ESD Susceptibility (Note 4)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5V to 5.5V
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0858CMJ/883	$-55°C \le T_A \le +125°C$
ADC0851CMJ/883	$-55°C \le T_A \le +125°C$
ADC0858BIN, ADC0858CIN	$-40°C \le T_A \le +85°C$
ADC0851BIN, ADC0851CIN	$-40°C \le T_A \le +85°C$
ADC0858BIV, ADC0858CIV	$-40°C \le T_A \le +85°C$
ADC0851BIV, ADC0851CIV	$-40°C \le T_A \le +85°C$

DC Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +4.5 V_{DC}, AGND = DGND = 0V and f_{OSC} = 1 MHz (R_{ext} = 3.16 kΩ, C_{ext} = 170 pF) unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits apply at T_A = T_J = +25°C.

Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units (Limits)
CONVERTER AND MULTIPLEXER CHARACTERISTICS				
Total Unadjusted Error (Note 7)				
ADC0851/8/BIN, ADC0851/8/BIV			**±½**	LSB (Max)
ADC0851/8/CIN, ADC0851/8/CMJ,			**±1**	LSB (Max)
ADC0851/8/CIV			**±1**	LSB (Max)
Comparator Offset				
ADC0851/8/BIN, ADC0858BIV		±2.5	**±10**	mV (Max)
ADC0851/8/CIN, ADC0851/8/CMJ,		±2.5	**±20**	mV (Max)
ADC0858CIV		±2.5	**±20**	mV (Max)
V_{REF} Input Resistance		6	**3.5** **10**	kΩ (Min) kΩ (Max)
Common Mode Input Voltage (Note 8)	All MUX Inputs and COM Input		**GND − 0.05** **V_{CC} + 0.05**	V (Min) V (Max)
DC Common Mode Error	ΔV_{CM} = −0.05V to +5.05V	±1/16	**±1/4**	LSB (Max)
Power Supply Sensitivity	V_{REF} = 4.75V V_{CC} = 5V ± 5%	±1/16	**±1/4**	LSB (Max)
	V_{REF} = 4.5V V_{CC} = 5V ± 10%	±1/16	**±1/2**	
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V Off Channel = 0V	−0.01	**−3**	µA (Max)
	On Channel = 0V Off Channel = 5V	+0.01	**+3**	µA (Max)
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 5V Off Channel = 0V	+0.01	**+3**	µA (Max)
	On Channel = 0V Off Channel = 5V	−0.01	**−3**	µA (Max)

DC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +4.5 V_{DC}, AGND = DGND = 0V and f_{OSC} = 1 MHz (R_{ext} = 3.16 kΩ, C_{ext} = 170 pF) unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits apply at T_A = T_J = +25°C.

Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units (Limits)
DIGITAL CHARACTERISTICS				
Logic "1" Input Voltage, V_{IH}	V_{CC} = 5.5V		**2.2**	V (Min)
Logic "0" Input Voltage, V_{IL}	V_{CC} = 4.5V		**0.8**	V(Max)
Logic "1" Input Current, I_{IH}	V_{IN} = V_{CC}	0.005	**3**	μA (Max)
Logic "0" Input Current, I_{IL}	V_{IN} = 0V	−0.005	**−3**	μA (Max)
Logic "1" Output Voltage, V_{OH} (Except $\overline{INT}$)	V_{CC} = 4.5V I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.2**	V (Min) V (Min)
Logic "0" Output Voltage, V_{OL}	I_{OUT} = 1.6 mA V_{CC} = 4.5V		**0.4**	V (Max)
TRI-STATE® Output Current (DO)	$\overline{CS}$ = Logic "1" (5V) V_{OUT} = 0.4V V_{OUT} = 5V	 −0.1 0.1	 **−3** **3**	 μA (Max) μA (Max)
I_{SOURCE} (Except $\overline{INT}$)	V_{OUT} Short to GND	−14	**−6.5**	mA (Min)
I_{SINK}	V_{OUT} Short to V_{CC}	16	**8**	mA (Min)
Supply Current, I_{CC} ADC0851 or ADC0858	f_{CLK} = 1 MHz f_{CLK} = 2 MHz (Note 10)	7 7.2	**10**	mA (Max) mA

AC Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +4.5 V_{DC}, AGND = DGND = 0V, f_{CLK} = 1 MHz, t_r = t_f = 5 ns unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits apply at T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units (Limits)
f_{CLK}	Data Clock Frequency		1	**2**	MHz (Max)
	Clock Duty Cycle (Note 11)			**40** **60**	% (Min) % (Max)
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge		30	**70**	ns (Min)
t_{HOLD}	Data Input Valid after CLK Rising Edge		5	**30**	ns (Min)
t_{PD1}, t_{PD0}	CLK Rising Edge to Output Data Valid	C_L = 100 pF	80	**200**	ns (Max)

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +4.5 V_{DC}, AGND = DGND = 0V, f_{CLK} = 1 MHz, t_r = t_f = 5 ns unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits apply at T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units (Limits)
t_{1H}, t_{0H}	Rising Edge of $\overline{CS}$ to Data Output Hi-Z	C = 100 pF, R = 2k (See TRI-STATE Test Circuits)	90	**200**	ns (Max)
f_{OSC}	Oscillator Clock Freq. (Analog Timing)	R_{ext} = 3.16 kΩ C_{ext} = 170 pF	1	**1.4** **0.6**	MHz (Max) MHz (Min)
t_{EOC}	$\overline{CS}$ to End of Conversion Delay			 **1** **2**	OSC Clock Periods Min Max
t_{Conv}	Conversion Time			 **17** **18**	OSC Clock Periods (Min) (Max)
$t_{\overline{CS}\text{-}\overline{INT}}$	$\overline{CS}$ to Interrupt Delay		60	**120**	ns (Max)
C_{IN}	Capacitance of Logic Input		5		pF
C_{OUT}	Capacitance of Logic Output		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground (AGND = DGND = 0V).

Note 3: All of the analog and digital input pins are internally diode clamped to the supply pins. Should the applied voltage at any pin exceed the power supply voltage, the additional absolute value of current at that pin (caused by the forward biasing of the internal diodes) should be limited to 5 mA or less.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Total unadjusted error includes comparator offset, ADC linearity and multiplexer error, and, is expressed in LSBs.

Note 8: Two on-chip diodes are tied to each analog input. The diodes will forward conduct for analog input voltages one diode drop below ground or one diode drop above V_{CC}. Care should be exercised when operating the device at low supply voltages (e.g., V_{CC} = 4.5V) because high analog inputs (5V) can cause the input diodes to conduct, especially at elevated temperatures. This will cause errors for analog inputs near full scale. The specification allows 50 mV forward bias of either clamp diode. Thus as long as V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC}.

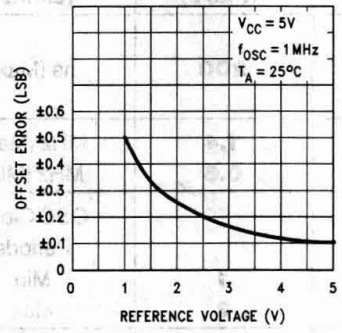
Note 9: Leakage current is measured with the oscillator clock disabled.

Note 10: Measured supply current does not include the DAC ladder current.

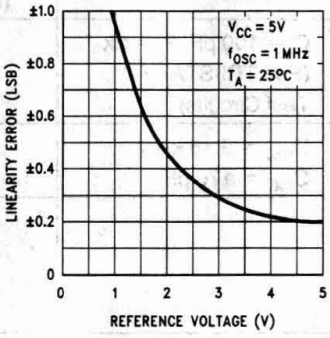
Note 11: A 40% to 60% clock duty cycle range ensures proper operation at all clock frequencies.

Typical Performance Characteristics

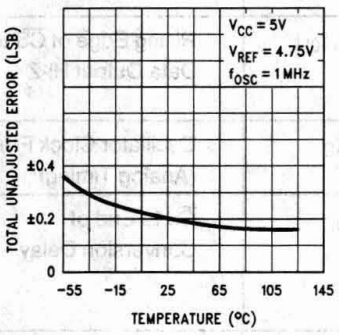
Offset Error vs Reference Voltage



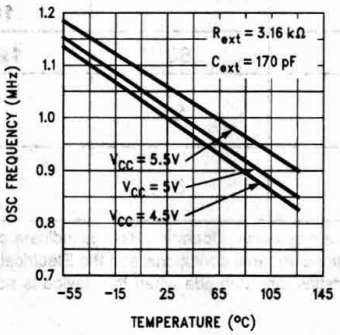
Linearity Error vs Reference Voltage



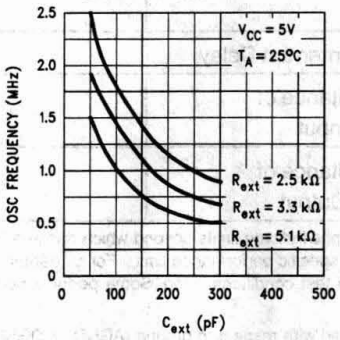
Total Unadjusted Error vs Temperature



OSC Frequency vs Temperature



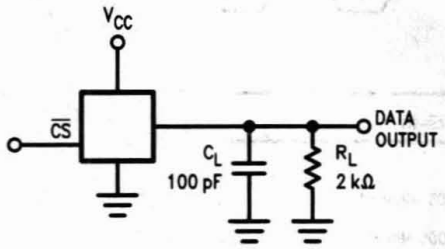
OSC Frequency vs R_{ext} and C_{ext}



TL/H/11021–5

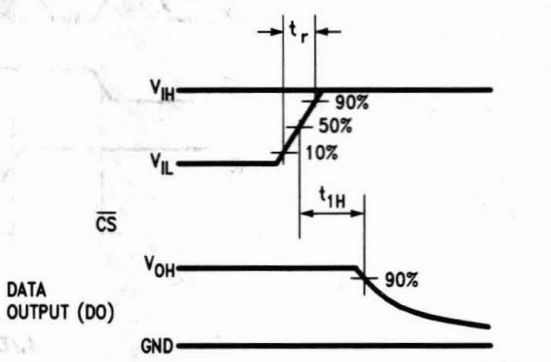
Test Circuits and Waveforms

t_{1H}



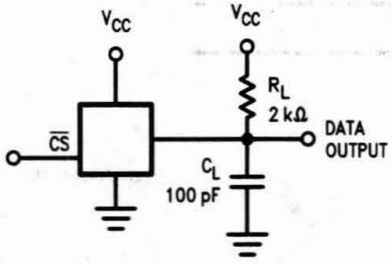
TL/H/11021-6

t_{1H}, C_L = 10 pF



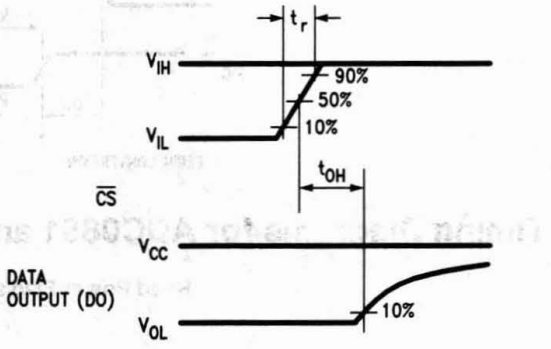
TL/H/11021-8

t_{0H}



TL/H/11021-7

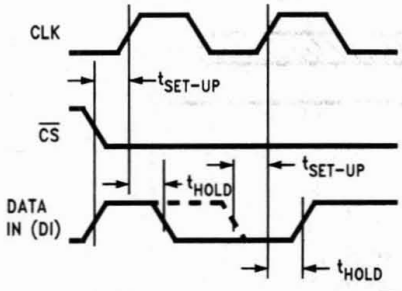
t_{1H}, C_L = 10 pF



TL/H/11021-9

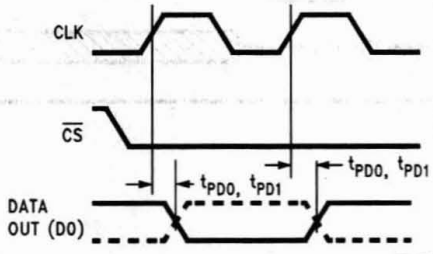
Timing Diagrams

Data Input Timing



TL/H/11021-10

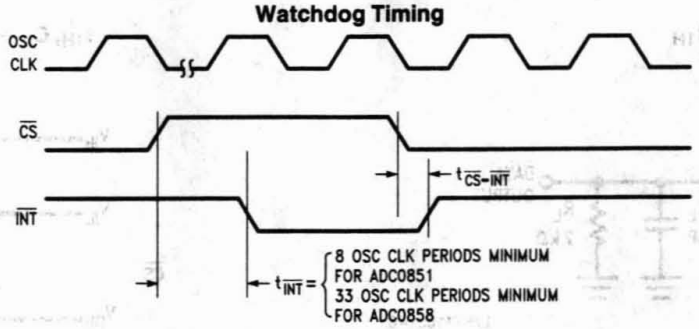
Data Output Timing



TL/H/11021-11

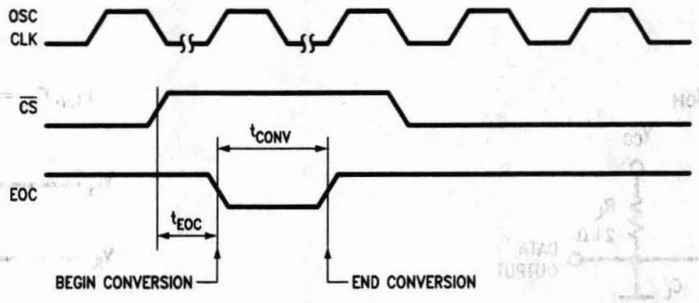
Timing Diagrams (Continued)

Watchdog Timing



TL/H/11021–12

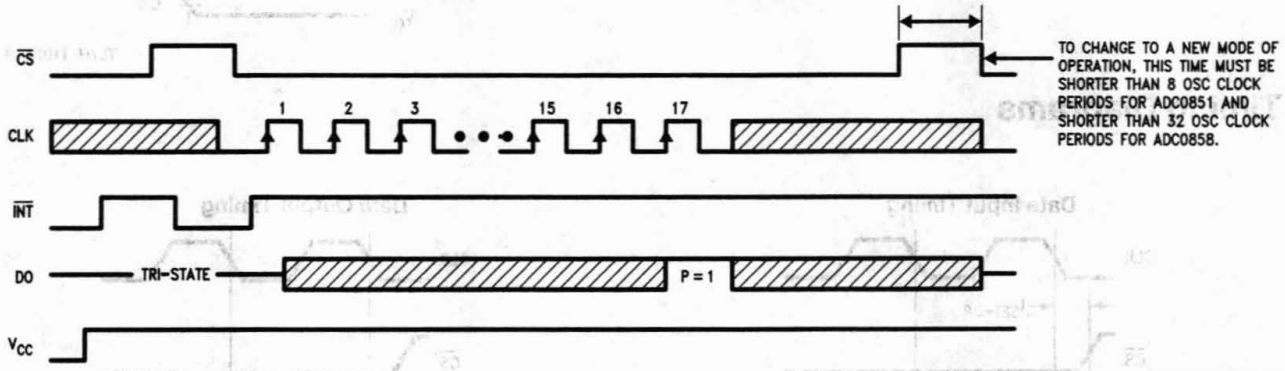
A/D Conversion Timing



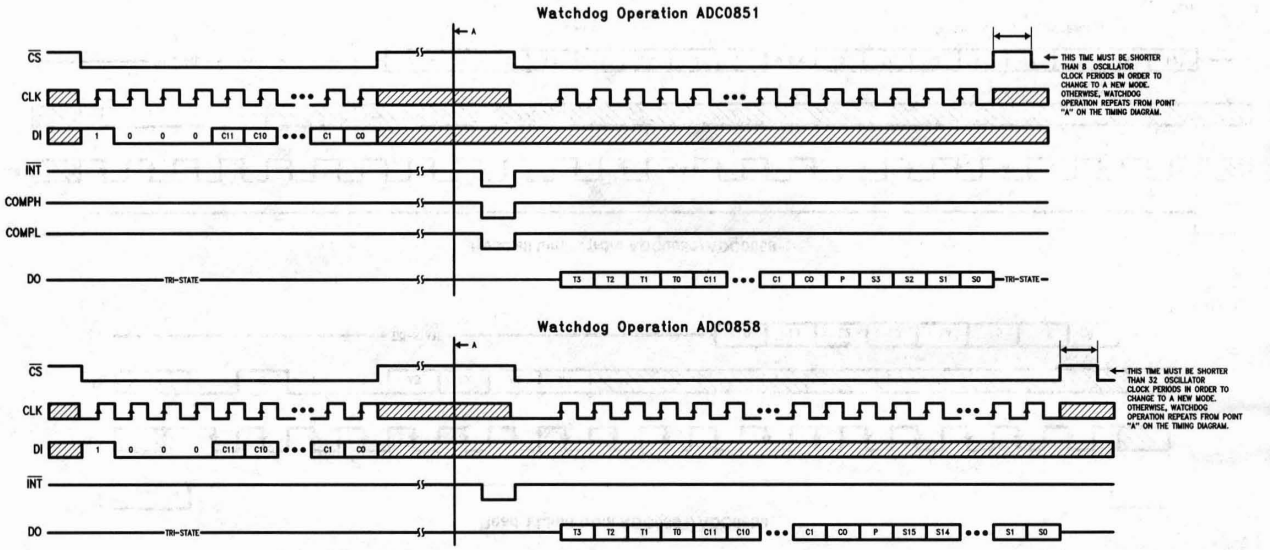
TL/H/11021–13

Timing Diagrams for ADC0851 and ADC0858

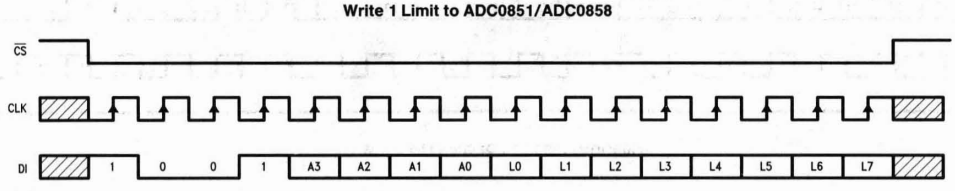
Read Power Flag after Power Up ADC0851/ADC0858



TL/H/11021–14


Watchdog Operation ADC0851
CS
CLK
DI
INT
COMPH
COMPL
DO
TRI-STATE
THIS TIME MUST BE SHORTER THAN 8 OSCILLATOR CLOCK PERIODS IN ORDER TO CHANGE TO A NEW MODE. OTHERWISE, WATCHDOG OPERATION REPEATS FROM POINT "A" ON THE TIMING DIAGRAM.
Watchdog Operation ADC0858
THIS TIME MUST BE SHORTER THAN 32 OSCILLATOR CLOCK PERIODS IN ORDER TO CHANGE TO A NEW MODE. OTHERWISE, WATCHDOG OPERATION REPEATS FROM POINT "A" ON THE TIMING DIAGRAM.

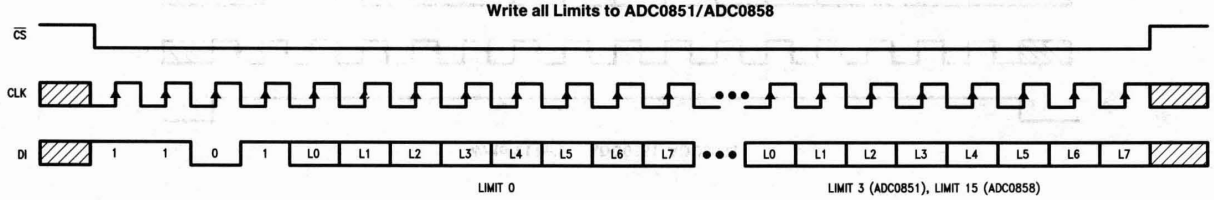
TL/H/11021–15



TL/H/11021–16

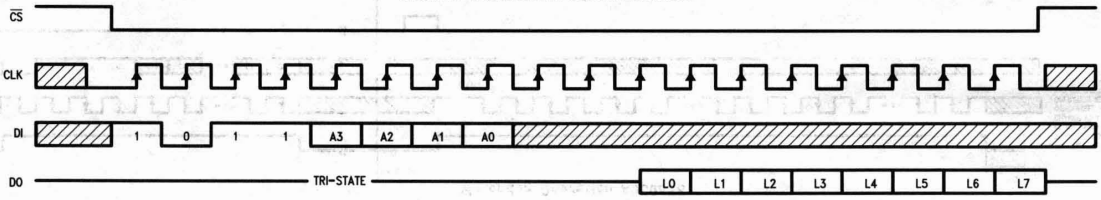
Timing Diagrams for ADC0851 and ADC0858 (Continued)

Write all Limits to ADC0851/ADC0858



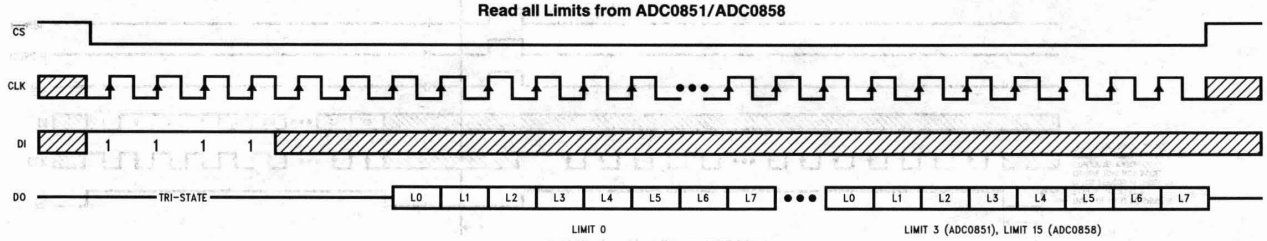
TL/H/11021–17

Read 1 Limit from ADC0851/ADC0858



TL/H/11021–18

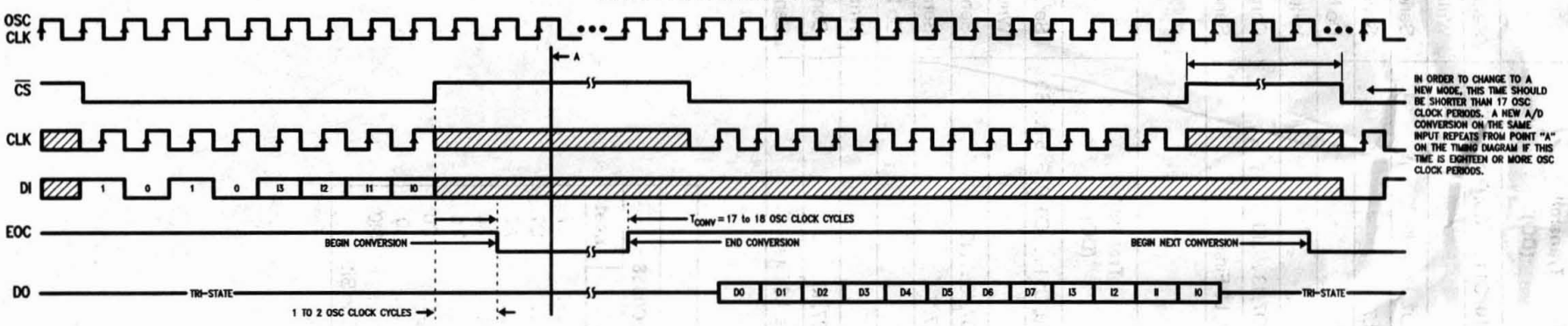
Read all Limits from ADC0851/ADC0858



TL/H/11021–19

Timing Diagrams for ADC0851 and ADC0858 (Continued)

1 A/D Conversion ADC0851/ADC0858


OSC CLK
A
CS
CLK
DI
1 0 1 0 I3 I2 I1 I0
EOC
DO
TRI-STATE
1 TO 2 OSC CLOCK CYCLES
BEGIN CONVERSION
T_{CONV} = 17 to 18 OSC CLOCK CYCLES
END CONVERSION
BEGIN NEXT CONVERSION
D0 D1 D2 D3 D4 D5 D6 D7 I3 I2 I1 I0
TRI-STATE
IN ORDER TO CHANGE TO A NEW MODE, THIS TIME SHOULD BE SHORTER THAN 17 OSC CLOCK PERIODS. A NEW A/D CONVERSION ON THE SAME INPUT REPEATS FROM POINT "A" ON THE TIMING DIAGRAM IF THIS TIME IS EIGHTEEN OR MORE OSC CLOCK PERIODS.

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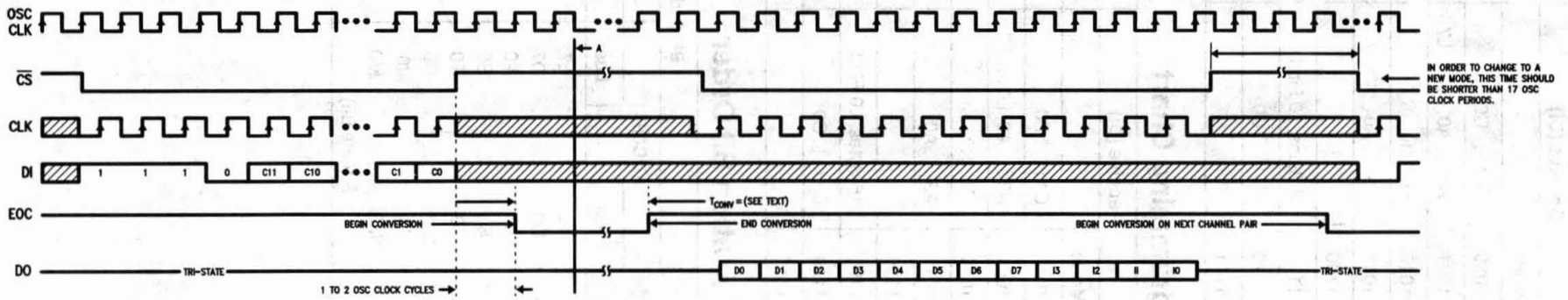
Auto A/D Conversion ADC0851/ADC0858


OSC CLK
A
CS
CLK
DI
1 1 1 0 C11 C10 C1 C0
EOC
DO
TRI-STATE
1 TO 2 OSC CLOCK CYCLES
BEGIN CONVERSION
T_{CONV} = (SEE TEXT)
END CONVERSION
BEGIN CONVERSION ON NEXT CHANNEL PAIR
D0 D1 D2 D3 D4 D5 D6 D7 I3 I2 I1 I0
TRI-STATE
IN ORDER TO CHANGE TO A NEW MODE, THIS TIME SHOULD BE SHORTER THAN 17 OSC CLOCK PERIODS.

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ADC0851 Programming Chart

Function	Receive (DI)		Transmit (DO)	Comments
	Mode			
Watchdog	1000	C11 . . . C0	T3 . . . T0, C11 . . . C0, P, S3 . . . S0	Send Data after $\overline{INT}$
Write 1 Limit	1001	A3 . . . A0, L0 . . . L7		Write Limit to RAM
1 A/D Conversion	1010	I3 . . . I0	D0 . . . D7, I3 . . . I0	Send Data after Conversion
Read 1 Limit	1011	A3 . . . A0	L0 . . . L7	Send Limit from RAM
Test	1100			Do Not Use (See Text)
Write all Limits	1101	4 Bytes, L0 First		Write All Limits to RAM
Auto A/D Convert	1110	C11 . . . C0	D0 . . . D7, I3 . . . I0	Continuous Conversion
Read all Limits	1111		4 Bytes, L0 First	Send all Limits from RAM

ADC0858 Programming Chart

Function	Receive (DI)		Transmit (DO)	Comments
	Mode			
Watchdog	1000	C11 . . . C0	T3 . . . T0, C11 . . . C0, P, S15 . . . S0	Send Data after $\overline{INT}$
Write 1 Limit	1001	A3 . . . A0, L0 . . . L7		Write Limit to RAM
1 A/D Conversion	1010	I3 . . . I0	D0 . . . D7, I3 . . . I0	Send Data after Conversion
Read 1 Limit	1011	A3 . . . A0	L0 . . . L7	Send Limit from RAM
Test	1100			Do Not Use (See Text)
Write all Limits	1101	16 Bytes, L0 First		Write all Limits to RAM
Auto A/D Convert	1110	C11 . . . C0	D0 . . . D7, I3 . . . I0	Continuous Conversion
Read all Limits	1111		16 Bytes, L0 First	Send all Limits from RAM

Serial Communication Bit Order

Information Type	Bit Order					
	ADC0851			ADC0858		
	First		Last	First		Last
Limit Data	L0	. . .	L7	L0	. . .	L7
A/D Conversion Data	D0	. . .	D7	D0	. . .	D7
Limit Address	A3	. . .	A0	A3	. . .	A0
Status	S3	. . .	S0	S15	. . .	S0
Channel Tag	T3	. . .	T0	T3	. . .	T0
Channel Configuration	C11	. . .	C0	C11	. . .	C0
Channel Information	I3	. . .	I0	I3	. . .	I0
Mode	M3	. . .	M0	M3	. . .	M0
Power Fail	P (One Bit)			P (One Bit)		

Pin Descriptions

V_{CC} Positive power supply pin. Bypass to analog ground with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

OSC Input/Output pin used to generate internal timing for A/D conversion. This pin is connected to an external resistor and capacitor to set the oscillation frequency for analog timing (see *Figure 12*).

$\overline{CS}$ This is the chip select input pin. It must be held low while data is transferred to or from the ADC0851/8 (see Timing Diagram).

CLK The serial clock input pin is used to clock serial data either into the data input pin (DI) or out of the data output pin (DO). Input data is loaded on the rising edge of CLK and the output data is valid at the falling edge of CLK.

DI Serial data digital input pin.

DO TRI-STATE data output pin.

$\overline{INT}$ This is the active low interrupt pin that indicates that at least one analog input channel voltage level has exceeded the programmed window limits. Since this pin has an open drain output, an external pull up resistor is required. This allows many devices to be wire-ORed together using a single pull-up resistor.

EOC End of conversion output pin. The low state indicates that an A/D conversion is in progress. The EOC pin goes high when the conversion is completed.

AGND Analog ground reference.

DGND Digital ground reference for the logic inputs. Both AGND and DGND should be at same potential.

V_{REF} This is the analog reference pin. The voltage applied to this pin sets the full scale A/D conversion range. Recommended voltages applied to this pin range from 1V to V_{CC}. Bypass to analog ground with a 0.1 μF ceramic capacitor in parallel with a 10μF tantalum capacitor.

COM The COM pin functions as an inverting differential input common to all analog inputs when each channel is configured as a single-ended channel. If the input channels are programmed as differential pairs then the COM input has no effect.

CH0–CH1 (ADC0851)
CH0–CH7 (ADC0858) CH0–CH7 are analog input channels which can be configured as single ended inputs or as differential pairs. The analog input voltage should stay within the power supply range.

COMPL, COMPH These output pins are available only on the ADC0851. During "Watchdog" operation, if either of the inputs exceeds the window limits, not only is an interrupt generated but also the COMPL and COMPH pins go low to indicate whether the upper or lower boundary was exceeded (See applications section for more information.)

General Overview

The ADC0851/58 is a versatile microprocessor-compatible data acquisition system with an on-board watchdog capability. The device is capable of synchronous serial interface with most microprocessors and includes a multiplexer, a RAM and a successive approximation register. The ADC0851 and the ADC0858 have two and eight input channels respectively.

1.0 Modes of Operation

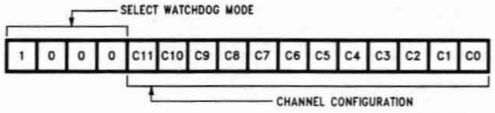
The device can be used in any one of the eight modes of operation listed below. A mode is selected by taking $\overline{CS}$ low and providing the IC with an input word whose first four bits specify the desired mode (see the "Programming Charts" for the mode selection codes):

1.1 WATCHDOG MODE

This mode of operation allows the device to operate as a digitally-programmable window comparator. The analog input voltage at each channel is compared against the upper and lower boundary limits stored in an internal RAM. When an input falls outside of its programmed window limits, an interrupt is generated. The microprocessor can then pull $\overline{CS}$ low which causes the device to produce a bit stream that indicates which channel(s) crossed which limit(s).

The watchdog mode is selected by taking $\overline{CS}$ low and shifting in the four bit word (1 0 0 0) followed by a twelve bit word that configures the analog inputs to operate either as single-ended or as differential pairs (CH0–CH1, CH2–CH3, etc.). When a channel is operating single-ended, its input voltage is compared to the upper and lower limits stored in RAM for that input. When two inputs are configured as a differential pair, the limits stored in the RAM for the channel with the lower number will be compared against the differential input voltage. For example, the differential voltage CH0–CH1 will be compared with the lower and upper limits for CH0. The limits are programmed using the "write one limit to RAM" or "write all limits to RAM" mode.

Data Input (DI) Word—ADC0851 or ADC0858



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1.2 WRITE ONE LIMIT TO RAM

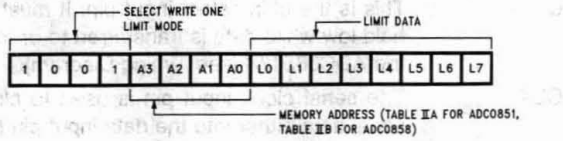
This mode allows the user to update a single limit for one of the input channels. This is accomplished by using a 16-bit stream of input data (see "Programming Chart"). The first four bits (1 0 0 1) select the mode, the next four bits select the input channel and the limit (upper or lower) that will be preset, and the last eight bits set the limit (or comparator threshold).

The limit data representing the input voltage limit (or comparator threshold) is expressed as per the following equation:

$$V_{LIM} = V_{REF} (1/2\ L7 + 1/4\ L6 + \ldots + 1/256\ L0)$$

where L7 is the MSB.

Data Input (DI) Word—ADC0851 or ADC0858


SELECT WRITE ONE LIMIT MODE
LIMIT DATA
1 0 0 1 A3 A2 A1 A0 L0 L1 L2 L3 L4 L5 L6 L7
MEMORY ADDRESS (TABLE IIA FOR ADC0851, TABLE IIB FOR ADC0858)

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1.3 WRITE ALL LIMITS TO RAM

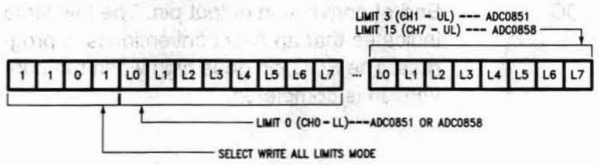
This mode is used to update each pair of lower and upper limits for all channels. This is accomplished by a stream of input data whose first four bits select the mode of operation followed by four bytes of limit data for the ADC0851 and sixteen bytes of limit data for the ADC0858.

The limit data representing the input voltage limit (or comparator threshold) is expressed as per the following equation:

$$V_{LIM} = V_{REF} (1/2\ L7 + 1/4\ L6 + \ldots + 1/256\ L0)$$

where L7 is the MSB.

Data Input (DI) Word—ADC0851 or ADC0858


LIMIT 3 (CH1 – UL) --- ADC0851
LIMIT 15 (CH7 – UL) --- ADC0858
1 1 0 1 L0 L1 L2 L3 L4 L5 L6 L7 ... L0 L1 L2 L3 L4 L5 L6 L7
LIMIT 0 (CH0 – LL)---ADC0851 OR ADC0858
SELECT WRITE ALL LIMITS MODE

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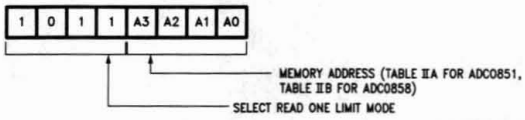
1.4 READ ONE LIMIT FROM RAM

When the ADC0851/8 is configured in this mode, the user can read back an 8-bit limit word from the RAM memory location pointed to by the limit address. An 8-bit input word selects the mode (1 0 1 1) and the memory location to be read.

Data Input (DI)—ADC0851 or ADC0858



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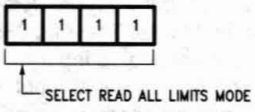
1.0 Modes of Operation (Continued)

1.5 READ ALL LIMITS FROM RAM

This mode of operation allows the device to serially output 8-bit limit data from each memory location in succession starting with CH0-lower limit (see Section 2.4 under interface considerations).

Data Input (DI) Word—ADC0851 or ADC0858



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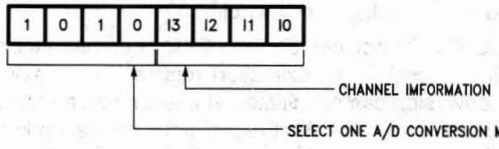
1.6 INITIATE ONE A/D CONVERSION

At any time, the user can initiate an A/D conversion on any input channel. Note that the input channels may be configured as single ended or differential inputs. The first four bits of the input word select the mode of operation and the next four bits assign the multiplexer configuration.

Data Input (DI) Word—ADC0851 or ADC0858



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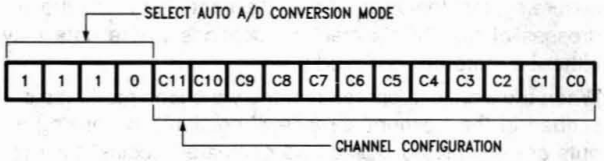
1.7 INITIATE AUTO A/D CONVERSION

When configured in this mode, an A/D conversion is done on a channel or channel pair and after the output data is transmitted, conversion begins on the next subsequent channel or channel pair. In this mode the device continually scans through the input channels making A/D conversions unless the device's mode of operation is changed. The first four bits of the input word select the mode of operation and the next twelve bits assign the multiplexer configuration.

Data Input (DI) Word—ADC0851 or ADC0858



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1.8 TEST MODE

This mode is used to test the ADC0851/8 at the factory and is **not** intended for normal use. If this mode is accidentally selected, the supply voltage must be disconnected and then reconnected to reset the device.

2.0 Conversion Timing vs Serial Interface Timing

Note that the ADC0851/8 uses two clock signals for proper operation. Connecting an external resister (R_{ext}) from the OSC pin (pin 2) to V_{CC} and an external capacitor (C_{ext}) from the OSC pin to ground causes the device's internal oscillator to generate the OSC clock signal for A/D conversion and watchdog timing. With R_{ext} = 3.16 kΩ and C_{ext} = 170 pF, the OSC clock frequency is approximately 1 MHz. Note that internally, ADC0851/8 divides the OSC clock frequency by two. An A/D conversion is completed in eighteen OSC clock periods maximum. It should be noted that the OSC pin of the ADC0851/8 should not be driven by an external clock.

An external clock signal is applied to the CLK pin (pin 4) of the ADC0851/8. The CLK signal is used to clock serial data either into the data input pin (DI) or out of the data output pin (DO).

Note that input data is loaded at the rising edge of CLK while the output data is valid at the falling edge of CLK. All digital timing such as data set-up and hold times and delays are measured with respect to the CLK signal. The OSC clock and CLK frequencies need not be the same.

3.0 Programming Information

The ADC0851 and ADC0858 communicate data serially over the DI (data input) and DO (data output) lines. The data format for the input and output words for various modes of operation are shown in the "programming charts."

There are nine types of data as shown in the "serial communication bit order" table. The order in which data is communicated is MSB first in all but two cases: Limit data and A/D conversion data. The various data types are described below.

3.1 LIMIT DATA (L0, L1, . . . L7)

Limits on the ADC0851/8 are 8 bits in width and can either represent an upper or lower boundary limit. Limit data can either be written (in the "write one limit" or "write all limits" mode) to or read (in the "read one limit" or "read all limits" mode) from the limit RAM. Being able to read back the limit data allows system testability, and it also allows independent software routines to see what window limits were previously written to the chip. During watchdog operation, a programmed limit must be crossed in order to cause an interrupt.

3.2 A/D CONVERSION DATA (D0, D1, . . . D7)

There are two A/D conversion modes (One A/D conversion and Auto A/D conversion) that produce 8-bit conversion data. During either type of A/D conversion, a single-ended analog input or a differential analog input pair is digitized to produce this conversion data.

3.3 LIMIT ADDRESS (A3, A2, . . . A0)

The limit address points to the location, within the limit RAM, to which limit data is sent or from which it is received. Limit address is used in the "write one limit to RAM", "write all limits to RAM", "read one limit from RAM" or "read all limits from RAM" mode. There are two addresses for each analog input; the even addresses correspond to the lower

3.0 Programming Information

(Continued)

limits while the odd addresses correspond to the upper limits. The ADC0851 and ADC0858 both use four bits (A3–A0) to address the limit RAM but the ADC0851 only decodes the two LSBs while ignoring the two MSBs. The ADC0858 decodes all four bits thus yielding sixteen limit addresses.

3.4 STATUS AND CHANNEL TAG DATA (S3, S2, . . . , S0, ADC0851; S15, S14, . . . , S0, ADC0858) (T3, T2, . . . , T0)

During watchdog mode, immediately after one analog input is determined to be outside of its programmed window limit, its channel number is stored in the channel tag register and the remaining inputs are checked one more time and the pass/fail status of each input is stored in the status register. When the microprocessor receives the interrupt signal, it can read the status and channel tag data by pulling $\overline{CS}$ low and clocking out the data.

3.5 CHANNEL CONFIGURATION DATA (C11, C10, . . . C0)

The channel configuration data assigns the configuration of the multiplexer. The data is comprised of twelve bits with each group of three bits addressing an analog input channel pair. Each channel pair can be configured for single-ended operation, differential operation, one single ended channel and one disabled channel, or both channels disabled. The channel configuration data is required when the device is in the watchdog or Auto A/D conversion mode.

3.6 CHANNEL INFORMATION DATA (I3, I2, . . . I0)

This data is used by the ADC0851/8 only when the device is configured in the "One A/D conversion" mode. The channel information data assigns the configuration of the multiplexer.

3.7 MODE ADDRESS (M3, M2, . . . M0)

The input word (DI) configures the ADC0851/8 for various modes of operation. The first four bits of the input word constitute the mode address which specifies the mode of operation.

3.8 POWER FAIL BIT (P)

The ADC0851/8 is automatically configured to the watchdog mode upon power-up and an interrupt is immediately generated after $\overline{CS}$ is pulled high. Pulling $\overline{CS}$ low produces a 17-bit data stream. The seventeenth bit of the output word DO in the watchdog mode is the power fail bit, P. If the output data is read after power-up then P will be at logical "1". Changing the mode of operation resets P to logical "0". Any subsequent power failure will cause the device to configure in the watchdog mode upon power-up with P at logical "1".

4.0 Initialization after Power-Up

The ADC0851/8 is automatically configured in the watchdog mode upon power-up. After reading the power fail bit $\overline{CS}$ is pulled high. To exit the watchdog mode and to change to a new mode of operation, $\overline{CS}$ should be high less than eight oscillator clock periods for the ADC0851 and less than thirty two oscillator clock periods for the ADC0858 respectively (see the Timing Diagram, "Read Power Flag after Power Up ADC0851/8"). When changing to a new mode of operation, the device readies itself to read a new input word clocked in at the data input (DI) pin. The input word configures the new mode of operation.

Functional Description

The simplified block diagram (*Figure 1*, front page) shows the various functional blocks. The ADC0851 and ADC0858 include 2- and 8-channel analog input multiplexers respectively. Using the appropriate serial input word at the Data Input (DI) pin, the analog channels can be configured for either single-ended operation or differential mode operation. The COM input pin provides additional flexibility since the COM pin functions as an inverting differential input common to all analog inputs when each channel is configured as a single ended channel. Applying an external DC voltage at the COM pin allows offsetting the single ended analog input voltages from ground (pseudo-differential mode). Input channels that are configured as differential pairs will be unaffected by the voltage at COM pin.

The ADC0851/8 includes an 8-bit DAC, a comparator and an 8-bit successive approximation register. An analog-to-digital conversion can be initiated at any time on any one of the input channels. The 8-bit digital word corresponding to the analog input voltage is serially clocked out at the Data Output (DO) pin. In addition to its use as a multiplexed A/D converter, the ADC0851/8 may also be used as a window comparator in the watchdog mode. An upper and lower boundary limit corresponding to each analog input voltage may be stored in an internal RAM. The RAM consists of sixteen memory locations, each 8 bit wide; however, for the ADC0851 only four memory locations are used. Limit data can either be written into or read back from the RAM. The read/write capability allows independent software routines to read back previously programmed window limits. Furthermore, currently programmed limits may also be read back to ensure system testability. An address register holds the addresses of the RAM's memory locations where data may either be stored or retrieved from.

When the device is operated in the watchdog mode (as described in the "general overview" section), the analog inputs are continually polled and compared against their respective window limits. Once an input signal that has exceeded either boundary limit is detected, a "1" is stored in the MSB position in a 16-bit status register, indicating a limit crossing. Note that the ADC0851 uses only four locations of the status register because it has only four limits. In addition, the tag register is updated so that the register holds the address which indicates the channel and the corresponding upper or lower limit that was crossed. After the first limit crossing is detected, the device cycles through the remaining limits and compares them against their respective input signals. If any additional limit crossing is or are detected then a "1" is stored in the appropriate locations of the status register. After the completion of this operation, the interrupt pin ($\overline{INT}$) goes low, providing a flag to a microprocessor. The microprocessor can then cause the serial status data to be shifted out by bringing the $\overline{CS}$ line low. Together with the status and tag bits, the microprocessor can determine which channel exceeded which limit. If desired the mi-

Functional Description (Continued)

croprocessor can then initiate an A/D conversion on any channel(s). The ADC0851 includes two additional output pins, COMPL and COMPH. During watchdog operation, if either of the inputs exceeds its respective window bounds then not only is an interrupt generated but a logic low at COMPL or COMPH indicates whether the lower or upper boundary was crossed.

A mode register within the ADC0851/8 allows the device to be used in any one of the eight modes of operation as described in the "general overview" section.

The features described make the ADC0851/8 ideal for use in microprocessor-based automotive, instrumentation and control applications. Such applications often require monitoring of various transducer signals and comparison against pre-programmed window limits. With its watchdog operation, the ADC0851/8 frees up the microprocessor from having to continually monitor the analog variables; the microprocessor is interrupted only when the input signal crosses the preset bounds. Furthermore, the window limits can easily be changed with simple software control.

Applications Information

I. Digital Interface Considerations

The ADC0851 and ADC0858 communicate data serially over the DI (Data Input) and DO (Data Output) pins. The data transfer is synchronous with the external clock (CLK) signal and is clocked in or out of the device at the rising edge of clock. Note that although the output data is clocked out starting at the rising edge of CLK, the data is valid at the falling edge of CLK.

All internal timing in the device is with respect to the oscillator clock. The oscillator frequency is set by connecting a resistor from the OSC pin (pin 2 for ADC0851 or ADC0858) to V_{CC} and a capacitor from the OSC pin to ground. The period of the oscillator clock will determine the A/D conversion time and chip select ($\overline{CS}$) high duration as will be discussed in the following sections.

1.0 Modes of Operation

To initiate the operation of the device in any one of the eight modes, the chip select ($\overline{CS}$) line must go low. After a $\overline{CS}$ low is detected, serial input data at the DI pin is clocked in starting at the first rising edge of the serial clock. The first four bits of the input word are reserved for specifying the mode of operation, with the first bit of the input word always being a logic "1". Table I shows the mode addresses for selecting the different modes of operation.

TABLE I. Modes of Operation

Mode Address				Mode
M3	M2	M1	M0	
1	0	0	0	Watchdog
1	0	0	1	Write One Limit
1	0	1	0	One A/D Conversion
1	0	1	1	Read One Limit
1	1	0	0	Test (for Factory Use Only)
1	1	0	1	Write All Limits
1	1	1	0	Auto A/D Conversion
1	1	1	1	Read All Limits

1.1 POWER FAILURE DETECTION/ INITIALIZATION AFTER POWER-UP

Upon power up, the device is automatically configured in the watchdog mode. The status of the power flag bit, P, provides power failure indication to the microprocessor. The timing diagram of *Figure 2* shows the sequence of events.

First consider the case of initial power up. After power is applied, $\overline{CS}$ should be brought high. Bringing $\overline{CS}$ high causes the $\overline{INT}$ pin to go low, which signals the microprocessor that a failure has occurred. The microprocessor can then interrogate the device as to the type of failure by bringing $\overline{CS}$ low. When $\overline{CS}$ goes low, it resets the $\overline{INT}$ pin to high and the output data is read starting at the first rising edge of clock (CLK) after $\overline{CS}$ has gone low. Since this is the first read cycle after power up, the power flag bit, P, is set high and appears at the rising edge of the seventeenth clock cycle after $\overline{CS}$ low is detected *(Figure 2)*. After the power flag is read by the microprocessor, $\overline{CS}$ is taken high. Note that the duration for which $\overline{CS}$ remains high (after the power flag is read) must be less than eight oscillator clock periods for ADC0851 and less than thirty-two oscillator clock periods for ADC0858. This is required to interrupt the device from watchdog mode so that when $\overline{CS}$ goes low, the device reads a valid data input (DI) word and configures to a new mode.

During normal operation, the power flag bit is reset to zero after the first "read" cycle and will be updated to a "1" only if a power interruption occurs.

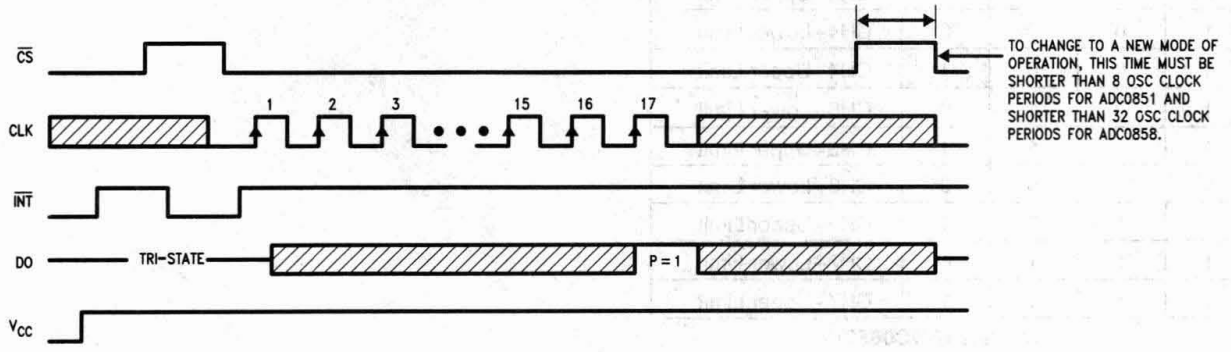

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FIGURE 2. Read Power Flag after Power Up ADC0851/ADC0858

2.0 Memory Access Modes

The ADC0851/8 has an internal RAM with sixteen memory locations (one location for the upper limit and one for the lower limit for each of the 8 input channels). Each memory location is 8 bits wide. An 8-bit limit word representing an upper or lower limit boundary can either be written to or read from the RAM. The ADC0851 uses only four memory locations for the four boundary limits corresponding to the two inputs. The eight channel ADC0858, however, makes use of all sixteen memory locations.

Each memory location is accessed by a specific address as shown by Table II(a) and (b). Note that even addresses correspond to the lower limits while the odd addresses correspond to the upper limits. The ADC0851 and ADC0858 both use 4 bits (A3, ... A0) to address the RAM, however, ADC0851 decodes only the two LSBs of the address data while ignoring the two MSBs.

TABLE IIa. RAM Address and Limit Data for ADC0851

RAM Address				Corresponding Channel and Limit
A3	A2	A1	A0	
X	X	0	0	CH0–Lower Limit
X	X	0	1	CH0–Upper Limit
X	X	1	0	CH1–Lower Limit
X	X	1	1	CH1–Upper Limit

Limit Data (ADC0851)

L0	L1	L2	L3	L4	L5	L6	L7

TABLE IIb. RAM Address and Limit Data for ADC0858

RAM Address				Corresponding Channel and Limit
A3	A2	A1	A0	
0	0	0	0	CH0–Lower Limit
0	0	0	1	CH0–Upper Limit
0	0	1	0	CH1–Lower Limit
0	0	1	1	CH1–Upper Limit
0	1	0	0	CH2–Lower Limit
0	1	0	1	CH2–Upper Limit
0	1	1	0	CH3–Lower Limit
0	1	1	1	CH3–Upper Limit
1	0	0	0	CH4–Lower Limit
1	0	0	1	CH4–Upper Limit
1	0	1	0	CH5–Lower Limit
1	0	1	1	CH5–Upper Limit
1	1	0	0	CH6–Lower Limit
1	1	0	1	CH6–Upper Limit
1	1	1	0	CH7–Lower Limit
1	1	1	1	CH7–Upper Limit

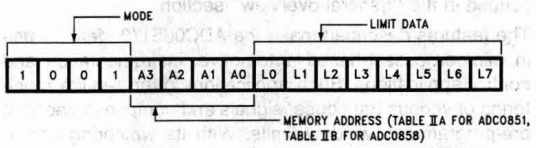
Limit Data (ADC0858)

L0	L1	L2	L3	L4	L5	L6	L7

2.1 WRITE ONE LIMIT

This mode is used to update a single memory location in the limit RAM. An 8-bit limit word is written to the location pointed to by the limit address. From Table I we can see that to initiate the operation of the device in the "write one limit" mode, the mode address has to be 1 0 0 1. The data format for the input word is as shown below.

Data Input (DI) Word—ADC0851 or ADC0858



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2.0 Memory Access Modes (Continued)

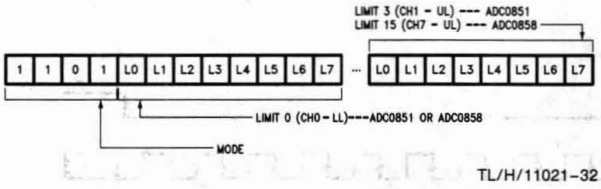
Note that the memory address is clocked in with the MSB (bit A3) first whereas the limit data is clocked in with the LSB (bit L0) first.

Figure 3 shows the timing diagram for writing one limit. After $\overline{CS}$ is brought low, the input word (DI) is clocked in starting at the first rising edge of CLK. Taking $\overline{CS}$ high after the MSB (bit L7) of the limit data is loaded completes the write operation.

2.2 WRITE ALL LIMITS MODE

This mode is used to update all memory locations in the limit RAM. An 8-bit limit word is written to each memory location. Note that there are four limit words for the ADC0851 and sixteen limit words for the ADC0858. To initiate the operation of the device in the "write all limits" mode, the mode address has to be 1 1 0 1 (see Table I). The data format for the input word is as shown below.

Data Input (DI) Word—ADC0851 or ADC0858


LIMIT 3 (CH1 − UL) --- ADC0851
LIMIT 15 (CH7 − UL) --- ADC0858
1 1 0 1 L0 L1 L2 L3 L4 L5 L6 L7 ... L0 L1 L2 L3 L4 L5 L6 L7
LIMIT 0 (CH0 − LL)---ADC0851 OR ADC0858
MODE

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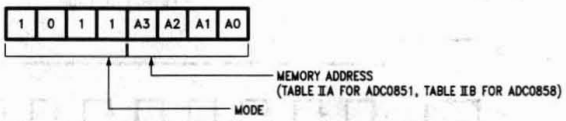
When writing all limits, memory address is not required. The limit data is sequentially written into the RAM starting at the location for CH0–Lower Limit and ending at; CH1–Upper Limit for the ADC0851 (see Table IIa), CH7–Upper Limit for ADC0858 (see Table IIb). Note that L0 corresponds to the LSB of the limit data.

Figure 4 shows the timing diagram. After $\overline{CS}$ is brought low, the input word (DI) is clocked in starting at the first rising edge of CLK. The first four bits of D1 configure the device in the "write all limits" mode. Next, the limit data is serially clocked in. To complete the operation, $\overline{CS}$ should be brought high after the data is loaded.

2.3 READ ONE LIMIT MODE

When the mode address is 1 0 1 1, the device is configured in the "read one limit" mode. One 8-bit limit word can be read from the RAM memory location pointed to by the limit address. The data format for the input word is as shown below.

Data Input (DI)—ADC0851 or ADC0858



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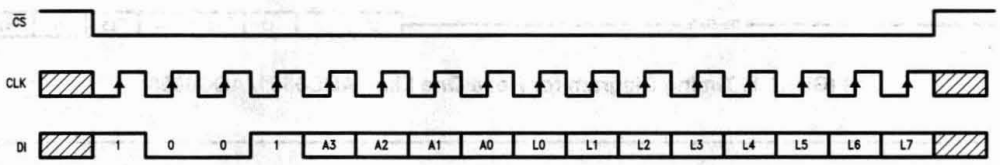

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FIGURE 3. Timing Diagram for Write One Limit

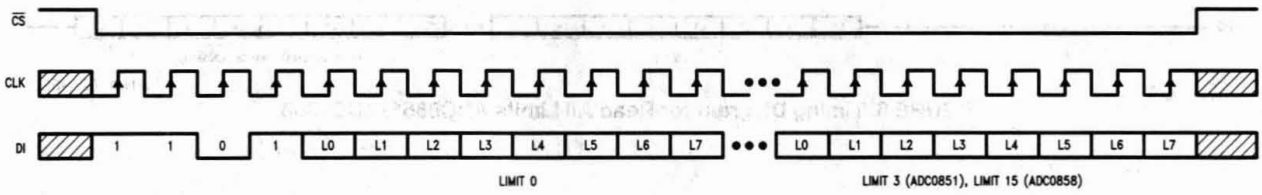

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FIGURE 4. Timing Diagram for Write All Limits

2.0 Memory Access Modes (Continued)

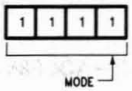
The address bits access specific memory locations as per Table II(a) and (b) for the ADC0851 and ADC0858 respectively. The address data is clocked in with the MSB (bit A3) first.

The timing diagram in *Figure 5* shows that after $\overline{CS}$ goes low, the first four bits of the input word configure the device to "read one limit" mode. Next, the address bits select the desired memory location. Third clock rising edge after the address data's LSB is loaded, the limit data is output with the LSB (bit L0) first.

2.4 READ ALL LIMITS MODE

With a mode address of 1 1 1 1, the device is configured in the "read all limits mode". When in this mode, 8-bit limit data from each memory location is serially transmitted out. The data format for the input word is as follows:

Data Input (DI) Word—ADC0851 or ADC0858



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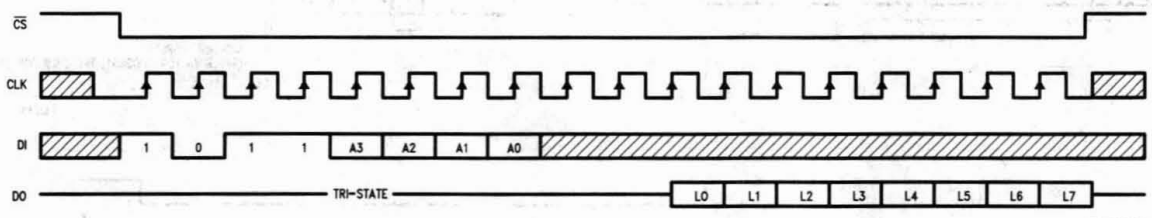

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FIGURE 5. Timing Diagram for Read One Limit ADC0851/ADC0858

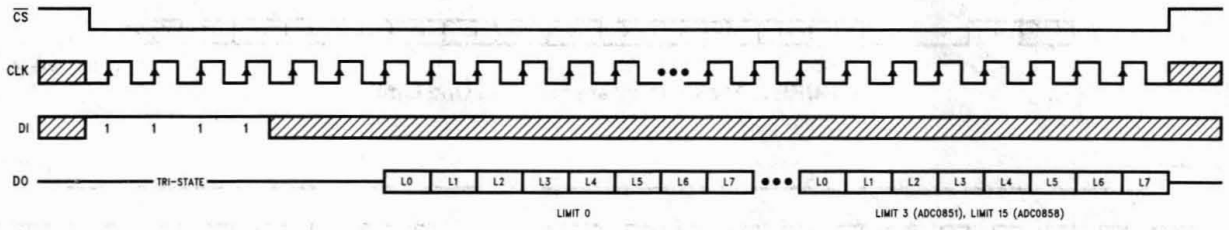

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FIGURE 6. Timing Diagram for Read All Limits ADC0851/ADC0858

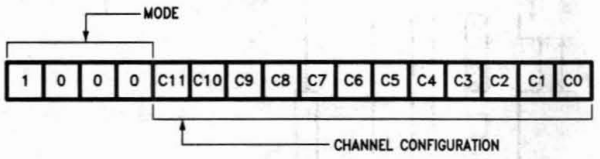
Note that no memory address data is required. The limit data is sequentially transmitted out starting from the memory location for CH0–Lower Limit and ending at; CH1–Upper Limit for the ADC0851 (see Table II(a)), CH7–Upper Limit for the ADC0858 (see Table II(b)).

The timing diagram of *Figure 6* shows that the input data is loaded starting at the first rising edge of CLK after $\overline{CS}$ goes low. Third clock rising edge after the last bit of the input data is loaded, the limit data is serially transmitted out. Four limit words are transmitted for the ADC0851; sixteen for the ADC0858. Each limit word is output with the LSB (bit L0) first. Taking $\overline{CS}$ high after the MSB of the last limit data is transmitted completes the operation.

3.0 Watchdog Mode

This is the primary real time operating mode. During watchdog operation, the upper and lower limits stored in the RAM are applied sequentially to the DAC's digital inputs. The DAC's analog output is applied to the comparator input and compared against the voltage at the enabled analog input pin. The data format for the input word is as shown below.

Data Input (DI) Word—ADC0851 or ADC0858



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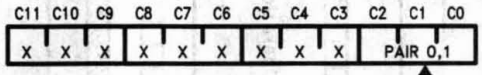
The last twelve bits of the input word assign the multiplexer channel configuration.

3.1 SELECTING THE CHANNEL CONFIGURATION

When the device is either in the watchdog or automatic A/D conversion mode, each pair of analog input channels must be programmed to determine which channel(s) will be active, and whether they will be operating single-ended or differentially. Table III(a) and (b) show the channel addresses for the ADC0851 and the ADC0858 in various channel configurations. When the channels are configured as single-ended inputs, the input voltages are measured with respect to the voltage at the COM pin. Applying a DC voltage at the COM pin will cause the device to measure the difference between the input signal and the voltage at the COM pin. The voltage at the COM pin has no effect on an input channel that is configured as a differential pair. When the channel pairs are configured as differential inputs (i.e., CH0–CH1, CH2–CH3, etc.) the differential voltage is compared with the limits for the lower numbered channel. For example, the differential voltage CH0–CH1 will be compared with the limits for CH0. Note that the channel pairs are programmed in groups of three bits. The channel address is input to the A/D converter with the MSB (bit C11) first.

The timing diagrams for ADC0851 and ADC0858 watchdog operation are shown in *Figure 7*. After a $\overline{CS}$ low is detected, the input word (DI) is clocked in starting at the first rising edge of the serial clock (CLK). Once the least significant bit of the channel address is loaded, $\overline{CS}$ should go high. Taking $\overline{CS}$ high after the proper input word is loaded initiates the operation of the device in the watchdog mode. To keep the device in continuous watchdog mode, $\overline{CS}$ should remain high for eight or more OSC clock periods for the ADC0851 and thirty-three or more OSC clock periods for the ADC0858. If the input signals are within the boundary limits, the interrupt pin (INT) remains at logic "1" and the Data Ouptut (DO) pin is in TRI-STATE. In addition, in the case of the ADC0851, the COMPL and COMPH pins remain at logic "1".

TABLE IIIa. Multiplexer Channel Configuration (ADC0851)



CHANNEL ADDRESS			CHANNEL CONFIGURATION			COMMENTS
C2	C1	C0	CH0	CH1	COM	
0	0	0	+	+	−	BOTH SINGLE-ENDED
1	0	0		+	−	CH1 ONLY
0	1	0	+		−	CH0 ONLY
1	1	0	+	−		DIFFERENTIAL CH0–CH1
X	X	1				CH0 AND CH1 DISABLED

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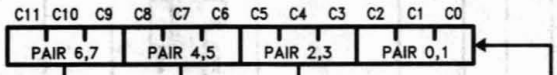
TABLE IIIb. Multiplexer Channel Configuration (ADC0858)



SUBSTITUTE CHANNELS 6 AND 7 INTO TABLE

SUBSTITUTE CHANNELS 4 AND 5 INTO TABLE

SUBSTITUTE CHANNELS 2 AND 3 INTO TABLE

X = DON'T CARE

CHANNEL ADDRESS			CHANNEL CONFIGURATION			COMMENTS
C2	C1	C0	CH0	CH1	COM	
0	0	0	+	+	−	BOTH SINGLE-ENDED
1	0	0		+	−	CH1 ONLY
0	1	0	+		−	CH0 ONLY
1	1	0	+	−		DIFFERENTIAL CH0–CH1
X	X	1				CH0 AND CH1 DISABLED

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3.0 Watchdog Mode (Continued)

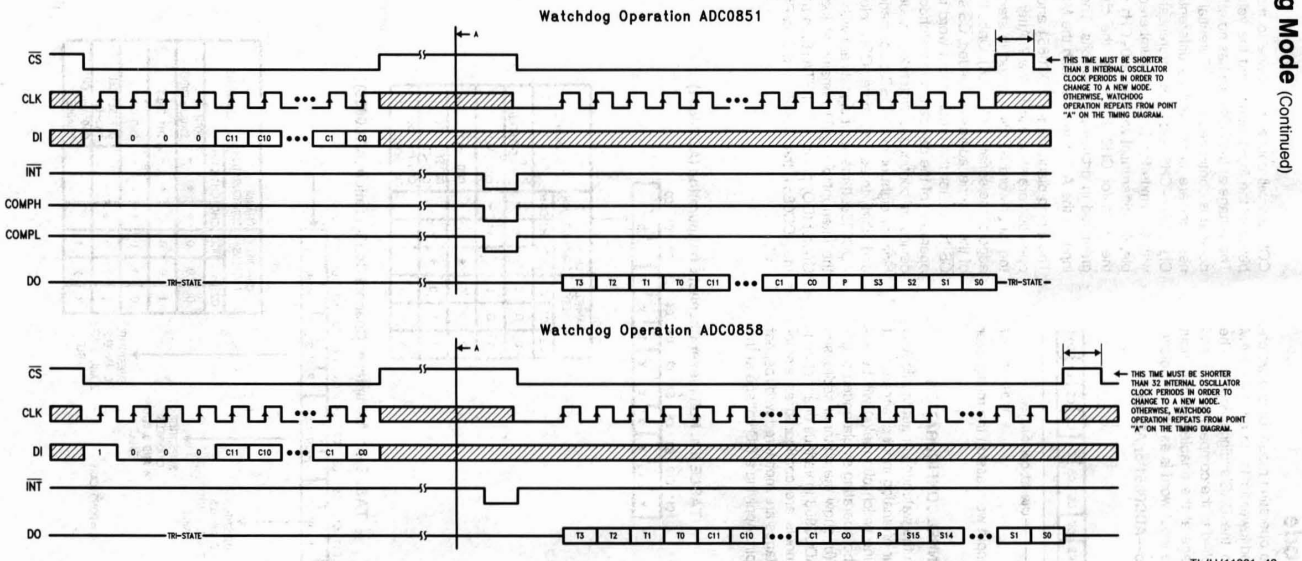
Watchdog Operation ADC0851
A
CS
CLK
DI
INT
COMPH
COMPL
DO
TRI-STATE
THIS TIME MUST BE SHORTER THAN 8 INTERNAL OSCILLATOR CLOCK PERIODS IN ORDER TO CHANGE TO A NEW MODE. OTHERWISE, WATCHDOG OPERATION REPEATS FROM POINT "A" ON THE TIMING DIAGRAM.
Watchdog Operation ADC0858
THIS TIME MUST BE SHORTER THAN 32 INTERNAL OSCILLATOR CLOCK PERIODS IN ORDER TO CHANGE TO A NEW MODE. OTHERWISE, WATCHDOG OPERATION REPEATS FROM POINT "A" ON THE TIMING DIAGRAM.
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FIGURE 7. Timing Diagrams for Watchdog Operation

3.0 Watchdog Mode (Continued)

The device will read the new input word and configure to a different mode if $\overline{CS}$ is high for less than eight oscillator clock periods for the ADC0851 and less than thirty-two oscillator clock periods for the ADC0858.

Once a boundary limit is crossed, $\overline{INT}$ goes low. Moreover, for ADC0851, COMPL goes low if a lower limit is crossed, whereas COMPH goes low if an upper limit is crossed. If the input signals exceed both the upper and lower boundary limits then both COMPL and COMPH would go low.

To output data after a limit crossing occurs (i.e., after $\overline{INT}$ goes low), $\overline{CS}$ should be brought low. Note that $\overline{INT}$, COMPL and COMPH would remain low as long as $\overline{CS}$ doesn't go low. After $\overline{CS}$ goes low $\overline{INT}$, COMPL and COMPH go high and one clock cycle later output data is transmitted starting at the first rising edge of CLK, however, the data is valid at the falling edge of CLK (*Figure 7*).

3.2 LIMIT CROSSING DETECTION

When the ADC0851/8 is configured in the watchdog mode, the device operates as a window comparator. First the lower window limit (stored in the RAM) for CH0 is compared against the input voltage at CH0. If the input voltage is greater than the lower limit, then no interrupt is generated. Next the upper window limit for CH0 is compared against CH0 input voltage. If the input voltage is less than the upper window limit then no interrupt is generated for CH0 and the device starts a similar comparison cycle for the next channel (CH1). Note that the lower limit can be greater than the upper limit; in this case the device will flag the microprocessor if the input signal falls inside a window.

TABLE IVa. Channel Tag Address and Status (ADC0851)

Tag #	Tag Address				Corresponding Limit and Channel
	T3	T2	T1	T0	
0	0	0	0	0	Lower Limit—CH0
1	0	0	0	1	Upper Limit—CH0
2	0	0	1	0	Lower Limit—CH1
3	0	0	1	1	Upper Limit—CH1

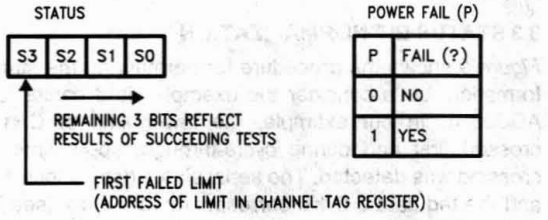

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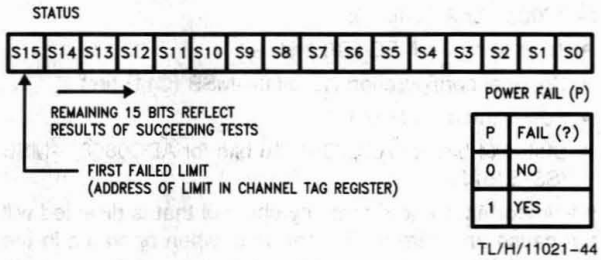
TABLE IVb. Channel Tag Address and Status (ADC0858)

Tag #	Tag Address				Corresponding Limit and Channel
	T3	T2	T1	T0	
0	0	0	0	0	Lower Limit—CH0
1	0	0	0	1	Upper Limit—CH0
2	0	0	1	0	Lower Limit—CH1
3	0	0	1	1	Upper Limit—CH1
4	0	1	0	0	Lower Limit—CH2
5	0	1	0	1	Upper Limit—CH2
6	0	1	1	0	Lower Limit—CH3
7	0	1	1	1	Upper Limit—CH3
8	1	0	0	0	Lower Limit—CH4
9	1	0	0	1	Upper Limit—CH4
10	1	0	1	0	Lower Limit—CH5
11	1	0	1	1	Upper Limit—CH5
12	1	1	0	0	Lower Limit—CH6
13	1	1	0	1	Upper Limit—CH6
14	1	1	1	0	Lower Limit—CH7
15	1	1	1	1	Upper Limit—CH7



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Each comparison takes 2 μs; thus a total of 4 μs is required per channel.

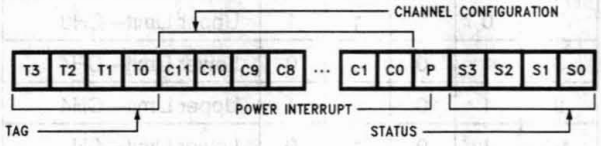
When in watchdog mode, the device will continuously cycle through the input channels until an input that has crossed its preset window limit is detected. When this occurs, a logical "1" is stored in the MSB (bit S3 for ADC0851 and S15 for ADC0858) position of the status register. In addition the tag register is updated with the channel's address (see Tables IV(a) and (b) for ADC0851 and ADC0858 respectively). Note that the tag address indicates which channel crossed which limit. Once the tag register is updated after the first limit is crossed, the device will once more cycle through the remaining channels and compare the input voltages against

3.0 Watchdog Mode (Continued)

their respective window limits. A logical "1" will be placed in the appropriate location of the status register for each limit that is crossed as the device cycles through the remaining channels. Note that the tag register is updated only once i.e., when the first limit is exceeded. After the last limit comparison is made subsequent to the first limit crossing, the device will cease any further limit comparisons and will cause the interrupt pin to go low. Taking $\overline{CS}$ low causes the data in the status and tag registers to be transmitted along with the programmed channel configuration information. In addition, an extra bit, P, is inserted between the channel and status information. This bit is updated to a logic "1" in case of a power interruption.

The format for the output data is as shown below.

Data Output (DO) Word—ADC0851



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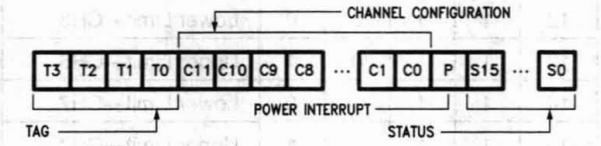
Data Output (DO) Word—ADC0858



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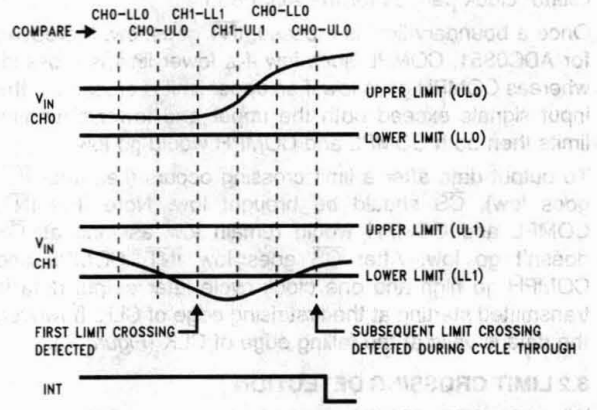
The order in which data is transmitted is as follows (ADC0851 or ADC0858):

- Tags (4 bits)—MSB (T3) first
- Channel configuration (12 bits)—MSB (C11) first
- Power interrupt (1 bit)
- Status (4 bits for ADC0851, 16 bits for ADC0858)—MSB (S3/S15) first

It is important to note that any channel that is disabled will not cause an interrupt. Furthermore, when operated in the differential mode, the arithmetic difference of the two voltages will be compared with the lower and upper limits for the lower numbered channel. For example, with CH0 and CH1 operating as a differential input pair, the CH0 limits will apply.

Consider an example where the lower limit of CH1 is crossed first and while the remaining limits are being checked, the upper limit of CH0 is crossed. *Figure 8* illustrates the sequence of events for the ADC0851. During watchdog operation, CH0's lower limit stored in the RAM is compared against the input voltage at CH0. Since no limit crossing is detected, the upper limit is compared against CH0 input voltage. Again no limit crossing is detected and so CH1's lower limit is next compared against the CH1 input voltage. This time a limit crossing is detected and a logic "1" is now stored in the MSB (S3) position of the status register (see Table IV(a)). Also the Tag register is updated with the corresponding address (0 0 1 0) from Table IV(a). The device now cycles through the remaining channels once more. Since no limit crossing is detected for the upper limit of CH1, a logic "0" is stored for S2 of the status register. Similarly a logic "0" is stored for S1 of the status register. Finally to complete the cycle, the last limit (upper limit of CH0) is checked and a limit crossing is detected. Consequently, a logic "1" is stored for S0. Note that the Tag register is only updated once when the first limit crossing is detected thus indicating which channel first exceeded its lower or upper limit.



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(Example: Lower limit of CH1 is crossed first. During cycle through, upper limit of CH0 is crossed)

FIGURE 8. Example of Limit Crossing Detection (ADC0851)

Assuming that there is no power interruption and that the ADC0851 was configured for single ended operation, the output word for our example would be:

(Example of ADC0851 Data Output. Single ended input. Lower limit of CH1 fails first. During cycle through, upper limit—CH0 failure is detected).

0	0	1	0	X	X	X	X	X	...	0	0	0	1	0	0	1
T3	T2	T1	T0	C11	C10	C9	C8	C7		C1	C0	P	S3	S2	S1	S0

X = Don't care, whatever bit was initially programmed (ADC0851 only).

The ADC0858 operates similar to the ADC0851 except that the ADC0858 has a 16-bit status word for the sixteen limits and sixteen tag addresses (See Table IV(b)). The output word transmitted to the microprocessor not only contains information as to how the channels are configured but also which input crossed which limit. If desired, the microprocessor can go through a status bit normalization routine to normalize the status information with the tag number as will be discussed next.

3.3 STATUS BIT NORMALIZATION

Figure 9 shows the procedure for normalizing the status information. Let's consider the example cited earlier for the ADC0851. In our example, the lower limit of CH1 was crossed first and during cycle-through, upper limit—CH0 crossing was detected. The serial status data is thus 1 0 0 1 and the tag data 0 0 1 0 corresponds to tag #2 (see Table IVa). Since the most significant bit (S3) of the status data is transmitted first, the data stored in the microprocessor's memory is 1 0 0 1. The microprocessor next computes the tag number from the tag data and rotates the status bits left "TAG" places as in *Figure 9*. For our example, the status bits are rotated by shifting left 2 places. The status information in the microprocessor's memory is now normalized i.e., U0 corresponds to tag 0, U1 corresponds to tag 1 and so on. From the example in *Figure 9* we can see that the status register in the microprocessor's memory shows that tag 2 and tag 1 failed. The ADC0858 uses a 16-bit status word and operates similar to the ADC0851. An example shown in *Figure 9* for the ADC0858 demonstrates how status bit normalization is carried out.

3.0 Watchdog Mode (Continued)

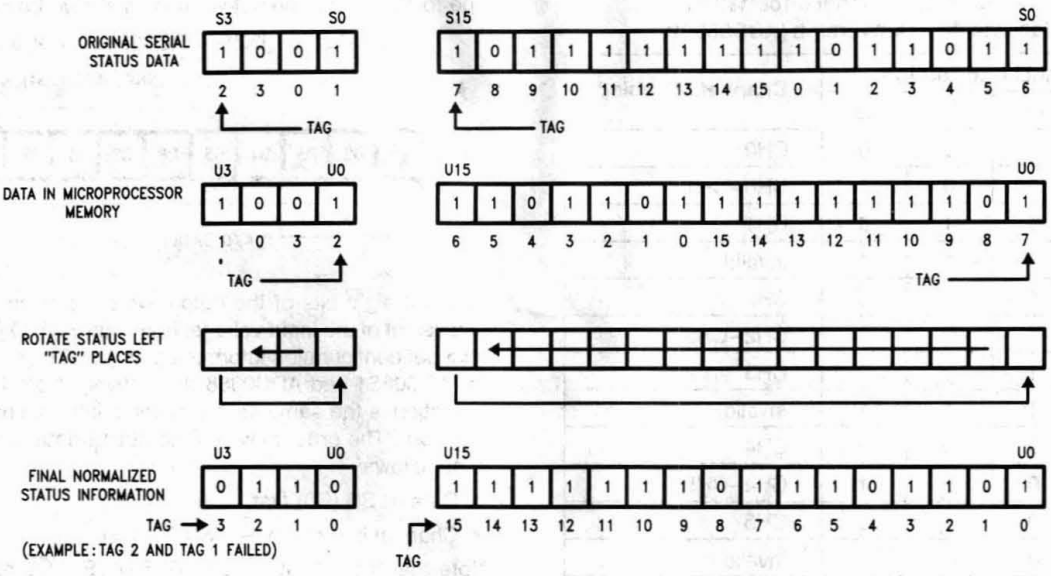

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FIGURE 9. Status Bit Normalization

4.0 A/D Conversion Modes

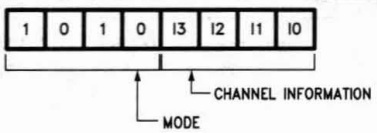
The ADC0851/8 can be used in two A/D conversion modes. In "One A/D conversion" mode, the device operates as a multiplexed A/D converter and a conversion may be initiated on any channel or channel pair configured in the differential mode. In the "Automatic A/D conversion" mode, an A/D conversion is done on a channel or channel pair and after the output data is transmitted, conversion begins on the next subsequent channel or channel pair. This process will continue unless the device's mode of operation is changed.

Note that the A/D conversion time is determined by the oscillator clock period and has no relation with the digital clock signal, CLK. The oscillator clock's frequency is set by connecting a resistor from the OSC pin (pin 2 for ADC0851 or ADC0858) to V_{CC} and a capacitor from the OSC pin to ground. The conversion time of the A/D converter is eighteen OSC clock periods maximum. Assuming that the oscillation clock frequency is set at 1 MHz (with R_{ext} = 3.16 kΩ and C_{ext} = 170 pF) then the conversion time would be 18 μs maximum.

4.1 ONE A/D CONVERSION MODE

This mode is used to initiate one A/D conversion on a single channel or channel pair configured in the differential mode. The necessary mode address as per Table I is 1 0 1 0. The format for the input word is as follows:

Data Input (DI) word—ADC0851 or ADC0858.



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(Table V(a) for ADC0851, Table V(b) for ADC0858)

The 4-bit data following the mode address is the channel information address. These four bits assign the MUX configuration for the single A/D conversion. The channel information addresses and the corresonding MUX configurations are shown in Table V(a) and (b) for ADC0851 and ADC0858 respectively. Note that the ADC0851 only decodes the two LSBs of the channel information data while ignoring the two MSBs (I3 and I2). When a channel pair is configured in the differential mode, it is important to note that the arithmetic difference of the channel voltages should not be negative. Negative difference voltage would result in all zeroes at the output.

TABLE V(a). Channel Information for One A/D Conversion (ADC0851)

Channel Information				Channels Enabled
I3	I2	I1	I0	
X	X	0	0	CH0
X	X	0	1	CH0–CH1
X	X	1	0	CH1
X	X	1	1	Invalid

4.0 A/D Conversion Modes (Continued)

TABLE V(b). Channel Information for One A/D Conversion (ADC0858)

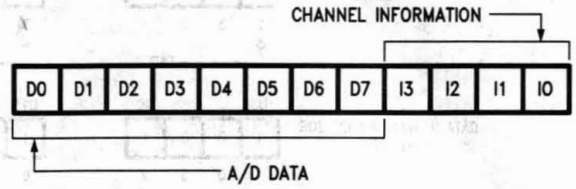
Channel Information				Channels Enabled
I3	I2	I1	I0	
0	0	0	0	CH0
0	0	0	1	CH0–CH1
0	0	1	0	CH1
0	0	1	1	Invalid
0	1	0	0	CH2
0	1	0	1	CH2–CH3
0	1	1	0	CH3
0	1	1	1	Invalid
1	0	0	0	CH4
1	0	0	1	CH4–CH5
1	0	1	0	CH5
1	0	1	1	Invalid
1	1	0	0	CH6
1	1	0	1	CH6–CH7
1	1	1	0	CH7
1	1	1	1	Invalid

The timing diagram for one A/D conversion is shown in *Figure 10*. After $\overline{CS}$ goes low, the input word (DI) is clocked in starting at the first rising edge of the digital clock signal, CLK. The first four bits of the input word configure the device for "one A/D conversion" mode while the following four bits (channel information address) assign the configuration of the MUX as per Table V(a) and (b) for the ADC0851 and the ADC0858 respectively. Any input data following the channel information address is ignored until the device's mode of operation is changed.

Taking $\overline{CS}$ high after the last bit of the channel information address loads the input word. Had $\overline{CS}$ been kept low longer, the following bits of the input word would have been ignored. The device takes one to two OSC clock periods after $\overline{CS}$ goes high to initiate the start of A/D conversion. The EOC output goes low, thus signalling the start of the conversion process. After a maximum of eighteen OSC clock periods, conversion is completed and EOC output goes high, thus signalling the end of conversion. The output data is now available and will be transmitted only if $\overline{CS}$ is brought low. The output data is transmitted starting at the first rising edge of CLK after $\overline{CS}$ goes low.

The format for the output word is as shown below.

Data Output (DO)—ADC0851 or ADC0858



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The first eight bits of the output word represent the digital equivalent of the input voltage. Bits I3 through I0 provide the channel configuration information as per Table V(a) and (b) for ADC0851 and ADC0858 respectively. Note that this information is the same as the channel information in the input word. The order in which the output data is transmitted is as follows:

- Data—LSB (D0) first
- Channel information—MSB (I3) first

Note that the output will be TRI-STATE if $\overline{CS}$ remains low after I0 is transmitted. Taking $\overline{CS}$ high after the output data is transmitted causes the device to initiate the start of the next A/D conversion on the same input while ignoring the data input word (DI). If the duration for which $\overline{CS}$ is high is less than seventeen OSC clock periods, the conversion process will be interrupted and the device will look for the mode address at the falling edge of $\overline{CS}$ so as to configure to a new mode of operation. However, if $\overline{CS}$ is high for eighteen or more OSC clock periods then the conversion operation will continue from point A on the timing diagram *(Figure 10)*.

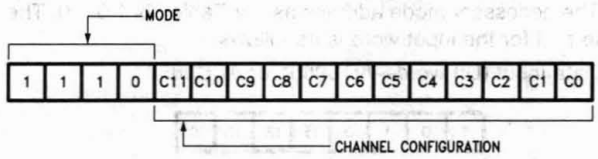
To ensure repetitive A/D conversion on the same input, $\overline{CS}$ going low should be synchronized with EOC going high. Thus after EOC goes high, the conversion is completed and $\overline{CS}$ can go low to transmit the output data. Meanwhile, if $\overline{CS}$ goes low while EOC is low then the conversion process is interrupted and the device is readied for a new mode of operation.

4.2 AUTO A/D CONVERSION MODE

When used in this mode, the ADC0851/8 offers added flexibility that many multiplexed A/D converters don't. In the auto A/D conversion mode, the ADC0851/8 scans through the selected input channels, performing A/D conversion on each channel without the need for reloading a new data input word each time. From Table I, the mode address for the "Auto A/D Conversion" mode is 1 1 1 0.

The format for the input word is as follows:

Data Input (DI) Word—ADC0851 or ADC0858



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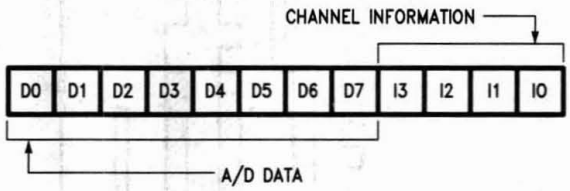
4.0 A/D Conversion Modes (Continued)

The 12-bit channel address following the mode address assigns the MUX configuration as per Table III(a) and (b) for ADC0851 and ADC0858 respectively. Note that the ADC0851 only decodes the three LSBs (C0, C1 and C2) of the channel address.

The timing diagram for "Auto A/D Conversion" mode is shown in *Figure 11*. The input word is loaded starting at the first rising edge of the CLK after $\overline{CS}$ goes low. The first four bits configure the device for the "Auto A/D Conversion" mode while the 12-bit channel address assigns the configuration of each channel pair. If $\overline{CS}$ remains low after C0 is loaded then any subsequent input data is ignored. Taking $\overline{CS}$ high after the input word is loaded initiates the start of A/D conversion. A/D conversion starts one to two OSC clock periods after $\overline{CS}$ goes high. The EOC output goes low to signal the start of an A/D conversion. The conversion time may range from 17 μs to 74 μs depending on how the channel pairs are configured. The EOC output goes high at the end of conversion thus signalling that the result of the A/D conversion can now be retrieved. The output data will be transmitted only if $\overline{CS}$ goes low and is transmitted starting at the first rising edge of CLK signal after $\overline{CS}$ goes low. The format for the output word is as follows:

Data Output (DO)—ADC0851 or ADC0858



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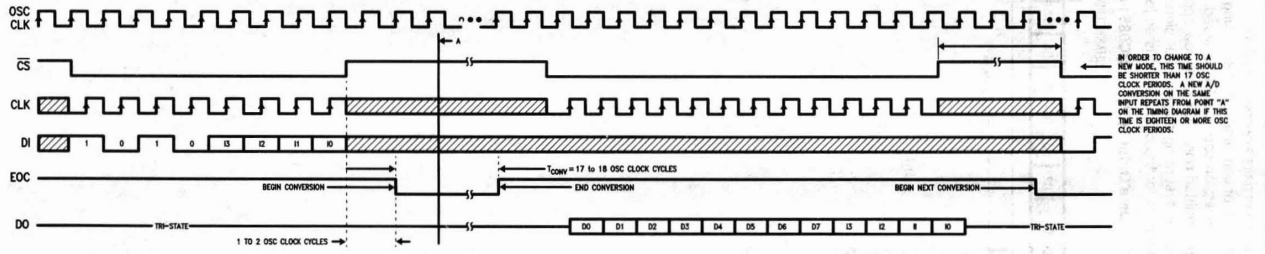

FIGURE 10. Timing Diagram for One A/D Conversion ADC0851/ADC0858

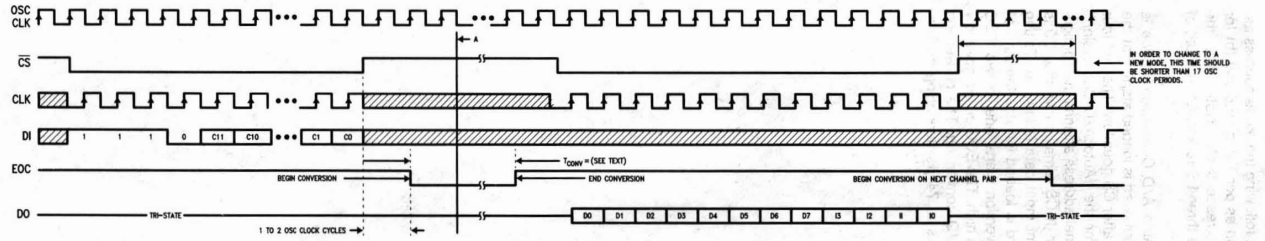

FIGURE 11. Timing Diagram for Auto A/D Conversion ADC0851/ADC0858

4.0 A/D Conversion Modes (Continued)

The first eight bits of the output word represents the digital equivalent of the analog input voltage. Status bits I3 through I0 provide the channel configuration information as per Table V(a) and (b) for ADC0851 and ADC0858 respectively.

Keeping $\overline{CS}$ low after I0 is transmitted causes the output to be TRI-STATE. Once the output data is transmitted, $\overline{CS}$ may go high to initiate the start of the next A/D conversion. The subsequent A/D conversion starts on the next channel pair that is configured as per the initially loaded input word *(Figure 11)*. Any data on the data input (DI) line is ignored. Note that if the duration for which $\overline{CS}$ is high is less than seventeen OSC clock periods then the conversion process would be interrupted and the device would look for the mode address at the falling edge of $\overline{CS}$ so that a new mode of operation can be configured.

To ensure proper operation in the "Auto A/D Conversion" mode, $\overline{CS}$ going low should be synchronized with EOC going high. Thus after EOC goes high, the conversion is completed and $\overline{CS}$ can go low to transmit the output data. After the output data is transmitted, $\overline{CS}$ should go high to initiate automatic A/D conversion on the next channel pair and remain high until the conversion is completed and EOC goes high. Meanwhile, if $\overline{CS}$ goes low while EOC is low then the conversion process is interrupted and the device is readied for a new mode of operation.

5.0 Test Mode

A mode address of 1 1 0 0 configures the device in the test mode. This mode is used to test the internal operation of the device at the factory and is not recommended for normal use. If the device is accidentally configured in the test mode then the power supply must be disconnected and reconnected again to reset the device.

6.0 Bidirectional I/O

If the microprocessor has bidirectional Input/Output capability then ADC0851/8's input and output pins can be tied together and a single wire can be used to serially input data to or output data from ADC0851/8. This capability is made possible because when the input word is clocked in, the output pin is in TRI-STATE and when the output word is clocked out, the data at the input pin is ignored.

II. Analog Considerations

1.0 A/D Conversion Time

The A/D conversion time is a function of the OSC clock frequency. The oscillator frequency is set by connecting an external resistor, R_{ext} from the ADC0851/8's OSC pin to V_{CC} and an external capacitor, C_{ext} from the OSC pin to ground. With R_{ext} = 3.16 kΩ and C_{ext} = 170 pF, the OSC frequency is 1 MHz at V_{CC} = 4.5V and 1.05 MHz at V_{CC} = 5.5V.

The OSC frequency will vary as the ambient temperature varies, this is shown by the Typical Performance Characteristics curve, "OSC Frequency vs Temperature". For a specified external resistor, the OSC frequency can be changed by varying the external capacitor as is shown by the Typical Performance Characteristics curve, "OSC Frequency vs R_{ext} and C_{ext}". Note that the OSC pin of the ADC0851/8 should not be driven by an external clock as this might cause improper operation. The A/D converter's conversion time is a minimum of seventeen OSC clock periods and a maximum of eighteen. *Figure 12* shows a typical connection for the ADC0851 and ADC0858.

2.0 The Reference

The magnitude of the reference voltage (V_{REF}) applied to the A/D converter determines the analog input voltage span (i.e., the difference between $V_{IN(max)}$ and $V_{IN(Min)}$) over which the 256 possible output codes apply. The reference voltage source connected to the V_{REF} pin of ADC0851/8 must be capable of driving a minimum load of 4 kΩ.

The ADC0851/8 can be used in either ratiometric applications or in systems requiring absolute accuracy. In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D's reference. This voltage is usually the system power supply, so the V_{REF} pin can be tied to V_{CC}.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin must be connected to a voltage source that is stable over time and temperature. The LM385 and LM336 micropower references are good low current devices for use with these A/D converters.

The maximum value of the reference voltage is limited by the A/D converter's power supply voltage, V_{CC}. The minimum value, however, can be as low as 1V while maintaining a typical Integral Linearity of ±1 LSB (see Typical Performance Characteristics curve, "Linearity Error vs Reference voltage"). This allows direct conversion of transducer outputs that provide less than a 5V output span. Due to the increased sensitivity of the A/D converter at low reference voltages (e.g., 1 LSB = 3.9 mV for a 1V full scale range), care must be exercised with regard to noise pickup, circuit layout, and system error voltage sources.

3.0 The Analog Inputs

3.1 REDUCING COMMON MODE ERROR

Rejection of common mode noise can be achieved by configuring the ADC0851/8's inputs in the differential mode since the offending common mode signal is common to both the selected "+" and "−" inputs. The time interval between sampling the "+" input and the "−" input is one oscillator clock period. A change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error(Max)} = V_{PEAK}(2\pi f_{CM})\,(1/f_{OSC})$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is the signal's peak voltage and f_{OSC} is the A/D converter's OSC clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV for a 5V full scale range) with the converter running at f_{OSC} = 250 kHz, its peak voltage would have to be 3.3V.

3.2 SOURCE RESISTANCE

For a source resistance under 2 kΩ, the ADC0851/8's total unadjusted error is typically ±0.2 LSB at V_{REF} = 4.75V and $f_{OSC} \leq$ 1 MHz (see Typical Performance Characteristics curves, "Total Unadjusted Error vs Source Impedance").

One source of error is the multiplexer's leakage current of 3 μA which contributes a 3 mV drop across a 1 kΩ source

3.0 The Analog Inputs (Continued)

resistance. Another source of error is the sampling nature of the A/D converter. Short spikes of current enter the "+" input and exit the "−" input at the rising and falling transition of the OSC clock . These currents decay rapidly and generally do not cause errors since the internal comparator is strobed at the end of a clock period. If large source resistances are used however, then the transients caused by the current spikes may not settle completely before conversion begins. If a capacitor is used at the input of the A/D converter for input filtering then the input signal source resistance should be kept at 1 kΩ or less.

3.3 ANALOG INPUT PROTECTION

Often the analog inputs of A/D converters are driven from voltage sources that can swing higher than V_{CC} or lower than GND. Analog inputs often come from op amps which use ±15V supplies. While during normal operation the input voltages stay within the 0V–5V A/D converter supply voltage range, at power up the input voltage may actually rise above or fall below the A/D converter's supply voltages. If the input voltage to any A/D converter input pin does fall outside the supply voltage by more than 0.3V (worst case) and the input draws more than 5 mA then there is a good possibility that the converter may latch up and provide a low impedance short between V_{CC} and GND.

Figure 13 shows the overvoltage protection circuit for the analog input. If, for instance, the amplifier's output saturates to its positive supply rail, then the junction of R1 and R2 would be clamped to V_{CC} plus a diode drop. Resistor R1 limits the op amp's output current and R2 limits the current flowing into the input of the A/D converter. Likewise, the junction of R1 and R2 would be clamped to a diode drop below ground if the op amp's output saturates to the negative rail.

4.0 Zero Scale and Full Scale Adjustment

4.1 ZERO SCALE ERROR

The zero scale error of the A/D converter does not require adjustment. If the minimum analog input voltage value, $V_{IN(Min)}$, is not at ground potential then a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the $V_{IN(-)}$ input of a differential input pair at this $V_{IN(Min)}$ value. This utilizes the differential mode operation of the A/D converter.

The zero scale error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage (the ideal ½ LSB value, ½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}) and the applied input voltage that causes an output digital code transition from 0000 0000 to 0000 0001.

4.2 FULL SCALE ADJUSTMENT

The full-scale adjustment can be made by applying an input voltage that is 1.5 LSB less than the desired analog full-scale voltage and then adjusting the magnitude of the V_{REF} input voltage for a digital output code that just changes from 1111 1110 to 1111 1111.

4.3 ADJUSTING FOR AN ARBITRARY ANALOG INPUT VOLTAGE RANGE

Analog input voltages that span from a positive non-zero minimum value can easily be accommodated by the ADC0851/8. In this case, the A/D converter is used in the differential mode and a reference voltage equal to $V_{IN(Min)}$ is applied to the $V_{IN(-)}$ input. Normally zero scale adjustment is not required because the zero scale error is very small. However, if zero scale adjustment is desired then a voltage equal to $V_{IN(Min)}$ plus ½ LSB (where 1 LSB = Input voltage span/256) should be applied to $V_{IN(+)}$ and the reference voltage at $V_{IN(-)}$ should be adjusted such that the output code just changes from 0000 0000 to 0000 0001.

Once the proper reference voltage is applied to the $V_{IN(-)}$ input then full scale adjustment can be made. Full scale adjustment is made by first applying a voltage to the $V_{IN(+)}$ input that is 1.5 LSB less than $V_{IN(Max)}$ i.e.;

$$V_{IN(+)\,FS\,ADJ} = V_{Max} - 1.5\,[(V_{Max} - V_{Min})/256]$$

where, V_{Max} = the high end of the analog input voltage range

V_{Min} = the low end of the analog input voltage range

The reference voltage, V_{REF} applied to the reference input pin of the A/D converter is adjusted so that the output code just changes from 1111 1110 to 1111 1111. This completes the adjustment procedure.

Typical Applications

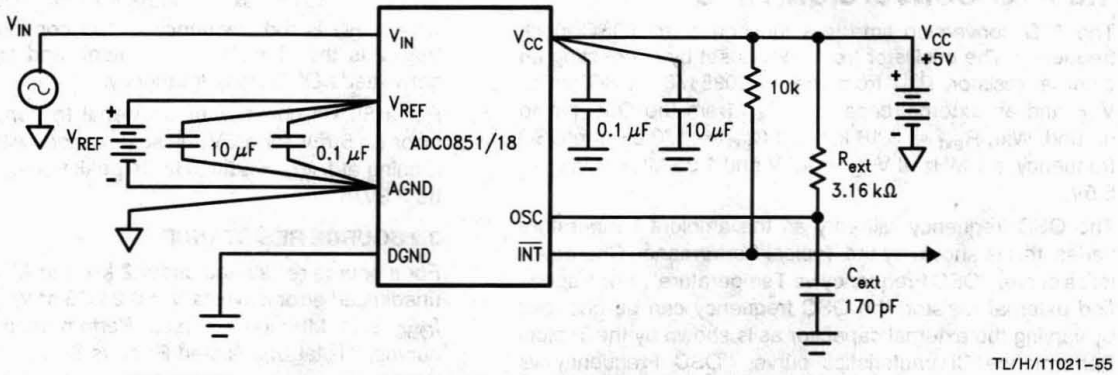

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FIGURE 12. Recommended Connection for ADC0851 and ADC0858

Typical Applications (Continued)

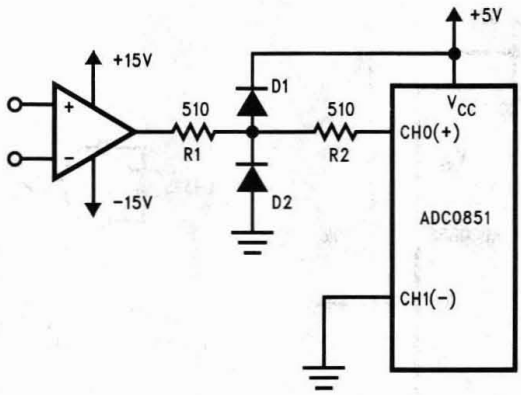

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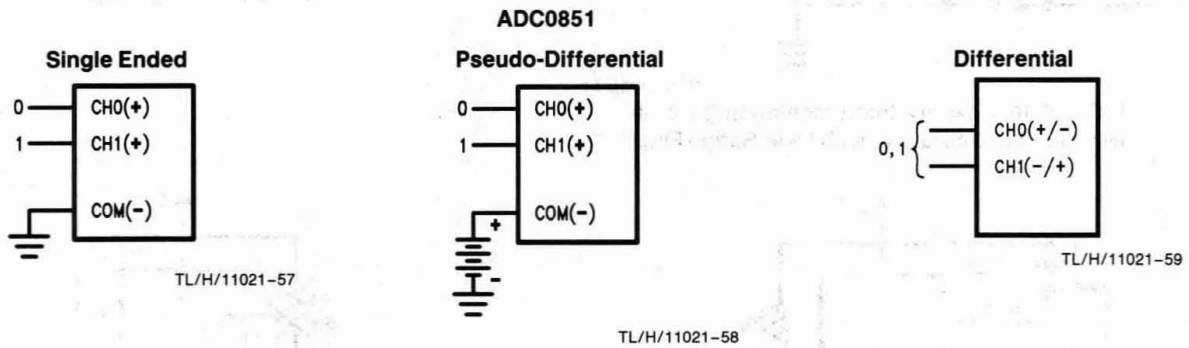
FIGURE 13. Over Voltage Protection of the Analog Inputs



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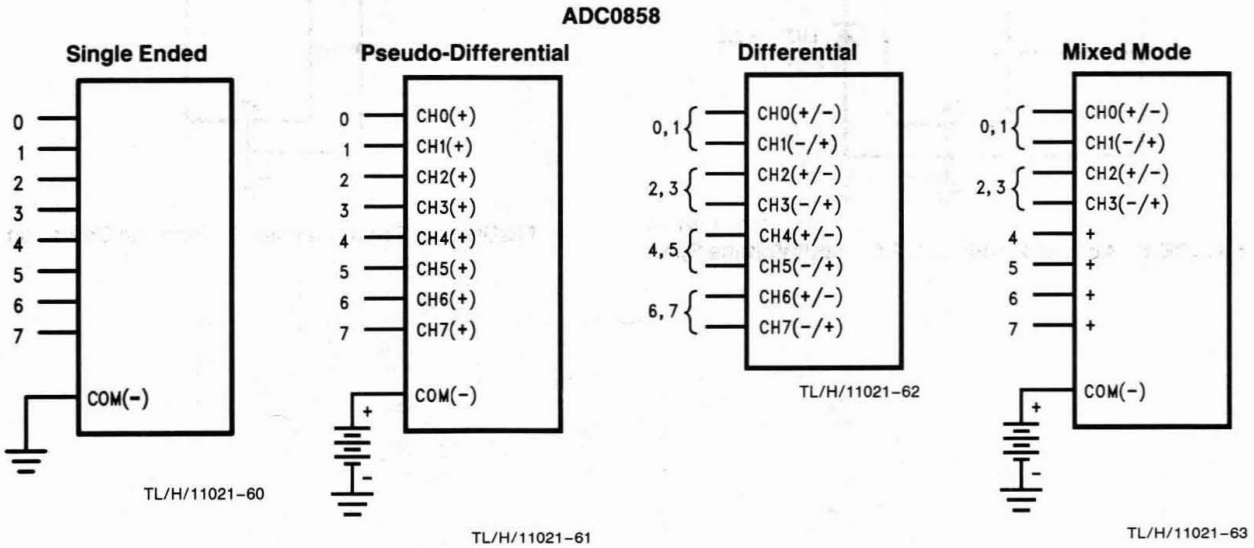
TL/H/11021–58

TL/H/11021–59

FIGURE 14. Analog Input Multiplexer Options for ADC0851



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TL/H/11021–62

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FIGURE 15. Analog Input Multiplexer Options for ADC0858

Typical Applications (Continued)

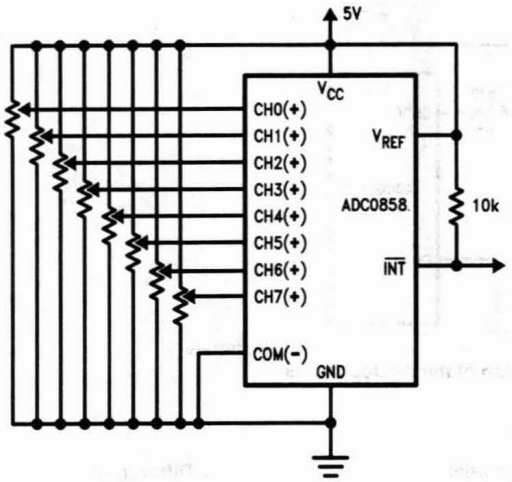

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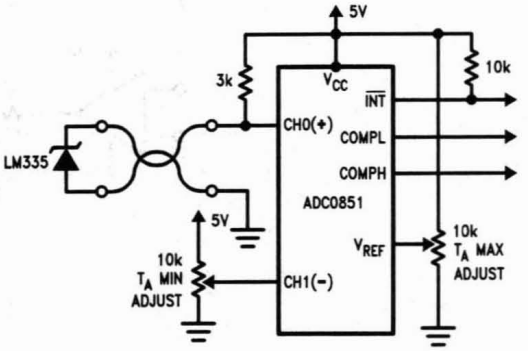
FIGURE 16. Adaptive Instrumentation Control (Ratiometric Operation) with Over Range Flag



TL/H/11021–65

FIGURE 17. Remote Temperature Sensor with Over Range Flag

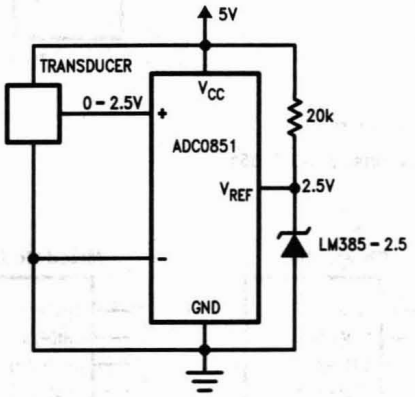


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FIGURE 18. Absolute Input with 2.5V Input Voltage Span

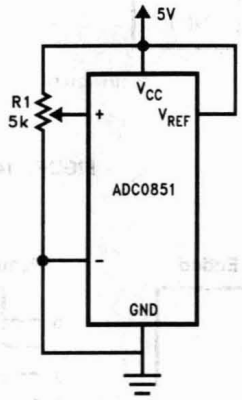

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FIGURE 19. Single Channel Ratiometric Operation

National Semiconductor

LM12434/LM12{L}438 12-Bit + Sign Data Acquisition System with Serial I/O and Self-Calibration

General Description

The LM12434 and LM12{L}438 are highly integrated Data Acquisition Systems. Operating on 3V to 5V, they combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word instruction RAM can store the conversion sequence for up to eight acquisitions through the LM12{L}438's eight-input multiplexer. The LM12434 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12434 and LM12{L}438 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits.

Acquisition times and conversion rates are programmable through the use of internal clock-driven timers. The differential reference voltage inputs can be externally driven for absolute or ratiometric operation.

All registers, RAM, and FIFO are directly accessible through the high speed and flexible serial I/O interface bus. The serial interface bus is user selectable to interface with the following protocols with zero glue logic: MICROWIRE/PLUS™, Motorola's SPI/QSPI, Hitachi's SCI, 8051 Family's Serial Port (Mode 0), I²C and the TMS320 Family's Serial Port.

An evaluation kit for demonstrating the LM12434 and LM12{L}438 is available.

Key Specifications

f_{CLK} = 8 MHz {L, f_{CLK} = 6 MHz}

- Resolution — 12-bit + sign or 8-bit + sign
- 13-bit conversion time — 5.5 μs {7.3 μs} (max)
- 9-bit conversion time — 2.6 μs {3.5 μs} (max)
- 13-bit Through-put rate — 140k samples/s {105k sample/s} (min)
- Comparison time ("watchdog" mode) — 1.4 μs {1.8 μs} (max)
- Serial Clock — 10 MHz {6 MHz} (max)
- Integral Linearity Error — ±1 LSB (max)
- V_{IN} range — GND to V_A^+
- Power dissipation — 45 mW {20 mW} (max)
- Stand-by mode power dissipation — 25 μW {16.5 μW} (typ)
- Supply voltage LM12L438 — 3.3V ±10%
  LM12434/8 — 5V ±10%

Features

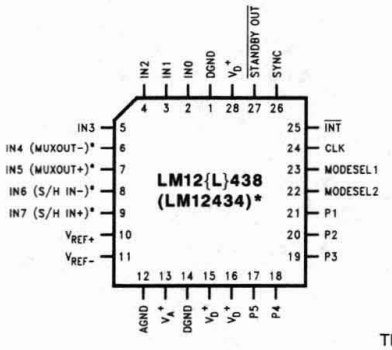
- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog" comparison mode
- Single-ended or differential inputs
- Built-in Sample-and-Hold
- Instruction RAM and event sequencer
- 8-channel (LM12{L}438) or 4-channel (LM12434) multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- Power down output for system power management
- Read while convert capability for maximum through-put rate

Applications

- Data Logging
- Portable Instrumentation
- Process Control
- Energy Management
- Robotics

Connection Diagrams

28-Pin PLCC Package

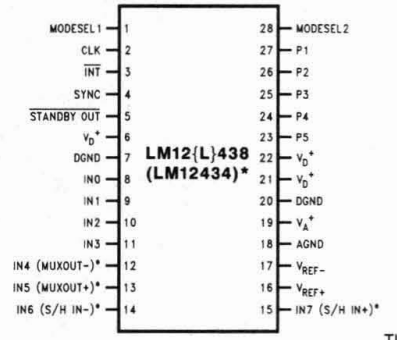


TL/H/11879–1

*Pin names in ( ) apply to the LM12434

Order Number LM12434CIV, LM12438CIV, or LM12L438CIV
See NS Package Number V28A

28-Pin Wide Body SO Package



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Order Number LM12434CIWM, LM12438CIWM, or LM12L438CIWM
See NS Package Number M28B

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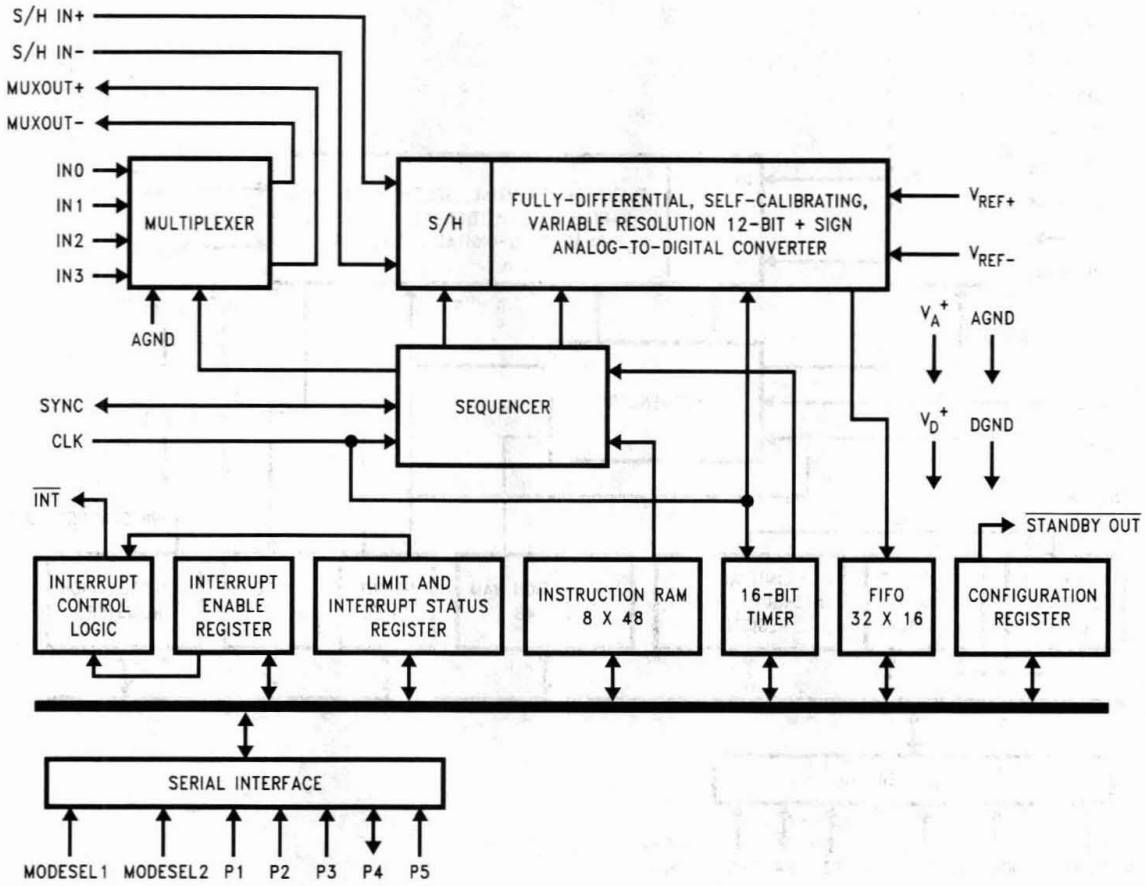
1.0 Functional Diagrams

LM12434



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INTERFACE	MODESEL1	MODESEL2	P1	P2	P3	P4	P5
Standard	0	1	$\overline{R}$/F	$\overline{CS}$	DI	DO	SCLK
8051	0	0	1*	1*	$\overline{CS}$	RXD	TXD
I^2C	1	0	SAD0	SAD1	SAD2	SDA	SCL
TMS320	1	1	FSR	FSX	DX	DR	SCLK

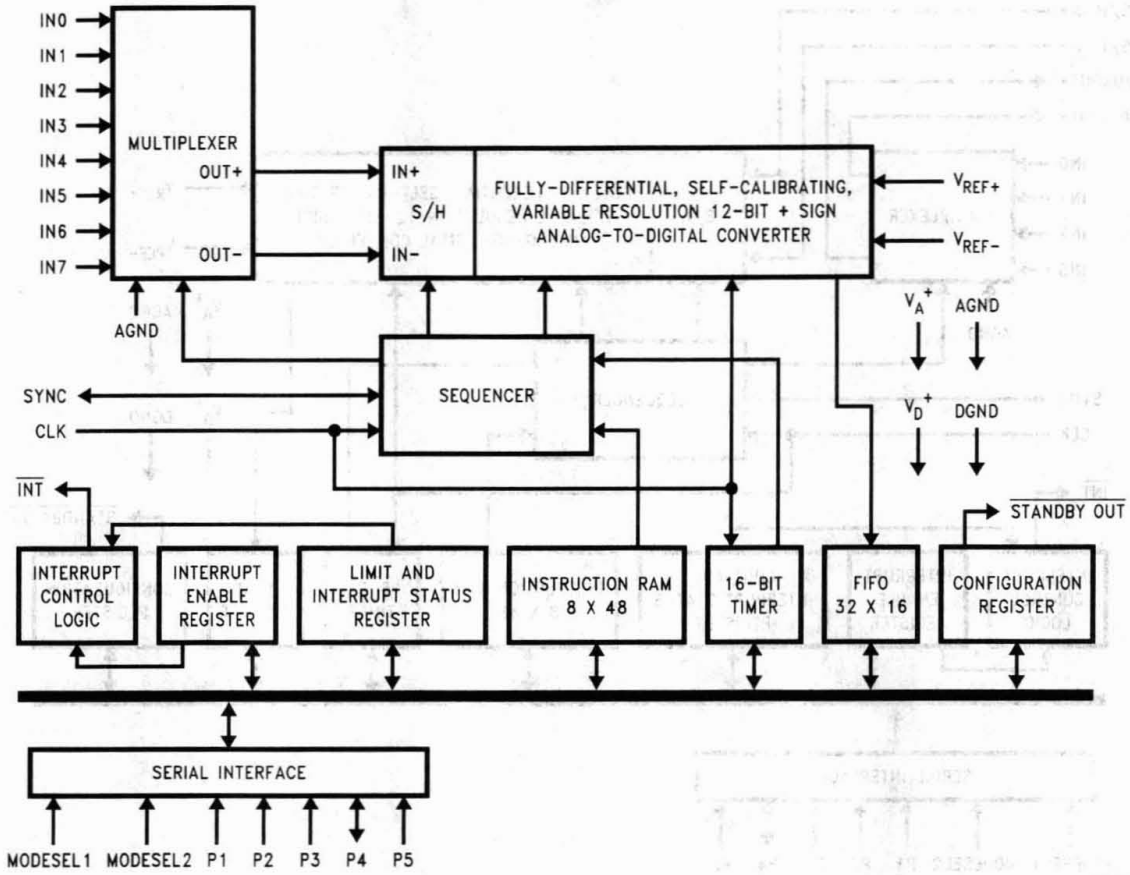
*Internal pull-up

Ordering Information (LM12434)

Part Number	Package Type	NSC Package Number	Temperature Range
LM12434CIV	28-Pin PLCC	V28A	−40°C to +85°C
LM12434CIWM	28-Pin Wide Body SO	M28B	−40°C to +85°C

1.0 Functional Diagrams (Continued)

LM12{L}438



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INTERFACE	MODESEL1	MODESEL2	P1	P2	P3	P4	P5
Standard	0	1	$\overline{R}$/F	$\overline{CS}$	DI	DO	SCLK
8051	0	0	1*	1*	$\overline{CS}$	RXD	TXD
I^2C	1	0	SAD0	SAD1	SAD2	SDA	SCL
TMS320	1	1	FSR	FSX	DX	DR	SCLK

*Internal pull-up

Ordering Information (LM12{L}438)

Part Number	Package Type	NSC Package Number	Temperature Range
LM12438CIV LM12L438CIV	28-Pin PLCC	V28A	−40°C to +85°C
LM12438CIWM LM12L438CIWM	28-Pin Wide Body SO	M28B	−40°C to +85°C
LM12438 Eval	Evaluation Board and Windows® based software		

2.0 Electrical Specifications

2.1 RATINGS

2.1.1 Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_A^+ and V_D^+)	6.0V
Voltage at Input and Output Pins except IN0–IN3 (LM12434) and IN0–IN7 (LM12{L}438)	−0.3V to V^+ + 0.3V
Voltage at Analog Inputs IN0–IN3 (LM12434) and IN0–IN7 (LM12{L}438)	GND − 5V to V^+ + 5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
$\lvert AGND - DGND \rvert$	300 mV
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation (T_A = 25°C) (Note 4)	
V Package	
WM Package	
Storage Temperature	−65°C to +150°C
Soldering Information, Lead Temperature (Note 19)	
V Package, Vapor Phase (60 seconds)	
Infrared (15 seconds)	
WM Package, Vapor Phase (60 seconds)	
Infrared (15 seconds)	
ESD Susceptibility (Note 5)	1.5 kV

2.1.2 Operating Ratings (Notes 1 & 2)

Temperature Range	($T_{min} \le T_A \le T_{max}$)
LM12434CIV/LM12{L}438CIV	$-40°C \le T_A \le 85°C$
LM12434CIWM, LM12{L}438CIWM	$-40°C \le T_A \le 85°C$
Supply Voltage	
V_A^+, V_D^+	3.0V to 5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤100 mV
$\lvert AGND - DGND \rvert$	≤100 mV
Analog Inputs Range	$GND \le V_{IN+} \le V_A^+$
V_{REF+} Input Voltage	$1V \le V_{REF+} \le V_A^+$
V_{REF-} Input Voltage	$0V \le V_{REF-} \le V_{REF+} - 1V$
$V_{REF+} - V_{REF-}$	$1V \le V_{REF} \le V_A^+$
V_{REF} Common Mode Range (Note 16)	$0.1\ V_A^+ \le V_{REFCM} \le 0.6\ V_A^+$

2.2 PERFORMANCE CHARACTERISTICS All specifications apply to the LM12434, LM12438, and LM12L438 unless otherwise noted. Specifications in braces { } apply only to the LM12L438.

2.2.1 Converter Static Characteristics The following specifications apply to the LM12434 and LM12{L}438 for $V_A^+ = V_D^+ = 5V$ {3.3V}, AGND = DGND = 0V, V_{REF+} = 4.096V {2.5V}, V_{REF-} = 0V, 12-bit + sign conversion mode, f_{CLK} = 8.0 MHz {6 MHz}, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \le 25\Omega$, fully-differential input with fixed 2.048V {1.25V} common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J$ = 25°C. (Notes 6, 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
ILE	Positive and Negative Integral Linearity Error	After Auto-Cal (Notes 12, 17)	±0.35	**±1**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Note 12)	±1		LSB
	Resolution with No Missing Codes	After Auto-Cal (Note 12)		**13**	Bits
DNL	Differential Non-Linearity	After Auto-Cal	±0.2	**±1**	LSB (max)
	Zero Error	After Auto-Cal (Notes 13, 17)	±0.2	**±1**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 17)	±0.2	**±2**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 17)	±0.2	**±2**	LSB (max)
	DC Common Mode Error	(Note 14)	±2	**±3.5** {±4.0}	LSB (max)
ILE	8-Bit + Sign and "Watchdog" Mode Positive and Negative Integral Linearity Error	(Note 12)	±0.15	**±1/2**	LSB (max)
TUE	8-Bit + Sign and "Watchdog" Mode Total Unadjusted Error	After Auto-Zero	±1/2	**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Resolution with No Missing Codes			**9**	Bits (max)

2.0 Electrical Specifications (Continued)

2.2.1 Converter Static Characteristics The following specifications apply to the LM12434 and LM12{L}438 for $V_A^+ = V_D^+ = 5V$ {3.3V}, AGND = DGND = 0V, $V_{REF+} = 4.096V$ {2.5V}, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz {6 MHz}, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V {1.25V} common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8 and 9) (Continued)

Symbol	Parameter		Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
DNL	8-Bit + Sign and "Watchdog" Mode Differential Non-Linearity			±0.15	**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Zero Error		After Auto-Zero	±0.05	**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Positive and Negative Full-Scale Error			±0.1	**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode DC Common Mode Error			±1/8		LSB
	Multiplexer Channel-to-Channel Matching			±0.05		LSB
V_{IN+}	Non-Inverting Input Range				**GND** **V_A^+**	V (min) V (max)
V_{IN-}	Inverting Input Range				**GND** **V_A^+**	V (min) V (max)
$V_{IN+} - V_{IN-}$	Differential Input Voltage Range				**$-V_A^+$** **V_A^+**	V (min) V (max)
$\frac{V_{IN+} - V_{IN-}}{2}$	Common Mode Input Voltage Range				**GND** **V_A^+**	V (min) V (max)
PSS	Power Supply Sensitivity (Note 15)	Zero Error Full-Scale Error Linearity Error	$V_A^+ = V_D^+ = 5V \pm 10\%$, $V_{REF+} = 4.096V$, $V_{REF-} = GND$	±0.05 ±0.25 ±0.2	**±1.0** **±1.5**	LSB (max) LSB (max) LSB
C_{REF}	V_{REF+}/V_{REF-} Input Capacitance			85		pF
C_{IN}	Selected Multiplexer Channel Input Capacitance			75		pF

2.2.2 Converter Dynamic Characteristics The following specifications apply only to the LM12434 and LM12438 for $V_A^+ = V_D^+ = 5V$, AGND = DGND = 0V, $V_{REF+} = 4.096V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz, throughput rate = 133.3 kHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V {1.25V} common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
	CLK Duty Cycle		50	 **40** **60**	% % (min) % (max)
t_C	Conversion Time	13-Bit Resolution, Sequencer State S5 *(Figure 10)*	44 (t_{CLK})	**44 (t_{CLK}) + 50 ns**	(max)
		9-Bit Resolution, Sequencer State S5 *(Figure 10)*	21 (t_{CLK})	**21 (t_{CLK}) + 50 ns**	(max)
t_A	Acquisition Time (Programmable)	Sequencer State S7 *(Figure 10)* Minimum for 13-Bits Maximum for 13-Bits (D = 15)	 9 (t_{CLK}) 39 (t_{CLK})	 **9 (t_{CLK}) + 50 ns** **39 (t_{CLK}) + 50 ns**	t_{CLK} = CLK Period (max) (max)
		Minimum for 9-Bits *(Figure 10)* Maximum for 9-Bits (D = 15)	2 (t_{CLK}) 2 (t_{CLK})	**2 (t_{CLK}) + 50 ns** **32 (t_{CLK}) + 50 ns**	(max) (max)

2.0 Electrical Specifications (Continued)

2.2.2 Converter Dynamic Characteristics The following specifications apply only to the LM12434 and LM12438 for $V_A^+ = V_D^+ = 5V$, AGND = DGND = 0V, $V_{REF+} = 4.096V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz, throughput rate = 133.3 kHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8 and 9) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
t_Z	Auto-Zero Time	Sequencer State S2 *(Figure 10)*	76 (t_{CLK})	**76 (t_{CLK}) + 50 ns**	(max)
t_{CAL}	Full Calibration Time	Sequencer State S2 *(Figure 10)*	4944 (t_{CLK})	**4944 (t_{CLK}) + 50 ns**	(max)
	Throughput Rate	(Note 18)	142	**140**	kHz (min)
t_{WD}	"Watchdog" Mode Comparison Time	Sequencer States S6, S4, and S5 *(Figure 10)*	11 (t_{CLK})	**11 (t_{CLK}) + 50 ns**	(max)
SNR	Signal-to-Noise Ratio, Differential Input	$V_{IN} = \pm 4.096V$ (Note 20) $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 79 79 70		 dB dB dB
SNR	Signal-to-Noise Ratio, Single-Ended Input	$V_{IN} = 4.096\ V_{p-p}$ $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 71 71 67		 dB dB dB
SINAD	Signal-to-Noise + Distortion Ratio, Differential Input	$V_{IN} = \pm 4.096V$ (Note 20) $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 79 78 67		 dB dB dB
SINAD	Signal-to-Noise + Distortion Ratio, Single-Ended Input	$V_{IN} = 4.096\ V_{p-p}$ $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 71 70 64		 dB dB dB
THD	Total Harmonic Distortion, Differential Input	$V_{IN} = \pm 4.096V$ (Note 20) $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 −90 −85 −71		 dBc dBc dBc
THD	Total Harmonic Distortion, Distortion, Single-Ended Input	$V_{IN} = 4.096\ V_{p-p}$ $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 −88 −82 −67		 dBc dBc dBc
ENOB	Effective Number of Bits, Differential Input	$V_{IN} = \pm 4.096V$ (Note 20) $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 12.6 12.2 12.1		 Bits Bits Bits
ENOB	Effective Number of Bits, Single-Ended Input	$V_{IN} = 4.096\ V_{p-p}$ $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 11.3 11.2 10.8		 Bits Bits Bits
SFDR	Spurious Free Dynamic Range, Differential Input	$V_{IN} = \pm 4.096V$ (Note 20) $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 90 86 76		 dBc dBc dBc
SFDR	Spurious Free Dynamic Range, Single-Ended Input	$V_{IN} = 4.096V\ V_{p-p}$ $f_{IN} = 1$ kHz $f_{IN} = 10$ kHz $f_{IN} = 62$ kHz	 90 85 72		 dBc dBc dBc

2.0 Electrical Specifications (Continued)

2.2.2 Converter Dynamic Characteristics The following specifications apply only to the LM12434 and LM12438 for $V_A^+ = V_D^+ = 5V$, AGND = DGND = 0V, $V_{REF+} = 4.096V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz, throughput rate = 133.3 kHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8 and 9) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
IMD	Two Tone Intermodulation Distortion Differential Input	$V_{IN} = \pm 4.096V$ (Note 20) $f_1 = 19.190$ kHz $f_2 = 19.482$ kHz	−82		dBc
IMD	Two Tone Intermodulation Distortion Single Ended Input	$V_{IN} = 4.096\ V_{pp}$ $f_1 = 19.190$ kHz $f_2 = 19.482$ kHz	−80		dBc
	Multiplexer Channel-to-Channel Crosstalk	$V_{IN} = 4.096\ V_{PP}$ $f_{IN} = 5$ kHz $f_{CROSSTALK} = 40$ kHz LM12434 MUXOUT Only and LM12438 MUX plus Converter (Note 21)	−90		dBc
t_{PU}	Power-Up Time		10		ms
t_{WU}	Wake-Up Time	(Note 22)	2		ms

2.2.3 DC Characteristics The following specifications apply to the LM12434 and LM12{L}438 for $V_A^+ = V_D^+ = 5V$ {3.3V], AGND = DGND = 0V, $V_{REF+} = 4.096V$ {2.5V}, $V_{REF-} = 0V$, $f_{CLK} = 8.0$ MHz {6 MHz}and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
I_D^+	V_D^+ Supply Current	$f_{CLK} = 8$ MHz {6 MHz} f_{SCLK} = Stopped $f_{SCLK} = 10$ MHz {8 MHz}	 2.0 {1.4} 4.0 {2.0}	 5.0 {2.5}	 mA (max) mA (max)
I_A^+	V_A^+ Supply Current	$f_{CLK} = 8$ MHz {6 MHz}	2.8 {2.2}	4.0 {3.5}	mA (max)
I_{ST}	Stand-By Supply Current ($I_D^+ + I_A^+$)	Stand-By Mode Selected f_{SCLK} = Stopped f_{CLK} = Stopped $f_{CLK} = 8$ MHz {6 MHz} $f_{SCLK} = 10$ MHz {8 MHz} f_{CLK} = Stopped $f_{CLK} = 8$ MHz {6 MHz}	 5{5} 120 {50} 1.4 {0.8} 1.4 {0.8}	 	 μA (max) μA (max) mA (max) mA (max)
	Multiplexer ON-Channel Leakage Current	$V_A^+ = 5.5V$ ON-Channel = 5.5V OFF-Channel = 0V ON-Channel = 0V OFF-Channel = 5.5V	 0.1 	 **1.0 {3.0}** **1.0 {3.0}**	 μA (max) μA (max)
	Multiplexer OFF-Channel Leakage Current	$V_A^+ = 5.5V$ {3.3V} ON-Channel = 5.5V {3.3V} OFF-Channel = 0V ON-Channel = 0V OFF-Channel = 5.5V {3.3V}	 0.1 	 **1.0 {3.0}** **1.0 {3.0}**	 μA (max) μA (max)

2.0 Electrical Specifications (Continued)

2.2.3 DC Characteristics The following specifications apply to the LM12434 and LM12{L}438 for $V_A^+ = V_D^+ = 5V$ {3.3V], AGND = DGND = 0V, $V_{REF+} = 4.096V$ {2.5V}, $V_{REF-} = 0V$, $f_{CLK} = 8.0$ MHz {6 MHz}and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
R_{ON}	Multiplexer ON-Resistance	LM12434			
		$V_{IN} = 5V$	650	**1000**	Ω(max)
		$V_{IN} = 2.5V$	700	**1000**	Ω(max)
		$V_{IN} = 0V$	630	**1000**	Ω(max)
	Multiplexer Channel-to-Channel R_{ON} matching	LM12434			
		$V_{IN} = 5V$	±1.0%	**±3.0%**	(max)
		$V_{IN} = 2.5V$	±1.0%	**±3.0%**	(max)
		$V_{IN} = 0V$	±1.0%	**±3.0%**	(max)

2.2.4 Digital DC Characteristics The following specifications apply to the LM12434 and LM12{L}438 for $V_A^+ = V_D^+ = 5V$ {3.3V}, AGND = DGND = 0V, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage	$V_A^+ = V_D^+ = 5.5V$ {3.6V}		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_A^+ = V_D^+ = 4.5V$ {3.0V}		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$ {3.3V}	0.005	**1.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	μA (max)
C_{IN}	All Digital Inputs		6		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_A^+ = V_D^+ = 4.5V$ {3.0V}			
		$I_{OUT} = -360\ \mu A$		**2.4**	V (min)
		$I_{OUT} = -10\ \mu A$		**4.25** {**2.9**}	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_A^+ = V_D^+ = 4.5V$ {3.0V} $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.05	**−3.0**	μA (max)
		$V_{OUT} = 5V$ {3.3V}	0.05	**3.0**	μA (max)

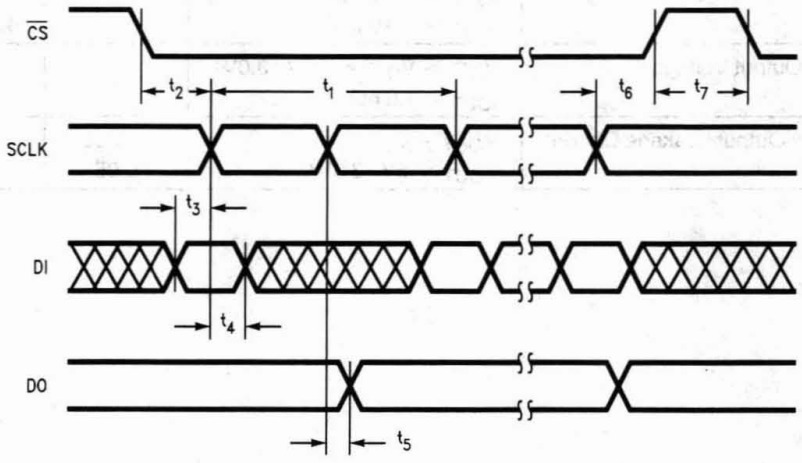
2.0 Electrical Specifications (Continued)

2.3 DIGITAL SWITCHING CHARACTERISTICS The following specifications apply to the LM12434 and LM12{L}438 for $V_A+ = V_D+ = 5V$ {3.3V}, AGND = DGND = 0V, C_L (load capacitance) on output lines = 80 pF unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX},** all other limits for $T_A = T_J = 25°C$. (Notes 6, 7, and 9)

2.3.1 Standard Mode Interface (MICROWIRE/PLUS™, SCI and SPI/QSPI)

Symbol (See *Figure* Below)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
t_1	SCLK (Serial Clock) Period			**100** {**125**}	ns (min)
t_2	CS Set-Up Time to First Clock Transition			**25** {**30**}	ns (min)
t_3	DI Valid Set-Up Time to Data Capture Transition of SCLK			**0**	ns (min)
t_4	DI Valid Hold Time to Data Capture Transition of SCLK			**40**	ns (min)
t_5	DO Hold Time from Data Shift Transition of SCLK			**70** {**120**}	ns (max)
t_6	CS Hold Time from Last SCLK Transition in a Read or Write Cycle (Excluding Burst Read Cycle)			**25**	ns (min)
t_7	CS Inactive to CS Active Again			**3**	CLK Cycle (min)*
t_8	SCLK Idle Time between the End of the Command Byte Transfer and the Start of the Data Transfer in Read Cycles			**3**	CLK Cycle (min)*

*CLK is the main clock input to the device, pin number 24 in PLCC package or pin number 2 in SO package.



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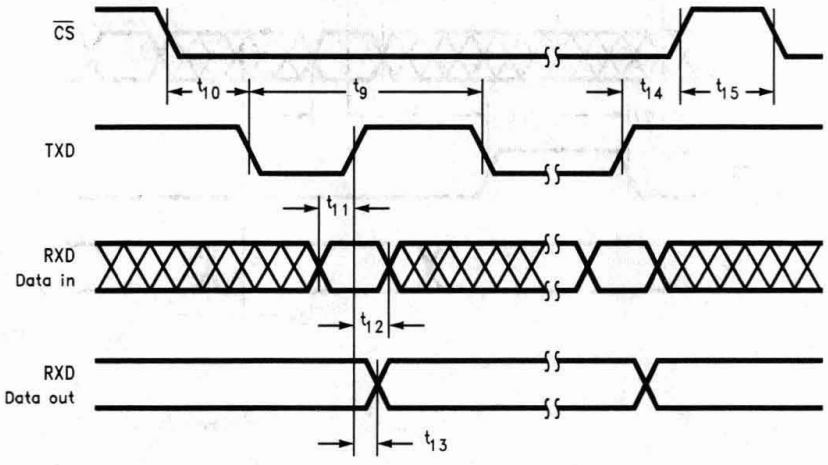
2.0 Electrical Specifications (Continued)

2.3 DIGITAL SWITCHING CHARACTERISTICS The following specifications apply to the LM12434 and LM12{L}438 for $V_A+ = V_D+ = 5V$ {3.3V}, AGND = DGND = 0V, C_L (load capacitance) on output lines = 80 pF unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX},** all other limits for $T_A = T_J = 25°C$. (Notes 6, 7, and 9) (Continued)

2.3.2 8051 Interface Mode

Symbol (See *Figure* Below)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
t_9	TXD (Serial Clock Period)			**125** {**250**}	ns (min)
t_{10}	CS Set-Up Time to First Clock Transition			**25** {**40**}	ns (min)
t_{11}	Data in Valid Set-Up Time to TXD Clock High			**40**	ns (min)
t_{12}	Data in Valid Hold Time from TXD Clock High			**40** {**90**}	ns (min)
t_{13}	Data Out Hold Time from TXD Clock High			**70** {**120**}	ns (max)
t_{14}	CS Hold Time from Last TXD High in a Read or Write Cycle (Excluding Burst Read Cycle)			**25** {**50**}	ns (min)
t_{15}	CS Inactive to CS Active Again			**3**	CLK Cycle (min)*
t_{16}	SCLK Idle Time between the End of the Command Byte Transfer and the Start of the Data Transfer in Read Cycles			**3**	CLK Cycle (min)*

*CLK is the main clock input to the device, pin number 24 in PLCC package or pin number 2 in SO package.



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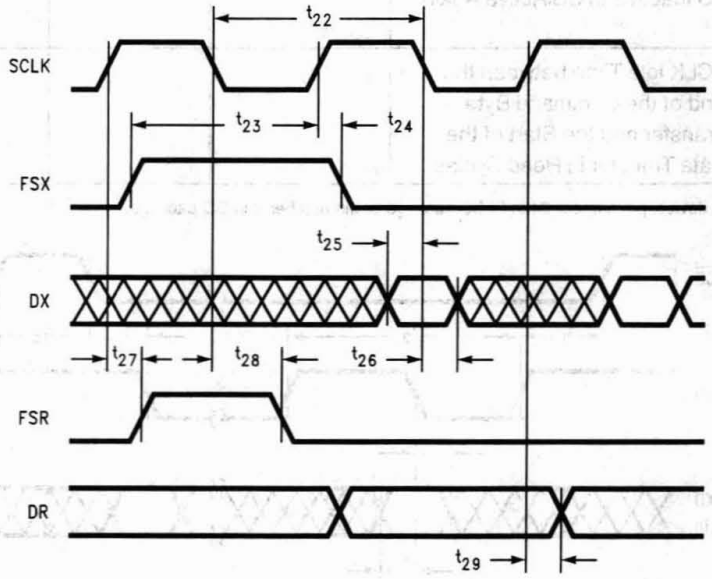
2.0 Electrical Specifications (Continued)

2.3 DIGITAL SWITCHING CHARACTERISTICS The following specifications apply to the LM12434 and LM12{L}438 for $V_A+ = V_D+ = 5V$ {3.3V}, AGND = DGND = 0V, C_L (load capacitance) on output lines = 80 pF unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX},** all other limits for $T_A = T_J = 25°C$. (Notes 6, 7, and 9) (Continued)

2.3.3 TMS320 Interface Mode

Symbol (See *Figure* Below)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
t_{22}	SCLK (Serial Clock) Period			**125** {**167**}	ns (min)
t_{23}	FSX Set-Up Time to SCLK High			**30** {**50**}	ns (min)
t_{24}	FSX Hold Time from SCLK High			**10**	ns (min)
t_{25}	Data in (DX) Set-Up Time to SCLK Low			**0**	ns (min)
t_{26}	Data in DX Hold Time from SCLK Low			**30** {**120**}	ns (min)
t_{27}	FSR High from SCLK High			**80** {**100**}	ns (max)
t_{28}	FSR Low from SCLK Low			**120**	ns (max)
t_{29}	SCLK High to Data Out (DR) Change			**90**	ns (max)



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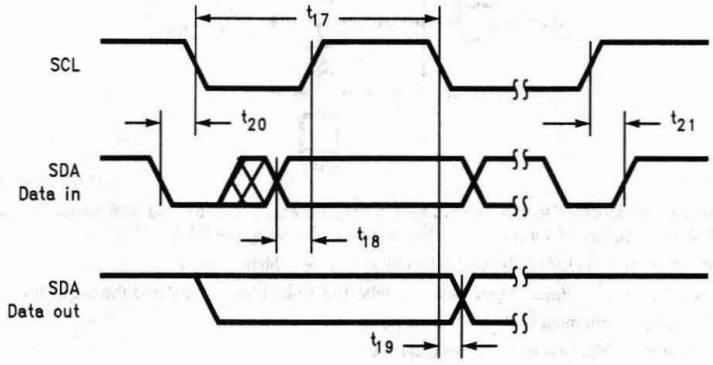
2.0 Electrical Specifications (Continued)

2.3 DIGITAL SWITCHING CHARACTERISTICS The following specifications apply to the LM12434 and LM12{L}438 for $V_A+ = V_D+ = 5V$ {3.3V}, AGND = DGND = 0V, C_L (load capacitance) on output lines = 80 pF unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX},** all other limits for $T_A = T_J = 25°C$. (Notes 6, 7, and 9) (Continued)

2.3.4 I²C Bus Interface

The switching characteristics of the LM12434/8 for I²C bus interface fully meets or exceeds the published specifications of the I²C bus. The following parameters given here are the timing relationships between SCL and SDA signals related to the LM12434/8. They are not the I²C bus specifications.

Symbol (See *Figure* Below)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
t_{17}	SCL (Clock) Period			**2500 {10000}**	ns (min)
t_{18}	Data in Set-Up Time to SCL High			**30**	ns (min)
t_{19}	Data Out Stable after SCL Low			**900 {1400}**	ns (max)
t_{20}	SDA Low Set-Up Time to SCL Low (Start Condition)			**40**	ns (min)
t_{21}	SDA High Hold Time after SCL High (Stop Condition)			**40**	ns (min)



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2.0 Electrical Specifications (Continued)

2.4 NOTES ON SPECIFICATIONS

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

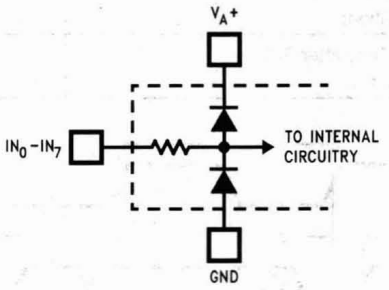
Note 2: All voltages are measured with respect to GND, unless otherwise specified. GND specifies either AGND and/or DGND and V^+ specifies either V_A^+ and/or V_D^+.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > (V_A^+ or V_D^+)), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 150°C, and the typical thermal resistance (Θ_{JA}) of the V package, when board mounted, is 70°C/W and in the WM package, when board mounted, is 60°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to each analog input through a series resistor, as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage the part. However, errors in the A/D conversion can occur if these diodes are forward biased by more than 100 mV. As an example, if V_A^+ is 4.5 V_{DC}, the full-scale input voltage must be ≤4.6 V_{DC} to ensure accurate conversions.



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Note 7: V_A^+ and V_D^+ must be connected together to the same power supply voltage and bypassed with separate capacitors at each V^+ pin to assure conversion/comparison accuracy. Refer to Section 8.0 for a detailed discussion on grounding the DAS.

Note 8: Accuracy is guaranteed when operating the LM12434/LM12{L}438 at f_{CLK} = 8 MHz {6 MHz}.

Note 9: With the test condition for V_{REF} ($V_{REF+} - V_{REF-}$) given as +4.096V, the 12-bit LSB is 1 mV and the 8-bit/"Watchdog" LSB is 19 mV.

Note 10: Typicals are at T_A = 25°C and represent most likely parametric norm.

Note 11: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error the straight line passes through negative full-scale and zero. (See *Figures 5b* and *5c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between −1 to 0 and 0 to +1 (see *Figure 6*).

Note 14: The DC common-mode error is measured with both the inverted and non-inverted inputs shorted together and driven from 0V to 5V {3.3V}. The measured value is referred to the resulting output value when the inputs are driven with a 2.5V {1.65V} signal.

Note 15: Power Supply Sensitivity is measured after Auto-Zero and/or Auto-Calibration cycle has been completed with V_A^+ and V_D^+ at the specified extremes.

Note 16: V_{REFCM} (Reference Voltage Common Mode Range) is defined as ($V_{REF+} + V_{REF-}$)/2. See *Figures 3* and *4*.

Note 17: The device self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.10 LSB.

Note 18: The Throughput Rate is for a single instruction repeated continuously while reading data during conversions with a serial clock frequency f_{SCLK} = 10 MHz {8 MHz}. Sequencer states 0 (1 clock cycle), 1 (1 clock cycle), 7 (9 clock cycles) and 5 (44 clock cycles) are used (see *Figure 10*) for a total of 56 clock cycles per conversion. The Throughput Rate is f_{CLK} (MHz)/N, where N is the number of clock cycles/conversion.

Note 19: See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Note 20: Each input referenced to the other input sees a ±4.096V (8.192 V_{p-p}) sine wave. However the voltage at each input stays within the supply rails. This is done by applying two sine waves with 180° phase shift and 4.096 V_{p-p} (between GND and V_A^+) to the inputs.

Note 21: Multiplexer channel-to-channel crosstalk is measured by placing a sinewave with a frequency of f_{IN} = 5 kHz on one channel and another sinewave with a frequency of $f_{CROSSTALK}$ = 40 kHz on the remaining channels. 8192 conversions are performed on the channel with the 5 kHz signal. A special response is generated by doing a FFT on these samples. The crosstalk is then calculated by subtracting the amplitude of the frequency component at 40 kHz from the amplitude of the fundamental frequency at 5 kHz.

Note 22: Interrupt 7 is set to return an out-of-standby flag 10 ms (typ) after the device is requested to come out of standby mode. However, characterization has shown the devices will perform to their rated specifications in 2 ms.

3.0 Electrical Characteristics

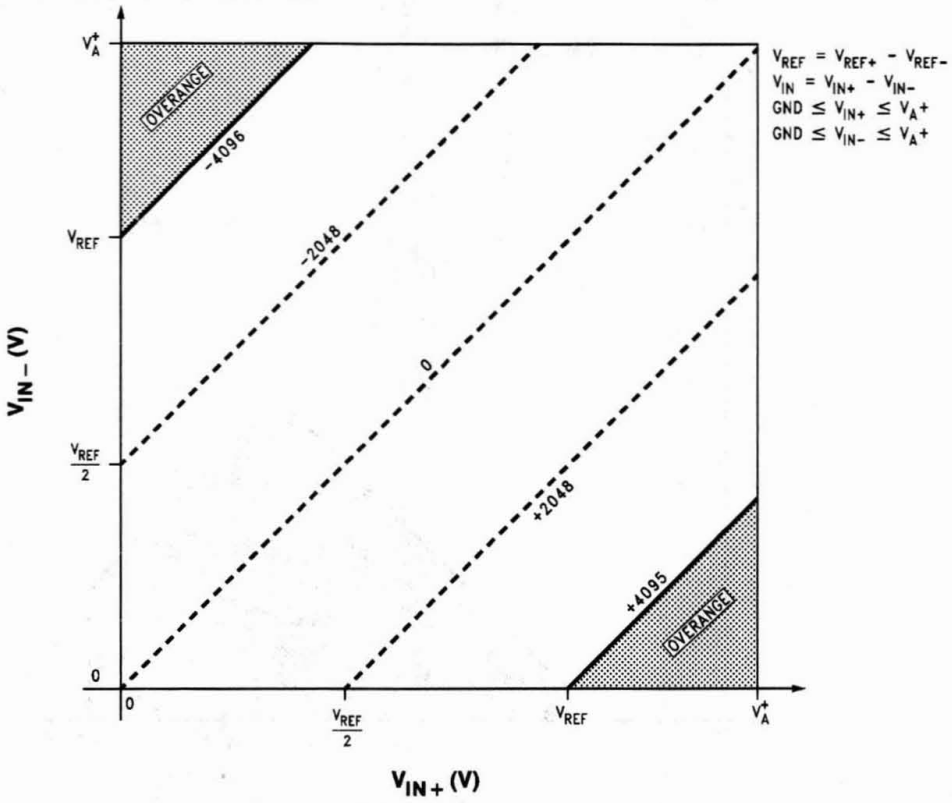

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FIGURE 1. Output Digital Code vs the Operating Input Voltage Range (General Case)

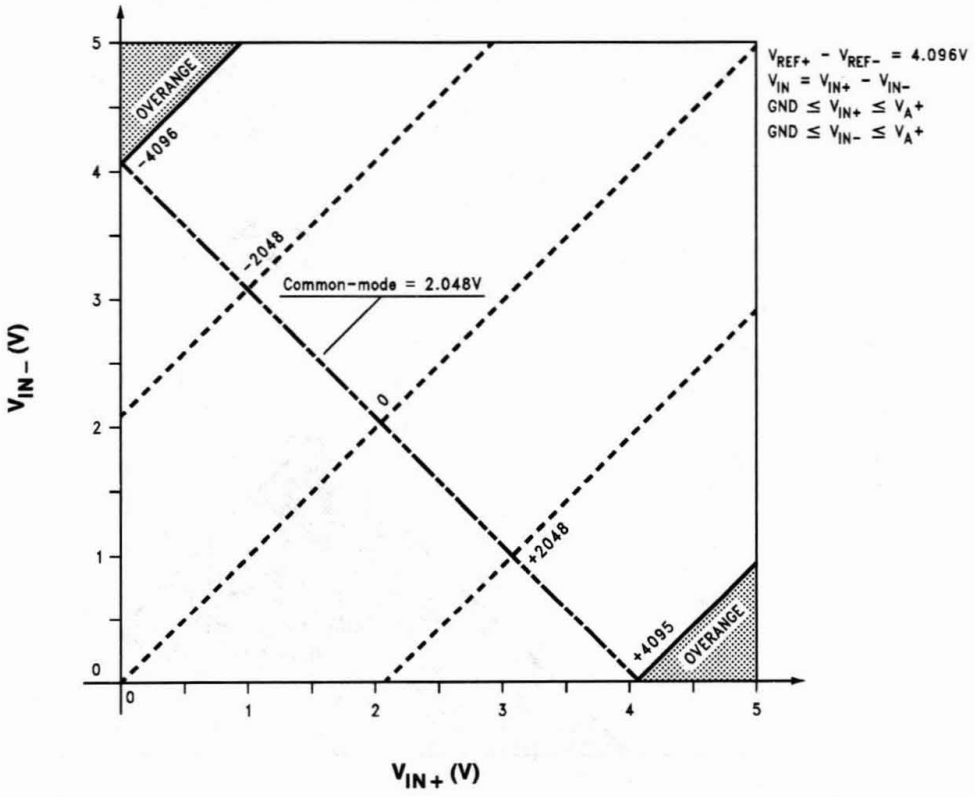

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FIGURE 2. Output Digital Code vs the Operating Input Voltage Range for $V_{REF} = 4.096V$

3.0 Electrical Characteristics (Continued)

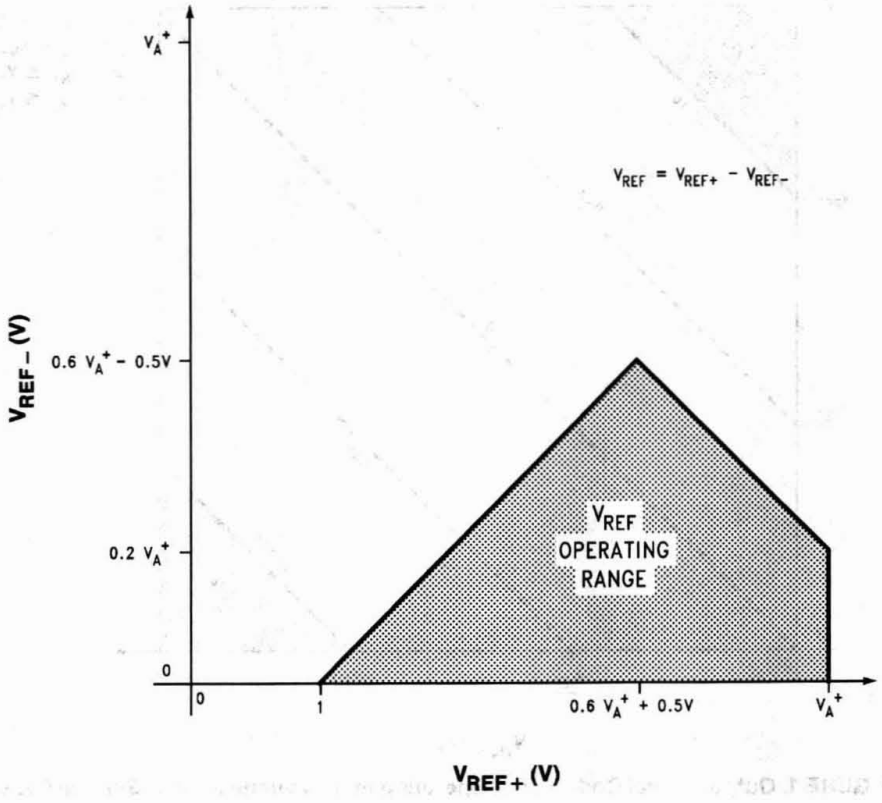

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FIGURE 3. V_{REF} Operating Range (General Case)

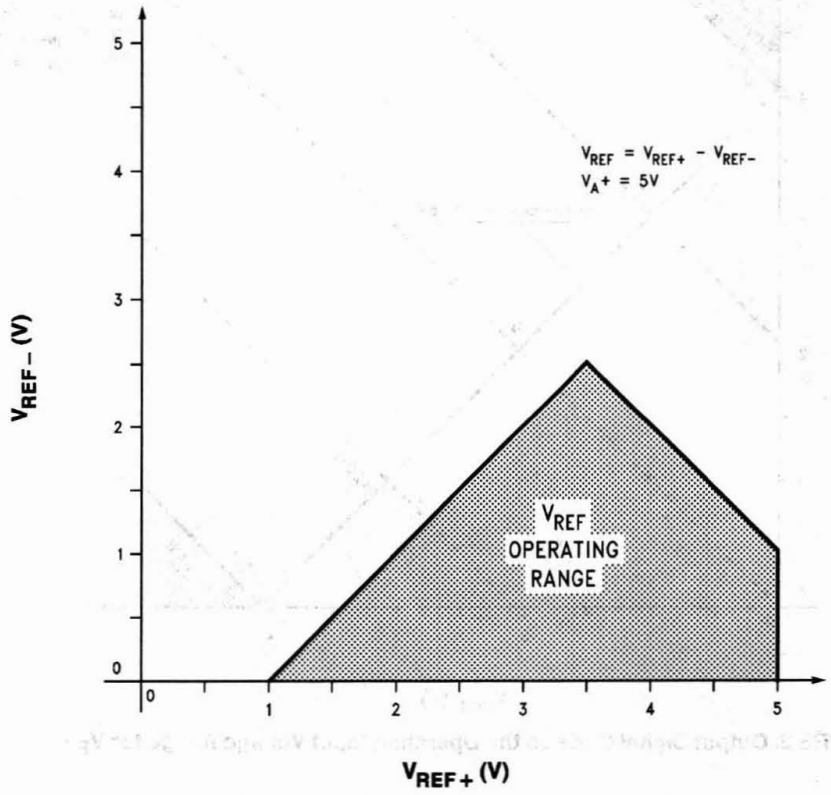

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FIGURE 4. V_{REF} Operating Range for $V_A^+ = 5V$

3.0 Electrical Characteristics (Continued)

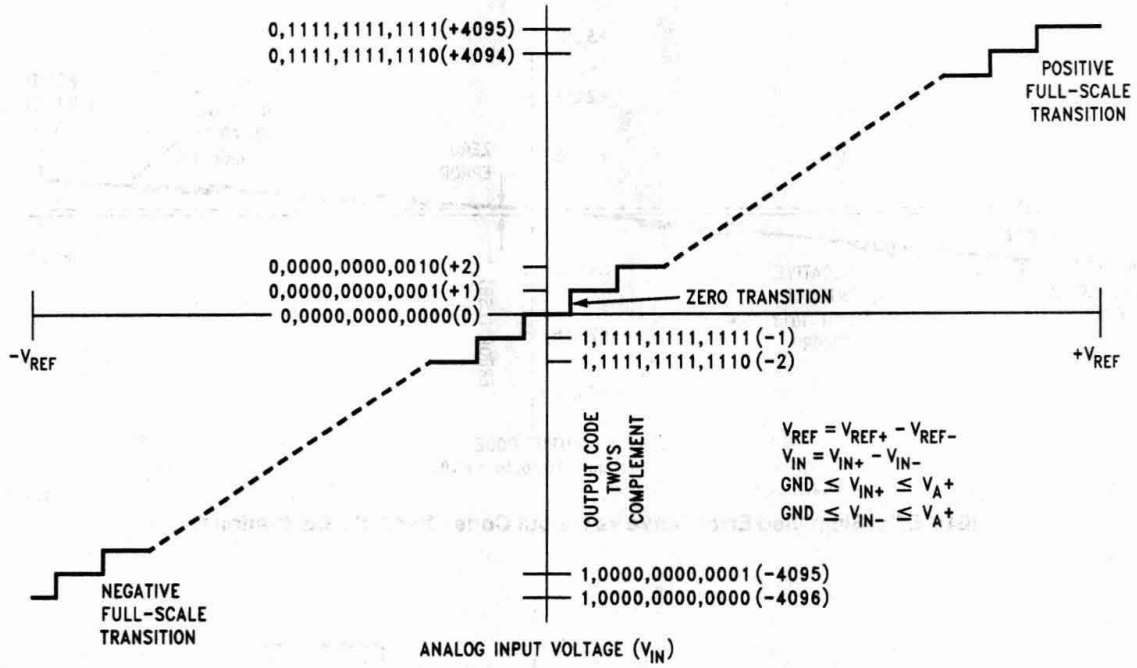

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FIGURE 5a. Transfer Characteristic

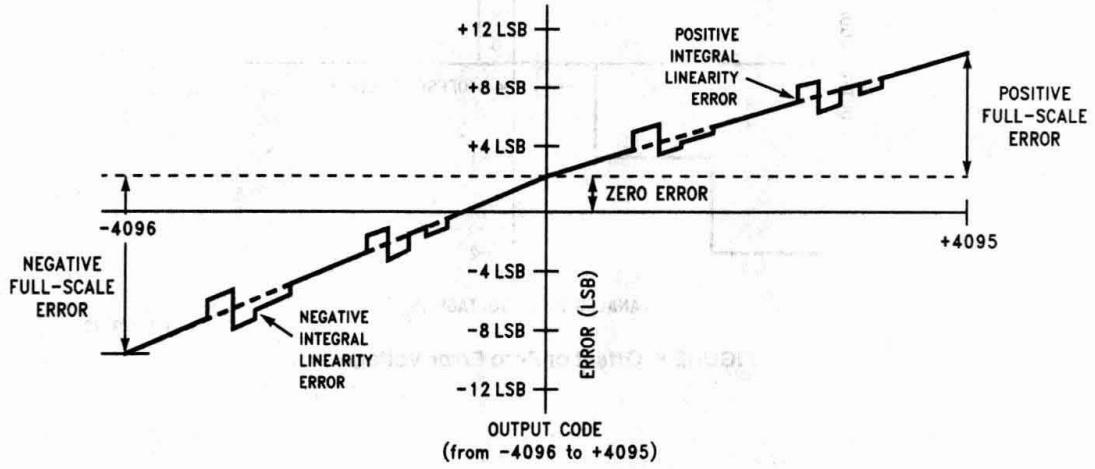

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FIGURE 5b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

3.0 Electrical Characteristics (Continued)

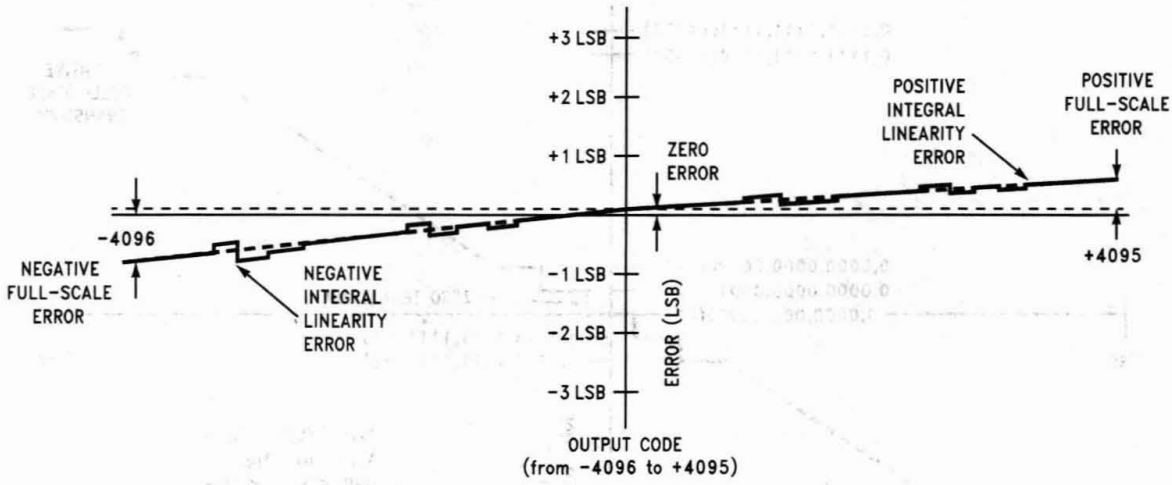

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FIGURE 5c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

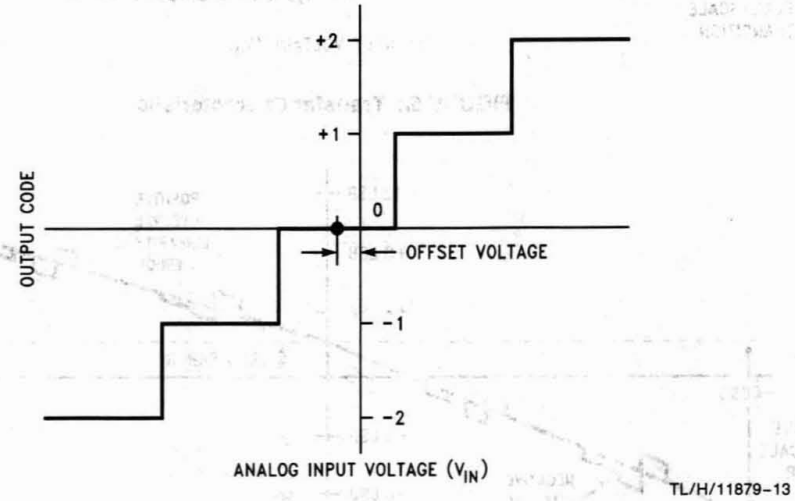

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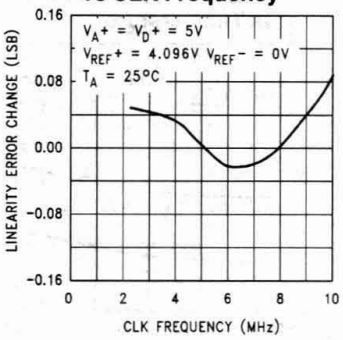
FIGURE 6. Offset or Zero Error Voltage

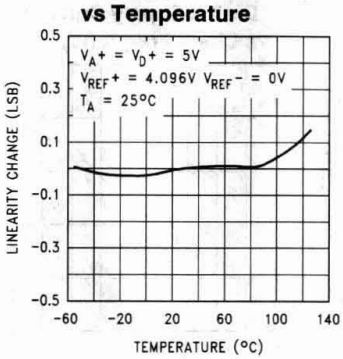
4.0 Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9)

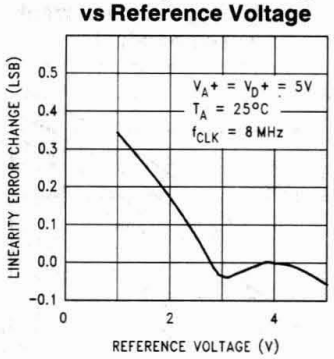
Linearity Error Change vs CLK Frequency



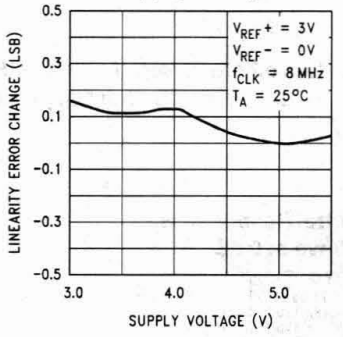
Linearity Error Change vs Temperature



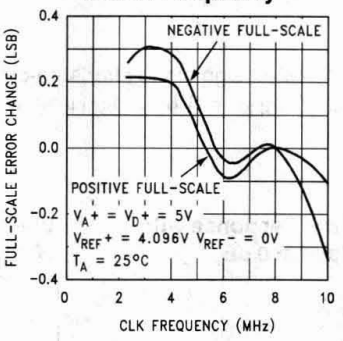
Linearity Error Change vs Reference Voltage



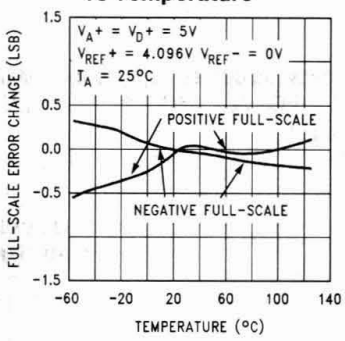
Linearity Error Change vs Supply Voltage



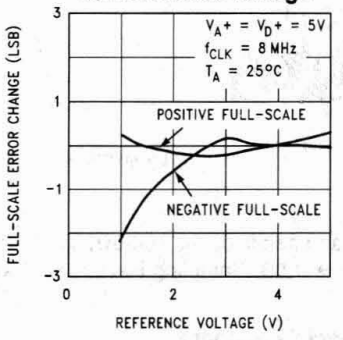
Full-Scale Error Change vs CLK Frequency



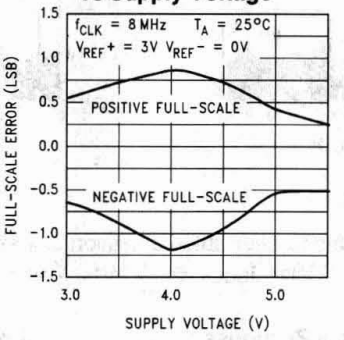
Full-Scale Error Change vs Temperature



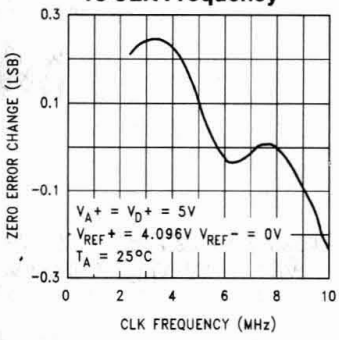
Full-Scale Error Change vs Reference Voltage



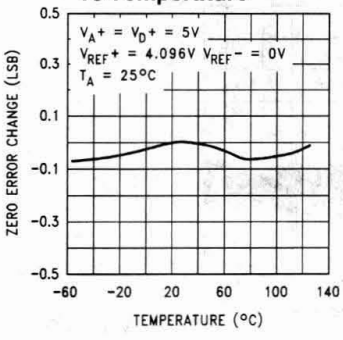
Full-Scale Error vs Supply Voltage



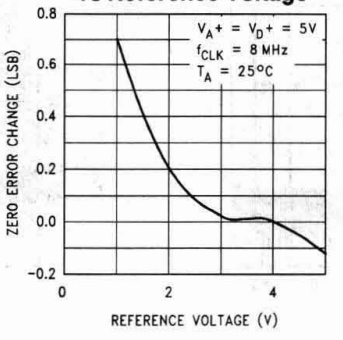
Zero Error Change vs CLK Frequency



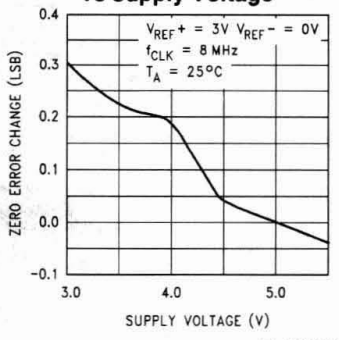
Zero Error Change vs Temperature



Zero Error Change vs Reference Voltage



Zero Error Change vs Supply Voltage



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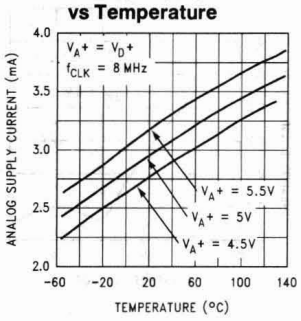
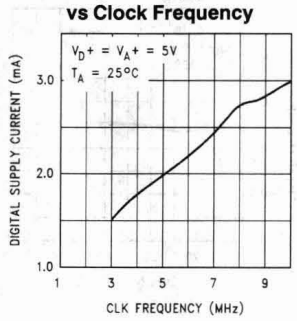
4.0 Typical Performance Characteristics (Continued)

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9)

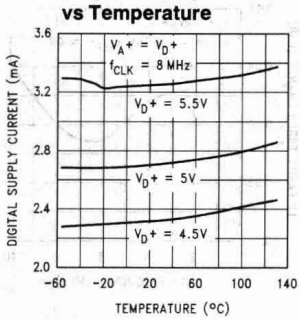
Analog Supply Current vs Temperature



***Digital Supply Current vs Clock Frequency**



***Digital Supply Current vs Temperature**



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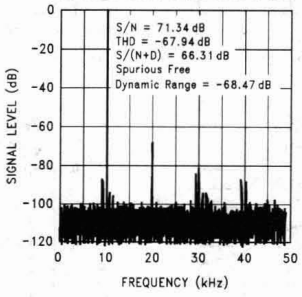
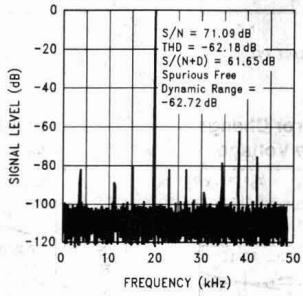
*Free-running conversion and SPI mode data read at 200 ns SCLK period.

The following curves apply to the LM12L438 in 12-bit + sign mode after auto-calibration unless otherwise specified. R_S = 50Ω, T_A = 25°C, $V_A^+ = V_D^+$ = 3.3V, V_{REF} = 2.5V, f_{CLK} = 6 MHz, f_{SCLK} = 8 MHz, V_{IN} = 2.5V → 0 dB, Sampling Rate = 100 kHz.

Unipolar Spectral Response with 10 kHz Sine Wave at 0 dB



Unipolar Spectral Response with 20 kHz Sine Wave at 0 dB



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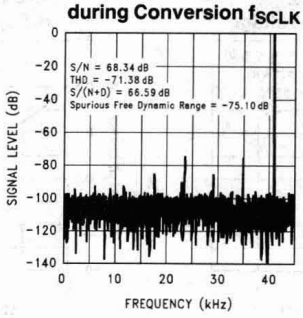
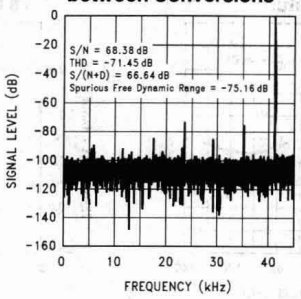
The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. R_S = 50Ω, T_A = 25°C, $V_A^+ = V_D^+$ = 5V, V_{REF} = 4.096V, f_{CLK} = 8 MHz, f_{SCLK} = 10 MHz, V_{IN} = 4.096V → 0 dB, Sampling Rate = 100 kHz.

Unipolar Special Response with 41.2 kHz Sine Wave at 0 dB Reading Data during Conversion f_{SCLK} = 10 MHz



Unipolar Special Response with 41.2 kHz Sine Wave at 0 dB Reading Data between Conversions

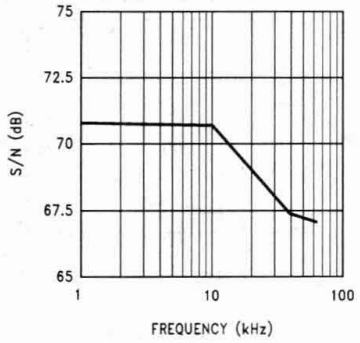


TL/H/11879–55

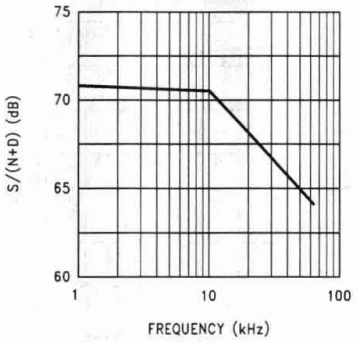
4.0 Typical Performance Characteristics (Continued)

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. $R_S = 50\Omega$, $T_A = 25°C$, $V_A^+ = V_D^+ = 5V$, $V_{REF} = 4.096V$, $f_{CLK} = 8$ MHz, $f_{SCLK} = 10$ MHz, $V_{IN} = 4.096V \rightarrow 0$ dB, Sampling Rate = 133.3 kHz.

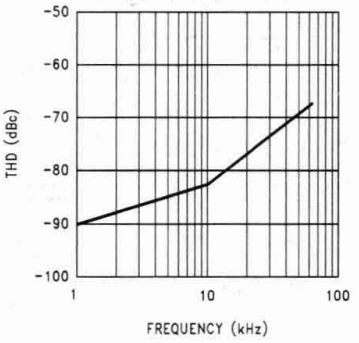
Unipolar Signal-to-Noise Ratio vs Input Frequency



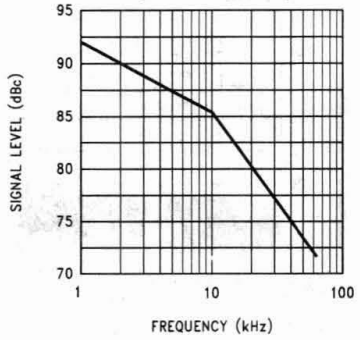
Unipolar Signal-to-Noise + Distortion vs Input Frequency



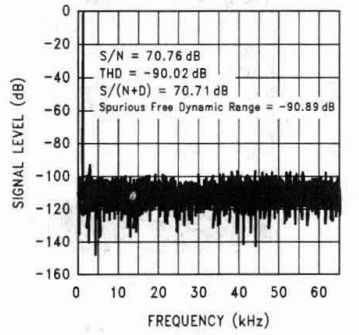
Unipolar Total Harmonic Distortion vs Input Frequency



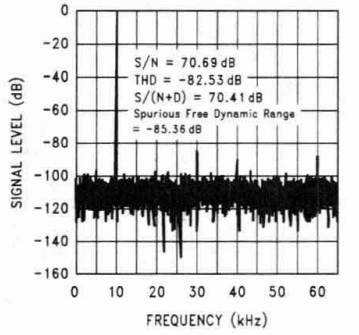
Unipolar Spurious Free Dynamic Range vs Input Frequency



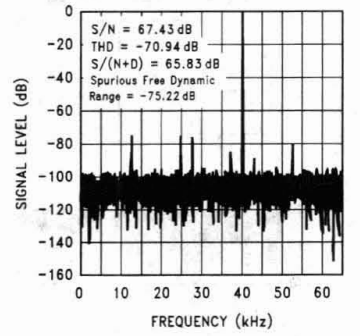
Unipolar Spectral Response with 1.025 kHz Sine Wave at 0 dB



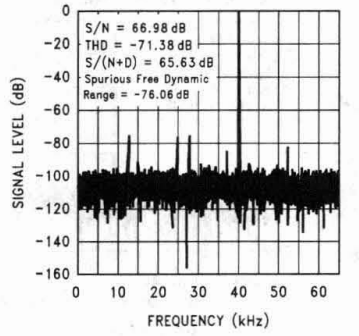
Unipolar Spectral Response with 10.010 kHz Sine Wave at 0 dB



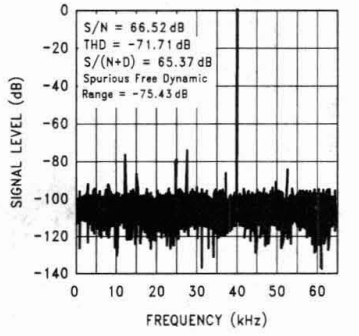
Unipolar Spectral Response with 40.283 kHz Sine Wave at 0 dB



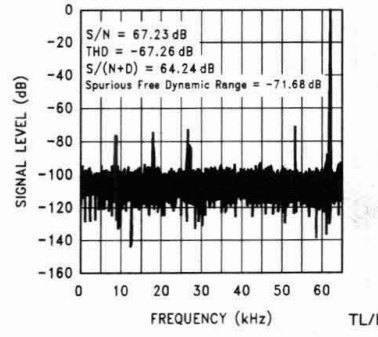
Unipolar Spectral Response with 40.283 kHz Sine Wave at −0.5 dB



Unipolar Spectral Response with 40.283 kHz Sine Wave at −1.0 dB



Unipolar Spectral Response with 62.256 kHz Sine Wave at 0 dB



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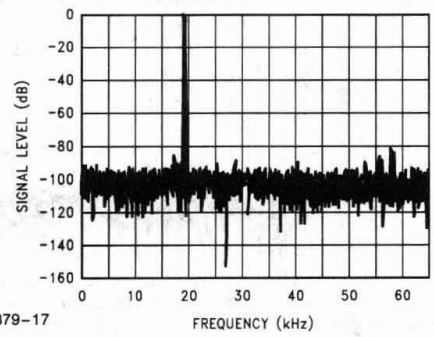
Unipolar Two Tone Spectral Response with f1 = 19.190 kHz and f2 = 19.482 kHz Sine Wave



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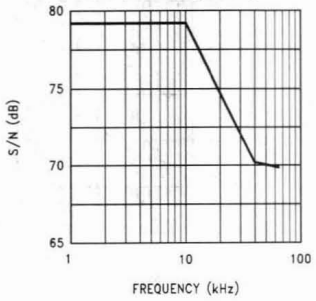
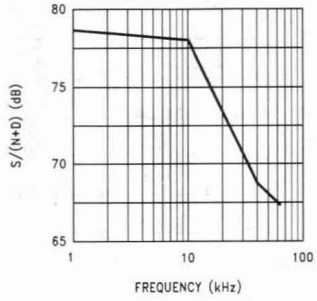
4.0 Typical Performance Characteristics (Continued)

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. $R_S = 50\Omega$, $T_A = 25°C$, $V_A^+ = V_D^+ = 5V$, $V_{REF} = 4.096V$, $f_{CLK} = 8$ MHz, $f_{SCLK} = 10$ MHz, $V_{IN} = \pm 4.096V \rightarrow 0$ dB, Sampling Rate = 133.3 kHz.

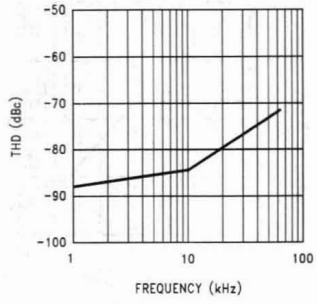
Bipolar Signal-to-Noise Ratio vs Input Frequency



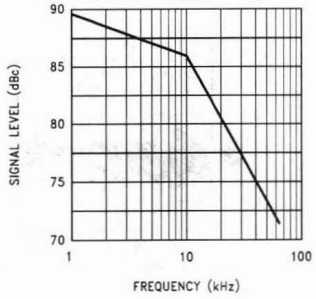
Bipolar Signal-to-Noise + Distortion vs Input Frequency



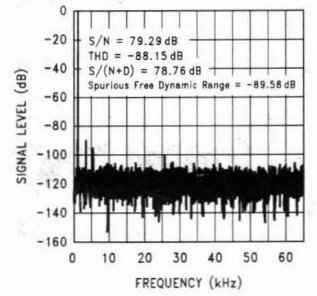
Bipolar Total Harmonic Distortion vs Input Frequency



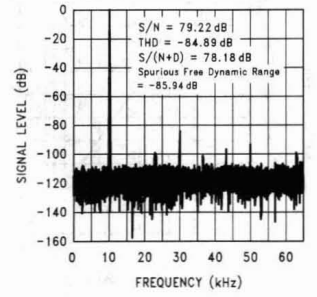
Bipolar Spurious Free Dynamic Range vs Input Frequency



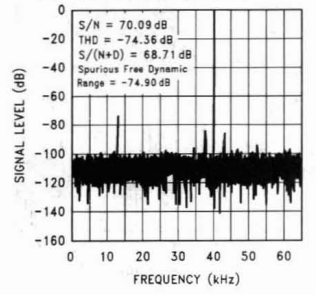
Bipolar Spectral Response with 1.025 kHz Sine Wave at 0 dB



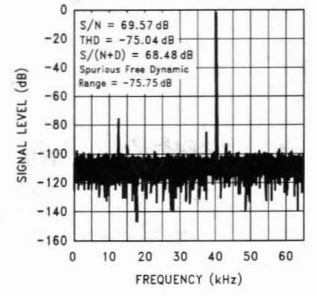
Bipolar Spectral Response with 10.010 kHz Sine Wave at 0 dB



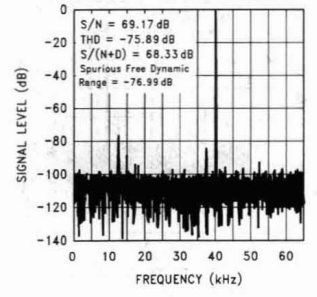
Bipolar Spectral Response with 40.283 kHz Sine Wave at 0 dB



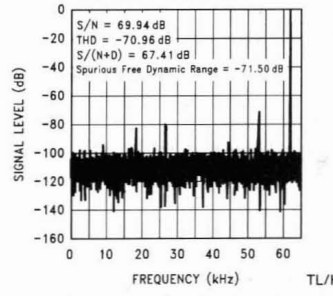
Bipolar Spectral Response with 40.283 kHz Sine Wave at −0.5 dB



Bipolar Spectral Response with 40.283 kHz Sine Wave at −1.0 dB



Bipolar Spectral Response with 62.25 kHz Sine Wave at 0 dB



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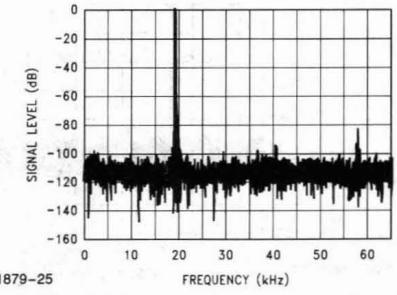
Bipolar Two Tone Spectral Response with f1 = 19.190 kHz and f2 = 19.482 kHz Sine Waves



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5.0 Pin Descriptions

TABLE I. LM12{L}438 Pin Description

Pin Number		Pin Name	Description
PLCC Pkg.	SO Pkg.		
1	7	DGND	Digital ground. This is the device's digital supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.
2 3 4 5 6 7 8 9	8 9 10 11 12 13 14 15	IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7	These are the eight analog inputs to the multiplexer. For each conversion to be performed, the active channels are selected according to the instruction RAM programming. Any individual channel can be selected for a single-ended conversion referenced to AGND, or any pair of channels, whether adjacent or non adjacent, can be selected as a fully differential input pairs.
10	16	V_{REF}^+	Positive reference input. The operating voltage range for this input is $1V \leq V_{REF}^+ \leq V_A^+$ (See *Figures 3* and *4*). In order to achieve 12-bit performance this pin should be by passed to AGND at least with a parallel combination of a 10 μF and a 0.1 μF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
11	17	V_{REF}^-	Negative reference input. The operating voltage range for this input is $0\ V \leq V_{REF}^- \leq V_{REF}^+ - 1V$ (See *Figures 3* and *4*). In order to achieve 12-bit performance, this pin should be bypassed to AGND at least with a parallel combination of a 10 μF and a 0.1 μF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
12	18	AGND	Analog ground. This is the device's analog supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.
13	19	V_A^+	Analog supply. This is the supply connection for the analog circuitry. The device operating supply voltage range is +3.0V to +5.5V. Accuracy is guaranteed only if the V_A^+ and V_D^+ are connected to the same potential. In order to achieve 12-bit performance, this pin should be bypassed to AGND at least with a parallel combination of a 10 μF and a 0.1 μF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
14	20	DGND	Digital ground. See above definition.
15 16	21 22	V_D^+	Digital supply. This is the supply connection for the analog circuitry. The device operating supply voltage range is +3.0V to +5.5V. The device accuracy is guaranteed only if the V_A^+ and V_D^+ are connected to the same potential. In order to achieve 12-bit performance this pin should be by passed to DGND at least with a parallel combination of a 10 μF and a 0.1 μF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
17	23	P5	P1–P5 are the multi-function serial interface input or output pins that have different assignments depending on the selected mode. Serial interface input: Standard: SCLK 8051: TXD I²C: SCL TMS320: DR
18	24	P4	Serial interface input/output: Standard: DO 8051: RXD I²C: SDA TMS320: DR
19	25	P3	Serial interface input: Standard: DI 8051: CS I²C: SAD2 TMS320: DX

5.0 Pin Descriptions (Continued)

TABLE I. LM12{L}438 Pin Description (Continued)

Pin Number		Pin Name	Description		
PLCC Pkg.	SO Pkg.				
20	26	P2	Serial interface input:	Standard:	CS
				8051:	1
				I^2C:	SAD1
				TMS320:	FSX
21	27	P1	Serial interface input:	Standard:	$\overline{R}$/F (Clock rise/fall)
				8051:	1
				I^2C:	SAD0
				TMS320:	FSR
22 23	28 1	MODESEL2 MODESEL1	Serial mode selection inputs. The logic states of these inputs determine the operation of the serial mode as shown below. The standard mode covers the National's MICROWIRE, Motorola's SPI and Hitachi's SCI protocols. MODESEL1, MODESEL2: 01 Standard mode 00 8051 10 I^2C 11 TMS320		
24	2	CLK	The device main clock input. The operating range of clock frequency is 0.05 MHz to 10.0 MHz. The device accuracy is guaranteed only for the clock frequencies indicated in the specification tables.		
25	3	$\overline{INT}$	Interrupt output. This is an active low output. An interrupt is generated any time a non-masked interrupt condition takes place. There are seven different conditions that can generate an interrupt. (Refer to Section 6.2.4). The interrupt is set high (inactive) by reading the interrupt status register. This output can drive up to 100 pF of capacitive loads. An external buffer should be used for driving higher capacitive loads.		
26	4	SYNC	Synchronization input/output. SYNC is an input if the Configuration Register's SYNC I/O bit is "0" and output when the bit is "1". When sync is an input, a rising edge on this pin causes the internal S/H to hold the input signal and a conversion cycle or a comparison cycle (depending on the programmed instruction) to be started. (The conversion or comparison actually begins on the rising edge of the CLK immediately following the rising edge of sync.) When output, it goes high at the start of a conversion or a comparison cycle and returns low when the cycle is completed. At power up the SYNC pin is set as an input. When used as an output it can drive up to 100 pF of capacitive loads. An external buffer should be used for driving higher capacitive loads.		
27	5	$\overline{STANDBYOUT}$	Stand-by output. This is an active low output. $\overline{STANDBYOUT}$ will be activated when the LM12{L}438 is put into stand-by mode through the Configuration Register's stand-by bit. It is used to force any other devices in the system (signal conditioning circuitry, for example) to go into power-down mode. This is done by connecting the "shutdown", "powerdown", "standby", etc. pins of the other ICs to $\overline{STANDBYOUT}$. In those cases where the peripheral ICs do not have the power-down inputs, $\overline{STANDBYOUT}$ can be used to turn off their power through an electronic switch. Note that the logic polarity of the $\overline{STANDBYOUT}$ is the opposite to that of the stand-by bit in the Configuration Register.		
28	6	V_D+	Digital supply. See above definition.		
LM12434 Pin Description (Same As LM12{L}438 with the exception of the following pins.)					
6 7	12 13	MUXOUT− MUXOUT+	Multiplexer outputs. These are the LM12434's externally available analog MUX output pins. Analog inputs are directed to these outputs based on the Instruction RAM programming.		
8 9	14 15	S/H IN− S/H IN+	Sample-and-hold inputs. These are the inverting and non-inverting inputs of the sample-and-hold. LM12434 allows external analog signal conditioning circuits to be placed between MUX outputs and S/H inputs.		

6.0 Operational Information

6.1 FUNCTIONAL DESCRIPTION

The LM12434 and LM12{L}438 are multi-functional Data Acquisition Systems that include a fully differential 12-bit-plus-sign self-calibrating analog-to-digital converter (ADC) with a two's-complement output format, an 8-channel (LM12{L}438) or a 4-channel (LM12434) analog multiplexer, a first-in-first-out (FIFO) register that can store 32 conversion results, and an Instruction RAM that can store as many as eight instructions to be sequentially executed. The LM12434 also has a differential multiplexer output and a differential S/H input. All of this circuitry operates on only a single +5V power supply. For simplicity, the DAS (Data Acquisition System) abbreviation is used as a generic name for the members of the LM12434 and LM12{L}438 family thoughout this discussion.

Figure 7 illustrates the functional block diagram or user programming model of the DAS. Note that this diagram is not meant to reflect the actual implementation of the internal building blocks. The model consists of the following blocks:

— A flexible analog multiplexer with differential output at the front end of the device.

— A fully-differential, self-calibrating 12-bit + sign ADC converter with sample and hold.

— A 32-word FIFO register as the output data buffer.

— An 8-word instruction RAM that can be programmed to repeatedly perform a series of conversions and comparisons on selected input channels.

— A series of registers for overall control and configuration of DAS operation and indication of internal operational status.

— Interrupt generation logic to request service from the processor under specified conditions.

— Serial interface logic for input/output operations between the DAS and the processor. All the registers shown in the diagram can be read and most of them can also be written to by the user through the input/output block.

— A controller unit that manages the interactions of the different blocks inside the DAS and controls the conversion, comparison and calibration sequences.

The DAS has 3 different modes of operation:

— 12-bit + sign conversion

— 8-bit + sign conversion

— 8-bit + sign comparison (also called "watchdog" mode)

The fully differential 12-bit-plus-sign ADC uses a charge redistribution topology that includes calibration capabilities. Charge re-distribution ADCs use a capacitor ladder in place of a resistor ladder to form an internal DAC. The DAC is used by a successive approximation register to generate intermediate voltages between the voltages applied to V_{REF}^- and V_{REF}^+. These intermediate voltages are compared against the sampled analog input voltage as each bit is charged.

Conversion accuracy is ensured by an internal auto-calibration system. Two different calibration modes are available; one compensates for offset voltage, or zero error, while the other corrects the ADC's linearity and offset errors.

When correcting offset only, the offset error is measured once and a correction coefficient is created. During the full calibration, the offset error is measured eight times, averaged, and a correction coefficient is created. After completion of either calibration mode, the offset correction coefficient is stored in an internal offset correction register.

The LM12434 and LM12{L}438's overall linearity correction is achieved by correcting the internal DAC's capacitor mismatch. Each capacitor is compared eight times against all remaining smaller value capacitors and any errors are averaged. A correction coefficient is then created and stored in one of the thirteen linearity correction registers. A state machine, using patterns stored in 16-bit x 8-bit ROM, executes each calibration algorithm.

Once the converter has been calibrated, an arithmetic logic unit (ALU) uses the offset correction coefficient and the 13 linearity correction coefficients to reduce the conversion's offset error and linearity error, in the background, during the 12-bit + sign conversion. 8-bit + sign conversions and "watchdog" comparisons use only the offset coefficient. An 8-bit + sign conversion requires less than half the time needed for a 12-bit + sign conversion.

Diagnostic Mode

A diagnostic mode is available that allows verification of the LM12{L}438's operation. The diagnostic mode is disabled in the LM12434. This mode internally connects the voltages present at the V_{REF}^+ and V_{REF}^- pins to the internal V_{IN}^+ and V_{IN}^- S/H inputs. This mode is activated by setting the Diagnostic bit (Bit 11) in the Configuration register to a "1". More information concerning this mode of operation can be found in Section 6.2.2.

Watchdog Mode

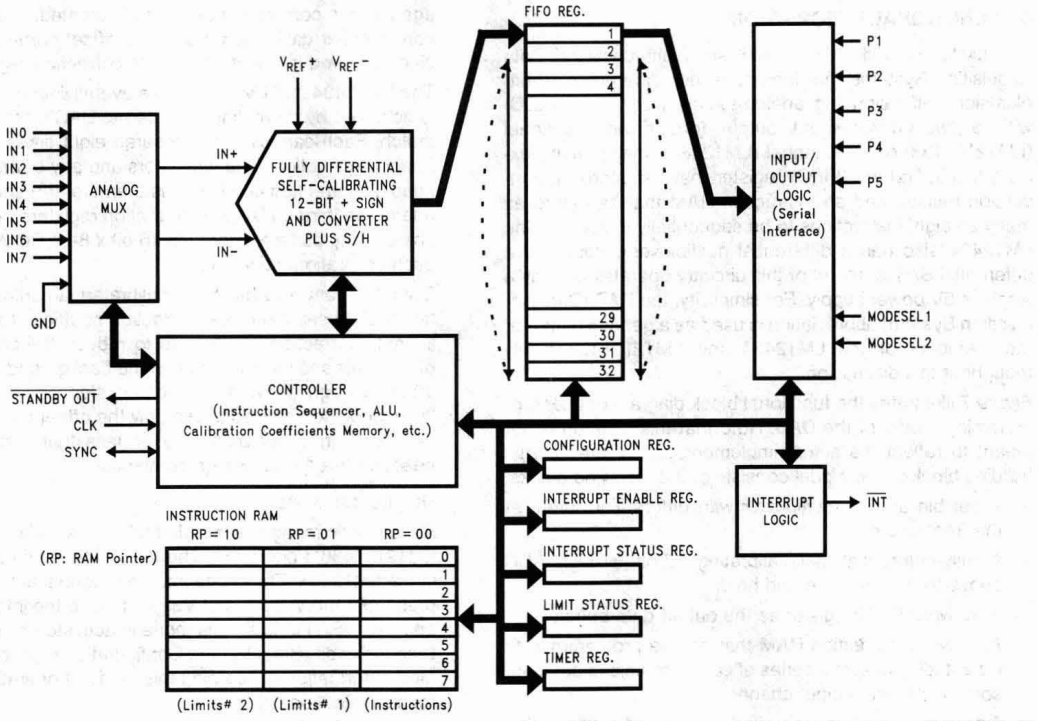
In the watchdog mode no conversion is performed, but the DAS samples an input and compares it with the values of the two limits stored in the Instruction RAM. If the input voltage is above or below the limits (as defined by the user) an interrupt can be generated to indicate a fault condition. The LM12434 and LM{L}438's "watchdog" mode is used to monitor a single-ended or differential signal's amplitude and generate an output if the signal's amplitude falls outsidde of a programmable "window". Each watchdog instruction includes two limits. An interrupt can be generated if the input signal is above or below either of the two limits. This allows interrupt to be generated when analog voltage inputs are "outside the window". After a "watchdog" mode interrupt, the processor can then request a conversion on the input signal and read the signal's magnitude.

Analog Input Multiplexer

The analog input multiplexer can be configured for any combination of single-ended or fully differential operation. Each input is referenced to AGND when a multiplexer channel operates in the single-ended mode. Fully differential analog input channels are formed by pairing any two channels together.

The LM12434's multiplexer outputs and S/H inputs (MUXOUT+, MUXOUT− and S/H IN+, S/H IN−) provide the option for additional analog signal processing after the multiplexer. Fixed-gain amplifiers, programmable-gain amplifiers, filters, and other processing circuits can operate on the multiplexer output signals before they are applied to the ADC's S/H inputs. If external processing is not used, connect MUXOUT+ to S/H IN+ and MUXOUT− to S/H IN−.

6.0 Operational Information (Continued)



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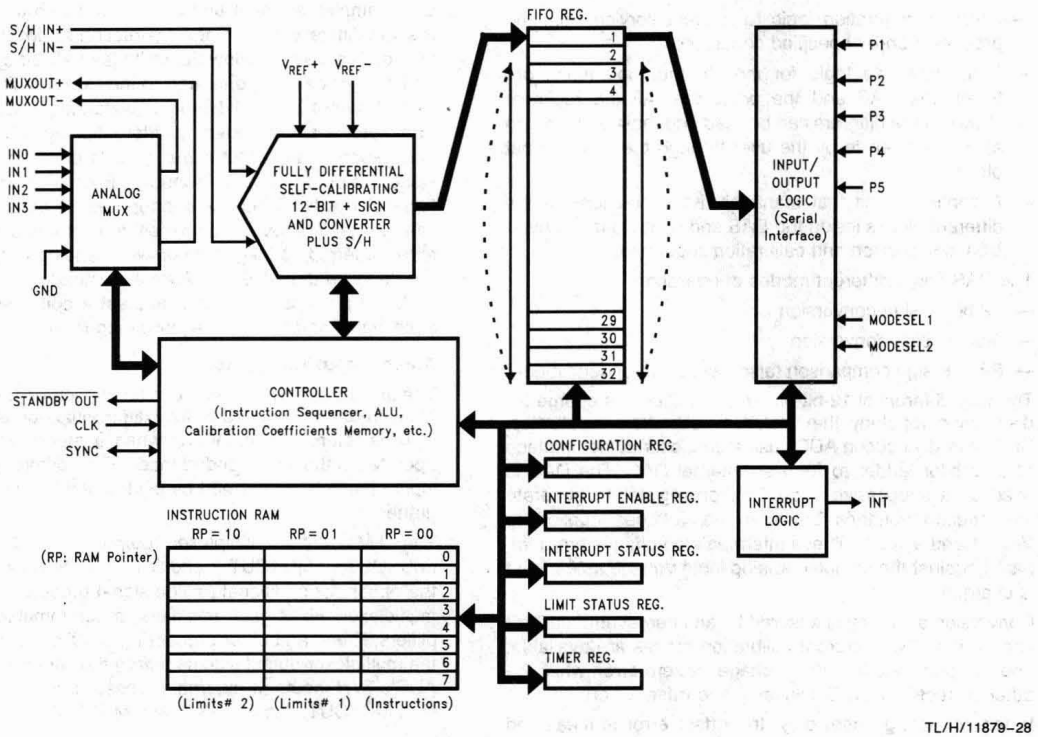
(a) The LM12{L}438



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(b) The LM12434

FIGURE 7. The LM12{L}438 and LM12434 Functional Block Diagram (Programming Model)

6.0 Operational Information (Continued)

Acquisition Time

The LM12434 and LM12{L}438's internal S/H is designed to operate at its minimum acquisition time (1.125 [1.5] μs for a 12-bit + sign conversion) when the source impedance, R_S, is less than or equal to 60 {80} Ω ($f_{CLK} \leq 8$ {6} MHz). When 60 {80} $\Omega < R_S \leq 4.17$ {5.56} kΩ, the internal S/H's acquisition time can be increased to a maximum of 4.88 {6.5} μs (12 + sign bits, $f_{CLK} = 8$ {6} MHz) to provide sufficient time for the sampling capacitor to charge. See Section 6.2.1 (Instruction RAM "00") Bits 12–15 for more information.

Instruction Register

The INSTRUCTION RAM is divided into 8 separate words, each with 48 (3 x 16) bit length. Each word is separated into three 16-bit sections. Each word has a unique address and different sections of the instruction word are selected by the 2-bit RAM pointer (RP) in the configuration register. As shown in *Figure 7*, the Instruction RAM sections are labeled Instructions, Limits #1 and Limits #2. The Instruction section holds operational (12-bit + sign, 8-bit + sign or watchdog) information such as the input channels to be selected, the mode of operation to be performed for each instruction, and the duration of the acquisition period. The other two sections are used in the watchdog mode and the user-defined limits are stored in them. Each watchdog instruction has 2 limits associated with it (usually a low limit and a high limit, but two low limits or two high limits may be programmed instead). The DAS starts executing from instruction 0 and moves through the next instructions up to any user-specified instruction and then "loop back" to instruction 0. It is not necessary to execute all 8 instructions in the instruction loop. The cycle may be repeatedly executed until stopped by the user. The processor should access the Instruction RAM only when the instruction sequencer is stopped.

FIFO Register

The FIFO Register stores the conversion results. This register is "Read only" and all the locations are accessed through a single address. Each time a conversion is performed the result is stored in the FIFO and the FIFO's internal write pointer points to the next location. The pointer rolls back to location 1 after a Write to location 32. The same flow occurs when reading from the FIFO. The internal FIFO Writes and the external FIFO Reads do not affect each other's pointer locations.

Microprocessor overhead is reduced through the use of the internal conversion FIFO. Thirty-two consecutive conversions can be completed and stored in the FIFO without any microprocessor intervention. The microprocessor can, at any time, interrogate the FIFO and retrieve its contents. It can also wait for the LM12434 and LM12{L}438 to issue an interrupt when the FIFO is full or after any number ($\leq$ 32) of conversions have been stored.

Configuration Register

The CONFIGURATION Register is the main "control panel" of the DAS. Writing 1s and 0s to the different bits of the Configuration Register commands the DAS start or stop the sequencer, reset the pointers and flags, go into "standby" mode for low power consumption, calibrate offset and linearity, and select sections of the RAM.

Other Registers

The INTERRUPT ENABLE Register lets the user activate up to 7 sources for interrupt generation (refer to Section 6.2.3). It also holds two user-programmable values. One is the number of conversions to be stored in the FIFO register before the generation of the Data Ready interrupt. The other value is the instruction number that generates an interrupt when the sequencer reaches that instruction.

The INTERRUPT STATUS and LIMIT STATUS Registers are "Read only" registers. They are used as vectors to indicate which conditions have generated the interrupt and what watchdog limit boundaries have been passed. Note that the bits are set in the status registers upon occurrence of their corresponding interrupt conditions, regardless of whether the condition is enabled for external interrupt generation.

The TIMER Register can be programmed to insert a delay before execution of each instruction. A bit in the instruction register enables or disables the insertion of the delay before the execution of an instruction.

Serial I/O

A very flexible serial synchronous interface is provided to facilitate reading from and writing to the LM12434 and LM12{L}438's registers. The communication between the LM12434 and LM12{L}438 and microcontrollers, microprocessors and other circuitry is accomplished through this serial interface. The serial interface is designed to directly communicate with the synchronous serial interfaces of the most popular microprocessors with no extra hardware requirement. The interface has been also designed to simplify software development.

6.0 Operational Information (Continued)

Instruction RAM RP = 10 Limits #2	(Read/Write) RP = 01 Limits #1	RP = 00 Instructions
ADD = 0000	ADD = 0000	ADD = 0000
ADD = 0001	ADD = 0001	ADD = 0001
ADD = 0010	ADD = 0010	ADD = 0010
ADD = 0011	ADD = 0011	ADD = 0011
ADD = 0100	ADD = 0100	ADD = 0100
ADD = 0101	ADD = 0101	ADD = 0101
ADD = 0110	ADD = 0110	ADD = 0110
ADD = 0111	ADD = 0111	ADD = 0111

RP = RAM Pointer
ADD = A3, A2, A1, A0

	(Read/Write)
CONFIGURATION REGISTER	ADD = 1000
	(Read/Write)
INTERRUPT ENABLE REGISTER	ADD = 1001
	(Read Only)
INTERRUPT STATUS REGISTER	ADD = 1010
	(Read/Write)
TIMER REGISTER	ADD = 1011
	(Read Only)
CONVERSION FIFO (32 Locations, 1 address)	ADD = 1100 --- --- ---
	(Read Only)
LIMIT STATUS REGISTER	ADD = 1101

FIGURE 8. LM12434 and LM12{L}438 User Accessible Registers

6.0 Operational Information (Continued)

6.2 INTERNAL USER-ACCESSIBLE REGISTERS

Figure 8 shows the LM12434 and LM12{L}438 internal user accessible registers. *Figure 9* shows the bit assignment for each register. All the registers are accessible through the serial interface bus. Following are the descriptions of the registers and their bit assignments.

6.2.1 Instruction RAM

The instruction RAM holds up to eight sequentially executable instructions. Each 48-bit long instruction is divided into three 16-bit sections. READ and WRITE operations can be issued to each 16-bit section using the instruction's address and the 2-bit "RAM pointer" in the Configuration register. The eight instructions are located at addresses 0000 through 0111. They can be accessed and programmed in random order.

Read/Write Operations

Any Instruction RAM READ or WRITE can affect the sequencer's operation.

Therefore, the Sequencer should be stopped by setting the RESET bit to a "1" or by resetting the START bit in the Configuration Register and waiting for the current instruction to finish execution before any Instruction RAM READ or WRITE is initiated.

A soft RESET should be issued by writing a "1" to the Configuration Register's RESET bit after any READ or WRITE to the Instruction RAM.

The three sections in the Instruction RAM are selected by the Configuration Register's 2-bit "RAM Pointer", bits D8 and D9. The first 16-bit Instruction RAM section is selected with the RAM Pointer equal to "00". This section can be programmed for multiplexer channel selection, conversion resolution, watchdog mode operation, timer or external SYNC use, pause in instruction and loop bit as described later. The second 16-bit section holds "watchdog" limit #1, its sign, and a bit that determines whether an interrupt can be generated when the input is greater than or less than limit #1. The third 16-bit section holds "watchdog" limit #2, its sign, and the "greater than/less than" selection bit.

Instruction RAM, Bank 1, RP = 00

Bit 0 is the LOOP bit. After an instruction with Bit 0 set to a "1" is executed, the sequencer will loop back to instruction 0. The next instruction to be executed will be instruction 0.

Bit 1 is the PAUSE bit. When the PAUSE bit is set ("1"), the Sequencer will stop after reading the current instruction. The instruction will not execute at this point, and the START bit in the Configuration register will reset to "0". Setting the PAUSE also causes an interrupt to be issued. The Sequencer is restarted by placing a "1" in the Configuration register's Bit 0 (Start bit).

After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer retrieves Instruction 0, decodes it, and waits for a "1" to be placed in the Configuration register's START bit. The START bit value of "1" "overrides" the action of Instruction 0's PAUSE bit when the Sequencer is started. Once started, the Sequencer executes Instruction 0 and retrieves, decodes, and executes each of the remaining instructions. With the PAUSE bit set to "1" in instruction 0, no PAUSE Interrupt (INT 5) is generated the first time the Sequencer executes Instruction 0. When the Sequencer encounters a LOOP bit or completes all eight instructions, Instruction 0 is retrieved and decoded. A set PAUSE bit in Instruction 0 now halts the Sequencer before the instruction is executed. If Pause = 0, the instruction loop continues to execute.

Bits 2–4 select which of the eight input channels (IN0–IN7) will be the non-inverting inputs to the LM12{L}438's ADC. (See Table III.) They select which of the four input channels (for IN0–IN3) will be the non-inverting inputs to the LM12434's ADC. (See Table IV.)

Bits 5–7 select which of the seven input channels (IN1 to IN7) will be the inverting inputs to the LM12{L}438 ADC. (See Table III.) They select which of the three input channels (IN1–IN4) will be the inverting inputs to the LM12434's ADC. (See Table IV.) Fully differential operation is created by selecting two multiplexer channels, one non-inverting and the other inverting. A code of "000" selects ground as the inverting input for single ended operation.

Bit 8 is the SYNC bit. Setting Bit 8 to "1" causes the Sequencer to hold operation at the internal S/H's acquisition cycle and to wait until a rising edge appears at the SYNC pin. When a rising edge appears, the S/H goes into the "Hold" mode and the ADC begins to perform a conversion on the next rising edge of CLK. To make the SYNC pin serve as an input, the Configuration register's "SYNC I/O" bit (Bit 7) must be set to a "0". With SYNC configured as an input, it is possible to synchronize the start of a conversion to external events. When SYNC pin is defined as an output (SYNC I/O bit = 1) the SYNC bit in the instruction registers must not be set to 1.

When the LM12434 and LM12{L}438 are used in the "watchdog" mode with external synchronization, two rising edges on the SYNC input are required to initiate the two comparisons that are performed during a watchdog instruction. The first rising edge initiates the comparison of the selected analog input signal with Limit #1 (found in Instruction RAM "01") and the second rising edge initiates the comparison of the same analog input signal with Limit #2 (found in Instruction RAM "10").

Bit 9 is the TIMER bit. When Bit 9 is set to "1", the Sequencer will halt until the internal 16-bit Timer counts down to zero. During this time interval, no "watchdog" comparisons or analog-to-digital conversions will be performed.

Bit 10 selects the ADC conversion resolution. Setting Bit 10 to "1" selects 8-bit + sign and resetting to "0" selects 12-bit + sign.

Bit 11 is the "watchdog" comparison mode enable bit. When operating in the "watchdog" comparison mode, the selected analog input signal is compared with the programmable values stored in Limit #1 and Limit #2 (see Instruction RAM "01" and Instruction RAM "10"). Setting Bit 11 to "1" causes two comparisons of the selected analog input signal, one with each of the two stored limits. When Bit 11 is reset to "0", an 8-bit + sign or 12-bit + sign (depending on the state of Bit 10 of Instruction RAM "00") conversion of the input signal can take place.

6.0 Operational Information (Continued)

A4	A3	A2	A1	Purpose	Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 00)	R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync	S/H IN− (MUXIN−)*			S/H IN+ (MUXIN+)*			Pause	Loop
0	0	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 01)	R/W	Don't Care						>/<	Sign	Limit #1							
0	0	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 10)	R/W	Don't Care						>/<	Sign	Limit #2							
1	0	0	0	Configuration Register	R/W	Don't Care				DIAG†	Test = 0	RAM Pointer		SYNC I/O	A/Z Each Cycle	I/S	Stand-by	Full CAL	Auto-Zero	Reset	Start
1	0	0	1	Interrupt Enable Register	R/W	Number of Conversion Results in FIFO to Generate Interrupt (INT2)					Instruction Number to Generate Interrupt (INT1)			INT7	X	INT5	INT4	INT3	INT2	INT1	INT0
1	0	1	0	Interrupt Status Register	R	Number of Unread Conversion Results in FIFO					Instruction Number being Executed			INST7	X	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	1	Timer Register	R/W	Timer Preset High Byte								Timer Preset Low Byte							
1	1	0	0	Conversion FIFO	R	Instruction Number or Extended Sign				Sign	Conversion Data: MSBs			Conversion Data: LSBs							
1	1	0	1	Limit Status Register	R	Limit #2: Status								Limit #1: Status							

*LM12434 (Refer to Table IV).
†LM12{L}438 only. Must be set to "0" for the LM12434.
X No interrupt is associated with this bit. When programming the interrupt Enable Register, bit-6 is a don't care condition.

FIGURE 9. Bit Assignments for LM12434 and LM12{L}438 Internal Registers

6.0 Operational Information (Continued)

CONFIGURATION REGISTER (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care				Diag.	Test	RAM Pointer		Sync I/O	A/Z Each Cycle	I/S	Stand-by	Full Cal	Auto Zero	Reset	Start

D0: Start: 0 stops the instruction execution. 1 starts the instruction execution.

D1: Reset: When set to 1, resets Start bit; also resets all the bits in status registers and resets the instruction pointer to zero. D1 will then automatically reset itself to zero after 2 clock pulses.

D2: Auto-Zero: When set to 1 a long (8-cycle) auto-zero calibration cycle is performed.

D3: Full Calibration: When set to 1 a full calibration cycle (linearity and auto-zero) is performed.

D4: Standby: When set to 1 the chip goes to low-power standby mode. Resetting the bit will return the chip to active mode after a short delay.

D5: I/S: Instruction # or extended sign. 0 = Bits 13–15 of the conversion result hold the instruction number to which the result belongs; 1 = Bits 13–15 of the result hold the extended sign bit.

D6: A/Z each Cycle: When set to 1 a short auto-zero cycle is performed before each conversion.

D7: Sync I/O: 0 = Sync pin is input: 1 = Sync pin is output.

D9–D8: RAM Pointer: Selects the sections of the instruction RAM, 00 = Instruction, 01 = Limits #1, 10 = Limits #2.

D10: This bit is used for production testing and must be kept zero for normal operation.

D11: Diagnostic: When set to 1, the LM12{L}438 will perform a diagnostic conversion along with a properly selected instruction. This mode is not available on the LM12434.

D15–D12: Don't Care.

INSTRUCTION RAM (Read/Write):

Instruction:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Acquisition Time				Watchdog	8/12	Timer	Sync	MUXIN−			MUXIN+			Pause	Loop

D0: Loop: 0 = Go to next instruction; 1 = Loop back to in instruction #0.

D1: Pause: 0 = No pause; 1 = Pause; don't do the instruction. The start bit in the Configuration register resets to 0 when a pause encountered; a 1 written to the Start bit restarts the instruction execution.

D4–D2: MUXIN+: For the LM12{L}438, these bits select which input channel is connected to the ADC's non-inverting input. For the LM12434, they select which input channel is connected to MUXOUT+.

D7–D5: MUXIN−: For the LM12{L}438, these bits select which input channel is connected to the ADC's inverting input. For the LM12434, they select which input channel is connected to MUXOUT−.

D8: Sync: 0 = Normal operation, internal timing, SYNC is an output. 1 = SYNC is an input; S/H and conversion (comparison) timing are controlled by an external signal applied to SYNC pin.

D9: Timer: 0 = Timer is not used for this instruction; 1 = Instruction execution does not begin until timer counts down to zero.

D10: 8/12: 0 = 12-bit + sign resolution. 1 = 8-bit + sign resolution.

D11: Watchdog: 0 = Conventional conversion (no watchdog comparison); 1 = Instruction performs watchdog comparisons.

D15–D12: Acquisition Time: Determines S/H acquisition time

For 12-bit + sign: (9+2D) clock cycles. For 8-bit + sign: (2 + 2D) clock cycles.
Where D = Contents of D15–D12.
For 12-bit + sign: Choose D for D ≥ 0.45 x R_S[kΩ] × f_{CLK}[MHz].
For 8-bit + sign: Choose D for D ≥ 0.36 x R_S[kΩ] × f_{CLK}[MHz].
Where R_S = Input source resistance.

FIGURE 9. Bit Assignments for LM12434 and LM12{L}438 Internal Registers (Continued)

6.0 Operational Information (Continued)

INSTRUCTION RAM (Read/Write): (Continued)

Limits #1 & 2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Don't Care						>/<	Sign	Limit							

D7–D0: Limit: 8-bit limit value.

D8: Sign: Sign of limit value, 0 = Positive; 1 = Negative.

D9: >/<: High Limit/Low limit. 0 = Inputs lower than limit generate interrupt, 1 = Inputs higher than limit generate interrupt.

D15–D10: Don't Care.

INTERRUPT ENABLE REGISTER (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Number of Conversion Results in FIFO to Generate Interrupt (INT2)					Instruction Number to Generate Interrupt (INT1)			INT7	X	INT5	INT4	INT3	INT2	INT1	INT0

Bits # 0 to 7 enable interrupt generation for the following conditions when the bit is set to 1.

D0: INT0: Generates an interrupt when a limit is passed in watchdog mode.

D1: INT1: Generates an interrupt when the sequencer has loaded the instruction number contained in bits D10, D9, and D8 of the Interrupt Enable register.

D2: INT2: Generates an interrupt when the number of conversion results in the FIFO is equal to the programmed value (D15–D11).

D3: INT3: Generates an interrupt when an auto-zero cycle is completed.

D4: INT4: Generates an interrupt when a full calibration cycle is completed.

D5: INT5: Generates an interrupt when a pause condition is encountered.

D6: This bit is a don't care condition. No interrupt is associated with this bit.

D7: INT7: Generates an interrupt when the chip is returned from standby and is ready for operation.

D10–D8: Programmable instruction number used to generate an interrupt when that instruction has been reached.

D15–D11: Programmable number of conversion results in the FIFO to generate an interrupt.

TIMER REGISTER (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
N = Timer Preset Value															

The Timer delays the execution of an instruction if the Timer bit is set in that instruction.

The time delay is:

Delay = (32 × N) + 2 [Clock Cycles]

FIGURE 9. Bit Assignments for LM12434 and LM12{L}438 Internal Registers (Continued)

6.0 Operational Information (Continued)

FIFO REGISTER (Read only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Instruction Number or Extended Sign			Sign	Conversion Result											

D11–D0: Conversion Result:
For 12-bit + sign: 12-bit result value
For 8-bit + sign: D11–D4 = result value, D3–D0 = 1110

D12: Sign: Conversion result sign bit, 0 = Positive, 1 = Negative

D15–D13: Instruction number associated with the conversion result or the extended sign bit for 2's complement arithmetic, selected by bit D5 (Channel Mask) of the Configuration register.

INTERRUPT STATUS REGISTER (Read only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Number of Unread Results in FIFO					Instruction Number Being Executed			INST7	X	INST5	INST4	INST3	INST2	INST1	INST0

Bits #0 to 7 are interrupt flags (vectors) that will be set to 1 when the following conditions occur. The bits are set to 1 whether the interrupt is enabled or disabled in the Interrupt Enable register. The bits are reset to 0 when the register is read, or by a device reset through the Configuration register.

D0: INST0: Is set to 1 when a limit is passed in watchdog mode.

D1: INST1: Is set to 1 when the sequencer has loaded the instruction number contained in bits D10, D9, and D8 of the Interrupt Enable register.

D2: INST2: Is set to 1 when number of conversion results in FIFO is equal to the programmed value (D15–D11) in the Interrupt Enable Register.

D3: INST3: Is set to 1 when an auto-zero cycle is completed.

D4: INST4: Is set to 1 when a full calibraton cycle is completed.

D5: INST5: Is set to 1 when a pause condition is encountered.

D6: Don't care.

D7: INST7: Is set to 1 when the chip is returned from standby and is ready.

D10–D8: Holds the instruction number presently being executed or will be executed following a Pause or Timer delay.

D15–D11: Holds the number of conversion results that have been put in the FIFO but that have not yet been read by the user.

LIMIT STATUS REGISTER (Read only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Limit #2: Status								Limit #1: Status							

The bits in this register are limit flags (vectors) that will be set to 1 when a limit is passed. The bits are associated to individual instruction limits as indicated below.

D0: Limit #1 of Instruction #0 is passed.
D1: Limit #1 of Instruction #1 is passed.
D2: Limit #1 of Instruction #2 is passed.
D3: Limit #1 of Instruction #3 is passed.
D4: Limit #1 of Instruction #4 is passed.
D5: Limit #1 of Instruction #5 is passed.
D6: Limit #1 of Instruction #6 is passed.
D7: Limit #1 of Instruction #7 is passed.
D8: Limit #2 of Instruction #0 is passed.
D9: Limit #2 of Instruction #1 is passed.
D10: Limit #2 of Instruction #2 is passed.
D11: Limit #2 of Instruction #3 is passed.
D12: Limit #2 of Instruction #4 is passed.
D13: Limit #2 of Instruction #5 is passed.
D14: Limit #2 of Instruction #6 is passed.
D15: Limit #2 of Instruction #7 is passed.

FIGURE 9. Bit Assignments for LM12434 and LM12{L}438 Internal Registers (Continued)

6.0 Operational Information (Continued)

Bits 12–15 store the user-programmable acquisition time. The Sequencer keeps the internal S/H in the acquisition mode for a fixed number of clock cycles (nine clock cycles, for 12-bit + sign conversions and two clock cycles for 8-bit + sign conversions or "watchdog" comparisons) plus a variable number of clock cycles equal to twice the value stored in Bits 12–15. Thus, the S/H's acquisition time is (9 + 2D) clock cycles for 12-bit + sign conversions and (2 + 2D) clock cycles for 8-bit + sign conversions or "watchdog" comparisons, where D is the value stored in Bits 12–15. The minimum acquisition time compensates for the typical internal multiplexer series resistance of 2 kΩ, and any additional delay created by Bits 12–15 compensates for source resistances greater than 60Ω {80Ω}. The necessary acquisition time is determined by the source impedance at the multiplexer input. If the source resistance $R_S < 60\Omega$ and the clock frequency is 8 MHz, the value stored in bits 12–15 (D) can be 0000. If $R_S > 60\Omega$, the following equations determine the value that should be stored in bits 12–15.

$$D = 0.45 \times R_S \times f_{CLK}$$

for 12-bits + sign

$$D = 0.36 \times R_S \times f_{CLK}$$

for 8-bits + sign and "watchdog"

R_S is in kΩ and f_{CLK} is in MHz. Round the result to the next higher integer value. If the value of 0 obtained from the expressions above is greater than 15, it is advisable to lower the source impedance by using an analog buffer between the signal source and the LM12{L}438's multiplexer inputs. The value of D can also be used to compensate for the settling or response time of external processing circuits connected between the LM12434's MUXOUT and S/H IN pins.

Instruction RAM, Bank 2 RP = 01

The second Instruction RAM section is selected by placing "01" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #1**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12434 and LM12{L}438 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first, followed by a comparison of the same sampled analog input signal with the value found in limit #2 (Instruction RAM "10").

Bit 8 holds limit #1's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #1 to generate an interrupt, while a "0" causes a voltage less than limit #1 to generate an interrupt.

Bits 10–15 are not used.

Instruction RAM, Bank 3, RP = 10

The third Instruction RAM section is selected by placing "10" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #2**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12434 and LM12{L}438 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first (Instruction RAM "01"), followed by a comparison of the same sampled analog input signal with the value found in limit #2.

Bit 8 holds limit #2's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #2 to generate an interrupt, while a "0" causes a voltage less than limit #2 to generate an interrupt.

Bits 10–15 are not used.

TABLE III. LM12{L}438 Operating Mode Input Channel Selection through Input Multiplexer

Normal Operating Mode			
Non-Inverting Input Channel Selection Bits in Instruction Register D4, D3, D2	**Input Channel to Be Connected to A/D Non-Inverting Input (IN+)**	**Inverting Input Channel Selection Bits in Instruction Register D7, D6, D5**	**Input Channel to Be Connected to A/D Inverting Input (IN−)**
000	IN0	000	GND
001	IN1	001	IN1
010	IN2	010	IN2
011	IN3	011	IN3
100	IN4	100	IN4
101	IN5	101	IN5
110	IN6	110	IN6
111	IN7	111	IN7

6.0 Operational Information (Continued)

TABLE IV. LM12434 Input Channel Selection through Input Multiplexer

Normal Operating Mode			
Non-Inverting Input Channel Selection Bits in Instruction Register D4, D3, D2	**Input Channel to Be Connected to MUX Non-Inverting Output (MUXOUT+)**	**Inverting Input Channel Selection Bits in Instruction Register D7, D6, D5**	**Input Channel to Be Connected to MUX Inverting Output (MUXOUT−)**
000	IN0	000	GND
001	IN1	001	IN1
010	IN2	010	IN2
011	IN3	011	IN3
1XX	None	1XX	None

TABLE V. LM12{L}438 Diagnostic Mode Input Channel Selection through Input Multiplexer

Diagnostic Mode			
Non-Inverting Input Channel Selection Bits in Instruction Register D4, D3, D2	**Input Channel to Be Connected to A/D Non-Inverting Input (IN+)**	**Inverting Input Channel Selection Bits in Instruction Register D7, D6, D5**	**Input Channel to Be Connected to A/D Inverting Input (IN−)**
000	None	000	None
001	V_{REF}^+	001	V_{REF}^-
010	IN2	010	IN2
011	IN3	011	IN3
100	IN4	100	IN4
101	IN5	101	IN5
110	IN6	110	IN6
111	IN7	111	IN7

6.0 Operational Information (Continued)

6.2.2 Configuration Register

The Configuration register is a 16-bit control register with read/write capability. It acts as the LM12434's and LM12{L}438's "control panel" holding global information as well as start/stop, reset, self-calibration, and stand-by commands.

Bit 0 is the START/STOP bit. Reading Bit 0 returns an indication of the Sequencer's status. A "0" indicates that the Sequencer is stopped and waiting to execute the next instruction. A "1" shows that the Sequencer is running. Writing a "0" halts the Sequencer when the current instruction has finished execution. The next instruction to be executed is pointed to by the instruction pointer found in the status register. Writing a "1" to Bit 0 restarts the Sequencer with the instruction currently pointed to by the instruction pointer. (See Bits 8–10 in the Interrupt Status register.)

Bit 1 is the DAS' system RESET bit. Writing a "1" to Bit 1 stops the Sequencer (resetting the Configuration register's START/STOP bit), resets the Instruction pointer to "000" (found in the Interrupt Status register), clears the Conversion FIFO, and resets all interrupt flags. The RESET bit will return to "0" after two clock cycles unless it is forced high by writing a "1" into the Configuration register's Standby bit. A reset signal is internally generated when power is first applied to the part. No operation should be started until the RESET bit is "0".

Bit 2 is the auto-zero bit. Writing a "1" to this bit initiates an auto-zero offset voltage calibration. Unlike the eight-sample auto-zero calibration performed during the full calibration procedure, Bit 2 initiates a "short" auto-zero by sampling the offset once and creating a correction coefficient (full calibration averages eight samples of the converter offset voltage when creating a correction coefficient). If the Sequencer is running when Bit 2 is set to "1", an auto-zero starts immediately after the conclusion of the currently running instruction. Bit 2 is reset automatically to a "0" and an interrupt flag (Bit 3, in the Interrupt Status register) is set at the end of the auto-zero (76 clock cycles). After completion of an auto-zero calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, an auto-zero is performed immediately at the time requested.

Bit 3 is the calibration bit. Writing a "1" to this bit initiates a complete calibration process that includes a "long" auto-zero offset voltage correction (this calibration averages eight samples of the comparator offset voltage when creating a correction coefficient) followed by an ADC linearity calibration. This complete calibration is started after the currently running instruction is completed if the Sequencer is running when Bit 3 is set to "1". Bit 3 is reset automatically to a "0" and an interrupt flag (Bit 4, in the Interrupt Status register) will be generated at the end of the calibration procedure (4944 clock cycles). After completion of a full auto-zero and linearity calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, a full calibration is performed immediately at the time requested.

Bit 4 is the Standby bit. Writing a "1" to Bit 4 immediately places the DAS in Standby mode. Normal operation returns when Bit 4 is reset to a "0". The Standby command ("1") disconnects the external clock from the internal circuitry, decreases the LM12434 and LM12{L}438's internal analog circuitry power supply current, and preserves all internal RAM contents. After writing a "0" to the Standby bit, the DAS returns to an operating state identical to that caused by exercising the RESET bit. A Standby completion interrupt is issued after a power-up delay to allow the analog circuitry to settle. The Sequencer should be restarted only after the Standby completion interrupt is issued (see Note 22). The Instruction RAM can still be accessed through read and write operations while the LM12434 and LM12{L}438 are in Standby Mode.

Bit 5 is the Channel Address Mask. If Bit 5 is set to a "1", Bits 13–15 in the conversion FIFO will be equal to the sign bit (Bit 12) of the conversion data. Resetting Bit 5 to a "0" causes conversion data Bits 13 through 15 to hold the instruction pointer value of the instruction to which the conversion data belongs.

Bit 6 selects a "short" auto-zero correction for every conversion. The Sequencer automatically inserts an auto-zero before every conversion or "watchdog" comparison if Bit 6 is set to "1". No automatic correction will be performed if Bit 6 is reset to "0".

The DAS' offset voltage, after calibration, has a typical drift of 0.1 LSB over a temperature range of −40°C to +85°C. This small drift is less than the variability of the change in offset that can occur when using the auto-zero correction with each conversion. This variability is the result of using only one sample of the offset voltage to create a correction value. This variability decreases when using the full calibration mode because eight samples of the offset voltage are taken, averaged, and used to create a correction value. Therefore, it is recommended that this mode not be used.

Bit 7 programs the SYNC pin (29) to operate as either an input or an output. The SYNC pin becomes an output when Bit 7 is a "1" and an input when Bit 7 is a "0". With SYNC programmed as an input, the rising edge of any logic signal applied to pin 29 will start a conversion or "watchdog" comparison. Programmed as an output, the logic level at pin 29 will go high at the start of a conversion or "watchdog" comparison and remain high until either have finished. See Instruction RAM "00", Bit 8.

Bits 8 and **9** form the RAM Pointer that is used to select each of a 48-bit instruction's three 16-bit sections during read or write actions. A "00" selects Instruction RAM section one, "01" selects section two, and "10" selects section three.

Bit 10 activates the Test mode that is used only during production testing. Always write "0" in this bit when programming the Instruction Register.

Bit 11 is the Diagnostic bit and is available only in the LM12{L}438. It can be activated by setting it to a "1". The Diagnostic mode, along with a properly chosen instruction, allows verification that the LM12{L}438's ADC is performing correctly. When activated, the inverting and non-inverting inputs are connected as shown in Table V. As an example, an instruction with "001" for both IN+ and IN− while using the Diagnostic mode typically results in a full-scale output.

6.2.3 Interrupts

The LM12434 and LM12{L}438 have seven possible interrupts, all with the same priority. Any of these interrupts will cause a hardware interrupt to appear on the $\overline{INT}$ pin (31) if

6.0 Operational Information (Continued)

they are not masked (by the Interrupt Enable register). The Interrupt Status register is then read to determine which of the seven interrupts has been issued.

The Interrupt Status register must be cleared by reading it after writing to the Interrupt Enable register. This removes any spurious interrupts on the $\overline{INT}$ pin generated during an Interrupt Enable register access.

Interrupt 0 is generated whenever the analog input voltage on a selected multiplexer channel crosses a limit while the LM12434 and LM12{L}438 are operating in the "watchdog" comparison mode. Two sequential comparisons are made when the LM12434 and LM12{L}438 are executing a "watchdog" instruction. Depending on the logic state of Bit 9 in the Instruction RAM's second and third sections, an interrupt will be generated either when the input signal's magnitude is greater than or less than the programmable limits. (See the Instruction RAM, Bit 9 description.) The Limit Status register will indicate which preprogrammed limit (#1 or #2) was crossed, and which instruction was executing when the limit was crossed.

Interrupt 1 is generated when the Sequencer reaches the instruction counter value specified in the Interrupt Enable register's bits 8–10. This flag appears before the instruction's execution. Instructions continue to execute as programmed.

Interrupt 2 is activated when the Conversion FIFO holds a number of conversions equal to the programmable value stored in the Interrupt Enable register's Bits 11–15. This value ranges from 00000 to 11111, with 00001 to 11111 representing 1 to 31 conversions stored in the FIFO, and 00000 generating an interrupt after 32 conversions. See Section 6.2.8 for more FIFO information.

The completion of the short, single-sampled auto-zero calibration generates **Interrupt 3**.

The completion of a full auto-zero and linearity self-calibration generates **Interrupt 4**.

Interrupt 5 is generated when the Sequencer encounters an instruction that has its Pause bit (Bit 1 in Instruction RAM "00") set to "1".

Interrupt 7 is issued after a short delay (10 ms typ) while the DAS returns from Standby mode to active operation using the Configuration register's Bit 4. This short delay allows the internal analog circuitry to settle sufficiently, ensuring accurate conversion results (see Note 22).

6.2.4 Interrupt Enable Register

The Interrupt Enable register at address location 1001 has READ/WRITE capability. An individual interrupt's ability to produce an external interrupt at pin 31 ($\overline{INT}$) is accomplished by placing a "1" in the appropriate bit location. Any of the internal interrupt-producing operations will set their corresponding bits to "1" in the Interrupt Status register regardless of the state of the associated bit in the Interrupt Enable register. See Section 2.3 for more information about each of the eight internal interrupts.

Bit 0 enables an external interrupt when an internal "watchdog" comparison limit interrupt has taken place.

Bit 1 enables an external interrupt when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 enables an external interrupt when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 enables an external interrupt when the single-sampled auto-zero calibration has been completed.

Bit 4 enables an external interrupt when a full auto-zero and linearity self-calibration has been completed.

Bit 5 enables an external interrupt when an internal Pause interrupt has been generated.

Bit 6 don't care condition.

Bit 7 enables an external interrupt when the LM12434 and LM12{L}438 returns from standby to active mode (see Note 22).

Bits 8–10 form the storage location of the user-programmable value against which the Sequencer's address is compared. When the Sequencer reaches an address that is equal to the value stored in Bits 8–10, an internal interrupt is generated and appears in Bit 1 of the Interrupt Status register. If Bit 1 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 ($\overline{INT}$).

The value stored in bits 8–10 ranges from 000 to 111, representing 1 to 8 instructions stored in the Instruction RAM. After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer is started by placing a "1" in the Configuration register's START bit. Setting the INT 1 trigger value to 000 **does not generate** an INT 1 the **first** time the Sequencer retrieves and decodes Instruction 000. The Sequencer **generates** INT 1 (by placing a "1" in the Interrupt Status register's Bit 1) the **second time and every subsequent time that** the Sequencer encounters Instruction 000. It is important to remember that the Sequencer continues to operate even if an Instruction interrupt (INT 1) is internally or externally generated. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

Bits 11–15 hold the number of conversions that must be stored in the Conversion FIFO in order to generate an internal interrupt. This internal interrupt appears in Bit 2 of the Interrupt Status register. If Bit 2 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 (INT).

6.2.5 Interrupt Status Register

This read-only register is located at address 1010. The corresponding flag in the Interrupt Status register goes high ("1") any time that an interrupt condition takes place, whether an interrupt is enabled or disabled in the Interrupt Enable register. Any of the active ("1") Interrupt Status register flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration Register).

Bit 0 is set to "1" when a "watchdog" comparison limit interrupt has taken place.

Bit 1 is set to "1" when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 is set to "1" when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 is set to "1" when the single-sampled auto-zero has been completed.

Bit 4 is set to "1" when an auto-zero and full linearity self-calibration has been completed.

Bit 5 is set to "1" when a Pause interrupt has been generated.

6.0 Operational Information (Continued)

Bit 6 no interrupt is associated with this bit. Don't care condition.

Bit 7 is set to "1" when the DAS returns from standby to active mode (see Note 22).

Bits 8–10 hold the Sequencer's current instruction number while it is running.

Bits 11–15 hold the current number of conversion results stored in FIFO but have not been read by the user. After each conversion, the result will be stored in the FIFO and the contents of these bits incremented by one. Each single read from FIFO decrements the contents of these bits by one. If more than 32 conversion results being stored in FIFO the numbers on these bits roll over from "11111" to "00000" and continue incrementing. If reads are performed from FIFO more than the number of conversions stored in it, the contents of these bits roll back from "00000" to "11111" and continue decrementing.

6.2.6 Limit Status Register

This read-only register is located at address 1101. This register is used in tandem with the Limit #1 and Limit #2 registers in the Instruction RAM. Whenever a given instruction's input voltage exceeds the limit set in its corresponding Limit register (#1 or #2) a bit corresponding to the instruction number is set in the Limit Status register. Any of the active ("1") Limit Status flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration register). This register holds the status of limits #1 and #2 for each of the eight instructions.

Bits 0–7 show the Limit #1 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #1 register. When, for example, instruction 3 is a "watchdog" operation (Bit 11 is set high) and the input for instruction 3 meets the magnitude and/or polarity data stored in instruction 3's Limit #1 register, Bit 3 in the Limit Status register will be set to a "1".

Bits 8–15 show the Limit #2 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #2 register. When, for example, the input to instruction 6 meets the value stored in instruction 6's Limit #2 register, Bit 14 in the Limit Status register will be set to a "1".

6.2.7 Timer

The LM12434 and LM12{L}438 have an on-board 16-bit timer that includes a 5-bit pre-scaler. It uses the clock signal applied to pin 23 as its input. It can generate time intervals of 0 through 2^{21} clock cycles in steps of 2^5. This time interval can be used to delay the execution of instructions. It can also be used to slow the conversion rate when converting slowly changing signals. This can reduce the amount of redundant data stored in the FIFO and retrieved by the controller.

The user-defined timing value used by the Timer is stored in the 16-bit READ/WRITE Timer register at location 1011 and is pre-loaded automatically. Bits 0–7 hold the preset value's low byte and Bits 8–15 hold the high byte. The Timer is activated by the Sequencer only if the current instruction's Bit 9 is set ("1"). If the equivalent decimal value "N" ($0 \leq N \leq 2^{16} - 1$) is written inside the 16-bit Timer register and the Timer is enabled by setting an instruction's bit 9 to a "1", the Sequencer will delay that instruction's execution by halting at state 3 (S3), as shown in *Figure 11,* for $32 \times N + 2$ clock cycles.

6.2.8 FIFO

The result of each conversion is stored in an internal read-only FIFO (First-In, First-Out) register. It is located at address 1100. This register has 32 16-bit wide locations. Each location holds 13 bits of conversion data. Bits 0–3 hold the four LSBs in the 12 bits + sign mode or "1110" in the 8 bits + sign mode. Bits 4–11 hold the eight MSBs and Bit 12 holds the sign bit. Bits 13–15 can hold either the sign bit, extending the register's two's complement data format to a full sixteen bits or the instruction address that generated the conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

The FIFO status should be read in the Interrupt Status register (Bits 11–15) to determine the number of conversion results that are held in the FIFO before retrieving them. This will help prevent conversion data corruption that may take place if the number of reads are greater than the number of conversion results contained in the FIFO. Trying to read the FIFO when it is empty may corrupt new data being written into the FIFO. Writing more than 32 conversion results into the FIFO by the ADC results in loss of the first conversion results. Therefore, to prevent data loss, it is recommended that the LM12434 and LM12{L}438's interrupt capability be used to inform the system controller that the FIFO is full.

Bits 0–12 hold 12-bit + sign conversion data. **Bits 0–3** will be 1110 when using 8-bit plus sign resolution.

Bits 13–15 hold either the instruction responsible for the associated conversion data or the sign bit. Either mode is selected with Bit 5 in the Configuration register.

Using the FIFO's full depth is achieved as follows. Set the value of the Interrupt Enable registers's Bits 11–15 to 00000 and the Interrupt Enable register's Bit 2 to a "1". This generates an external interrupt when the 31st conversion is stored in the FIFO. This gives the host processor a chance to send a "0" to the LM12434 and LM12{L}438's Start bit (Configuration register) and halt the ADC before it completes the 32nd conversion. The Sequencer halts after the current (32) conversion is completed. The conversion data is then transferred to the FIFO and occupies the 32nd location. FIFO overflow is avoided if the Sequencer is halted before the start of the 32nd conversion by placing a "0" in the Start bit (Configuration register). It is important to remember that the Sequencer **continues to operate even if a FIFO interrupt (INT 2) is internally or externally generated**. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

6.0 Operational Information (Continued)

6.3 INSTRUCTION SEQUENCER

The Sequencer uses a 3-bit counter (Instruction Pointer, or IP) to retrieve the programmable conversion instructions stored in the Instruction RAM. The counter is reset to 000 during chip reset or if the current executed instruction has its Loop bit (Bit 1 in any Instruction RAM "00") set high ("1"). It increments at the end of the currently executed instruction and points to the next instruction. It will continue to increment up to 111 unless an instruction's Loop bit is set. If this bit is set, the counter resets to "000" and execution begins again with the first instruction. If all instructions have their Loop bit reset to "0", the Sequencer will execute all eight instructions continuously. Therefore, it is important to realize that if less than eight instructions are programmed, the Loop bit on the last instruction must be set. Leaving this bit reset to "0" allows the Sequencer to execute "unprogrammed" instructions, the results of which may be unpredictable.

The Sequencer's Instruction Pointer value is readable at any time and is found in the Status register at Bits 8–10. *Figure 10* illustrates the instruction execution flow as performed by the sequencer. The Sequencer can go through eight states during instruction execution:

State 0: The current instruction's first 16 bits are read from the Instruction RAM "00". This state is one clock cycle long.

State 1: Checks the state of the Calibration and Start bits. This is the "rest" state whenever the Sequencer is stopped using the reset, a Pause command, or the Start bit is reset low ("0"). When the Start bit is set to a "1", this state is one clock cycle long.

State 2: Perform calibration. If bit 2 or bit 6 of the Configuration register is set to a "1", state 2 is 76 clock cycles long. If the Configuration register's bit 3 is set to a "1", state 2 is 4944 clock cycles long.

State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below

$$32T + 2$$

where $0 \leq T \leq 2^{16} - 1$.

State 7: Sample the input signal and read Limit #1's value if needed. The number of clock cycles for acquiring the input signal in the 12-bit + sign mode varies according to

$$9 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

The number of clock cycles for acquiring the input signal in the 8-bit + sign or "watchdog" mode varies according to

$$2 + 2D$$

State 6: Perform first watchdog comparison. This state is 5 clock cycles long.

State 4: Read Limit #2. This state is 1 clock cycle long.

State 5: Perform a conversion or second watchdog comparison. This state takes 44 clock cycles for a 12-bit + sign conversions or 21 clock cycles for a 8-bit + sign conversions. The "watchdog" comparison mode takes 5 clock cycles.

6.0 Operational Information (Continued)

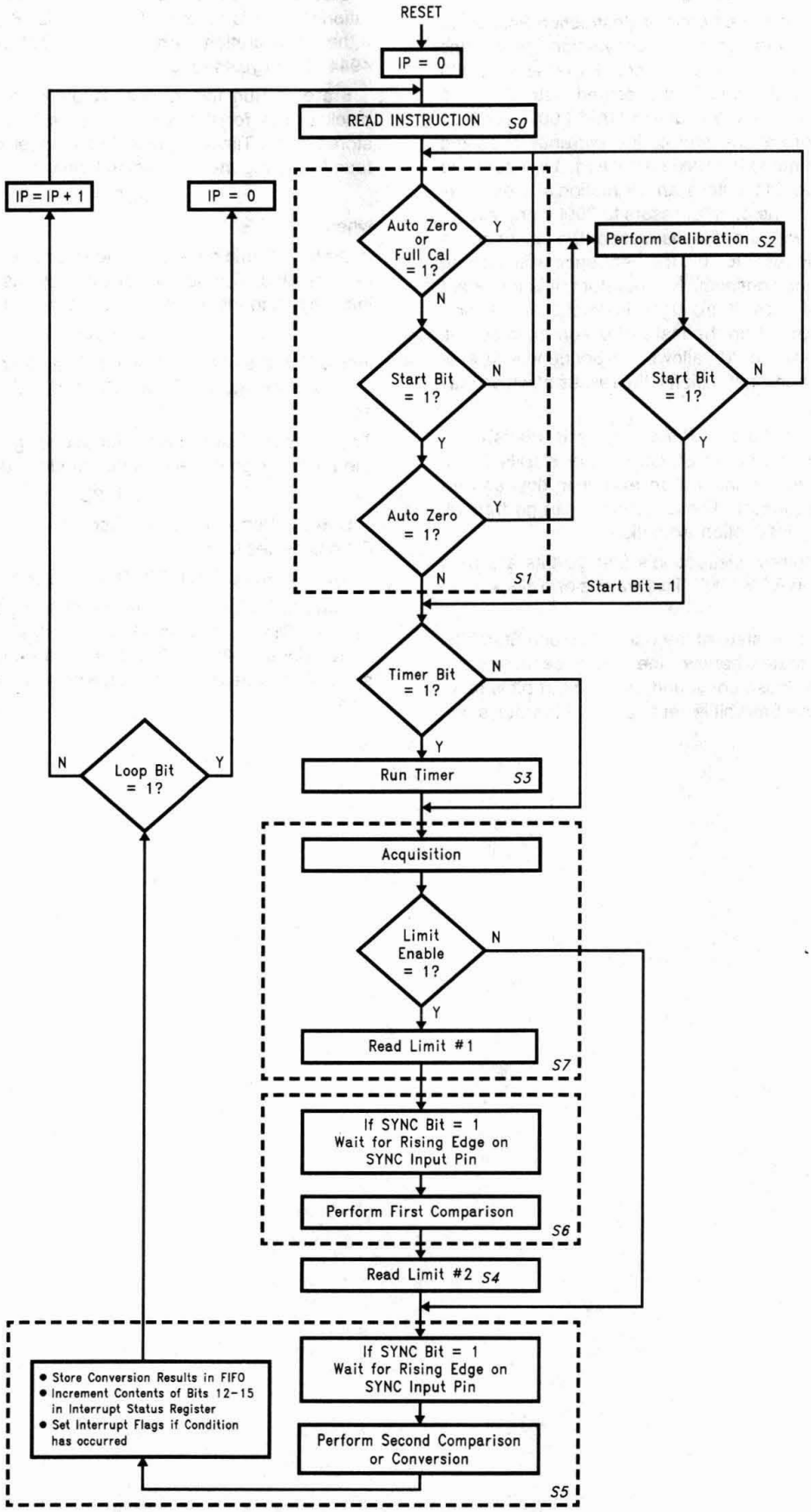

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FIGURE 10. Sequencer Logic Flow Chart (IP = Instruction Pointer)

7.0 Digital Interface

In order to read from or write to the registers of the LM12434 and LM12{L}438 a very flexible serial synchronous interface is provided. Communication between the LM12434 and LM12{L}438 and microcontrollers, microprocessors and other circuitry is accomplished through this serial interface. The serial interface is designed to directly communicate with synchronous serial interface of the most popular microprocessors and I²C serial protocol with no additional hardware required. The interface has been also designed to accommodate easy and straightforward software programming.

The LM12434 and LM12{L}438 supports four selectable protocols as shown in Table VI. The MODESEL1 and MODESEL2 inputs select the desired protocol. These pins are normally hardwired for a selected protocol, but they can also be controlled by the system in case a protocol change within the system is required. P1–P5 are multi-function serial interface input or output pins that have different assignments depending on the selected interface mode.

The "Standard" interface mode uses a simple shift register type of serial data transfer. It supports several microcontrollers' serial synchronous protocols, including: National Semiconductor's MICROWIRE/PLUS, Motorola's SPI, QSPI, and Hitachi's synchronous SCI. Section 7.1.1 shows general block diagrams of how the serial DAS, configured in the Standard Interface Mode, can be connected to the HPC and 68HC11. Also, detailed assembly routines are included for single writes, single reads and burst read operations.

The "8051" mode supports the synchronous serial interface of the 8051 family of microcontrollers (8051 serial interface Mode 0). It is also compatible with the serial interface in the MCS-96 family of 16-bit microcontrollers. Section 7.2.1 shows a general block diagram of how the serial DAS, configured in the 8051 Interface Modes can be connected to the 8051 family of μCs. Also, detailed assembly routines for a single write, single read and burst read operations are included.

The "TMS320" mode is designed to directly interact with the serial interface of the TMS320C3x and TMS320C5x families of digital signal processors. This interface is also compatible with the similar serial interfaces on the DSP56000 and the ADSP2100 families of DSP processors. Section 7.3.1 shows a general block diagram of how the serial DAS, configured in the TMS320 interface mode, can be connected to the TMS320C3x family of DSP processors. Also, detailed assembly routines for a single write, single read and burst read operations are included.

The "I²C" mode supports the Philips' I²C bus specification for both the standard (100 kHz maximum data rate) and the fast (400 kHz maximum data rate) modes of operation. The DAS behaves as a slave device on the I²C bus and receives and transmits the information under the control of a bus master. Section 7.4.1 shows a general block diagram of how the serial DAS, configured in the I²C Interface mode, can be connected to an I²C bus using an I²C controller (PCD8584).

All the serial interface modes allow for three basic types of data transfer; these are single write, single read and burst read. In a single write or read, 16 bits (2 bytes) of data is written to or read from one of the registers inside the DAS. In a burst read, multiple reads are performed from one register without having to repeatedly send the control and register address information for each read. The burst read can be performed on any LM12434 and LM12{L}438's register, however it is primarily provided for multiple reads from the FIFO register (one address, 32 locations), where a sequence of conversion results is stored.

7.1 STANDARD INTERFACE MODE

The standard interface mode is a simple shift register type of serial data transfer. The serial clock synchronizes the transfer of data to and from the LM12434 and LM12{L}438. The interface uses 4 lines: 2 data lines (DI and DO), a serial clock line (SCLK) and a chip-select (CS) line. More than one device can share the data and serial clock lines provided that each device has its own chip-select line.

The LM12434 and LM12{L}438 standard mode is selected when the MODESEL1 and MODESEL2 pins have the logic state of "01". *Figure 12* shows a typical connection diagram for the LM12434 and LM12{L}438 standard mode serial interface. The CS, DI, DO, and SCLK lines are respectively assigned to interface pins P2 through P5. The P1 pin is assigned to a signal called R/F (Rise/Fall). The logic level on this pin specifies the polarity of the serial clock:

— If R/F = 1, data is shifted after falling edge and is stable and captured at the rising edge of the SCLK.

— If R/F = 0, data is shifted after rising edge and is stable and captured at the falling edge of the SCLK.

TABLE VI. LM12434 and LM12{L}438 Interface Modes and Pin Assignments

Interface Mode	MODESEL1	MODESEL2	P1	P2	P3	P4	P5
Standard	0	1	$\overline{R}$/F	$\overline{CS}$	DI	DO	SCLK
8051	0	0	1*	1*	$\overline{CS}$	RXD	TXD
TMS320	1	1	FSR	FSX	DX	DR	CLK
I²C	1	0	Slave AD0	Slave AD1	Slave AD2	SDA	SCL

*Internally pulled-up

7.0 Digital Interface (Continued)

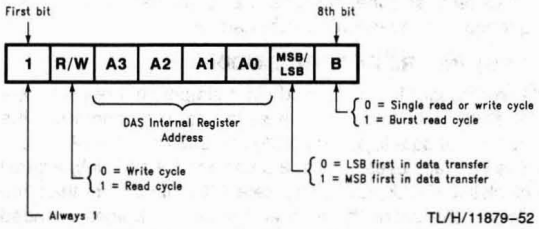
In both cases the data transfer is insensitive to idle state of the SCLK. SCLK can stay at either logic level high or low when not clocking (see *Figure 11*)

Data transfer in this mode is basically byte-oriented. This is compatible with the serial interface of the target microcontrollers and microprocessors. As mentioned, the LM12434 and LM12{L}438 have three different communication cycles: write cycle, read cycle and burst read cycle. At the start of each data transfer cycle, "command byte" is written to the serial DAS, followed by write or read data. The command byte informs the LM12434 and LM12{L}438 about the communication cycle. The command byte carries the following information:

— what type of data transfer (communication cycle) is started

— which device register to be accessed

The command byte has the following format:



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Note that the first bit may be either the MSB or the LSB of the byte depending on the processor type, but it must be the first bit transmitted to the LM12434 and LM12{L}438.

Figure 11 shows the timing diagrams for different communication cycles. *Figures 11a, b, c, d* show write cycles for various combinations of R/F pin logic level and SCLK idle state. *Figures 11e, f, g, h* show read cycles for similar sets of conditions. *Figure 11i* shows a burst read cycle for the case of R/F = 0 and low SCLK idle state. Note that these timing diagrams depict general relationships between the SCLK edges, the data bits and $\overline{CS}$. These diagrams are not meant to show guaranteed timing. (See specification tables for parametric switching characteristics.)

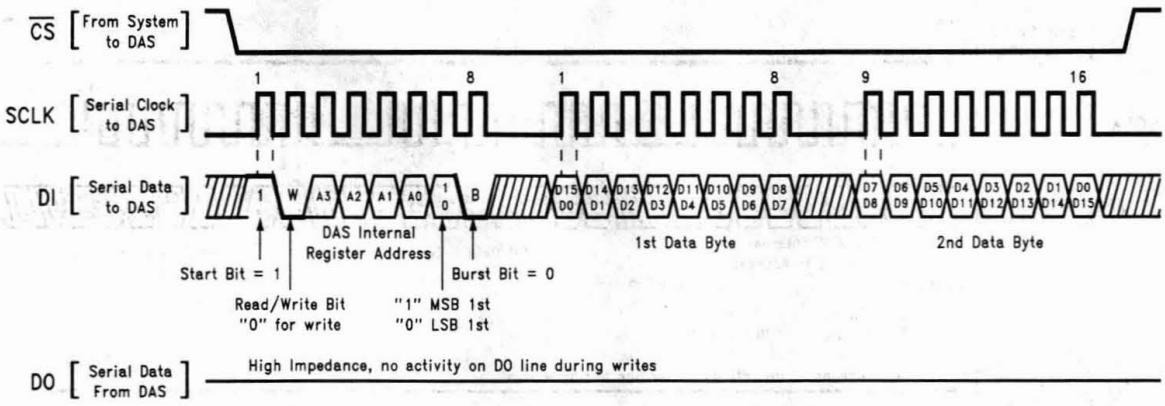
Write cycle: A write cycle begins with the falling edge of $\overline{CS}$. Then a command byte is written to the DAS on the DI line synchronized by SCLK. The command byte has the R/W and B bits equal to zero. Following the command byte, 16 bits of data (2 bytes) is shifted in on the same DI line. This data is written to the register addressed in the command byte (A3, A2, A1, A0). The data is interpreted as MSB or LSB first based on the logic level of the 7th bit (MSB/LSB) in the command byte. There is no activity on the DO line during write cycles and the DAS leaves the DO line in the high impedance state. $\overline{CS}$ will go high after the transfer of the last bit, thus completing the write cycle.

Read cycle: A read cycle starts the same way as a write cycle, except that the command byte's R/W bits equal to one. Following the command byte, the DAS outputs the data on the DO line synchronized with the microcontroller's SCLK. The data is read from the register addressed in the command byte. Data is shifted out MSB or LSB first, depending on the logic level of the MSB/LSB bit. The logic state of the DI line is "don't care" after the command byte. $\overline{CS}$ will go high after the transfer of the last data bit, then completing the read cycle.

Burst read cycle: A burst read cycle starts the same way as a single read cycle, but the B bit in the command byte is set to one, indicating a burst read cycle. Following the command byte the data is output on the DO line as long as the DAS receives SCLK from the system. To tell the DAS when a burst read cycle is completed pull $\overline{CS}$ high after the 8th and before the 15th SCLK cycle during the last data byte transfer (see *Figure 11i*). After $\overline{CS}$ high is detected and the last data bit is transferred, the DAS is ready for a new communication cycle to begin.

The timing diagrams in *Figure 11* show the transfer of data in packets of 8 bits (bytes). This represents the way the serial ports of most microcontrollers and microprocessors produce serial clock and data. The DAS does not require a gap between the first and second byte of the data; 16 continuous clock cycles will transfer the data word. However, there should be a gap equal to 3 CLK (the DAS main clock input, not the SCLK) cycles between the end of the command byte and the start of the data during a read cycle. This is not a concern in most systems for two reasons. First, the processor generally has some inherent gap between byte transfers. Second, the SCLK frequency is usually significantly slower than the CLK frequency. For example, a 68HC11 processor with an 8 MHz crystal generates a maximum SCLK frequency of 1 MHz. If the DAS is running with a 6 MHz CLK, there are 6 cycles of CLK within each cycle of SCLK and the requirement is satisfied even if SCLK operates continuously during and after the command byte.

7.0 Digital Interface (Continued)


CS [From System to DAS]
SCLK [Serial Clock to DAS]
DI [Serial Data to DAS]
DO [Serial Data From DAS]
1
8
1
8
9
16
1 W A3 A2 A1 A0 1 0 B
D15 D0 D14 D1 D13 D2 D12 D3 D11 D4 D10 D5 D9 D6 D8 D7
D7 D8 D6 D9 D5 D10 D4 D11 D3 D12 D2 D13 D1 D14 D0 D15
DAS Internal Register Address
1st Data Byte
2nd Data Byte
Start Bit = 1
Burst Bit = 0
Read/Write Bit "0" for write
"1" MSB 1st "0" LSB 1st
High Impedance, no activity on DO line during writes

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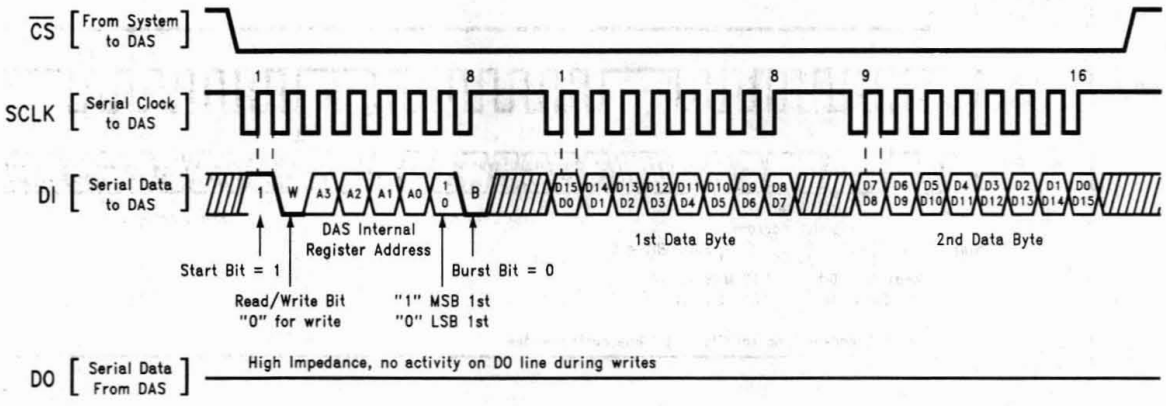
(a) Write Cycle, R/F Input (P1) = 1
Idle State of SCLK = 0, Data Stable at Rising Edge and Shifted at Falling Edge of the SCLK


CS [From System to DAS]
SCLK [Serial Clock to DAS]
DI [Serial Data to DAS]
DO [Serial Data From DAS]
1
8
1
8
9
16
1 W A3 A2 A1 A0 1 0 B
D15 D0 D14 D1 D13 D2 D12 D3 D11 D4 D10 D5 D9 D6 D8 D7
D7 D8 D6 D9 D5 D10 D4 D11 D3 D12 D2 D13 D1 D14 D0 D15
DAS Internal Register Address
1st Data Byte
2nd Data Byte
Start Bit = 1
Burst Bit = 0
Read/Write Bit "0" for write
"1" MSB 1st "0" LSB 1st
High Impedance, no activity on DO line during writes

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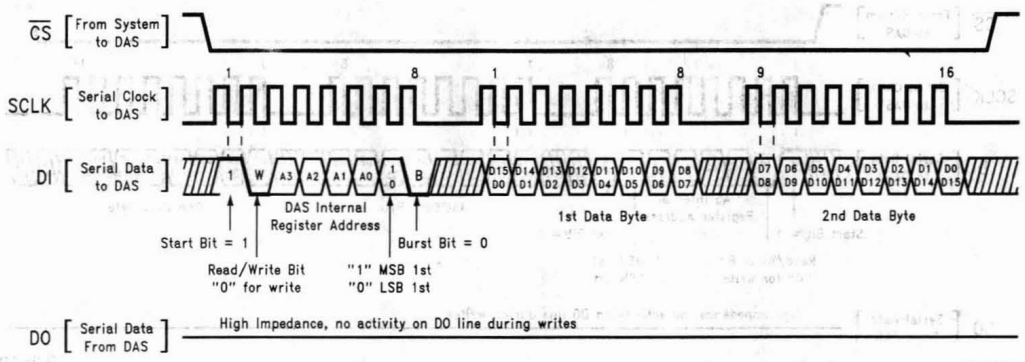
(b) Write Cycle, R/F Input (P1) = 1
Idle State of SCLK = 1, Data Stable at Rising Edge and Shifted at Falling Edge of the SCLK

FIGURE 11. Timing Diagrams for LM12434 and LM12{L}438 Standard Serial Interface

7.0 Digital Interface (Continued)


CS [From System to DAS]
SCLK [Serial Clock to DAS]
DI [Serial Data to DAS]
DO [Serial Data From DAS]
1
8
1
8
9
16
1 W A3 A2 A1 A0 1 0 B
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
DAS Internal Register Address
1st Data Byte
2nd Data Byte
Start Bit = 1
Burst Bit = 0
Read/Write Bit "0" for write
"1" MSB 1st "0" LSB 1st
High Impedance, no activity on DO line during writes

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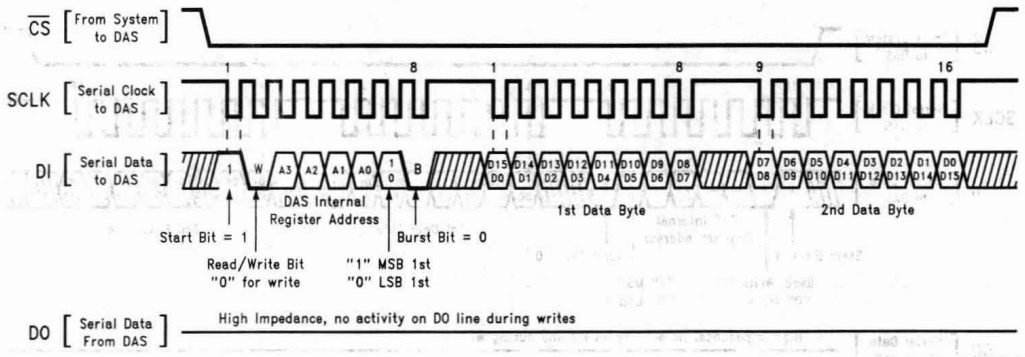
(c) Write Cycle, R/F Input (P1) = 0
Idle State of SCLK = 0, Data Stable at Falling Edge and Shifted at Rising Edge of the SCLK


CS [From System to DAS]
SCLK [Serial Clock to DAS]
DI [Serial Data to DAS]
DO [Serial Data From DAS]
1
8
1
8
9
16
1 W A3 A2 A1 A0 1 0 B
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
DAS Internal Register Address
1st Data Byte
2nd Data Byte
Start Bit = 1
Burst Bit = 0
Read/Write Bit "0" for write
"1" MSB 1st "0" LSB 1st
High Impedance, no activity on DO line during writes

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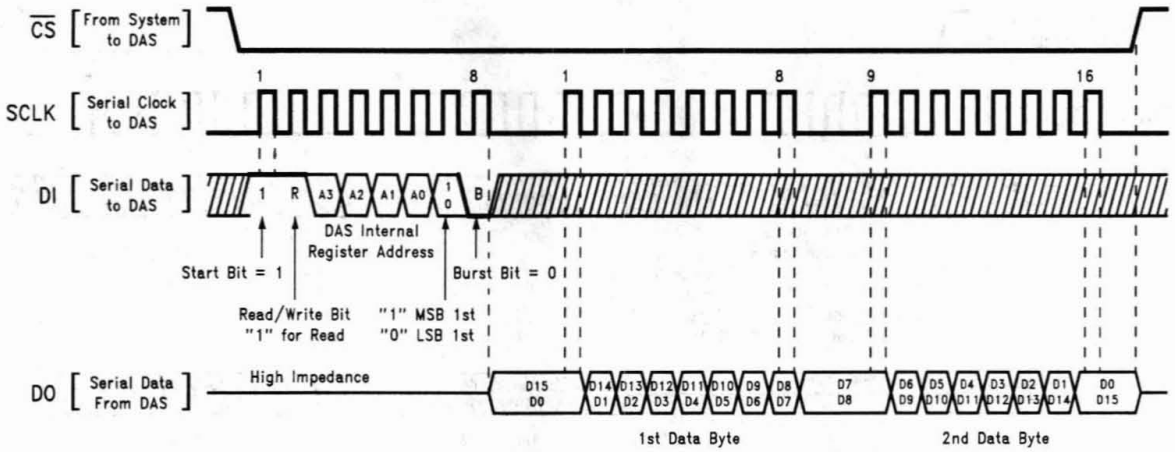
(d) Write Cycle, R/F Input (P1) = 0
Idle State of SCLK = 1, Data Stable at Falling Edge and Shifted at Rising Edge of the SCLK

FIGURE 11. Timing Diagrams for LM12434 and LM12{L}438 Standard Serial Interface (Continued)

7.0 Digital Interface (Continued)



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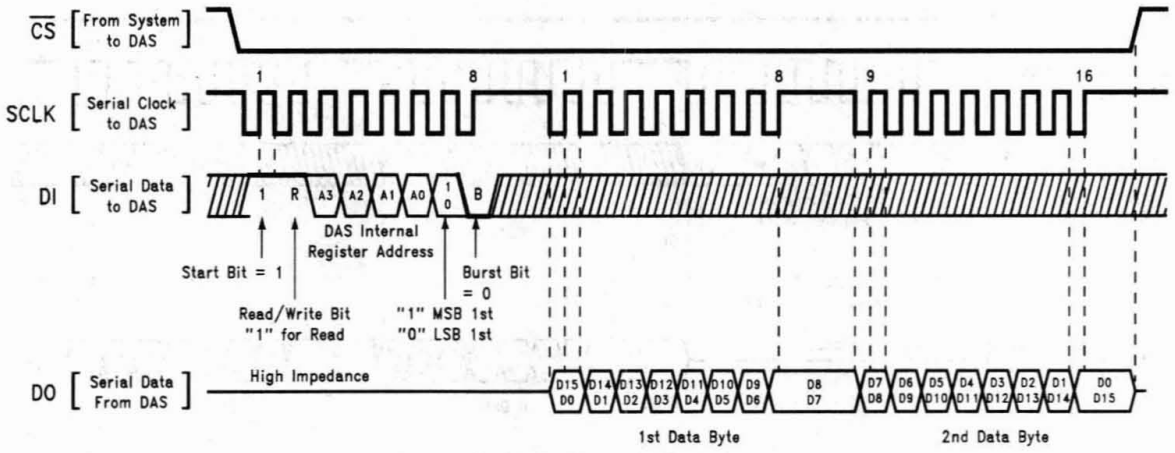
(e) Read Cycle, R/F Input (P1) = 1
Idle State of SCLK = 0, Data Stable at Rising Edge and Shifted at Falling Edge of the SCLK



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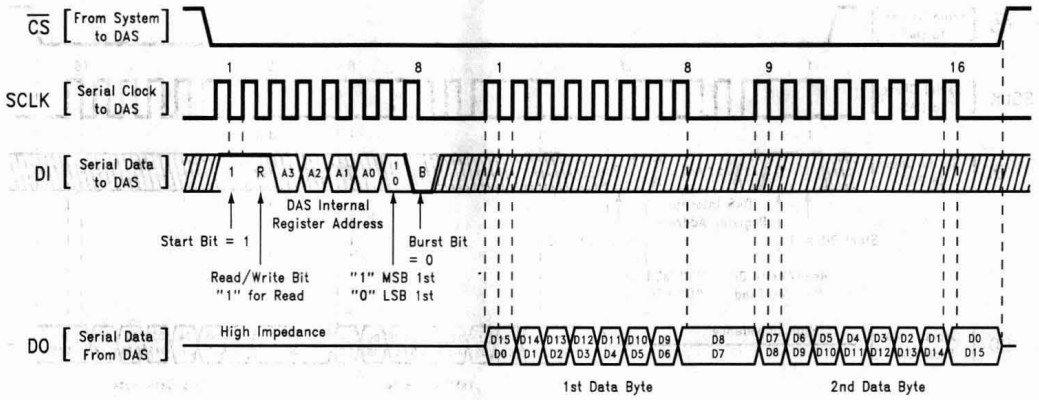
(f) Read Cycle, R/F Input (P1) = 1
Idle State of SCLK = 1, Data Stable at Rising Edge and Shifted at Falling Edge of the SCLK

FIGURE 11. Timing Diagrams for LM12434 and LM12{L}438 Standard Serial Interface (Continued)

7.0 Digital Interface (Continued)



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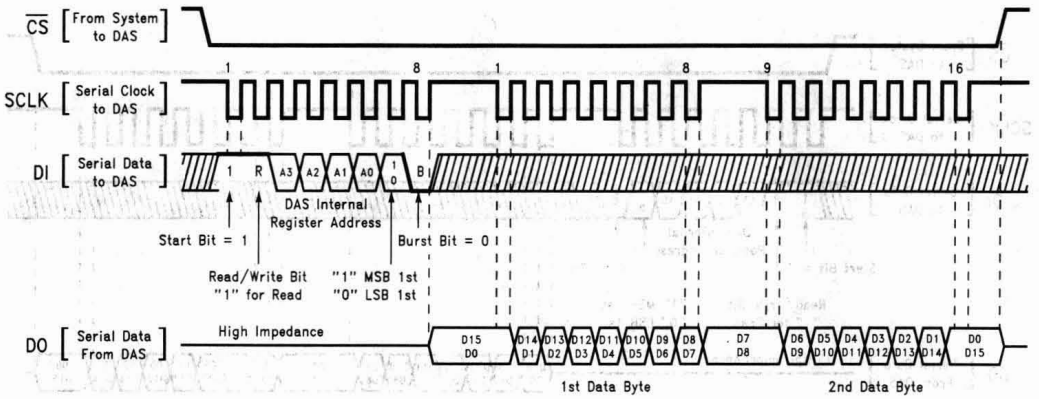
(g) Read Cycle, R/F Input (P1) = 0
Idle State of SCLK = 0, Data Stable at Falling Edge and Shifted at Rising Edge of the SCLK



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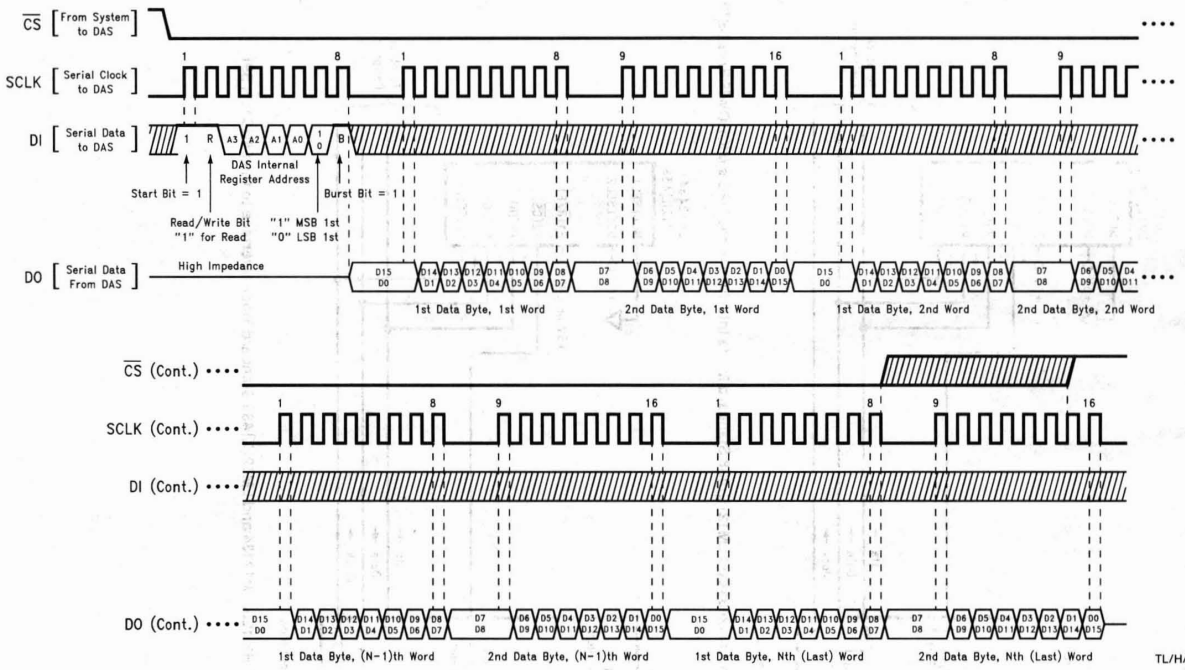
(h) Read Cycle, R/F Input (P1) = 0
Idle State of SCLK = 1, Data Stable at Falling Edge and Shifted at Rising Edge of the SCLK

FIGURE 11. Timing Diagrams for LM12434 and LM12{L}438 Standard Serial Interface (Continued)


CS [From System to DAS]
SCLK [Serial Clock to DAS]
DI [Serial Data to DAS]
DO [Serial Data From DAS]
Start Bit = 1
Read/Write Bit "1" for Read
DAS Internal Register Address
"1" MSB 1st "0" LSB 1st
Burst Bit = 1
High Impedance
1st Data Byte, 1st Word
2nd Data Byte, 1st Word
1st Data Byte, 2nd Word
2nd Data Byte, 2nd Word
CS (Cont.)
SCLK (Cont.)
DI (Cont.)
DO (Cont.)
1st Data Byte, (N-1)th Word
2nd Data Byte, (N-1)th Word
1st Data Byte, Nth (Last) Word
2nd Data Byte, Nth (Last) Word
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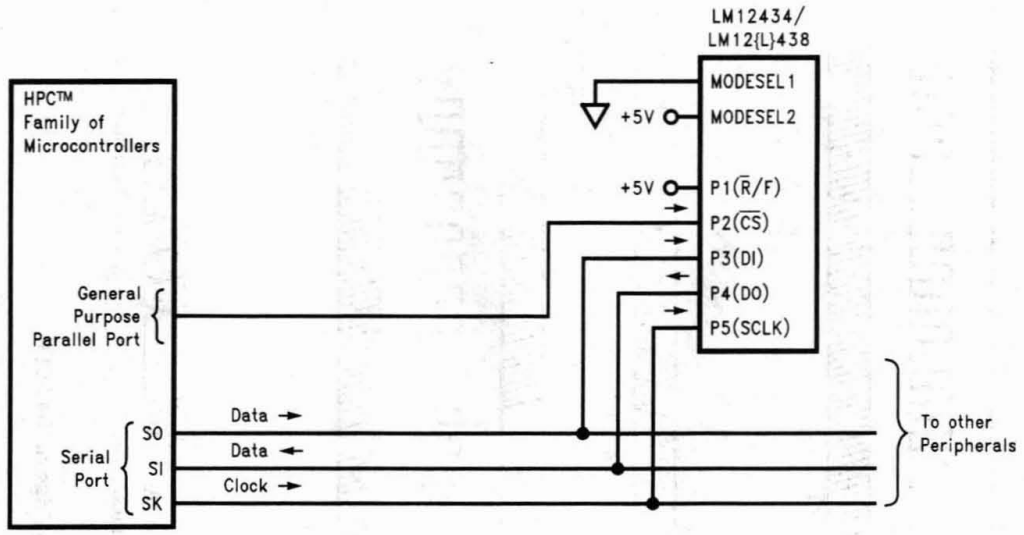
(i) Burst Read Cycle, R/F Input (P1) = 1
Idle State of SCLK = 0, Data Stable at Rising Edge and Shifted at Falling Edge of the SCLK

FIGURE 11. Timing Diagrams for LM12434 and LM12{L}438 Standard Serial Interface (Continued)

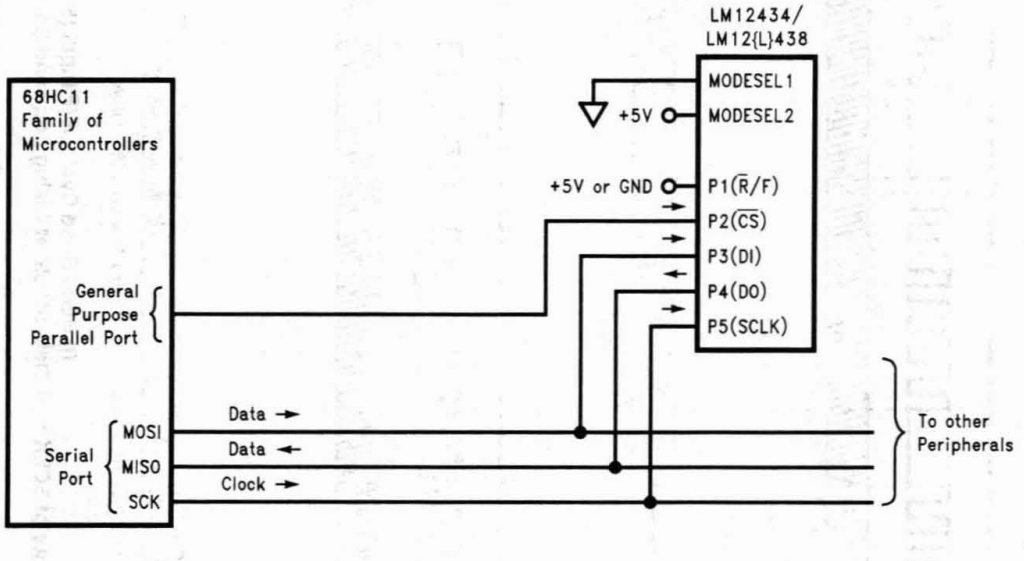
7.0 Digital Interface (Continued)

7.1.1 Examples of Interfacing to the HPC's MICROWIRE/PLUS and 68HC11's SPI



Note: Other device pins are not shown.

FIGURE 12a. LM12434 and LM12{L}438 Standard Mode Interface to the HPC's MICROWIRE/PLUS™



Note: Other device pins are not shown.

FIGURE 12b. LM12434 and LM12{L}438 Standard Mode Interface to the 68HC11's SPI

7.0 Digital Interface (Continued)

HPC Assembly Code Example

```
;*************************************************************************
; THE HPC MICROCONTROLLER ASSEMBLY SUBROUTINES FOR INTERFACE TO THE LM12434 AND LM12{L}438
; SERIAL DATA ACQUISITION SYSTEM (SDAS) CHIP.
;*************************************************************************

;*************************************************************************
; HPC's CONTROL REGISTER ADDRESSES SYMBOLIC DEFINITIONS, USED IN
; INTERFACE ROUTINES
;*************************************************************************

;       A       = 0x00C8        ;ACCUMULATOR
;       B       = 0x00CC        ;B REGISTER
;       K       = 0x00CA        ;K REGISTER
;       X       = 0x00CE        ;X REGISTER
        PORTB   = 0x00E2        ;PORT B DATA REGISTER
        IRPD    = 0x00D2        ;INTERRUPT PENDING REGISTER
        SIO     = 0x00D6        ;MICROWIRE INPUT/OUTPUT SHIFT REGISTER
        AL      = 0x00C8        ;ACCUMULATOR LOW ORDER BYTE
        AH      = 0x00C9        ;ACCUMULATOR HIGH ORDER BYTE
        uWDONE  = 0x00          ;SYMBOL FOR BIT-0 IN IRPD REGISTER TO TEST
                                ;THE END OF MICROWIRE TRANSFER
;*************************************************************************
; SERIAL DAS RELATED REGISTERS, CONSTANTS AND MEMORY BLOCK BASE ADDRESSES
; SYMBOLIC DEFINITIONS
;*************************************************************************

        RINSTR0 = 0xC2          ;SERIAL DAS INSTRUCTION RAM AND LIMITS 1 & 2
        WINSTR0 = 0x82          ;READ AND WRITE CONTROL BYTES. THESE BYTES
        RINSTR1 = 0xC6          ;CONTAIN THE ADDRESS OF THE SDAS REGISTER, THE
        WINSTR1 = 0x86          ;READ/WRITE BIT AND THE MSB/LSB BIT
        RINSTR2 = 0xCA          ;PREDEFINED.
        WINSTR2 = 0x8A          ; "
        RINSTR3 = 0xCE          ; "
        WINSTR3 = 0x8E          ; "
        RINSTR4 = 0xD2          ; "
        WINSTR4 = 0x92          ; "
        RINSTR5 = 0xD6          ; "
        WINSTR5 = 0x96          ; "
        RINSTR6 = 0xDA          ; "
        WINSTR6 = 0x9A          ; "
        RINSTR7 = 0xDE          ; "
        WINSTR7 = 0x9E          ; "

        RCONFIG = 0xE2          ;SDAS CONFIGURATION REG. READ CONTROL BYTE.
        WCONFIG = 0xA2          ;SDAS CONFIGURATION REG. WRITE CONTROL BYTE.
        RINTEN  = 0xE6          ;SDAS INTERRUPT ENABLE REG. READ CONTROL BYTE.
        WINTEN  = 0xA6          ;SDAS INTERRUPT ENABLE REG. WRITE CONTROL BYTE.
        RINTSTAT= 0xEA          ;SDAS INTERRUPT STATUS REG. READ CONTROL BYTE.
        RTIMER  = 0xEE          ;SDAS TIMER REG. READ CONTROL BYTE.
        WTIMER  = 0xAE          ;SDAS TIMER REG. WRITE CONTROL BYTE.
        RSFIFO  = 0xF2          ;SDAS FIFO , SINGLE READ CONTROL BYTE.
        RBFIFO  = 0xF3          ;SDAS FIFO , BURST READ CONTROL BYTE.
        RLMTSTAT= 0xF6          ;SDAS LIMIT STATUS REG. READ CONTROL BYTE.

        DAS_CS  = 0x0X          ;BIT-X OF HPC PORT B USED FOR SDAS CHIP
                                ;SELECT.

        DATA_BLK= 0xXXXX        ;SYMBOLIC STARING ADDRESS OF THE DATA BLOCK
                                ;IN SYSTEM MEMORY, USED TO STORE THE
                                ;CONVERSION RESULTS READ FROM FIFO IN BURST
                                ;READ ROUTINE.
        DATA_BUF= 0xXXXX        ;SYMBOLIC ADDRESS FOR A 16 BIT DATA BUFFER
        CNTRL_BUF=0xXXXX        ;SYMBOLIC ADDRESS FOR AN 8 BIT BUFFER USED
                                ;IN ROUTINES FOR CONTROL BYTE.
        RSLT_NUM= 0xXXXX        ;SYMBOLIC DEFINITION FOR THE NUMBER OF
                                ;RESULTS TO BE READ FROM FIFO IN BURST READ

;*************************************************************************
; SERIAL DAS READS AND WRITES ARE PERFORMED BY SUBROUTINES SER_WR & SER_RD,
; THESE ROUTINES USE THE CNTRL_BUF REGISTER AS CONTROL INPUT AND THE DATA_BUF
; REGISTER AS DATA BUFFER, FOR WRITES DATA IS LOADED IN THE DATA_BUF REG. AND
; FOR READS DATA RETURNS IN THE DATA_BUF REGISTER.
;*************************************************************************
```

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7.0 Digital Interface (Continued)

HPC Assembly Code Example (Continued)

```
;--- AN EXAMPLE OF A WRITE TO CONFIGURATION REGISTER:

        LD      CNTRL_BUF.B,#WCONFIG    ;CONFIGURATION REG. WRITE COMMAND
                                        ;LOADED IN THE CNTRL_BUF.
        LD      DATA_BUF.W,#0x0002      ;DATA LOADED ON THE DATA_BUF REG. RESET SDAS,
                                        ;PAUSE=1, RAM POINTER=00.
        JSR     SER_WR                  ;CALLING SER_WR FOR DATA TRANSFER.

;--- AN EXAMPLE OF A READ FROM CONFIGURATION REGISTER:

        LD      B.B,#RCONFIG            ;CONFIGURATION REG. READ COMMAND
                                        ;LOADED IN THE CNTRL_BUF.
        JSR     SER_RD                  ;CALLING SER_RD FOR DATA TRANSFER.

;*************************************************************************
; DATA WRITE SUBROUTINE "SER_WR", FOR SERIAL I/O TRANSFER OF DATA BETWEEN THE
; HPC AND THE SERIAL DAS WITH uW SERIAL INTERFACE. BEFORE CALLING THE ROUTINE,
; THE DATA TRANSFER CONTROL BYTE SHOULD BE LOADED IN THE CNTRL_BUF AND THE
; DATA TO BE WRITTEN TO THE SDAS SHOULD BE LOADED IN THE DATA_BUF.
;*************************************************************************

SER_WR:
        RBIT    DAS_CS,PORTB.B          ;RESET THE PORT B BIT-X TO SELECT
                                        ;THE SDAS1.
        LD      SIO.B,CNTRL_BUF.B       ;LOAD THE CONTROL BYTE TO HPC's SIO
                                        ;REGISTER, BYTE TRANSFER IS STARTED.
WAIT1:  IFBIT   uWDONE,IRPD.B           ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      WBYTE1                  ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT1                   ;GO AHEAD FOR FIRST DATA BYTE TRANSFER.

WBYTE1: LD      SIO.B,(DATA_BUF+1).B    ;LOAD HIGH ORDER BYTE OF DATA TO SIO
                                        ;REGISTER, TRANSFER IS STARTED.
WAIT2:  IFBIT   uWDONE,IRPD.B           ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      WBYTE2                  ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT2                   ;GO AHEAD FOR SECOND DATA BYTE TRANSFER.

WBYTE2: LD      SIO.B,DATA_BUF.B        ;LOAD LOW ORDER BYTE OF DATA TO SIO
                                        ;REGISTER, TRANSFER IS STARTED.
WAIT3:  IFBIT   uWDONE,IRPD.B           ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      WDONE                   ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT3                   ;DESELECT THE SDAS AND RETURN.

WDONE:  SBIT    DAS_CS,PORTB.B          ;SET THE BIT TO DESELECT THE SDAS.
        RET                             ;RETURN FROM SUBROUTINE.

;*************************************************************************
; DATA READ SUBROUTINE "SER_RD", FOR SERIAL I/O TRANSFER OF DATA BETWEEN THE
; HPC AND THE SERIAL DAS WITH uW SERIAL INTERFACE. BEFORE CALLING THE ROUTINE,
; THE DATA TRANSFER CONTROL BYTE SHOULD BE LOADED IN THE CNTRL_BUF AND THE
; DATA IS LOADED IN THE DATA_BUF UPON RETURN FROM SUBROUTINE.
;*************************************************************************

SER_RD:
        RBIT    DAS_CS,PORTB.B          ;RESET THE PORT B BIT-X TO SELECT
                                        ;THE SDAS1.
        LD      SIO.B,CNTRL_BUF.B       ;LOAD THE CONTROL BYTE TO HPC's SIO
                                        ;REGISTER, BYTE TRANSFER IS STARTED.
WAIT4:  IFBIT   uWDONE,IRPD.B           ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      RBYTE1                  ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT4                   ;GO AHEAD FOR FIRST DATA BYTE TRANSFER.

RBYTE1: LD      SIO.B,#0x00             ;LOAD THE SIO REGISTER WITH ZERO,
                                        ;THIS IS JUST A DUMMY LOAD TO START
                                        ;THE DATA TRANSFER
WAIT5:  IFBIT   uWDONE,IRPD.B           ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      RBYTE2                  ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT5                   ;GO AHEAD FOR SECOND DATA BYTE TRANSFER.

RBYTE2: LD      (DATA_BUF+1).B,SIO.B    ;LOAD HIGH ORDER BYTE OF THE DATA_BUF REGISTER
                                        ;WITH DATA JUST READ FROM SDAS.
        LD      SIO.B,#0x00             ;LOAD THE SIO REGISTER WITH ZERO,
                                        ;THIS IS JUST A DUMMY LOAD TO START
```

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7.0 Digital Interface (Continued)

HPC Assembly Code Example (Continued)

```
                                    ;THE DATA TRANSFER
WAIT6:  IFBIT   uWDONE,IRPD.B       ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      RDONE               ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT6               ;LOAD THE READ DATA TO AL, DESELECT THE
                                    ;SDAS AND RETURN.

RDONE:  LD      DATA_BUF.B,SIO.B    ;LOAD LOW ORDER BYTE OF THE DATA_BUF REGISTER
                                    ;WITH THE DATA JUST READ FROM SDAS.
        SBIT    DAS_CS,PORTB.B      ;SET THE BX TO DESELECT THE SDAS.
        RET                         ;RETURN FROM SUBROUTINE.

;*************************************************************************
; FIFO BURST READ SUBROUTINE "RD_FIFO",USED FOR READING THE CONVERSION RESULTS
; FROM FIFO IN BURST READ MODE. DATA IS READ FROM FIFO AND STORED IN THE
; SYSTEM MEMORY STARTING FROM THE DATA_BLK ADDRESS. NUMBER OF CONVERSION
; RESULTS BEING READ IS RSLT_NUM WHICH IS LOADED IN THE X REGISTER. IT IS ASSUMED
; THAT THE HPC IS USING 16 BIT DATA BUS.
;*************************************************************************

RD_FIFO:

        LD      BK.W,#DATA_BLK,#(DATA_BLK+2*RSLT_NUM-1)
                                    ;SET B FOR STARTING ADDRESS OF MEMORY
                                    ;AND K FOR ENDING ADDRESS MINUS ONE
LPFIFO:
        LD      X.W,#RSLY_NUM       ;A COUNTER TO KEEP TRACK OF # OF FIFO
                                    ;READS FOR TERMINATION OF BURST MODE
                                    ;BY PULLING THE CHIP SELECT HIGH DURING
                                    ;THE LAST READ CYCLE AND BEFORE THE
                                    ;14TH CLOCK EDGE.
        RBIT    DAS_CS,PORTB.B      ;RESET THE PORT B BIT-X TO SELECT
                                    ;THE SDAS.
        LD      SIO.B,#RBFIFO       ;LOAD THE BURST FIFO READ CONTROL BYTE
                                    ;TO SIO REG. BYTE TRANSFER IS STARTED.
WAIT7:  IFBIT   uWDONE,IRPD.B       ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      MSBYTE              ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT7               ;GO AHEAD FOR FIRST DATA BYTE READ.

MSBYTE: LD      SIO.B,#0x00         ;LOAD THE SIO WITH 0, THIS IS JUST A
                                    ;DUMMY LOAD TO START THE DATA TRANSFER
WAIT8:  IFBIT   uWDONE,IRPD.B       ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      LSBYTE              ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT8               ;GO AHEAD FOR SECOND DATA BYTE READ.

LSBYTE: LD      AH.B,SIO.B          ;LOAD HIGH ORDER BYTE OF THE A REGISTER
                                    ;WITH DATA JUST READ FROM THE SDAS.
        LD      SIO.B,#0x00         ;LOAD THE SIO WITH 0, THIS IS JUST A
                                    ;DUMMY LOAD TO START THE DATA TRANSFER.

        DECSZ   X                   ;DECREMENT X AND SET THE SDAS CHIP-
        JP      WAIT9               ;SELECT BIT IF LAST READ CYCLE (X=0),
        SBIT    DAS_CS,PORTB.B      ;OTHERWISE CONTINUE.

WAIT9:  IFBIT   uWDONE,IRPD.B       ;WAIT AND CHECK THE uWDONE BIT FOR
        JP      CMPLT               ;COMPLETION OF DATA TRANSFER. WHEN DONE,
        JP      WAIT9               ;LOAD THE READ DATA TO AL.

CMPLT:  LD      AL.B,SIO.B          ;LOAD LOW ORDER BYTE OF THE A REGISTER
                                    ;WITH THE DATA JUST READ FROM THE SDAS.
        XS      A,[B+].W            ;STORE A TO THE DATA_BLK WITH B AUTO-
                                    ;INCREMENT AND SKIP IF GREATER THAN K.
        JP      MSBYTE              ;GO FOR THE NEXT FIFO DATA

        RET

;*************************************************************************
; THIS ROUTINE INITIALIZES THE SDAS SERIAL INTERFACE IN CASE A
; COMMUNICATION CYCLE IS INTERRUPTED IN THE MIDDLE OF A CYCLE FOR ANY REASON.
;*************************************************************************

SDAS_SER_PORT_RST:

        SBIT    DAS_CS,PORTB.B      ;DESELECT THE SDAS
```

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7.0 Digital Interface (Continued)

HPC Assembly Code Example (Continued)

```
        LD      SIO.B,#0x00             ;RESET SEQUENCE FOR THE SDAS INTER-
RWAIT1: IFBIT   uWDONE,IRPD.B           ;FACE TO BRING IT OUT OF A HANGUP BY
        JP      R_NXT2                  ;APPLYING 24 SERIAL CLOCK PULSE WHILE
        JP      RWAIT1                  ;CHIP SELECT IS HIGH, THIS IS EQUAL TO
R_NXT2: LD      SIO.B,#0x00             ;POWER UP RESET FOR THE INTERFACE
RWAIT2: IFBIT   uWDONE,IRPD.B           ;FACE TO BRING IT OUT OF A HANGUP
        JP      R_NXT3                  ;NOTE THAT THIS ROUTINE DOES NOT RESET
        JP      RWAIT2                  ;THE SERIAL DAS BUT ONLY THE SERIAL INTERFACE
R_NXT3: LD      SIO.B,#0x00             ;THIS ROUTINE IS USEFUL DURING
RWAIT3: IFBIT   uWDONE,IRPD.B           ;SOFTWARE DEVELOPMENT OR IN CASE THAT
        RET                             ;A COMMUNICATION CYCLE NEEDS TO BE
        JP      RWAIT3                  ;INTERRUPTED BY SYSTEM REQUIREMENTS.
```

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68HC11 Assembly Code Example

```
*****************************************************************************
* THE 68HC11 MICROCONTROLLERS FAMILY ASSEMBLY SUBROUTINES FOR INTERFACE TO
* THE LM12434 AND LM12{L}438 SERIAL DATA ACQUISITION SYSTEM (SDAS) CHIP.
*****************************************************************************

*****************************************************************************
* 68HC11 CONTROLLER REGISTER'S ADDRESSES SYMBOLIC DEFINITIONS, USED IN
* INTERFACE ROUTINES
*****************************************************************************
PORTD   EQU     $1008   ; Port D data register
*                       ; " -    , -  ,SS* ,SCK ;MOSI,MISO,TxD ,RxD "
*                       ; PORT D "SS" BIT IS USED FOR SDAS CHIP SELECT
DDRD    EQU     $1009   ; Port D data direction
SPCR    EQU     $1028   ; SPI control register
*                       ; "SPIE,SPE ,DWOM,MSTR;CPOL,CPHA,SPR1,SPR0"
SPSR    EQU     $1029   ; SPI status register
*                       ; "SPIF,WCOL, -  ,MODF; -    , -  , -  , -  "
SPDR    EQU     $102A   ; SPI data register; Read-Buffer; Write-Shifter
*
*****************************************************************************
* SERIAL DAS RELATED REGISTERS, CONSTANTS AND MEMORY BLOCKS BASE ADDRESSES
* SYMBOLIC DEFINITIONS
*****************************************************************************
*
RINSTR0   EQU   $C2         ;SERIAL DAS INSTRUCTION RAM AND LIMITS 1 & 2
WINSTR0   EQU   $82         ;READ AND WRITE CONTROL BYTES. THESE BYTES
RINSTR1   EQU   $C6         ;CONTAIN ADDRESSES OF THE SDAS REGISTER, THE
WINSTR1   EQU   $86         ;READ/WRITE BIT AND THE MSB/LSB BIT
RINSTR2   EQU   $CA         ;PREDEFINED.
WINSTR2   EQU   $8A         ; "
RINSTR3   EQU   $CE         ; "
WINSTR3   EQU   $8E         ; "
RINSTR4   EQU   $D2         ; "
WINSTR4   EQU   $92         ; "
RINSTR5   EQU   $D6         ; "
WINSTR5   EQU   $96         ; "
RINSTR6   EQU   $DA         ; "
WINSTR6   EQU   $9A         ; "
RINSTR7   EQU   $DE         ; "
WINSTR7   EQU   $9E         ; "

RCONFIG   EQU   $E2         ;SDAS CONFIGURATION REG. READ CONTROL BYTE.
WCONFIG   EQU   $A2         ;SDAS CONFIGURATION REG. WRITE CONTROL BYTE.
RINTEN    EQU   $E6         ;SDAS INTERRUPT ENABLE REG. READ CONTROL BYTE.
WINTEN    EQU   $A6         ;SDAS INTERRUPT ENABLE REG. WRITE CONTROL BYTE.
RINTSTAT  EQU   $EA         ;SDAS INTERRUPT STATUS REG. READ CONTROL BYTE.
RTIMER    EQU   $EE         ;SDAS TIMER REG. READ CONTROL BYTE.
WTIMER    EQU   $AE         ;SDAS TIMER REG. WRITE CONTROL BYTE.
RSFIFO    EQU   $F2         ;SDAS FIFO , SINGLE READ CONTROL BYTE.
RBFIFO    EQU   $F3         ;SDAS FIFO , BURST READ CONTROL BYTE.
RLMTSTAT  EQU   $F6         ;SDAS LIMIT STATUS REG. READ CONTROL BYTE.
*
*
```

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7.0 Digital Interface (Continued)

68HC11 Assembly Code Example (Continued)

```
DATA_BLK  EQU   $10          ;SYMBOLIC STARTING ADDRESS OF THE DATA BLOCK
*                            ;IN SYSTEM MEMORY, USED TO STORE THE
*                            ;CONVERSION RESULTS READ FROM FIFO IN BURST
*                            ;READ ROUTINE.
DATA_BUF  EQU   $42          ;SYMBOLIC ADDRESS FOR A 16 BIT DATA BUFFER
CNTRL_BUF EQU   $40          ;SYMBOLIC ADDRESS FOR AN 8 BIT BUFFER USED
*                            ;IN ROUTINES FOR CONTROL BYTE.
RSLT_NUM  EQU   $10          ;SYMBOLIC DEFINITION FOR THE NUMBER OF
*                            ;RESULTS TO BE READ FROM FIFO IN BURST READ
*
*******************************************************************************
* SERIAL DAS READS AND WRITES ARE PERFORMED BY SUBROUTINE SER_IO.
* THIS ROUTINE USES THE CNTRL_BUF REGISTER AS CONTROL INPUT AND THE DATA_BUF
* REGISTER AS DATA BUFFER, FOR WRITES DATA IS LOADED ON THE DATA_BUF REG. AND
* FOR READS DATA RETURNS IN THE DATA_BUF REGISTER.
*******************************************************************************

*--- AN EXAMPLE OF A WRITE TO CONFIGURATION REGISTER:

        LDAA    #WCONFIG            ;CONFIGURATION REG. WRITE COMMAND
        STAA    CNTRL_BUF           ;LOADED IN THE CNTRL_BUF.
        LDD     #$0010              ;DATA LOADED ON THE DATA_BUF REG.
        STD     DATA_BUF            ;RESET= 1, RAM POINTER=00.
        JSR     SER_IO              ;CALLING SER_WR FOR DATA TRANSFER.

*--- AN EXAMPLE OF A READ FROM CONFIGURATION REGISTER:

        LDAA    #RCONFIG            ;CONFIGURATION REG. READ COMMAND
        STAA    CNTRL_BUF           ;LOADED IN THE CNTRL_BUF.
        JSR     SER_IO              ;CALLING SER_RD FOR DATA TRANSFER.

*******************************************************************************
* DATA WRITE/READ SUBROUTINE "SER_IO", FOR SERIAL I/O TRANSFER OF DATA BETWEEN
* THE 68HC11 AND THE SERIAL DAS WITH SPI SERIAL INTERFACE. BEFORE CALLING THE
* ROUTINE, THE DATA TRANSFER CONTROL BYTE SHOULD BE LOADED IN THE CNTRL_BUF.
* FOR WRITES THE DATA TO BE WRITTEN TO THE SDAS SHOULD BE LOADED IN DATA_BUF.
* FOR READS, DATA IS LOADED INTO THE DATA_BUF UPON RETURN FROM THIS SUBROUTINE.
*******************************************************************************

SER_IO:
        BCLR    PORTD,Y $20         ; DROP CHIP SELECT
        LDAA    CNTRL_BUF           ; LOAD A WITH CONTROL BYTE
        STAA    SPDR                ; START SPI SEND
SEND1   LDAA    SPSR                ; GET SPI STATUS TO WAIT FOR SPIF
        ANDA    #$80                ; MASKING THE EIGHTH BIT WITH THE SPIF BIT
        BEQ     SEND1               ; IF SPIF=0 THEN BRANCH, ELSE SKIP
        LDAA    DATA_BUF            ; GET MSB DATA BYTE AND SEND
        STAA    SPDR                ; START SPI SEND. THIS WILL ALSO CLEAR THE SPIF BIT
SEND2   LDAA    SPSR                ; GET SPI STATUS TO WAIT FOR SPIF
        ANDA    #$80                ; MASKING THE EIGHTH BIT WITH THE SPIF BIT
        BEQ     SEND2               ; IF SPIF=0 THEN BRANCH, ELSE SKIP
        LDAA    SPDR                ; LOADS 1 DATA BYTE (MSB/LSB) SENT FROM DAS INTO ACC A
        STAA    DATA_BUF            ; STORE MSB DATA BYTE IN RAM BUFFER
        LDAA    DATA_BUF+1          ; GET LSB DATA BYTE TO SEND
        STAA    SPDR                ; START SPI SEND
SEND3   LDAA    SPSR                ; GET SPI STATUS TO WAIT FOR SPIF
        ANDA    #$80                ; MASKING THE EIGHTH BIT WITH THE SPIF BIT
        BEQ     SEND3               ; IF SPIF=0 THEN BRANCH, ELSE SKIP
        LDAA    SPDR                ; LOADS 1 DATA BYTE (MSB/LSB) SENT FROM DAS INTO ACC A
        STAA    DATA_BUF            ; STORE MSB DATA BYTE IN RAM BUFFER
        BSET    PORTD,Y $20         ; DONE -- RAISE CS
        RTS
```

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1

7.0 Digital Interface (Continued)

68HC11 Assembly Code Example (Continued)

```
*****************************************************************************
* FIFO BURST READ SUBROUTINE "RD_FIFO", FOR READING THE CONVERSION RESULTS
* FROM FIFO IN BURST READ MODE. DATA IS READ FROM FIFO AND STORED IN THE
* SYSTEM MEMORY STARTING FROM THE DATA_BLK ADDRESS. NUMBER OF CONVERSION
* RESULTS BEING READ IS RSLT_NUM WHICH IS LOADED IN THE X REGISTER. IT IS ASSUMED
* THAT THE HPC IS USING 16 BIT DATA BUS.
*****************************************************************************
RD_FIFO:
        LDX     #DATA_BLK           ; LOAD X WITH DATA BLOCK BASE ADDRESS
        LDAB    #RSLT_NUM           ; LOAD B WITH NUMBER OF RESULTS
        LSLB                        ; MAKE INTO BYTE COUNT
        DECB                        ; ONE LESS FOR LAST BYTE
        BCLR    PORTD,Y $20         ; DROP CHIP SELECT
        LDAA    #RBFIFO             ; LOAD A WITH BURST READ COMMAND
        STAA    SPDR                ; SEND COMMAND
BURST1  LDAA    SPSR                ; GET SPI STATUS TO WAIT FOR SPIF
        ANDA    #$80                ; MASKING THE EIGHTH BIT WITH THE SPIF BIT
        BEQ     BURST1              ; IF SPIF=0 THEN BRANCH, ELSE SKIP

BLOOP
        CLRA                        ; CLEAR DATA BYTE TO SEND
        STAA    SPDR                ; START SPI, RECEIVE A DATA BYTE
BURST2  LDAA    SPSR                ; GET SPI STATUS TO WAIT FOR SPIF
        ANDA    #$80                ; MASKING THE EIGHTH BIT WITH THE SPIF BIT
        BEQ     BURST2              ; IF SPIF=0 THEN BRANCH, ELSE SKIP
        LDAA    SPDR                ; GET THE RECEIVED DATA BYTE
        STAA    0,X                 ; STORE DATA BYTE
        INX                         ; POINT TO NEXT DATA BYTE
        DECB                        ; COUNTING DOWN # OF BYTES
        BNE     BLOOP               ; STILL MORE DATA BYTES TO GET
        BSET    PORTD,Y $20         ; RAISE CS TO END BURST READ
        STAA    SPDR                ; START SPI, RECEIVE LAST BYTE
BURST3  LDAA    SPSR                ; GET SPI STATUS TO WAIT FOR SPIF
        ANDA    #$80                ; MASKING THE EIGHTH BIT WITH THE SPIF BIT
        BEQ     BURST3              ; IF SPIF=0 THEN BRANCH, ELSE SKIP
        LDAA    SPDR                ; GET RECEIVED DATA BYTE
        STAA    0,X                 ; STORE DATA BYTE IN RAM BUFFER
        RTS
```

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7.0 Digital Interface (Continued)

7.2 8051 INTERFACE MODE

The 8051 interface mode is designed to work directly with the 8051 family of microcontrollers' mode 0 serial interface. This interface mode is a simple shift register type of serial data transfer. The serial clock synchronizes the transfer of data to and from the LM12434 and LM12{L}438. The interface uses 3 lines: a bidirectional data line (RXD), a serial clock line (TXD) and a chip-select ($\overline{CS}$) line. More than one device can share the data and serial clock lines provided that each device has its own chip-select line.

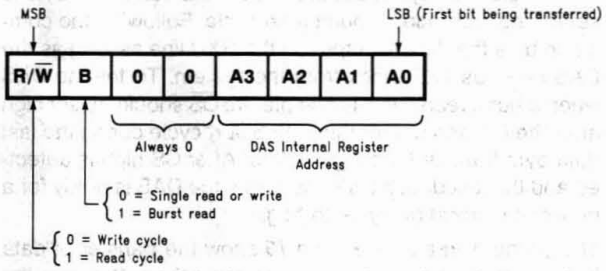
The 8051 mode is selected when the MODESEL1 and MODESEL2 pins have the logic state of "00". *Figure 14* shows a typical connection diagram for the 8051 mode serial interface. The $\overline{CS}$, RXD and TXD lines are respectively assigned to interface pins P3 through P5. The P1 and P2 pins are not used in this mode and should be left open or connected to logic "1". In this interface the idle state of the serial clock TXD is logic "1". The data is stable at both edges of the TXD clock and is shifted after its rising edge. The interface has a bidirectional RXD data line. The LM12434 and LM12{L}438 leaves the RXD line in a high impedance state whenever it is not outputting any data.

Data transfer in this mode is byte oriented. As mentioned, the LM12434 and LM12{L}438 has three different communication cycles: write cycle, read cycle and burst read cycle. At the start of each data transfer cycle, "command byte" is written to the LM12434 and LM12{L}438, followed by write or read data. The command byte informs the LM12434 and LM12{L}438 about the communication cycle and carries the following information:

— what type of data transfer (communication cycle) is started

— which device register is to be accessed

The command byte has the following format:



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The first bit is the LSB of the byte based on the 8051 mode 0 serial interface protocol.

Figure 13 shows the timing diagrams for different communication cycles. *Figure 13a* shows a write cycle. *Figure 13b* shows a read cycle. *Figure 13c* shows a burst read cycle. Note that these timing diagrams depict general relationships between the SCLK edges, the data bits and $\overline{CS}$. These diagrams are not meant to show guaranteed timing performance. (See specification tables for parametric switching characteristics.)

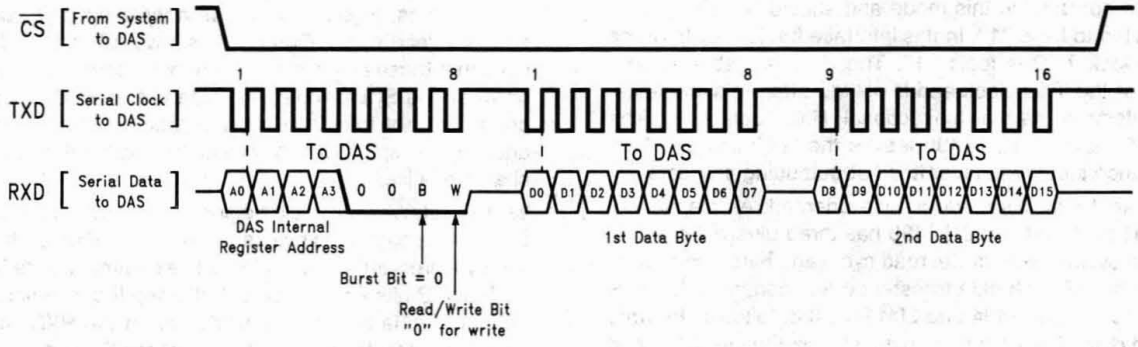
Write cycle: A write cycle begins with the falling edge of the $\overline{CS}$. Then a command byte is written to the DAS on the RXD line synchronized by TXD clock. The command byte has the R/W and B bits equal to zero. Following the command byte, 16 bits of data (2 bytes) is shifted in on the RXD line. The data is written to the register addressed in the command byte (A3, A2, A1, A0). The data is always LSB first in this interface. $\overline{CS}$ will go high after the transfer of the last bit, thus completing the write cycle.

Read cycle: A read cycle starts the same way as a write cycle, except that the command bytes R/$\overline{W}$ bit is equal to one. Following the command byte, the DAS outputs the data on the RXD line synchronized with the microcontroller's TXD clock. The data is read from the register addressed in the command byte. Data is shifted in LSB first. Again, $\overline{CS}$ will go high after the transfer of the last data bit, thus completing the read cycle.

7.0 Digital Interface (Continued)

Burst read cycle: A burst read cycle starts the same way as a single read cycle, but the B bit in the command byte is set to one, indicating a burst read cycle. Following the command byte the data is output on the RXD line as long as the DAS receives TXD clock from the system. To tell the DAS when a burst read cycle is completed, $\overline{CS}$ should be set high after the 8th and before the 15th SCLK cycle during the last data byte transfer (see *Figure 13c*). After $\overline{CS}$ high is detected and the last data bit is transferred, the DAS is ready for a new communication cycle to begin.

The timing diagrams in *Figure 13* show the transfer of data in packets of 8 bits (bytes). This represents the way the serial ports of the 8051 family of microcontrollers produce the serial clock and data. The DAS does not require a gap between the first and second bytes of the data; 16 continuous clock cycles will transfer the data word. However, there should be a gap equal to 3 CLK (the DAS main clock input, not the TXD clock) cycles between the end of the command byte and the start of the data during a read cycle. This is not concerned in most systems for two reasons. First, the processor generally has some inherent gap between byte transfers. Second, the TXD frequency is usually significantly slower than the CLK frequency. For example, an 8051 processor with 12 MHz crystal generates a TXD of 1 MHz. If the DAS is running with 6 MHz CLK, there are 6 cycles of CLK within each cycle of TXD and the requirement is satisfied even if TXD comes continuously after command byte. The user should pay attention to this requirement if running the TXD with a speed near or higher than CLK.



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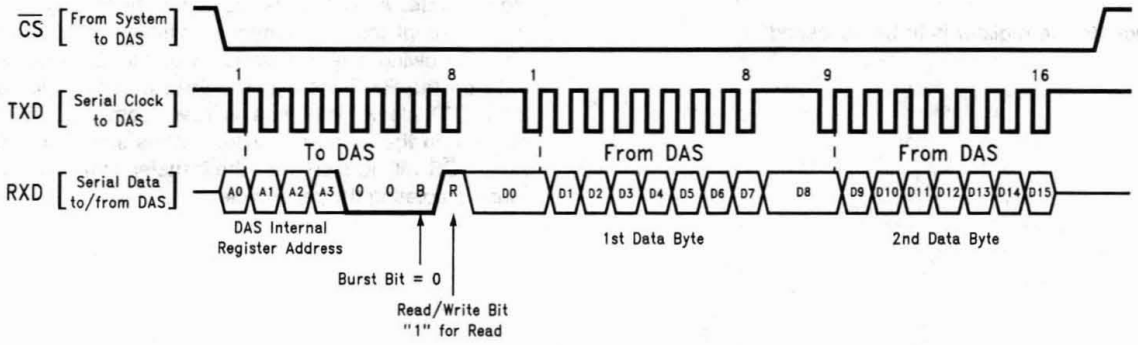
(a) Write Cycle
Idle State of SCLK = 1, Data Shifted at the Rising Edge of the SCLK



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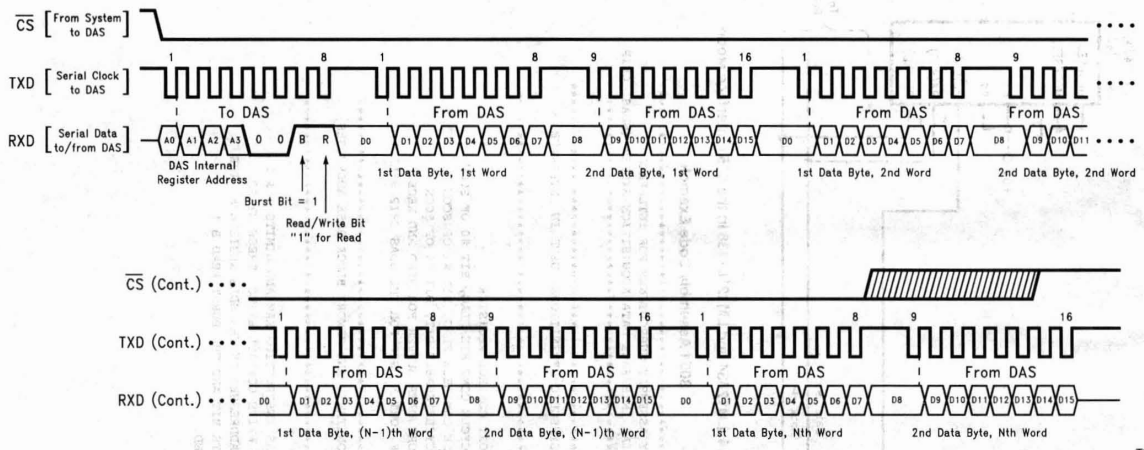
(b) Read Cycle
Idle State of SCLK = 1, Data Shifted at the Rising Edge of the SCLK

FIGURE 13. Timing Diagrams for LM12434 and LM12{L}438 8051 Serial Interface Mode



(c) Burst Read Cycle
Idle State of SCLK = 1, Data Shifted after the Rising Edge of the SCLK

FIGURE 13. Timing Diagrams for LM12434 and LM12{L}438 8051 Serial Interface Mode (Continued)

7.0 Digital Interface (Continued)

7.2.1 Example of Interfacing to the 8051

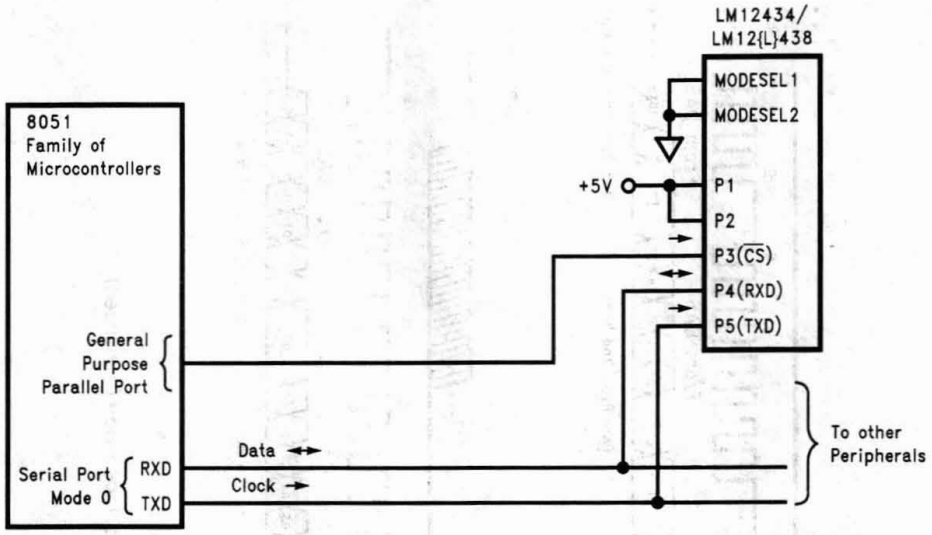


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FIGURE 14. LM12434 and LM12{L}438 in the 8051 Interface Mode

8051 Assembly Code Example

```
;*****************************************************************************
; THE 8051 MICROCONTROLLERS FAMILY ASSEMBLY SUBROUTINES FOR INTERFACE TO
; THE LM12434 and LM12{L}438, SERIAL INTERFACE DATA ACQUISITION SYSTEM (SDAS) CHIP
;*****************************************************************************

;*****************************************************************************
; 8051 CONTROLLER REGISTER, BITS SYMBOLIC DEFINITIONS, USED IN INTERFACE
; ROUTINES
;*****************************************************************************

;SCON                    ;SERIAL PORT CONTROL REGISTER
R_DONE     BIT    SCON.0  ;RECEIVE CYCLE COMPLETE FLAG, BIT #0 OF SCON
S_DONE     BIT    SCON.1  ;SEND CYCLE COMPLETE FLAG, BIT #1 OF SCON
R_EN       BIT    SCON.4  ;RECEIVE CYCLE ENABLE BIT, BIT #4 OF SCON
;SBUF                    ;SERIAL PORT DATA BUFFER FOR SEND AND RECEIVE
SDAS_SLCT  BIT    P3.4    ;PIN #4 OF PORT 3 USED FOR THE SDAS CHIP SELECT

;*****************************************************************************
; SERIAL DAS RELATED REGISTERS, CONSTANTS AND MEMORY BLOCK BASE ADDRESSES
; SYMBOLIC DEFINITIONS
;*****************************************************************************

RINSTR0    EQU    80H     ;SERIAL DAS INSTRUCTION RAM AND LIMITS 1 & 2
WINSTR0    EQU    00H     ;READ AND WRITE CONTROL BYTES. THESE BYTES
RINSTR1    EQU    81H     ;CONTAIN ADDRESSES OF THE SDAS REGISTERS, THE
WINSTR1    EQU    01H     ;READ/WRITE BIT AND THE BURST READ BIT
RINSTR2    EQU    82H     ;PREDEFINED.
WINSTR2    EQU    02H     ; "
RINSTR3    EQU    83H     ; "
WINSTR3    EQU    03H     ; "
RINSTR4    EQU    84H     ; "
WINSTR4    EQU    04H     ; "
RINSTR5    EQU    85H     ; "
WINSTR5    EQU    05H     ; "
RINSTR6    EQU    86H     ; "
WINSTR6    EQU    06H     ; "
RINSTR7    EQU    87H     ; "
WINSTR7    EQU    07H     ; "
```

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7.0 Digital Interface (Continued)

8051 Assembly Code Example (Continued)

```
RCONFIG   EQU   88H     ;SDAS CONFIGURATION REG. READ CONTROL BYTE.
WCONFIG   EQU   08H     ;SDAS CONFIGURATION REG. WRITE CONTROL BYTE.
RINTEN    EQU   89H     ;SDAS INTERRUPT ENABLE REG. READ CONTROL BYTE.
WINTEN    EQU   09H     ;SDAS INTERRUPT ENABLE REG. WRITE CONTROL BYTE.
RINTSTAT  EQU   8AH     ;SDAS INTERRUPT STATUS REG. READ CONTROL BYTE.
RTIMER    EQU   8BH     ;SDAS TIMER REG. READ CONTROL BYTE.
WTIMER    EQU   0BH     ;SDAS TIMER REG. WRITE CONTROL BYTE.
RSFIFO    EQU   8CH     ;SDAS FIFO , SINGLE READ CONTROL BYTE.
RBFIFO    EQU   0CCH    ;SDAS FIFO , BURST READ CONTROL BYTE.
RLMTSTAT  EQU   8DH     ;SDAS LIMIT STATUS REG. READ CONTROL BYTE.


DATA_BLK  EQU   0XXH    ;SYMBOLIC STARTING ADDRESS OF THE DATA BLOCK
                        ;IN SYSTEM MEMORY, USED TO STORE THE
                        ;CONVERSION RESULTS READ FROM FIFO IN BURST
                        ;READ ROUTINE.
DATA_BUF  EQU   0XXH    ;SYMBOLIC ADDRESS FOR A 16 BIT DATA BUFFER
CNTRL_BUF EQU   0XXH    ;SYMBOLIC ADDRESS FOR AN 8 BIT BUFFER USED
                        ;IN ROUTINES FOR CONTROL BYTE.
RSLT_NUM  EQU   0XXH    ;SYMBOLIC DEFINITION FOR THE NUMBER OF
                        ;RESULTS TO BE READ FROM FIFO IN BURST READ

;*****************************************************************************
; SERIAL DAS READS AND WRITES ARE PERFORMED BY SUBROUTINES SER_WR & SER_RD,
; THESE ROUTINES USE THE "CNTRL_BUF" REGISTER AS CONTROL INPUT AND THE
; "DATA_BUF" REGISTER AS DATA BUFFER, FOR WRITES DATA IS LOADED ON THE
; "DATA_BUF" REGISTER, AND FOR READS DATA RETURNS IN THE "DATA_BUF" REGISTER.
;*****************************************************************************

;--- AN EXAMPLE OF A WRITE TO CONFIGURATION REGISTER:

        MOV     CNTRL_BUF,#WCONFIG      ;LOAD CNTRL_BUF WITH WRITE CONTROL
                                        ;BYTE
        MOV     DATA_BUF,#02H           ;LOAD LOW ORDER BYTE OF DATA TO
                                        ;DATA_BUF
        MOV     DATA_BUF+1,#00H         ;LOAD HIGH ORDER BYTE OF DATA TO
                                        ;DATA_BUF
        LCALL   SER_WR                  ;SER_WR ROUTINE TRANSFERS THE DATA

;--- AN EXAMPLE OF A READ FROM CONFIGURATION REGISTER:

        MOV     CNTRL_BUF,#RTIMER       ;LOAD CNTRL_BUF WITH READ CONTROL
                                        ;BYTE
        LCALL   SER_RD                  ;SER_RD ROUTINE READS THE DATA
```

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1

7.0 Digital Interface (Continued)

8051 Assembly Code Example (Continued)

```
;*****************************************************************************
; DATA WRITE SUBROUTINE "SER_WR", FOR A SERIAL WRITE TO THE DAS. BEFORE CALLING THE
; ROUTINE, THE WRITE CONTROL BYTE SHOULD BE LOADED IN THE "CNTRL_BUF"
; AND THE DATA TO BE WRITTEN TO THE SDAS SHOULD BE LOADED IN THE "DATA_BUF".
;*****************************************************************************

SER_WR:
        CLR     SDAS_SLCT               ;SELECT THE SDAS, CHIP SELECT=0
        CLR     S_DONE                  ;CLEAR SEND CYCLE DONE FLAG
        MOV     SBUF,CNTRL_BUF          ;START SENDING THE WRITE CONTROL BYTE
SENDW:  JNB     S_DONE,SENDW            ;WAIT HERE UNTIL SEND CYCLE COMPLETED

        CLR     S_DONE                  ;CLEAR SEND CYCLE DONE FLAG
        MOV     SBUF,DATA_BUF           ;START SENDING LOW ORDER BYTE OF DATA
SEND1:  JNB     S_DONE,SEND1            ;WAIT HERE UNTIL SEND CYCLE COMPLETED

        CLR     S_DONE                  ;CLEAR SEND CYCLE DONE FLAG
        MOV     SBUF,DATA_BUF+1         ;START SENDING HIGH ORDER BYTE OF DATA
SEND2:  JNB     S_DONE,SEND2            ;WAIT HERE UNTIL SEND CYCLE COMPLETED

        SETB    SDAS_SLCT               ;DESELECT THE SDAS, CHIP SELECT=1
        RET
;*****************************************************************************
; DATA READ SUBROUTINE "SER_RD", FOR A SERIAL READ  FROM THE DAS. BEFORE CALLING THE
; ROUTINE, THE READ CONTROL BYTE SHOULD BE LOADED ON THE "CNTRL_BUF"
; AND THE DATA IS LOADED IN THE "DATA_BUF" UPON RETURN FROM SUBROUTINE.
;*****************************************************************************
SER_RD:
        CLR     SDAS_SLCT               ;SELECT THE SDAS, CHIP SELECT=0
        CLR     S_DONE                  ;CLEAR SEND CYCLE DONE FLAG
        MOV     SBUF,CNTRL_BUF          ;START SENDING THE READ CONTROL BYTE
SENDR:  JNB     S_DONE,SENDR            ;WAIT HERE UNTIL SEND CYCLE COMPLETED

        SETB    R_EN                    ;ENABLE DATA RECEIVE CYCLES

        CLR     R_DONE                  ;START A DATA BYTE RECEIVE CYCLE
RCV1:   JNB     R_DONE,RCV1             ;WAIT HERE UNTIL RECEIVE COMPLETED
        MOV     DATA_BUF,SBUF           ;STORE LOW ORDER BYTE IN DATA_BUF

        CLR     R_DONE                  ;START A DATA BYTE RECEIVE CYCLE
RCV2:   JNB     R_DONE,RCV2             ;WAIT HERE UNTIL RECEIVE COMPLETED
        MOV     DATA_BUF+1,SBUF         ;STORE HIGH ORDER BYTE IN DATA_BUF

        SETB    SDAS_SLCT               ;DESELECT THE SDAS, CHIP SELECT=1
        CLR     R_EN                    ;DISABLE DATA RECEIVE CYCLES
        RET
```

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7.0 Digital Interface (Continued)

8051 Assembly Code Example (Continued)

```
;*************************************************************************
; FIFO BURST READ SUBROUTINE "RD_FIFO", FOR READING THE CONVERSION RESULTS
; FROM FIFO IN BURST READ MODE. DATA IS READ FROM FIFO AND STORED IN THE
; SYSTEM MEMORY STARTING FROM THE "DATA_BLK" ADDRESS. NUMBER OF CONVERSION
; RESULTS BEING READ IS "RSLT_NUM". THIS ROUTINE USES THE R0 AND R1 REGISTERS.
; IT IS ASSUMED THAT THEY ARE IN THE PRESENT REGISTER BANK.
; R0 IS THE POINTER TO "DATA_BLK" WHERE THE CONVERSION RESULTS ARE STORED.
; R1 IS USED AS A COUNTER TO KEEP TRACK OF THE NUMBER OF RESULTS TO BE READ
; FROM FIFO.
;*************************************************************************
RD_FIFO:
        MOV     R0,DATA_BLK             ;SETTING DATA BLOCK POINTER
        MOV     A,#RSLT_NUM             ;NUMBER OF RESULTS TO BE READ IN ACC
        RL      A                       ;CALCULATING # OF DATA BYTES TO BE
                                        ;READ FROM FIFO, EACH CONVERSION
                                        ;RESULTS IS 2 BYTES
        MOV     R1,A                    ;NUMBER OF DATA BYTES TO R1 COUNTER
        DEC     R1                      ;TOTAL DATA BYTES MINUS 1 IN COUNTER

        CLR     SDAS_SLCT               ;SELECT THE SDAS, CHIP SELECT=0
        CLR     S_DONE                  ;CLEAR SEND CYCLE DONE FLAG
        MOV     SBUF,#RBFIFO            ;START SENDING THE FIFO BURST READ
                                        ;CONTROL BYTE
SENDB:  JNB     S_DONE,SENDB            ;WAIT HERE UNTIL SEND CYCLE COMPLETED

        SETB    R_EN                    ;ENABLE DATA RECEIVE CYCLES

RD_LP:  CLR     R_DONE                  ;START A DATA BYTE RECEIVE CYCLE
RCVB:   JNB     R_DONE,RCVB             ;WAIT HERE UNTIL RECEIVE COMPLETED
        MOV     @R0,SBUF                ;STORE DATA BYTES IN DATA_BLK
        INC     R0                      ;POINTING TO NEXT DATA LOCATION
        DJNZ    R1,RD_LP                ;READ NEXT BYTE IF NOT THE LAST ONE

        SETB    SDAS_SLCT               ;DESELECT THE SDAS, BEFOR READING
                                        ;THE LAST BYTE, BURST READ TERMINATION
        CLR     R_DONE                  ;START A DATA BYTE RECEIVE CYCLE
RCVL:   JNB     R_DONE,RCVL             ;WAIT HERE UNTIL RECEIVE COMPLETED
        MOV     @R0,SBUF                ;STORE THE LAST DATA BYTE

        CLR     R_EN                    ;DISABLE DATA RECEIVE CYCLES
        RET
;*************************************************************************
; THIS ROUTINE INITIALIZES THE SDAS SERIAL INTERFACE IN CASE THAT A
; COMMUNICATION CYCLE HAS BEEN INTERRUPTED. THIS ROUTINE APPLYS 24
; SERIAL CLOCK PULSES TO THE DAS WHILE ITS CHIP SELECT
; IS HIGH. THIS ROUTINE CAN BE USED AT THE START OF THE PROGRAM DURING CODE
; DEVELOPMENT OR ANYWHERE THAT A READ OR WRITE CYCLE MUST BE INTERRUPTED
; BECAUSE OF THE SYSTEM REQUIREMENT.
;*************************************************************************
SDAS_SER_PORT_RST:
        SETB    SDAS_SLCT               ;DESELECT THE SDAS, CHIP SELECT=1
        SETB    R_EN                    ;ENABLE DATA RECEIVE CYCLES

        CLR     R_DONE                  ;START A CYCLE, 8 PULSES APPLIED
TRY1:   JNB     R_DONE,TRY1             ;WAIT HERE UNTIL CYCLE COMPLETED
        CLR     R_DONE                  ;START A CYCLE, 8 PULSES APPLIED
TRY2:   JNB     R_DONE,TRY2             ;WAIT HERE UNTIL CYCLE COMPLETED
        CLR     R_DONE                  ;START A CYCLE, 8 PULSES APPLIED
TRY3:   JNB     R_DONE,TRY3             ;WAIT HERE UNTIL CYCLE COMPLETED

        CLR     R_EN                    ;DISABLE DATA RECEIVE CYCLES
        RET
```

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7.0 Digital Interface (Continued)

7.3 TMS320 INTERFACE MODE

The TMS320 interface mode is designed to work directly with the serial interface port of the TMS320C3x and TMS320C5x families of digital signal processors. This interface uses five lines: two data lines (DX, DR), two frame synchronization signal lines (FSX, FSR), and a serial clock line (SCLK). Note that the TMS320C3x/5x serial interface has two separate serial clock lines for transmit and receive called CLKX and CLKR, but the LM12434 and LM12{L}438 only uses one clock input for both receive and transmit. Typically, CLKX is specified as an output and drives SCLK as well as CLKR (defined as an input). The serial clock for this interface mode is a free running clock, with the data stream synchronized by SCLK. The start of each data transfer (the beginning of a data packet) is synchronized by FSX (Transmit Frame Sync) or FSR (Receive Frame Sync). This interface can communicate with one device; no device select signal is used. The following discussion assumes that the reader has a basic knowledge of the architecture and operation of the TMS320C3x/5x serial interface port.

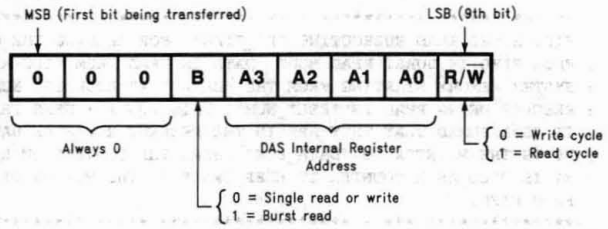
The TMS320 interface mode is selected when the MODESEL1 and MODESEL2 pins have the logic state of "11". *Figure 16* shows a typical connection diagram for the LM12434 and LM12{L}438 in the TMS320 serial interface mode. The FSR, FSX, DX, DR, and SCLK lines are assigned to interface pins P1 through P5.

Data transfer in this mode is programmable by the processor for 8-, 16-, 24-, or 32-bit data packets for the TMS320C3x and 8-, or 16-bit data packets for TMS320C5x. The LM12434 and LM12{L}438 uses 16-bit and 32-bit data packets. For the TMS320C5x the 32-bit packet is composed of two successive 16-bit packets with no gaps between them. The data bits in each packet are transferred MSB first, and are shifted in on the rising edge of SCLK and are stable and captured at the falling edge of the SCLK. As with the "Standard" and "8051" interface modes, the LM12434 and LM12{L}438 has three different communication cycles: write cycle, read cycle and burst read cycle. At the start of each data transfer cycle, a stream of 9 data bits (the "command packet") is written to the LM12434 and LM12{L}438 and informs it about the communication cycle. The placement of these 9 bits in the data packet is different in the read and write cycles and is discussed for each case separately. The command packet carries the following information:

— what type of data transfer (communication cycle) is started

— which device register is to be accessed

The command packet has the following format:



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The first bit of the command packet is always the MSB of the data packet to to be transferred.

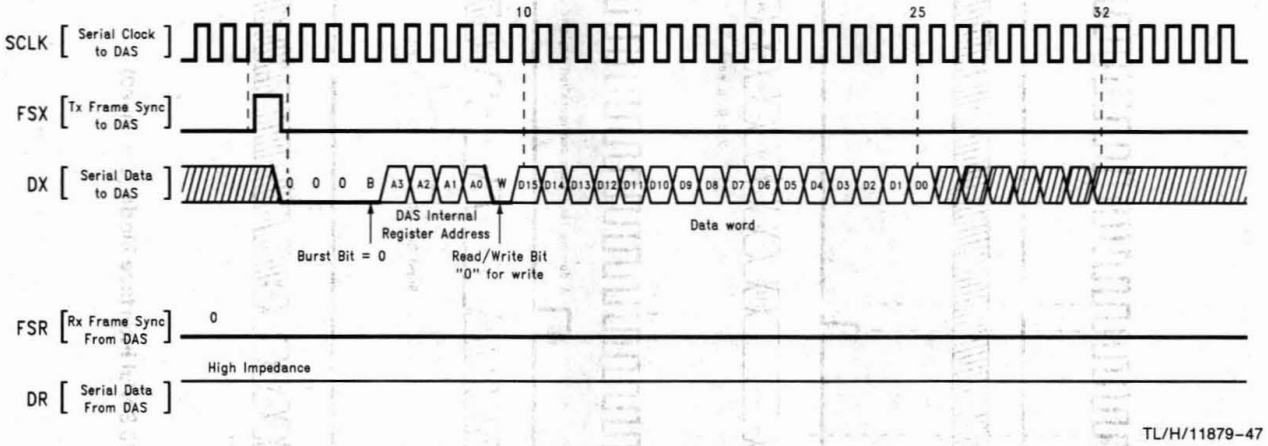
Figure 15 shows the timing diagrams for the three communication cycles. *Figure 15a* shows a write cycle. *Figure 15b* shows a read cycle, and *Figure 15c* shows a burst read cycle. Note that these timing diagrams depict general relationships between the SCLK edges, the data bits and the frame synchronization signals (FSX, FSR). These diagrams are not meant to show guaranteed timing performance. (See specification tables for parametric switching characteristics.)

Write cycle: A write cycle begins with an FSX pulse from the processor. The first data bit is received by the DAS on the DX line during the next SCLK falling edge after the falling edge of FSX. A 32-bit data packet is written to the DAS. The TMS320C3x does this with a 32-bit transfer, using its serial port 32-bit register. With the TMS320C5x family two successive 16-bit transfers are initiated without any gap in between. The first 9 bits (MSBs) of the data are the command packet with the R/$\overline{W}$ bit and B bit equal to zero. Following the command packet, a 16-bit data stream starts on the falling edge of the 10th SCLK cycle and continues through the 25th cycle. The last 7 bits in the 32-bit data packet are "don't care" and are ignored by the DAS. The data is written to the register addressed in the command packet (A3, A2, A1, A0). There is no activity on the FSR and DR lines during a write cycle. The write cycle is completed after the last data bit is transferred.

Read cycle: A read cycle also begins with an FSX pulse from the processor. The read cycle uses 16-bit data transfer. Following the FSX pulse, 16 bits of data are written to the DAS on the DX line. The first 9 bits (MSBs) of data are the command packet with the R/$\overline{W}$ bit equal to one and the B bit equal to zero. The last 7 bits (LSBs) are "don't care" and are ignored by the DAS. About 3 to 4 CLK (the DAS main clock input, not the SCLK) cycles after the R/$\overline{W}$ bit is received, the DAS generates an FSR pulse to initiate the data transfer. Following the FSR pulse, the DAS will send 16 bits of data to the processor on the DR line. The first bit (MSB) of the data appears on the DR line on the next SCLK cycle following the FSR pulse. The data is read from the register addressed in the command packet. The read cycle is completed after the last data bit is transferred.

7.0 Digital Interface (Continued)

Burst read cycle: A burst read cycle starts the same way as a single read cycle, but the B bit in the command packet is set to one, indicating a burst read cycle. After the first 16 bits of data carrying the command packet is written to the DAS, the DAS begins to send out the data words from the addressed register on the DR line repeatedly. Each data word is preceded by an FSR pulse for synchronization. To terminate a burst read cycle, the processor does a dummy read from the configuration register during the last data word. This dummy read should be started so that its FSR pulse occurs during the 15th to 17th SCLK cycle of the last data word as shown in *Figure 15c*. The dummy read terminates the burst read cycle and shifts out the contents of the configuration register on the DR line. This data can be discarded. After transfer of the last data bit from the configuration register, the DAS is ready for a new communication cycle to begin.


SCLK [Serial Clock to DAS]
FSX [Tx Frame Sync to DAS]
DX [Serial Data to DAS]
FSR [Rx Frame Sync From DAS]
DR [Serial Data From DAS]
1
10
25
32
0 0 0 B A3 A2 A1 A0 W D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
DAS Internal Register Address
Data word
Burst Bit = 0
Read/Write Bit "0" for write
0
High Impedance

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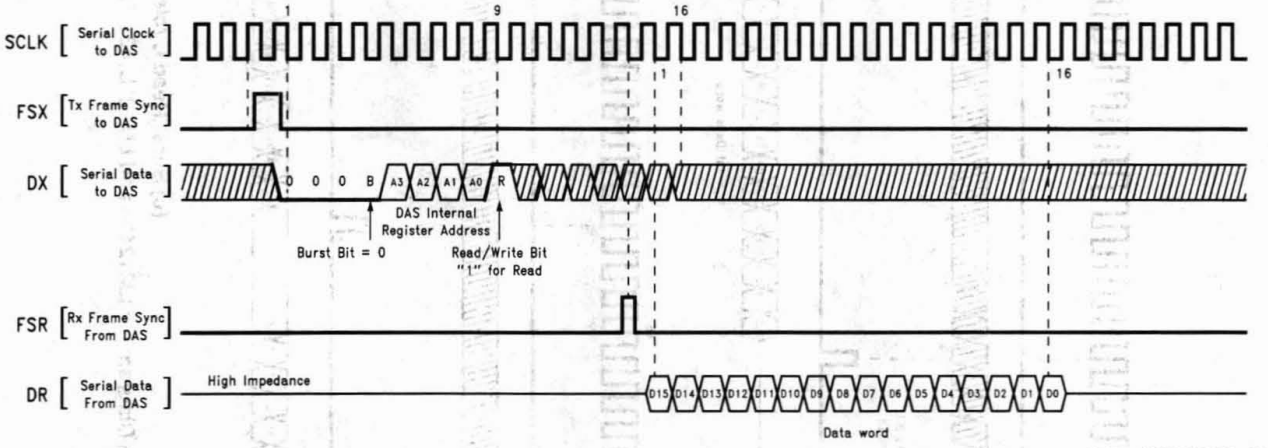
(a) Write Cycle


SCLK [Serial Clock to DAS]
FSX [Tx Frame Sync to DAS]
DX [Serial Data to DAS]
FSR [Rx Frame Sync From DAS]
DR [Serial Data From DAS]
1
9
16
1
16
0 0 0 B A3 A2 A1 A0 R
DAS Internal Register Address
Data word
Burst Bit = 0
Read/Write Bit "1" for Read
High Impedance
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

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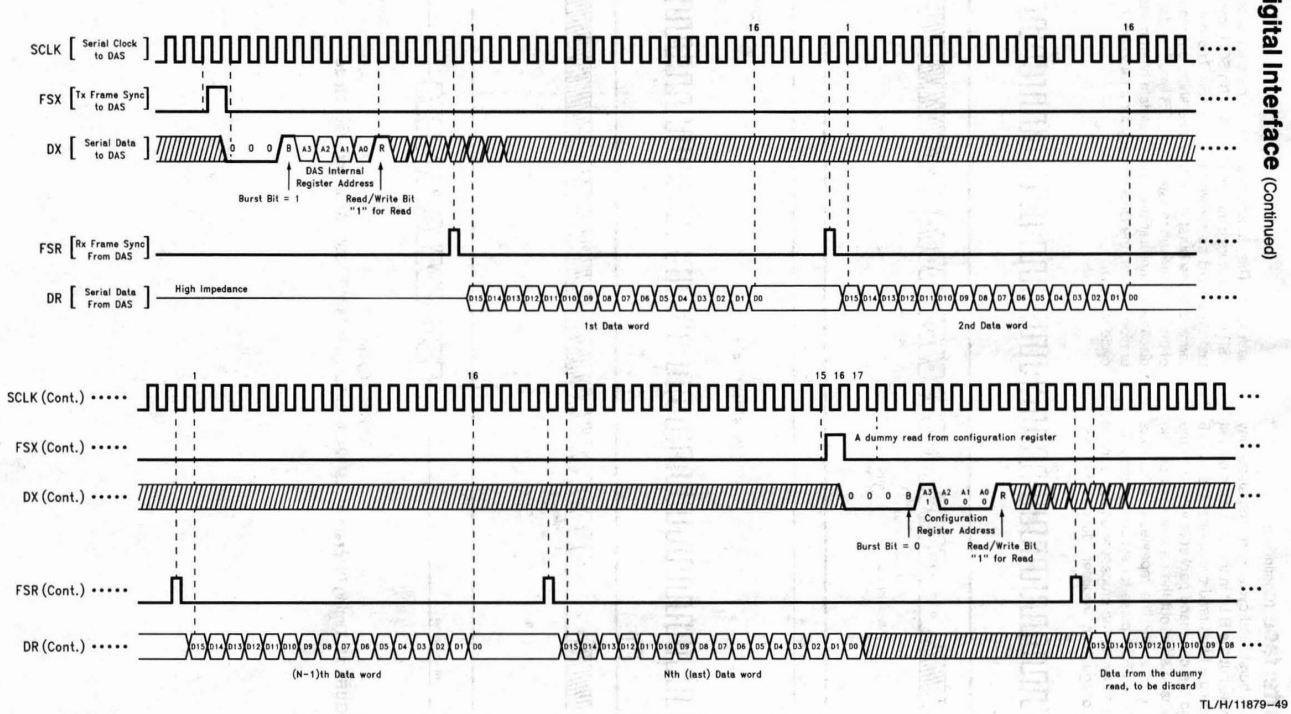
(b) Read Cycle

FIGURE 15. Timing Diagram for LM12434 and LM12{L}438 TMS320 Serial Interface Mode


SCLK [Serial Clock to DAS]
FSX [Tx Frame Sync to DAS]
DX [Serial Data to DAS]
0 0 0 B A3 A2 A1 A0 R
DAS Internal Register Address
Burst Bit = 1
Read/Write Bit "1" for Read
FSR [Rx Frame Sync From DAS]
DR [Serial Data From DAS]
High Impedance
1st Data word
2nd Data word
SCLK (Cont.)
FSX (Cont.)
DX (Cont.)
A dummy read from configuration register
Configuration Register Address
Burst Bit = 0
Read/Write Bit "1" for Read
FSR (Cont.)
DR (Cont.)
(N-1)th Data word
Nth (last) Data word
Data from the dummy read, to be discard

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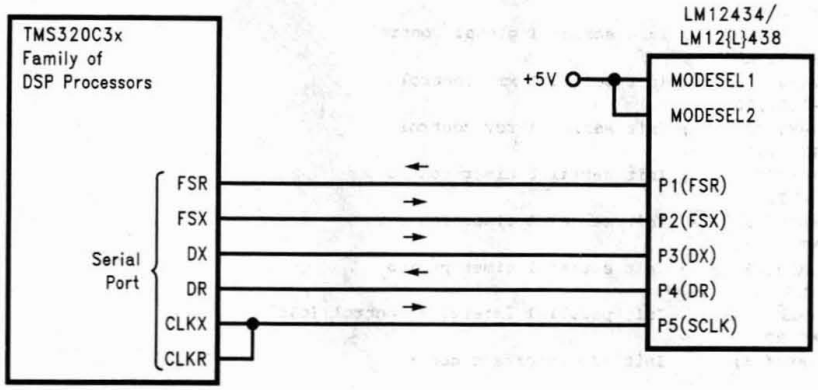
(c) Burst Read Cycle

FIGURE 15. Timing Diagram for LM12434 and LM12{L}438 TMS320 Serial Interface Mode (Continued)

7.0 Digital Interface (Continued)

7.3.1 Example of Interfacing to the TMS320C3x



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Note: Other device pins are not shown.

FIGURE 16. LM12434 and LM12{L}438 in the TMS320 Interface Mode

TMS320C3x Assembly Code Example

```
; TMS320C3x ASSEMBLY ROUTINES FOR INTERFACE TO THE LM12434 AND LM12{L}438 SERIAL DAS
; LM12438 REGISTER ADDRESSES
CONFIG          .word 00000008H         ; CONFIGUREATION REGISTER
INTEN           .word 00000009H         ; INTERRUPT ENABLE REGISTER
INTSTAT         .word 0000000AH         ; INTERRUPT STATUS REGISTER
TIMER           .word 0000000BH         ; TIMER REGISTER
FIFO            .word 0000000CH         ; FIFO
FIFODATA        .word 00000000H
                .space 32               ; 32 reserved spaces for FIFO data
LIMIT           .word 0000000DH         ; LIMIT REGISTER

; INSTRUCTION RAM 0-8 (NOTE: CONFIG. REG. RAM POINTER SELECTS BANKS 0, 1 OR 2)

RAM0            .word 00000000H         ; INSTRUCTION RAM 0
RAM1            .word 00000001H         ; INSTRUCTION RAM 1
RAM2            .word 00000002H         ; INSTRUCTION RAM 2
RAM3            .word 00000003H         ; INSTRUCTION RAM 3
RAM4            .word 00000004H         ; INSTRUCTION RAM 4
RAM5            .word 00000005H         ; INSTRUCTION RAM 5
RAM6            .word 00000006H         ; INSTRUCTION RAM 6
RAM7            .word 00000007H         ; INSTRUCTION RAM 7
CLNDATA         .word 0000FFFFH         ; USED FOR ZEROING DON'T CARE DATA BITS

        .text
* THE PROCESSOR IS INITIALIZED. THE REMAINING APPLICATION-
* DEPENDENT PART OF THE SYSTEM (BOTH ON- AND OFF-CHIP SHOULD
* NOW BE INITIALIZED.
*
* FIRST, INITIALIZE THE CONTROL REGISTER. IN THIS EXAMPLE,
* EVERYTHING IS INITIALIZED TO ZERO SINCE THE ACTUAL INITIALIZATION
* IS APPLICATION DEPENDENT.
*
        LDI     @CTRL,AR0       ; LOAD in AR0 the pointer to control
*                               ; registers
        LDI     @DMACTL,R0
        STI     R0,*+AR0(0)     ; Init DMA control
        LDI     @TIM0CTL,R0
        STI     R0,*+AR0(32)    ; Init timer 0 control
        LDI     @TIM1CTL,R0
        STI     R0,*+AR0 (48)   ; Init timer 1 control
        LDI     @SERGLOB0,R0
        STI     R0,*+AR0(64)    ; Init serial 0 global control
        LDI     @SERPRTX0,R0
        STI     R0,*+AR0(66)    ; Init serial 0 xmt control
        LDI     @SERPRTR0,R0
        STI     R0,*+AR0(67)    ; Init serial 0 rcv control
```

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7.0 Digital Interface (Continued)

TMS320C3x Assembly Code Example (Continued)

```
        LDI     @SERTIM0,R0
        STI     R0,*+AR0(68)    ; Init serial 0 timer control
        LDI     @SERGLOB1,R0
        STI     R0,*+AR0(80)    ; Init serial 1 global control
        LDI     @SERPRTX1,R0
        STI     R0,*+AR0(82)    ; Init serial 1 xmt control
        LDI     @SERPRTR1,R0
        STI     R0,*+AR0(83)    ; Init serial 1 rcv control
        LDI     @SERTIM1,R0
        STI     R0,*+AR0(84)    ; Init serial 1 timer control
;       LDI     @STIMCNT1,R0
;       STI     R0,*+AR0(85)    ; Init serial 1 timer counter
;       LDI     @STIMPRD1,R0
;       STI     R0,*+AR0(86)    ; Init serial 1 timer period
        LDI     @PARINT,R0
        STI     R0,*+AR0(100)   ; Init parallel interface control (c30 only)
        LDI     @IOINT,R0
        STI     R0,*+AR0(96)    ; Init I/O interface control
*
        LDI     @STCK,SP        ; Initialize the stack pointer
        OR      2000H,ST        ; Global interrupt enable
*
        BR      BEGIN           ; Branch to the beginning of application.
BEGIN   NOP
        LDI     0,IOF           ; PROGRAM XF1 PORT AS AN INPUT PORT
        LDI     @CTRL,AR0       ; LOAD in AR0 the pointer to control
        LDI     @CONFIG,R0
        LDI     0082H,R1        ; SYNC. PIN OUTPUT
        CALL    SWRITE          ; SOFT RESET LM12438

        LDI     @INTEN,R0
        LDI     0714H,R1        ; 32 CONVERSIONS
        LDI     0C714H,R1       ; 24 CONVERSIONS
        CALL    SWRITE          ; INIT. INTERRUPT ENABLE REG.

        LDI     @TIMER,R0
        LDI     0AAAAH,R1
        CALL    SWRITE          ; LOAD SOME VALUE IN TIMER

        LDI     @RAM0,R0        ; INSTRUCTIONS FOR 8 CONVERSION
        LDI     0000H,R1        ; ON EACH CHANNEL (0-7) ALL SINGLE ENDED
        CALL    SWRITE          ; SET RAM0
        LDI     @RAM1,R0
        LDI     0004H,R1
        CALL    SWRITE          ; SET RAM1
        LDI     @RAM2,R0
        LDI     0008H,R1
        CALL    SWRITE          ; SET RAM2
        LDI     @RAM3,R0
        LDI     000CH,R1
        CALL    SWRITE          ; SET RAM3
        LDI     @RAM4,R0
        LDI     0010H,R1
        CALL    SWRITE          ; SET RAM4
        LDI     @RAM5,R0
        LDI     0014H,R1
        CALL    SWRITE          ; SET RAM5
        LDI     @RAM6,R0
        LDI     0018H,R1
        CALL    SWRITE          ; SET RAM6
        LDI     @RAM7,R0
        LDI     001CH,R1
        CALL    SWRITE          ; SET RAM7

        LDI     @CONFIG,R0      ; START FULL CALIBRATION
        LDI     0088H,R1        ; SYNC. PIN OUTPUT
        CALL    SWRITE
```

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7.0 Digital Interface (Continued)

TMS320C3x Assembly Code Example (Continued)

```
CHKINT1 TSTB    80H,IOF         ; TEST XF1 INPUT CONNECTED TO LM12438'S INTERRUPT
        BNZ     CHKINT1         ; FOR COMPLETION OF FULL CALIBRATION

        LDI     @INTSTAT,R0
        CALL    SREAD           ; READ INTERRUPT STATUS REG.

DOAGAIN LDI     @CONFIG,R0      ; IF FULL CALIBRATION IS DONE SET THE START BIT
        LDI     0081H,R1        ; OF LM12438 CONFIG. REG. (SYNC. PIN OUTPUT)
        CALL    SWRITE          ; START LM12438 SEQUENCER

CHKINT2 TSTB    80H,IOF         ; TEST XF1 INPUT CONNECTED TO LM12438'S INTERRUPT
        BNZ     CHKINT2         ; (COMPLETION OF 24 FIFO CONVERSIONS)

        LDI     @CONFIG,R0
        LDI     0080H,R1        ; STOP THE CONVERSION (IS NOT NECESSARY)
        CALL    SWRITE
        LDI     @INTSTAT,R0
        CALL    SREAD           ; READ INTERRUPT STATUS REG.
        LDI     32,R4
FLOOP   LDI     R4,R1
        LDI     @FIFO,R0        ; READ FIFO
        CALL    BREAD
        SUBB    1,R4
        BNZ     FLOOP
        LDI     @CONFIG,R0
        LDI     0002H,R1        ; RESET LM12438 (SYNC. PIN OUTPUT)
        CALL    SWRITE
        BR      DOAGAIN
        IDLE

; LM12438 BURST READ ROUTINE THROUGH SERIAL PORT1
BREAD   PUSH    ST              ; SAVE STATUS REG.
        PUSH    AR0             ; SAVE AR0
        PUSH    AR1             ; SAVE AR1
        PUSH    AR2             ; SAVE AR2
        PUSH    R0              ; SAVE R0
        PUSH    R1              ; SAVE R1
        PUSH    R2              ; SAVE R2
        PUSH    R3              ; SAVE R3
        PUSH    R4              ; SAVE R4

        LDI     @CTRL,AR0       ; LOAD in AR0 the pointer to control
        LDI     @FIFODATA,AR2   ; USE AR2 AS POINTER TO FIFO DATA
        LDI     @SERGLOB1R,R2   ; PREPARE FOR 16 BIT TRANSMIT

        CMPI    0,R1            ; IF COUNTER IS 0 (USER'S ERROR)
        BZ      BDONE2          ; TERMINATE NOW ELSE CONTINUE

        CMPI    1,R1            ; IF A SINGLE READ REQUIRED THEN
        BZ      SINGLE          ; CALL THE SINGLE READ SUBROUTINE
        BR      MLTIPLE         ; ELSE GO ON

SINGLE  LDI     @FIFO,R0        ; FOR SINGLE READ FIFO ADDRESS IS
        CALL    SREAD           ; CALLING SINGLE READ ROUTINE
        STI     R1,*AR2++(1)    ; STORE READ DATA INTO FIFODATA
        BR      BDONE2          ; TERMINATE

MLTIPLE LDI     13,R4           ; SET UP R4 AS THE DELAY COUNTER
        LDI     @SERGLOB1R,R2   ; PREPARE FOR 16 BIT TRANSMIT
        STI     R2,*+AR0(80)    ; Init serial 1 global control

        RPTS    7               ; POSITION THE ADDRESS
        ROL     R0              ; TO START AT BIT #10
        OR      1080H,R0        ; SET THE READ BIT
        LDI     R0,R3           ; R0 IS FREED FOR LAST READ

        LDI     @CONFIG,R0      ; PREPARE FOR A LAST CONFIG REG. READ
        RPTS    7               ; WHICH WILL STOP LM12438 FROM GENERATING
        ROL     R0              ; FURTHER BURST READS
        OR      80H,R0          ; SET THE READ BIT
```

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7.0 Digital Interface (Continued)

TMS320C3x Assembly Code Example (Continued)

```
        STI     R3,*+AR0(88)    ; Init serial 1 data xmt register
        RPTS    2H              ; PROVIDE DELAY FOR UPDATE OF
        NOP                     ; XSREMPTY BIT IN GLOB CONT REG.
        LDI     1000B,R3
CHKR2   TSTB    *+AR0(80),R3    ; CHECK SER. 1 CONTROL XSREMPTY
        BNZ     CHKR2           ; IF XSREMPTY=1 THEN KEEP CHECKING

COUNT   NOP
        SUBB    1,R1            ; DECREMENT COUNTER (R1) AND CHECK FOR ZERO
        LDI     1,R3            ; PREPARE R3 FOR CHECKING RRDY BIT

RCONT3  TSTB    *+AR0(80),R3
        BZ      RCONT3          ; IF RRDY=0 THEN CHECK AGAIN

RDONE2  LDI     *+AR0(92),R3    ; LOAD DRR (RECEIVED DATA), RRDY IS CLEARED
        AND     0FFFFH,R3       ; CLEAN UP THE UPPER BITS
        STI     R3,*AR2++(1)    ; PLACE READ DATA IN FIFODATA
        CMPI    1,R1            ; IF COUNTER=1 THEN TERMINATE
        BNZ     COUNT           ; ELSE CONTINUE

BSTDONE RPTS    R4              ; WAIT FOR THE 16TH CLOCK RISE
        NOP                     ; BEFORE SENDING THE TERMINATING
                                ; READ FROM CONFIG. REG
        STI     R0,*+AR0(88)    ; XMT FOR LAST READ FROM CONFIG REG
RCONT4  LDI     *+AR0(80),R3    ; READ SER. 1 CONTROL REGISTER TO
        TSTB    0001B,R3        ; CHECK FOR RRDY BIT
        BZ      RCONT4          ; IF RRDY IS 1, EXIT THE BURST ROUTINE

RCONT5  LDI     *+AR0(92),R3    ; READ THE LAST BURST DATA IN DRR
        AND     0FFFFH,R3       ; CLEAN UP THE UPPER BITS
        STI     R3,*AR2++(1)    ; PLACE IT IN FIFODATA

RCONT6  LDI     *+AR0(80),R3    ; READ SER. 1 CONTROL REGISTER TO
        TSTB    0001B,R3          CHECK FOR RRDY BIT
        BZ      RCONT6

BDONE2  LDI     *+AR0(92),R3    ; READ THE DRR (CLEAR RRDY BIT)
        POP     R4              ; RESTORE R4
        POP     R3              ; RESTORE R3
        POP     R2              ; RESTORE R2
        POP     R1              ; RESTORE R1
        POP     R0              ; RESTORE R0
        POP     AR2             ; RESTORE AR2
        POP     AR1             ; RESTORE AR1
        POP     AR0             ; RESTORE AR0
        POP     ST              ; RESTORE ST
        RETS
```

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7.0 Digital Interface (Continued)

TMS320C3x Assembly Code Example (Continued)

```
; LM12438 SINGLE READ ROUTINE THROUGH SERIAL PORT1
SREAD   PUSH    ST              ; SAVE STATUS REG.
        PUSH    AR0             ; SAVE AR0
        PUSH    R0              ; SAVE R0  THE READ ADDRESS
        PUSH    R2              ; SAVE R2
        LDI     @CTRL,AR0       ; LOAD in AR0 the pointer to control
        LDI     @SERGLOB1R,R2   ; PREPARE FOR 16 BIT TRANSMIT
                                ; AND 16 BIT RECIEVE
        STI     R2,*+AR0(80)    ; Init serial 1 global control
        RPTS    7               ; POSITION THE ADDRESS
        ROL     R0              ; TO START AT BIT #10
        OR      80H,R0          ; SET THE READ BIT
        STI     R0,*+AR0(88)    ; Init serial 1 data xmt register
        RPTS    2H              ; PROVIDE DELAY FOR UPDATE OF
        NOP                     ; XSREMPTY BIT IN GLOB CONT REG.
CHKR1   LDI     *+AR0(80),R0    ; READ SER. 1 CONTROL XSREMPTY
        TSTB    1000B,R0        ; CHECK
        BNZ     CHKR1           ; IF IT IS CLEAR (TRANSMIT COMPLETE) CONTINUE

RCONT1  LDI     *+AR0(80),R0    ; READ SER. 1 CONTROL
        TSTB    0001B,R0        ; CHEK RRDY BIT
        BZ      RCONT1          ; IF RRDY IS 1 (RECEIVE COMPLETE) CONTINUE

RDONE1  LDI     *+AR0(92),R1    ; LOAD DRR (RECEIVED DATA) INTO R1
        AND     0FFFFH,R1       ; CLEAN UP UPPER BITS
        POP     R2              ; RESTORE R2
        POP     R0              ; RESTORE R0    THE READ ADDRESS
        POP     AR0             ; RESTORE AR0
        POP     ST              ; RESTORE ST
        RETS
; LM12438 WRITE ROUTINE THROUGH SERIAL PORT1
SWRITE  PUSH    ST              ; SAVE STATUS REG.
        PUSH    AR0             ; SAVE AR0
        PUSH    R2              ; SAVE R2
        LDI     @CTRL,AR0       ; LOAD in AR0 the pointer to control
        LDI     @SERGLOB1W,R2   ; PREPARE FOR 32 BIT TRANSMIT
        STI     R2,*+AR0(80)    ; Init serial 1 global control
        AND     @CLNDATA,R1     ; CLEAN UP UNUSED ADD. BITS
        RPTS    23              ; POSITION THE ADDRESS TO START AT BIT #27
        ROL     R0              ;
        RPTS    6               ; POSITION DATA TO START AT BIT #22
        ROL     R1              ;
        OR      R1,R0           ;
        STI     R0,*+AR0(88)    ; Init serial 1 data xmt register
        RPTS    2H              ; PROVIDE DELAY FOR UPDATE OF
        NOP                     ; XSREMPTY BIT IN GLOB CONT REG.
CHK1    LDI     *+AR0(80),R0    ; READ SER. 1 CONTROL XSREMPTY
        TSTB    1000B,R0        ; CHECK
        BNZ     CHK1            ; IF IT IS CLEAR (TRANSMIT COMPLETE) CONTINUE

WDONE1  POP     R2              ; RESTORE R2
        POP     AR0             ; RESTORE AR0
        POP     ST              ; RESTORE ST
        RETS
```

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7.0 Digital Interface (Continued)

7.4 I²C BUS INTERFACE

The I²C bus is a serial synchronous bus structure. It is a multi-master bus, which means that more than one device capable of controlling the bus can be connected to it. The bus uses 2 wires, serial data (SDA) and serial clock (SCL), to carry information between the devices connected to the bus. Both data and clock lines are bidirectional and are connected to the positive power supply via a pull-up resistor. Each device is identified by a unique address, whether it is a microprocessor/controller or a peripheral such as memory, keyboard, data-converter or display. Each device can operate as either transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters and slaves when performing data transfer. A master is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered slave. It should be apparent that the I²C bus is not merely an interconnecting wire, it embodies comprehensive formats and procedures for addressing, transfer cycles start and stop, clock generation/synchronization and bus arbitration. The following discussion assumes that the reader is familiar with the specification and architecture of the I²C bus.

The LM12434 and LM12{L}438's I²C bus interface is selected when the MODESEL1 and MODESEL2 pins have the logic state of "10". *Figure 18* shows a typical connection diagram for the LM12434 and LM12{L}438 to the I²C bus. As was mentioned, communication on the I²C bus is performed on 2 lines, SCL (serial clock) and SDA (serial data); pins P5 and P4 are assigned to these lines. The DAS operates as a slave on the I²C bus. As a result, the SCL line is an input (no clock is generated by the LM12434 and LM12{L}438) and the SDA line is a bi-directional serial data path. According to I²C bus specifications, the DAS has a 7-bit slave address. The four most significant bits of the slave address are hard wired inside the LM12434 and LM12{L}438 and are "0101". The three least significant bits of the address are assigned to pins P3–P1. Therefore, the LM12434 and LM12{L}438 I²C slave address is:

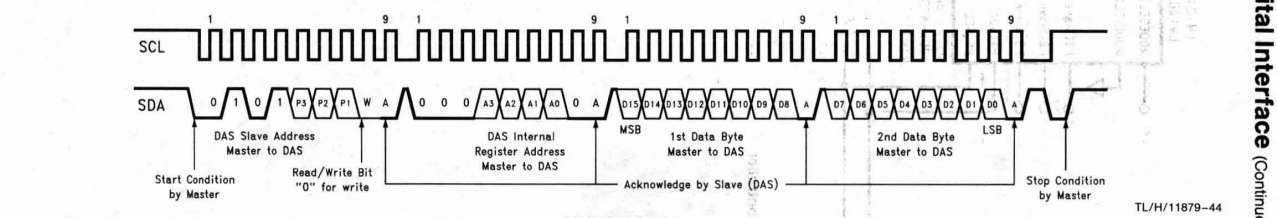
0	1	0	1	P3	P2	P1
MSB						LSB

Tying the P3–P1 pins to different logic levels allows up to eight LM12434 and LM12{L}438's to be addressed on a single I²C bus.

Figure 17 shows the timing diagram for the read and write cycles for the LM12434 and LM12{L}438's I²C interface. This timing diagram depicts the general relationship between the serial clock edges and the data bits. It is not meant to show guaranteed timing performance. (See specification tables for parametric switching characteristics.) The DAS's I²C interface timing parameters fully meet or exceed the I²C bus specification. Data transfer on the I²C bus is byte oriented and the 16-bit data to be written to or read from each register is transferred in two bytes.

Write cycle: A write cycle is illustrated in *Figure 17a*. Communication is initiated with a start condition generated by a master (I²C bus specification), followed by a byte of the DAS's slave address with the read/write bit (8th bit) being "0", indicating a write cycle will follow. At the 9th SCL clock pulse of the first data packet, the DAS pulls the SDA line low ("0") to acknowledge that it has been addressed. The next byte is the address of the DAS register to be accessed. The format of this byte is three "0's" (MSBs) followed by four bits of register address (MSB first as shown) and a "0" as the last bit (LSB). After the DAS acknowledges the address byte, the 16-bit data proceeds in two bytes, beginning with the high order byte (MSB first). The direction of the data in a write cycle is from master to DAS with acknowledgement given by the DAS at the end of each byte. The cycle is completed by a stop condition generated by the master.

Read/burst read cycle: The read and burst read cycles for the I²C interface are combined in a single format. A read cycle is shown in *Figure 17b*. A read cycle starts the same as a write with a slave address byte for write followed by a register address byte. After the register address byte is written to the DAS, the bus should be released without any stop condition. The master then applies a repeat start condition followed by the DAS's slave address, but with the read/write bit being "1", indicating a read request from the master. The DAS (slave) acknowledges its address and beginning with the next byte, the direction of the data will be from DAS to master. The DAS starts to transmit the contents of its register (addressed previously at second byte of the cycle) synchronized with the clocks applied by the master. An even number of data bytes should be read from the DAS (two bytes per register). At the end of each byte received from the DAS the bus master generates an acknowledge. The DAS continues to repeat transmitting its register contents as long as the master is transmitting clocks and acknowledges at the end of each byte. The DAS recognizes the end of the transfer whenever the master does not acknowledge at the end of an even numbered byte. At this point, the master should generate a stop condition as required by the I²C bus specification. Notice that the master may read only one word (single read) or as many words (two bytes each) as it needs using the read procedure.


SCL
SDA
0 1 0 1 P3 P2 P1 W A 0 0 0 A3 A2 A1 A0 0 A D15 D14 D13 D12 D11 D10 D9 D8 A D7 D6 D5 D4 D3 D2 D1 D0 A
MSB
LSB
DAS Slave Address Master to DAS
DAS Internal Register Address Master to DAS
1st Data Byte Master to DAS
2nd Data Byte Master to DAS
Start Condition by Master
Read/Write Bit "0" for write
Acknowledge by Slave (DAS)
Stop Condition by Master
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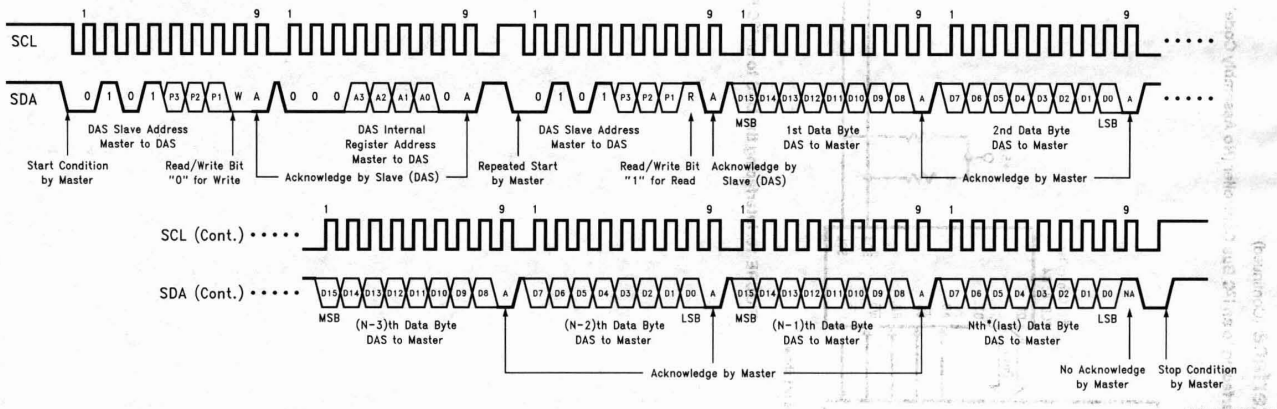
(a) Write Cycle


SCL
SDA
0 1 0 1 P3 P2 P1 W A 0 0 0 A3 A2 A1 A0 0 A 0 1 0 1 P3 P2 P1 R A D15 D14 D13 D12 D11 D10 D9 D8 A D7 D6 D5 D4 D3 D2 D1 D0 A
MSB
LSB
DAS Slave Address Master to DAS
DAS Internal Register Address Master to DAS
Repeated Start by Master
1st Data Byte DAS to Master
2nd Data Byte DAS to Master
Start Condition by Master
Read/Write Bit "0" for Write
Acknowledge by Slave (DAS)
Read/Write Bit "1" for Read
Acknowledge by Slave (DAS)
Acknowledge by Master
SCL (Cont.)
SDA (Cont.)
D15 D14 D13 D12 D11 D10 D9 D8 A D7 D6 D5 D4 D3 D2 D1 D0 A D15 D14 D13 D12 D11 D10 D9 D8 A D7 D6 D5 D4 D3 D2 D1 D0 NA
(N-3)th Data Byte DAS to Master
(N-2)th Data Byte DAS to Master
(N-1)th Data Byte DAS to Master
Nth*(last) Data Byte DAS to Master
Acknowledge by Master
No Acknowledge by Master
Stop Condition by Master
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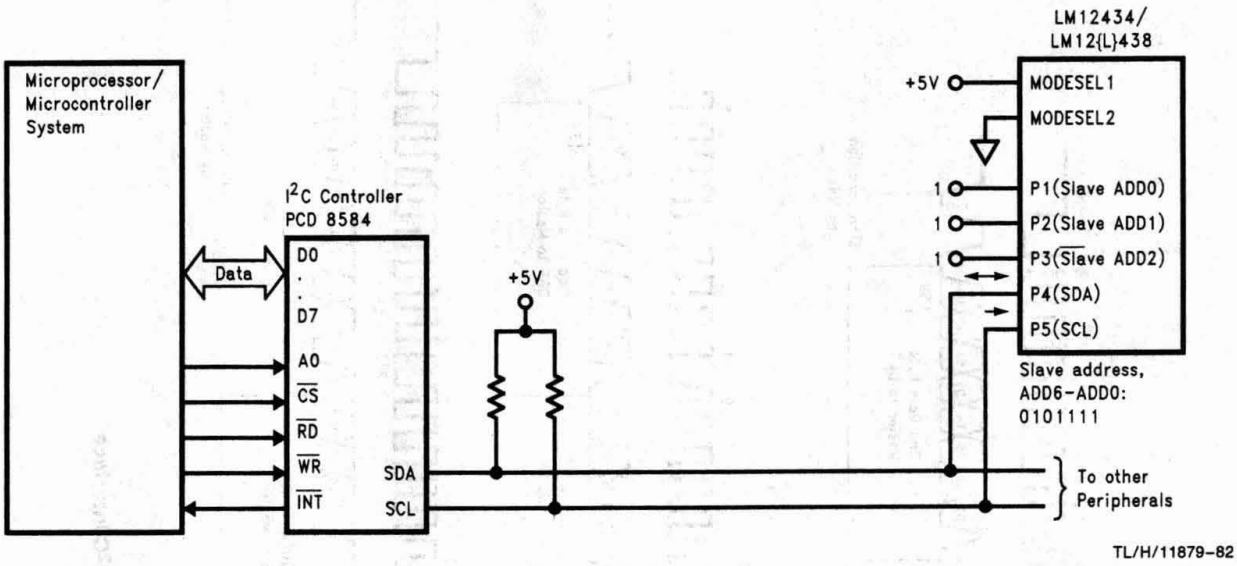
*n should be an even number.

(b) Read Cycle/Burst Read Cycle

FIGURE 17. Timing Diagrams for LM12434 and LM12{L}438 I²C Interface

7.0 Digital Interface (Continued)

7.4.1 Example of Interfacing to an I²C Bus Controller (No Assembly Code)



Note: Other device pins are not shown.

FIGURE 18. Interfacing the DAS to an I²C Bus Controller

8.0 Analog Considerations

8.1 REFERENCE VOLTAGE

The difference between the voltages applied to the V_{REF+} and V_{REF-} is the analog input voltage span (the difference between the voltages applied across two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground, over which 4095 positive and 4096 negative codes exist). The voltage sources driving V_{REF+} or V_{REF-} must have very low output impedance and noise. The circuit in *Figure 19* is an example of a very stable reference appropriate for use with the LM12434 and LM12{L}438.

The ADC can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF+} pin is connected to V_A^+ and V_{REF-} is connected to GND. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions.

For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

8.2 INPUT RANGE

The LM12434 and LM12{L}438's fully differential ADC and reference voltage inputs generate a two's-complement output that is found by using the equation below.

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (4096) - \tfrac{1}{2} \qquad \text{(12-bit)}$$

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (256) - \tfrac{1}{2} \qquad \text{(8-bit)}$$

Round up to the next integer value between −4096 to 4095 for 12-bit resolution and between −256 to 255 for 8-bit resolution if the result of the above equation is not a whole number. As an example, V_{REF+} = 2.5V, V_{REF-} = 1V, V_{IN+} = 1.5V and V_{IN-} = GND. The 12-bit + sign output code is positive full-scale, or 0,1111,1111,1111. If V_{REF+} = 5V, V_{REF-} = 1V, V_{IN+} = 3V, and V_{IN-} = GND, the 12-bit + sign output code is 0,1100,0000,0000.

8.3 INPUT CURRENT

A charging current flows into or out of (depending on the input voltage polarity) the analog input pins, IN0–IN7 at the start of the analog input acquisition time (t_{ACQ}). This current's peak value will depend on the actual input voltage applied.

8.4 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<60Ω for 8 MHz operation), the input charging current will decay, before the end of the S/H's acquisition time, to a value that will not introduce any conversion errors. For higher source impedances, the S/H's acquisition time can be increased. As an example, operating with a 8 MHz clock frequency and maximum acquisition time, the LM12434 and LM12438's analog inputs can handle source impedances as high as 4.17 kΩ. Refer to Section 6.2.1, Instruction RAM "00", Bits 12–15 for further information.

8.5 INPUT BYPASS CAPACITANCE

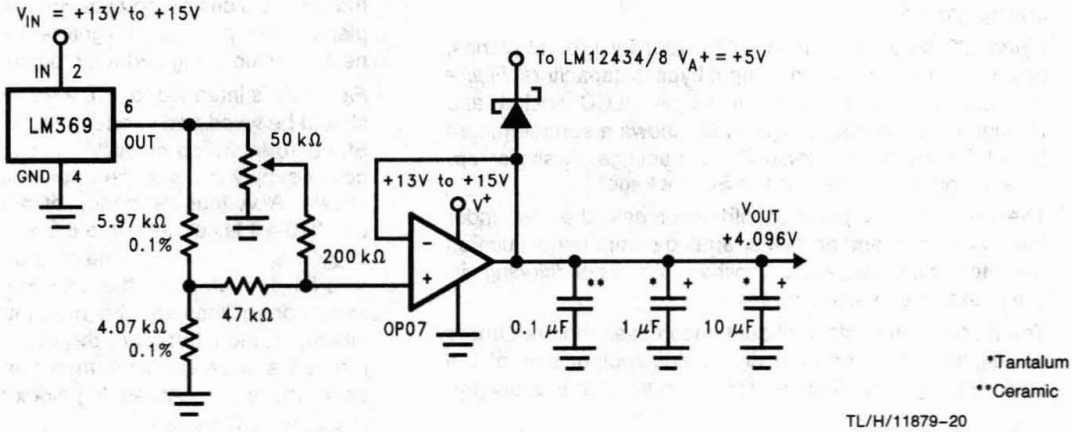
External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, IN0–IN7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

8.6 INPUT NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

8.7 POWER SUPPLY CONSIDERATIONS

Decoupling and bypassing the power supply on a high resolution ADC is an important design task. Noise spikes on the V_A+ (analog supply) or V_D+ (digital supply) can cause conversion errors. The analog comparator used in the ADC will respond to power supply noise and will make erroneous conversion decisions. The DAS is especially sensitive to power supply spikes that occur during the auto-zero or linearity calibration cycles.



TL/H/11879–20

FIGURE 19. Low Drift Extremely Stable Reference Circuit

8.0 Analog Considerations (Continued)

The LM12434/8 is designed to operate from a single +5V power supply. The LM12{L}438 is designed to operate from a single +3.3V supply. The separate supply and ground pins for the analog and digital portions of the circuit allow separate external bypassing. To minimize power supply noise and ripple adequate bypass capacitors should be placed directly between power supply pins and their associated grounds. Both supply pins are generally connected to the same supply source. In systems with separate analog and digital supplies, the DAS should be powered from the analog supply. At least a 10 μF tantalum electrolytic capacitor in parallel with a 0.1 μF monolithic ceramic capacitor is recommended for bypassing each power supply. The key consideration for these capacitors is to have the low series resistance and inductance. The capacitors should be placed as close as physically possible to the supply and ground pins with the smaller capacitor closer to the device. The capacitors also should have the shortest possible leads in order to minimize series lead inductance. Surface mount chip capacitors are optimal in this respect and should be used when possible.

When the power supply regulator is not local on the board, adequate bypassing (a high value electrolytic capacitor) should be placed at the power entry point. The value of the capacitor depends on the total supply current of the circuits on the PC board. All supply currents should be supplied by the capacitor instead of being drawn from the external supply lines, while the external supply charges the capacitor at a steady rate.

The DAS has two V_D+ and DGND pins on two sides of its package. It is recommended to use a 0.1 μF plus a 10 μF capacitor between pins 15 and 16 (V_D+) and 14 (DGND) and a 0.1 μF capacitor between pins 28 (V_D+) and 1 (DGND) for the PLCC package. The respective pins for the SO package are 21 and 22 (V_D+) and 20 (DGND), 6 (V_D+) and 7 (DGND). The layout diagrams in Section 8.8 show the recommended placement for the supply bypass capacitors.

8.8 PC BOARD LAYOUT AND GROUNDING CONSIDERATIONS

To get the best possible performance from the LM12434 and LM12{L}438, the printed circuit boards should have separate analog and digital ground planes. The reason for using two ground planes is to prevent digital and analog ground currents from sharing the same path until they reach a very low impedance power supply point. This will prevent noisy digital switching currents from being injected into the analog ground.

Figure 20 illustrates a favorable layout for ground planes, power supply and reference input bypass capacitors. *Figure 20a* shows a layout using a 28-pin PLCC socket and through-hole assembly. *Figure 20b* shows a surface mount layout for the same 28-pin PLCC package. A similar approach should be used for the SO package.

The analog ground plane should encompass the area under the analog pins and any other analog components such as the reference circuit, input amplifiers, signal conditioning circuits, and analog signal traces.

The digital ground plane should encompass the area under the digital circuits and the digital input/output pins of the DAS. Having a continuous digital ground plane under the data and clock traces is very important. This reduces the overshoot/undershoot and high frequency ringing on these lines that can be capacitively coupled to analog circuitry sections through stray capacitances.

The AGND and DGND in the LM12434 and LM12{L}438 are not internally connected together. They should be connected together on the PC board right at the chip. This will provide the shortest return path for the signals being exchanged between the internal analog and digital sections of the DAS.

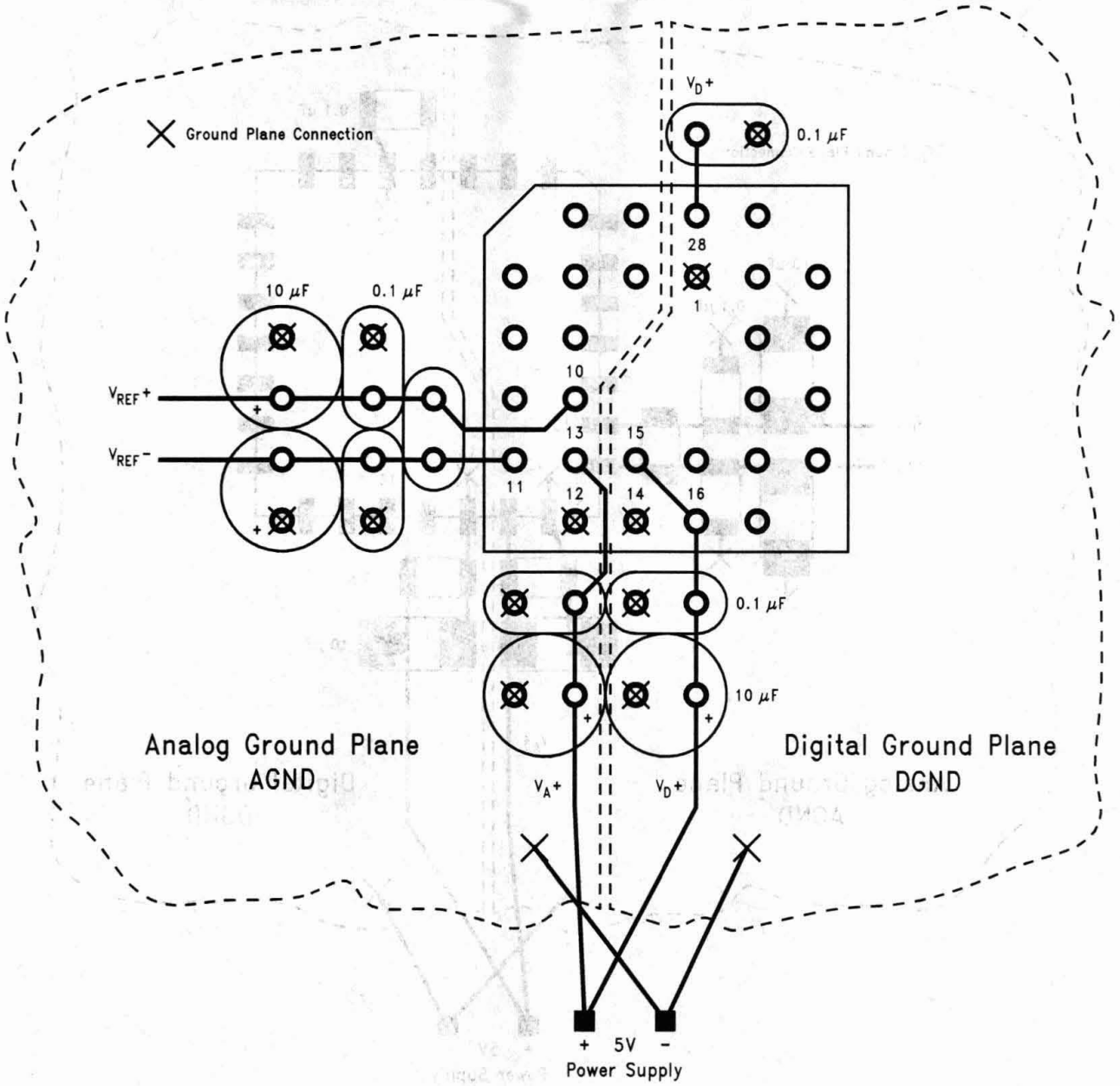
It is also a good design practice to have power plane layers in the PC board. This will improve the supply bypassing (an effective distributed capacitance between power and ground plane layers) and voltage drops on the supply lines. However, power planes are not essential as ground planes are for the performance of the DAS. If power planes are used, they should be separated into two planes and the area and connections should follow the same guidelines as mentioned for the ground planes. Each power plane should be laid out over its associated ground planes, avoiding any overlap between power and ground planes of different types. When the power planes are not used, it is recommended to use separate supply traces for the V_A+ and V_D+ pins from a low impedance supply point (the regulator output or the power entry point to the PC board). This will help ensure that the noisy digital supply does not corrupt the analog supply.

When measuring AC input signals with the DAS, any cross-talk between analog input/output lines and the reference lines (IN0–IN7, MUXOUT±, S/H IN±, V_{REF}±) should be minimized. Cross talk is minimized by reducing any stray capacitance between the lines. This can be done by increasing the clearance between traces, keeping the traces as short as possible, shielding traces from each other by placing them on different sides of the AGND plane, or running AGND traces between them.

Figure 20 also shows the reference input bypass capacitors. Here the reference inputs are considered to be differential. The performance of the DAS improves by having a 0.1 μF capacitor between the $V_{REF}+$ and $V_{REF}-$, and by bypassing in a manner similar to that described in Section 8.7 for the supply pins. When a single ended reference is used, $V_{REF}-$ is connected to AGND and only two capacitors are used between $V_{REF}+$ and $V_{REF}-$ (0.1 μF + 10 μF). It is recommended to directly connect the AGND side of these capacitors to the $V_{REF}-$ instead of connecting $V_{REF}-$ and the ground sides of the capacitors separately to the ground planes. This provides a significantly lower-impedance connection when using surface mount technology.

Figure 21 is intended to give a general idea of how the DAS should be wired and interfaced to a μC that operates in the Standard Interface mode. All necessary analog and digital power supply and voltage reference bypass capacitors are shown. A voltage reference of 4.096V generated by the LM4040-4.1 is connected to the $V_{REF}+$ of the DAS and the $V_{REF}-$ is connected to analog ground. The serial interface pins P1 through P5 of the DAS are connected to the μC's serial control lines and the interrupt pin of the DAS is wired directly to the interrupt of the μC. In this diagram the DAS runs on a separate clock than the μC, however, in some applications the DAS analog clock (CLK) may be a derivative of the μC's clock.

8.0 Analog Considerations (Continued)



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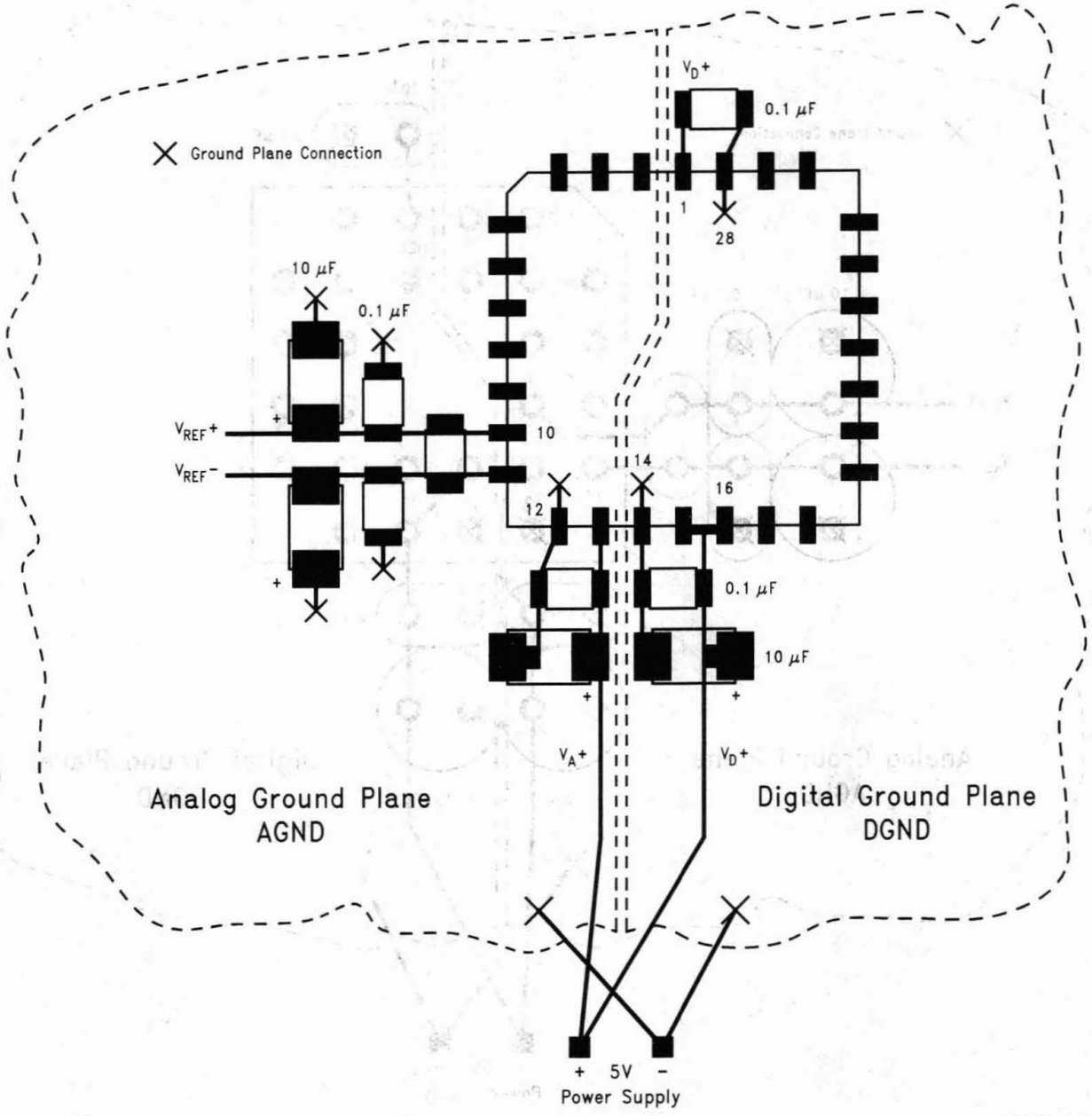
(a) Through Hole Technology with 28-Pin PLCC Socket

FIGURE 20. Printed Circuit Board Layout for LM12434 and LM12{L}438

8.0 Analog Considerations (Continued)



TL/H/11879–51

(b) Surface Mount Technology for 28-Pin PLCC Package

FIGURE 20. Printed Circuit Board Layout for LM12434 and LM12{L}438 (Continued)

8.0 Analog Considerations (Continued)

Microcontroller (Standard Interface Mode)

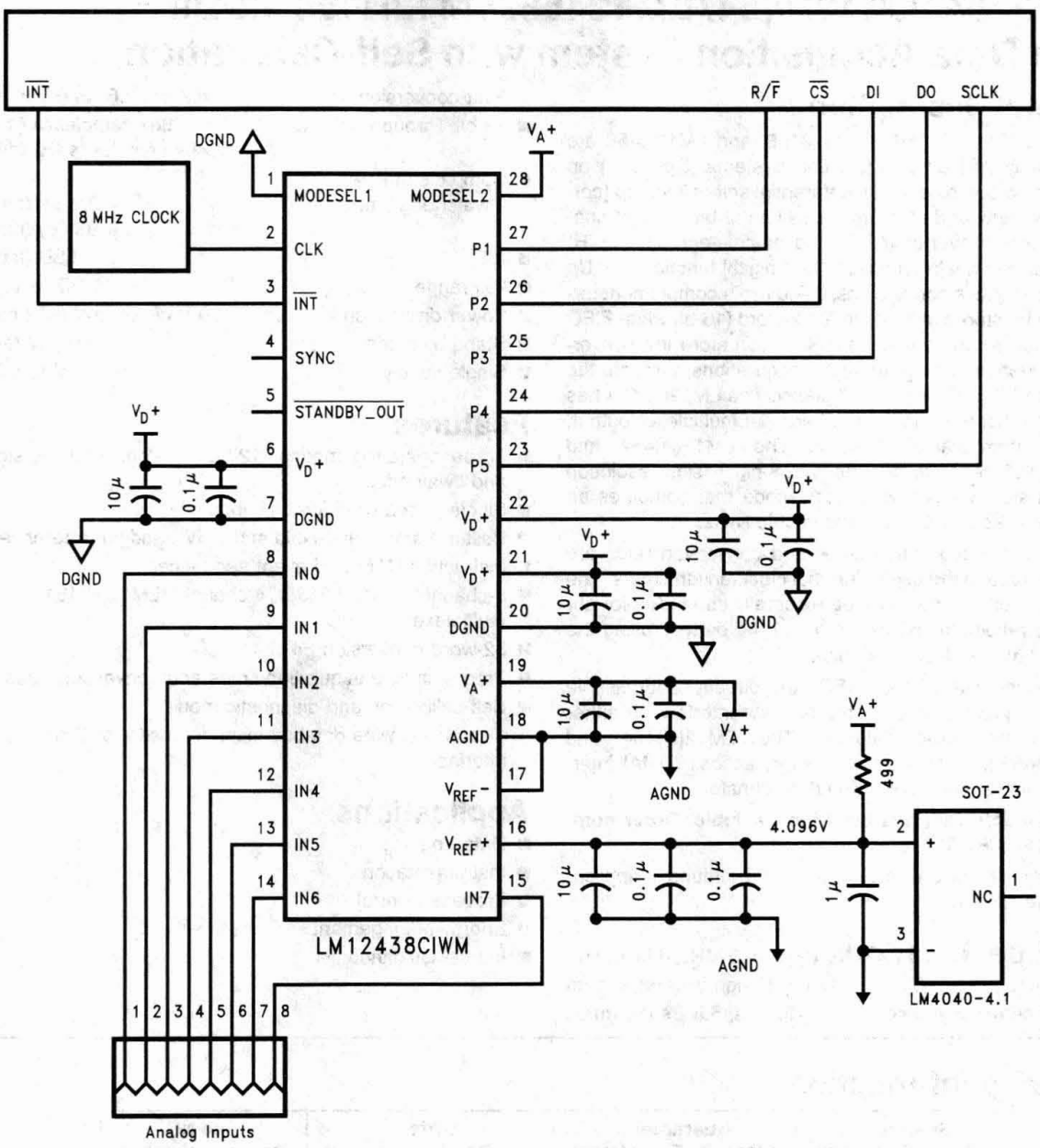


FIGURE 21. General Schematic of the DAS Operating in Standard Interface Mode

National Semiconductor

LM12454/LM12H454/LM12458/LM12H458 12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12454, LM12H454, LM12458, and LM12H458 are highly integrated Data Acquisition Systems. Operating on just 5V, they combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12(H)458's eight-input multiplexer. The LM12(H)454 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12(H)454 and LM12(H)458 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits.

Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers. The reference voltage input can be externally generated for absolute or ratiometric operation or can be derived using the internal 2.5V bandgap reference.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit databus. The LM12(H)454 and LM12(H)458 include a direct memory access (DMA) interface for high-speed conversion data transfer.

An evaluation/interface board is available. Order number LM12458EVAL.

Additional applications information can be found in applications note AN-906.

Key Specifications (f_{CLK} = 5 MHz; 8 MHz, H)

- Resolution — 12-bit + sign or 8-bit + sign
- 13-bit conversion time — 8.8 μs, 5.5 μs (H) (max)
- 9-bit conversion time — 4.2 μs, 2.6 μs (H) (max)
- 13-bit Through-put rate — 88k samples/s (min); 140k samples/s (H) (min)
- Comparison time ("watchdog" mode) — 2.2 μs (max); 1.4 μs (H) (max)
- ILE — ±1 LSB (max)
- V_{IN} range — GND to V_A^+
- Power dissipation — 30 mW, 34 mW (H) (max)
- Stand-by mode — 50 μW (typ)
- Single supply — 3V to 5.5V

Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog"
- Single-ended or differential inputs
- Built-in Sample-and-Hold and 2.5V bandgap reference
- Instruction RAM and event sequencer
- 8-channel (LM12(H)458), 4-channel (LM12(H)454) multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide databus microprocessor or DSP interface

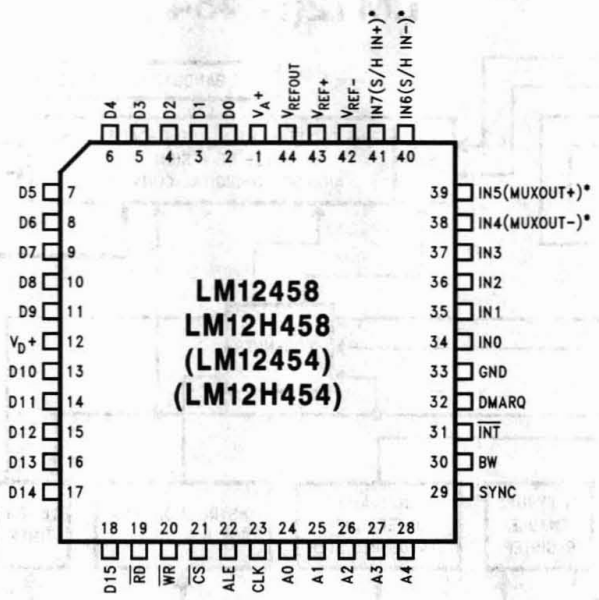
Applications

- Data Logging
- Instrumentation
- Process Control
- Energy Management
- Inertial Guidance

Ordering Information

Guaranteed Clock Freq (min)	Guaranteed Linearity Error (max)	Order Part Number	See NS Package Number
8 MHz	±1.0 LSB	LM12H454CIV	V44A
		LM12H458CIV	V44A
		LM12H458CIVF	VGZ44A
		LM12H458MEL/883 or 5962-9319502MYA	EL44A
		LM12H458MW/883 or 5962-9319502MXA	WA44A
5 MHz	±1.0 LSB	LM12454CIV	V44A
		LM12458CIV	V44A
		LM12458CIVF	VGZ44A
		LM12458MEL/883 or 5962-9319501MYA	EL44A
		LM12458MW/883 or 5962-9319501MXA	WA44A

Connection Diagrams



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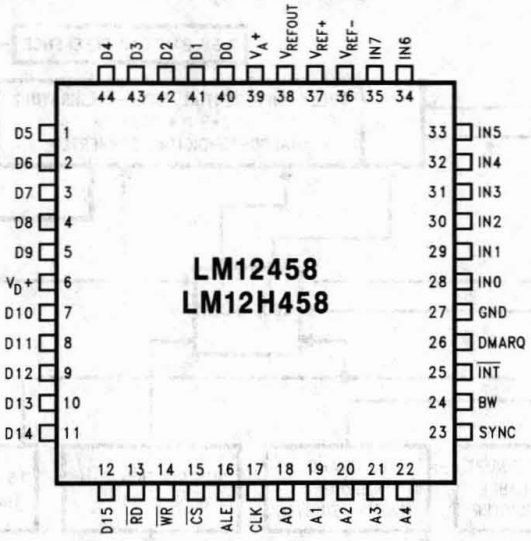
*Pin names in ( ) apply to the LM12454 and LM12H454.

Order Number LM12454CIV, LM12H454CIV, LM12458CIV or LM12H458CIV
See NS Package Number V44A

Order Number LM12458MEL/883 or 5962-9319501MYA,
LM12H458MEL/883 or 5962-9319502MYA,
LM12458MW/883 or 5962-9319501MXA,
LM12H458MW/883 or 5962-9319502MXA
See NS Package Number EL44A or WA44A

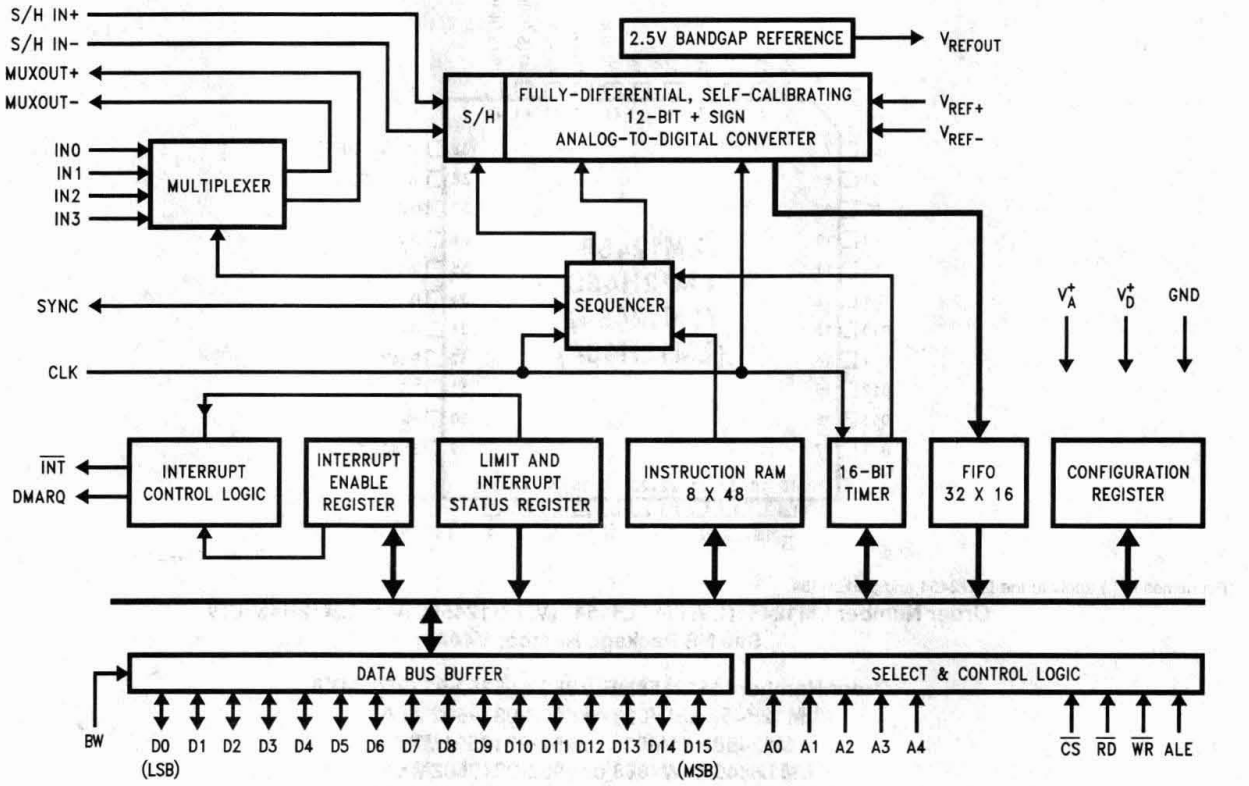


TL/H/11264–34

Order Number LM12458CIVF or LM12H458CIVF
See NS Package Number VGZ44A

Functional Diagrams

LM12(H)454



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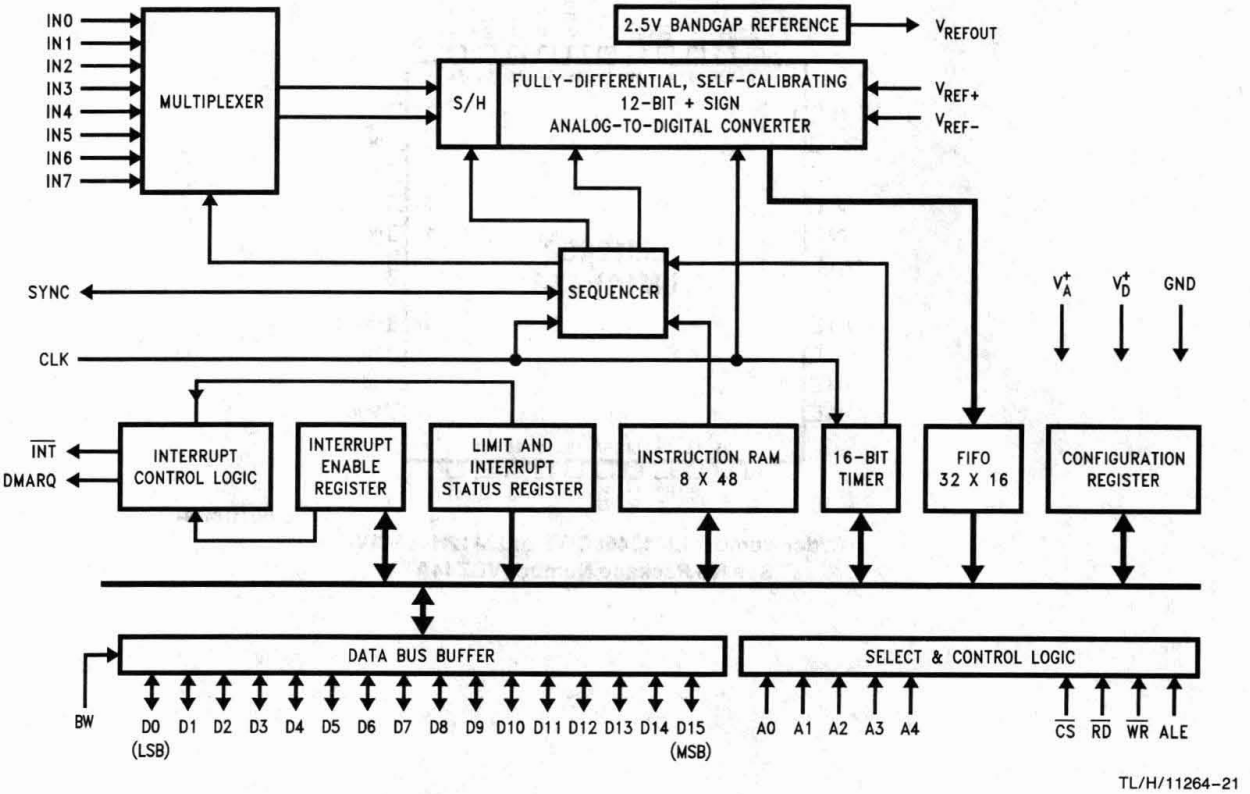
LM12(H)458



TL/H/11264–21

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_A^+ and V_D^+)	6.0V
Voltage at Input and Output Pins except IN0–IN3 (LM12(H)454) and IN0–IN7 (LM12(H)458)	−0.3V to V^+ + 0.3V
Voltage at Analog Inputs IN0–IN3 (LM12(H)454) and IN0–IN7 (LM12(H)458)	GND − 5V to V^+ + 5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation (T_A = 25°C) V Package (Note 4)	875 mW
Storage Temperature	−65°C to +150°C
Lead Temperature V Package, Infrared, 15 sec.	+300°C
EL and W Packages, Solder, 10 sec.	+250°C
ESD Susceptibility (Note 5)	1.5 kV
LM12(H)458MEL(MW)/883	2.0 kV

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	
LM12(H)454CIV/LM12(H)458CIV	$-40°C \le T_A \le 85°C$
LM12(H)458MEL(MW)/883	$-55°C \le T_A \le 125°C$
Supply Voltage	
V_A^+, V_D^+	3.0V to 5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤100 mV
V_{IN+} Input Range	$GND \le V_{IN+} \le V_A^+$
V_{IN-} Input Range	$GND \le V_{IN-} \le V_A^+$
V_{REF+} Input Voltage	$1V \le V_{REF+} \le V_A^+$
V_{REF-} Input Voltage	$0V \le V_{REF-} \le V_{REF+} - 1V$
$V_{REF+} - V_{REF-}$	$1V \le V_{REF} \le V_A^+$
V_{REF} Common Mode Range (Note 16)	$0.1\,V_A^+ \le V_{REFCM} \le 0.6\,V_A^+$

Converter Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, f_{CLK} = 8.0 MHz (LM12H454/8) or f_{CLK} = 5.0 MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \le 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J$ = 25°C. (Notes 6, 7, 8, 9 and 19)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
ILE	Positive and Negative Integral Linearity Error	After Auto-Cal (Notes 12, 17)	±1/2	**±1**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Note 12)	±1		LSB
	Resolution with No Missing Codes	After Auto-Cal (Note 12)		**13**	Bits (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±¾**	LSB (max)
	Zero Error	After Auto-Cal (Notes 13, 17) LM12H454 LM12H458	±1/2	**±1** **±1.5** **±1.5**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 17) LM12(H)458MEL/MW	±1/2	**±2** **±2.5**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 17) LM12(H)458MEL/MW	±1/2	**±2** **±2.5**	LSB (max)
	DC Common Mode Error	(Note 14)	±2	**±3.5**	LSB (max)
ILE	8-Bit + Sign and "Watchdog" Mode Positive and Negative Integral Linearity Error	(Note 12)		**±1/2**	LSB (max)
TUE	8-Bit + Sign and "Watchdog" Mode Total Unadjusted Error	After Auto-Zero	±1/2	**±3/4**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Resolution with No Missing Codes			**9**	Bits (max)
DNL	8-Bit + Sign and "Watchdog" Mode Differential Non-Linearity			**±3/4**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Zero Error	After Auto-Zero		**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Positive and Negative Full-Scale Error			**±1/2**	LSB (max)

Converter Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz (LM12H454/8) or $f_{CLK} = 5.0$ MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, 9 and 19) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
	8-Bit + Sign and "Watchdog" Mode DC Common Mode Error		±1/8		LSB
	Multiplexer Channel-to-Channel Matching		±0.05		LSB
V_{IN+}	Non-Inverting Input Range			**GND** **V_A^+**	V (min) V (max)
V_{IN-}	Inverting Input Range			**GND** **V_A^+**	V (min) V (max)
$V_{IN+} - V_{IN-}$	Differential Input Voltage Range			**$-V_A^+$** **V_A^+**	V (min) V (max)
$\frac{V_{IN+} - V_{IN-}}{2}$	Common Mode Input Voltage Range			**GND** **V_A^+**	V (min) V (max)
PSS	Power Supply Zero Error Sensitivity Full-Scale Error (Note 15) Linearity Error	$V_A^+ = V_D^+ = 5V \pm 10\%$ $V_{REF+} = 4.5V$, $V_{REF-} = GND$	±0.2 ±0.4 ±0.2	**±1.75** **±2**	LSB (max) LSB (max) LSB
C_{REF}	V_{REF+}/V_{REF-} Input Capacitance		85		pF
C_{IN}	Selected Multiplexer Channel Input Capacitance		75		pF

Converter AC Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz (LM12H454/8) or $f_{CLK} = 5.0$ MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, 9 and 19)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
	Clock Duty Cycle		50	 **40** **60**	% % (min) % (max)
t_C	Conversion Time	13-Bit Resolution, Sequencer State S5 *(Figure 11)*	44 (t_{CLK})	**44 (t_{CLK}) + 50 ns**	(max)
		9-Bit Resolution, Sequencer State S5 *(Figure 11)*	21 (t_{CLK})	**21 (t_{CLK}) + 50 ns**	(max)
t_A	Acquisition Time	Sequencer State S7 *(Figure 11)* Built-in minimum for 13-Bits	9 (t_{CLK})	**9 (t_{CLK}) + 50 ns**	(max)
		Built-in minimum for 9-Bits and "Watchdog" mode	2 (t_{CLK})	**2 (t_{CLK}) + 50 ns**	(max)
t_Z	Auto-Zero Time	Sequencer State S2 *(Figure 11)*	76 (t_{CLK})	**76 (t_{CLK}) + 50 ns**	(max)
t_{CAL}	Full Calibration Time	Sequencer State S2 *(Figure 11)*	4944 (t_{CLK})	**4944 (t_{CLK}) + 50 ns**	(max)
	Throughput Rate (Note 18)	 LM12H454, LM12H458	89 142	**88** **140**	kHz (min)
t_{WD}	"Watchdog" Mode Comparison Time	Sequencer States S6, S4, and S5 *(Figure 11)*	11 (t_{CLK})	**11 (t_{CLK}) + 50 ns**	(max)

Converter AC Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 5.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, 9 and 19) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
DSNR	Differential Signal-to-Noise Ratio	$V_{IN} = \pm 5V$			
		$f_{IN} = 1$ kHz	77.5		dB
		$f_{IN} = 20$ kHz	75.2		dB
		$f_{IN} = 40$ kHz	74.7		dB
SESNR	Single-Ended Signal-to-Noise Ratio	$V_{IN} = 5\ V_{p-p}$			
		$f_{IN} = 1$ kHz	69.8		dB
		$f_{IN} = 20$ kHz	69.2		dB
		$f_{IN} = 40$ kHz	66.6		dB
DSINAD	Differential Signal-to-Noise + Distortion Ratio	$V_{IN} = \pm 5V$			
		$f_{IN} = 1$ kHz	76.9		dB
		$f_{IN} = 20$ kHz	73.9		dB
		$f_{IN} = 40$ kHz	70.7		dB
SESINAD	Single-Ended Signal-to-Noise + Distortion Ratio	$V_{IN} = 5\ V_{p-p}$			
		$f_{IN} = 1$ kHz	69.4		dB
		$f_{IN} = 20$ kHz	68.3		dB
		$f_{IN} = 40$ kHz	65.7		dB
DTHD	Differential Total Harmonic Distortion	$V_{IN} = \pm 5V$			
		$f_{IN} = 1$ kHz	−85.8		dB
		$f_{IN} = 20$ kHz	−79.9		dB
		$f_{IN} = 40$ kHz	−72.9		dB
SETHD	Single-Ended Total Harmonic Distortion	$V_{IN} = 5\ V_{p-p}$			
		$f_{IN} = 1$ kHz	−80.3		dB
		$f_{IN} = 20$ kHz	−75.6		dB
		$f_{IN} = 40$ kHz	−72.8		dB
DENOB	Differential Effective Number of Bits	$V_{IN} = \pm 5V$			
		$f_{IN} = 1$ kHz	12.6		Bits
		$f_{IN} = 20$ kHz	12.2		Bits
		$f_{IN} = 40$ kHz	12.1		Bits
SEENOB	Single-Ended Effective Number of Bits	$V_{IN} = 5\ V_{p-p}$			
		$f_{IN} = 1$ kHz	11.3		Bits
		$f_{IN} = 20$ kHz	11.2		Bits
		$f_{IN} = 40$ kHz	10.8		Bits
DSFDR	Differential Spurious Free Dynamic Range	$V_{IN} = \pm 5V$			
		$f_{IN} = 1$ kHz	87.2		dB
		$f_{IN} = 20$ kHz	78.9		dB
		$f_{IN} = 40$ kHz	72.8		dB
	Multiplexer Channel-to-Channel Crosstalk	$V_{IN} = 5\ V_{PP}$, $f_{IN} = 40$ kHz, LM12(H)454 MUXOUT Only	−76		dB
		LM12(H)458 MUX plus Converter	−78		dB
t_{PU}	Power-Up Time		10		ms
t_{WU}	Wake-Up Time		10		ms

DC Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, $f_{CLK} = 8.0$ MHz (LM12H454/8) or $f_{CLK} = 5.0$ MHz (LM12454/8), and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 19)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
I_D^+	V_D^+ Supply Current	$\overline{CS}$ = "1"			
		LM12454/8	0.55	**1.0**	mA (max)
		LM12H454/8	0.55	**1.2**	
I_A^+	V_A^+ Supply Current	$\overline{CS}$ = "1"			
		LM12454/8	3.1	**5.0**	mA (max)
		LM12H454/8	3.1	**5.5**	
I_{ST}	Stand-By Supply Current ($I_D^+ + I_A^+$)	Power-Down Mode Selected			
		Clock Stopped	10		μA (max)
		8 MHz Clock	40		μA (max)
	Multiplexer ON-Channel Leakage Current	$V_A^+ = 5.5V$			
		ON-Channel = 5.5V		**0.3**	
		OFF-Channel = 0V	0.1		μA (max)
		LM12(H)458MEL/MW		**0.5**	
		ON-Channel = 0V		**0.3**	
		OFF-Channel = 5.5V	0.1		μA (max)
		LM12(H)458MEL/MW		**0.5**	
	Multiplexer OFF-Channel Leakage Current	$V_A^+ = 5.5V$			
		ON-Channel = 5.5V		**0.3**	
		OFF-Channel = 0V	0.1		μA (max)
		LM12(H)458MEL/MW		**0.5**	
		ON-Channel = 0V		**0.3**	
		OFF-Channel = 5.5V	0.1		μA (max)
		LM12(H)458MEL/MW		**0.5**	
R_{ON}	Multiplexer ON-Resistance	LM12(H)454			
		$V_{IN} = 5V$	800	**1500**	Ω(max)
		$V_{IN} = 2.5V$	850	**1500**	Ω(max)
		$V_{IN} = 0V$	760	**1500**	Ω(max)
	Multiplexer Channel-to-Channel R_{ON} matching	LM12(H)454			
		$V_{IN} = 5V$	±1.0%	**±3.0%**	(max)
		$V_{IN} = 2.5V$	±1.0%	**±3.0%**	(max)
		$V_{IN} = 0V$	±1.0%	**±3.0%**	(max)

Internal Reference Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 19)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
V_{REFOUT}	Internal Reference Output Voltage	LM12(H)458MEL/MW	2.5	**2.5 ±4%** **2.5 ±6%**	V (max)
$\Delta V_{REF}/\Delta T$	Internal Reference Temperature Coefficient		40		ppm/°C
$\Delta_{REF}/\Delta I_L$	Internal Reference Load Regulation	Sourcing ($0 < I_L \leq +4$ mA)		**0.2**	%/mA (max)
		Sinking ($-1 \leq I_{IL} < 0$ mA)		**1.2**	%/mA (max)
ΔV_{REF}	Line Regulation	$4.5V \leq V_A^+ \leq 5.5V$	3	**20**	mV (max)
I_{SC}	Internal Reference Short Circuit Current	$V_{REFOUT} = 0V$	13	**25**	mA (max)
$\Delta V_{REF}/\Delta t$	Long Term Stability		200		ppm/kHr
t_{SU}	Internal Reference Start-Up Time	$V_A^+ = V_D^+ = 0V \rightarrow 5V$ $C_L = 100\ \mu F$	10		ms

Digital Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, unless otherwise specified. **Boldface limits apply for $T_A = T_J =$ T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 19)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage	$V_A^+ = V_D^+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_A^+ = V_D^+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$ LM12(H)458MEL/MW	0.005	**1.0** **2.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$ LM12(H)458MEL/MW	−0.005	**−1.0** **−2.0**	μA (max)
C_{IN}	D0–D15 Input Capacitance		6		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_A^+ = V_D^+ = 4.5V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_A^+ = V_D^+ = 4.5V$ $I_{OUT} = 1.6\ mA$		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3.0** **3.0**	μA (max) μA (max)

Digital Timing Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $t_r = t_f =$ 3 ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J$ $= T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 19)

Symbol (See *Figures 8a, 8b,* and *8c*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
1, 3	$\overline{CS}$ or Address Valid to ALE Low Set-Up Time			**40**	ns (min)
2, 4	$\overline{CS}$ or Address Valid to ALE Low Hold Time			**20**	ns (min)
5	ALE Pulse Width			**45**	ns (min)
6	$\overline{RD}$ High to Next ALE High			**35**	ns (min)
7	ALE Low to $\overline{RD}$ Low			**20**	ns (min)
8	$\overline{RD}$ Pulse Width			**100**	ns (min)
9	$\overline{RD}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**100**	ns (min)
10	ALE Low to $\overline{WR}$ Low			**20**	ns (min)
11	$\overline{WR}$ Pulse Width			**60**	ns (min)
12	$\overline{WR}$ High to Next ALE High			**75**	ns (min)
13	$\overline{WR}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**140**	ns (min)
14	Data Valid to $\overline{WR}$ High Set-Up Time			**40**	ns (min)
15	Data Valid to $\overline{WR}$ High Hold Time			**30**	ns (min)
16	$\overline{RD}$ Low to Data Bus Out of TRI-STATE		40	**10** **70**	ns (min) ns (max)
17	$\overline{RD}$ High to TRI-STATE	$R_L = 1\ k\Omega$	30	**10** **110**	ns (min) ns (max)
18	$\overline{RD}$ Low to Data Valid (Access Time)		30	**10** **80**	ns (min) ns (max)

Digital Timing Characteristics

The following specifications apply to the LM12454, LM12H454, LM12458, and LM12H458 for $V_A^+ = V_D^+ = 5V$, $t_r = t_f = 3$ ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 19) (Continued)

Symbol (See *Figures 8a, 8b,* and *8c*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
20	Address Valid or $\overline{CS}$ Low to $\overline{RD}$ Low			**20**	ns (min)
21	Address Valid or $\overline{CS}$ Low to $\overline{WR}$ Low			**20**	ns (min)
19	Address Invalid from $\overline{RD}$ or $\overline{WR}$ High			**10**	ns (min)
22	$\overline{INT}$ High from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)
23	DMARQ Low from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

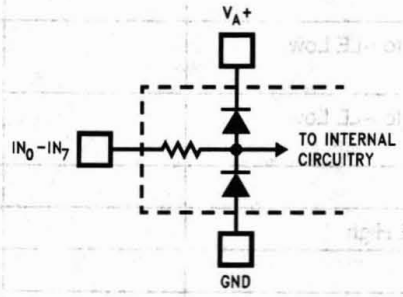
Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > (V_A^+$ or $V_D^+)$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$, and the typical thermal resistance (Θ_{JA}) of the LM12(H)454 and LM12(H)458 in the V package, when board mounted, is 47°C/W, in the W package, when board mounted, is 50°C/W ($\theta J_C = 5.8°C/W$), and in the EL package, when board mounted, is 70°C/W ($\theta J_C = 3.5°C/W$).

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to each analog input through a series resistor, as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage the LM12(H)454 or the LM12(H)458. However, errors in the A/D conversion can occur if these diodes are forward biased by more than 100 mV. As an example, if V_A^+ is 4.5 V_{DC}, full-scale input voltage must be ≤4.6 V_{DC} to ensure accurate conversions.



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Note 7: V_A^+ and V_D^+ must be connected together to the same power supply voltage and bypassed with separate capacitors at each V^+ pin to assure conversion/comparison accuracy.

Note 8: Accuracy is guaranteed when operating at $f_{CLK} = 5$ MHz for the LM12454/8 and $f_{CLK} = 8$ MHz for the LM12H454/8.

Note 9: With the test condition for V_{REF} ($V_{REF+} - V_{REF-}$) given as +5V, the 12-bit LSB is 1.22 mV and the 8-bit/"Watchdog" LSB is 19.53 mV.

Note 10: Typicals are at $T_A = 25°C$ and represent most likely parametric norm.

Note 11: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error the straight line passes through negative full-scale and zero. (See *Figures 5b* and *5c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between −1 to 0 and 0 to +1 (see *Figure 6*).

Note 14: The DC common-mode error is measured with both inputs shorted together and driven from 0V to 5V. The measured value is referred to the resulting output value when the inputs are driven with a 2.5V signal.

Note 15: Power Supply Sensitivity is measured after Auto-Zero and/or Auto-Calibration cycle has been completed with V_A^+ and V_D^+ at the specified extremes.

Note 16: V_{REFCM} (Reference Voltage Common Mode Range) is defined as $(V_{REF+} + V_{REF-})/2$.

Note 17: The LM12(H)454/8's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.10 LSB.

Note 18: The Throughput Rate is for a single instruction repeated continuously. Sequencer states 0 (1 clock cycle), 1 (1 clock cycle), 7 (9 clock cycles) and 5 (44 clock cycles) are used (see *Figure 11*). One additional clock cycle is used to read the conversion result stored in the FIFO, for a total of 56 clock cycles per conversion. The Throughput Rate is f_{CLK} (MHz)/N, where N is the number of clock cycles/conversion.

Note 19: A military RETS specification is available upon request. At the time of printing, the LM12(H)458CMEL/883 RETS specification complied with the **boldface** values in the Limits column.

Electrical Characteristics

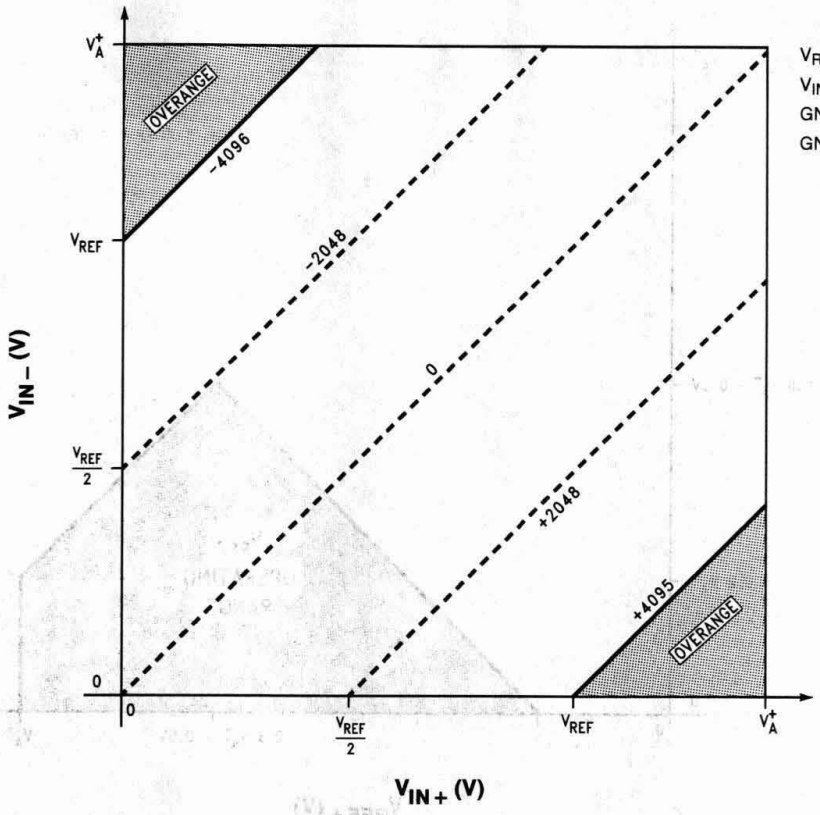

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FIGURE 1. The General Case of Output Digital Code vs the Operating Input Voltage Range

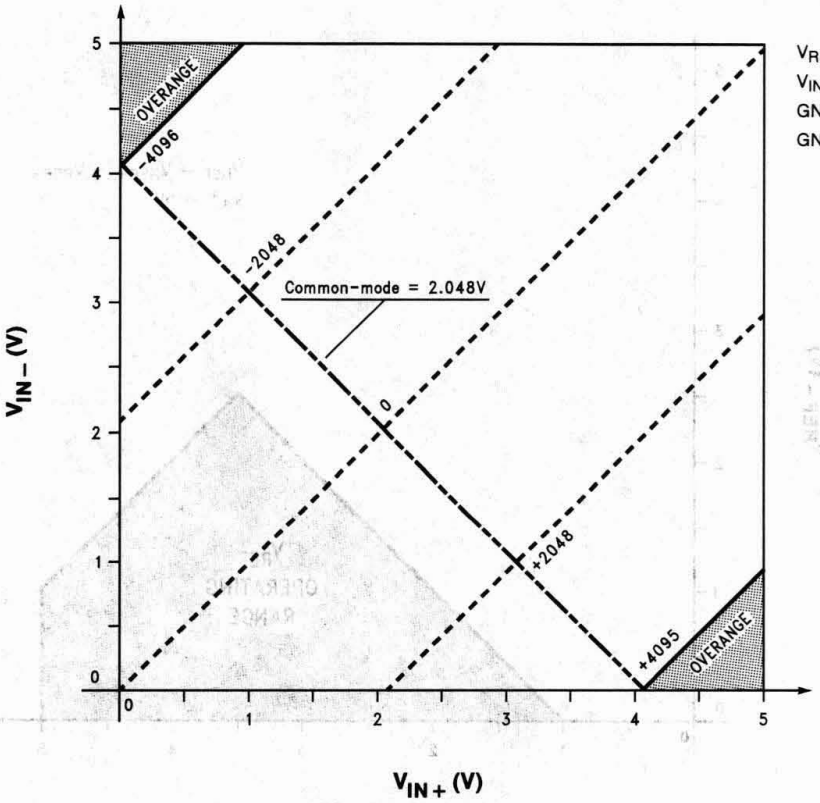

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FIGURE 2. Specific Case of Output Digital Code vs the Operating Input Voltage Range for $V_{REF} = 4.096V$

Electrical Characteristics (Continued)

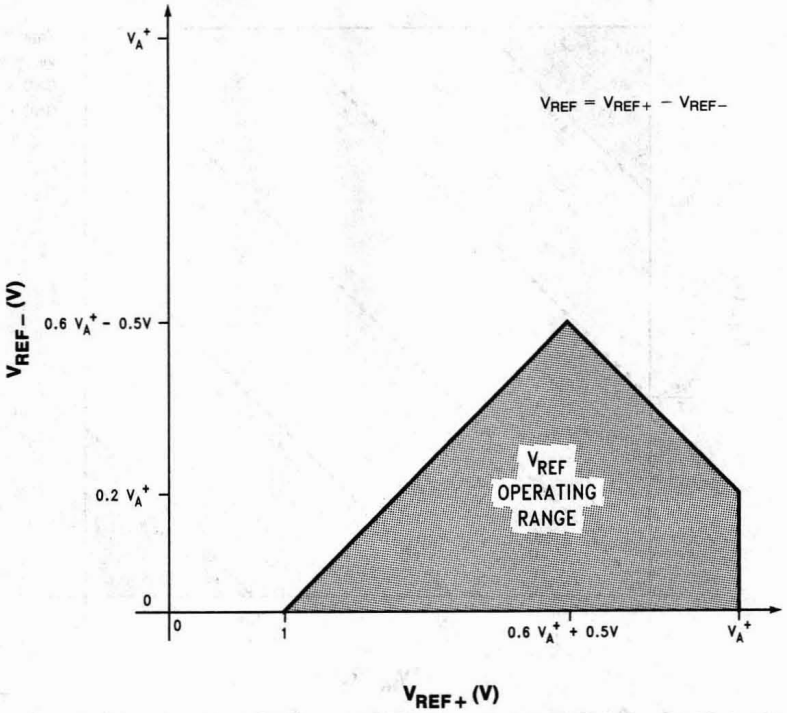

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FIGURE 3. The General Case of the V_{REF} Operating Range

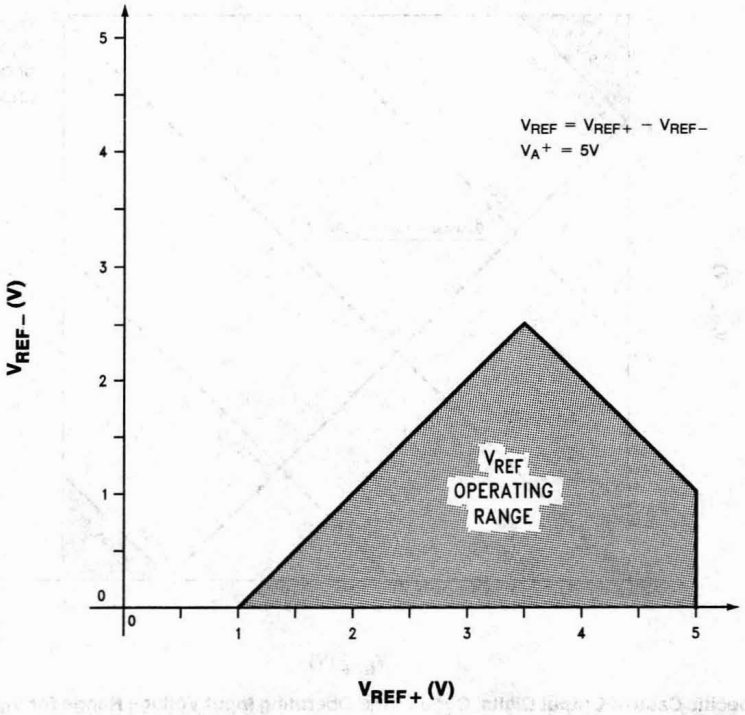

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FIGURE 4. The Specific Case of the V_{REF} Operating Range for $V_A^+ = 5V$

Electrical Characteristics (Continued)

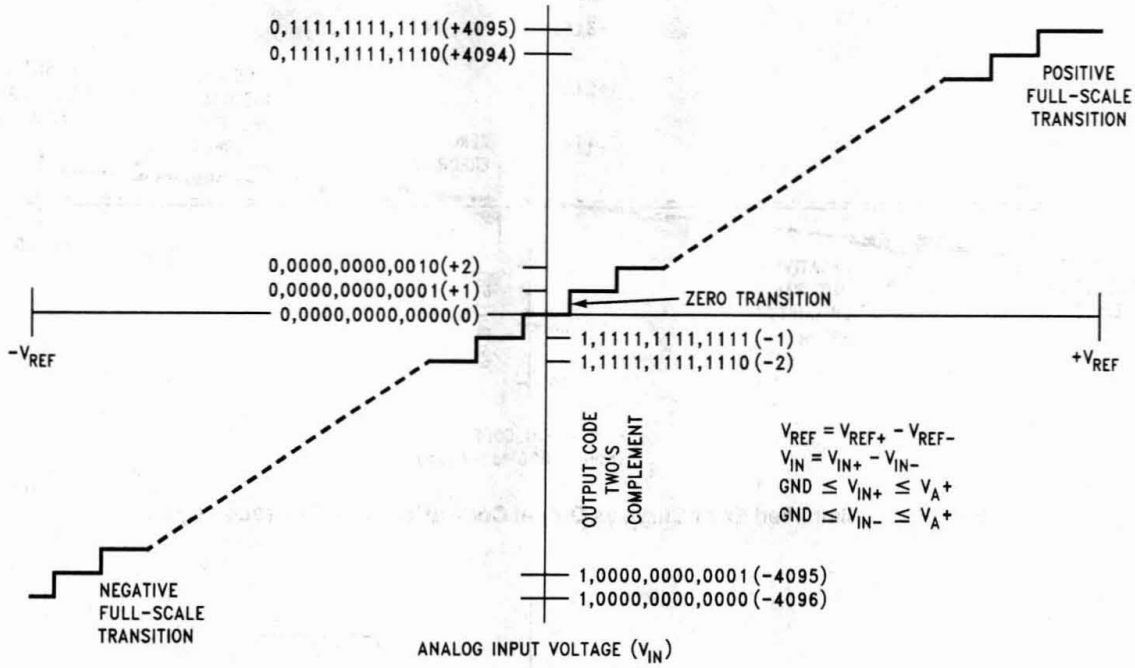

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FIGURE 5a. Transfer Characteristic

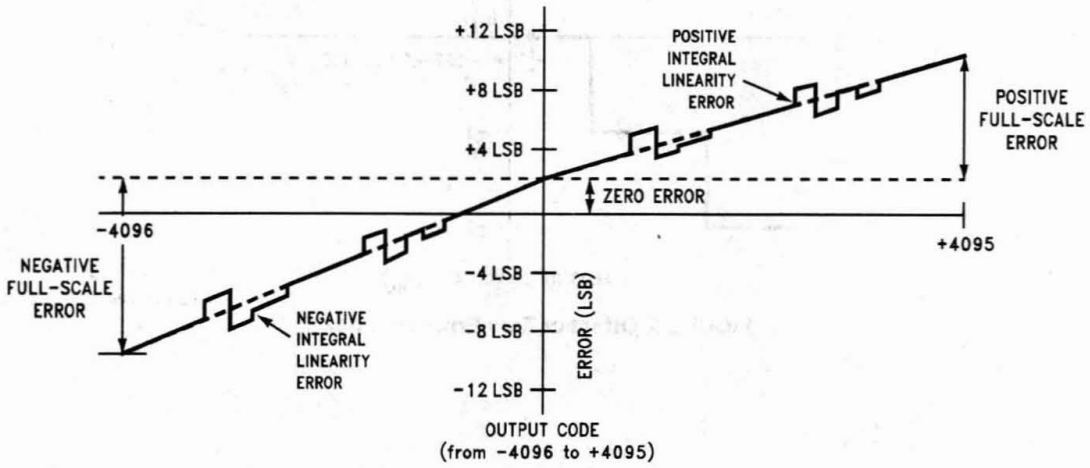

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FIGURE 5b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

Electrical Characteristics (Continued)

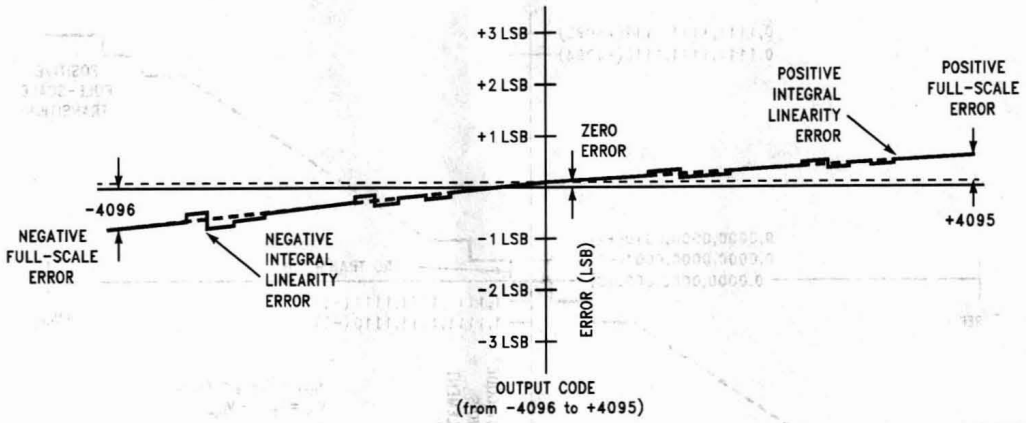


FIGURE 5c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

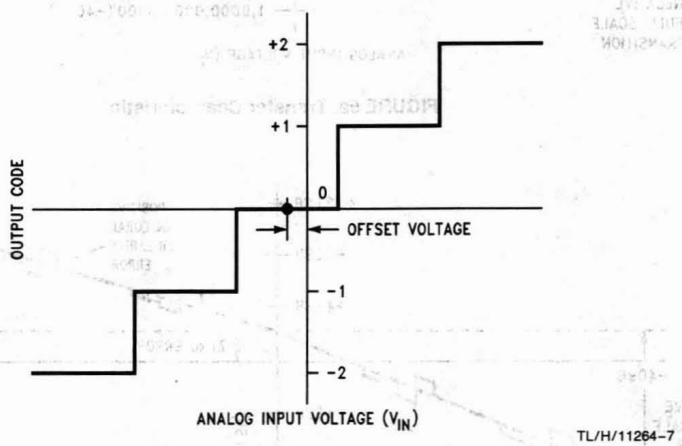
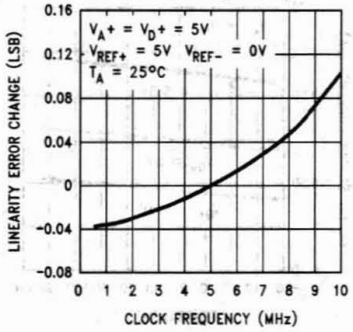


FIGURE 6. Offset or Zero Error Voltage

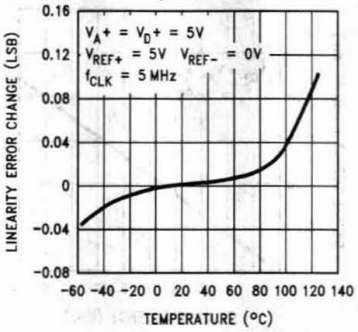
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9)

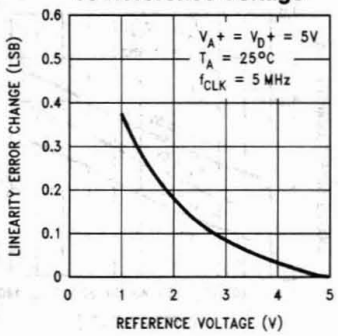
Linearity Error Change vs Clock Frequency



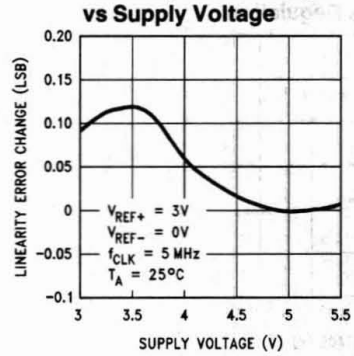
Linearity Error Change vs Temperature



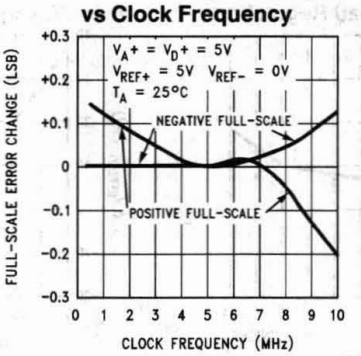
Linearity Error Change vs Reference Voltage



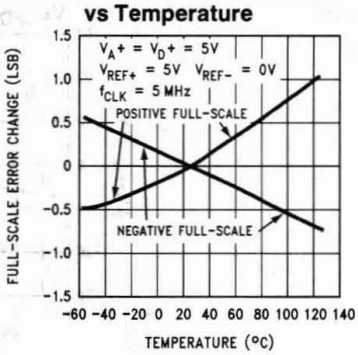
Linearity Error Change vs Supply Voltage



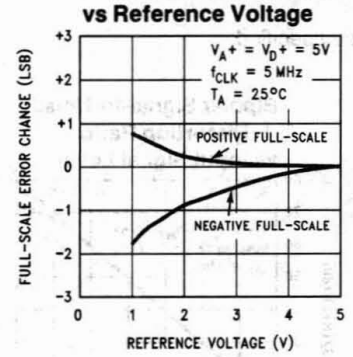
Full-Scale Error Change vs Clock Frequency



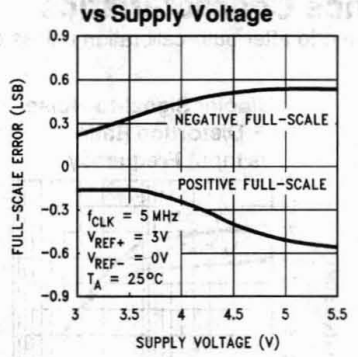
Full-Scale Error Change vs Temperature



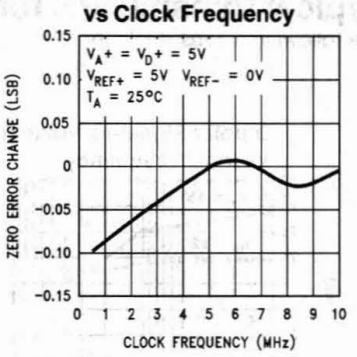
Full-Scale Error Change vs Reference Voltage



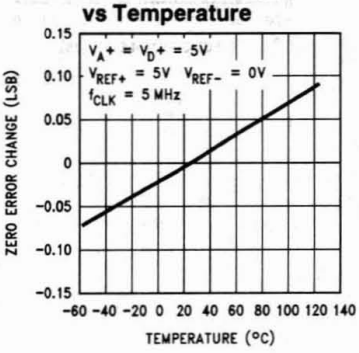
Full-Scale Error vs Supply Voltage



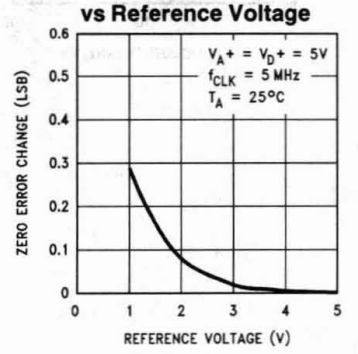
Zero Error Change vs Clock Frequency



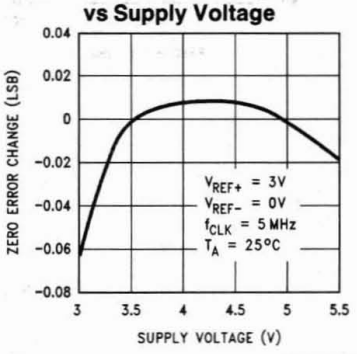
Zero Error Change vs Temperature



Zero Error Change vs Reference Voltage



Zero Error Change vs Supply Voltage



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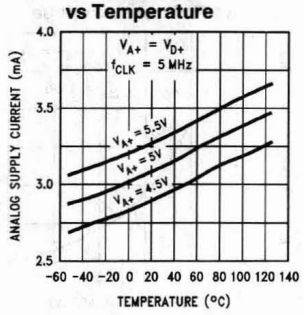
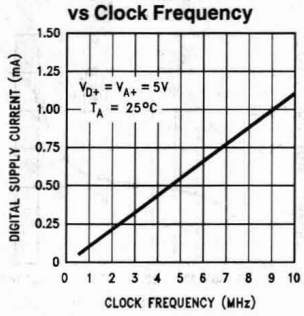
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9) (Continued)

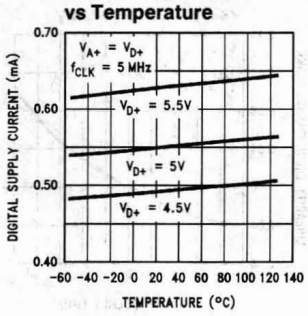
Analog Supply Current vs Temperature



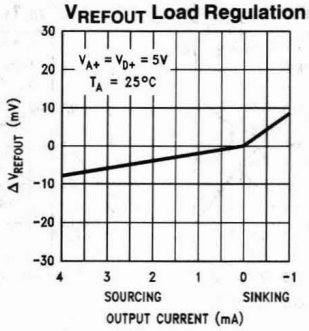
Digital Supply Current vs Clock Frequency



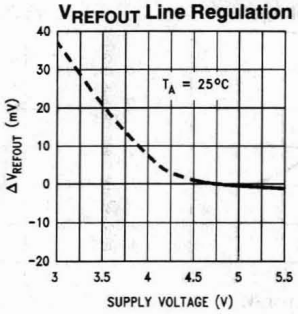
Digital Supply Current vs Temperature



V_{REFOUT} Load Regulation



V_{REFOUT} Line Regulation

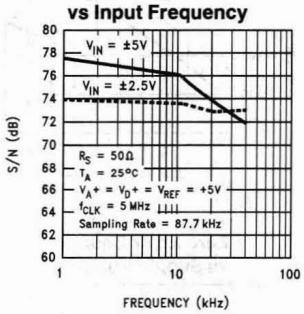


TL/H/11264–9

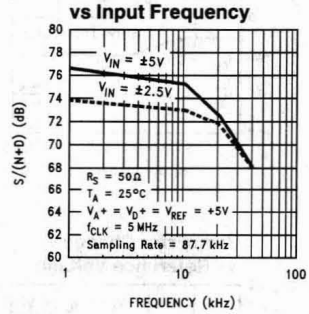
Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

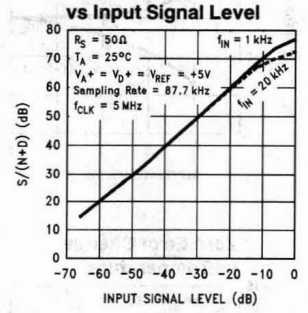
Bipolar Signal-to-Noise Ratio vs Input Frequency



Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



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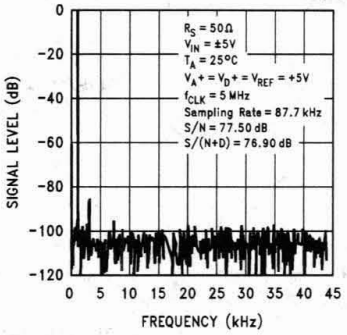
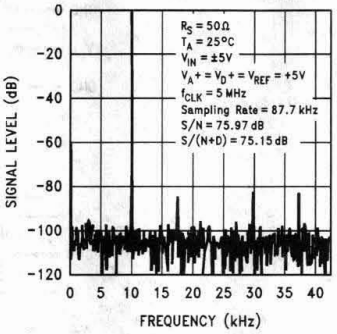
Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

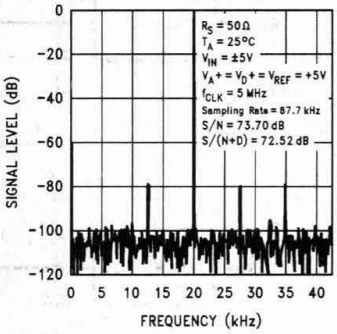
Bipolar Spectral Response with 1.028 kHz Sine Wave Input



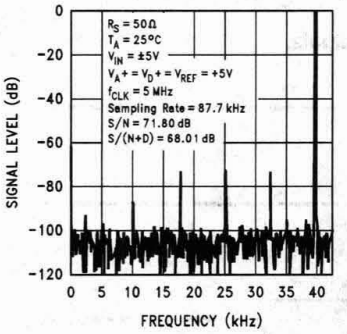
Bipolar Spectral Response with 10 kHz Sine Wave Input



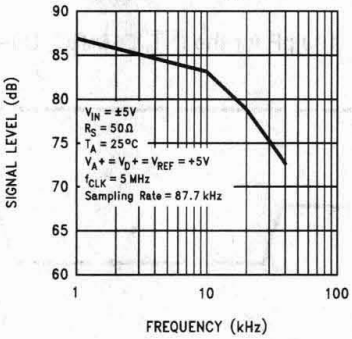
Bipolar Spectral Response with 20 kHz Sine Wave Input



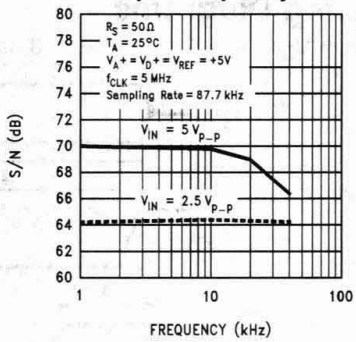
Bipolar Spectral Response with 40 kHz Sine Wave Input



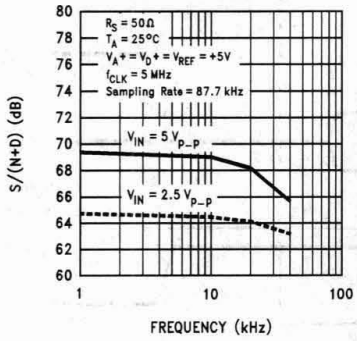
Bipolar Spurious Free Dynamic Range



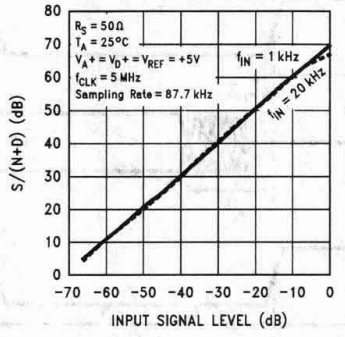
Unipolar Signal-to-Noise Ratio vs Input Frequency



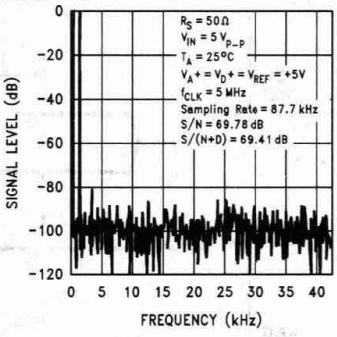
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



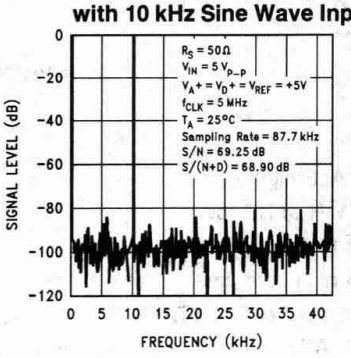
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



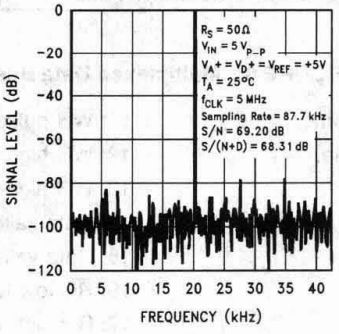
Unipolar Spectral Response with 1.028 kHz Sine Wave Input



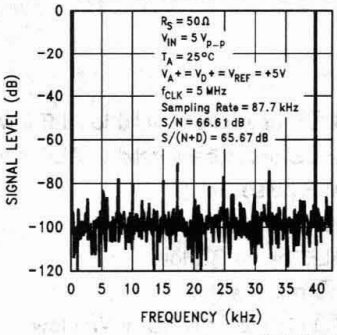
Unipolar Spectral Response with 10 kHz Sine Wave Input



Unipolar Spectral Response with 20 kHz Sine Wave Input



Unipolar Spectral Response with 40 kHz Sine Wave Input



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Test Circuits and Waveforms

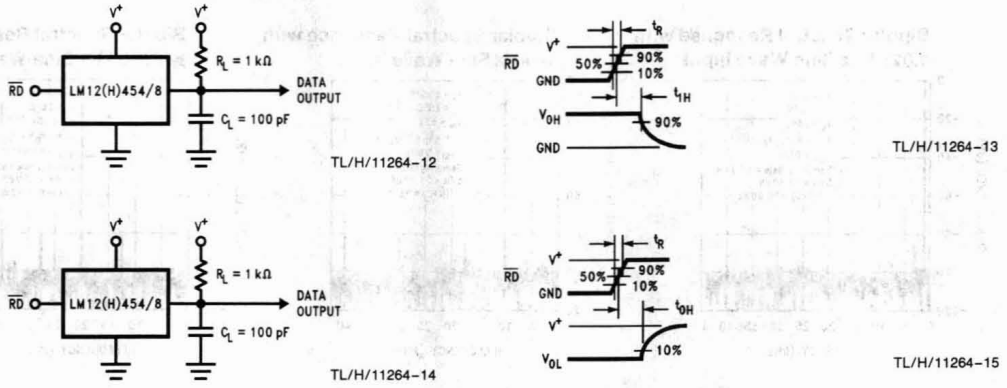

FIGURE 7. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

$V_A^+ = V_D^+ = +5V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

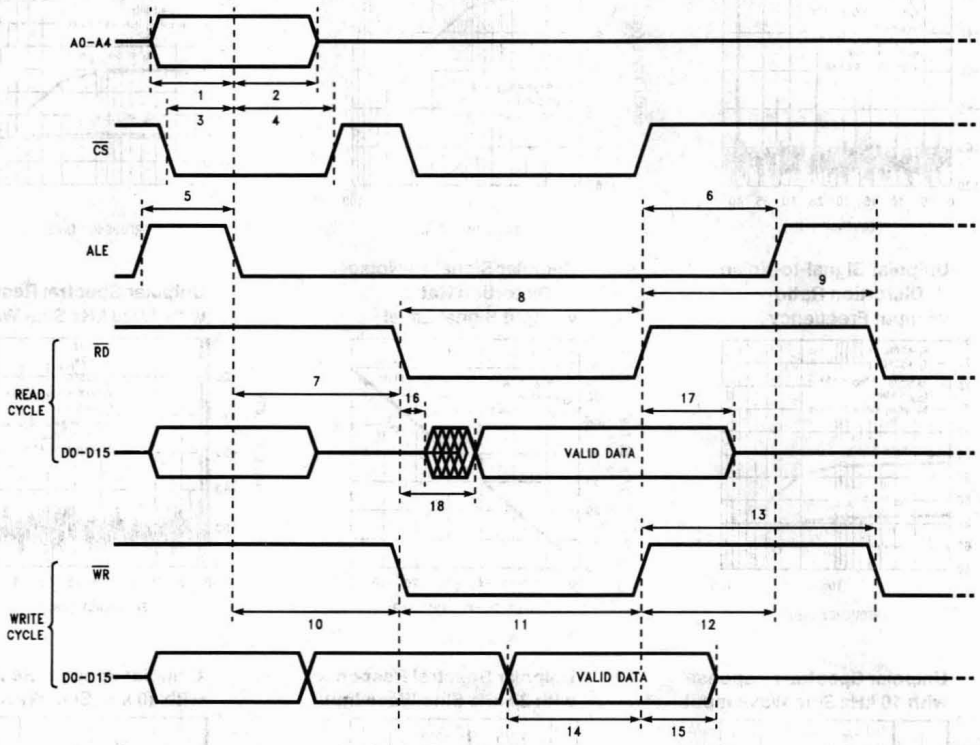

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FIGURE 8a. Multiplexed Data Bus

1, 3: $\overline{CS}$ or Address valid to ALE low set-up time.
2, 4: $\overline{CS}$ or Address valid to ALE low hold time.
5: ALE pulse width
6: $\overline{RD}$ high to next ALE high
7: ALE low to $\overline{RD}$ low
8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
10: ALE low to $\overline{WR}$ low
11: $\overline{WR}$ pulse width
12: $\overline{WR}$ high to next ALE high
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)

Timing Diagrams

$V_A^+ = V_D^+ = +5V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs. (Continued)

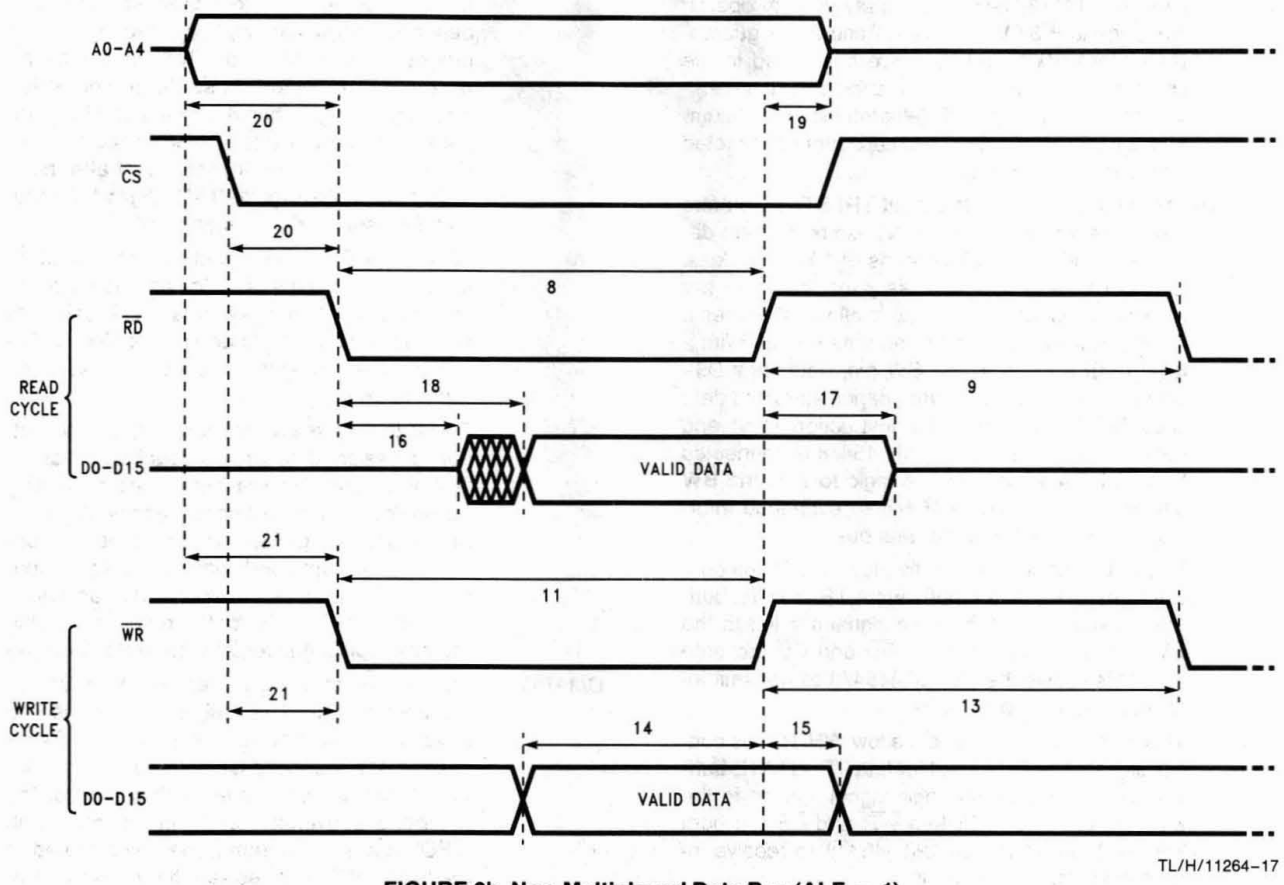

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FIGURE 8b. Non-Multiplexed Data Bus (ALE = 1)

8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
11: $\overline{WR}$ pulse width
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)
19: Address invalid from $\overline{RD}$ or $\overline{WR}$ high (hold time)
20: $\overline{CS}$ low or address valid to $\overline{RD}$ low
21: $\overline{CS}$ low or address valid to $\overline{WR}$ low

$V_A^+ = V_D^+ = +5V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

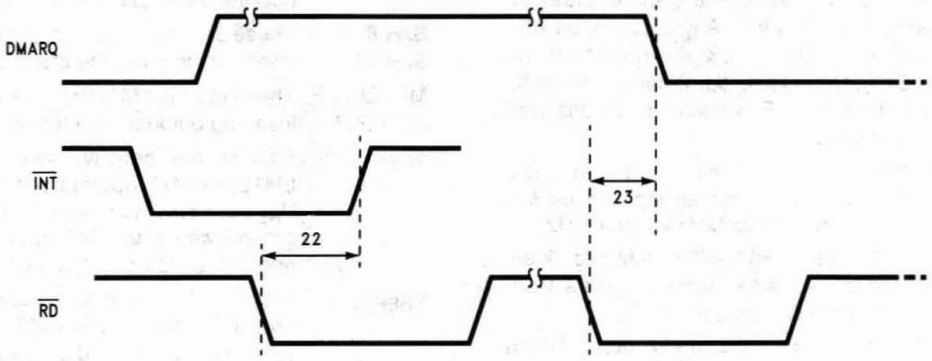

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FIGURE 8c. Interrupt and DMARQ

22: $\overline{INT}$ high from $\overline{RD}$ low
23: DMARQ low from $\overline{RD}$ low

Pin Description

V_A^+ V_D^+ These are the analog and digital supply voltage pins. The LM12(H)454/8's supply voltage operating range is +3.0V to +5.5V. Accuracy is guaranteed only if V_A^+ and V_D^+ are connected to the same power supply. Each pin should have a parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors connected between it and ground.

D0–D15 The internal data input/output TRI-STATE buffers are connected to these pins. These buffers are designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. These pins allows the user a means of instruction input and data output. With a logic **high** applied to the **BW** pin, data lines D8–D15 are placed in a high impedance state and data lines D0–D7 are used for instruction input and data output when the LM12(H)454/8 is connected to an 8-bit wide data bus. A logic **low** on the **BW** pin allows the LM12(H)454/8 to exchange information over a 16-bit wide data bus.

$\overline{RD}$ This is the input for the active low READ bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{RD}$ and $\overline{CS}$ are both low. This allows the LM12(H)454/8 to transmit information onto the databus.

$\overline{WR}$ This is the input for the active low WRITE bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{WR}$ and $\overline{CS}$ are both low. This allows the LM12(H)454/8 to receive information from the databus.

$\overline{CS}$ This is the input for the active low Chip Select control signal. A logic low should be applied to this pin only during a READ or WRITE access to the LM12(H)454/8. The internal clocking is halted and conversion stops while Chip Select is low. Conversion resumes when the Chip Select input signal returns high.

ALE This is the Address Latch Enable input. It is used in systems containing a multiplexed databus. When ALE is asserted **high**, the LM12(H)454/8 accepts information on the databus as a valid address. A high-to-low transition will latch the address data on A0–A4 while the $\overline{CS}$ is low. Any changes on A0–A4 and $\overline{CS}$ while ALE is low will not affect the LM12(H)454/8. See *Figure 8a*. When a non-multiplexed bus is used, ALE is continuously asserted **high**. See *Figure 8b*.

CLK This is the external clock input pin. The LM12(H)454/8 operates with an input clock frequency in the range of 0.05 MHz to 10.0 MHz.

A0–A4 These are the LM12(H)454/8's address lines. They are used to access all internal registers, Conversion FIFO, and Instruction **RAM**.

SYNC This is the synchronization input/output. When used as an output, it is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. SYNC is an **input** if the Configuration register's "I/O Select" bit is **low**. A rising edge on this pin causes the internal S/H to hold the input signal. The next rising clock edge either starts a conversion or makes a comparison to a programmable limit depending on which function is requested by a programming instruction. This pin will be an **output** if "I/O Select" is set **high**. The SYNC output goes high when a conversion or a comparison is started and low when completed. (See Section 2.2). An internal reset after power is first applied to the LM12(H)454/8 automatically sets this pin as an input.

BW This is the Bus Width input pin. This input allows the LM12(H)454/8 to interface directly with either an 8- or 16-bit databus. A logic high sets the width to 8 bits and places D8–D15 in a high impedance state. A logic low sets the width to 16 bits.

$\overline{INT}$ This is the active low interrupt output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. An interrupt signal is generated any time a non-masked interrupt condition takes place. There are eight different conditions that can cause an interrupt. Any interrupt is reset by reading the Interrupt Status register. (See Section 2.3.)

DMARQ This is the active high Direct Memory Access Request output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. It goes high whenever the number of conversion results in the conversion FIFO equals a programmable value stored in the Interrupt Enable register. It returns to a logic low when the FIFO is empty.

GND This is the LM12(H)454/8 ground connection. It should be connected to a low resistance and inductance analog ground return that connects directly to the system power supply ground.

IN0–IN7 (IN0–IN3 LM12H454 LM12454) These are the eight (LM12(H)458) or four (LM12(H)454) analog inputs. A given channel is selected through the instruction RAM. Any of the channels can be configured as an independent single-ended input. Any pair of channels, whether adjacent or non-adjacent, can operate as a fully differential pair.

S/H IN+ S/H IN− These are the LM12(H)454's non-inverting and inverting inputs to the internal S/H.

MUXOUT+ MUXOUT− These are the LM12(H)454's non-inverting and inverting outputs from the internal multiplexer.

$V_{REF}-$ This is the negative reference input. The LM12(H)454/8 operate with $0V \leq V_{REF}- \leq V_{REF}+$. This pin should be bypassed to ground with a parallel combination of 10 μF and 0.1 μF (ceramic) capacitors.

$V_{REF}+$ This is the positive reference input. The LM12(H)454/8 operate with $0V \leq V_{REF}+ \leq V_A^+$. This pin should be bypassed to ground with a parallel combination of 10 μF and 0.1 μF (ceramic) capacitors.

V_{REFOUT} This is the internal 2.5V bandgap's output pin. This pin should be bypassed to ground with a 100 μF capacitor.

Application Information

1.0 Functional Description

The LM12(H)454 and LM12(H)458 are multi-functional Data Acquisition Systems that include a fully differential 12-bit-plus-sign self-calibrating analog-to-digital converter (ADC) with a two's-complement output format, an 8-channel (LM12(H)458) or a 4-channel (LM12(H)454) analog multiplexer, an internal 2.5V reference, a first-in-first-out (FIFO) register that can store 32 conversion results, and an Instruction RAM that can store as many as eight instructions to be sequentially executed. The LM12(H)454 also has a differential multiplexer output and a differential S/H input. All of this circuitry operates on only a single +5V power supply.

The LM12(H)454/8 have three modes of operation:

12-bit + sign with correction
8-bit + sign without correction
8-bit + sign comparison mode ("watchdog" mode)

The fully differential 12-bit-plus-sign ADC uses a charge re-distribution topology that includes calibration capabilities. Charge re-distribution ADCs use a capacitor ladder in place of a resistor ladder to form an internal DAC. The DAC is used by a successive approximation register to generate intermediate voltages between the voltages applied to V_{REF-} and V_{REF+}. These intermediate voltages are compared against the sampled analog input voltage as each bit is generated. The number of intermediate voltages and comparisons equals the ADC's resolution. The correction of each bit's accuracy is accomplished by calibrating the capacitor ladder used in the ADC.

Two different calibration modes are available; one compensates for offset voltage, or zero error, while the other corrects both offset error and the ADC's linearity error.

When correcting offset only, the offset error is measured once and a correction coefficient is created. During the full calibration, the offset error is measured eight times, averaged, and a correction coefficient is created. After completion of either calibration mode, the offset correction coefficient is stored in an internal offset correction register.

The LM12(H)454/8's overall linearity correction is achieved by correcting the internal DAC's capacitor mismatch. Each capacitor is compared eight times against all remaining smaller value capacitors and any errors are averaged. A correction coefficient is then created and stored in one of the thirteen internal linearity correction registers. An internal state machine, using patterns stored in an internal 16 x 8-bit ROM, executes each calibration algorithm.

Once calibrated, an internal arithmetic logic unit (ALU) uses the offset correction coefficient and the 13 linearity correction coefficients to reduce the conversion's offset error and linearity error, in the background, during the 12-bit + sign conversion. The 8-bit + sign conversion and comparison modes use only the offset coefficient. The 8-bit + sign mode performs a conversion in less than half the time used by the 12-bit + sign conversion mode.

The LM12(H)454/8's "watchdog" mode is used to monitor a single-ended or differential signal's amplitude. Each sampled signal has two limits. An interrupt can be generated if the input signal is above or below either of the two limits. This allows interrupts to be generated when analog voltage inputs are "inside the window" or, alternatively, "outside the window". After a "watchdog" mode interrupt, the processor can then request a conversion on the input signal and read the signal's magnitude.

The analog input multiplexer can be configured for any combination of single-ended or fully differential operation. Each input is referenced to ground when a multiplexer channel operates in the single-ended mode. Fully differential analog input channels are formed by pairing any two channels together.

The LM12(H)454's multiplexer outputs and S/H inputs (MUXOUT+, MUXOUT− and S/H IN+, S/H IN−) provide the option for additional analog signal processing. Fixed-gain amplifiers, programmable-gain amplifiers, filters, and other processing circuits can operate on the signal applied to the selected multiplexer channel(s). If external processing is not used, connect MUXOUT+ to S/H IN+ and MUXOUT− to S/H IN−.

The LM12(H)454/8's internal S/H is designed to operate at its minimum acquisition time (1.13 μs, 12 bits) when the source impedance, R_S, is $\leq 60\Omega$ ($f_{CLK} \leq 8$ MHz). When $60\Omega < R_S \leq 4.17\ k\Omega$, the internal S/H's acquisition time can be increased to a maximum of 4.88 μs (12 bits, f_{CLK} = 8 MHz). See Section 2.1 (Instruction RAM "00") Bits 12–15 for more information.

An internal 2.5V bandgap reference output is available at pin 44. This voltage can be used as the ADC reference for ratiometric conversion or as a virtual ground for front-end analog conditioning circuits. The V_{REFOUT} pin should be bypassed to ground with a 100 μF capacitor.

Microprocessor overhead is reduced through the use of the internal conversion FIFO. Thirty-two consecutive conversions can be completed and stored in the FIFO without any microprocessor intervention. The microprocessor can, at any time, interrogate the FIFO and retrieve its contents. It can also wait for the LM12(H)454/8 to issue an interrupt when the FIFO is full or after any number ($\leq$32) of conversions have been stored.

Conversion sequencing, internal timer interval, multiplexer configuration, and many other operations are programmed and set in the Instruction RAM.

A diagnostic mode is available that allows verification of the LM12(H)458's operation. The diagnostic mode is disabled in the LM12(H)454. This mode internally connects the voltages present at the V_{REFOUT}, V_{REF+}, V_{REF-}, and GND pins to the internal V_{IN+} and V_{IN-} S/H inputs. This mode is activated by setting the Diagnostic bit (Bit 11) in the Configuration register to a "1". More information concerning this mode of operation can be found in Section 2.2.

2.0 Internal User-Programmable Registers

2.1 INSTRUCTION RAM

The instruction RAM holds up to eight sequentially executable instructions. Each 48-bit long instruction is divided into three 16-bit sections. READ and WRITE operations can be issued to each 16-bit section using the instruction's address and the 2-bit "RAM pointer" in the Configuration register. The eight instructions are located at addresses 0000 through 0111 (A4–A1, BW = 0) when using a 16-bit wide data bus or at addresses 00000 through 01111 (A4–A0, BW = 1) when using an 8-bit wide data bus. They can be accessed and programmed in random order.

Any Instruction RAM READ or WRITE can affect the sequencer's operation:

The Sequencer should be stopped by setting the RESET bit to a "1" or by resetting the START bit in the Configuration Register and waiting for the current instruction to finish execution before any Instruction RAM READ or WRITE is initiated.

A soft RESET should be issued by writing a "1" to the Configuration Register's RESET bit after any READ or WRITE to the Instruction RAM.

The three sections in the Instruction RAM are selected by the Configuration Register's 2-bit "RAM Pointer", bits D8 and D9. The first 16-bit Instruction RAM section is selected with the RAM Pointer equal to "00". This section provides multiplexer channel selection, as well as resolution, acquisition time, etc. The second 16-bit section holds "watchdog" limit #1, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit. The third 16-bit section holds "watchdog" limit #2, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit.

Instruction RAM "00"

Bit 0 is the LOOP bit. It indicates the last instruction to be executed in any instruction sequence when it is set to a "1". The next instruction to be executed will be instruction 0.

Bit 1 is the PAUSE bit. This controls the Sequencer's operation. When the PAUSE bit is set ("1"), the Sequencer will stop after reading the current instruction and before executing it, and the start bit in the Configuration register is automatically reset to a "0". Setting the PAUSE also causes an interrupt to be issued. The Sequencer is restarted by placing a "1" in the Configuration register's Bit 0 (Start bit).

After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer retrieves Instruction 000, decodes it, and waits for a "1" to be placed in the Configuration's START bit. The START bit value of "0" "overrides" the action of Instruction 000's PAUSE bit when the Sequencer is started. Once started, the Sequencer executes Instruction 000 and retrieves, decodes, and executes each of the remaining instructions. No PAUSE Interrupt (INT 5) is generated the first time the Sequencer executes Instruction 000 having a PAUSE bit set to "1". When the Sequencer encounters a LOOP bit or completes all eight instructions, Instruction 000 is retrieved and decoded. A set PAUSE bit in Instruction 000 now halts the Sequencer before the instruction is executed.

Bits 2–4 select which of the eight input channels ("000" to "111" for IN0–IN7) will be configured as non-inverting inputs to the LM12(H)458's ADC. (See Page 25, Table I.) They select which of the four input channels ("000" to "011" for IN0–IN4) will be configured as non-inverting inputs to the LM12(H)454's ADC. (See Page 25, Table II.)

Bits 5–7 select which of the seven input channels ("001" to "111" for IN1 to IN7) will be configured as inverting inputs to the LM12(H)458's ADC. (See Page 25, Table I.) They select which of the three input channels ("001" to "011" for IN1–IN4) will be configured as inverting inputs to the LM12(H)454's ADC. (See Page 25, Table II.) Fully differential operation is created by selecting two multiplexer channels, one operating in the non-inverting mode and the other operating in the inverting mode. A code of "000" selects ground as the inverting input for single ended operation.

Bit 8 is the SYNC bit. Setting Bit 8 to "1" causes the Sequencer to suspend operation at the end of the internal S/H's acquisition cycle and to wait until a rising edge appears at the SYNC pin. When a rising edge appears, the S/H acquires the input signal magnitude and the ADC performs a conversion on the clock's next rising edge. When the SYNC pin is used as an input, the Configuration register's "I/O Select" bit (Bit 7) must be set to a "0". With SYNC configured as an input, it is possible to synchronize the start of a conversion to an external event. This is useful in applications such as digital signal processing (DSP) where the exact timing of conversions is important.

When the LM12(H)454/8 are used in the "watchdog" mode with external synchronization, two rising edges on the SYNC input are required to initiate two comparisons. The first rising edge initiates the comparison of the selected analog input signal with Limit #1 (found in Instruction RAM "01") and the second rising edge initiates the comparison of the same analog input signal with Limit #2 (found in Instruction RAM "10").

Bit 9 is the TIMER bit. When Bit 9 is set to "1", the Sequencer will halt until the internal 16-bit Timer counts down to zero. During this time interval, no "watchdog" comparisons or analog-to-digital conversions will be performed.

Bit 10 selects the ADC conversion resolution. Setting Bit 10 to "1" selects 8-bit + sign and when reset to "0" selects 12-bit + sign.

Bit 11 is the "watchdog" comparison mode enable bit. When operating in the "watchdog" comparison mode, the selected analog input signal is compared with the programmable values stored in Limit #1 and Limit #2 (see Instruction RAM "01" and Instruction RAM "10"). Setting Bit 11 to "1" causes two comparisons of the selected analog input signal with the two stored limits. When Bit 11 is reset to "0", an 8-bit + sign or 12-bit + sign (depending on the state of Bit 10 of Instruction RAM "00") conversion of the input signal can take place.

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	Purpose	Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 00)	R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync	V_{IN-} (MUXOUT−)*			V_{IN+} (MUXOUT+)*			Pause	Loop
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 01)	R/W	Don't Care						>/<	Sign	Limit #1							
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 10)	R/W	Don't Care						>/<	Sign	Limit #2							
1	0	0	0	Configuration Register	R/W	Don't Care				DIAG†	Test = 0	RAM Pointer		I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full CAL	Auto-Zero	Reset	Start
1	0	0	1	Interrupt Enable Register	R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1			INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
1	0	1	0	Interrupt Status Register	R	Actual Number of Conversion Results in Conversion FIFO					Address of Sequencer Instruction being Executed			INST7	INST6	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	1	Timer Register	R/W	Timer Preset High Byte								Timer Preset Low Byte							
1	1	0	0	Conversion FIFO	R	Address or Sign			Sign	Conversion Data: MSBs				Conversion Data: LSBs							
1	1	0	1	Limit Status Register	R	Limit #2: Status								Limit #1: Status							

*LM12(H)454 (Refer to Table II).
†LM12(H)458 only. Must be set to "0" for the LM12(H)454.

FIGURE 9. LM12(H)454/8 Memory Map for 16-Bit Wide Databus (BW = "0", Test Bit = "0" and A0 = Don't Care)

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	A0	Purpose	Type	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 00)	R/W	V_{IN-} (MUXOUT−)*			V_{IN+} (MUXOUT+)*			Pause	Loop
0	0 to 1	0 to 1	0 to 1	1		R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 01)	R/W	Comparison Limit #1							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						> / <	Sign
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 10)	R/W	Comparison Limit #2							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						> / <	Sign
1	0	0	0	0	Configuration Register	R/W	I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full Cal	Auto-Zero	Reset	Start
1	0	0	0	1		R/W	Don't Care				DIAG†	Test = 0	RAM Pointer	
1	0	0	1	0	Interrupt Enable Register	R/W	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
1	0	0	1	1		R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1		
1	0	1	0	0	Interrupt Status Register	R	INST7	INST6	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	0	1		R	Actual Number of Conversions Results in Conversion FIFO					Address of Sequencer Instruction being Executed		
1	0	1	1	0	Timer Register	R/W	Timer Preset: Low Byte							
1	0	1	1	1		R/W	Timer Preset: High Byte							
1	1	0	0	0	Conversion FIFO	R	Conversion Data: LSBs							
1	1	0	0	1		R	Address or Sign			Sign	Conversion Data: MSBs			
1	1	0	1	0	Limit Status Register	R	Limit #1 Status							
1	1	0	1	1		R	Limit #2 Status							

*LM12(H)454 (Refer to Table II).

†LM12(H)458 only. Must be set to "0" for the LM12(H)454.

FIGURE 10. LM12(H)454/8 Memory Map for 8-Bit Wide Databus (BW = "1" and Test Bit = "0")

2.0 Internal User-Programmable Registers (Continued)

Bits 12–15 are used to store the user-programmable acquisition time. The Sequencer keeps the internal S/H in the acquisition mode for a fixed number of clock cycles (nine clock cycles, for 12-bit + sign conversions and two clock cycles for 8-bit + sign conversions or "watchdog" comparisons) plus a variable number of clock cycles equal to twice the value stored in Bits 12–15. Thus, the S/H's acquisition time is (9 + 2D) clock cycles for 12-bit + sign conversions and (2 + 2D) clock cycles for 8-bit + sign conversions or "watchdog" comparisons, where D is the value stored in Bits 12–15. The minimum acquisition time compensates for the typical internal multiplexer series resistance of 2 kΩ, and any additional delay created by Bits 12–15 compensates for source resistances greater than 60Ω (100Ω). (For this acquisition time discussion, numbers in ( ) are shown for the LM12(H)454/8 operating at 5 MHz.) The necessary acquisition time is determined by the source impedance at the multiplexer input. If the source resistance (R_S) < 60Ω (100Ω) and the clock frequency is 8 MHz, the value stored in bits 12–15 (D) can be 0000. If R_S > 60Ω (100Ω), the following equations determine the value that should be stored in bits 12–15.

$$D = 0.45 \times R_S \times f_{CLK}$$

for 12-bits + sign

$$D = 0.36 \times R_S \times f_{CLK}$$

for 8-bits + sign and "watchdog"

R_S is in kΩ and f_{CLK} is in MHz. Round the result to the next higher integer value. If D is greater than 15, it is advisable to lower the source impedance by using an analog buffer between the signal source and the LM12(H)458's multiplexer inputs. The value of D can also be used to compensate for the settling or response time of external processing circuits connected between the LM12(H)454's MUXOUT and S/H IN pins.

Instruction RAM "01"

The second Instruction RAM section is selected by placing a "01" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #1**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12(H)454/8 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first, followed by a comparison of the same sampled analog input signal with the value found in limit #2 (Instruction RAM "10").

Bit 8 holds limit #1's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #1 to generate an interrupt, while a "0" causes a voltage less than limit #1 to generate an interrupt.

Bits 10–15 are not used.

Instruction RAM "10"

The third Instruction RAM section is selected by placing a "10" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #2**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12(H)454/8 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first (Instruction RAM "01"), followed by a comparison of the same sampled analog input signal with the value found in limit #2.

Bit 8 holds limit #2's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #2 to generate an interrupt, while a "0" causes a voltage less than limit #2 to generate an interrupt.

Bits 10–15 are not used.

2.2 CONFIGURATION REGISTER

The Configuration register, 1000 (A4–A1, BW = 0) or 1000x (A4–A0, BW = 1) is a 16-bit control register with read/write capability. It acts as the LM12(H)454's and LM12(H)458's "control panel" holding global information as well as start/stop, reset, self-calibration, and stand-by commands.

Bit 0 is the START/STOP bit. Reading Bit 0 returns an indication of the Sequencer's status. A "0" indicates that the Sequencer is stopped and waiting to execute the next instruction. A "1" shows that the Sequencer is running. Writing a "0" halts the Sequencer when the current instruction has finished execution. The next instruction to be executed is pointed to by the instruction pointer found in the status register. A "1" restarts the Sequencer with the instruction currently pointed to by the instruction pointer. (See Bits 8–10 in the Interrupt Status register.)

Bit 1 is the LM12(H)454/8's system RESET bit. Writing a "1" to Bit 1 stops the Sequencer (resetting the Configuration register's START/STOP bit), resets the Instruction pointer to "000" (found in the Interrupt Status register), clears the Conversion FIFO, and resets all interrupt flags. The RESET bit will return to "0" after two clock cycles unless it is forced high by writing a "1" into the Configuration register's Standby bit. A reset signal is internally generated when power is first applied to the part. No operation should be started until the RESET bit is "0".

Writing a "1" to **Bit 2** initiates an auto-zero offset voltage calibration. Unlike the eight-sample auto-zero calibration performed during the full calibration procedure, Bit 2 initiates a "short" auto-zero by sampling the offset once and creating a correction coefficient (full calibration averages eight samples of the converter offset voltage when creating a correction coefficient). If the Sequencer is running when Bit 2 is set to "1", an auto-zero starts immediately after the conclusion of the currently running instruction. Bit 2 is reset automatically to a "0" and an interrupt flag (Bit 3, in the Interrupt Status register) is set at the end of the auto-zero (76 clock cycles). After completion of an auto-zero calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, an auto-zero is performed immediately at the time requested.

Writing a "1" to **Bit 3** initiates a complete calibration process that includes a "long" auto-zero offset voltage correction (this calibration averages eight samples of the comparator offset voltage when creating a correction coefficient) followed by an ADC linearity calibration. This complete calibration is started after the currently running instruction is completed if the Sequencer is running when Bit 3 is set to "1". Bit 3 is reset automatically to a "0" and an interrupt flag (Bit 4, in the Interrupt Status register) will be generated at the end of the calibration procedure (4944 clock cycles). After completion of a full auto-zero and linearity calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, a full calibration is performed immediately at the time requested.

2.0 Internal User-Programmable Registers (Continued)

Bit 4 is the Standby bit. Writing a "1" to Bit 4 immediately places the LM12(H)454/8 in Standby mode. Normal operation returns when Bit 4 is reset to a "0". The Standby command ("1") disconnects the external clock from the internal circuitry, decreases the LM12(H)454/8's internal analog circuitry power supply current, and preserves all internal RAM contents. After writing a "0" to the Standby bit, the LM12(H)454/8 returns to an operating state identical to that caused by exercising the RESET bit. A Standby completion interrupt is issued after a power-up completion delay that allows the analog circuitry to settle. The Sequencer should be restarted only after the Standby completion is issued. The Instruction RAM can still be accessed through read and write operations while the LM12(H)454/8 are in Standby Mode.

Bit 5 is the Channel Address Mask. If Bit 5 is set to a "1", Bits 13–15 in the conversion FIFO will be equal to the sign bit (Bit 12) of the conversion data. Resetting Bit 5 to a "0" causes conversion data Bits 13 through 15 to hold the instruction pointer value of the instruction to which the conversion data belongs.

Bit 6 is used to select a "short" auto-zero correction for every conversion. The Sequencer automatically inserts an auto-zero before every conversion or "watchdog" comparison if Bit 6 is set to "1". No automatic correction will be performed if Bit 6 is reset to "0".

The LM12(H)454/8's offset voltage, after calibration, has a typical drift of 0.1 LSB over a temperature range of −40°C to +85°C. This small drift is less than the variability of the change in offset that can occur when using the auto-zero correction with each conversion. This variability is the result of using only one sample of the offset voltage to create a correction value. This variability decreases when using the full calibration mode because eight samples of the offset voltage are taken, averaged, and used to create a correction value.

Bit 7 is used to program the SYNC pin (29) to operate as either an input or an output. The SYNC pin becomes an output when Bit 7 is a "1" and an input when Bit 7 is a "0". With SYNC programmed as an input, the rising edge of any logic signal applied to pin 29 will start a conversion or "watchdog" comparison. Programmed as an output, the logic level at pin 29 will go high at the start of a conversion or "watchdog" comparison and remain high until either have finished. See Instruction RAM "00", Bit 8.

Bits 8 and **9** form the RAM Pointer that is used to select each of a 48-bit instruction's three 16-bit sections during read or write actions. A "00" selects Instruction RAM section one, "01" selects section two, and "10" selects section three.

Bit 10 activates the Test mode that is used only during production testing. Leave this bit reset to "0".

Bit 11 is the Diagnostic bit and is available only in the LM12(H)458. It can be activated by setting it to a "1" (the Test bit must be reset to a "0"). The Diagnostic mode, along with a correctly chosen instruction, allows verification that the LM12(H)458's ADC is performing correctly. When activated, the inverting and non-inverting inputs are connected as shown in Table I. As an example, an instruction with "001" for both V_{IN+} and V_{IN-} while using the Diagnostic mode typically results in a full-scale output.

2.3 INTERRUPTS

The LM12(H)454 and LM12(H)458 have eight possible interrupts, all with the same priority. Any of these interrupts will cause a hardware interrupt to appear on the $\overline{INT}$ pin (31) if they are not masked (by the Interrupt Enable register). The Interrupt Status register is then read to determine which of the eight interrupts has been issued.

TABLE I. LM12(H)458 Input Multiplexer Channel Configuration Showing Normal Mode and Diagnostic Mode

Channel Selection Data	Normal Mode		Diagnostic Mode	
	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}
000	IN0	GND	V_{REFOUT}	GND
001	IN1	IN1	V_{REF+}	V_{REF-}
010	IN2	IN2	IN2	IN2
011	IN3	IN3	IN3	IN3
100	IN4	IN4	IN4	IN4
101	IN5	IN5	IN5	IN5
110	IN6	IN6	IN6	IN6
111	IN7	IN7	IN7	IN7

TABLE II. LM12(H)454 Input Multiplexer Channel Configuration

Channel Selection Data	MUX+	MUX−
000	IN0	GND
001	IN1	IN1
010	IN2	IN2
011	IN3	IN3
1XX	OPEN	OPEN

The Interrupt Status register, 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1) must be cleared by reading it after writing to the Interrupt Enable register. This removes any spurious interrupts on the $\overline{INT}$ pin generated during an Interrupt Enable register access.

Interrupt 0 is generated whenever the analog input voltage on a selected multiplexer channel crosses a limit while the LM12(H)454/8 are operating in the "watchdog" comparison mode. Two sequential comparisons are made when the LM12(H)454/8 are executing a "watchdog" instruction. Depending on the logic state of Bit 9 in the Instruction RAM's second and third sections, an interrupt will be generated either when the input signal's magnitude is greater than or less than the programmable limits. (See the Instruction RAM, Bit 9 description.) The Limit Status register will indicate which preprogrammed limit, #1 or #2 and which instruction was executing when the limit was crossed.

Interrupt 1 is generated when the Sequencer reaches the instruction counter value specified in the Interrupt Enable register's bits 8–10. This flag appears before the instruction's execution.

Interrupt 2 is activated when the Conversion FIFO holds a number of conversions equal to the programmable value

2.0 Internal User-Programmable Registers (Continued)

stored in the Interrupt Enable register's Bits 11–15. This value ranges from 0001 to 1111, representing 1 to 31 conversions stored in the FIFO. A user-programmed value of 0000 has no meaning. See Section 3.0 for more FIFO information.

The completion of the short, single-sampled auto-zero calibration generates **Interrupt 3**.

The completion of a full auto-zero and linearity self-calibration generates **Interrupt 4**.

Interrupt 5 is generated when the Sequencer encounters an instruction that has its Pause bit (Bit 1 in Instruction RAM "00") set to "1".

The LM12(H)454/8 issues **Interrupt 6** whenever it senses that its power supply voltage is dropping below 4V (typ). This interrupt indicates the potential corruption of data returned by the LM12(H)454/8.

Interrupt 7 is issued after a short delay (10 ms typ) while the LM12(H)454/8 returns from Standby mode to active operation using the Configuration register's Bit 4. This short delay allows the internal analog circuitry to settle sufficiently, ensuring accurate conversion results.

2.4 INTERRUPT ENABLE REGISTER

The Interrupt Enable register at address location 1001 (A4–A1, BW = 0) or 1001x (A4–A0, BW = 1) has READ/WRITE capability. An individual interrupt's ability to produce an external interrupt at pin 31 ($\overline{INT}$) is accomplished by placing a "1" in the appropriate bit location. Any of the internal interrupt-producing operations will set their corresponding bits to "1" in the Interrupt Status register regardless of the state of the associated bit in the Interrupt Enable register. See Section 2.3 for more information about each of the eight internal interrupts.

Bit 0 enables an external interrupt when an internal "watchdog" comparison limit interrupt has taken place.

Bit 1 enables an external interrupt when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 enables an external interrupt when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 enables an external interrupt when the single-sampled auto-zero calibration has been completed.

Bit 4 enables an external interrupt when a full auto-zero and linearity self-calibration has been completed.

Bit 5 enables an external interrupt when an internal Pause interrupt has been generated.

Bit 6 enables an external interrupt when a low power supply condition ($V_A^+ < 4V$) has generated an internal interrupt.

Bit 7 enables an external interrupt when the LM12(H)454/8 return from power-down to active mode.

Bits 8–10 form the storage location of the user-programmable value against which the Sequencer's address is compared. When the Sequencer reaches an address that is equal to the value stored in Bits 8–10, an internal interrupt is generated and appears in Bit 1 of the Interrupt Status register. If Bit 1 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 ($\overline{INT}$).

The value stored in bits 8–10 ranges from 000 to 111, representing 0 to 7 instructions stored in the Instruction RAM. After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer is started by placing a "1" in the Configuration register's START bit. Setting the INT 1 trigger value to 000 **does not generate** an INT 1 the **first** time the Sequencer retrieves and decodes Instruction 000. The Sequencer **generates** INT 1 (by placing a "1" in the Interrupt Status register's Bit 1) the **second time and after** the Sequencer encounters Instruction 000. It is important to remember that the Sequencer continues to operate even if an Instruction interrupt (INT 1) is internally or externally generated. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

Bits 11–15 hold the number of conversions that must be stored in the Conversion FIFO in order to generate an internal interrupt. This internal interrupt appears in Bit 2 of the Interrupt Status register. If Bit 2 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 (INT).

2.5 INTERRUPT STATUS REGISTER

This read-only register is located at address 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1). The corresponding flag in the Interrupt Status register goes high ("1") any time that an interrupt condition takes place, whether an interrupt is enabled or disabled in the Interrupt Enable register. Any of the active ("1") Interrupt Status register flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration Register).

Bit 0 is set to "1" when a "watchdog" comparison limit interrupt has taken place.

Bit 1 is set to "1" when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 is set to "1" when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 is set to "1" when the single-sampled auto-zero has been completed.

Bit 4 is set to "1" when an auto-zero and full linearity self-calibration has been completed.

Bit 5 is set to "1" when a Pause interrupt has been generated.

Bit 6 is set to "1" when a low-supply voltage condition ($V_A^+ < 4V$) has taken place.

Bit 7 is set to "1" when the LM12(H)454/8 return from power-down to active mode.

Bits 8–10 hold the Sequencer's actual instruction address while it is running.

Bits 11–15 hold the actual number of conversions stored in the Conversion FIFO while the Sequencer is running.

2.6 LIMIT STATUS REGISTER

The read-only register is located at address 1101 (A4–A1, BW = 0) or 1101x (A4–A0, BW = 1). This register is used in tandem with the Limit #1 and Limit #2 registers in the Instruction RAM. Whenever a given instruction's input voltage exceeds the limit set in its corresponding Limit register (#1 or #2), a bit, corresponding to the instruction number, is set in the Limit Status register. Any of the active ("1") Limit Status flags are reset to "0" whenever this register is

2.0 Internal User-Programmable Registers (Continued)

read or a device reset is issued (see Bit 1 in the Configuration register). This register holds the status of limits #1 and #2 for each of the eight instructions.

Bits 0–7 show the Limit #1 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #1 register. When, for example, instruction 3 is a "watchdog" operation (Bit 11 is set high) and the input for instruction 3 meets the magnitude and/or polarity data stored in instruction 3's Limit #1 register, Bit 3 in the Limit Status register will be set to a "1".

Bits 8–15 show the Limit #2 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #2 register. When, for example, the input to instruction 6 meets the value stored in instruction 6's Limit #2 register, Bit 14 in the Limit Status register will be set to a "1".

2.7 TIMER

The LM12(H)454/8 have an on-board 16-bit timer that includes a 5-bit pre-scaler. It uses the clock signal applied to pin 23 as its input. It can generate time intervals of 0 through 2^{21} clock cycles in steps of 2^5. This time interval can be used to delay the execution of instructions. It can also be used to slow the conversion rate when converting slowly changing signals. This can reduce the amount of redundant data stored in the FIFO and retrieved by the controller.

The user-defined timing value used by the Timer is stored in the 16-bit READ/WRITE Timer register at location 1011 (A4–A1, BW = 0) or 1011x (A4–A0, BW = 1) and is preloaded automatically. Bits 0–7 hold the preset value's low byte and Bits 8–15 hold the high byte. The Timer is activated by the Sequencer only if the current instruction's Bit 9 is set ("1"). If the equivalent decimal value "N" ($0 \leq N \leq 2^{16} - 1$) is written inside the 16-bit Timer register and the Timer is enabled by setting an instruction's bit 9 to a "1", the Sequencer will delay the same instruction's execution by halting at state 3 (S3), as shown in *Figure 11,* for $32 \times N + 2$ clock cycles.

2.8 DMA

The DMA works in tandem with Interrupt 2. An active DMA Request on pin 32 (DMARQ) requires that the FIFO interrupt be enabled. The voltage on the DMARQ pin goes high when the number of conversions in the FIFO equals the 5-bit value stored in the Interrupt Enable register (bits 11–15). The voltage on the $\overline{INT}$ pin goes low at the same time as the voltage on the DMARQ pin goes high. The voltage on the DMARQ pin goes low when the FIFO is emptied. The Interrupt Status register must be read to clear the FIFO interrupt flag in order to enable the next DMA request.

DMA operation is optimized through the use of the 16-bit databus connection (a logic "0" applied to the BW pin). Using this bus width allows DMA controllers that have single address Read/Write capability to easily unload the FIFO. Using DMA on an 8-bit databus is more difficult. Two read operations (low byte, high byte) are needed to retrieve each conversion result from the FIFO. Therefore, the DMA controller must be able to repeatedly access two constant addresses when transferring data from the LM12(H)454/8 to the host system.

3.0 FIFO

The result of each conversion stored in an internal read-only FIFO (First-In, First-Out) register. It is located at 1100 (A4–A1, BW = 0) or 1100x (A4–A0, BW = 1). This register has 32 16-bit wide locations. Each location holds 13-bit data. Bits 0–3 hold the four LSB's in the 12 bits + sign mode or "1110" in the 8 bits + sign mode. Bits 4–11 hold the eight MSB's and Bit 12 holds the sign bit. Bits 13–15 can hold either the sign bit, extending the register's two's complement data format to a full sixteen bits or the instruction address that generated the conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

The FIFO status should be read in the Interrupt Status register (Bits 11–15) to determine the number of conversion results that are held in the FIFO before retrieving them. This will help prevent conversion data corruption that may take place if the number of reads are greater than the number of conversion results contained in the FIFO. Trying to read the FIFO when it is empty may corrupt new data being written into the FIFO. Writing more than 32 conversion data into the FIFO by the ADC results in loss of the first conversion data. Therefore, to prevent data loss, it is recommended that the LM12(H)454/8's interrupt capability be used to inform the system controller that the FIFO is full.

The lower portion (A0 = 0) of the data word (Bits 0–7) should be read first followed by a read of the upper portion (A0 = 1) when using the 8-bit bus width (BW = 1). Reading the upper portion first causes the data to shift down, which results in loss of the lower byte.

Bits 0–12 hold 12-bit + sign conversion data. **Bits 0–3** will be 1110 (LSB) when using 8-bit plus sign resolution.

Bits 13–15 hold either the instruction responsible for the associated conversion data or the sign bit. Either mode is selected with Bit 5 in the Configuration register.

Using the FIFO's full depth is achieved as follows. Set the value of the Interrupt Enable register's Bits 11–15 to 11111 and the Interrupt Enable register's Bit 2 to a "1". This generates an external interrupt when the 31st conversion is stored in the FIFO. This gives the host processor a chance to send a "0" to the LM12(H)454/8's Start bit (Configuration register) and halt the ADC before it completes the 32nd conversion. The Sequencer halts after the current (32) conversion is completed. The conversion data is then transferred to the FIFO and occupies the 32nd location. FIFO overflow is avoided if the Sequencer is halted before the start of the 32nd conversion by placing a "0" in the Start bit (Configuration register). It is important to remember that the Sequencer **continues to operate even if a FIFO interrupt (INT 2) is internally or externally generated**. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

4.0 Sequencer

The Sequencer uses a 3-bit counter (Instruction Pointer, or IP, in *Figure 7)* to retrieve the programmable conversion instructions stored in the Instruction RAM. The 3-bit counter is reset to 000 during chip reset or if the current executed instruction has its Loop bit (Bit 1 in any Instruction RAM "00") set high ("1"). It increments at the end of the currently executed instruction and points to the next instruction. It will continue to increment up to 111 unless an instruction's Loop bit is set. If this bit is set, the counter resets to "000" and execution begins again with the first instruction. If all instructions have their Loop bit reset to "0", the Sequencer will execute all eight instructions continuously. Therefore, it is important to realize that if less than eight instructions are programmed, the Loop bit on the last instruction must be set. Leaving this bit reset to "0" allows the Sequencer to execute "unprogrammed" instructions, the results of which may be unpredictable.

The Sequencer's Instruction Pointer value is readable at any time and is found in the Status register at Bits 8–10. The Sequencer can go through eight states during instruction execution:

State 0: The current instruction's first 16 bits are read from the Instruction RAM "00". This state is one clock cycle long.

State 1: Checks the state of the Calibration and Start bits. This is the "rest" state whenever the Sequencer is stopped using the reset, a Pause command, or the Start bit is reset low ("0"). When the Start bit is set to a "1", this state is one clock cycle long.

State 2: Perform calibration. If bit 2 or bit 6 of the Configuration register is set to a "1", state 2 is 76 clock cycles long. If the Configuration register's bit 3 is set to a "1", state 2 is 4944 clock cycles long.

State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below

$$32T + 2$$

where $0 \leq T \leq 2^{16} - 1$.

State 7: Run the acquisition delay and read Limit #1's value if needed. The number of clock cycles for 12-bit + sign mode varies according to

$$9 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

The number of clock cycles for 8-bit + sign or "watchdog" mode varies according to

$$2 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

State 6: Perform first comparison. This state is 5 clock cycles long.

State 4: Read Limit #2. This state is 1 clock cycle long.

State 5: Perform a conversion or second comparison. This state takes 44 clock cycles when using the 12-bit + sign mode or 21 clock cycles when using the 8-bit + sign mode. The "watchdog" mode takes 5 clock cycles.

4.0 Sequencer (Continued)

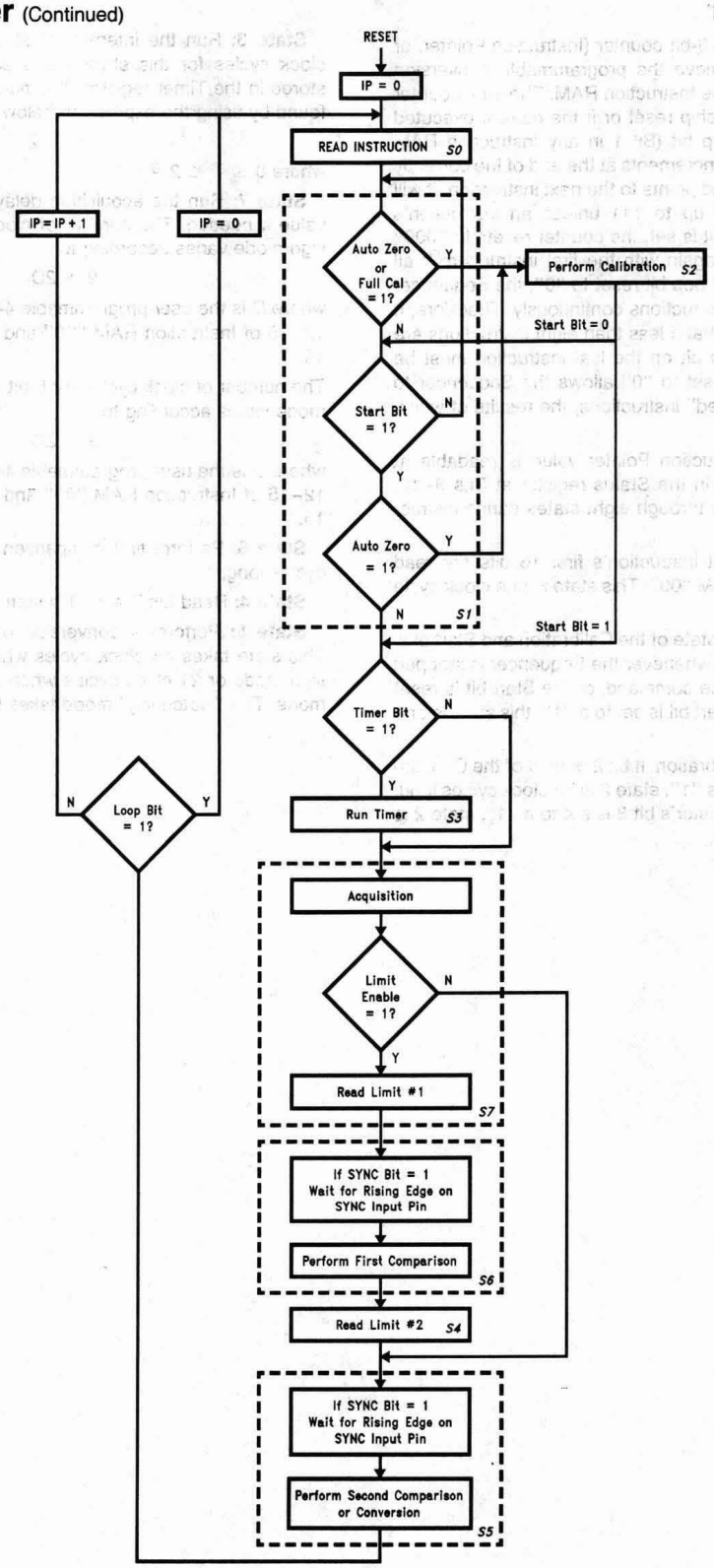

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FIGURE 11. Sequencer Logic Flow Chart (IP = Instruction Pointer)

5.0 Analog Considerations

5.1 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF+} and V_{REF-} defines the analog input voltage span (the difference between the voltages applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF+} or V_{REF-} must have very low output impedance and noise. The circuit in *Figure 12* is an example of a very stable reference appropriate for use with the LM12(H)454/8.

The ADC can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF+} pin is connected to V_A^+ and V_{REF-} is connected to GND. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions.

For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

When using the LM12(H)454/8's internal 2.5V bandgap reference, a parallel combination of a 100 μF capacitor and a 0.1 μF capacitor connected to the V_{REFOUT} pin is recommended for low noise operation. When left unconnected, the reference remains stable without a bypass capacitor. However, ensure that stray capacitance at the V_{REFOUT} pin remains below 50 pF.

5.2 INPUT RANGE

The LM12(H)454/8's fully differential ADC and reference voltage inputs generate a two's-complement output that is found by using the equation below.

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (4096) - \tfrac{1}{2} \qquad \text{(12-bit)}$$

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (256) - \tfrac{1}{2} \qquad \text{(8-bit)}$$

Round up to the next integer value between -4096 to 4095 for 12-bit resolution and between -256 to 255 for 8-bit resolution if the result of the above equation is not a whole number. As an example, V_{REF+} = 2.5V, V_{REF-} = 1V, V_{IN+} = 1.5V and V_{IN-} = GND. The 12-bit + sign output code is positive full-scale, or 0,1111,1111,1111. If V_{REF+} = 5V, V_{REF-} = 1V, V_{IN+} = 3V, and V_{IN-} = GND, the 12-bit + sign output code is 0,1100,0000,0000.

5.3 INPUT CURRENT

A charging current flows into or out of (depending on the input voltage polarity) the analog input pins, IN0–IN7 at the start of the analog input acquisition time (t_{ACQ}). This current's peak value will depend on the actual input voltage applied.

5.4 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<100Ω for 5 MHz operation and <60Ω for 8 MHz operation), the input charging current will decay, before the end of the S/H's acquisition time, to a value that will not introduce any conversion errors. For higher source impedances, the S/H's acquisition time can be increased. As an example, operating with a 5 MHz clock frequency and maximum acquisition time, the LM12(H)454/8's analog inputs can handle source impedance as high as 6.67 kΩ. When operating at 8 MHz and maximum acquisition time, the LM12H454/8's analog inputs can handle source impedance as high as 4.17 kΩ. Refer to Section 2.1, Instruction RAM "00", Bits 12–15 for further information.

5.5 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, IN0–IN7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. It will not degrade the conversion accuracy.

5.6 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

5.7 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF monolithic ceramic capacitors are recom-

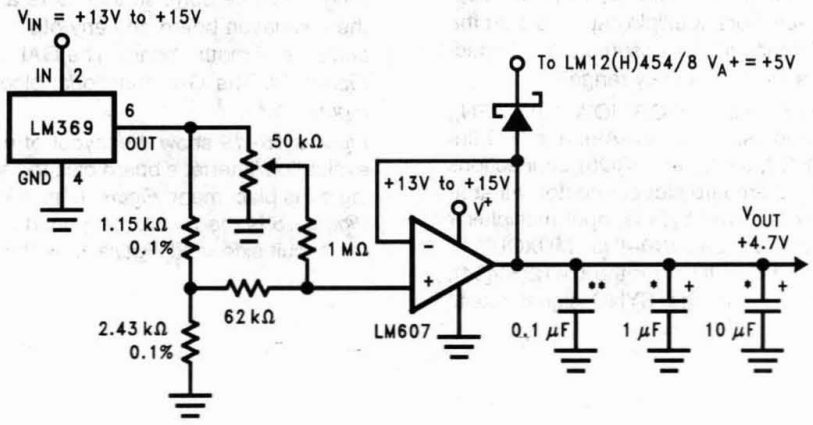


FIGURE 12. Low Drift Extremely Stable Reference Circuit

5.0 Analog Considerations (Continued)

mended for supply bypassing. Separate bypass capacitors should be used for the V_A+ and V_D+ supplies and placed as close as possible to these pins.

5.8 GROUNDING

The LM12(H)454/8's nominal high resolution performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all analog signal handling circuitry. The digital and analog ground planes are connected at only one point, the power supply ground. This greatly reduces the occurrence of ground loops and noise.

It is recommended that stray capacitance between the analog inputs or outputs (LM12(H)454: IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+, S/H IN−; LM12(H)458: IN0–IN7, $V_{REF}+$, and $V_{REF}-$) be reduced by increasing the clearance ($+1/16$th inch) between the analog signal and reference pins and the ground plane.

5.9 CLOCK SIGNAL LINE ISOLATION

The LM12(H)454/8's performance is optimized by routing the analog input/output and reference signal conductors (pins 34–44) as far as possible from the conductor that carries the clock signal to pin 23. Ground traces parallel to the clock signal trace can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

6.0 Application Circuits

6.1 PC EVALUATION/INTERFACE BOARD

Figure 13 is the schematic of an evaluation/interface board designed to interface the LM12(H)454 or LM12(H)458 with an XT or AT style computer. The board can be used to develop both software and hardware. The board hardwires the BW (Bus Width) pin to a logic high, selecting an 8-bit wide databus. Therefore, it is designed for an 8-bit expansion slot on the computer's motherboard.

The circuit operates on a single +5V supply derived from the computer's +12V supply using an LM340 regulator. This greatly attenuates noise that may be present on the computer's power supply lines. However, your application may only need an LC filter.

Figure 13 also shows the recommended supply (V_A+ and V_D+) and reference input ($V_{REF}+$ and $V_{REF}-$) bypassing. The digital and analog supply pins can be connected together to the same supply voltage. However, they need separate, multiple bypass capacitors. Multiple capacitors on the supply pins and the reference inputs ensures a low impedance bypass path over a wide frequency range.

All digital interface control signals (IOR, IOW, and AEN), data lines (DB0–DB7), address lines (A0–A9), and IRQ (interrupt request) lines (IRQ2, IRQ3, and IRQ5) connections are made through the motherboard slot connector. All analog signals applied to, or received by, the input multiplexer (IN0–IN7 for the LM12(H)458 and IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+ and S/H IN− for the LM12(H)454), $V_{REF}+$, $V_{REF}-$, V_{REFOUT}, and the SYNC signal input/output are applied through a DB-37 connector on the rear side of the board. *Figure 13* shows that there are numerous analog ground connections available on the DB-37 connector.

The voltage applied to $V_{REF}-$ and $V_{REF}+$ is selected using two jumpers, JP1 and JP2. JP1 selects between the voltage applied to the DB-37's pin 24 or GND and applies it to the LM12(H)454/8's $V_{REF}-$ input. JP2 selects between the LM12(H)454/8's internal reference output, V_{REFOUT}, and the voltage applied to the DB-37's pin 22 and applies it to the LM12(H)454/8's $V_{REF}+$ input.

TABLE III. LM12(H)454/8 Evaluation/Interface Board SW DIP-8 Switch Settings for Available I/O Memory Locations

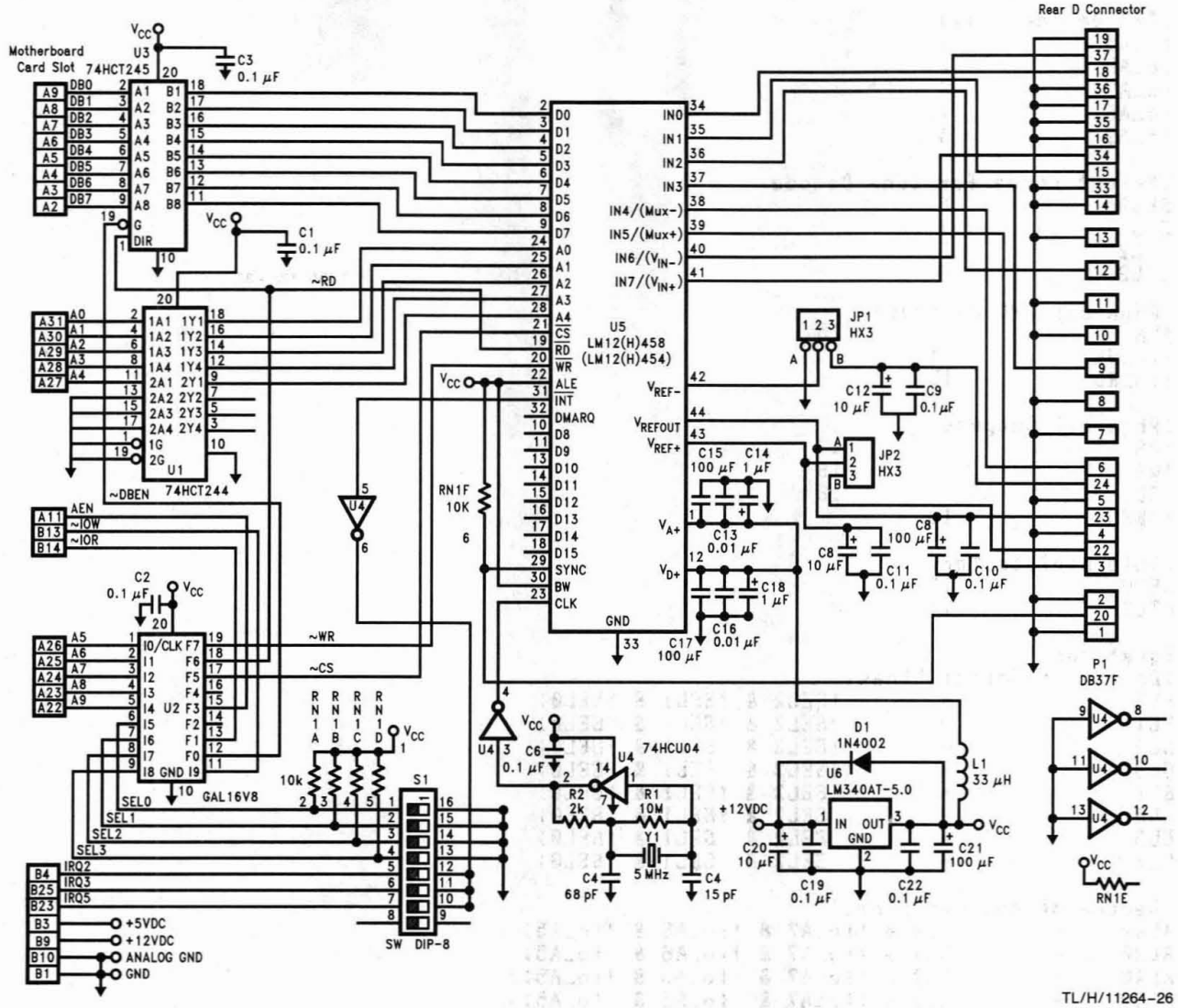
Hexidecimal I/O Memory Base Address	SW DIP-8			
	SW1 (SEL0)	SW2 (SEL1)	SW3 (SEL2)	SW4 (SEL3)
100	ON	ON	ON	ON
120	OFF	ON	ON	ON
140	ON	OFF	ON	ON
160	OFF	OFF	ON	ON
180	ON	ON	OFF	ON
1A0	OFF	ON	OFF	ON
1C0	ON	OFF	OFF	ON
300	OFF	OFF	OFF	ON
340	ON	ON	ON	OFF
280	OFF	ON	ON	OFF
2A0	ON	OFF	ON	OFF

The board allows the use of one of three Interrupt Request (IRQ) lines IRQ2, IRQ3, and IRQ5. The individual IRQ line can be selected using switches 5, 6, and 7 of SW DIP-8. When using any of these three IRQs, the user needs to ensure that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard.

Switches 1–4, along with address lines A5–A9 are used as inputs to GAL16V8 Programmable Gate Array (U2). This device forms the interface between the computer's control and address lines and generates the control signals used by the LM12(H)454/8 for $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$. It also generates the signal that controls the data buffers. Several address ranges within the computer's I/O memory map are available. Refer to Table III for the switch settings that gives the desired I/O memory address range. Selection of an address range must be done so that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard. The GAL equations are shown in *Figure 14*. The GAL functional block diagram is shown in *Figure 15*.

Figures 16–19 show the layout of each layer in the 3-layer evaluation/interface board plus the silk-screen layout showing parts placement. *Figure 17* is the top or component side, *Figure 18* is the middle or ground plane layer, *Figure 19* is the circuit side, and *Figure 16* is the parts layout.

6.0 Application Circuits (Continued)



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Note: The layout utilizes a split ground plane. The analog ground plane is placed under all analog signals and U5 pins 1, 34–44. The remaining signals and pins are placed over the digital ground. The single point ground connection is at U6, pin 2, and this is connected to the motherboard pin B1.

Parts List:

Y1	HC49U, 8 MHz crystal	C7, C21	100 µF, 25V, electrolytic
D1	1N4002	C8, C12, C20	10 µF, 35V, electrolytic
L1	33 µH	C13, C16	0.01 µF, 50V, monolithic ceramic
P1	DB37F; parallel connector	C14, C18	1 µF, 35V, tantalum
R1	10 MΩ, 5%, ¼W	C15, C17	100 µF, 50V, ceramic disk
R2	2 kΩ, 5%, ¼W	U1	MM74HCT244N
RN1	10 kΩ, 6 resistor SIP, 5%, ⅛W	U2	GAL16V8-20LNC
JP1, JP2	HX3, 3-pin jumper	U3	MM74HCT245N
S1	SW DIP-8; 8 SPST switches	U4	MM74HCU04N
C1–3, C6, C9–11, C19, C22	0.1 µF, 50V, monolithic ceramic	U5	LM12(H)458CIV or LM12(H)454CIV
C4	68 pF, 50V, ceramic disk	U6	LM340AT-5.0
C5	15 pF, 50V, ceramic disk	SK1	44-pin PLCC socket
		A1	LM12(H)458/4 Rev. D PC Board

FIGURE 13. Schematic and Parts List for the LM12(H)454/8 Evaluation/Interface Board for XT and AT Style Computers, Order Number LM12458EVAL

6.0 Application Circuits (Continued)

```
;I/O Decode Lines
io_A5           1
io_A6           2
io_A7           3
io_A8           4
io_A9           5

;Select Lines for Zone Decode
SEL0            6
SEL1            7
SEL2            8
SEL3            9

;Physical I/O Controls
AEN                     15
!io_WR          11
!io_RD          13

;Physical Outputs
!CS                     17
!WR                     19
!RD                     18
!DBEN           12

;Intermediate Terms:
DEC0            16
FILT            14

Equations
;Decode of Select Lines:
SL0             =       !SEL2 & !SEL1 & !SEL0;
SL1             =       !SEL2 & !SEL1 &  SEL0;
SL2             =       !SEL2 &  SEL1 & !SEL0;
SL3             =       !SEL2 &  SEL1 &  SEL0;
SL4             =        SEL2 & !SEL1 & !SEL0;
SL5             =        SEL2 & !SEL1 &  SEL0;
SL6             =        SEL2 &  SEL1 & !SEL0;
SL7             =        SEL2 &  SEL1 &  SEL0;

;Decode of Address Lines:
AL00    =       SL0 & !io_A7 & !io_A6 & !io_A5;
AL20    =       SL1 & !io_A7 & !io_A6 &  io_A5;
AL40    =       SL2 & !io_A7 &  io_A6 & !io_A5;
AL60    =       SL3 & !io_A7 &  io_A6 &  io_A5;
AL80    =       SL4 &  io_A7 & !io_A6 & !io_A5;
ALA0    =       SL5 &  io_A7 & !io_A6 &  io_A5;
ALC0    =       SL6 &  io_A7 &  io_A6 & !io_A5;

AH01    =       !SEL3 & !io_A9 &  io_A8;
AH02    =        SEL3 &  io_A9 & !io_A8 &  io_A7 & !io_A6;
AH03    =        SEL3 &  io_A9 &  io_A8 & !io_A7 & !io_A5;

;Intermediate Address Groups:
DEC0    =       !AEN & (AL00 + AL20 + AL40 + AL60 + AL80 + ALA0 + ALC0);

;DAS Chip Select Decode:
FILT    =       CS & ( io_WR + io_RD);
CS              =       ( io_WR  + io_RD) & DEC0 & ( AH01 + AH02 + AH03);
DBEN    =       CS & DEC0 & ( io_WR + io_RD);

;Delayed Read/ Write Decodes:
WR              =       io_WR & FILT;
RD              =       io_RD & FILT;
```

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FIGURE 14. Logic Equations Used to Program the GAL16V8

6.0 Application Circuits (Continued)

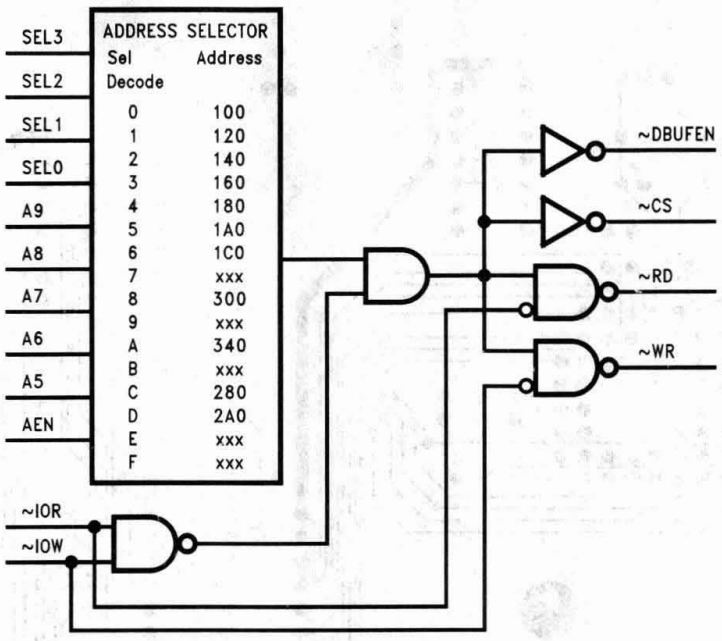

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FIGURE 15. GAL Functional Block Diagram

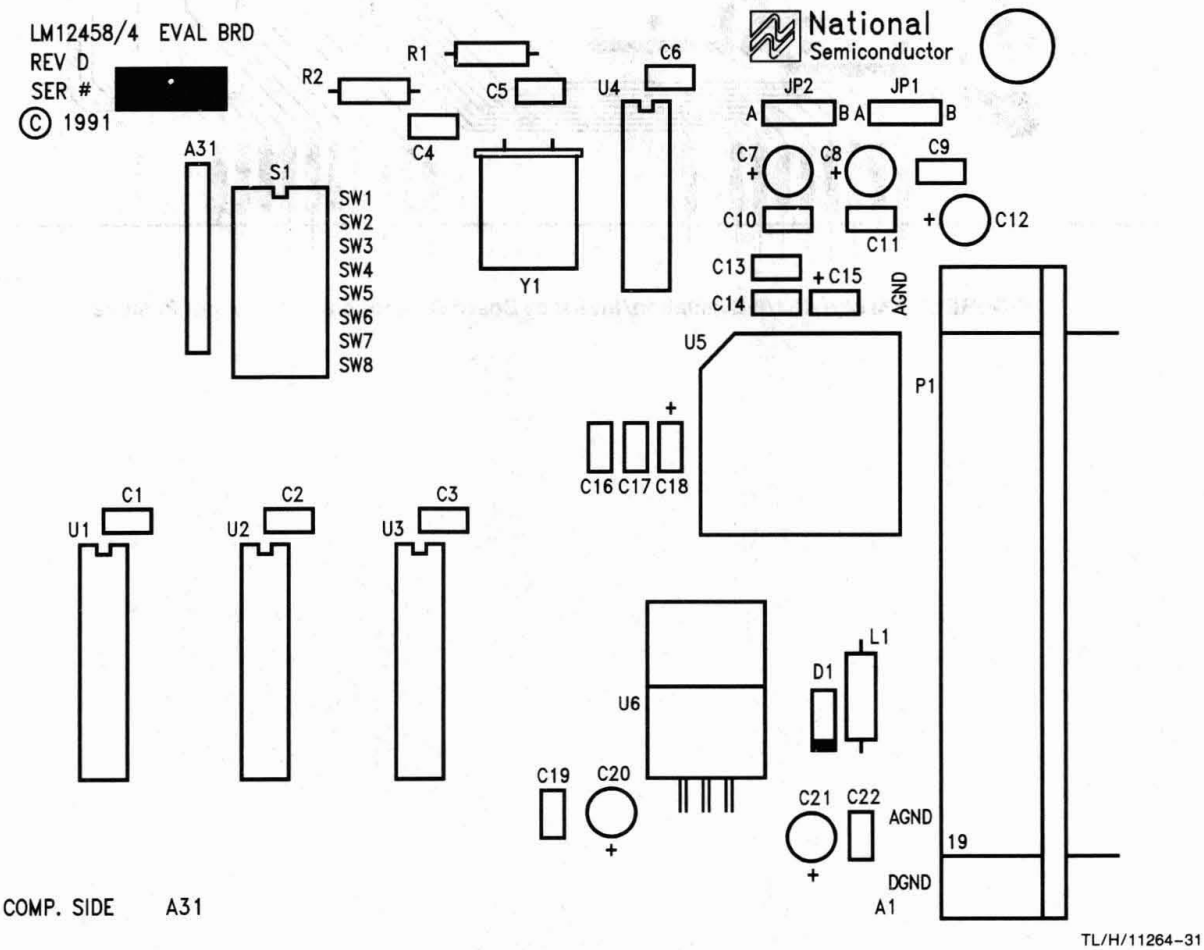

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FIGURE 16. Silk-Screen Layout Showing Parts Placement on the LM12(H)454/8 Evaluation/Interface Board

6.0 Application Circuits (Continued)

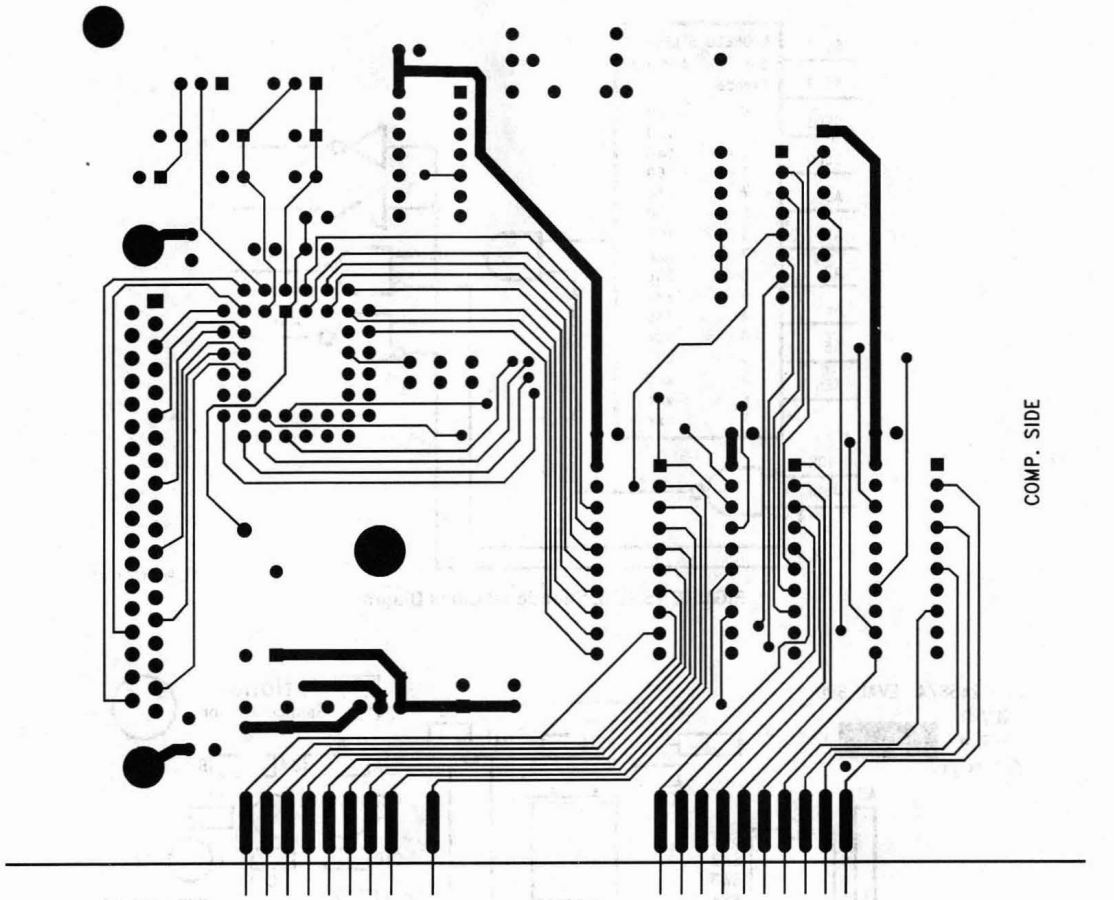

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FIGURE 17. LM12(H)454/8 Evaluation/Interface Board Component-Side Layout Positive

6.0 Application Circuits (Continued)

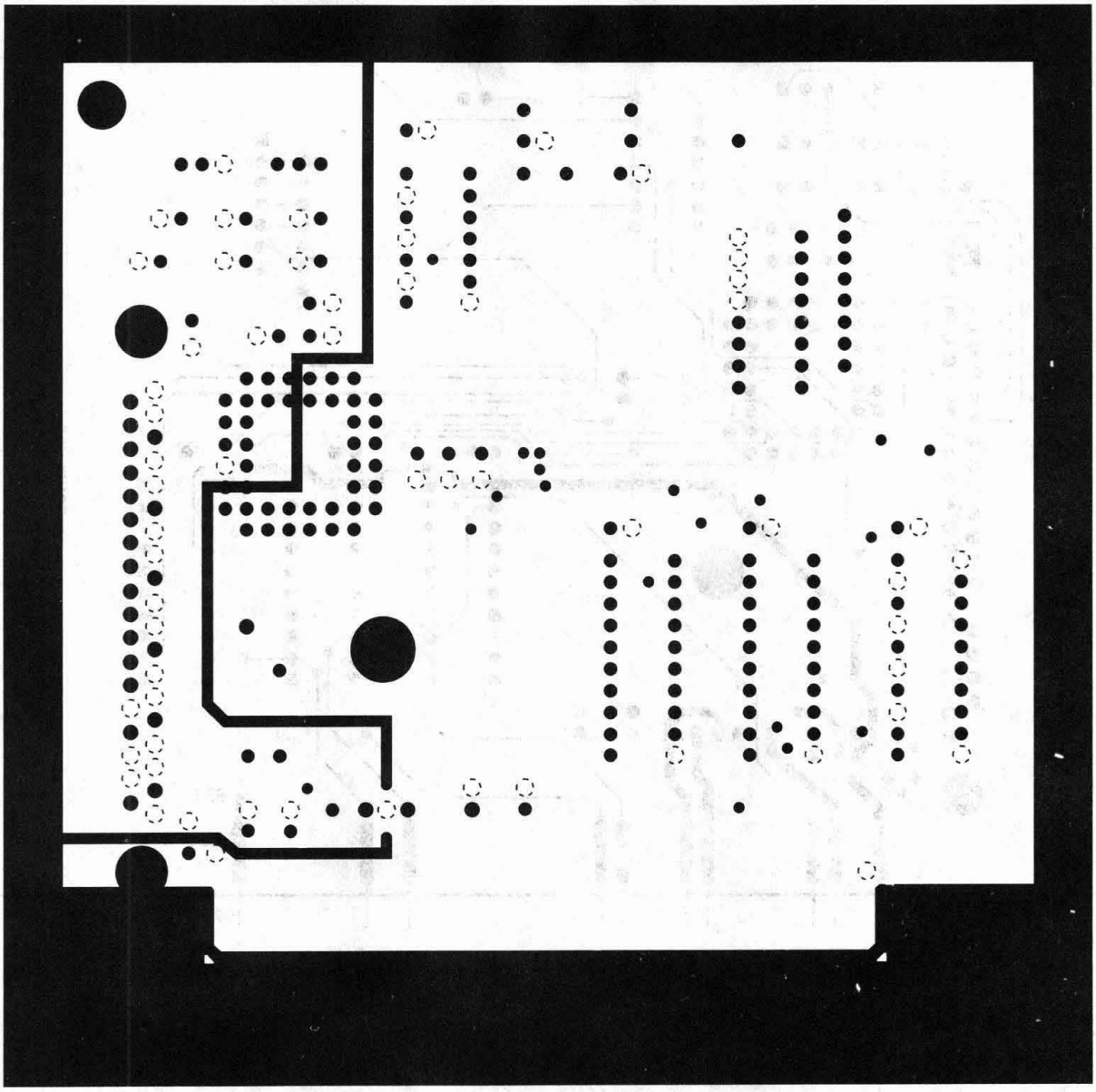

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FIGURE 18. LM12(H)454/8 Evaluation/Interface Board Ground-Plane Layout Negative

6.0 Application Circuits (Continued)

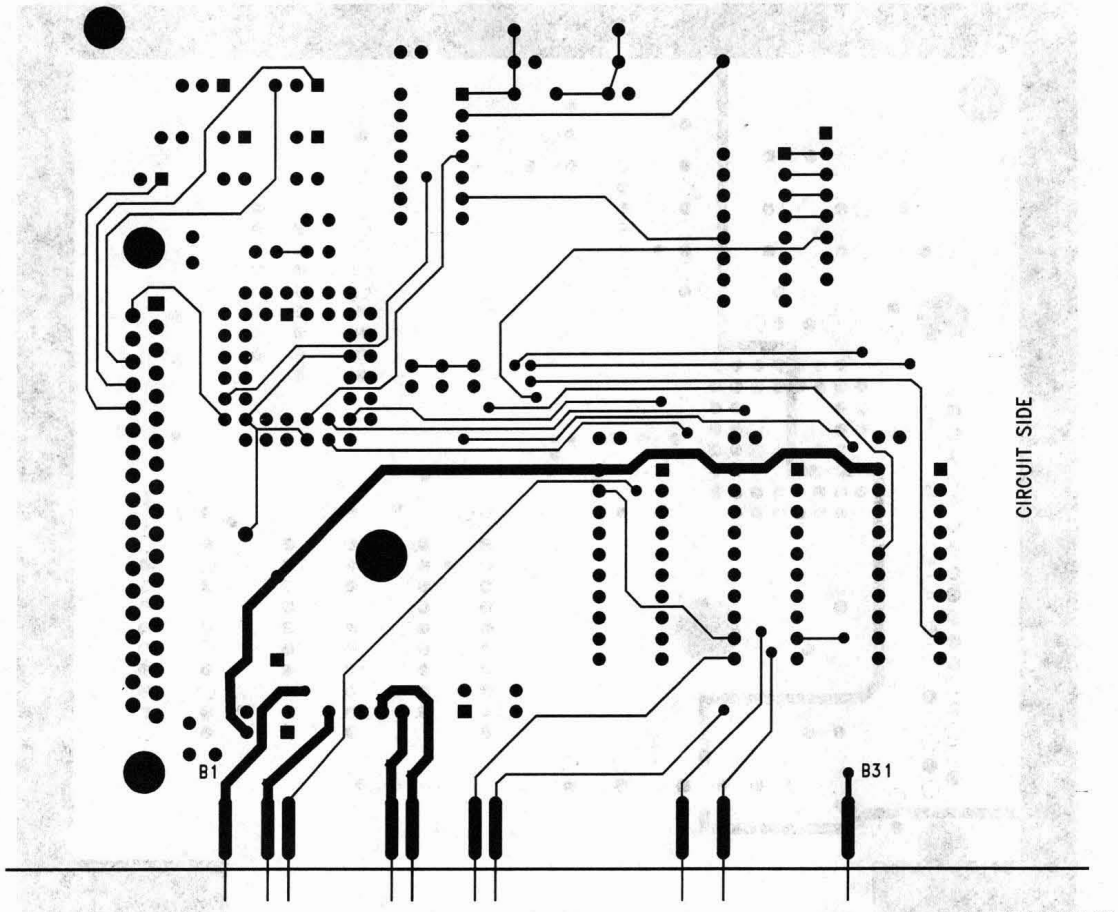

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FIGURE 19. LM12(H)454/8 Evaluation/Interface Circuit-Side Layout Positive

National Semiconductor

LM12L454/LM12L458 12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12L454 and LM12L458 are highly integrated 3.3V Data Acquisition Systems. They combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12L458's eight-input multiplexer. The LM12L454 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12L454 and LM12L458 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits. Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit databus. The LM12L454 and LM12L458 include a direct memory access (DMA) interface for high-speed conversion data transfer.

Key Specifications (f_{CLK} = 6 MHz)

- Resolution — 12-bit + sign or 8-bit + sign
- 13-bit conversion time — 7.3 μs
- 9-bit conversion time — 3.5 μs
- 13-bit Through-put rate — 106k samples/s (min)
- Comparison time ("watchdog" mode) — 1.8 μs (max)
- ILE — ±1 LSB (max)
- V_{IN} range — GND to V_A^+
- Power dissipation — 15 mW (max)
- Stand-by mode — 5 μW (typ)
- Single supply — 3V to 5.5V

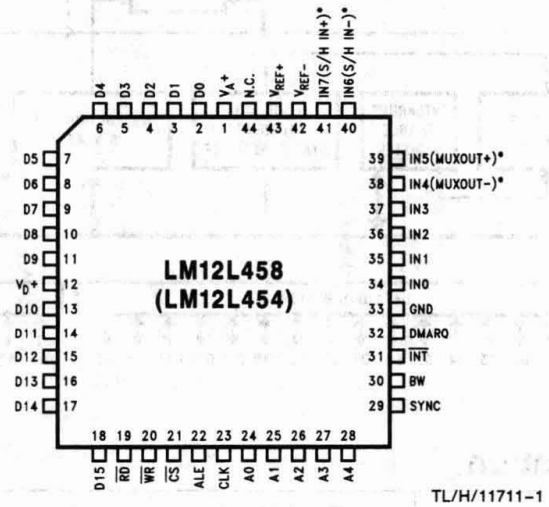
Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog"
- Single-ended or differential inputs
- Built-in Sample-and-Hold
- Instruction RAM and event sequencer
- 8-channel (LM12L458), 4-channel (LM12L454) multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide databus microprocessor or DSP interface
- CMOS compatible I/O

Applications

- Data Logging
- Process Control
- Energy Management
- Medical Instrumentation

Connection Diagram



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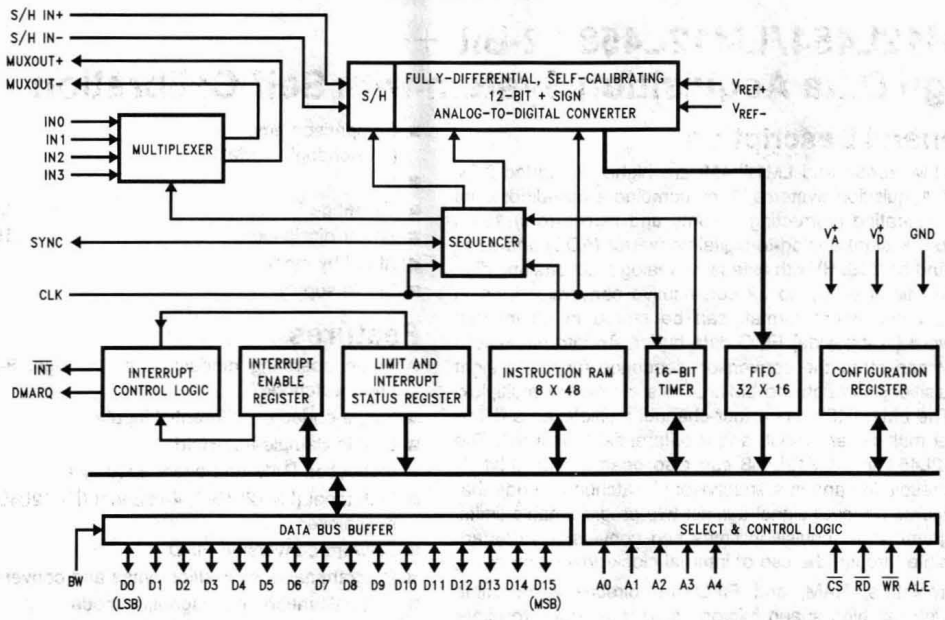
*Pin names in ( ) apply to the LM12L454.

Order Number LM12L454CIV or LM12L458CIV
See NS Package Number V44A

Functional Diagrams

LM12L454



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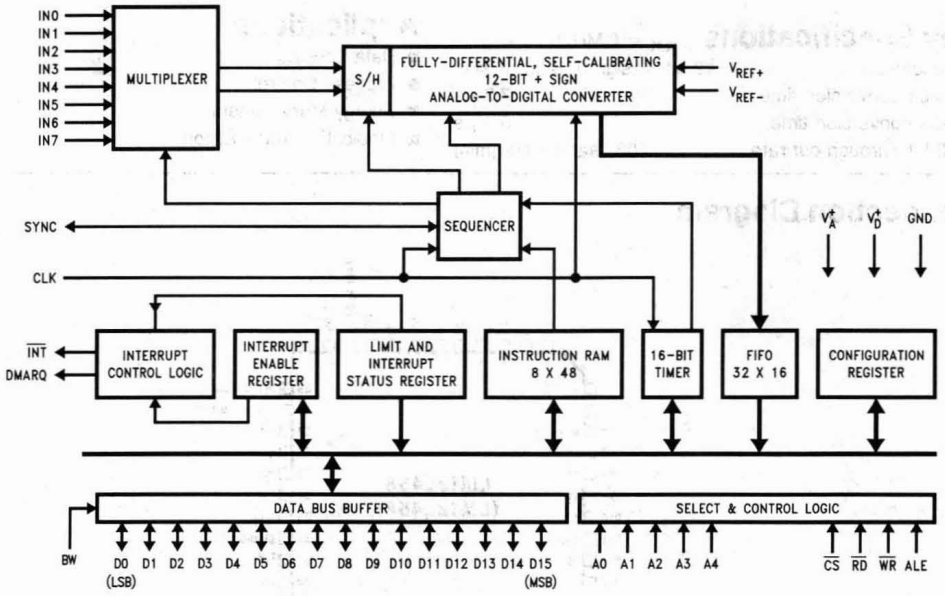
LM12L458



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Ordering Information

Guaranteed Clock Freq (min)	Guaranteed Linearity Error (max)	Order Part Number	See NS Package Number
6 MHz	±1.0 LSB	LM12L454CIV	V44A
		LM12L458CIV	V44A

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_A^+ and V_D^+)	6.0V
Voltage at Input and Output Pins except IN0–IN3 (LM12L454) and IN0–IN7 (LM12L458)	−0.3V to V^+ + 0.3V
Voltage at Analog Inputs IN0–IN3 (LM12L454) and IN0–IN7 (LM12L458)	GND − 5V to V^+ + 5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation (T_A = 25°C) V Package (Note 4)	875 mW
Storage Temperature	−65°C to +150°C
Lead Temperature V Package, Infrared, 15 sec.	+300°C
ESD Susceptibility (Note 5)	1.5 kV

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1, 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$) LM12L454CIV/LM12L458CIV	−40°C ≤ T_A ≤ 85°C
Supply Voltage V_A^+, V_D^+	3.0V to 5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤100 mV
V_{IN+} Input Range	GND ≤ V_{IN+} ≤ V_A^+
V_{IN-} Input Range	GND ≤ V_{IN-} ≤ V_A^+
V_{REF+} Input Voltage	1V ≤ V_{REF+} ≤ V_A^+
V_{REF-} Input Voltage	0V ≤ V_{REF-} ≤ V_{REF+} − 1V
V_{REF+} − V_{REF-}	1V ≤ V_{REF} ≤ V_A^+
V_{REF} Common Mode Range (Note 16)	0.1 V_A^+ ≤ V_{REFCM} ≤ 0.6 V_A^+

Converter Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 6.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \le 25\Omega$, fully-differential input with fixed 1.25V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
ILE	Positive and Negative Integral Linearity Error	After Auto-Cal (Notes 12, 17)	±1/2	**±1**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Note 12)	±1		LSB
	Resolution with No Missing Codes	After Auto-Cal (Note 12)		**13**	Bits (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1**	LSB (max)
	Zero Error	After Auto-Cal (Notes 13, 17)	±1/4	**±1**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 17)	±1/2	**±3**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 17)	±1/2	**±3**	LSB (max)
	DC Common Mode Error	(Note 14)	±2	**±4**	LSB (max)
ILE	8-Bit + Sign and "Watchdog" Mode Positive and Negative Integral Linearity Error	(Note 12)		**±1/2**	LSB (max)
TUE	8-Bit + Sign and "Watchdog" Mode Total Unadjusted Error	After Auto-Zero	±1/2	**±3/4**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Resolution with No Missing Codes			**9**	Bits (max)
DNL	8-Bit + Sign and "Watchdog" Mode Differential Non-Linearity			**±1**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Zero Error	After Auto-Zero		**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Positive and Negative Full-Scale Error			**±1/2**	LSB (max)

Converter Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 6.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 1.25V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 9) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
	8-Bit + Sign and "Watchdog" Mode DC Common Mode Error		±1/8		LSB
	Multiplexer Channel-to-Channel Matching		±0.05		LSB
V_{IN+}	Non-Inverting Input Range			**GND** **V_A^+**	V (min) V (max)
V_{IN-}	Inverting Input Range			**GND** **V_A^+**	V (min) V (max)
$V_{IN+} - V_{IN-}$	Differential Input Voltage Range			**$-V_A^+$** **V_A^+**	V (min) V (max)
$\frac{V_{IN+} - V_{IN-}}{2}$	Common Mode Input Voltage Range			**GND** **V_A^+**	V (min) V (max)
PSS	Power Supply Sensitivity (Note 15) — Zero Error Full-Scale Error Linearity Error	$V_A^+ = V_D^+ = 3.3V \pm 10\%$ $V_{REF+} = 2.5V$, $V_{REF-} = GND$	±0.2 ±0.4 ±0.2	**±1.75** **±2**	LSB (max) LSB (max) LSB
C_{REF}	V_{REF+} / V_{REF-} Input Capacitance		85		pF
C_{IN}	Selected Multiplexer Channel Input Capacitance		75		pF

Converter AC Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 6.0$ MHz, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 1.25V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, 8, and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
	Clock Duty Cycle		50	 **40** **60**	% % (min) % (max)
t_C	Conversion Time	13-Bit Resolution, Sequencer State S5 *(Figure 11)*	44 (t_{CLK})	**44 (t_{CLK}) + 50 ns**	(max)
		9-Bit Resolution, Sequencer State S5 *(Figure 11)*	21 (t_{CLK})	**21 (t_{CLK}) + 50 ns**	(max)
t_A	Acquisition Time	Sequencer State S7 *(Figure 11)* Built-in minimum for 13-Bits	9 (t_{CLK})	**9 (t_{CLK}) + 50 ns**	(max)
		Built-in minimum for 9-Bits and "Watchdog" mode	2 (t_{CLK})	**2 (t_{CLK}) + 50 ns**	(max)
t_Z	Auto-Zero Time	Sequencer State S2 *(Figure 11)*	76 (t_{CLK})	**76 (t_{CLK}) + 50 ns**	(max)
t_{CAL}	Full Calibration Time	Sequencer State S2 *(Figure 11)*	4944 (t_{CLK})	**4944 (t_{CLK}) + 50 ns**	(max)
	Throughput Rate (Note 18)		107	**106**	kHz (min)
t_{WD}	"Watchdog" Mode Comparison Time	Sequencer States S6, S4, and S5 *(Figure 11)*	11 (t_{CLK})	**11 (t_{CLK}) + 50 ns**	(max)
t_{PU}	Power-Up Time		10		ms
t_{WU}	Wake-Up Time		10		ms

DC Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, $f_{CLK} = 6.0$ MHz and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
I_D^+	V_D^+ Supply Current	$\overline{CS}$ = "1" LM12L454/8	0.4	**1.0**	mA (max)
I_A^+	V_A^+ Supply Current	$\overline{CS}$ = "1" LM12L454/8	2.25	**3.5**	mA (max)
I_{ST}	Stand-By Supply Current ($I_D^+ + I_A^+$)	Power-Down Mode Selected Clock Stopped 6 MHz Clock	 1.5 30	 4.5	 μA (max) μA (max)
	Multiplexer ON-Channel Leakage Current	$V_A^+ = 3.6V$ ON-Channel = 3.6V, OFF-Channel = 0V ON-Channel = 0V, OFF-Channel = 3.6V	 0.1 0.1	 **0.3** **0.3**	 μA (max) μA (max)
	Multiplexer OFF-Channel Leakage Current	$V_A^+ = 3.6V$ ON-Channel = 3.6V, OFF-Channel = 0V ON-Channel = 0V, OFF-Channel = 3.6V	 0.1 0.1	 **0.3** **0.3**	 μA (max) μA (max)
R_{ON}	Multiplexer ON-Resistance	LM12L454 $V_{IN} = 3.3V$ $V_{IN} = 1.65V$ $V_{IN} = 0V$	 850 1300 830	 **1500** **2000** **1500**	 Ω(max) Ω(max) Ω(max)
	Multiplexer Channel-to-Channel R_{ON} matching	LM12L454 $V_{IN} = 3.3V$ $V_{IN} = 1.65V$ $V_{IN} = 0V$	 ±1.0% ±1.0% ±1.0%	 ±**3.0%** ±**3.0%** ±**3.0%**	 (max) (max) (max)

1

Digital Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage	$V_A^+ = V_D^+ = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_A^+ = V_D^+ = 3.0V$ ALE, Pin 22		**0.7** **0.6**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 3.3V$	0.005	**1.0** **2.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0** **−2.0**	μA (max)
C_{IN}	D0–D15 Input Capacitance		6		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_A^+ = V_D^+ = 3.0V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **2.85**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_A^+ = V_D^+ = 3.0V$ $I_{OUT} = 1.6$ mA $I_{OUT} = 10\ \mu A$		**0.4** **0.1**	V (max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$ $V_{OUT} = 3.3V$	−0.01 0.01	**−3.0** **3.0**	μA (max) μA (max)

Digital Timing Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $t_r = t_f = 3$ ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8)

Symbol (See *Figures 8a, 8b,* and *8c*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
1, 3	$\overline{CS}$ or Address Valid to ALE Low Set-Up Time			**40**	ns (min)
2, 4	$\overline{CS}$ or Address Valid to ALE Low Hold Time			**20**	ns (min)
5	ALE Pulse Width			**45**	ns (min)
6	$\overline{RD}$ High to Next ALE High			**35**	ns (min)
7	ALE Low to $\overline{RD}$ Low			**20**	ns (min)
8	$\overline{RD}$ Pulse Width			**100**	ns (min)
9	$\overline{RD}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**100**	ns (min)
10	ALE Low to $\overline{WR}$ Low			**20**	ns (min)
11	$\overline{WR}$ Pulse Width			**60**	ns (min)
12	$\overline{WR}$ High to Next ALE High			**75**	ns (min)
13	$\overline{WR}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**140**	ns (min)
14	Data Valid to $\overline{WR}$ High Set-Up Time			**40**	ns (min)
15	Data Valid to $\overline{WR}$ High Hold Time			**30**	ns (min)
16	$\overline{RD}$ Low to Data Bus Out of TRI-STATE		30	**10** **70**	ns (min) ns (max)
17	$\overline{RD}$ High to TRI-STATE	$R_L = 1\ k\Omega$	30	**10** **110**	ns (min) ns (max)
18	$\overline{RD}$ Low to Data Valid (Access Time)		30	**10** **95**	ns (min) ns (max)

Digital Timing Characteristics

The following specifications apply to the LM12L454 and LM12L458 for $V_A^+ = V_D^+ = 3.3V$, $t_r = t_f = 3$ ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7, and 8) (Continued)

Symbol (See *Figures 8a, 8b,* and *8c*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Unit (Limit)
20	Address Valid or $\overline{CS}$ Low to $\overline{RD}$ Low			**20**	ns (min)
21	Address Valid or $\overline{CS}$ Low to $\overline{WR}$ Low			**20**	ns (min)
19	Address Invalid from $\overline{RD}$ or $\overline{WR}$ High			**10**	ns (min)
22	$\overline{INT}$ High from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)
23	DMARQ Low from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

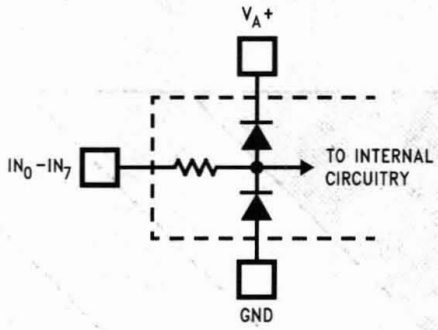
Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > (V_A^+$ or $V_D^+)$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$, and the typical thermal resistance (Θ_{JA}) of the LM12L454 and LM12L458 in the V package, when board mounted, is 47°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to each analog input through a series resistor, as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage the LM12L454 or the LM12L458. However, errors in the A/D conversion can occur if these diodes are forward biased by more than 100 mV. As an example, if V_A^+ is 3.0 V_{DC}, full-scale input voltage must be ≤3.1 V_{DC} to ensure accurate conversions.



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Note 7: V_A^+ and V_D^+ must be connected together to the same power supply voltage and bypassed with separate capacitors at each V^+ pin to assure conversion/comparison accuracy.

Note 8: Accuracy is guaranteed when operating at $f_{CLK} = 6$ MHz.

Note 9: With the test condition for $V_{REF} = V_{REF+} - V_{REF-}$ given as +2.5V, the 12-bit LSB is 305 μV and the 8-bit/"Watchdog" LSB is 4.88 mV.

Note 10: Typicals are at $T_A = 25°C$ and represent most likely parametric norm.

Note 11: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error the straight line passes through negative full-scale and zero. (See *Figures 5b* and *5c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between −1 to 0 and 0 to +1 (see *Figure 6*).

Note 14: The DC common-mode error is measured with both inputs shorted together and driven from 0V to 2.5V. The measured value is referred to the resulting output value when the inputs are driven with a 1.25V signal.

Note 15: Power Supply Sensitivity is measured after Auto-Zero and/or Auto-Calibration cycle has been completed with V_A^+ and V_D^+ at the specified extremes.

Note 16: V_{REFCM} (Reference Voltage Common Mode Range) is defined as $(V_{REF+} + V_{REF-})/2$.

Note 17: The LM12L454/8's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.10 LSB.

Note 18: The Throughput Rate is for a single instruction repeated continuously. Sequencer states 0 (1 clock cycle), 1 (1 clock cycle), 7 (9 clock cycles) and 5 (44 clock cycles) are used (see *Figure 11*). One additional clock cycle is used to read the conversion result stored in the FIFO, for a total of 56 clock cycles per conversion. The Throughput Rate is f_{CLK} (MHz)/N, where N is the number of clock cycles/conversion.

Electrical Characteristics

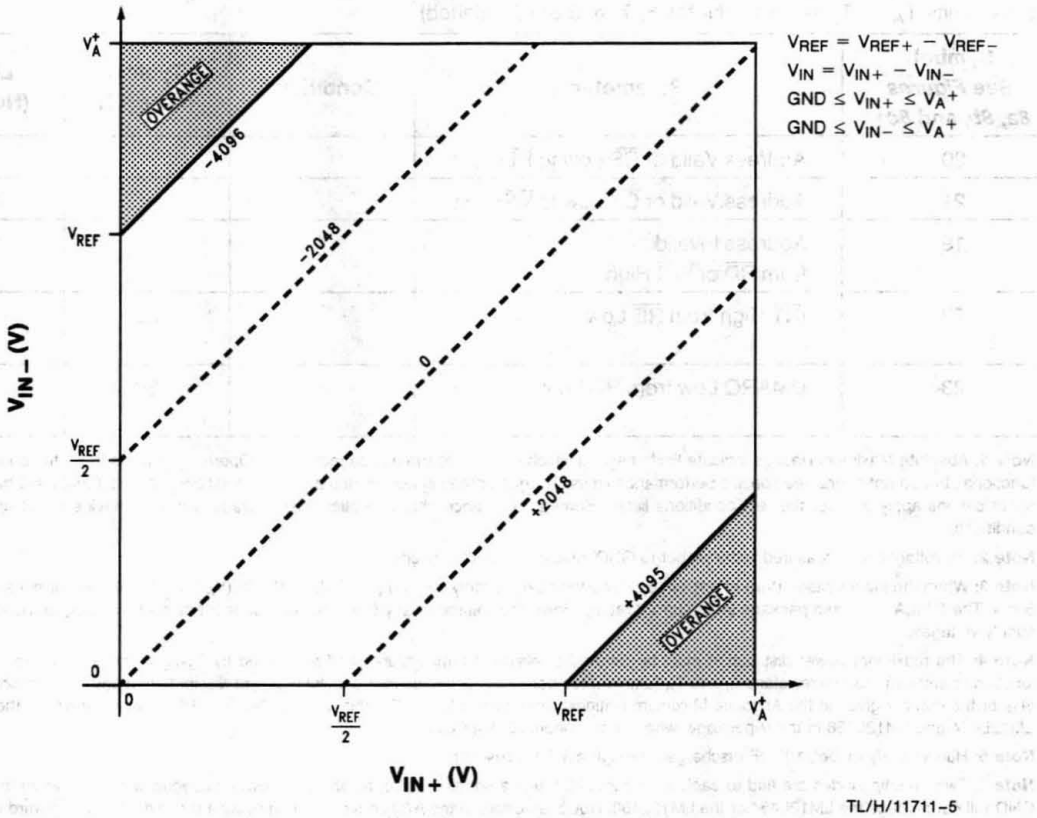

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FIGURE 1. The General Case of Output Digital Code vs the Operating Input Voltage Range

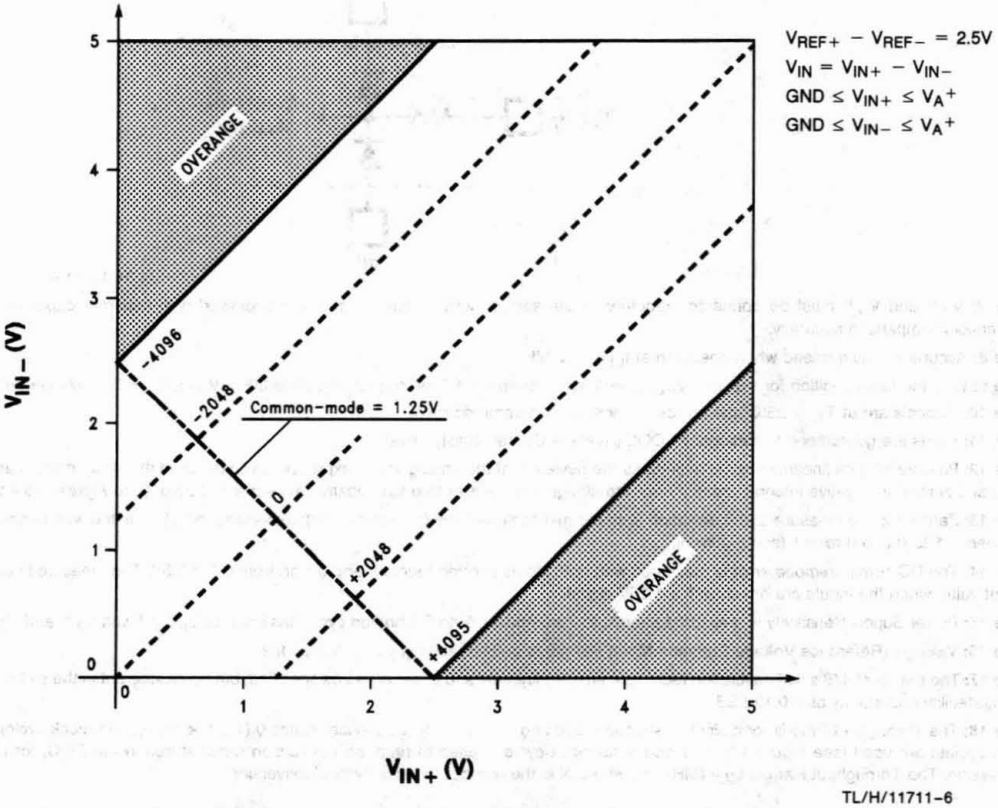

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FIGURE 2. Specific Case of Output Digital Code vs the Operating Input Voltage Range for $V_{REF} = 2.5V$

Electrical Characteristics (Continued)

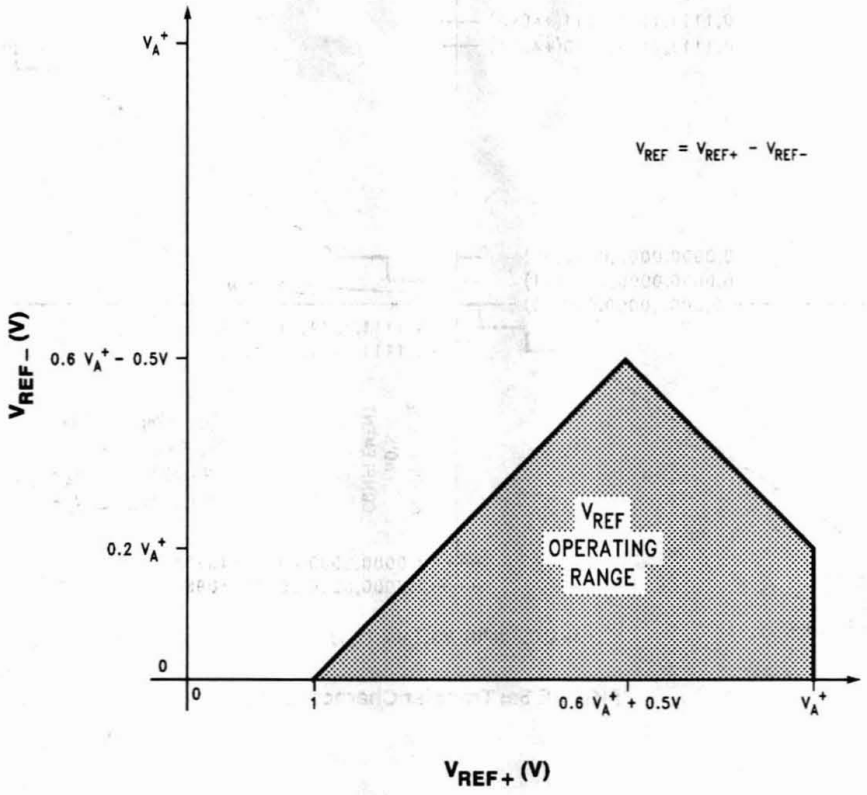

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FIGURE 3. The General Case of the V_{REF} Operating Range

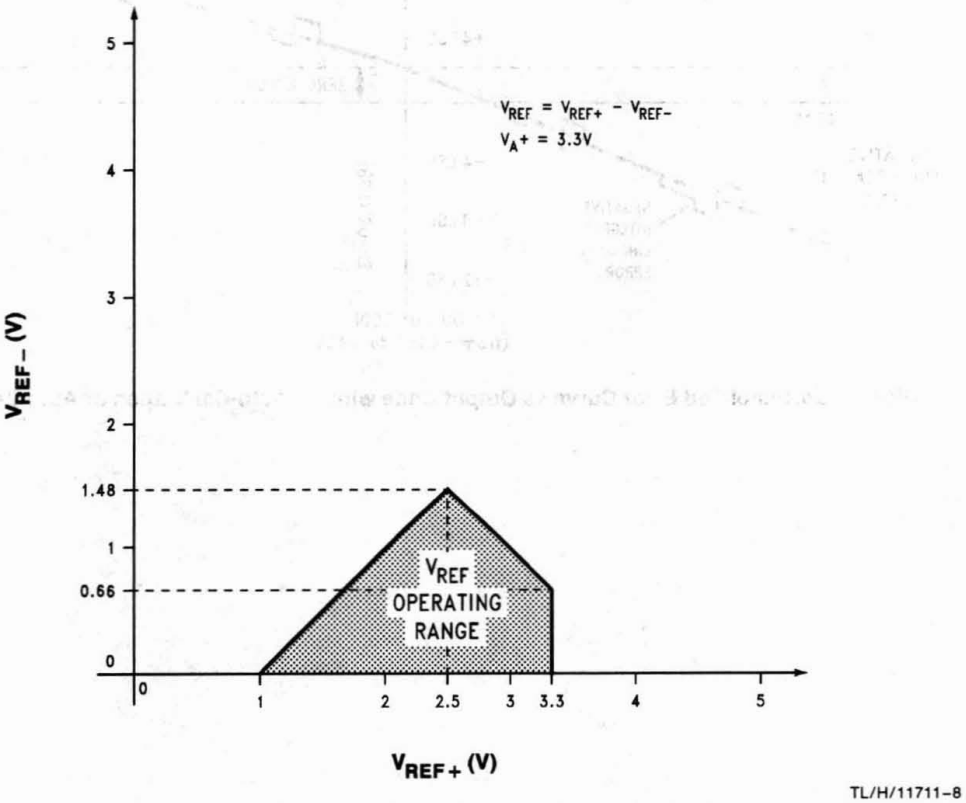

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FIGURE 4. The Specific Case of the V_{REF} Operating Range for $V_A^+ = 3.3V$

Electrical Characteristics (Continued)

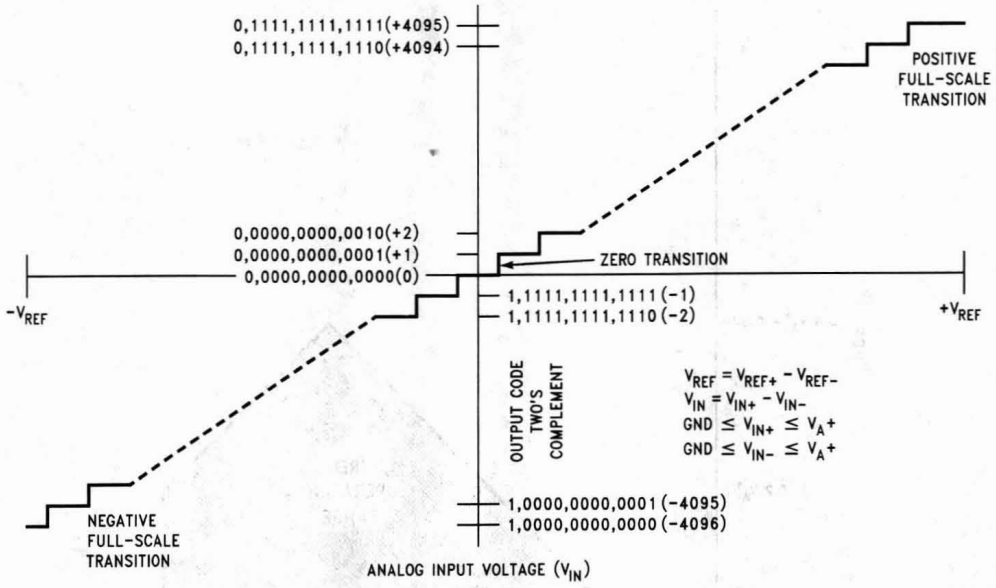

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FIGURE 5a. Transfer Characteristic

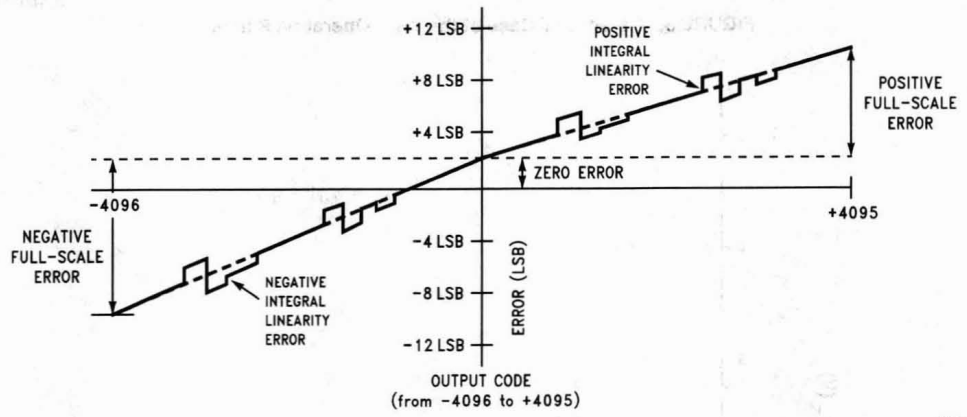

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FIGURE 5b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

Electrical Characteristics (Continued)

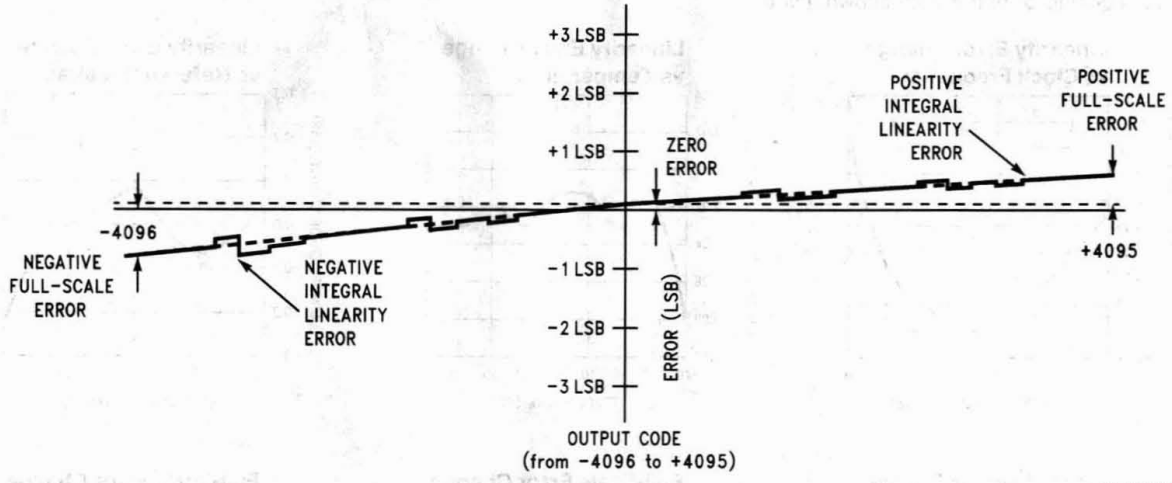

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FIGURE 5c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

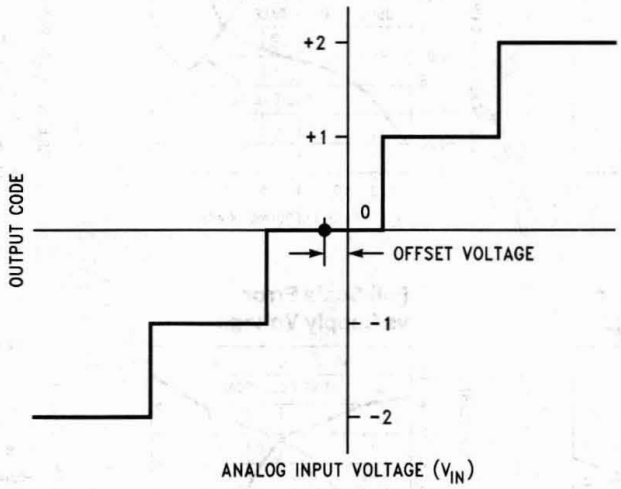

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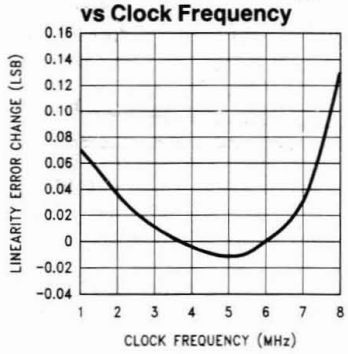
FIGURE 6. Offset or Zero Error Voltage

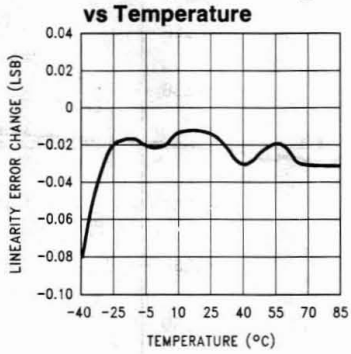
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration with $V_A^+ = V_D^+ = 3.3V$, $V_{REF+} = 2.5V$, $V_{REF-} = 0V$, $T_A = 25°C$, and $f_{CLK} = 6$ MHz unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9)

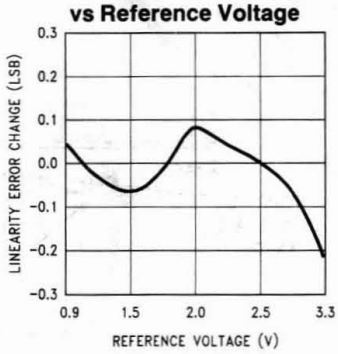
Linearity Error Change vs Clock Frequency



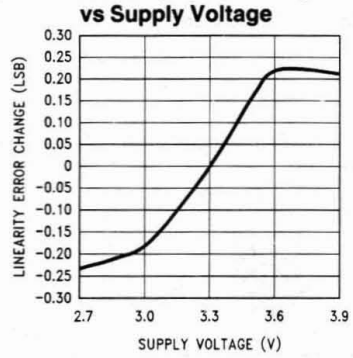
Linearity Error Change vs Temperature



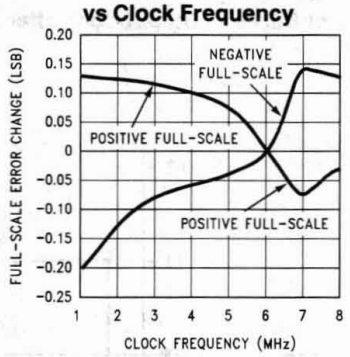
Linearity Error Change vs Reference Voltage



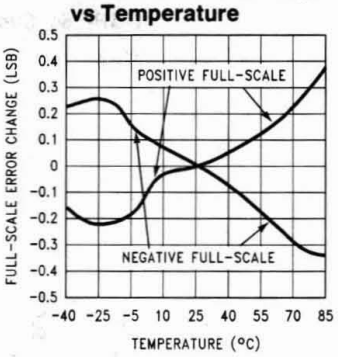
Linearity Error Change vs Supply Voltage



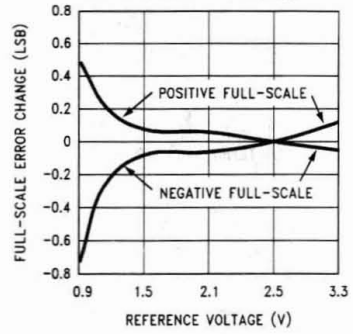
Full-Scale Error Change vs Clock Frequency



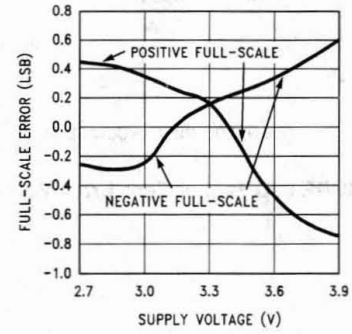
Full-Scale Error Change vs Temperature



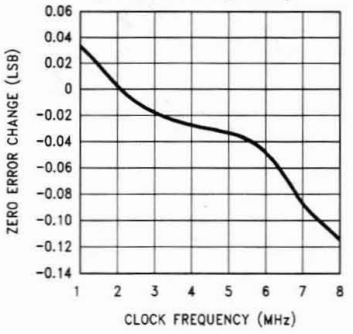
Full-Scale Error Change vs Reference Voltage



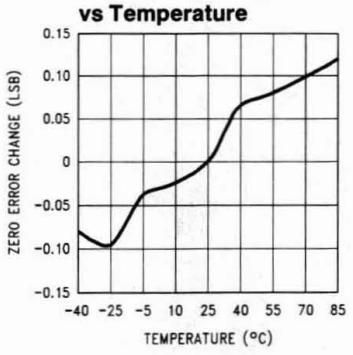
Full-Scale Error vs Supply Voltage



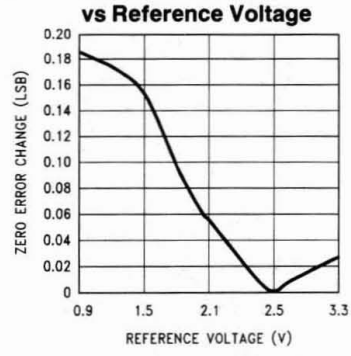
Zero Error Change vs Clock Frequency



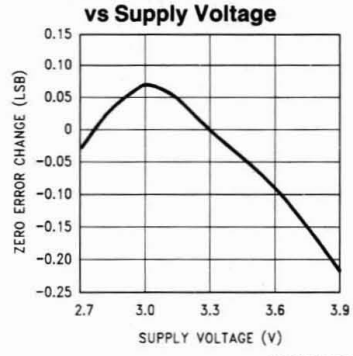
Zero Error Change vs Temperature



Zero Error Change vs Reference Voltage



Zero Error Change vs Supply Voltage



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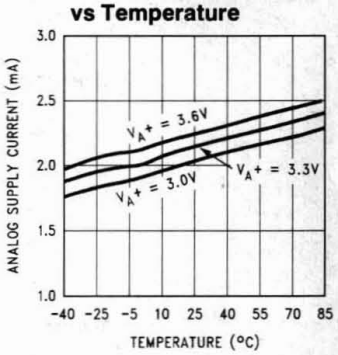
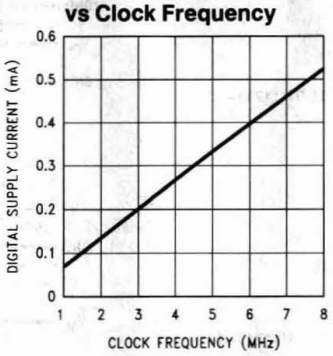
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Note 9) (Continued)

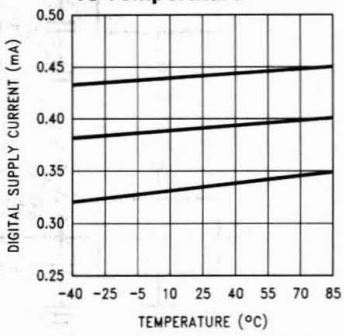
Analog Supply Current vs Temperature



Digital Supply Current vs Clock Frequency



Digital Supply Current vs Temperature



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Test Circuits and Waveforms

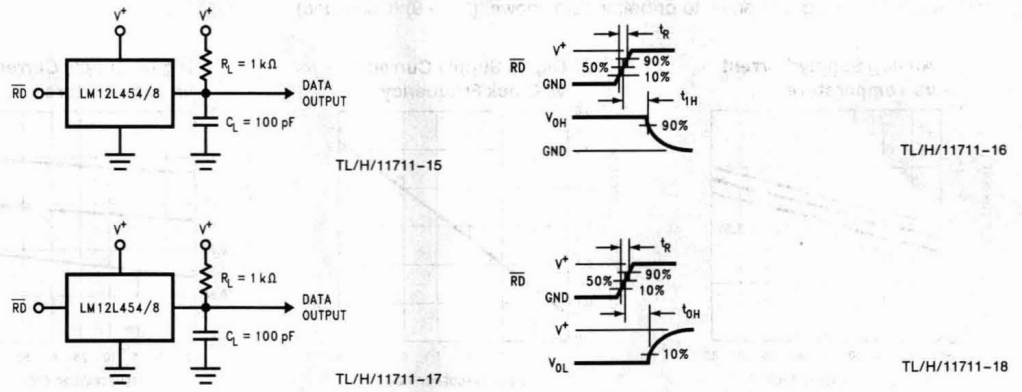

FIGURE 7. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

$V_A^+ = V_D^+ = +3.3V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

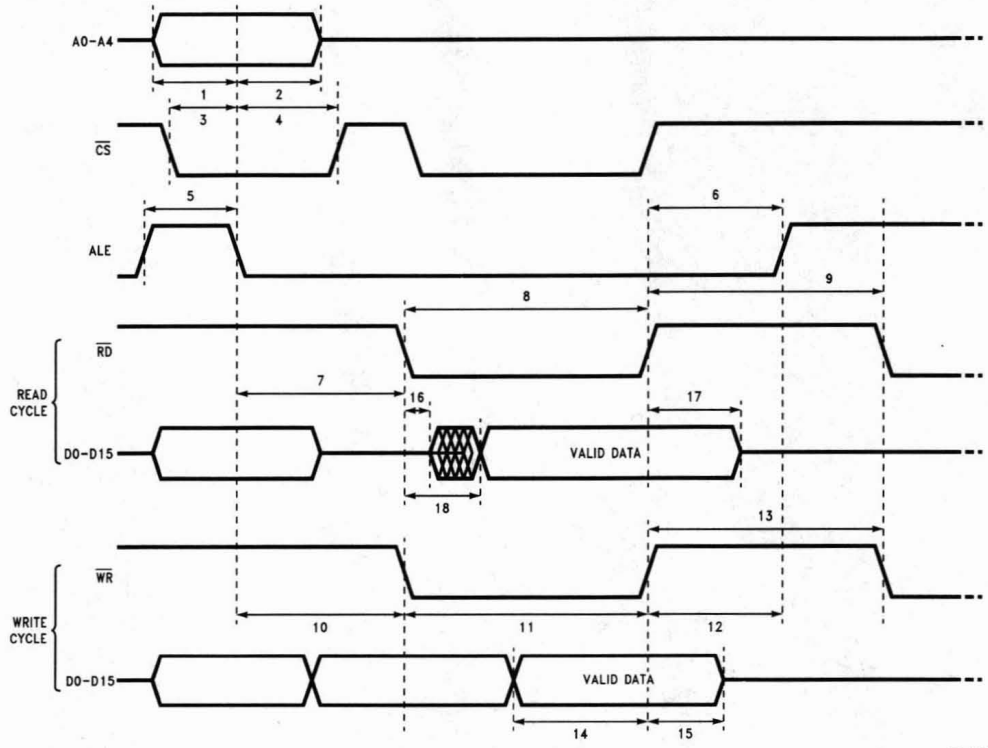

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FIGURE 8a. Multiplexed Data Bus

1, 3: $\overline{CS}$ or Address valid to ALE low set-up time.
2, 4: $\overline{CS}$ or Address valid to ALE low hold time.
5: ALE pulse width
6: $\overline{RD}$ high to next ALE high
7: ALE low to $\overline{RD}$ low
8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
10: ALE low to $\overline{WR}$ low
11: $\overline{WR}$ pulse width
12: $\overline{WR}$ high to next ALE high
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)

Timing Diagrams

$V_A^+ = V_D^+ = +3.3V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs. (Continued)

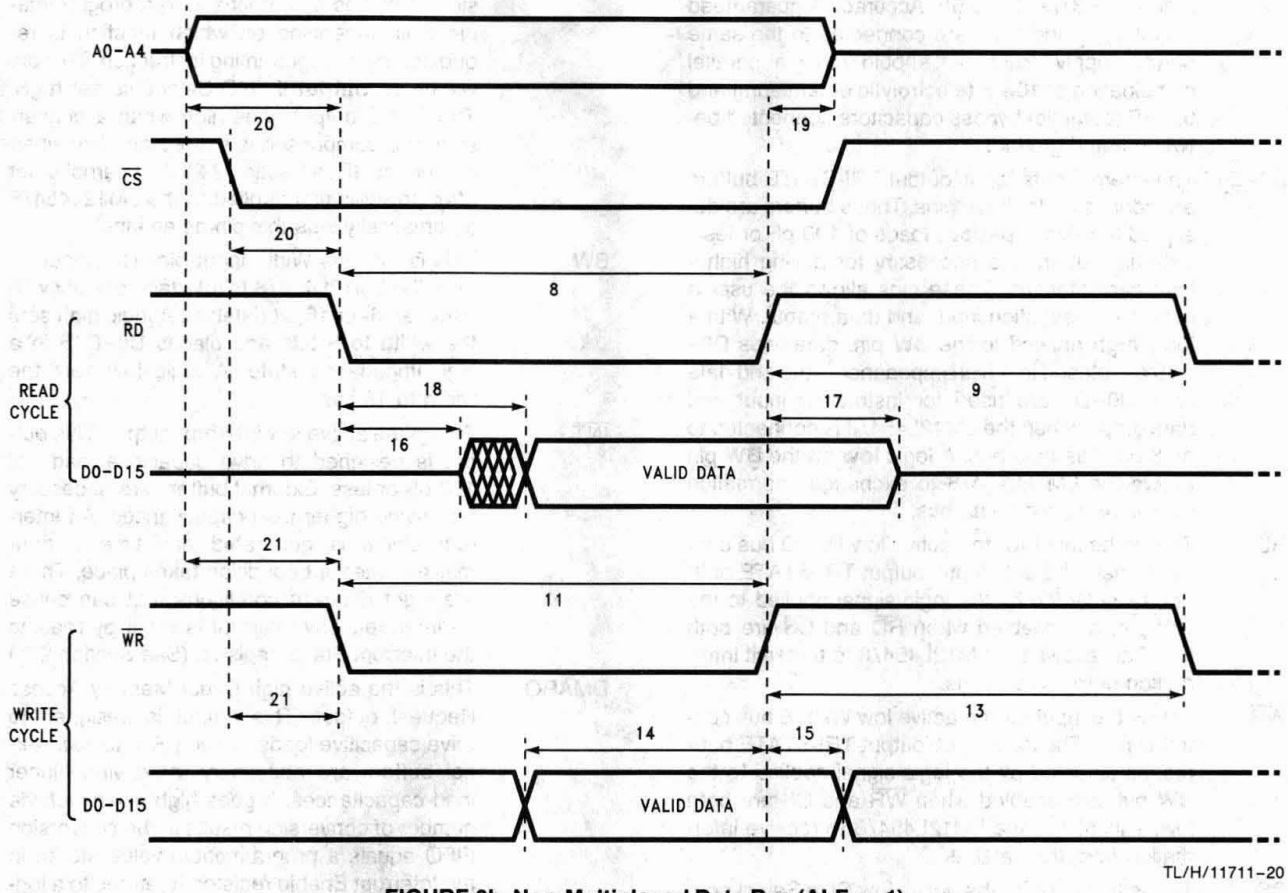

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FIGURE 8b. Non-Multiplexed Data Bus (ALE = 1)

8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
11: $\overline{WR}$ pulse width
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)
19: Address invalid from $\overline{RD}$ or $\overline{WR}$ high (hold time)
20: $\overline{CS}$ low or address valid to $\overline{RD}$ low
21: $\overline{CS}$ low or address valid to $\overline{WR}$ low

$V_A^+ = V_D^+ = +3.3V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

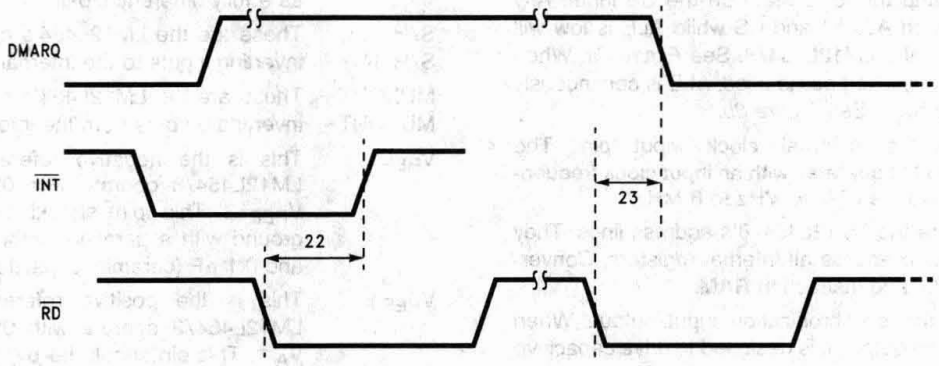

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FIGURE 8c. Interrupt and DMARQ

22: $\overline{INT}$ high from $\overline{RD}$ low
23: DMARQ low from $\overline{RD}$ low

Pin Description

V_A^+ V_D^+ These are the analog and digital supply voltage pins. The LM12L454/8's supply voltage operating range is +3.0V to +5.5V. Accuracy is guaranteed only if V_A^+ and V_D^+ are connected to the same power supply. Each pin should have a parallel combination of 10 μF (electrolytic or tantalum) and 0.1 μF (ceramic) bypass capacitors connected between it and ground.

D0–D15 The internal data input/output TRI-STATE buffers are connected to these pins. These buffers are designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. These pins allows the user a means of instruction input and data output. With a logic **high** applied to the **BW** pin, data lines D8–D15 are placed in a high impedance state and data lines D0–D7 are used for instruction input and data output when the LM12L454/8 is connected to an 8-bit wide data bus. A logic **low** on the **BW** pin allows the LM12L454/8 to exchange information over a 16-bit wide data bus.

$\overline{RD}$ This is the input for the active low READ bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{RD}$ and $\overline{CS}$ are both low. This allows the LM12L454/8 to transmit information onto the databus.

$\overline{WR}$ This is the input for the active low WRITE bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{WR}$ and $\overline{CS}$ are both low. This allows the LM12L454/8 to receive information from the databus.

$\overline{CS}$ This is the input for the active low Chip Select control signal. A logic low should be applied to this pin only during a READ or WRITE access to the LM12L454/8. The internal clocking is halted and conversion stops while Chip Select is low. Conversion resumes when the Chip Select input signal returns high.

ALE This is the Address Latch Enable input. It is used in systems containing a multiplexed databus. When ALE is asserted **high**, the LM12L454/8 accepts information on the databus as a valid address. A high-to-low transition will latch the address data on A0–A4 and the logic state on the $\overline{CS}$ input. Any changes on A0–A4 and $\overline{CS}$ while ALE is low will not affect the LM12L454/8. See *Figure 8a*. When a non-multiplexed bus is used, ALE is continuously asserted **high**. See *Figure 8b*.

CLK This is the external clock input pin. The LM12L454/8 operates with an input clock frequency in the range of 0.05 MHz to 8 MHz.

A0–A4 These are the LM12L454/8's address lines. They are used to access all internal registers, Conversion FIFO, and Instruction **RAM**.

SYNC This is the synchronization input/output. When used as an output, it is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. SYNC is an **input** if the Configuration register's "I/O Select" bit is **low**. A rising edge on this pin causes the internal S/H to hold the input signal. The next rising clock edge either starts a conversion or makes a comparison to a programmable limit depending on which function is requested by a programming instruction. This pin will be an **output** if "I/O Select" is set **high**. The SYNC output goes high when a conversion or a comparison is started and low when completed. (See Section 2.2). An internal reset after power is first applied to the LM12L454/8 automatically sets this pin as an input.

BW This is the Bus Width input pin. This input allows the LM12L454/8 to interface directly with either an 8- or 16-bit databus. A logic high sets the width to 8 bits and places D8–D15 in a high impedance state. A logic low sets the width to 16 bits.

$\overline{INT}$ This is the active low interrupt output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. An interrupt signal is generated any time a non-masked interrupt condition takes place. There are eight different conditions that can cause an interrupt. Any interrupt is reset by reading the Interrupt Status register. (See Section 2.3.)

DMARQ This is the active high Direct Memory Access Request output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. It goes high whenever the number of conversion results in the conversion FIFO equals a programmable value stored in the Interrupt Enable register. It returns to a logic low when the FIFO is empty.

GND This is the LM12L454/8 ground connection. It should be connected to a low resistance and inductance analog ground return that connects directly to the system power supply ground.

IN0–IN7 (IN0–IN3 LM12L454) These are the eight (LM12L458) or four (LM12L454) analog inputs. A given channel is selected through the instruction RAM. Any of the channels can be configured as an independent single-ended input. Any pair of channels, whether adjacent or non-adjacent, can operate as a fully differential pair.

S/H IN+ S/H IN− These are the LM12L454's non-inverting and inverting inputs to the internal S/H.

MUXOUT+ MUXOUT− These are the LM12L454's non-inverting and inverting outputs from the internal multiplexer.

V_{REF-} This is the negative reference input. The LM12L454/8 operate with $0V \leq V_{REF-} \leq V_{REF+}$. This pin should be bypassed to ground with a parallel combination of 10 μF and 0.1 μF (ceramic) capacitors.

V_{REF+} This is the positive reference input. The LM12L454/8 operate with $0V \leq V_{REF+} \leq V_A^+$. This pin should be bypassed to ground with a parallel combination of 10 μF and 0.1 μF (ceramic) capacitors.

N.C. This is a no connect pin.

Application Information

1.0 Functional Description

The LM12L454 and LM12L458 are multi-functional Data Acquisition Systems that include a fully differential 12-bit-plus-sign self-calibrating analog-to-digital converter (ADC) with a two's-complement output format, an 8-channel (LM12L458) or a 4-channel (LM12L454) analog multiplexer, a first-in-first-out (FIFO) register that can store 32 conversion results, and an Instruction RAM that can store as many as eight instructions to be sequentially executed. The LM12L454 also has a differential multiplexer output and a differential S/H input. All of this circuitry operates on only a single +3.3V power supply.

The LM12L454/8 have three modes of operation:

12-bit + sign with correction
8-bit + sign without correction
8-bit + sign comparison mode ("watchdog" mode)

The fully differential 12-bit-plus-sign ADC uses a charge re-distribution topology that includes calibration capabilities. Charge re-distribution ADCs use a capacitor ladder in place of a resistor ladder to form an internal DAC. The DAC is used by a successive approximation register to generate intermediate voltages between the voltages applied to V_{REF-} and V_{REF+}. These intermediate voltages are compared against the sampled analog input voltage as each bit is generated. The number of intermediate voltages and comparisons equals the ADC's resolution. The correction of each bit's accuracy is accomplished by calibrating the capacitor ladder used in the ADC.

Two different calibration modes are available; one compensates for offset voltage, or zero error, while the other corrects both offset error and the ADC's linearity error.

When correcting offset only, the offset error is measured once and a correction coefficient is created. During the full calibration, the offset error is measured eight times, averaged, and a correction coefficient is created. After completion of either calibration mode, the offset correction coefficient is stored in an internal offset correction register.

The LM12L454/8's overall linearity correction is achieved by correcting the internal DAC's capacitor mismatch. Each capacitor is compared eight times against all remaining smaller value capacitors and any errors are averaged. A correction coefficient is then created and stored in one of the thirteen internal linearity correction registers. An internal state machine, using patterns stored in an internal 16 x 8-bit ROM, executes each calibration algorithm.

Once calibrated, an internal arithmetic logic unit (ALU) uses the offset correction coefficient and the 13 linearity correction coefficients to reduce the conversion's offset error and linearity error, in the background, during the 12-bit + sign conversion. The 8-bit + sign conversion and comparison modes use only the offset coefficient. The 8-bit + sign mode performs a conversion in less than half the time used by the 12-bit + sign conversion mode.

The LM12L454/8's "watchdog" mode is used to monitor a single-ended or differential signal's amplitude. Each sampled signal has two limits. An interrupt can be generated if the input signal is above or below either of the two limits. This allows interrupts to be generated when analog voltage inputs are "inside the window" or, alternatively, "outside the window". After a "watchdog" mode interrupt, the processor can then request a conversion on the input signal and read the signal's magnitude.

The analog input multiplexer can be configured for any combination of single-ended or fully differential operation. Each input is referenced to ground when a multiplexer channel operates in the single-ended mode. Fully differential analog input channels are formed by pairing any two channels together.

The LM12L454's multiplexer outputs and S/H inputs (MUXOUT+, MUXOUT− and S/H IN+, S/H IN−) provide the option for additional analog signal processing. Fixed-gain amplifiers, programmable-gain amplifiers, filters, and other processing circuits can operate on the signal applied to the selected multiplexer channel(s). If external processing is not used, connect MUXOUT+ to S/H IN+ and MUXOUT− to S/H IN−.

The LM12L454/8's internal S/H is designed to operate at its minimum acquisition time (1.5 μs, 12 bits) when the source impedance, R_S, is $\leq 80\Omega$ ($f_{CLK} \leq 6$ MHz). When $80\Omega < R_S \leq 5.56\ k\Omega$, the internal S/H's acquisition time can be increased to a maximum of 6.5 μs (12 bits, $f_{CLK} =$ 6 MHz). See Section 2.1 (Instruction RAM "00") Bits 12–15 for more information.

Microprocessor overhead is reduced through the use of the internal conversion FIFO. Thirty-two consecutive conversions can be completed and stored in the FIFO without any microprocessor intervention. The microprocessor can, at any time, interrogate the FIFO and retrieve its contents. It can also wait for the LM12L454/8 to issue an interrupt when the FIFO is full or after any number ($\leq$32) of conversions have been stored.

Conversion sequencing, internal timer interval, multiplexer configuration, and many other operations are programmed and set in the Instruction RAM.

A diagnostic mode is available that allows verification of the LM12L458's operation. The diagnostic mode is disabled in the LM12L454. This mode internally connects the voltages present at the V_{REF+}, V_{REF-}, and GND pins to the internal V_{IN+} and V_{IN-} S/H inputs. This mode is activated by setting the Diagnostic bit (Bit 11) in the Configuration register to a "1". More information concerning this mode of operation can be found in Section 2.2.

2.0 Internal User-Programmable Registers

2.1 INSTRUCTION RAM

The instruction RAM holds up to eight sequentially executable instructions. Each 48-bit long instruction is divided into three 16-bit sections. READ and WRITE operations can be issued to each 16-bit section using the instruction's address and the 2-bit "RAM pointer" in the Configuration register. The eight instructions are located at addresses 0000 through 0111 (A4–A1, BW = 0) when using a 16-bit wide data bus or at addresses 00000 through 01111 (A4–A0, BW = 1) when using an 8-bit wide data bus. They can be accessed and programmed in random order.

Any Instruction RAM READ or WRITE can affect the sequencer's operation:

The Sequencer should be stopped by setting the RESET bit to a "1" or by resetting the START bit in the Configuration Register and waiting for the current instruction to finish execution before any Instruction RAM READ or WRITE is initiated.

A soft RESET should be issued by writing a "1" to the Configuration Register's RESET bit after any READ or WRITE to the Instruction RAM.

The three sections in the Instruction RAM are selected by the Configuration Register's 2-bit "RAM Pointer", bits D8 and D9. The first 16-bit Instruction RAM section is selected with the RAM Pointer equal to "00". This section provides multiplexer channel selection, as well as resolution, acquisition time, etc. The second 16-bit section holds "watchdog" limit #1, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit. The third 16-bit section holds "watchdog" limit #2, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit.

Instruction RAM "00"

Bit 0 is the LOOP bit. It indicates the last instruction to be executed in any instruction sequence when it is set to a "1". The next instruction to be executed will be instruction 0.

Bit 1 is the PAUSE bit. This controls the Sequencer's operation. When the PAUSE bit is set ("1"), the Sequencer will stop after reading the current instruction, but before executing it and the start bit, in the Configuration register, is automatically reset to a "0". Setting the PAUSE also causes an interrupt to be issued. The Sequencer is restarted by placing a "1" in the Configuration register's Bit 0 (Start bit).

After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer retrieves Instruction 000, decodes it, and waits for a "1" to be placed in the Configuration's START bit. The START bit value of "0" "overrides" the action of Instruction 000's PAUSE bit when the Sequencer is started. Once started, the Sequencer executes Instruction 000 and retrieves, decodes, and executes each of the remaining instructions. No PAUSE Interrupt (INT 5) is generated the first time the Sequencer executes Instruction 000 having a PAUSE bit set to "1". When the Sequencer encounters a LOOP bit or completes all eight instructions, Instruction 000 is retrieved and decoded. A set PAUSE bit in Instruction 000 now halts the Sequencer before the instruction is executed.

Bits 2–4 select which of the eight input channels ("000" to "111" for IN0–IN7) will be configured as non-inverting inputs to the LM12L458's ADC. (See Page 22, Table I.) They select which of the four input channels ("000" to "011" for IN0–IN4) will be configured as non-inverting inputs to the LM12L454's ADC. (See Page 22, Table II.)

Bits 5–7 select which of the seven input channels ("001" to "111" for IN1 to IN7) will be configured as inverting inputs to the LM12L458's ADC. (See Page 22, Table I.) They select which of the three input channels ("001" to "011" for IN1–IN4) will be configured as inverting inputs to the LM12L454's ADC. (See Page 22, Table II.) Fully differential operation is created by selecting two multiplexer channels, one operating in the non-inverting mode and the other operating in the inverting mode. A code of "000" selects ground as the inverting input for single ended operation.

Bit 8 is the SYNC bit. Setting Bit 8 to "1" causes the Sequencer to suspend operation at the end of the internal S/H's acquisition cycle and to wait until a rising edge appears at the SYNC pin. When a rising edge appears, the S/H acquires the input signal magnitude and the ADC performs a conversion on the clock's next rising edge. When the SYNC pin is used as an input, the Configuration register's "I/O Select" bit (Bit 7) must be set to a "0". With SYNC configured as an input, it is possible to synchronize the start of a conversion to an external event. This is useful in applications such as digital signal processing (DSP) where the exact timing of conversions is important.

When the LM12L454/8 are used in the "watchdog" mode with external synchronization, two rising edges on the SYNC input are required to initiate two comparisons. The first rising edge initiates the comparison of the selected analog input signal with Limit #1 (found in Instruction RAM "01") and the second rising edge initiates the comparison of the same analog input signal with Limit #2 (found in Instruction RAM "10").

Bit 9 is the TIMER bit. When Bit 9 is set to "1", the Sequencer will halt until the internal 16-bit Timer counts down to zero. During this time interval, no "watchdog" comparisons or analog-to-digital conversions will be performed.

Bit 10 selects the ADC conversion resolution. Setting Bit 10 to "1" selects 8-bit + sign and when reset to "0" selects 12-bit + sign.

Bit 11 is the "watchdog" comparison mode enable bit. When operating in the "watchdog" comparison mode, the selected analog input signal is compared with the programmable values stored in Limit #1 and Limit #2 (see Instruction RAM "01" and Instruction RAM "10"). Setting Bit 11 to "1" causes two comparisons of the selected analog input signal with the two stored limits. When Bit 11 is reset to "0", an 8-bit + sign or 12-bit + sign (depending on the state of Bit 10 of Instruction RAM "00") conversion of the input signal can take place.

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	Purpose	Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 00)	R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync	V_{IN-} (MUXOUT−)*			V_{IN+} (MUXOUT+)*			Pause	Loop
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 01)	R/W	Don't Care						>/<	Sign	Limit #1							
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 10)	R/W	Don't Care						>/<	Sign	Limit #2							
1	0	0	0	Configuration Register	R/W	Don't Care				DIAG†	Test = 0	RAM Pointer		I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full CAL	Auto-Zero	Reset	Start
1	0	0	1	Interrupt Enable Register	R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1			INT7	Don't Care	INT5	INT4	INT3	INT2	INT1	INT0
1	0	1	0	Interrupt Status Register	R	Actual Number of Conversion Results in Conversion FIFO					Address of Sequencer Instruction being Executed			INST7	"0"	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	1	Timer Register	R/W	Timer Preset High Byte								Timer Preset Low Byte							
1	1	0	0	Conversion FIFO	R	Address or Sign			Sign	Conversion Data: MSBs				Conversion Data: LSBs							
1	1	0	1	Limit Status Register	R	Limit #2: Status								Limit #1: Status							

*LM12L454 (Refer to Table II).
†LM12L458 only. Must be set to "0" for the LM12L454.

FIGURE 9. LM12L454/8 Memory Map for 16-Bit Wide Databus (BW = "0", Test Bit = "0" and A0 = Don't Care)

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	A0	Purpose	Type	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 00)	R/W	V_{IN-} (MUXOUT−)*			V_{IN+} (MUXOUT+)*			Pause	Loop
0	0 to 1	0 to 1	0 to 1	1		R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 01)	R/W	Comparison Limit #1							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						>/<	Sign
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 10)	R/W	Comparison Limit #2							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						>/<	Sign
1	0	0	0	0	Configuration Register	R/W	I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full Cal	Auto-Zero	Reset	Start
1	0	0	0	1		R/W	Don't Care				DIAG†	Test = 0	RAM Pointer	
1	0	0	1	0	Interrupt Enable Register	R/W	INT7	Don't Care	INT5	INT4	INT3	INT2	INT1	INT0
1	0	0	1	1		R/W	Number of Conversions in Conversion FIFO to Generate INT2						Sequencer Address to Generate INT1	
1	0	1	0	0	Interrupt Status Register	R	INST7	"0"	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	0	1		R	Actual Number of Conversions Results in Conversion FIFO						Address of Sequencer Instruction being Executed	
1	0	1	1	0	Timer Register	R/W	Timer Preset: Low Byte							
1	0	1	1	1		R/W	Timer Preset: High Byte							
1	1	0	0	0	Conversion FIFO	R	Conversion Data: LSBs							
1	1	0	0	1		R	Address or Sign			Sign	Conversion Data: MSBs			
1	1	0	1	0	Limit Status Register	R	Limit #1 Status							
1	1	0	1	1		R	Limit #2 Status							

*LM12L454 (Refer to Table II).

†LM12L458 only. Must be set to "0" for the LM12L454.

FIGURE 10. LM12L454/8 Memory Map for 8-Bit Wide Databus (BW = "1" and Test Bit = "0")

2.0 Internal User-Programmable Registers (Continued)

Bits 12–15 are used to store the user-programmable acquisition time. The Sequencer keeps the internal S/H in the acquisition mode for a fixed number of clock cycles (nine clock cycles, for 12-bit + sign conversions and two clock cycles for 8-bit + sign conversions or "watchdog" comparisons) plus a variable number of clock cycles equal to twice the value stored in Bits 12–15. Thus, the S/H's acquisition time is (9 + 2D) clock cycles for 12-bit + sign conversions and (2 + 2D) clock cycles for 8-bit + sign conversions or "watchdog" comparisons, where D is the value stored in Bits 12–15. The minimum acquisition time compensates for the typical internal multiplexer series resistance of 2 kΩ, and any additional delay created by Bits 12–15 compensates for source resistances greater than 80Ω. (For this acquisition time discussion, numbers in ( ) are shown for the LM12L454/8 operating at 6 MHz. The necessary acquisition time is determined by the source impedance at the multiplexer input. If the source resistance (R_S) < 80Ω and the clock frequency is 6 MHz, the value stored in bits 12–15 (D) can be 0000. If R_S > 80Ω, the following equations determine the value that should be stored in bits 12–15.

$$D = 0.45 \times R_S \times f_{CLK}$$

for 12-bits + sign

$$D = 0.36 \times R_S \times f_{CLK}$$

for 8-bits + sign and "watchdog"

R_S is in kΩ and f_{CLK} is in MHz. Round the result to the next higher integer value. If D is greater than 15, it is advisable to lower the source impedance by using an analog buffer between the signal source and the LM12L458's multiplexer inputs. The value of D can also be used to compensate for the settling or response time of external processing circuits connected between the LM12L454's MUXOUT and S/H IN pins.

Instruction RAM "01"

The second Instruction RAM section is selected by placing a "01" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #1**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12L454/8 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first, followed by a comparison of the same sampled analog input signal with the value found in limit #2 (Instruction RAM "10").

Bit 8 holds limit #1's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #1 to generate an interrupt, while a "0" causes a voltage less than limit #1 to generate an interrupt.

Bits 10–15 are not used.

Instruction RAM "10"

The third Instruction RAM section is selected by placing a "10" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #2**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12L454/8 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first (Instruction RAM "01"), followed by a comparison of the same sampled analog input signal with the value found in limit #2.

Bit 8 holds limit #2's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #2 to generate an interrupt, while a "0" causes a voltage less than limit #2 to generate an interrupt.

Bits 10–15 are not used.

2.2 CONFIGURATION REGISTER

The Configuration register, 1000 (A4–A1, BW = 0) or 1000x (A4–A0, BW = 1) is a 16-bit control register with read/write capability. It acts as the LM12L454's and LM12L458's "control panel" holding global information as well as start/stop, reset, self-calibration, and stand-by commands.

Bit 0 is the START/STOP bit. Reading Bit 0 returns an indication of the Sequencer's status. A "0" indicates that the Sequencer is stopped and waiting to execute the next instruction. A "1" shows that the Sequencer is running. Writing a "0" halts the Sequencer when the current instruction has finished execution. The next instruction to be executed is pointed to by the instruction pointer found in the status register. A "1" restarts the Sequencer with the instruction currently pointed to by the instruction pointer. (See Bits 8–10 in the Interrupt Status register.)

Bit 1 is the LM12L454/8's system RESET bit. Writing a "1" to Bit 1 stops the Sequencer (resetting the Configuration register's START/STOP bit), resets the Instruction pointer to "000" (found in the Interrupt Status register), clears the Conversion FIFO, and resets all interrupt flags. The RESET bit will return to "0" after two clock cycles unless it is forced high by writing a "1" into the Configuration register's Stand-by bit. A reset signal is internally generated when power is first applied to the part. No operation should be started until the RESET bit is "0".

Writing a "1" to **Bit 2** initiates an auto-zero offset voltage calibration. Unlike the eight-sample auto-zero calibration performed during the full calibration procedure, Bit 2 initiates a "short" auto-zero by sampling the offset once and creating a correction coefficient (full calibration averages eight samples of the converter offset voltage when creating a correction coefficient). If the Sequencer is running when Bit 2 is set to "1", an auto-zero starts immediately after the conclusion of the currently running instruction. Bit 2 is reset automatically to a "0" and an interrupt flag (Bit 3, in the Interrupt Status register) is set at the end of the auto-zero (76 clock cycles). After completion of an auto-zero calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, an auto-zero is performed immediately at the time requested.

Writing a "1" to **Bit 3** initiates a complete calibration process that includes a "long" auto-zero offset voltage correction (this calibration averages eight samples of the comparator offset voltage when creating a correction coefficient) followed by an ADC linearity calibration. This complete calibration is started after the currently running instruction is completed if the Sequencer is running when Bit 3 is set to "1". Bit 3 is reset automatically to a "0" and an interrupt flag (Bit 4, in the Interrupt Status register) will be generated at the end of the calibration procedure (4944 clock cycles). After completion of a full auto-zero and linearity calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, a full calibration is performed immediately at the time requested.

2.0 Internal User-Programmable Registers (Continued)

Bit 4 is the Standby bit. Writing a "1" to Bit 4 immediately places the LM12L454/8 in Standby mode. Normal operation returns when Bit 4 is reset to a "0". The Standby command ("1") disconnects the external clock from the internal circuitry, decreases the LM12L454/8's internal analog circuitry power supply current, and preserves all internal RAM contents. After writing a "0" to the Standby bit, the LM12L454/8 returns to an operating state identical to that caused by exercising the RESET bit. A Standby completion interrupt is issued after a power-up completion delay that allows the analog circuitry to settle. The Sequencer should be restarted only after the Standby completion is issued. The Instruction RAM can still be accessed through read and write operations while the LM12L454/8 are in Standby Mode.

Bit 5 is the Channel Address Mask. If Bit 5 is set to a "1", Bits 13–15 in the conversion FIFO will be equal to the sign bit (Bit 12) of the conversion data. Resetting Bit 5 to a "0" causes conversion data Bits 13 through 15 to hold the instruction pointer value of the instruction to which the conversion data belongs.

Bit 6 is used to select a "short" auto-zero correction for every conversion. The Sequencer automatically inserts an auto-zero before every conversion or "watchdog" comparison if Bit 6 is set to "1". No automatic correction will be performed if Bit 6 is reset to "0".

The LM12L454/8's offset voltage, after calibration, has a typical drift of 0.1 LSB over a temperature range of −40°C to +85°C. This small drift is less than the variability of the change in offset that can occur when using the auto-zero correction with each conversion. This variability is the result of using only one sample of the offset voltage to create a correction value. This variability decreases when using the full calibration mode because eight samples of the offset voltage are taken, averaged, and used to create a correction value.

Bit 7 is used to program the SYNC pin (29) to operate as either an input or an output. The SYNC pin becomes an output when Bit 7 is a "1" and an input when Bit 7 is a "0". With SYNC programmed as an input, the rising edge of any logic signal applied to pin 29 will start a conversion or "watchdog" comparison. Programmed as an output, the logic level at pin 29 will go high at the start of a conversion or "watchdog" comparison and remain high until either have finished. See Instruction RAM "00", Bit 8.

Bits 8 and **9** form the RAM Pointer that is used to select each of a 48-bit instruction's three 16-bit sections during read or write actions. A "00" selects Instruction RAM section one, "01" selects section two, and "10" selects section three.

Bit 10 activates the Test mode that is used only during production testing. Leave this bit reset to "0".

Bit 11 is the Diagnostic bit and is available only in the LM12L458. It can be activated by setting it to a "1" (the Test bit must be reset to a "0"). The Diagnostic mode, along with a correctly chosen instruction, allows verification that the LM12L458's ADC is performing correctly. When activated, the inverting and non-inverting inputs are connected as shown in Table I. As an example, an instruction with "001" for both V_{IN+} and V_{IN-} while using the Diagnostic mode typically results in a full-scale output.

2.3 INTERRUPTS

The LM12L454 and LM12L458 have eight possible interrupts, all with the same priority. Any of these interrupts will cause a hardware interrupt to appear on the $\overline{INT}$ pin (31) if they are not masked (by the Interrupt Enable register). The Interrupt Status register is then read to determine which of the eight interrupts has been issued.

TABLE I. LM12L458 Input Multiplexer Channel Configuration Showing Normal Mode and Diagnostic Mode

Channel Selection Data	Normal Mode		Diagnostic Mode	
	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}
000	IN0	GND		
001	IN1	IN1	V_{REF+}	V_{REF-}
010	IN2	IN2	IN2	IN2
011	IN3	IN3	IN3	IN3
100	IN4	IN4	IN4	IN4
101	IN5	IN5	IN5	IN5
110	IN6	IN6	IN6	IN6
111	IN7	IN7	IN7	IN7

TABLE II. LM12L454 Input Multiplexer Channel Configuration

Channel Selection Data	MUX+	MUX−
000	IN0	GND
001	IN1	IN1
010	IN2	IN2
011	IN3	IN3
1XX	OPEN	OPEN

The Interrupt Status register, 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1) must be cleared by reading it after writing to the Interrupt Enable register. This removes any spurious interrupts on the $\overline{INT}$ pin generated during an Interrupt Enable register access.

Interrupt 0 is generated whenever the analog input voltage on a selected multiplexer channel crosses a limit while the LM12L454/8 are operating in the "watchdog" comparison mode. Two sequential comparisons are made when the LM12L454/8 are executing a "watchdog" instruction. Depending on the logic state of Bit 9 in the Instruction RAM's second and third sections, an interrupt will be generated either when the input signal's magnitude is greater than or less than the programmable limits. (See the Instruction RAM, Bit 9 description.) The Limit Status register will indicate which preprogrammed limit, #1 or #2 and which instruction was executing when the limit was crossed.

Interrupt 1 is generated when the Sequencer reaches the instruction counter value specified in the Interrupt Enable register's bits 8–10. This flag appears before the instruction's execution.

Interrupt 2 is activated when the Conversion FIFO holds a number of conversions equal to the programmable value

2.0 Internal User-Programmable Registers (Continued)

stored in the Interrupt Enable register's Bits 11–15. This value ranges from 0001 to 1111, representing 1 to 31 conversions stored in the FIFO. A user-programmed value of 0000 has no meaning. See Section 3.0 for more FIFO information.

The completion of the short, single-sampled auto-zero calibration generates **Interrupt 3**.

The completion of a full auto-zero and linearity self-calibration generates **Interrupt 4**.

Interrupt 5 is generated when the Sequencer encounters an instruction that has its Pause bit (Bit 1 in Instruction RAM "00") set to "1".

Interrupt 7 is issued after a short delay (10 ms typ) while the LM12L454/8 returns from Standby mode to active operation using the Configuration register's Bit 4. This short delay allows the internal analog circuitry to settle sufficiently, ensuring accurate conversion results.

2.4 INTERRUPT ENABLE REGISTER

The Interrupt Enable register at address location 1001 (A4–A1, BW = 0) or 1001x (A4–A0, BW = 1) has READ/WRITE capability. An individual interrupt's ability to produce an external interrupt at pin 31 ($\overline{INT}$) is accomplished by placing a "1" in the appropriate bit location. Any of the internal interrupt-producing operations will set their corresponding bits to "1" in the Interrupt Status register regardless of the state of the associated bit in the Interrupt Enable register. See Section 2.3 for more information about each of the eight internal interrupts.

Bit 0 enables an external interrupt when an internal "watchdog" comparison limit interrupt has taken place.

Bit 1 enables an external interrupt when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 enables an external interrupt when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 enables an external interrupt when the single-sampled auto-zero calibration has been completed.

Bit 4 enables an external interrupt when a full auto-zero and linearity self-calibration has been completed.

Bit 5 enables an external interrupt when an internal Pause interrupt has been generated.

Bit 6 is a "Don't Care".

Bit 7 enables an external interrupt when the LM12L454/8 return from power-down to active mode.

Bits 8–10 form the storage location of the user-programmable value against which the Sequencer's address is compared. When the Sequencer reaches an address that is equal to the value stored in Bits 8–10, an internal interrupt is generated and appears in Bit 1 of the Interrupt Status register. If Bit 1 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 ($\overline{INT}$).

The value stored in bits 8–10 ranges from 000 to 111, representing 0 to 7 instructions stored in the Instruction RAM. After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer is started by placing a "1" in the Configuration register's START bit. Setting the INT 1 trigger value to 000 **does not generate** an INT 1 the **first** time the Sequencer retrieves and decodes Instruction 000. The Sequencer **generates** INT 1 (by placing a "1" in the Interrupt Status register's Bit 1) the **second time and after** the Sequencer encounters Instruction 000. It is important to remember that the Sequencer continues to operate even if an Instruction interrupt (INT 1) is internally or externally generated. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

Bits 11–15 hold the number of conversions that must be stored in the Conversion FIFO in order to generate an internal interrupt. This internal interrupt appears in Bit 2 of the Interrupt Status register. If Bit 2 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 ($\overline{INT}$).

2.5 INTERRUPT STATUS REGISTER

This read-only register is located at address 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1). The corresponding flag in the Interrupt Status register goes high ("1") any time that an interrupt condition takes place, whether an interrupt is enabled or disabled in the Interrupt Enable register. Any of the active ("1") Interrupt Status register flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration Register).

Bit 0 is set to "1" when a "watchdog" comparison limit interrupt has taken place.

Bit 1 is set to "1" when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 is set to "1" when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 is set to "1" when the single-sampled auto-zero has been completed.

Bit 4 is set to "1" when an auto-zero and full linearity self-calibration has been completed.

Bit 5 is set to "1" when a Pause interrupt has been generated.

Bit 6 is a "Don't Care".

Bit 7 is set to "1" when the LM12L454/8 return from power-down to active mode.

Bits 8–10 hold the Sequencer's actual instruction address while it is running.

Bits 11–15 hold the actual number of conversions stored in the Conversion FIFO while the Sequencer is running.

2.6 LIMIT STATUS REGISTER

The read-only register is located at address 1101 (A4–A1, BW = 0) or 1101x (A4–A0, BW = 1). This register is used in tandem with the Limit #1 and Limit #2 registers in the Instruction RAM. Whenever a given instruction's input voltage exceeds the limit set in its corresponding Limit register (#1 or #2), a bit, corresponding to the instruction number, is set in the Limit Status register. Any of the active ("1") Limit Status flags are reset to "0" whenever this register is

2.0 Internal User-Programmable Registers (Continued)

read or a device reset is issued (see Bit 1 in the Configuration register). This register holds the status of limits #1 and #2 for each of the eight instructions.

Bits 0–7 show the Limit #1 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #1 register. When, for example, instruction 3 is a "watchdog" operation (Bit 11 is set high) and the input for instruction 3 meets the magnitude and/or polarity data stored in instruction 3's Limit #1 register, Bit 3 in the Limit Status register will be set to a "1".

Bits 8–15 show the Limit #2 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #2 register. When, for example, the input to instruction 6 meets the value stored in instruction 6's Limit #2 register, Bit 14 in the Limit Status register will be set to a "1".

2.7 TIMER

The LM12L454/8 have an on-board 16-bit timer that includes a 5-bit pre-scaler. It uses the clock signal applied to pin 23 as its input. It can generate time intervals of 0 through 2^{21} clock cycles in steps of 2^5. This time interval can be used to delay the execution of instructions. It can also be used to slow the conversion rate when converting slowly changing signals. This can reduce the amount of redundant data stored in the FIFO and retrieved by the controller.

The user-defined timing value used by the Timer is stored in the 16-bit READ/WRITE Timer register at location 1011 (A4–A1, BW = 0) or 1011x (A4–A0, BW = 1) and is preloaded automatically. Bits 0–7 hold the preset value's low byte and Bits 8–15 hold the high byte. The Timer is activated by the Sequencer only if the current instruction's Bit 9 is set ("1"). If the equivalent decimal value "N" ($0 \leq N \leq 2^{16} - 1$) is written inside the 16-bit Timer register and the Timer is enabled by setting an instruction's bit 9 to a "1", the Sequencer will delay the same instruction's execution by halting at state 3 (S3), as shown in *Figure 11,* for $32 \times N + 2$ clock cycles.

2.8 DMA

The DMA works in tandem with Interrupt 2. An active DMA Request on pin 32 (DMARQ) requires that the FIFO interrupt be enabled. The voltage on the DMARQ pin goes high when the number of conversions in the FIFO equals the 5-bit value stored in the Interrupt Enable register (bits 11–15). The voltage on the $\overline{INT}$ pin goes low at the same time as the voltage on the DMARQ pin goes high. The voltage on the DMARQ pin goes low when the FIFO is emptied. The Interrupt Status register must be read to clear the FIFO interrupt flag in order to enable the next DMA request.

DMA operation is optimized through the use of the 16-bit databus connection (a logic "0" applied to the BW pin). Using this bus width allows DMA controllers that have single address Read/Write capability to easily unload the FIFO. Using DMA on an 8-bit databus is more difficult. Two read operations (low byte, high byte) are needed to retrieve each conversion result from the FIFO. Therefore, the DMA controller must be able to repeatedly access two constant addresses when transferring data from the LM12L454/8 to the host system.

3.0 FIFO

The result of each conversion stored in an internal read-only FIFO (First-In, First-Out) register. It is located at 1100 (A4–A1, BW = 0) or 1100x (A4–A0, BW = 1). This register has 32 16-bit wide locations. Each location holds 13-bit data. Bits 0–3 hold the four LSB's in the 12 bits + sign mode or "1110" in the 8 bits + sign mode. Bits 4–11 hold the eight MSB's and Bit 12 holds the sign bit. Bits 13–15 can hold either the sign bit, extending the register's two's complement data format to a full sixteen bits or the instruction address that generated the conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

The FIFO status should be read in the Interrupt Status register (Bits 11–15) to determine the number of conversion results that are held in the FIFO before retrieving them. This will help prevent conversion data corruption that may take place if the number of reads are greater than the number of conversion results contained in the FIFO. Trying to read the FIFO when it is empty may corrupt new data being written into the FIFO. Writing more than 32 conversion data into the FIFO by the ADC results in loss of the first conversion data. Therefore, to prevent data loss, it is recommended that the LM12L454/8's interrupt capability be used to inform the system controller that the FIFO is full.

The lower portion (A0 = 0) of the data word (Bits 0–7) should be read first followed by a read of the upper portion (A0 = 1) when using the 8-bit bus width (BW = 1). Reading the upper portion first causes the data to shift down, which results in loss of the lower byte.

Bits 0–12 hold 12-bit + sign conversion data. **Bits 0–3** will be 1110 (LSB) when using 8-bit plus sign resolution.

Bits 13–15 hold either the instruction responsible for the associated conversion data or the sign bit. Either mode is selected with Bit 5 in the Configuration register.

Using the FIFO's full depth is achieved as follows. Set the value of the Interrupt Enable registers's Bits 11–15 to 1111 and the Interrupt Enable register's Bit 2 to a "1". This generates an external interrupt when the 31st conversion is stored in the FIFO. This gives the host processor a chance to send a "0" to the LM12L454/8's Start bit (Configuration register) and halt the ADC before it completes the 32nd conversion. The Sequencer halts after the current (32) conversion is completed. The conversion data is then transferred to the FIFO and occupies the 32nd location. FIFO overflow is avoided if the Sequencer is halted before the start of the 32nd conversion by placing a "0" in the Start bit (Configuration register). It is important to remember that the Sequencer **continues to operate even if a FIFO interrupt (INT 2) is internally or externally generated**. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

4.0 Sequencer

The Sequencer uses a 3-bit counter (Instruction Pointer, or IP, in *Figure 7)* to retrieve the programmable conversion instructions stored in the Instruction RAM. The 3-bit counter is reset to 000 during chip reset or if the current executed instruction has its Loop bit (Bit 1 in any Instruction RAM "00") set high ("1"). It increments at the end of the currently executed instruction and points to the next instruction. It will continue to increment up to 111 unless an instruction's Loop bit is set. If this bit is set, the counter resets to "000" and execution begins again with the first instruction. If all instructions have their Loop bit reset to "0", the Sequencer will execute all eight instructions continuously. Therefore, it is important to realize that if less than eight instructions are programmed, the Loop bit on the last instruction must be set. Leaving this bit reset to "0" allows the Sequencer to execute "unprogrammed" instructions, the results of which may be unpredictable.

The Sequencer's Instruction Pointer value is readable at any time and is found in the Status register at Bits 8–10. The Sequencer can go through eight states during instruction execution:

State 0: The current instruction's first 16 bits are read from the Instruction RAM "00". This state is one clock cycle long.

State 1: Checks the state of the Calibration and Start bits. This is the "rest" state whenever the Sequencer is stopped using the reset, a Pause command, or the Start bit is reset low ("0"). When the Start bit is set to a "1", this state is one clock cycle long.

State 2: Perform calibration. If bit 2 or bit 6 of the Configuration register is set to a "1", state 2 is 76 clock cycles long. If the Configuration register's bit 3 is set to a "1", state 2 is 4944 clock cycles long.

State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below

$$32T + 2$$

where $0 \leq T \leq 2^{16} - 1$.

State 7: Run the acquisition delay and read Limit #1's value if needed. The number of clock cycles for 12-bit + sign mode varies according to

$$9 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

The number of clock cycles for 8-bit + sign or "watchdog" mode varies according to

$$2 + 2D$$

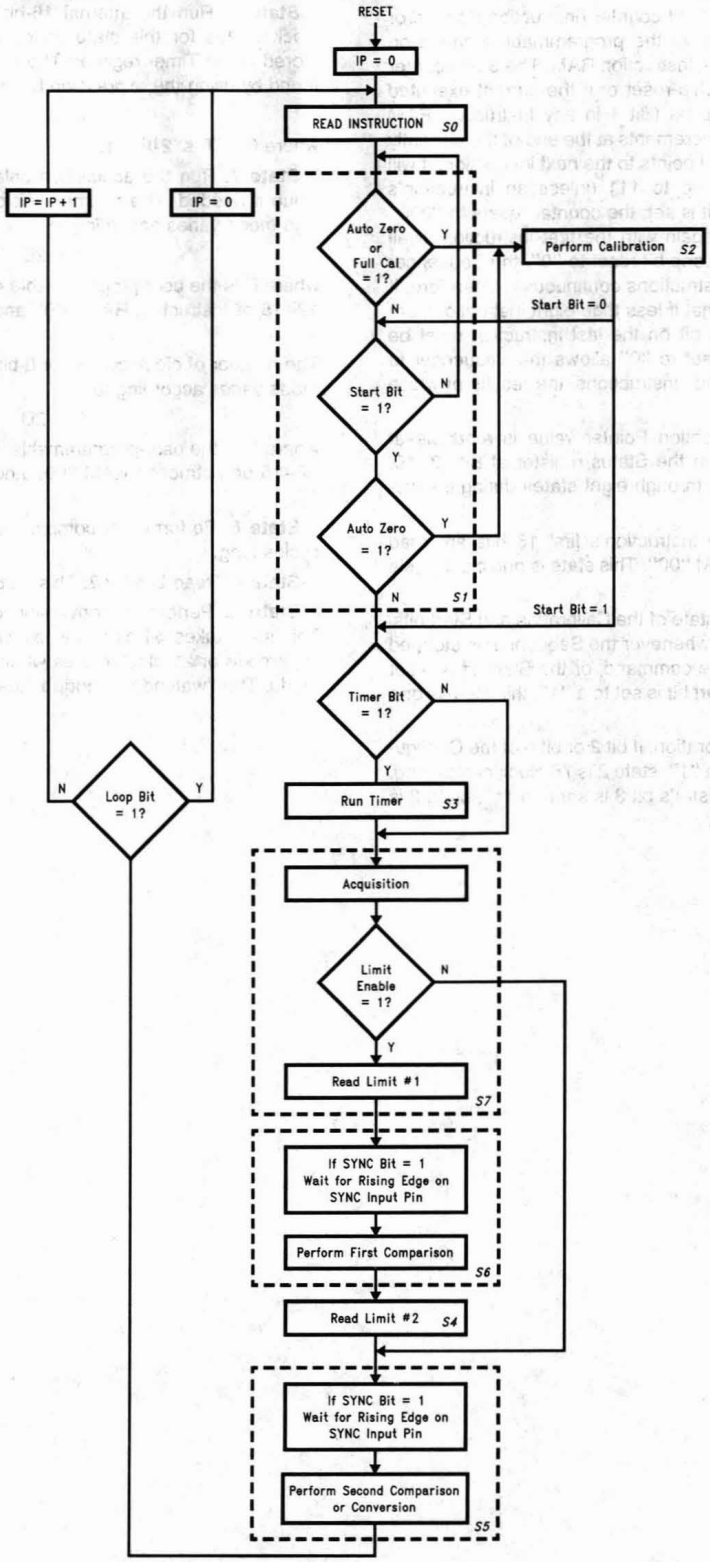
where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

State 6: Perform first comparison. This state is 5 clock cycles long.

State 4: Read Limit #2. This state is 1 clock cycle long.

State 5: Perform a conversion or second comparison. This state takes 44 clock cycles when using the 12-bit + sign mode or 21 clock cycles when using the 8-bit + sign mode. The "watchdog" mode takes 5 clock cycles.

4.0 Sequencer (Continued)



TL/H/11711–22

FIGURE 11. Sequencer Logic Flow Chart (IP = Instruction Pointer)

5.0 Analog Considerations

5.1 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF+} and V_{REF-} defines the analog input voltage span (the difference between the voltages applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF+} or V_{REF-} must have very low output impedance and noise. The circuit in *Figure 12* is an example of a very stable reference appropriate for use with the LM12L454/8.

The ADC can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF+} pin is connected to V_A^+ and V_{REF-} is connected to GND. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions.

For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

5.2 INPUT RANGE

The LM12L454/8's fully differential ADC and reference voltage inputs generate a two's-complement output that is found by using the equation below.

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (4096) - \tfrac{1}{2} \qquad \text{(12-bit)}$$

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (256) - \tfrac{1}{2} \qquad \text{(8-bit)}$$

Round up to the next integer value between −4096 to 4095 for 12-bit resolution and between −256 to 255 for 8-bit resolution if the result of the above equation is not a whole number. As an example, V_{REF+} = 2.5V, V_{REF-} = 1V, V_{IN+} = 1.5V and V_{IN-} = GND. The 12-bit + sign output code is positive full-scale, or 0,1111,1111,1111. If V_{REF+} = 3.3V, V_{REF-} = 1V, V_{IN+} = 3V, and V_{IN-} = GND, the 12-bit + sign output code is 0,1100,0000,0000.

5.3 INPUT CURRENT

A charging current flows into or out of (depending on the input voltage polarity) the analog input pins, IN0–IN7 at the start of the analog input acquisition time (t_{ACQ}). This current's peak value will depend on the actual input voltage applied.

5.4 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<80Ω for 6 MHz operation) the input charging current will decay, before the end of the S/H's acquisition time, to a value that will not introduce any conversion errors. For higher source impedances, the S/H's acquisition time can be increased. As an example, operating with a 6 MHz clock frequency and maximum acquisition time, the LM12L454/8's analog inputs can handle source impedance as high as 5.56 kΩ. Refer to Section 2.1, Instruction RAM "00", Bits 12–15 for further information.

5.5 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, IN0–IN7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. It will not degrade the conversion accuracy.

5.6 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

5.7 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF monolithic ceramic capacitors are recom-

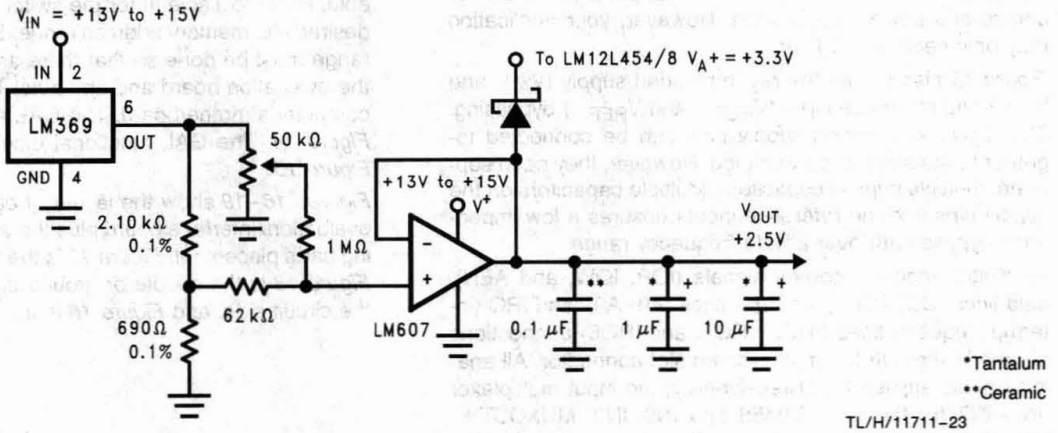


FIGURE 12. Low Drift Extremely Stable Reference Circuit

5.0 Analog Considerations (Continued)

mended for supply bypassing. Separate bypass capacitors should be used for the V_A+ and V_D+ supplies and placed as close as possible to these pins.

5.8 GROUNDING

The LM12L454/8's nominal high resolution performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all analog signal handling circuitry. The digital and analog ground planes are connected at only one point, the power supply ground. This greatly reduces the occurrence of ground loops and noise.

It is recommended that stray capacitance between the analog inputs or outputs (LM12L454: IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+, S/H IN−; LM12L458: IN0–IN7, $V_{REF}+$, and $V_{REF}-$) be reduced by increasing the clearance (+1/16th inch) between the analog signal and reference pins and the ground plane.

5.9 CLOCK SIGNAL LINE ISOLATION

The LM12L454/8's performance is optimized by routing the analog input/output and reference signal conductors (pins 34–44) as far as possible from the conductor that carries the clock signal to pin 23. Ground traces parallel to the clock signal trace can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

6.0 Application Circuits

6.1 PC EVALUATION/INTERFACE BOARD

Figure 13 is the schematic of an evaluation/interface board designed to interface the LM12(H)454 or LM12(H)458 with an XT or AT style computer. The LM12(H)454/8 is the 5V version of the Data Acquisition System. It is functionally equivalent to the LM12L454/8. See the LM12(H)454/8 datasheet for further information. The board can be used to develop both software and hardware for applications using the LM12L454/8. The board hardwires the BW (Bus Width) pin to a logic high, selecting an 8-bit wide databus. Therefore, it is designed for an 8-bit expansion slot on the computer's motherboard.

The circuit operates on a single +5V supply derived from the computer's +12V supply using an LM340 regulator. This greatly attenuates noise that may be present on the computer's power supply lines. However, your application may only need an LC filter.

Figure 13 also shows the recommended supply (V_A+ and V_D+) and reference input ($V_{REF}+$ and $V_{REF}-$) bypassing. The digital and analog supply pins can be connected together to the same supply voltage. However, they need separate, multiple bypass capacitors. Multiple capacitors on the supply pins and the reference inputs ensures a low impedance bypass path over a wide frequency range.

All digital interface control signals (IOR, IOW, and AEN), data lines (DB0–DB7), address lines (A0–A9), and IRQ (interrupt request) lines (IRQ2, IRQ3, and IRQ5) connections are made through the motherboard slot connector. All analog signals applied to, or received by, the input multiplexer (IN0–IN7 for the LM12(H)458 and IN0–IN3, MUXOUT+, MUXOUT−, S/H IN+ and S/H IN− for the LM12(H)454), $V_{REF}+$, $V_{REF}-$, V_{REFOUT}, and the SYNC signal input/output are applied through a DB-37 connector on the rear side of the board. *Figure 13* shows that there are numerous analog ground connections available on the DB-37 connector.

The voltage applied to $V_{REF}-$ and $V_{REF}+$ is selected using two jumpers, JP1 and JP2. JP1 selects between the voltage applied to the DB-37's pin 24 or GND and applies it to the LM12(H)454/8's $V_{REF}-$ input. JP2 selects between the LM12(H)454/8's internal reference output, V_{REFOUT}, and the voltage applied to the DB-37's pin 22 and applies it to the LM12(H)454/8's $V_{REF}+$ input.

TABLE III. LM12(H)454/8 Evaluation/Interface Board SW DIP-8 Switch Settings for Available I/O Memory Locations

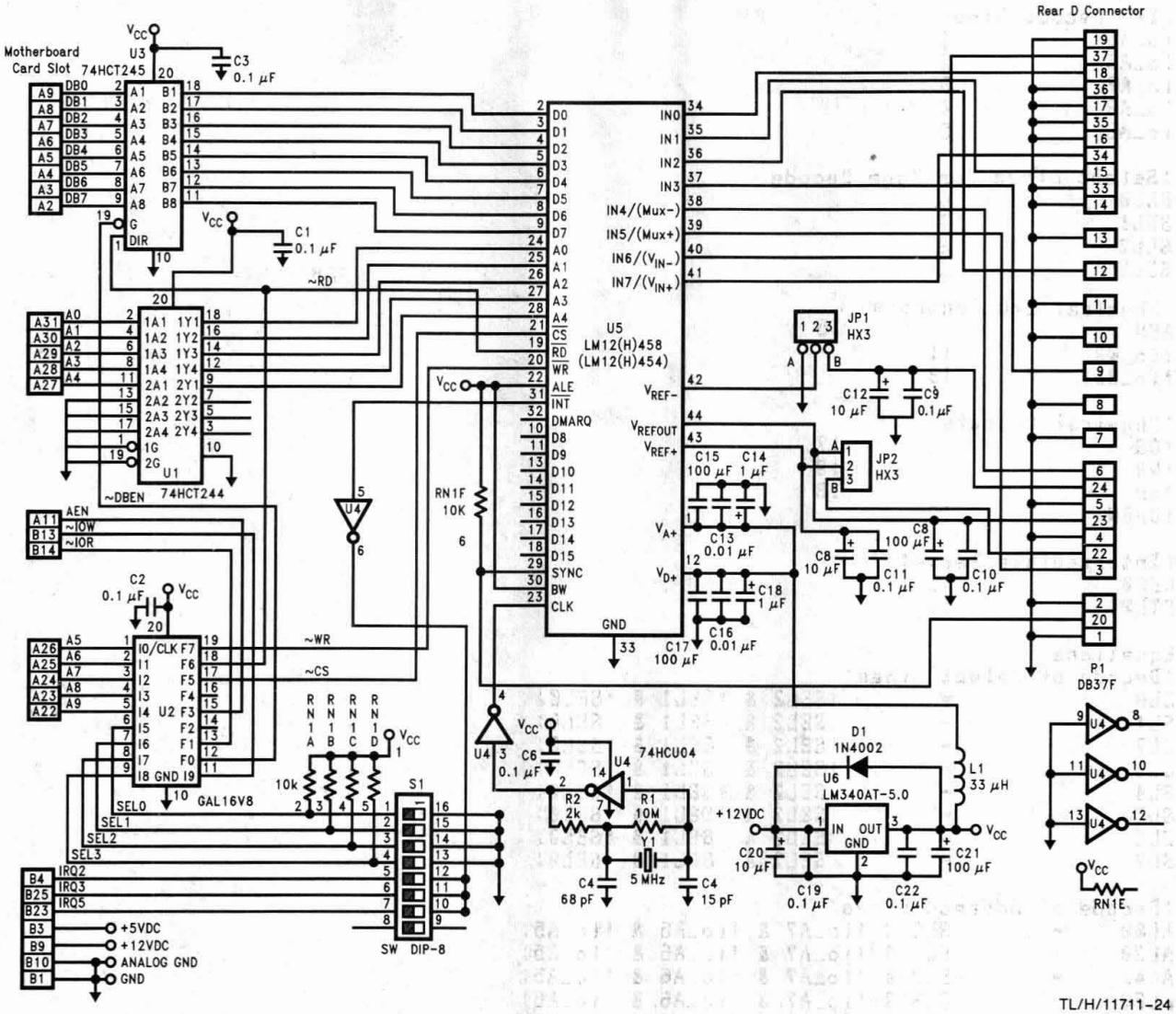
Hexidecimal I/O Memory Base Address	SW DIP-8			
	SW1 (SEL0)	SW2 (SEL1)	SW3 (SEL2)	SW4 (SEL3)
100	ON	ON	ON	ON
120	OFF	ON	ON	ON
140	ON	OFF	ON	ON
160	OFF	OFF	ON	ON
180	ON	ON	OFF	ON
1A0	OFF	ON	OFF	ON
1C0	ON	OFF	OFF	ON
300	OFF	OFF	OFF	ON
340	ON	ON	ON	OFF
280	OFF	ON	ON	OFF
2A0	ON	OFF	ON	OFF

The board allows the use of one of three Interrupt Request (IRQ) lines IRQ2, IRQ3, and IRQ5. The individual IRQ line can be selected using switches 5, 6, and 7 of SW DIP-8. When using any of these three IRQs, the user needs to ensure that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard.

Switches 1–4, along with address lines A5–A9 are used as inputs to GAL16V8 Programmable Gate Array (U2). This device forms the interface between the computer's control and address lines and generates the control signals used by the LM12(H)454/8 for $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$. It also generates the signal that controls the data buffers. Several address ranges within the computer's I/O memory map are available. Refer to Table III for the switch settings that gives the desired I/O memory address range. Selection of an address range must be done so that there are no conflicts between the evaluation board and any other boards attached to the computer's motherboard. The GAL equations are shown in *Figure 14*. The GAL functional block diagram is shown in *Figure 15*.

Figures 16–19 show the layout of each layer in the 3-layer evaluation/interface board plus the silk-screen layout showing parts placement. *Figure 17* is the top or component side, *Figure 18* is the middle or ground plane layer, *Figure 19* is the circuit side, and *Figure 16* is the parts layout.

6.0 Application Circuits (Continued)



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Note: The layout utilizes a split ground plane. The analog ground plane is placed under all analog signals and U5 pins 1, 34–44. The remaining signals and pins are placed over the digital ground. The single point ground connection is at U6, pin 2, and this is connected to the motherboard pin B1.

Parts List:

Y1	HC49U, 8 MHz crystal
D1	1N4002
L1	33 µH
P1	DB37F; parallel connector
R1	10 MΩ, 5%, 1/4W
R2	2 kΩ, 5%, 1/4W
RN1	10 kΩ, 6 resistor SIP, 5%, 1/8W
JP1, JP2	HX3, 3-pin jumper
S1	SW DIP-8; 8 SPST switches
C1–3, C6, C9–11, C19, C22	0.1 µF, 50V, monolithic ceramic
C4	68 pF, 50V, ceramic disk
C5	15 pF, 50V, ceramic disk
C7, C21	100 µF, 25V, electrolytic
C8, C12, C20	10 µF, 35V, electrolytic
C13, C16	0.01 µF, 50V, monolithic ceramic
C14, C18	1 µF, 35V, tantalum
C15, C17	100 µF, 50V, ceramic disk
U1	MM74HCT244N
U2	GAL16V8-20LNC
U3	MM74HCT245N
U4	MM74HCU04N
U5	LM12H458CIV or LM12H454CIV
U6	LM340AT-5.0
SK1	44-pin PLCC socket
A1	LM12H458/4 Rev. D PC Board

FIGURE 13. Schematic and Parts List for the LM12(H)454/8 Evaluation/Interface Board for XT and AT Style Computers, Order Number LM12458EVAL

6.0 Application Circuits (Continued)

```
;I/O Decode Lines
io_A5           1
io_A6           2
io_A7           3
io_A8           4
io_A9           5

;Select Lines for Zone Decode
SEL0            6
SEL1            7
SEL2            8
SEL3            9

;Physical I/O Controls
AEN                     15
!io_WR          11
!io_RD          13

;Physical Outputs
!CS                     17
!WR                     19
!RD                     18
!DBEN           12

;Intermediate Terms:
DEC0            16
FILT            14

Equations
;Decode of Select Lines:
SL0             =       !SEL2 & !SEL1 & !SEL0;
SL1             =       !SEL2 & !SEL1 &  SEL0;
SL2             =       !SEL2 &  SEL1 & !SEL0;
SL3             =       !SEL2 &  SEL1 &  SEL0;
SL4             =        SEL2 & !SEL1 & !SEL0;
SL5             =        SEL2 & !SEL1 &  SEL0;
SL6             =        SEL2 &  SEL1 & !SEL0;
SL7             =        SEL2 &  SEL1 &  SEL0;

;Decode of Address Lines:
AL00    =       SL0 & !io_A7 & !io_A6 & !io_A5;
AL20    =       SL1 & !io_A7 & !io_A6 &  io_A5;
AL40    =       SL2 & !io_A7 &  io_A6 & !io_A5;
AL60    =       SL3 & !io_A7 &  io_A6 &  io_A5;
AL80    =       SL4 &  io_A7 & !io_A6 & !io_A5;
ALA0    =       SL5 &  io_A7 & !io_A6 &  io_A5;
ALC0    =       SL6 &  io_A7 &  io_A6 & !io_A5;

AH01    =       !SEL3 & !io_A9 &  io_A8;
AH02    =        SEL3 &  io_A9 & !io_A8 &  io_A7 & !io_A6;
AH03    =        SEL3 &  io_A9 &  io_A8 & !io_A7 & !io_A5;

;Intermediate Address Groups:
DEC0    =       !AEN & (AL00 + AL20 + AL40 + AL60 + AL80 + ALA0 + ALC0);

;DAS Chip Select Decode:
FILT    =       CS & ( io_WR + io_RD);
CS              =       ( io_WR  + io_RD) & DEC0 & ( AH01 + AH02 + AH03);
DBEN    =       CS & DEC0 & ( io_WR + io_RD);

;Delayed Read/ Write Decodes:
WR              =       io_WR & FILT;
RD              =       io_RD & FILT;
```

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FIGURE 14. Logic Equations Used to Program the GAL16V8

6.0 Application Circuits (Continued)

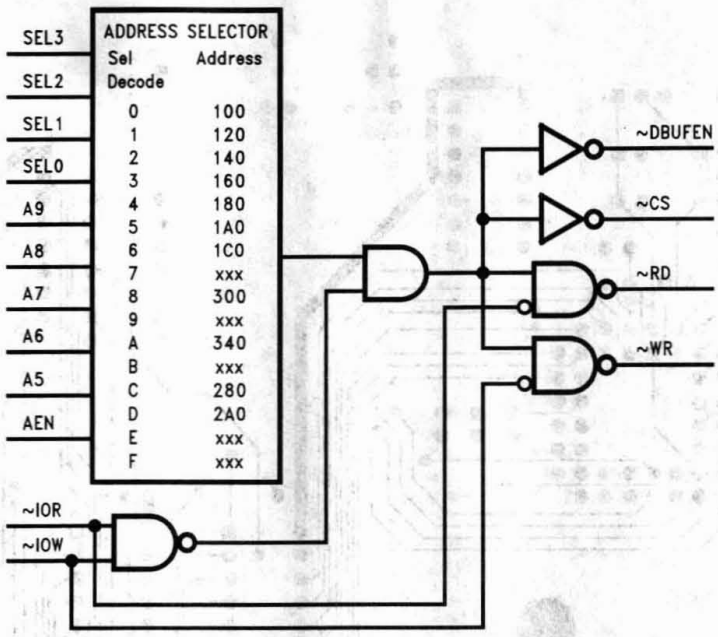

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FIGURE 15. GAL Functional Block Diagram

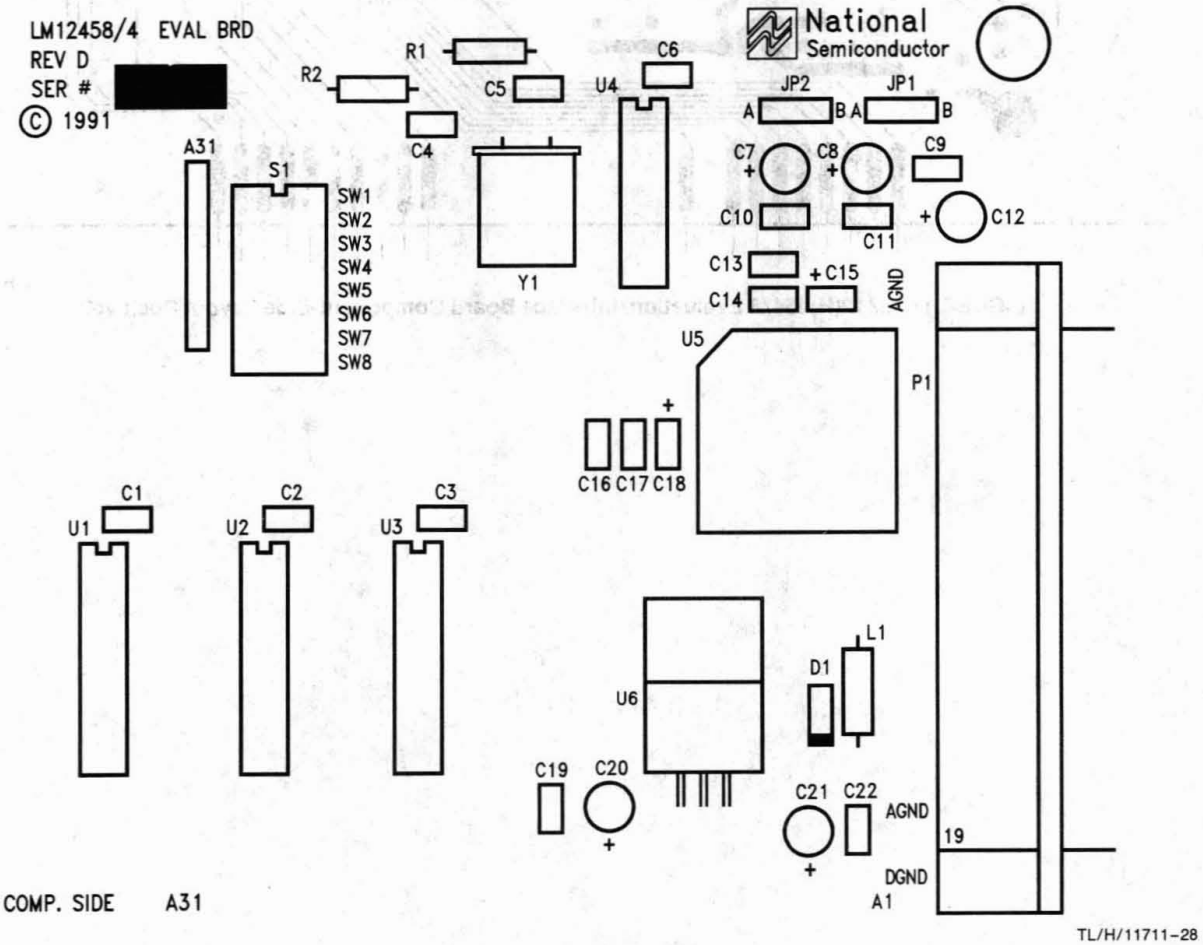

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FIGURE 16. Silk-Screen Layout Showing Parts Placement on the LM12(H)454/8 Evaluation/Interface Board

6.0 Application Circuits (Continued)

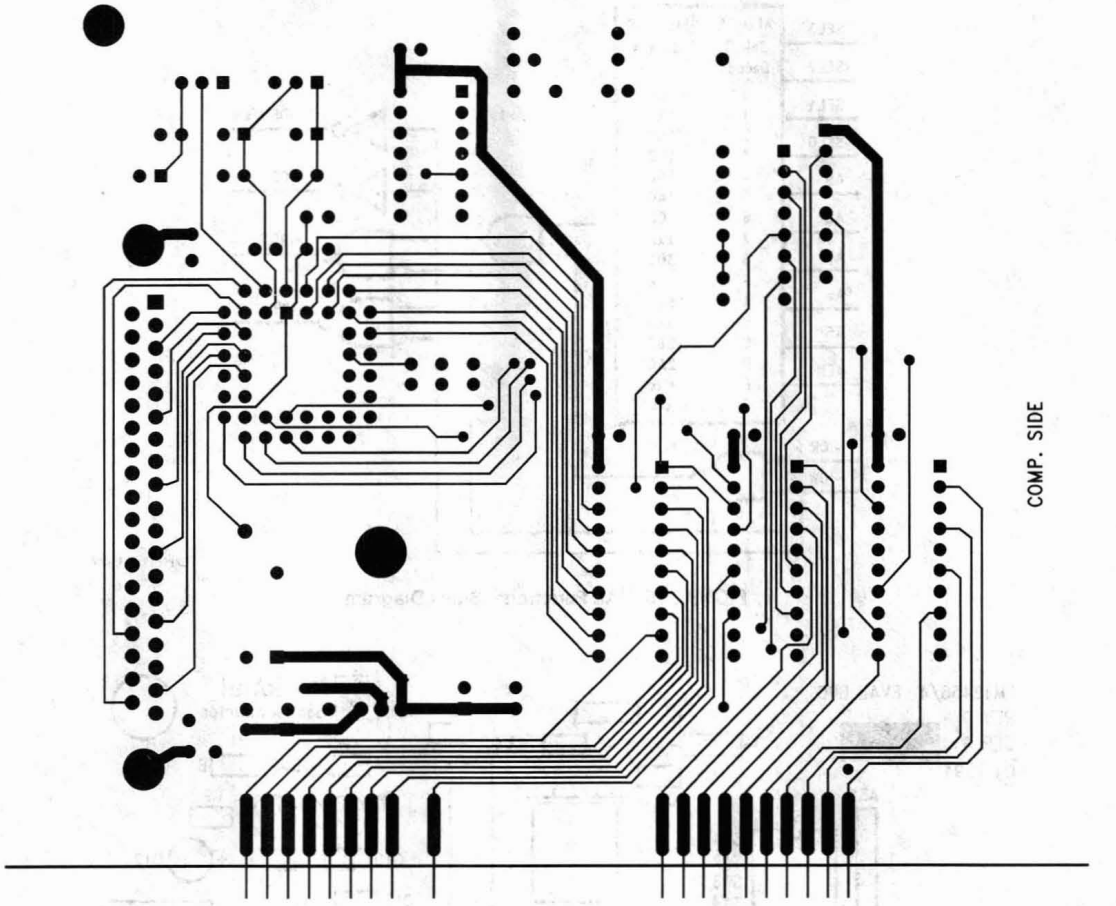

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FIGURE 17. LM12(H)454/8 Evaluation/Interface Board Component-Side Layout Positive

6.0 Application Circuits (Continued)

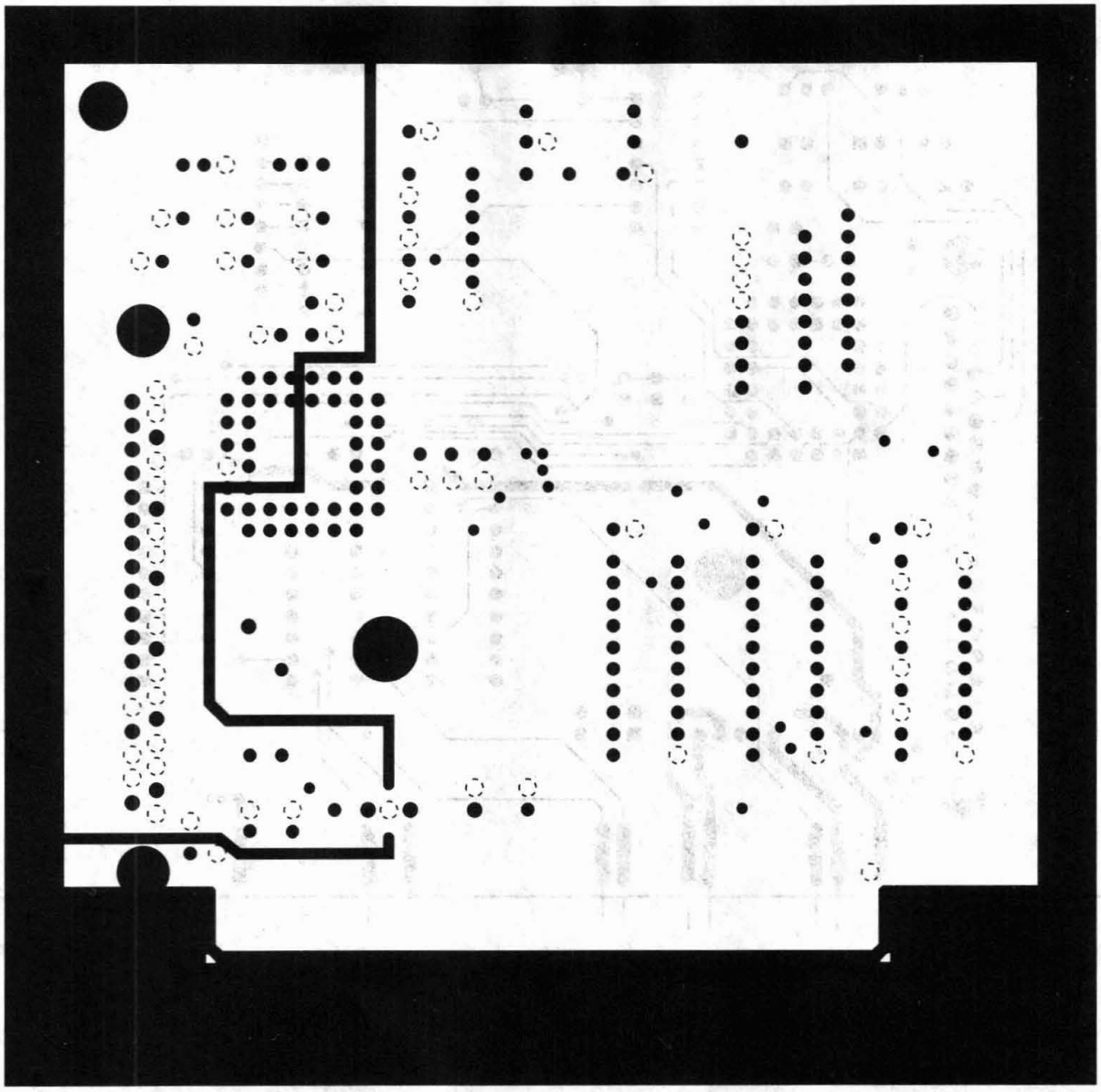

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FIGURE 18. LM12(H)454/8 Evaluation/Interface Board Ground-Plane Layout Negative

6.0 Application Circuits (Continued)

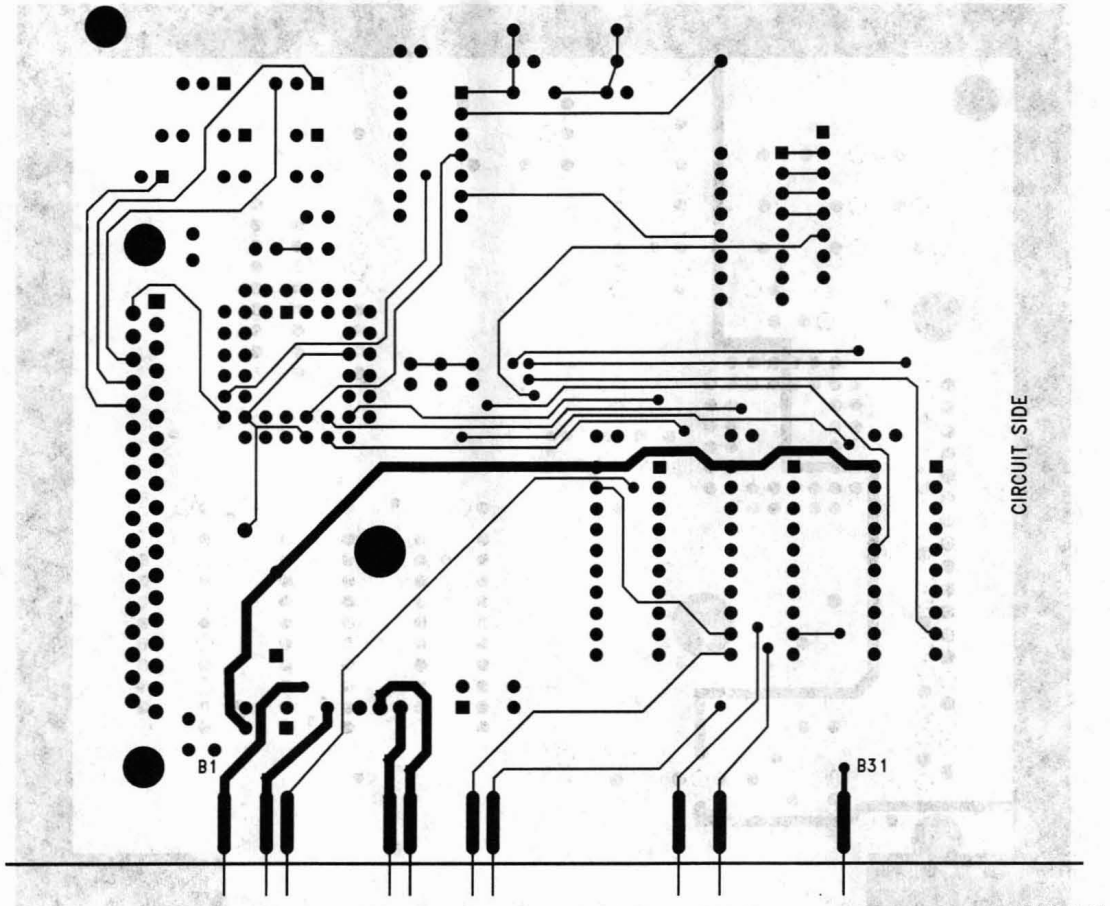

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FIGURE 19. LM12(H)454/8 Evaluation/Interface Circuit-Side Layout Positive

Section 2

Analog-to-Digital Converters

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Definition Of Terms A/D Converters

Conversion Time: The time required for a complete measurement by an analog-to-digital converter. Since the Conversion Time does not include acquisition time, multiplexer set up time, or other elements of a complete conversion cycle, the conversion time may be less than the Throughput Time.

DC Common-Mode Error: This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

Differential Nonlinearity (DNL): Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB input voltage span that is associated with each output code. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to missing codes in an ADC.

Dynamic Specifications: The specifications of an ADC pertaining to an AC input signal. These include S/N ratio, SNR, SINAD, S/(N+D), ENOB, THD, IMD, FPBW, and SSBW.

Effective Number of Bits (ENOB): The ENOB of an ADC is determined from a measurement of its SINAD and the following equation: ENOB = (SINAD − 1.76)/6.02. This specification combines the effects of many of the other dynamic specifications; errors resulting from dynamic differential and integral nonlinearity, missing codes, THD, and aperture jitter show up in ENOB.

Full Power Bandwidth (FPBW): The frequency at which the S/N ratio has dropped by 3 dB (relative to its low frequency level) for an input signal that is at or near full-scale. This corresponds to a drop in ENOB by ½ bit relative to its low frequency level.

Gain Error (Full Scale Error): The difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation of an ADC transfer function from the line between the ADC's measured endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB. This specification is commonly referred to as INL or ILE.

Intermodulation Distortion (IMD): Two nearby frequency components in a signal will interact through the nonlinearities in an ADC to produce signal at additional frequencies. IMD is commonly defined as the ratio of the rms sum of the distortion product amplitudes to the rms sum of the input frequency amplitudes.

LSB (Least-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Missing Codes: When an incremental increase or decrease in input voltage causes the converter to increment or decrement its numeric output by more than one LSB the converter is said to exhibit "missing codes". If there are missing codes, there are digital codes which cannot be reached by any input voltage value.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Offset Error (Zero Error): This is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Offset error is usually expressed in LSBs.

Peak Harmonic: The amplitude, relative to the fundamental, of the largest harmonic resulting from the A/D conversion of an AC signal.

Power Supply Sensitivity: The sensitivity of a converter to changes in the dc power supply voltages.

Quantization Error: The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

Ratiometric Operation: Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion**. Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

Resolution: The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of digital codes is equal to 2^n. As an example, a 12-bit converter maps the analog signal into $2^{12} = 4096$ digital codes.

Signal-to-Noise Ratio (S/N or SNR): The ratio of the signal amplitude to the background noise level. The background noise is determined by integrating the noise spectral density over the bandwidth of interest.

SINAD (Signal-to-Noise + Distortion Ratio): Similar to the S/N ratio, the SINAD includes harmonic distortion components as part of the noise. (See S/(N+D)

S/N+D (Signal-to-Noise + Distortion Ratio): Similar to the S/N ratio, the S/N+D includes harmonic distortion components as part of the noise. (See SINAD)

Small Signal Bandwidth (SSBW): The frequency at which the S/N ratio has dropped by 3 dB (relative to its low frequency level) for an input signal that is much smaller than the full-scale input (20 dB or 40 dB below full-scale, for example).

Static Specifications: The specifications of an ADC pertaining to a DC signal input. These include gain error, offset error, and differential and integral linearity errors.

Total Harmonic Distortion (THD): Due to inherent nonlinearities even in an ideal ADC transfer function, ADC's will produce harmonics of the input signal frequency. THD is defined as the ratio of the rms sum of the harmonic distortion product amplitudes to the input signal amplitude.

Throughput Rate: The maximum continuous conversion rate of the ADC.

Throughput Time: The inverse of the Throughput Rate.

Total Unadjusted Error (TUE): The maximum deviation of the voltage corresponding to the center of a digital code's associated input voltage span from the ideal case. Total unadjusted error includes offset error, gain error, and differential and integral nonlinearity errors.

National Semiconductor

A/D Converter Selection Guide

(Sorted by Resolution and Speed)

Part No.	I/O Type	Res' (Bits)	Conversion Time (Max)	Accuracy (Max)	# MUX Inputs	S/H	On-Board Reference	Supply Voltage	Temp Range	Power (mW Max)	Packages	Comments
ADC0801	Parallel	8	110 μs	±¼ LSB	1	N	N	+5V	I, M	9 mW	J, N	Differential Input
ADC0802	Parallel	8	110 μs	±½ LSB	1	N	N	+5V	C, I, M	9 mW	J, N, M, V	Differential Input
ADC0803	Parallel	8	110 μs	±½ LSB	1	N	N	+5V	C, I, M	9 mW	J, N, M, V	Differential Input
ADC0804	Parallel	8	110 μs	±1 LSB	1	N	N	+5V	C, I	12.5 mW	J, N, M, V	Differential Input
ADC0805	Parallel	8	110 μs	±1 LSB	1	N	N	+5V	I	9 mW	N	Ratiometric Operation
ADC0808	Parallel	8	100 μs	±½ LSB	8	N	N	+5V	I, M	15 mW	J, N, V	
ADC0809	Parallel	8	100 μs	±1 LSB	8	N	N	+5V	I	15 mW	N, V	
ADC0816	Parallel	8	100 μs	±½ LSB	16	N	N	+5V	I	15 mW	J, N	
ADC0817	Parallel	8	100 μs	±1 LSB	16	N	N	+5V	I	15 mW	N	
ADC0800	Parallel	8	50 μs	±2 LSB	1	N	N	+5V, −12V	C, M	100 mW	J	
ADC0841B	Parallel	8	40 μs	±½ LSB	1	N	N	+5V	C, I	13 mW	N, V	
ADC0841C	Parallel	8	40 μs	±1 LSB	1	N	N	+5V	C, I	13 mW	N, V	
ADC0844B	Parallel	8	40 μs	±½ LSB	4	N	N	+5V	C, I	13 mW	J, N	
ADC0844C	Parallel	8	40 μs	±1 LSB	4	N	N	+5V	C, I	13 mW	J, N	
ADC0848B	Parallel	8	40 μs	±½ LSB	8	N	N	+5V	C, I	13 mW	J, N, V	
ADC0848C	Parallel	8	40 μs	±1 LSB	8	N	N	+5V	C, I	13 mW	J, N, V	
ADC0811B	Serial	8	32 μs	±½ LSB	11	N	N	+5V	I, C	15 mW	N, V	
ADC0811C	Serial	8	32 μs	±1 LSB	11	N	N	+5V	I, C	15 mW	J, N, V	
ADC0831B	Serial	8	32 μs	±½ LSB	1	N	N	+5V	C	15 mW	J, N	
ADC0831C	Serial	8	32 μs	±1 LSB	1	N	N	+5V	C, I	15 mW	J, N, M	
ADC0832B	Serial	8	32 μs	±½ LSB	2	N	N	+5V	C, I	32 mW	N, M	
ADC0832C	Serial	8	32 μs	±1 LSB	2	N	N	+5V	C, I	32 mW	N, M	
ADC0833B	Serial	8	32 μs	±½ LSB	4	N	N	+5V	C	15 mW	N	
ADC0833C	Serial	8	32 μs	±1 LSB	4	N	N	+5V	C, I	15 mW	J, N	
ADC0834B	Serial	8	32 μs	±½ LSB	4	N	N	+5V	C	15 mW	N	
ADC0834C	Serial	8	32 μs	±1 LSB	4	N	N	+5V	C, I	15 mW	J, N, M	
ADC0838B	Serial	8	32 μs	±½ LSB	8	N	N	+5V	C, I	15 mW	J, N, V	
ADC0838C	Serial	8	32 μs	±1 LSB	8	N	N	+5V	C, I	15 mW	J, N, M, V	
ADC0819B	Serial	8	16 μs	±½ LSB	19	N	N	+5V	C	15 mW	N, V	
ADC0819C	Serial	8	16 μs	±1 LSB	19	N	N	+5V	C, I	15 mW	N, V	
ADC08031B	Serial	8	8 μs	±½ LSB	1	Y	Y	+5V	I	20 mW	N, M	

Package Codes:

J	Cerdip	V	PLCC
H	Metal Can	MS	SSOP
N	Plastic Dip	VF	PQFP
M	Small Outline		

Temperatures:

C	0°C to +70°C
I	−25°C to +85°C or −40°C to +85°C
M	−55°C to +125°C

Part No.	I/O Type	Res' (Bits)	Conversion Time (Max)	Accuracy (Max)	# MUX Inputs	S/H	On-Board Reference	Supply Voltage	Temp Range	Power (mW Max)	Packages	Comments
ADC08031C	Serial	8	8 μs	±1 LSB	1	Y	Y	+5V	C, I, M	20 mW	J, N, M	
ADC08032B	Serial	8	8 μs	±½ LSB	2	Y	Y	+5V	I	20 mW	N, M	
ADC08032C	Serial	8	8 μs	±1 LSB	2	Y	Y	+5V	I	20 mW	N, M	
ADC08034B	Serial	8	8 μs	±½ LSB	4	Y	Y	+5V	I	20 mW	N, M	
ADC08034C	Serial	8	8 μs	±1 LSB	4	Y	Y	+5V	I	20 mW	N, M	
ADC08038B	Serial	8	8 μs	±½ LSB	8	Y	Y	+5V	I	20 mW	N, M	
ADC08038C	Serial	8	8 μs	±1 LSB	8	Y	Y	+5V	I, M	20 mW	J, N, M	
ADC08131B	Serial	8	8 μs	±½ LSB	1	Y	Y	+5V	I	20 mW	N	Guaranteed Reference O/P
ADC08131C	Serial	8	8 μs	±1 LSB	1	Y	Y	+5V	I	20 mW	N	Guaranteed Reference O/P
ADC08134B	Serial	8	8 μs	±½ LSB	4	Y	Y	+5V	I	20 mW	N, M	Guaranteed Reference O/P
ADC08134C	Serial	8	8 μs	±1 LSB	4	Y	Y	+5V	I	20 mW	N, M	Guaranteed Reference O/P
ADC08138B	Serial	8	8 μs	±½ LSB	8	Y	Y	+5V	I	20 mW	N, M	Guaranteed Reference O/P
ADC08138C	Serial	8	8 μs	±1 LSB	8	Y	Y	+5V	I	20 mW	N, M	Guaranteed Reference O/P
ADC08231B	Serial	8	2 μs	±½ LSB	8	Y	Y	+5V	I	20 mW	N, M	
ADC08231C	Serial	8	2 μs	±1 LSB	8	Y	Y	+5V	I	20 mW	N, M	
ADC08234B	Serial	8	2 μs	±½ LSB	8	Y	Y	+5V	I	20 mW	N, M	
ADC08234C	Serial	8	2 μs	±1 LSB	8	Y	Y	+5V	I	20 mW	N, M	
ADC08238B	Serial	8	2 μs	±½ LSB	8	Y	Y	+5V	I	20 mW	N, M	
ADC08238C	Serial	8	2 μs	±1 LSB	8	Y	Y	+5V	I, M	20 mW	J, N, M	
ADC0820B	Parallel	8	1.2 μs	±½ LSB	1	Y	N	+5V	C, I	75 mW	N, M, V	
ADC0820C	Parallel	8	1.2 μs	±1 LSB	1	Y	N	+5V	C, I	75 mW	J, N, M, V, MS	
ADC08061B	Parallel	8	560 ns	±½ LSB	1	Y	N	+5V	I	100 mW	N, M	High Speed Upgrade for ADC0820
ADC08061C	Parallel	8	560 ns	±1 LSB	1	Y	N	+5V	I, M	100 mW	J, N, M	High Speed Upgrade for ADC0820
ADC08062B	Parallel	8	560 ns	±½ LSB	2	Y	N	+5V	I	100 mW	N, M	
ADC08062C	Parallel	8	560 ns	±1 LSB	2	Y	N	+5V	I	100 mW	N, M	
ADC08161B	Parallel	8	560 ns	±½ LSB	1	Y	N	+5V	I	100 mW	N, M	ADC08061 with On-Board Reference
ADC08161C	Parallel	8	560 ns	±1 LSB	1	Y	N	+5V	I	100 mW	N, M	ADC08061 with On-Board Reference
ADC1021C	Parallel	10	200 μs	±1 LSB	1	N	N	+5V	C, I	25 mW	J, V	
ADC1001	Byte-Wide	10	50 μs	±1 LSB	1	N	N	+5V	C, I	25 mW	J	
ADC1005B	Byte-Wide	10	50 μs	±½ LSB	1	N	N	+5V	C, I	15 mW	J	
ADC1005C	Byte-Wide	10	50 μs	±1 LSB	1	N	N	+5V	C, I	15 mW	J, V	

Package Codes:

J	Cerdip	V	PLCC
H	Metal Can	MS	SSOP
N	Plastic Dip	VF	PQFP
M	Small Outline		

Temperatures:

C	0°C to +70°C
I	−25°C to +85°C or −40°C to +85°C
M	−55°C to +125°C

A/D Converter Selection Guide (Continued)

Part No.	I/O Type	Res' (Bits)	Conversion Time (Max)	Accuracy (Max)	# MUX Inputs	S/H	On-Board Reference	Supply Voltage	Temp Range	Power (mW Max)	Packages	Comments
ADC1031	Serial	10	13.7 μs	±1 LSB	1	Y	N	+5V	I	15 mW	N	
ADC1034	Serial	10	13.7 μs	±1 LSB	4	Y	N	+5V	I, M	15 mW	J, N, M	
ADC1038	Serial	10	13.7 μs	±1 LSB	8	Y	N	+5V	I, M	15 mW	J, N, M	
ADC1061	Parallel	10	1.8 μs	±2 LSB	1	Y	N	+5V	I, M	235 mW	J, N, M	
ADC10061	Parallel	10	900 ns	±1 LSB	1	Y	N	+5V	I, M	235 mW	J, N, M	1 MS/s Throughput
ADC10062	Parallel	10	900 ns	±1 LSB	2	Y	N	+5V	I, M	235 mW	J, N, M	1 MS/s Throughput
ADC10064	Parallel	10	900 ns	±1 LSB	4	Y	N	+5V	I, M	235 mW	J, N, M	1 MS/s Throughput
ADC10461	Parallel	10	900 ns	±1 LSB	1	Y	N	+5V	I	235 mW	N, M	AC Tested Version of ADC10061
ADC10462	Parallel	10	900 ns	±1 LSB	2	Y	N	+5V	I	235 mW	N, M	AC Tested Version of ADC10062
ADC10464	Parallel	10	900 ns	±1 LSB	4	Y	N	+5V	I	235 mW	N, M	AC Tested Version of ADC10064
ADC10664	Parallel	10	466 ns	±1.5 LSB	4	Y	N	+5V	I	235 mW	N, M	AC Tested, 2 MS/s Throughput
ADC10662	Parallel	10	466 ns	±1.5 LSB	2	Y	N	+5V	I	235 mW	N, M	AC Tested, 2 MS/s Throughput
ADC10731	Serial	10 + Sign	5 μs	±1 LSB	1	Y	Y	+5V	I	37 mW	N, M	Software Power-Down to 18 μW
ADC10732	Serial	10 + Sign	5 μs	±1 LSB	2	Y	Y	+5V	I	37 mW	N, M	Software Power-Down to 18 μW
ADC10734	Serial	10 + Sign	5 μs	±1 LSB	4	Y	Y	+5V	I	37 mW	N, M	Software Power-Down to 18 μW
ADC10738	Serial	10 + Sign	5 μs	±1 LSB	8	Y	Y	+5V	I	37 mW	N, M	Software Power-Down to 18 μW
ADC10831	Serial	10 + Sign	5 μs	±1 LSB	1	Y	Y	±5V	I	59 mW	N, M	Software Power-Down to 33 μW
ADC10832	Serial	10 + Sign	5 μs	±1 LSB	2	Y	Y	±5V	I	59 mW	N, M	Software Power-Down to 33 μW
ADC10834	Serial	10 + Sign	5 μs	±1 LSB	4	Y	Y	±5V	I	59 mW	N, M	Software Power-Down to 33 μW
ADC10838	Serial	10 + Sign	5 μs	±1 LSB	8	Y	Y	±5V	I	59 mW	N, M	Software Power-Down to 33 μW
ADC10154	Byte-Wide	10 + Sign	4.4 μs	±1 LSB	4	Y	Y	+5V, ±5V	I	33 mW	N, M	
ADC10158	Byte-Wide	10 + Sign	4.4 μs	±1 LSB	8	Y	Y	+5V, ±5V	I	33 mW	N, M	
ADC12062B	Parallel	12	980 ns	±1 LSB	2	Y	N	+5V	I	75 mW	V, VF	
ADC12062C	Parallel	12	980 ns	±1½ LSB	2	Y	N	+5V	I	75 mW	V, VF	
ADC12662	Parallel	12	660 ns	±1½ LSB	2	Y	N	+5V	I	200 mW	V, VF	
ADC1205C	Parallel	12 + Sign	100 μs	±1 LSB	1	N	N	+5V, ±5V	C, I	235 mW	J	
ADC1225	Parallel	12 + Sign	100 μs	±1 LSB	1	N	N	+5V, ±5V	C, I	235 mW	J	
ADC1241B	Parallel	12 + Sign	13.8 μs	±½ LSB	1	Y	N	+5V, ±5V	I	70 mW	J	Self Calibrating
ADC1241C	Parallel	12 + Sign	13.8 μs	±1 LSB	1	Y	N	+5V, ±5V	I, M	70 mW	J	Self Calibrating
ADC12441	Parallel	12 + Sign	13.8 μs	±1 LSB	1	Y	N	+5V, ±5V	I	70 mW	J	AC Tested
ADC12030	Serial	12 + Sign	8.8 μs	±1 LSB	2	Y	N	+5V	I	33 mW	N, M	Software Power-Down to 100 μW

Package Codes: J Cerdip; H Metal Can; N Plastic Dip; M Small Outline; V PLCC; MS SSOP; VF PQFP

Temperatures: C 0°C to +70°C; I −25°C to +85°C or −40°C to +85°C; M −55°C to +125°C

A/D Converter Selection Guide (Continued)

Part No.	I/O Type	Res' (Bits)	Conversion Time (Max)	Accuracy (Max)	# MUX Inputs	S/H	On-Board Reference	Supply Voltage	Temp Range	Power (mW Max)	Packages	Comments
ADC12032	Serial	12 + Sign	8.8 μs	±1 LSB	2	Y	N	+5V	I	33 mW	N, M	Software Power-Down to 100 μW
ADC12034	Serial	12 + Sign	8.8 μs	±1 LSB	4	Y	N	+5V	I	33 mW	N, M	Software Power-Down to 100 μW
ADC12038	Serial	12 + Sign	8.8 μs	±1 LSB	8	Y	N	+5V	I	33 mW	N, M	Software Power-Down to 100 μW
ADC12L030	Serial	12 + Sign	8.8 μs	±1 LSB	2	Y	N	+5V	I	15 mW	N, M	3V Guaranteed Operation
ADC12L032	Serial	12 + Sign	8.8 μs	±1 LSB	2	Y	N	+5V	I	15 mW	N, M	3V Guaranteed Operation
ADC12L034	Serial	12 + Sign	8.8 μs	±1 LSB	4	Y	N	+5V	I	15 mW	N, M	3V Guaranteed Operation
ADC12L038	Serial	12 + Sign	8.8 μs	±1 LSB	8	Y	N	+5V	I	15 mW	N, M	3V Guaranteed Operation
ADC1251B	Byte-Wide	12 + Sign	7.7 μs	±½ LSB	1	Y	N	+5V, ±5V	I	113 mW	J	Self Calibrating
ADC1251C	Byte-Wide	12 + Sign	7.7 μs	±1 LSB	1	Y	N	+5V, ±5V	I, M	113 mW	J	Self Calibrating
ADC12451	Byte-Wide	12 + Sign	7.7 μs	±1 LSB	1	Y	N	+5V, ±5V	I	113 mW	J	AC Tested
ADC12H030	Serial	12 + Sign	5.5 μs	±1 LSB	2	Y	N	+5V	I	36 mW	N, M	Software Power-Down to 100 μW
ADC12H032	Serial	12 + Sign	5.5 μs	±1 LSB	2	Y	N	+5V	I	36 mW	N, M	Software Power-Down to 100 μW
ADC12H034	Serial	12 + Sign	5.5 μs	±1 LSB	4	Y	N	+5V	I	36 mW	N, M	Software Power-Down to 100 μW
ADC12H038	Serial	12 + Sign	5.5 μs	±1 LSB	8	Y	N	+5V	I	36 mW	N, M	Software Power-Down to 100 μW
ADC16071	Serial	16	192 kS/s	SINAD: 72 dB	1	Y	N	+5V	I	500 mW	N, M	Delta Sigma Architecture
ADC16471	Serial	16	192 kS/s	SINAD: 72 dB	1	Y	Y	+5V	I	500 mW	N, M	Delta Sigma Architecture
LM131	Frequency	V-F	N/A	0.01%	1	N/A	N	+5V to +40V	C, I, M	30 mW	N, M, H	V to F Converter, 100 kHz Max

Package Codes:

J	Cerdip	V	PLCC
H	Metal Can	MS	SSOP
N	Plastic Dip	VF	PQFP
M	Small Outline		

Temperatures:

C	0°C to +70°C
I	−25°C to +85°C
	or −40°C to +85°C
M	−55°C to +125°C

National Semiconductor

ADC0800 8-Bit A/D Converter

General Description

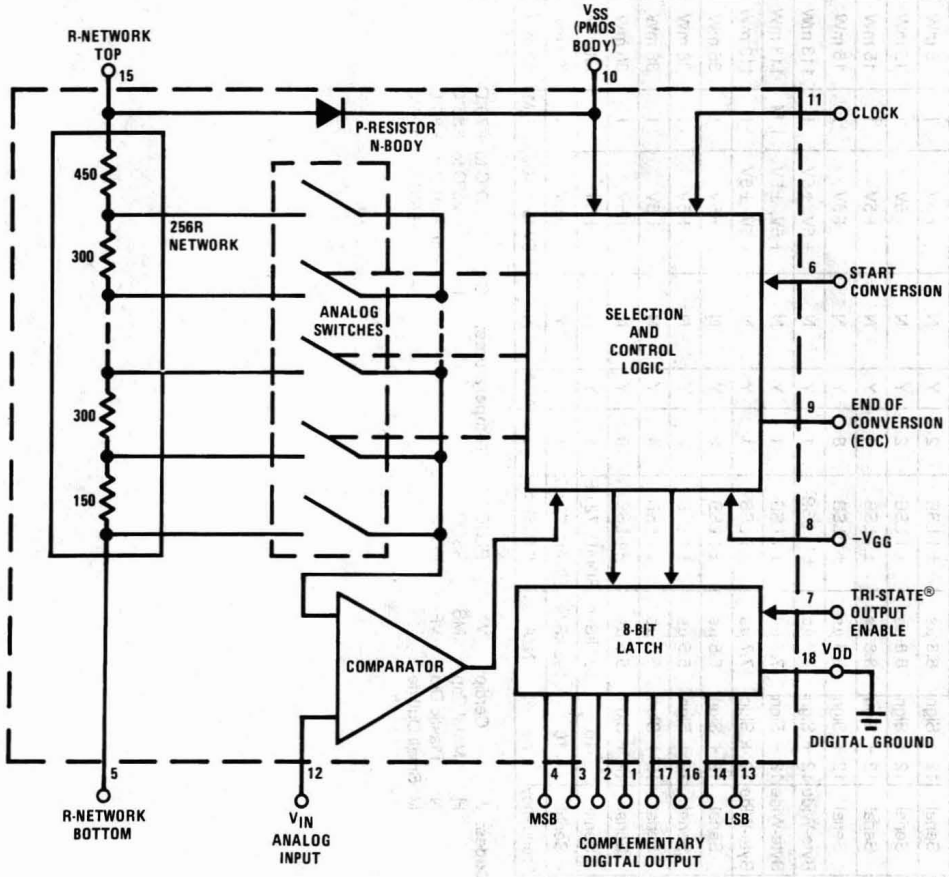
The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

■ Low cost	
■ ±5V, 10V input ranges	
■ No missing codes	
■ Ratiometric conversion	
■ TRI-STATE outputs	
■ Fast	$T_C = 50\ \mu s$
■ Contains output latches	
■ TTL compatible	
■ Supply voltages	5 V_{DC} and −12 V_{DC}
■ Resolution	8 bits
■ Linearity	±1 LSB
■ Conversion speed	40 clock periods
■ Clock range	50 to 800 kHz

Block Diagram



(00000000 = + full-scale)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	$V_{SS}-22V$
Supply Voltage (V_{GG})	$V_{SS}-22V$
Voltage at Any Input	$V_{SS}+0.3V$ to $V_{SS}-22V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	875 mW
ESD Susceptibility (Note 4)	500V
Storage Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0800PD	$-55°C \le T_A \le +125°C$
ADC0800PCD	$0°C \le T_A \le +70°C$

Electrical Characteristics

These specifications apply for $V_{SS}=5.0\ V_{DC}$, $V_{GG}=-12.0\ V_{DC}$, $V_{DD}=0\ V_{DC}$, a reference voltage of 10.000 V_{DC} across the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}=5.000\ V_{DC}$ and $V_{R\text{-}NETWORK\ BOTTOM}=-5.000\ V_{DC}$), and a clock frequency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to $V_{R\text{-}NETWORK\ BOTTOM}=-5\ V_{DC}$. Unless otherwise noted, these specifications apply over an ambient temperature range of −55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

Parameter	Conditions	Min	Typ	Max	Units
Non-Linearity	$T_A=25°C$, (Note 8) Over Temperature, (Note 8)			±1 ±2	LSB LSB
Differential Non-Linearity				±½	LSB
Zero Error				±2	LSB
Zero Error Temperature Coefficient	(Note 9)			0.01	%/°C
Full-Scale Error				±2	LSB
Full-Scale Error Temperature Coefficient	(Note 9)			0.01	%/°C
Input Leakage				1	μA
Logical "1" Input Voltage	All Inputs	$V_{SS}-1.0$		V_{SS}	V
Logical "0" Input Voltage	All Inputs	V_{GG}		$V_{SS}-4.2$	V
Logical Input Leakage	$T_A=25°C$, All Inputs, $V_{IL}=V_{SS}-10V$			1	μA
Logical "1" Output Voltage	All Outputs, $I_{OH}=100\ \mu A$	2.4			V
Logical "0" Output Voltage	All Outputs, $I_{OL}=1.6$ mA			0.4	V
Disabled Output Leakage	$T_A=25°C$, All Outputs, $V_{OL}=V_{SS}$@10V			2	μA
Clock Frequency	$0°C \le T_A \le +70°C$ $-55°C \le T_A \le +125°C$	50 100		800 500	kHz kHz
Clock Pulse Duty Cycle		40		60	%
TRI-STATE Enable/Disable Time				1	μs
Start Conversion Pulse	(Note 10)	1		3½	Clock Periods
Power Supply Current	$T_A=25°C$			20	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the ADC0800PD and ADC0800PCD when board mounted is 66°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

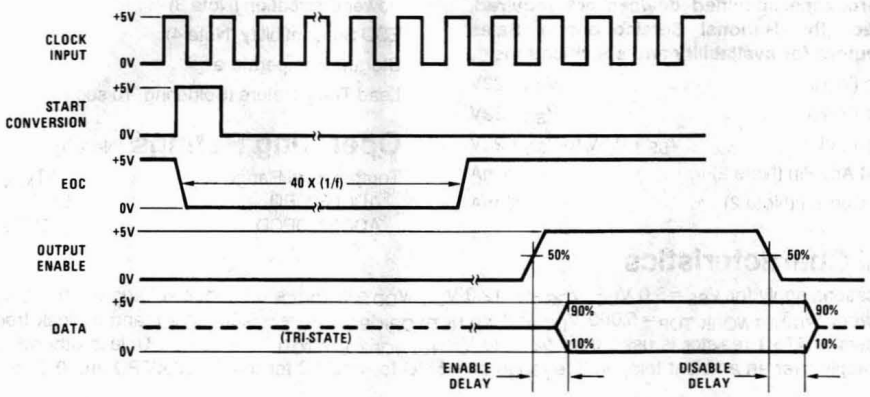
Note 7: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 8: Non-linearity specifications are based on best straight line.

Note 9: Guaranteed by design only.

Note 10: Start conversion pulse duration greater than 3½ clock periods will cause conversion errors.

Timing Diagram



TL/H/5670–2

Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and $\frac{3}{4}$ V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time in the latches. The data outputs are activated when the Output Enable is high, and in TRI-STATE when Output Enable is low. The Enable Delay time is approximately 200 ns. Each conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. $V_{REF} = 10.00V$ with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, applied to the top of the R-network (pin 15), must not exceed V_{SS}, to prevent forward biasing the on-chip parasitic silicon diodes that exist between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp that is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage that is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{GG}$ supply voltage to ensure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_S \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pickup due to unavoidable series lead inductance.
For $5k < R_S \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_S > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to ensure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage swing for the Clock, Start Conversion and Output Enable should be ($V_{SS} - 1.0V$).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse that occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses that occur during this last 4 clock period interval may be ignored (see *Figure 1* and *2* for high speed operation). This is a problem only for high conversion rates and keeping the number of conversions per second less than $f_{CLOCK}/44$ automatically guarantees proper operation. For example, for an 800 kHz clock, approximately 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

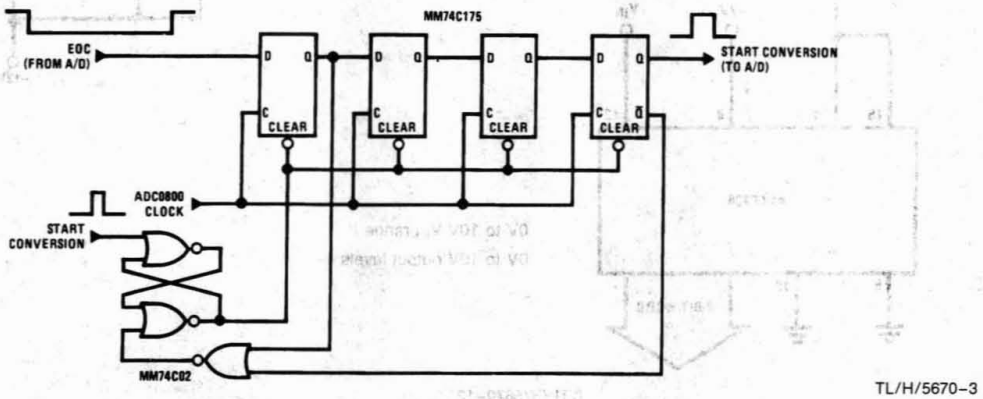
Standard supplies are $V_{SS} = +5V$, $V_{GG} = -12V$ and $V_{DD} = 0V$. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to V_{SS}—V_{GG}. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

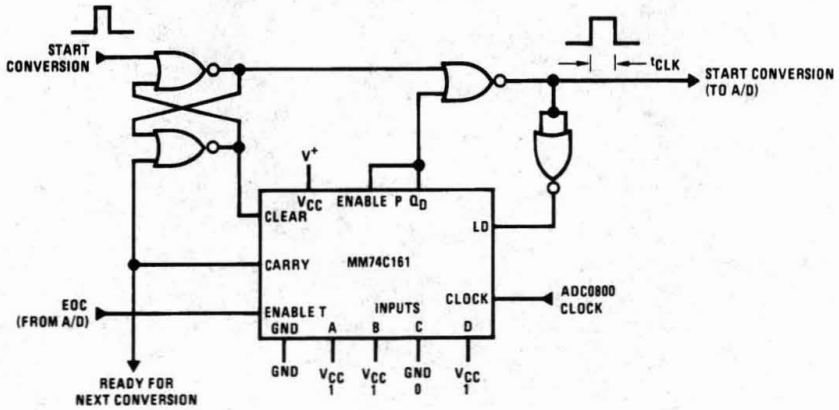
To prevent missing a start pulse that may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, to continuously convert for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.



TL/H/5670–3

FIGURE 1. Delaying an Asynchronous Start Pulse



TL/H/5670–10

FIGURE 2. A/D Control Logic

Application Hints (Continued)

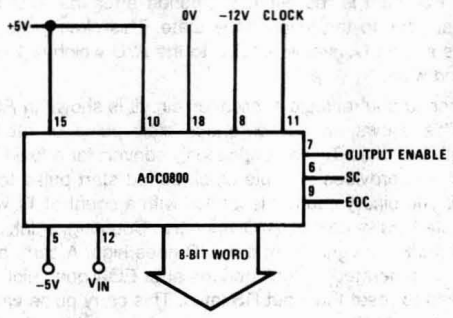
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is ½ LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 ½ LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within ±2 LSB for the ADC0800 without adjustment. In most cases, adjustment can be accomplished by having a 1 kΩ pot on pin 15.

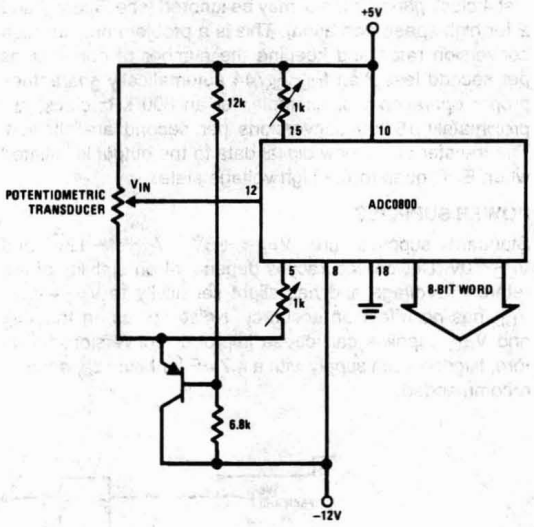
Typical Applications

General Connection



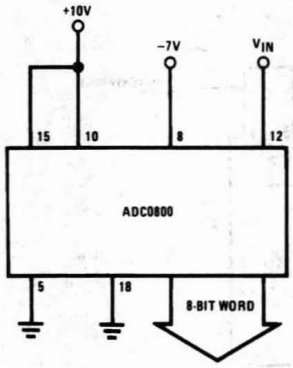
TL/H/5670–11

Ratiometric Input Signal with Tracking Reference



TL/H/5670–4

Hi-Voltage CMOS Output Levels



0V to 10V V_{IN} range
0V to 10V output levels

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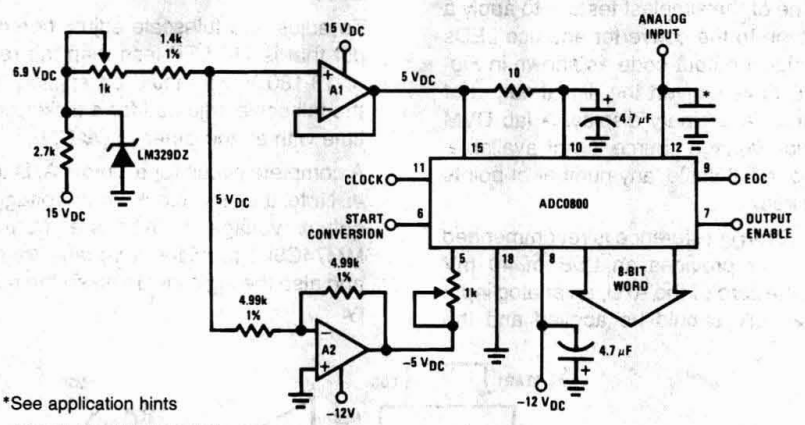
Typical Applications (Continued)

$V_{REF} = 10\ V_{DC}$ With TTL Logic Levels

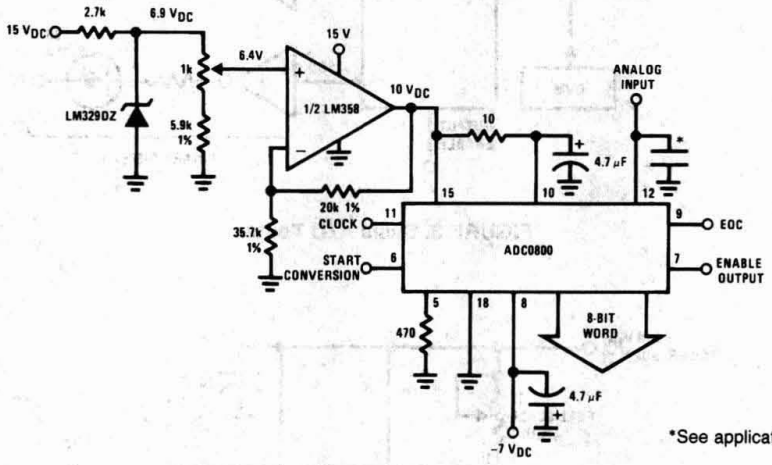


*See application hints

A1 and A2 = LM358N dual op amp

TL/H/5670–13

$V_{REF} = 10\ V_{DC}$ With 10V CMOS Logic Levels



*See application hints

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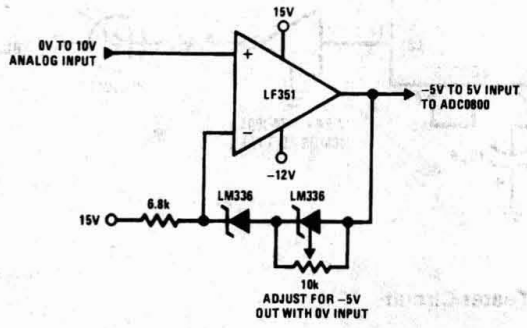
Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^-).

TL/H/5670–5

Typical Applications (Continued)

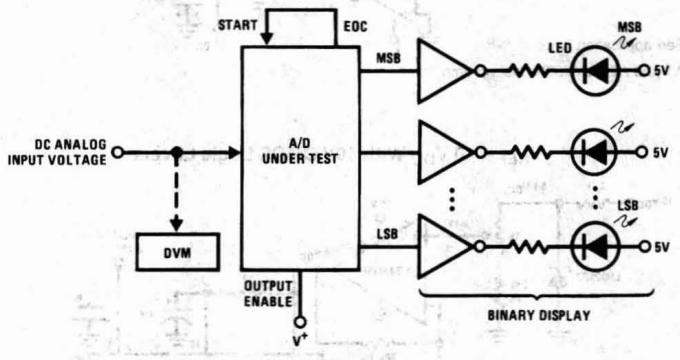
TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 3*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of ½ LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

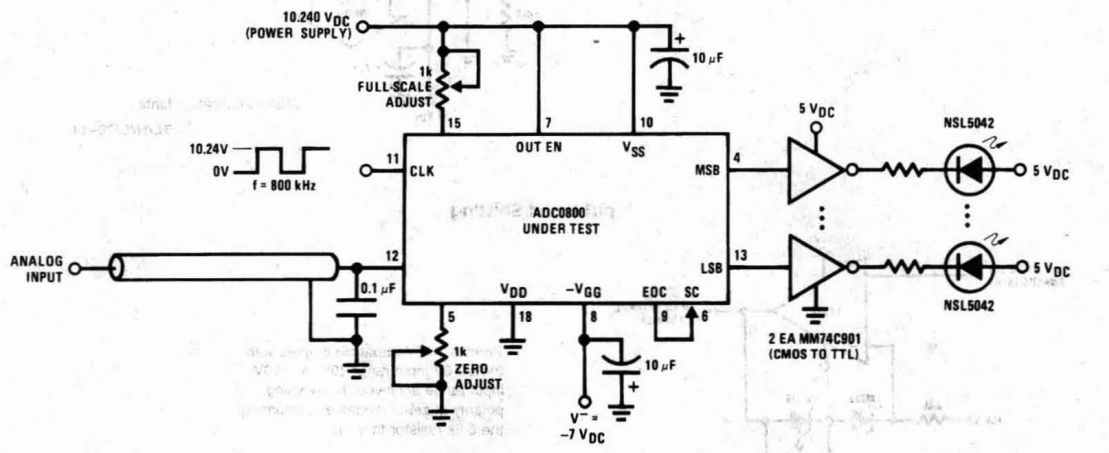
To adjust the full-scale adjust potentiometer, an analog input that is 1½ LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 4*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.



TL/H/5670–15

FIGURE 3. Basic A/D Tester



TL/H/5670–7

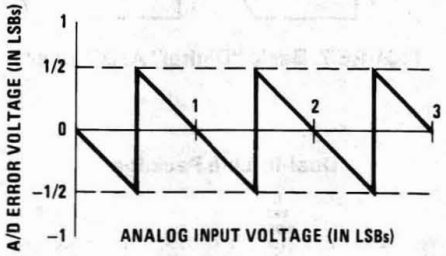
FIGURE 4. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.280 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by $\pm\frac{1}{2}$ LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 5* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
					MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1	1	1	1	15/16	15/256	9.600	0.600
E	1	1	1	0	7/8	7/128	8.960	0.560
D	1	1	0	1	13/16	13/256	8.320	0.520
C	1	1	0	0	3/4	3/64	7.680	0.480
B	1	0	1	1	11/16	11/256	7.040	0.440
A	1	0	1	0	5/8	5/128	6.400	0.400
9	1	0	0	1	9/16	9/256	5.760	0.360
8	1	0	0	0	1/2	1/32	5.120	0.320
7	0	1	1	1	7/16	7/256	4.480	0.280
6	0	1	1	0	3/8	3/128	3.840	0.240
5	0	1	0	1	5/16	5/256	3.200	0.200
4	0	1	0	0	1/4	1/64	2.560	0.160
3	0	0	1	1	3/16	3/256	1.920	0.120
2	0	0	1	0	1/8	1/128	1.280	0.080
1	0	0	0	1	1/16	1/256	0.640	0.040
0	0	0	0	0			0	0



TL/H/5670–8

FIGURE 5. Error Plot of a Perfect A/D Showing Effects of Quantization Error

Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 6*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A−C".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 7* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

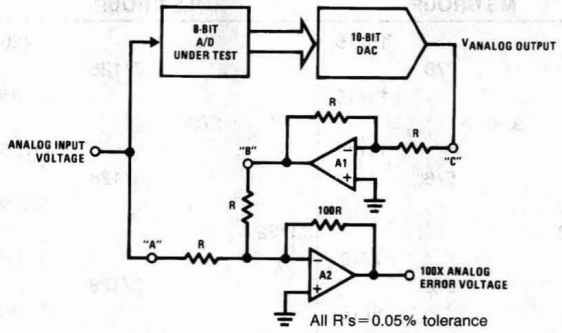


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FIGURE 6. A/D Tester with Analog Error Output

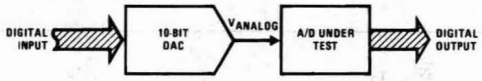

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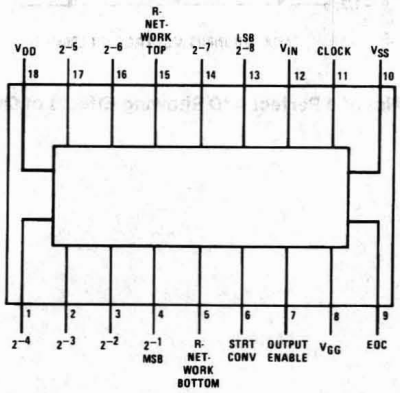
FIGURE 7. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



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Top View

Order Number ADC0800PD
or ADC0800PCD
See NS Package Number D18A

National Semiconductor

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

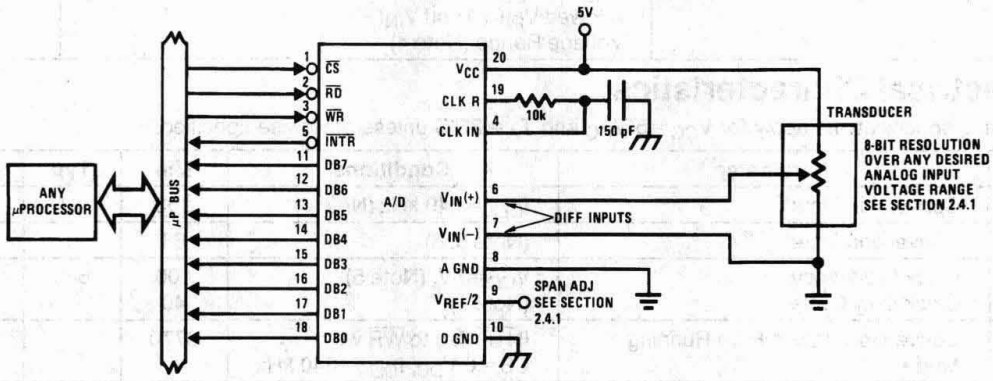
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3″ standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



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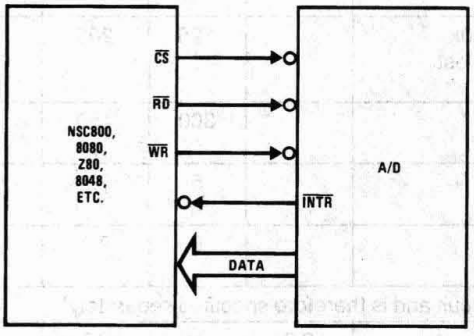
8080 Interface



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Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	**Full-Scale Adjusted**	**$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)**	**$V_{REF}/2$ = No Connection (No Adjustments)**
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 $I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0$ mA, $V_{CC} = 4.75\ V_{DC}$			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640$ kHz, $V_{REF}/2 =$ NC, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK} = 640$ kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

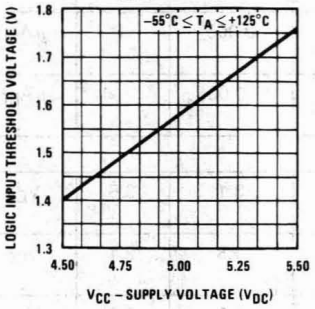
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

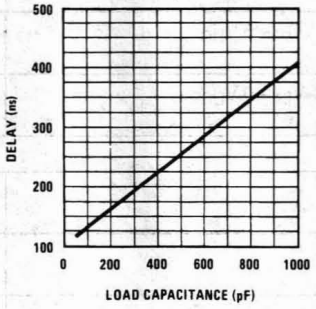
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

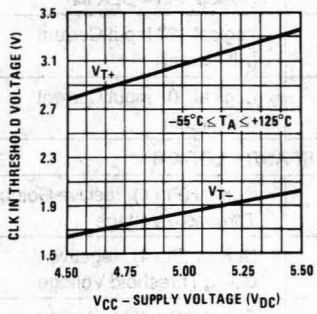
Logic Input Threshold Voltage vs. Supply Voltage



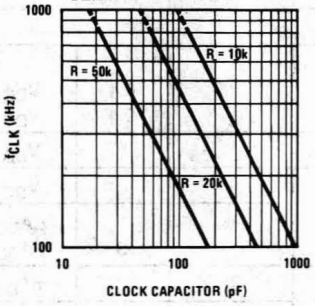
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



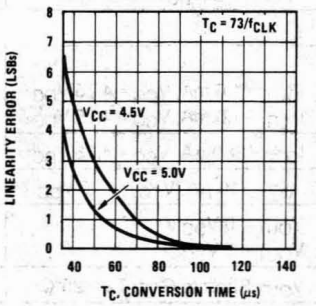
CLK IN Schmitt Trip Levels vs. Supply Voltage



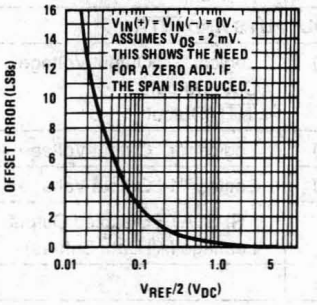
f_{CLK} vs. Clock Capacitor



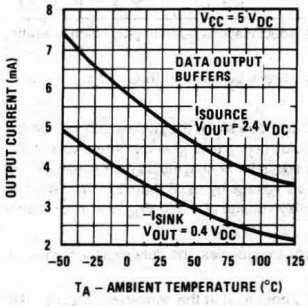
Full-Scale Error vs Conversion Time



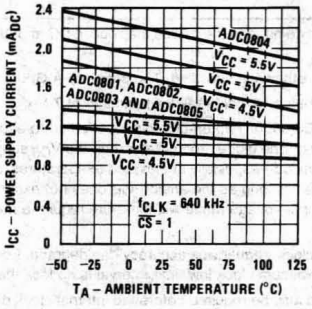
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



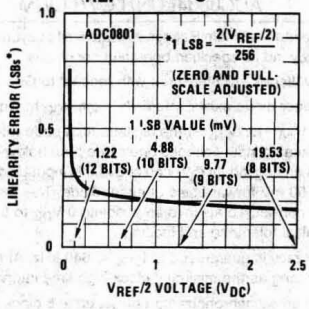
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

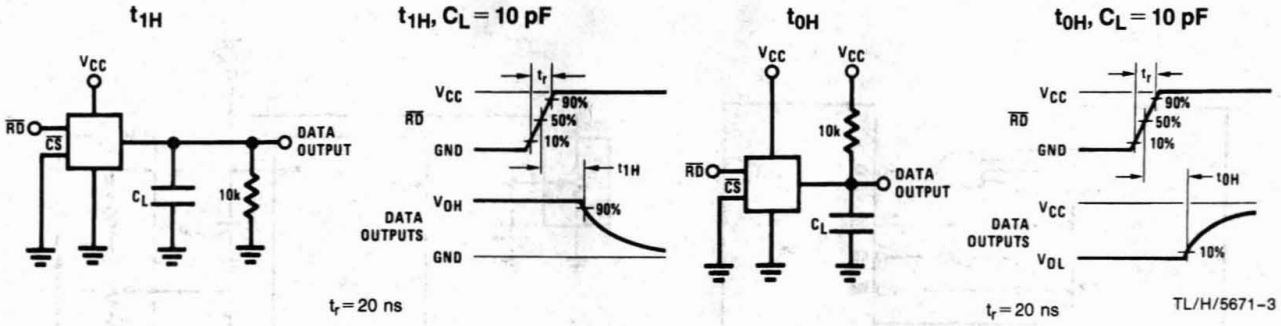


Linearity Error at Low $V_{REF}/2$ Voltages



TL/H/5671–2

TRI-STATE Test Circuits and Waveforms



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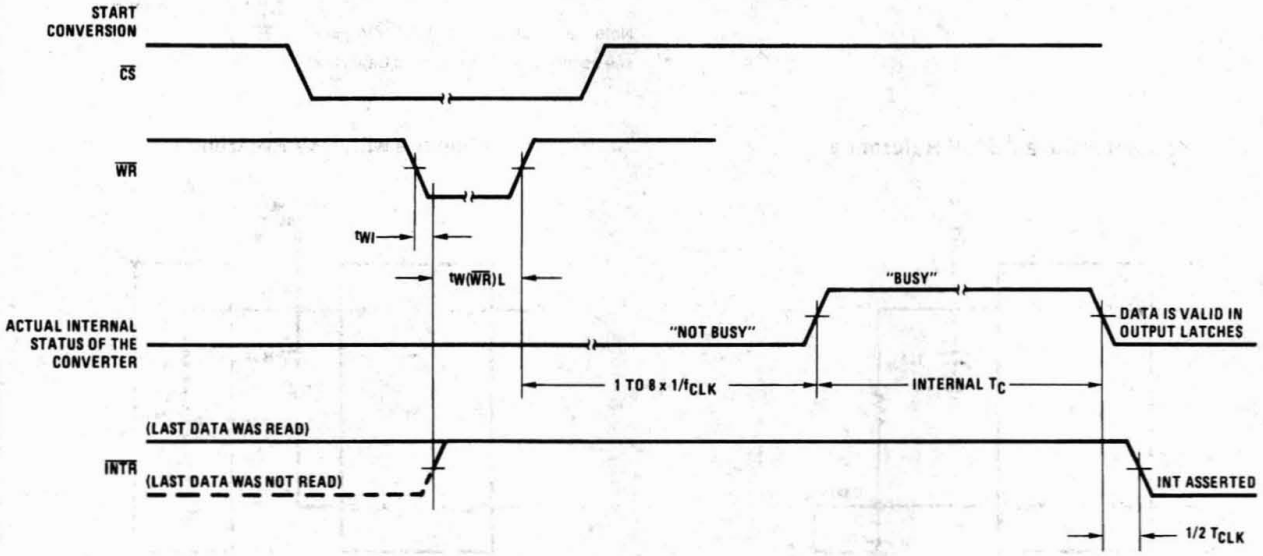
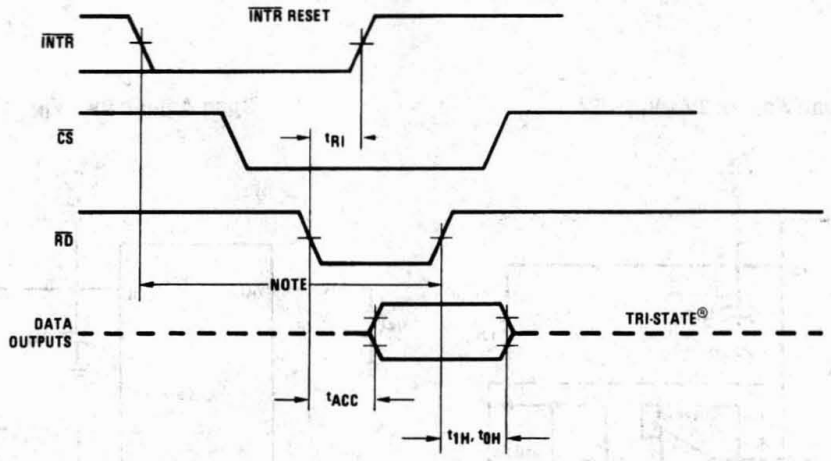
Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$



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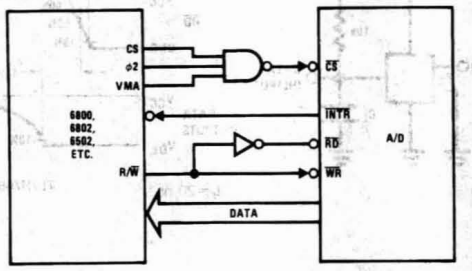
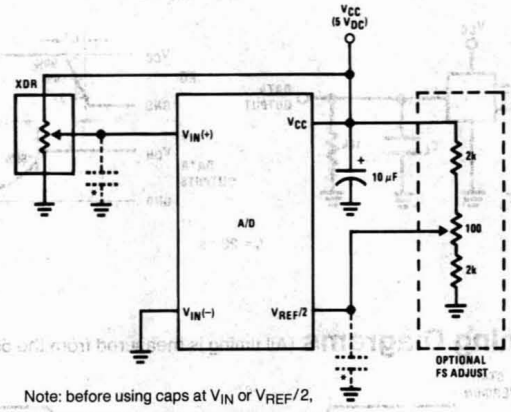
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications (Continued)

6800 Interface

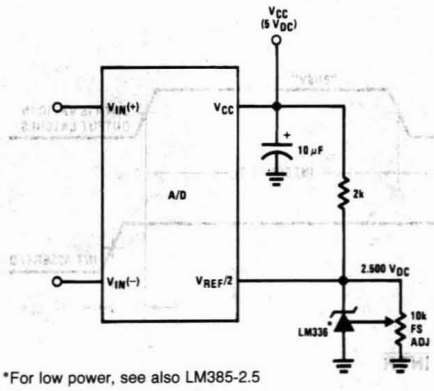


Ratiometric with Full-Scale Adjust



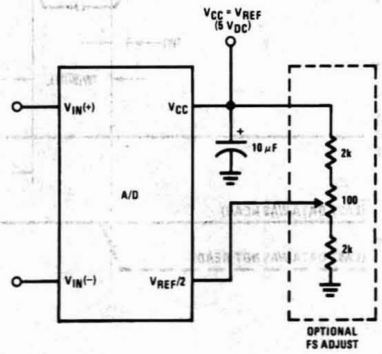
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

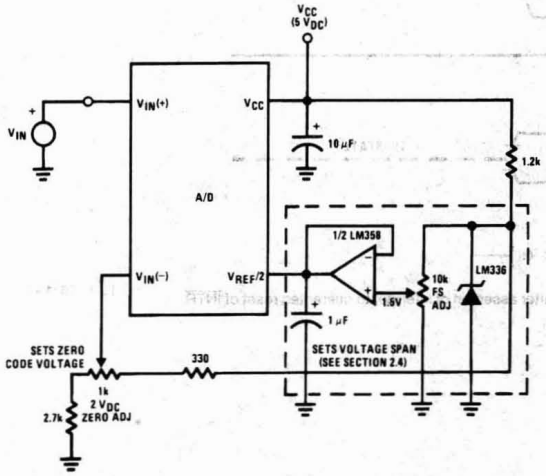


*For low power, see also LM385-2.5

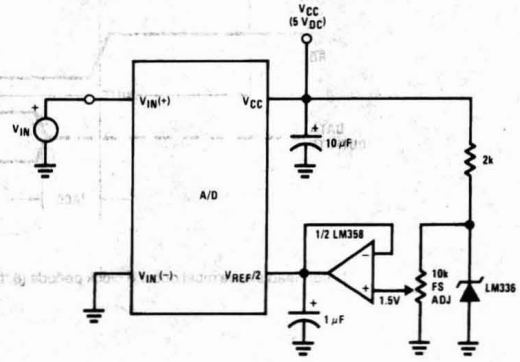
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



Span Adjust: $0V \leq V_{IN} \leq 3V$



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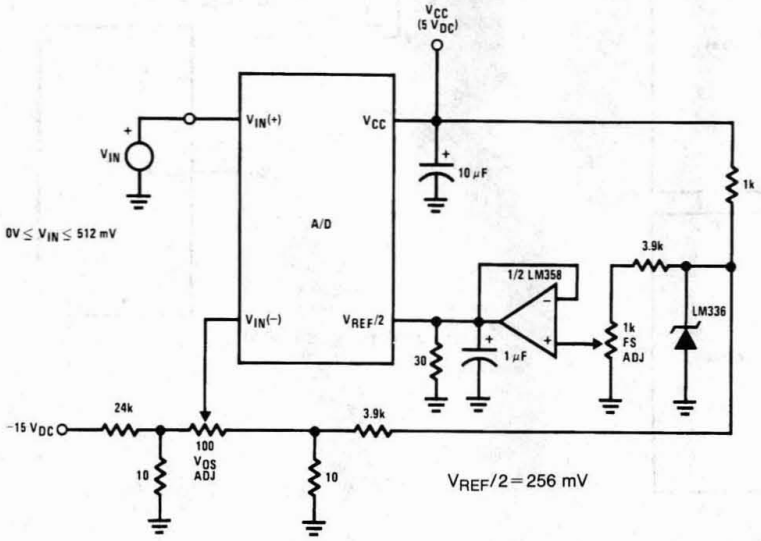
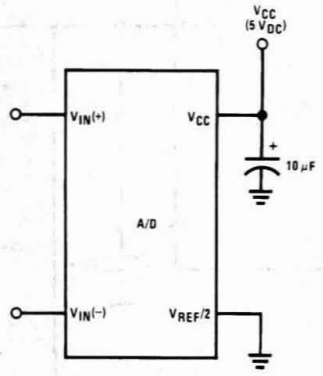
Typical Applications (Continued)

Directly Converting a Low-Level Signal



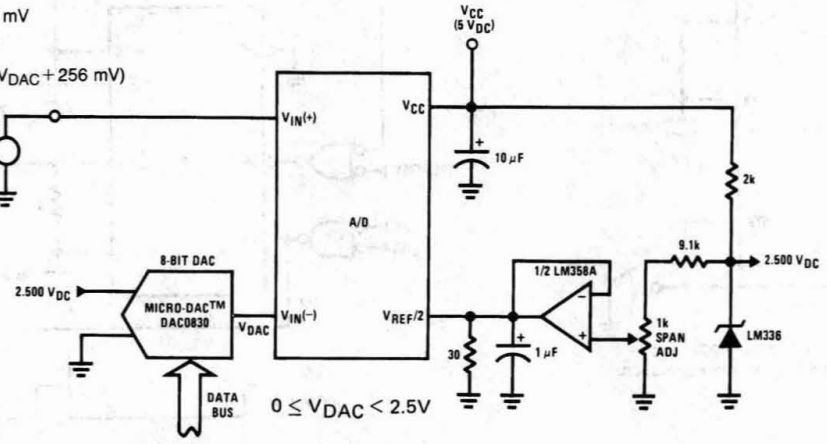
A μP Interfaced Comparator



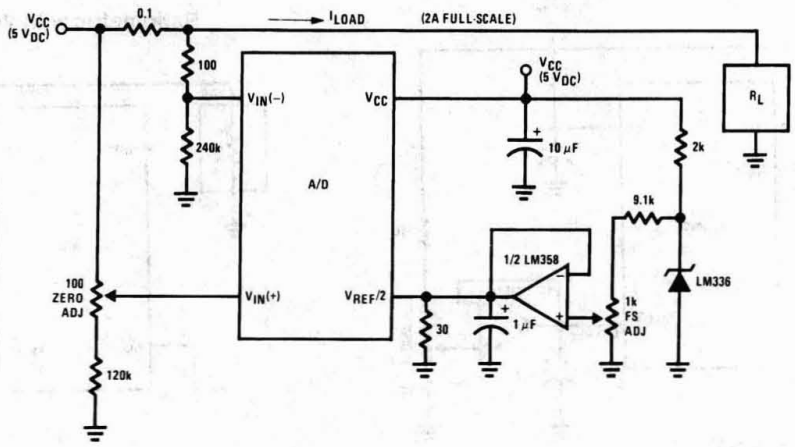
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with μP Controlled Range

$V_{REF}/2$ = 128 mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256\ mV)$



Digitizing a Current Flow



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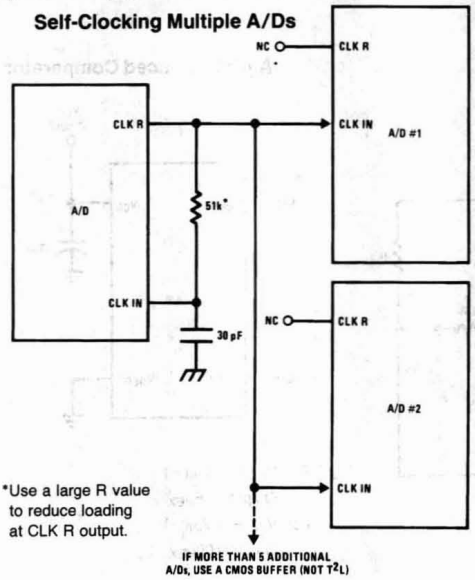
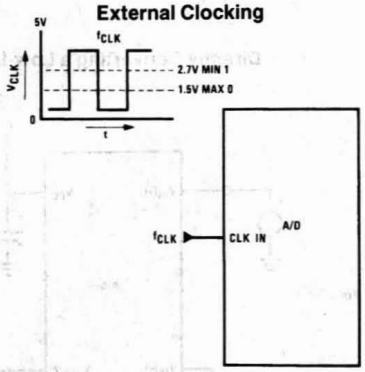
Typical Applications (Continued)

Self-Clocking Multiple A/Ds

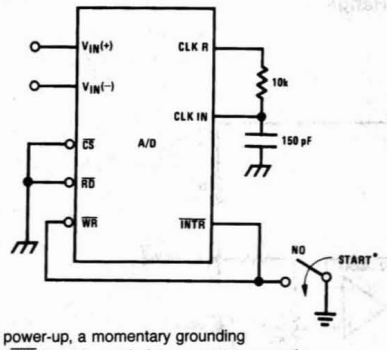


External Clocking



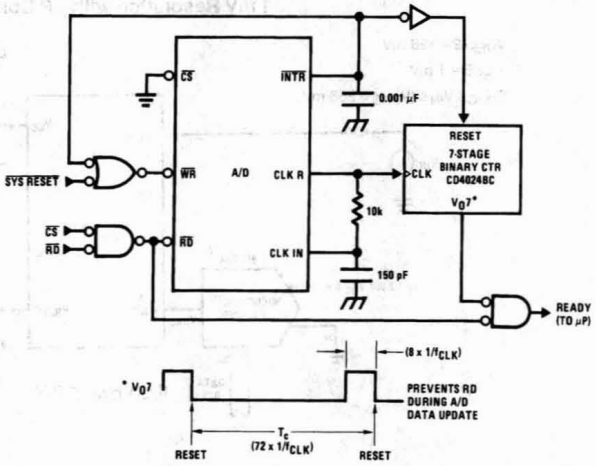
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

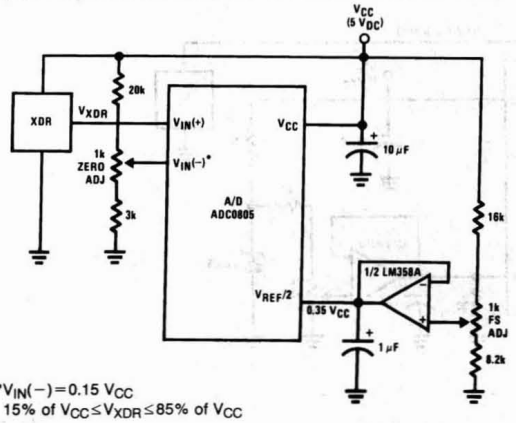


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

μP Interface for Free-Running A/D

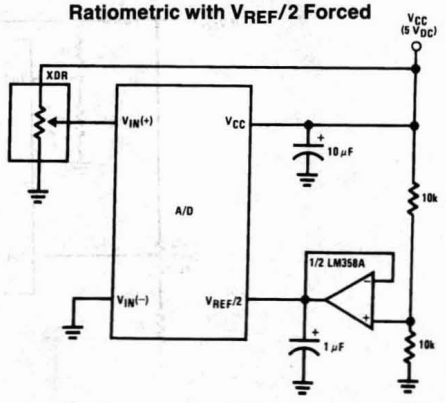


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



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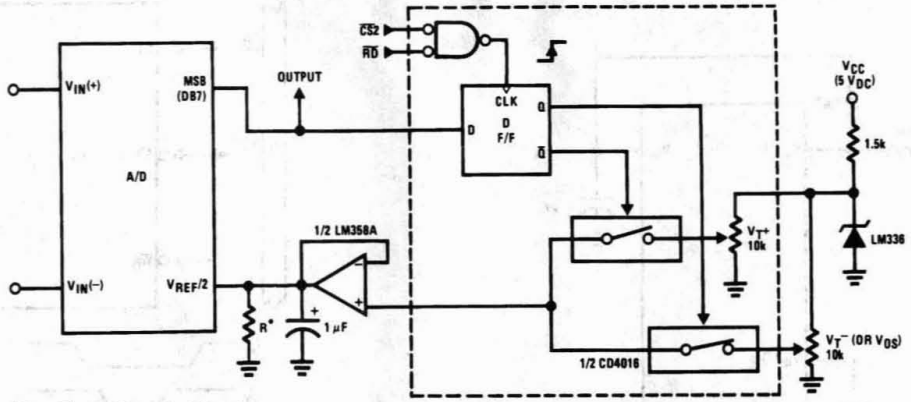
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

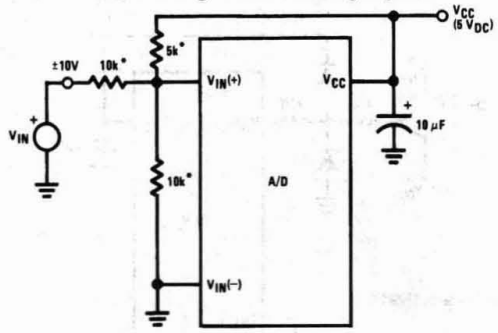


*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

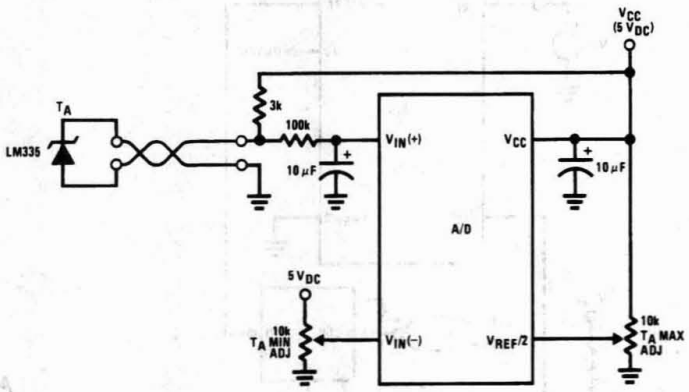
Omit circuitry within the dotted area if hysteresis is not needed

Handling ± 10V Analog Inputs

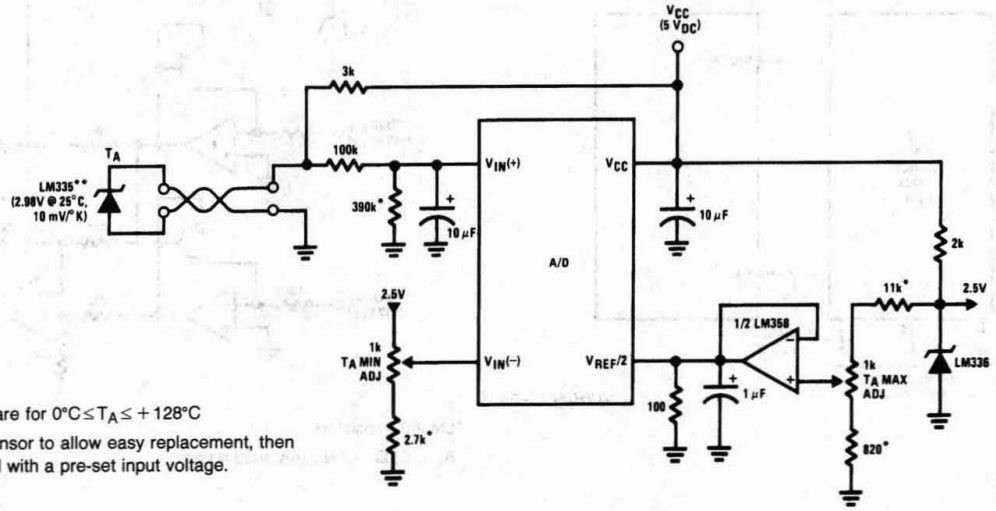


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter



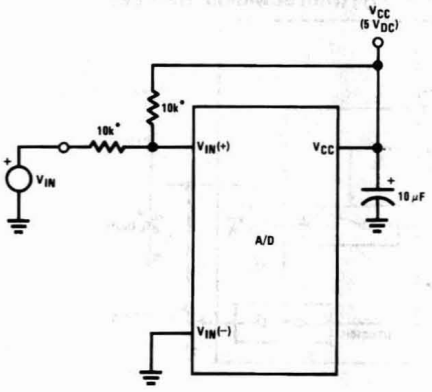
*Circuit values shown are for $0°C \leq T_A \leq +128°C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

TL/H/5671–8

Typical Applications (Continued)

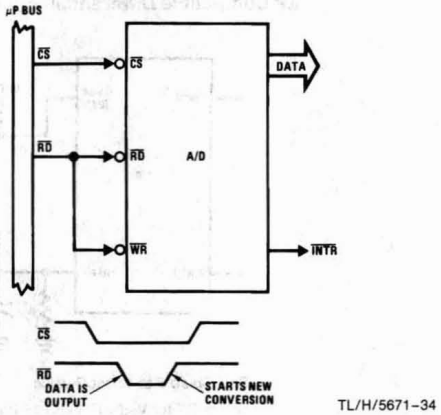
Handling ±5V Analog Inputs



TL/H/5671–33

*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



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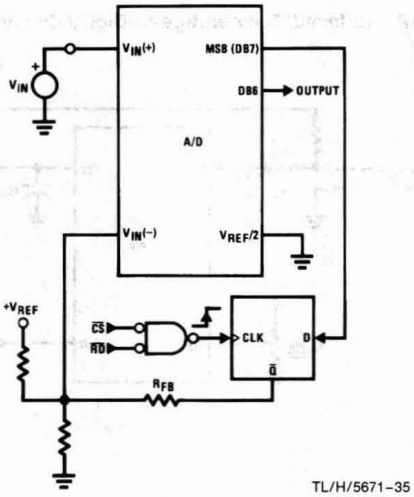
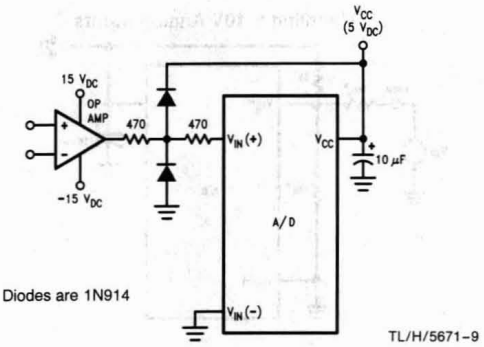
μP Interfaced Comparator with Hysteresis



TL/H/5671–35

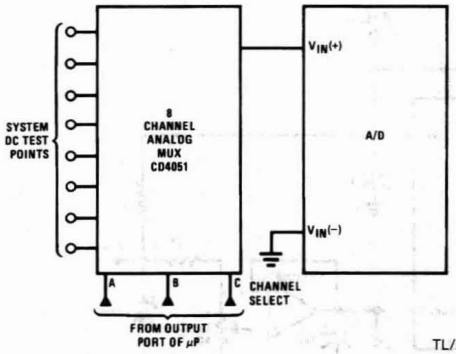
Protecting the Input



Diodes are 1N914

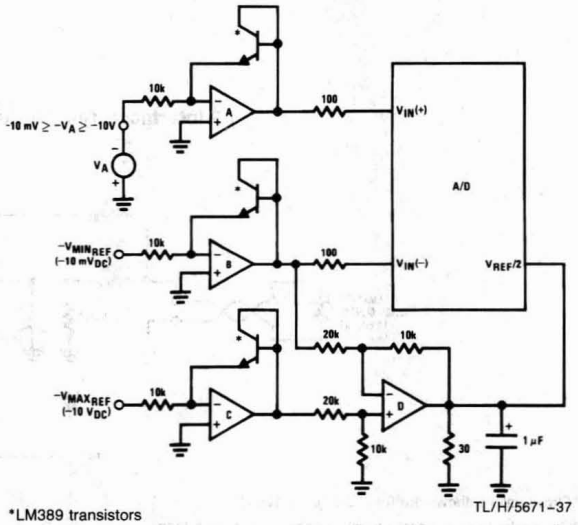
TL/H/5671–9

Analog Self-Test for a System



TL/H/5671–36

A Low-Cost, 3-Decade Logarithmic Converter



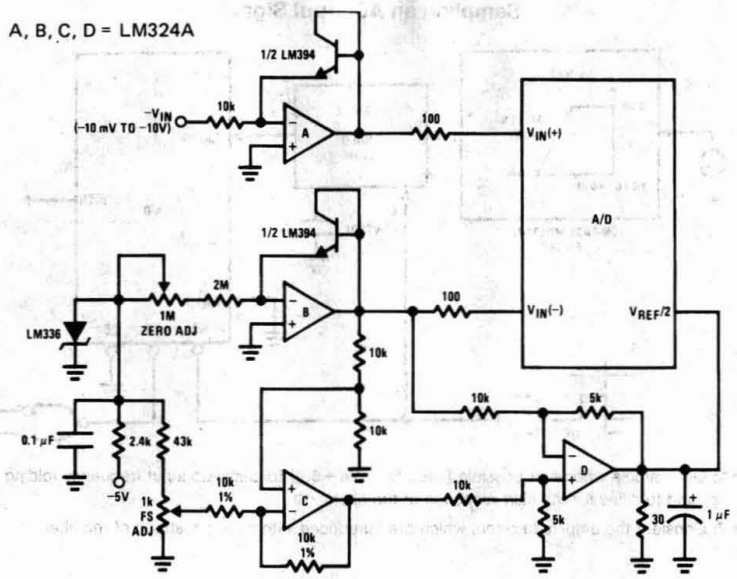
TL/H/5671–37

*LM389 transistors

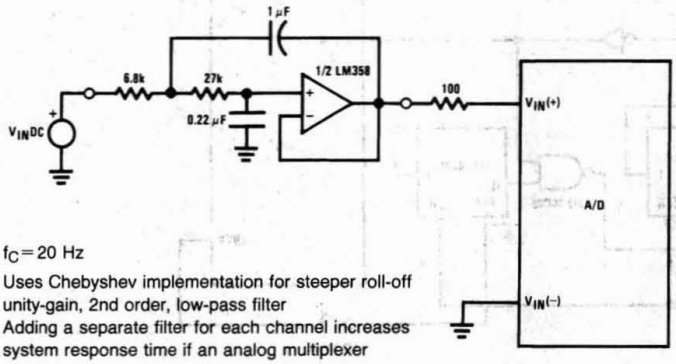
A, B, C, D = LM324A quad op amp

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



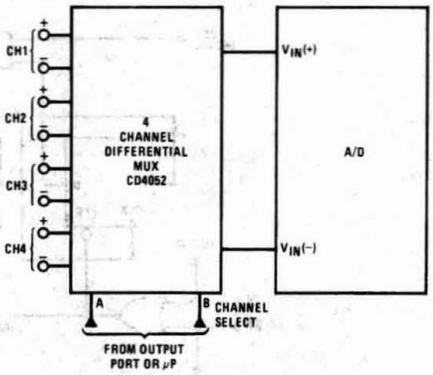
Noise Filtering the Analog Input



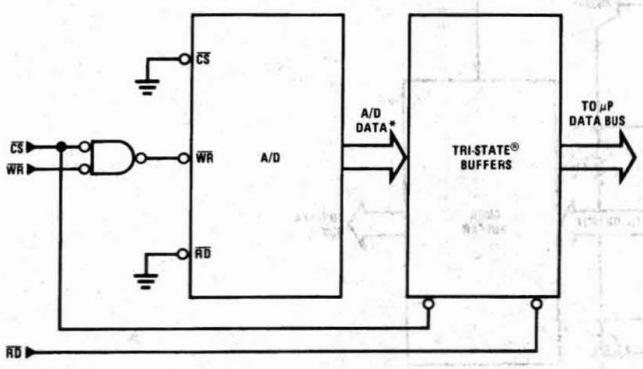
$f_C = 20$ Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

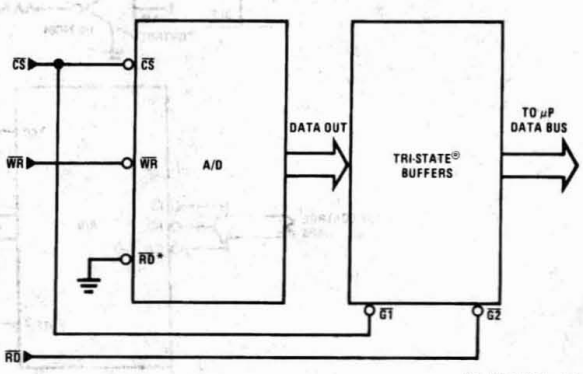


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

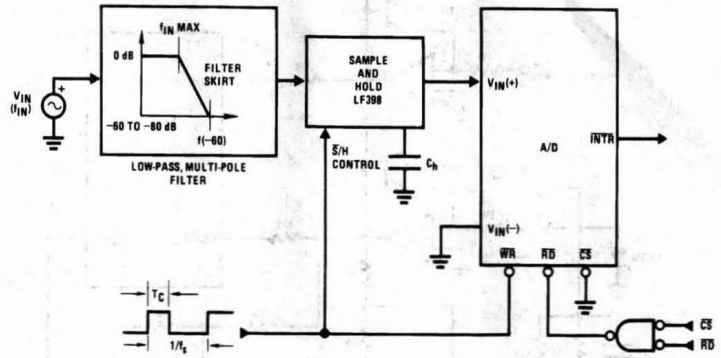


TL/H/5671–10

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

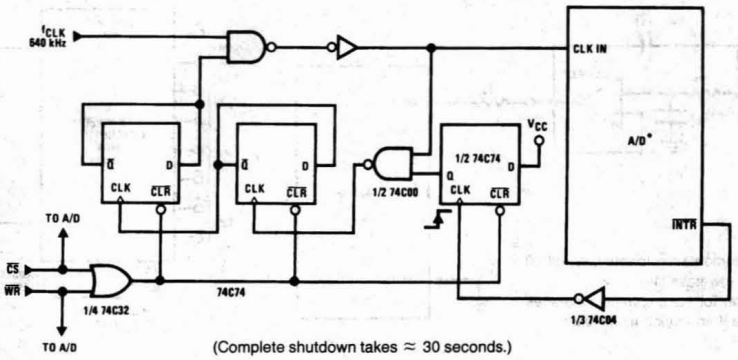
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

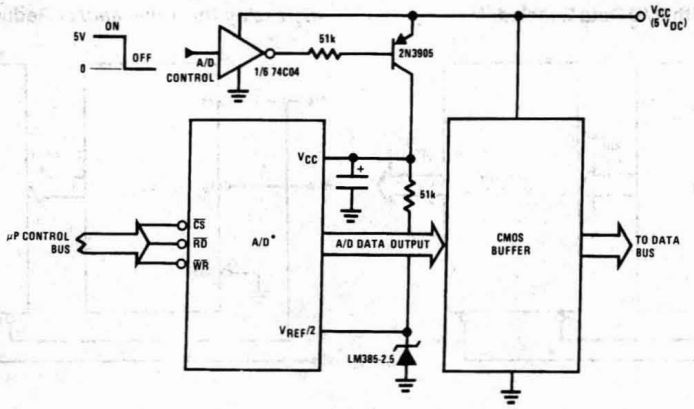
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

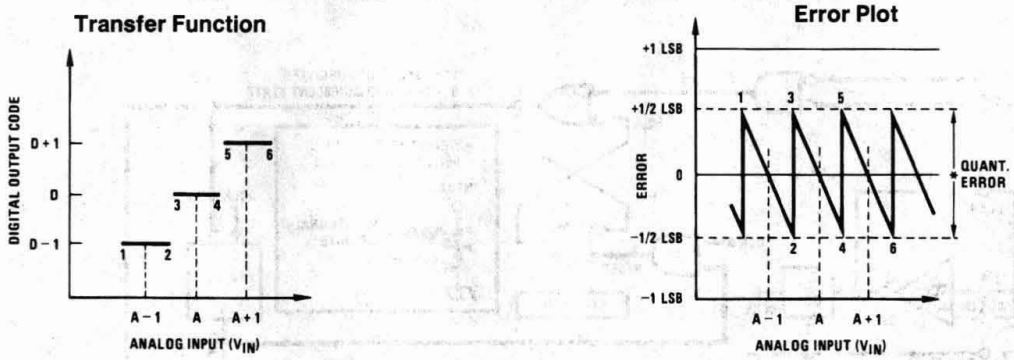
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

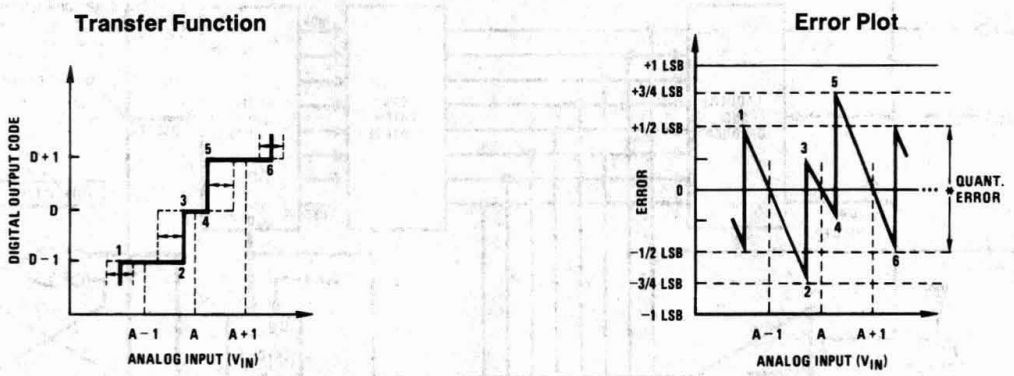
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

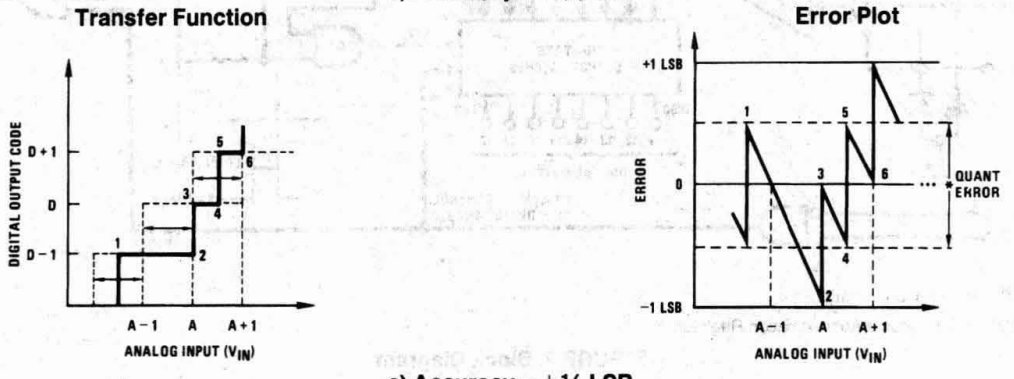
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB: A Perfect A/D



b) Accuracy = ±¼ LSB



c) Accuracy = ±½ LSB

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FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description (Continued)

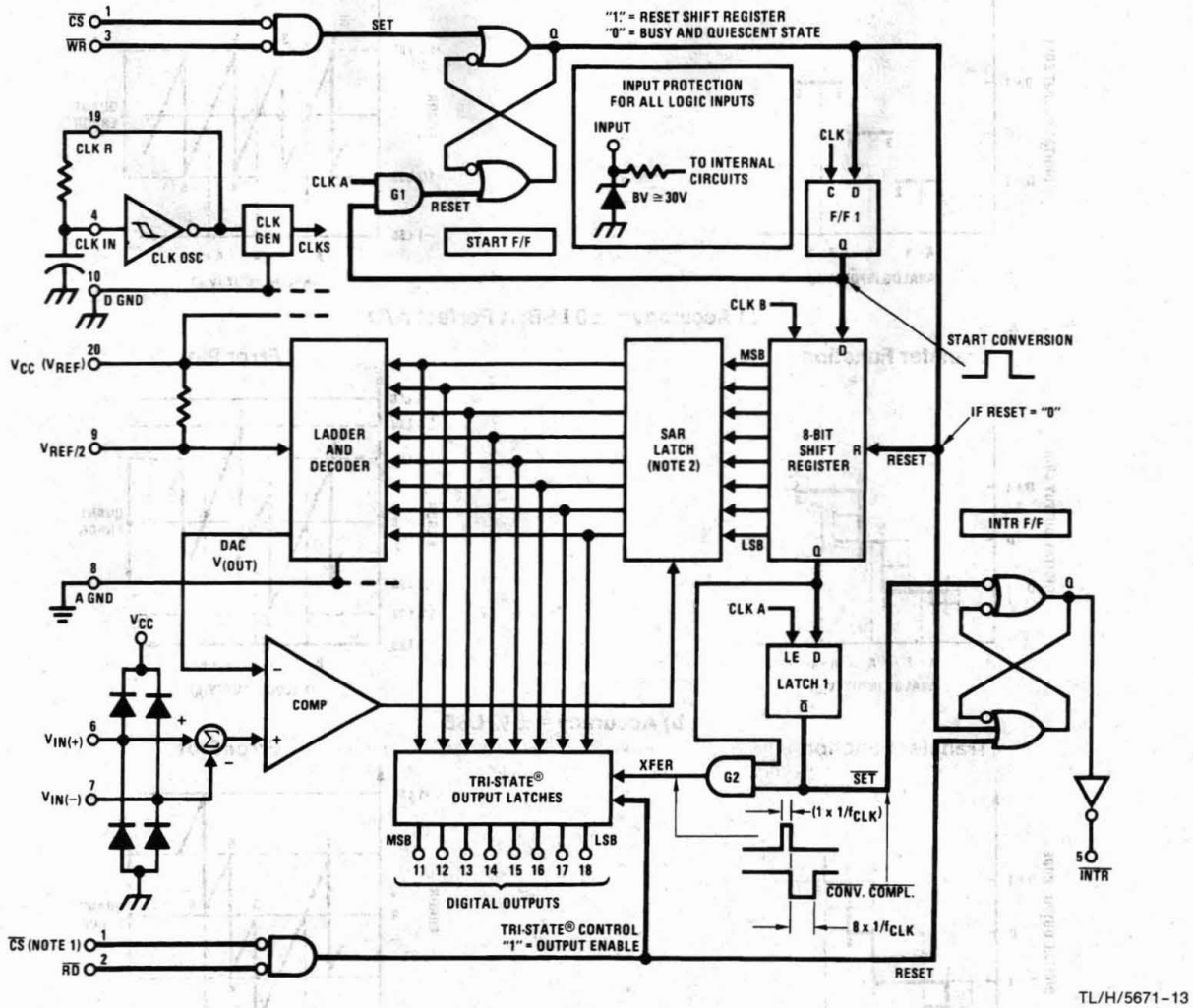
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



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Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^{2}L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

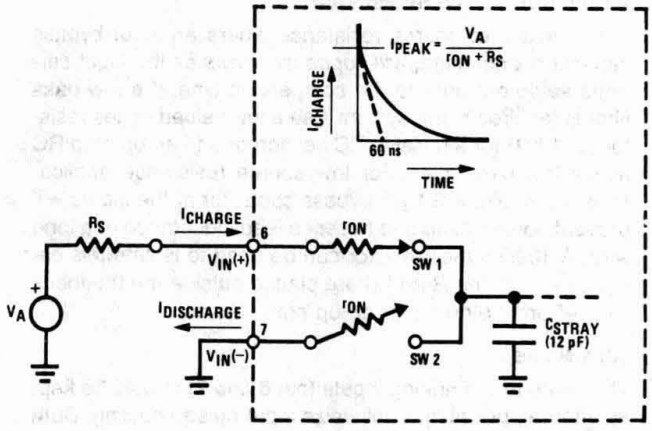
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



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r_{ON} of SW 1 and SW 2 ≅ 5 kΩ

$r = r_{ON} C_{STRAY} \cong 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

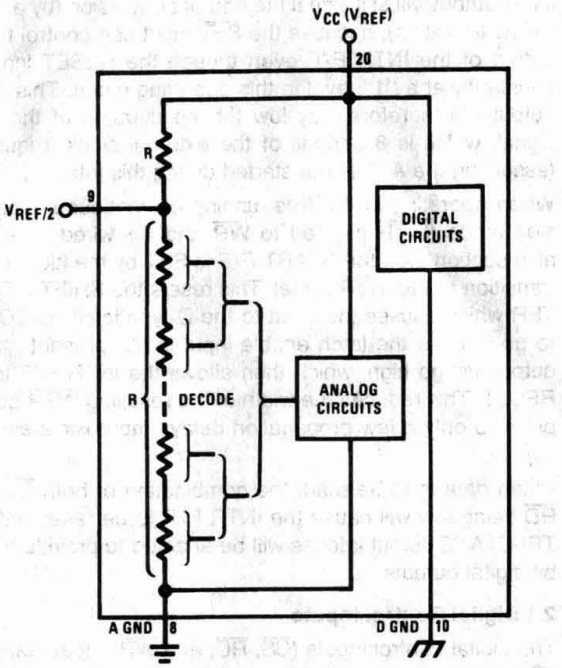

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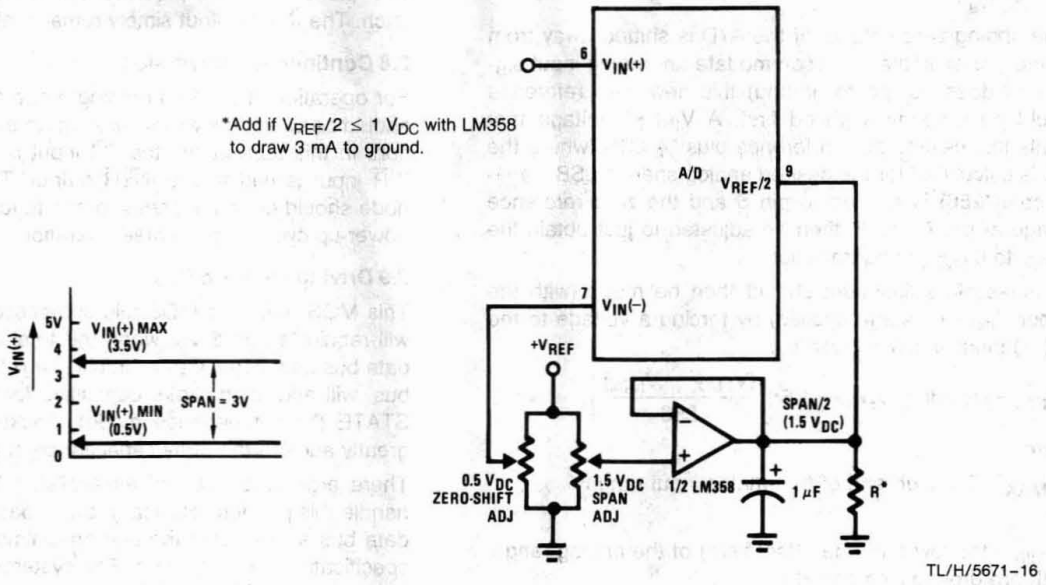
FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

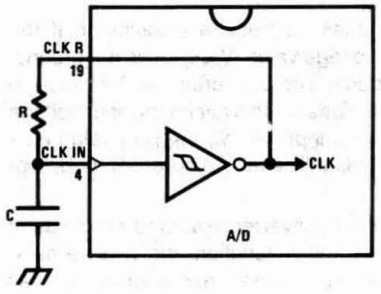
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$$R \cong 10\ k\Omega$$

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FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

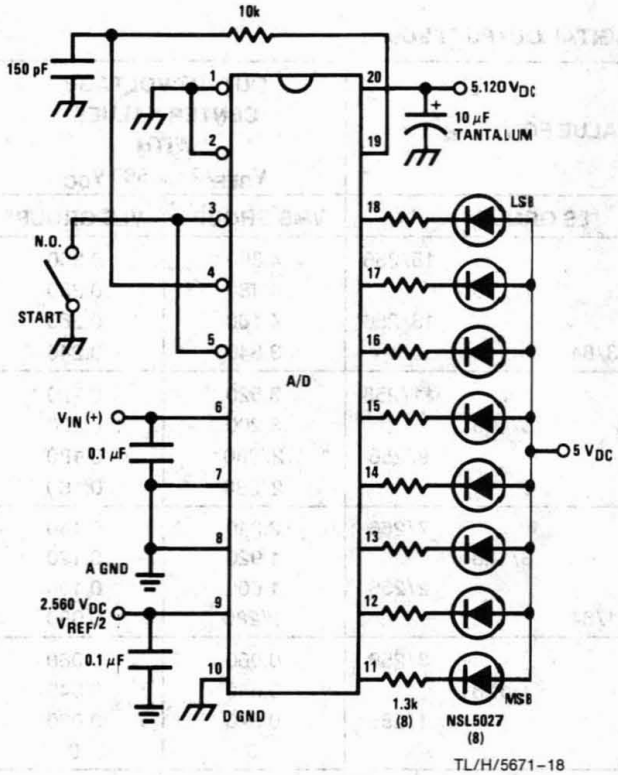

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FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Functional Description (Continued)

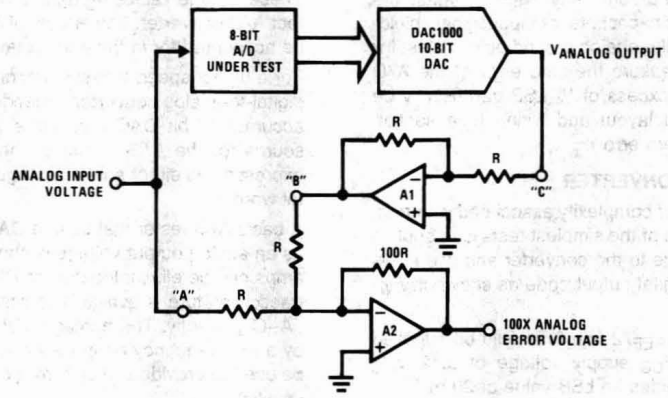

FIGURE 8. A/D Tester with Analog Error Output

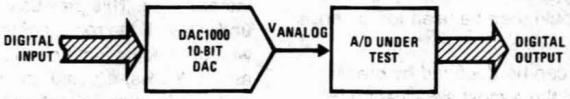

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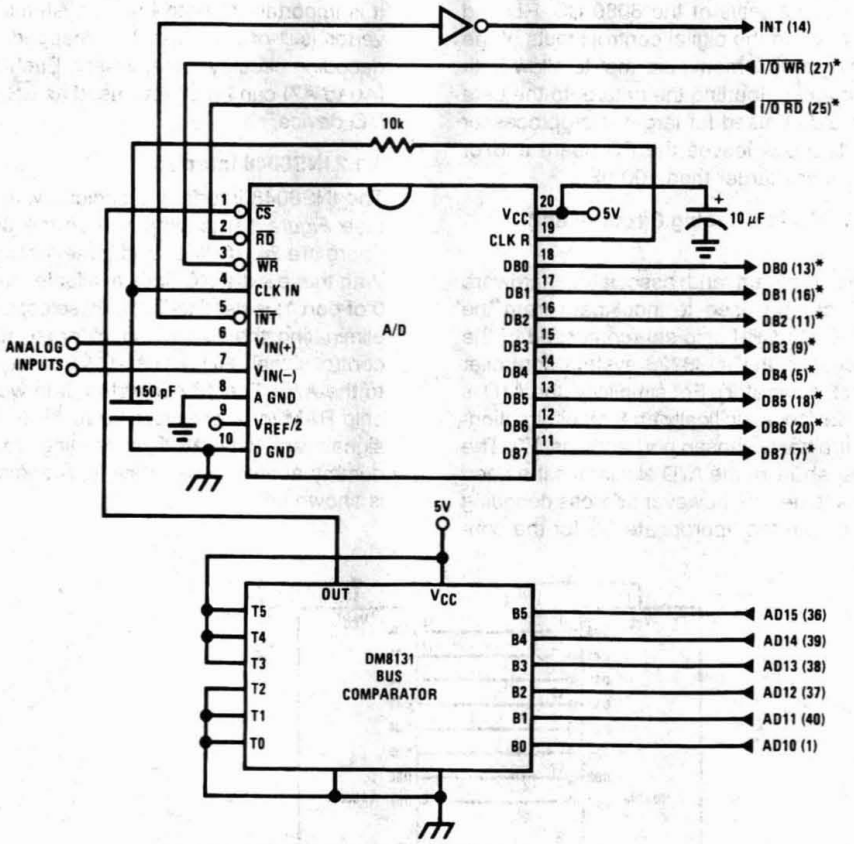
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2/880	0.180
8	1 0 0 0	1/2	1/32	2/560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1/280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*Display Output = VMS Group + VLS Group

Functional Description (Continued)



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Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:          JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:          LXI H 0200H         ; HL pair will point to
                                                        ; data storage locations
0103    31 00 04    RETURN:         LXI SP 0400H        ; Initialize stack pointer (Note 1)
0106    7D                          MOV A, L            ; Test # of bytes entered
0107    FE 0F                       CPI 0F H            ; If # = 16. JMP to
0109    CA 13 01                    JZ CONT             ; user program
010C    D3 E0                       OUT E0 H            ; Start A/D
010E    FB                          EI                  ; Enable interrupt
010F    00          LOOP:           NOP                 ; Loop until end of
0110    C3 0F 01                    JMP LOOP            ; conversion
0113      •         CONT:             •
  •       •           •               •
  •       •         (User program to  •
  •       •         process data)     •
  •       •           •               •
  •       •           •               •
0300    DB E0       LD DATA:        IN E0 H             ; Load data into accumulator
0302    77                          MOV M, A            ; Store data
0303    23                          INX H               ; Increment storage pointer
0304    C3 03 01                    JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

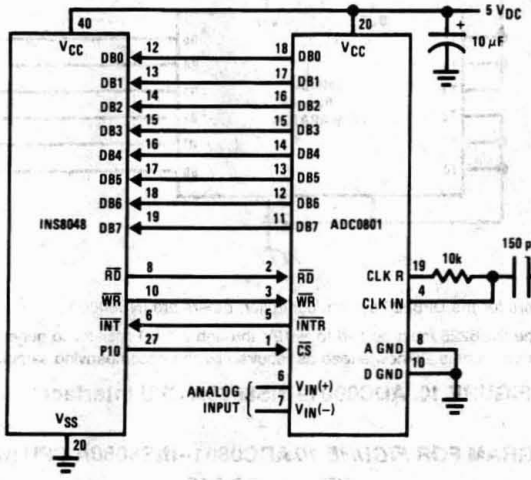

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                JMP     10H          ; Program starts at addr 10
                     ORG     3H
04 50                JMP     50H          ; Interrupt jump vector
                     ORG     10H          ; Main program
99 FE                ANL     P1, #0FEH    ; Chip select
81                   MOVX    A, @R1       ; Read in the 1st data
                                          ; to reset the intr
89 01      START:    ORL     P1, #1       ; Set port pin high
B8 20                MOV     R0, #20H     ; Data address
B9 FF                MOV     R1, #0FFH    ; Dummy address
BA 10                MOV     R2, #10H     ; Counter for 16 bytes
23 FF      AGAIN:    MOV     A, #0FFH     ; Set ACC for intr loop
99 FE                ANL     P1, #0FEH    ; Send CS (bit 0 of P1)
91                   MOVX    @R1, A       ; Send WR out
05                   EN      I            ; Enable interrupt
96 21      LOOP:     JNZ     LOOP         ; Wait for interrupt
EA 1B                DJNZ    R2, AGAIN    ; If 16 bytes are read
00                   NOP                  ; go to user's program
00                   NOP
                     ORG     50H
81         INDATA:   MOVX    A, @R1       ; Input data, CS still low
A0                   MOV     @R0, A       ; Store in memory
18                   INC     R0           ; Increment storage counter
89 01                ORL     P1, #1       ; Reset CS signal
27                   CLR     A            ; Clear ACC to get out of
93                   RETR                 ; the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

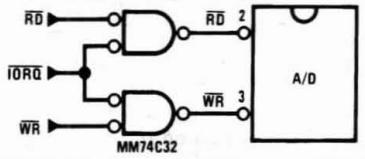

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FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

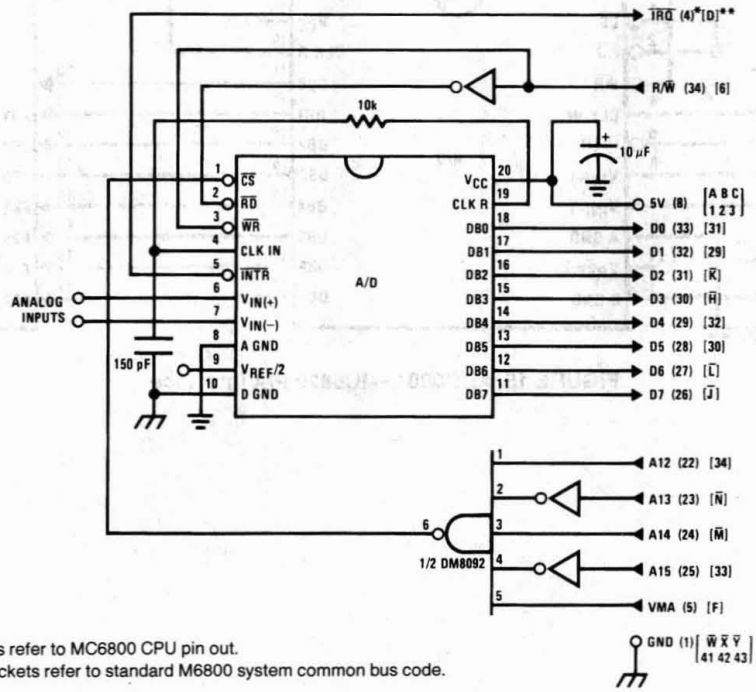
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.
Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

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FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010    DF 36       DATAIN   STX    TEMP2     ;Save contents of X
0012    CE 00 2C             LDX    #$002C    ;Upon IRQ low CPU
0015    FF FF F8             STX    $FFF8     ;jumps to 002C
0018    B7 50 00             STAA   $5000     ;Start ADC0801
001B    0E                   CLI
001C    3E          CONVRT   WAI               ;Wait for interrupt
001D    DE 34                LDX    TEMP1
001F    8C 02 0F             CPX    #$020F    ;Is final data stored?
0022    27 14                BEQ    ENDP
0024    B7 50 00             STAA   $5000     ;Restarts ADC0801
0027    08                   INX
0028    DF 34                STX    TEMP1
002A    20 F0                BRA    CONVRT
002C    DE 34       INTRPT   LDX    TEMP1
002E    B6 50 00             LDAA   $5000     ;Read data
0031    A7 00                STAA   X         ;Store it at X
0033    3B                   RTI
0034    02 00       TEMP1    FDB    $0200     ;Starting address for
                                               ;data storage
0036    00 00       TEMP2    FDB    $0000
0038    CE 02 00    ENDP     LDX    #$0200    ;Reinitialize TEMP1
003B    DF 34                STX    TEMP1
003D    DE 36                LDX    TEMP2
003F    39                   RTS               ;Return from subroutine
                                               ;To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

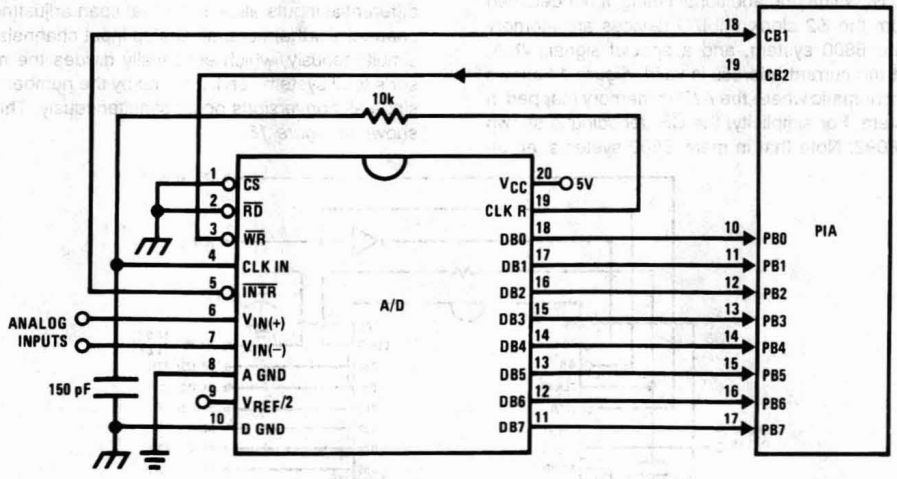

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FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010    CE 00 38    DATAIN    LDX    #$0038    ; Upon IRQ low CPU
0013    FF FF F8              STX    $FFF8     ; jumps to 0038
0016    B6 80 06              LDAA   PIAORB    ; Clear possible IRQ flags
0019    4F                    CLRA
001A    B7 80 07              STAA   PIACRB
001D    B7 80 06              STAA   PIAORB    ; Set Port B as input
0020    0E                    CLI
0021    C6 34                 LDAB   #$34
0023    86 3D                 LDAA   #$3D
0025    F7 80 07    CONVRT    STAB   PIACRB    ; Starts ADC0801
0028    B7 80 07              STAA   PIACRB
002B    3E                    WAI              ; Wait for interrupt
002C    DE 40                 LDX    TEMP1
002E    8C 02 0F              CPX    #$020F    ; Is final data stored?
0031    27 0F                 BEQ    ENDP
0033    08                    INX
0034    DF 40                 STX    TEMP1
0036    20 ED                 BRA    CONVRT
0038    DE 40       INTRPT    LDX    TEMP1
003A    B6 80 06              LDAA   PIAORB    ; Read data in
003D    A7 00                 STAA   X         ; Store it at X
003F    3B                    RTI
0040    02 00       TEMP1     FDB    $0200     ; Starting address for
                                                ; data storage
0042    CE 02 00    ENDP      LDX    #$0200    ; Reinitialize TEMP1
0045    DF 40                 STX    TEMP1
0047    39                    RTS              ; Return from subroutine
                    PIAORB    EQU    $8006     ; To user's program
                    PIACRB    EQU    $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

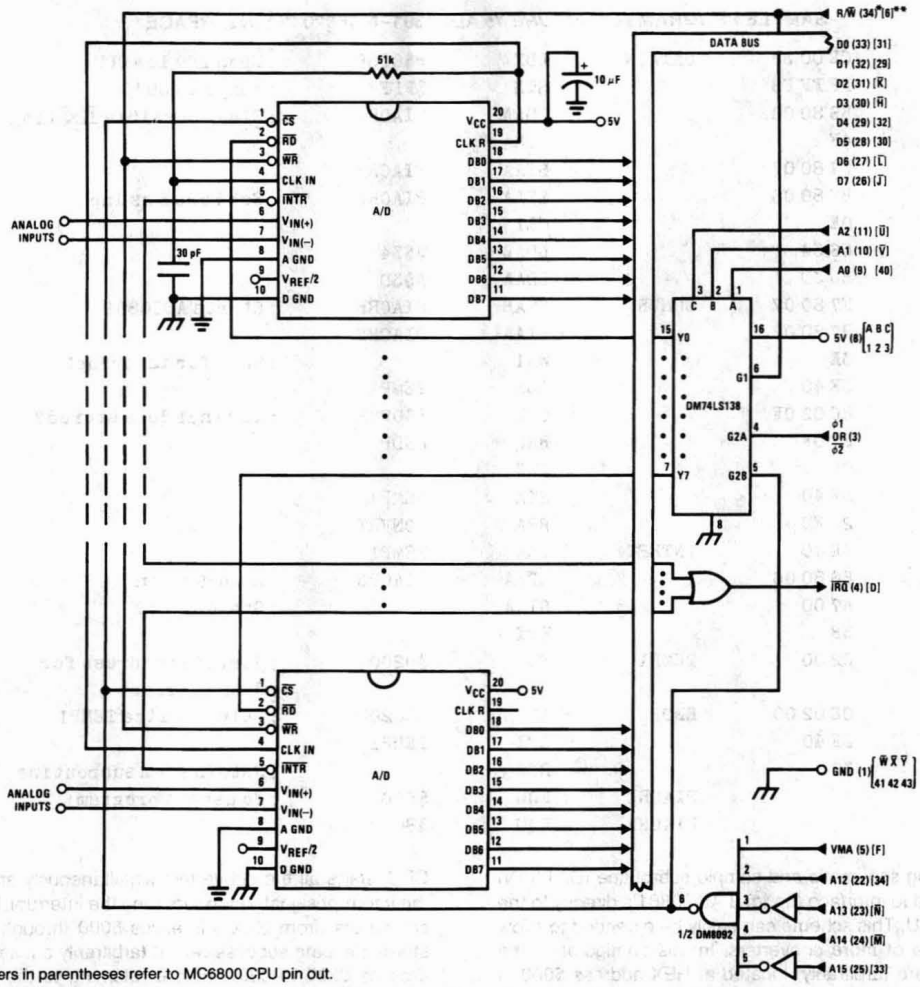
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for $\frac{1}{4}$ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

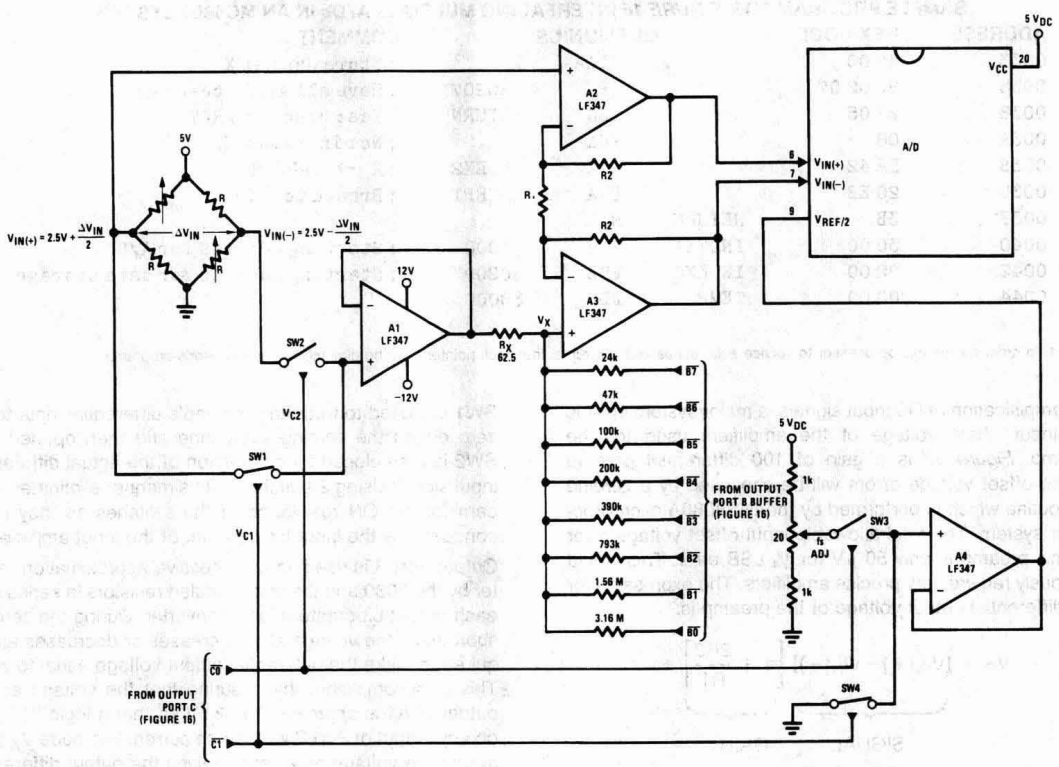
$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move $\pm$12 mV with a resolution of 50 μV, which will null the offset error term to $\frac{1}{4}$ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)



Note 1: R2 = 49.5 R1

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

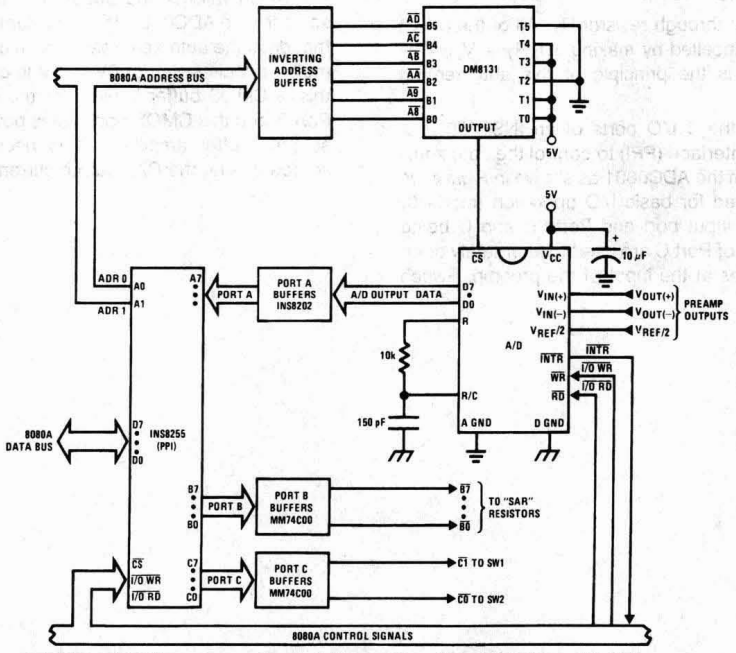


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FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

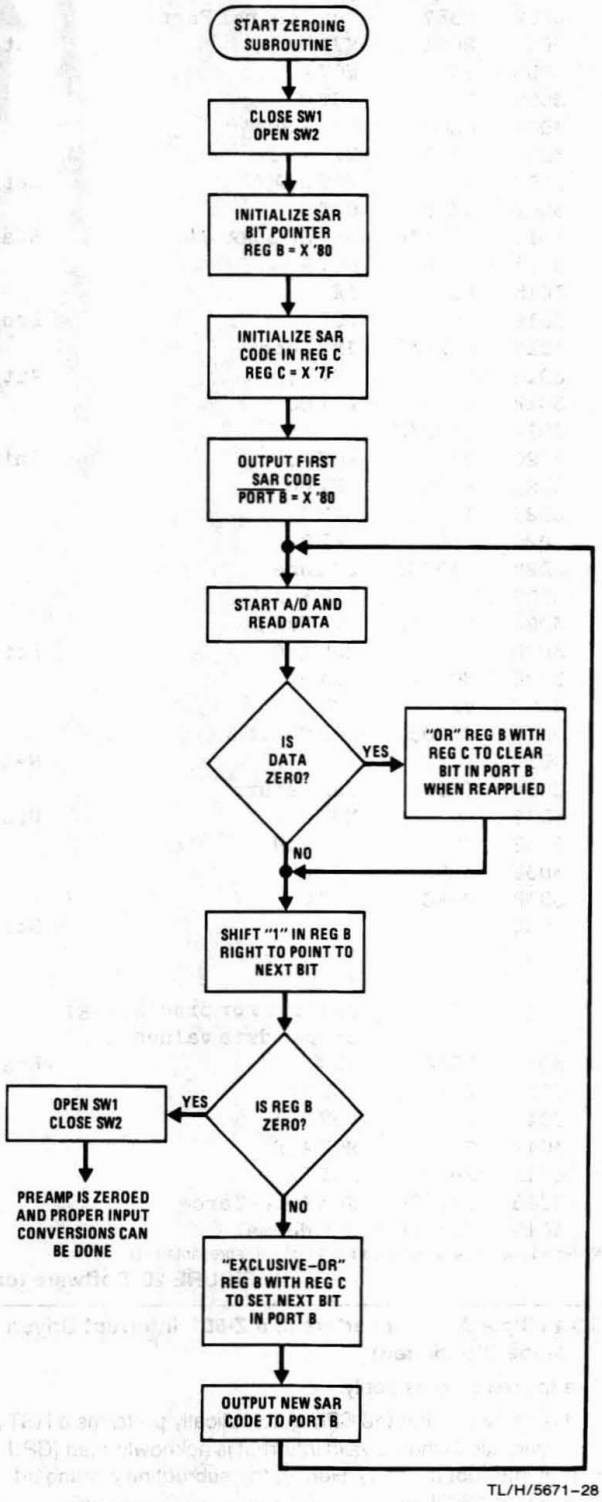
START ZEROING SUBROUTINE
CLOSE SW1 OPEN SW2
INITIALIZE SAR BIT POINTER REG B = X '80
INITIALIZE SAR CODE IN REG C REG C = X '7F
OUTPUT FIRST SAR CODE PORT B = X '80
START A/D AND READ DATA
IS DATA ZERO?
YES
"OR" REG B WITH REG C TO CLEAR BIT IN PORT B WHEN REAPPLIED
NO
SHIFT "1" IN REG B RIGHT TO POINT TO NEXT BIT
IS REG B ZERO?
YES
OPEN SW1 CLOSE SW2
PREAMP IS ZEROED AND PROPER INPUT CONVERSIONS CAN BE DONE
NO
"EXCLUSIVE-OR" REG B WITH REG C TO SET NEXT BIT IN PORT B
OUTPUT NEW SAR CODE TO PORT B

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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00   3E90     MVI 90
3D02   D3E7     Out Control Port                    ; Program PPI
3D04   2601     MVI H 01          Auto-Zero Subroutine
3D06   7C       MOV A,H
3D07   D3E6     OUT C                              ; Close SW1 open SW2
3D09   0680     MVI B 80                           ; Initialize SAR bit pointer
3D0B   3E7F     MVI A 7F                           ; Initialize SAR code
3D0D   4F       MOV C,A           Return
3D0E   D3E5     OUT B                              ; Port B = SAR code
3D10   31AA3D   LXI SP 3DAA       Start            ; Dimension stack pointer
3D13   D3E4     OUT A                              ; Start A/D
3D15   FB       IE
3D16   00       NOP               Loop             ; Loop until INT asserted
3D17   C3163D   JMP Loop
3D1A   7A       MOV A,D           Auto-Zero
3D1B   C600     ADI 00
3D1D   CA2D3D   JZ Set C                           ; Test A/D output data for zero
3D20   78       MOV A,B           Shift B
3D21   F600     ORI 00                             ; Clear carry
3D23   1F       RAR                                ; Shift "1" in B right one place
3D24   FE00     CPI 00                             ; Is B zero? If yes last
3D26   CA373D   JZ Done                            ; approximation has been made
3D29   47       MOV B,A
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C           Set C
3D2E   B0       ORA B                              ; Set bit in C that is in same
3D2F   4F       MOV C,A                            ; position as "1" in B
3D30   C3203D   JMP Shift B
3D33   A9       XRA C             New C            ; Clear bit in C that is in
3D34   C30D3D   JMP Return                         ; same position as "1" in B
3D37   47       MOV B,A           Done             ; then output new SAR code.
3D38   7C       MOV A,H                            ; Open SW1, close SW2 then
3D39   EE03     XRI 03                             ; proceed with program. Preamp
3D3B   D3E6     OUT C                              ; is now zeroed.
3D3D            •                 Normal
                •
                •
                Program for processing
                proper data values
3C3D   DBE4     IN A              Read A/D Subroutine  ; Read A/D data
3C3F   EEFF     XRI FF                             ; Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B                            ; Is B Reg = 0? If not stay
3C43   E6FF     ANI FF                             ; in auto zero subroutine
3C45   C21A3D   JNZ Auto-Zero
3C48   C33D3D   JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

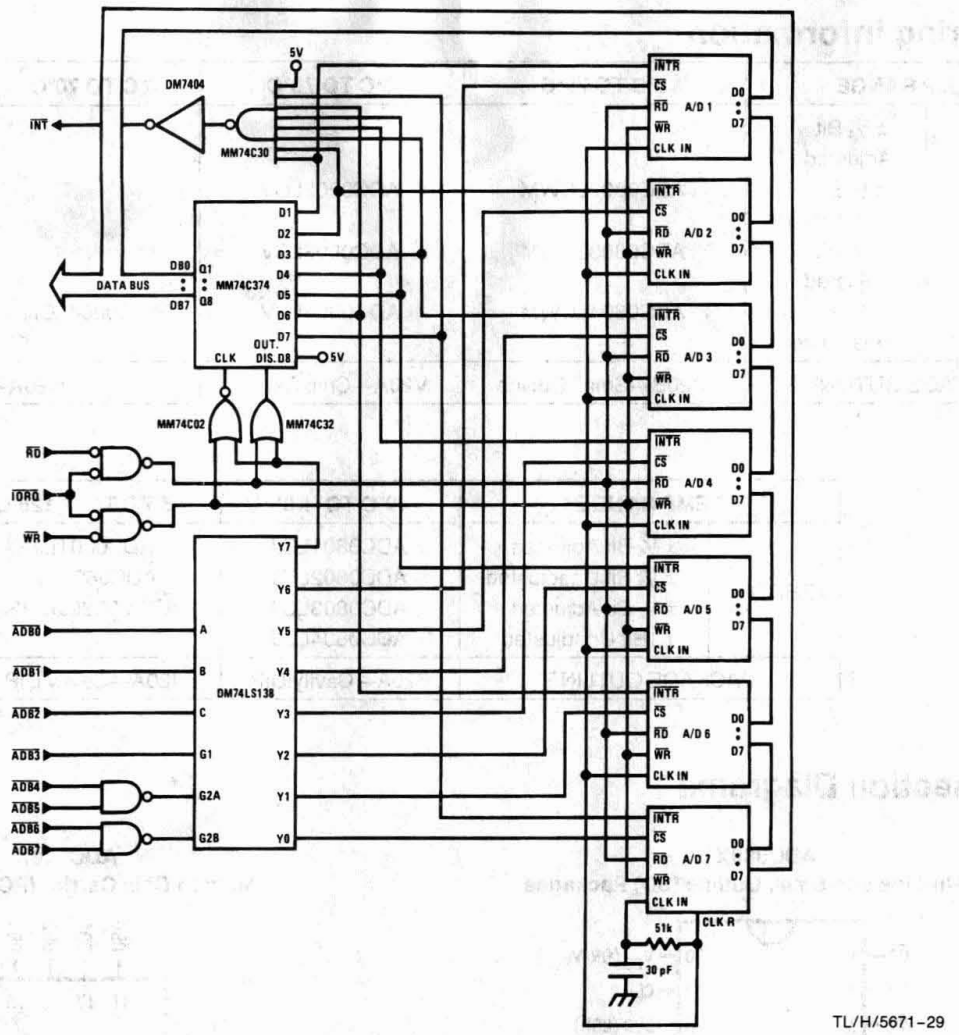

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FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE	SOURCE STATEMENT		COMMENT
0038	E5		PUSH HL	; Save contents of all registers affected by
0039	C5		PUSH BC	; this subroutine.
003A	F5		PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	; Load status word into accumulator.
0044	47		LD B,A	; Save the status word.
0045	79	TEST	LD A,C	; Test to see if the status of all A/D's have
0046	FE 08		CP, X08	; been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	; Test a single bit in status word by looking for
004C	1F		RRA	; a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	; If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF		XOR FF	; the data.
0059	77		LD (HL),A	; Store the data
005A	2C		INC L	
005B	71		LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	; Test next bit in status word.
0060	F1	DONE	POP AF	; Re-establish all registers as they were
0061	C1		POP BC	; before the interrupt.
0062	E1		POP HL	
0063	C9		RET	; Return to original program

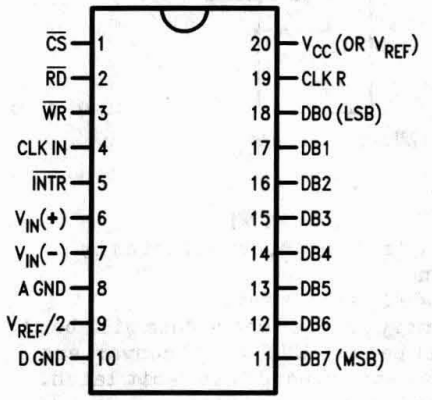
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted				ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	±½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	±¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	±½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ,
	±½ Bit Adjusted	ADC0803LCJ	ADC0802LJ/883
	±1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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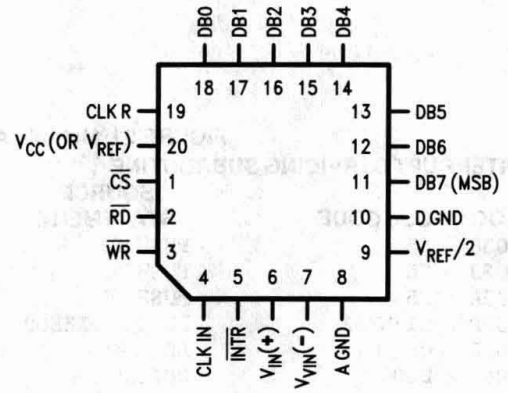
ADC080X
Molded Chip Carrier (PCC) Package



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See Ordering Information

National Semiconductor

ADC0808/ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

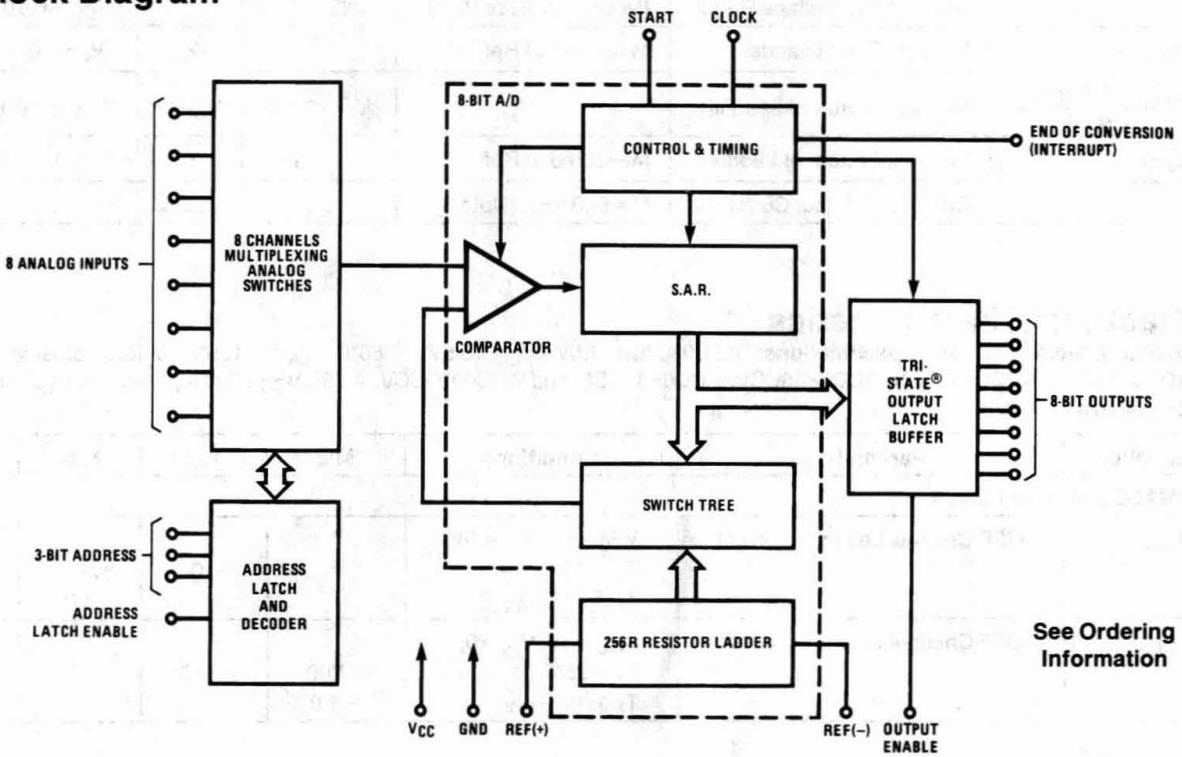
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

Block Diagram



See Ordering Information

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin	$-0.3V$ to ($V_{CC}+0.3V$)
Except Control Inputs	
Voltage at Control Inputs	$-0.3V$ to $+15V$
(START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation at $T_A=25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	400V

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN}\le T_A\le T_{MAX}$
ADC0808CJ	$-55°C\le T_A\le +125°C$
ADC0808CCJ, ADC0808CCN, ADC0809CCN	$-40°C\le T_A\le +85°C$
ADC0808CCV, ADC0809CCV	$-40°C\le T_A\le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: $V_{CC}=5$ $V_{DC}=V_{REF+}$, $V_{REF(-)}=GND$, $T_{MIN}\le T_A\le T_{MAX}$ and $f_{CLK}=640$ kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		$V_{CC}+0.10$	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	$V_{CC}+0.1$	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2$-0.1	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	$f_c=640$ kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ $4.5V\le V_{CC}\le 5.5V$, $-55°C\le T_A\le +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75\le V_{CC}\le 5.25V$, $-40°C\le T_A\le +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=5V$,				
		$T_A=25°C$		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=0$,				
		$T_A=25°C$	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN}=15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN}=0$	-1.0			μA
I_{CC}	Supply Current	$f_{CLK}=640$ kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O=1.2$ mA			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O=5V$ $V_O=0$	 -3		3	μA μA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_S	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S=0\Omega$ *(Figure 5)*		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L=50$ pF, $R_L=10$k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L=10$ pF, $R_L=10$k *(Figure 8)*		125	250	ns
t_C	Conversion Time	$f_C=640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μS
f_C	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8+2 μS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 12)		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached $+\frac{1}{2}$ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

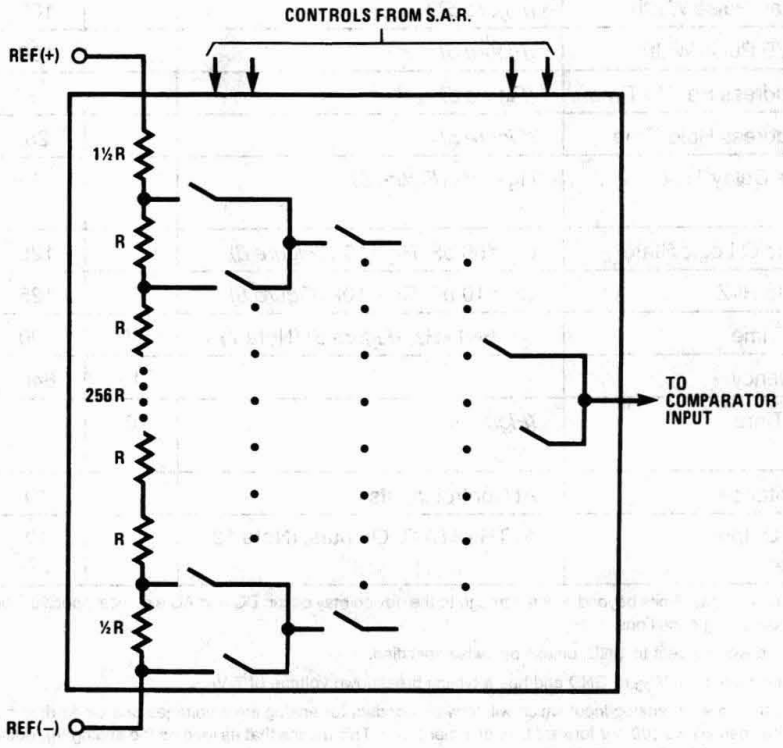

FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed throught a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

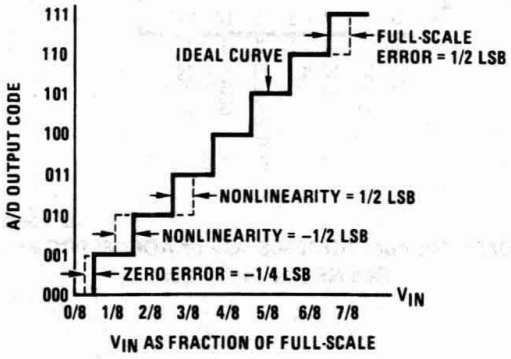

FIGURE 2. 3-Bit A/D Transfer Curve

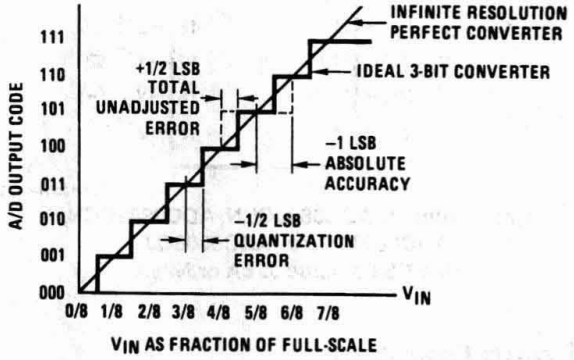

FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

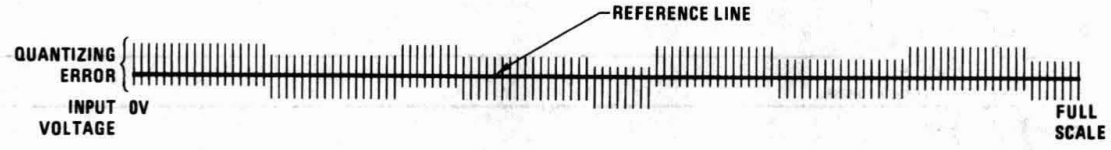

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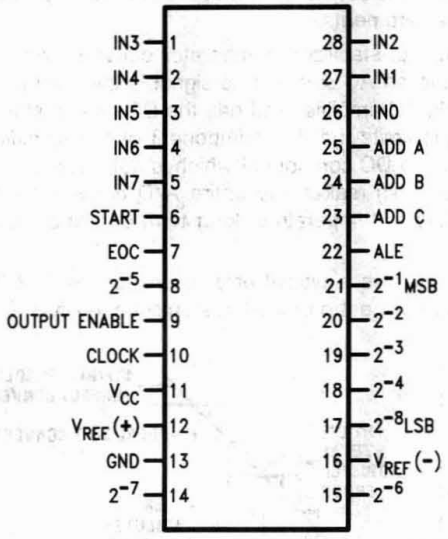
FIGURE 4. Typical Error Curve

Connection Diagrams

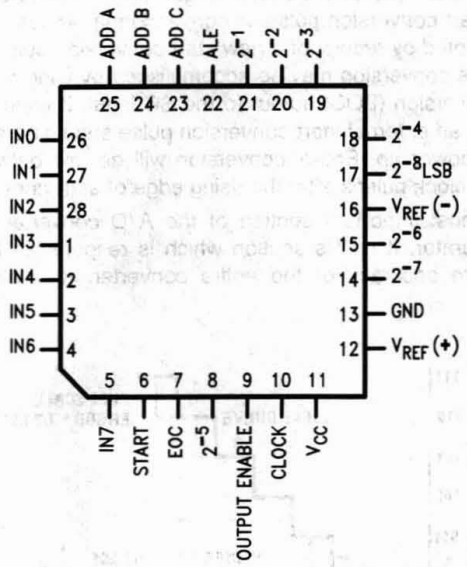
Dual-In-Line Package



TL/H/5672–11

Order Number ADC0808CCN, ADC0809CCN, ADC0808CCJ or ADC0808CJ
See NS Package J28A or N28A

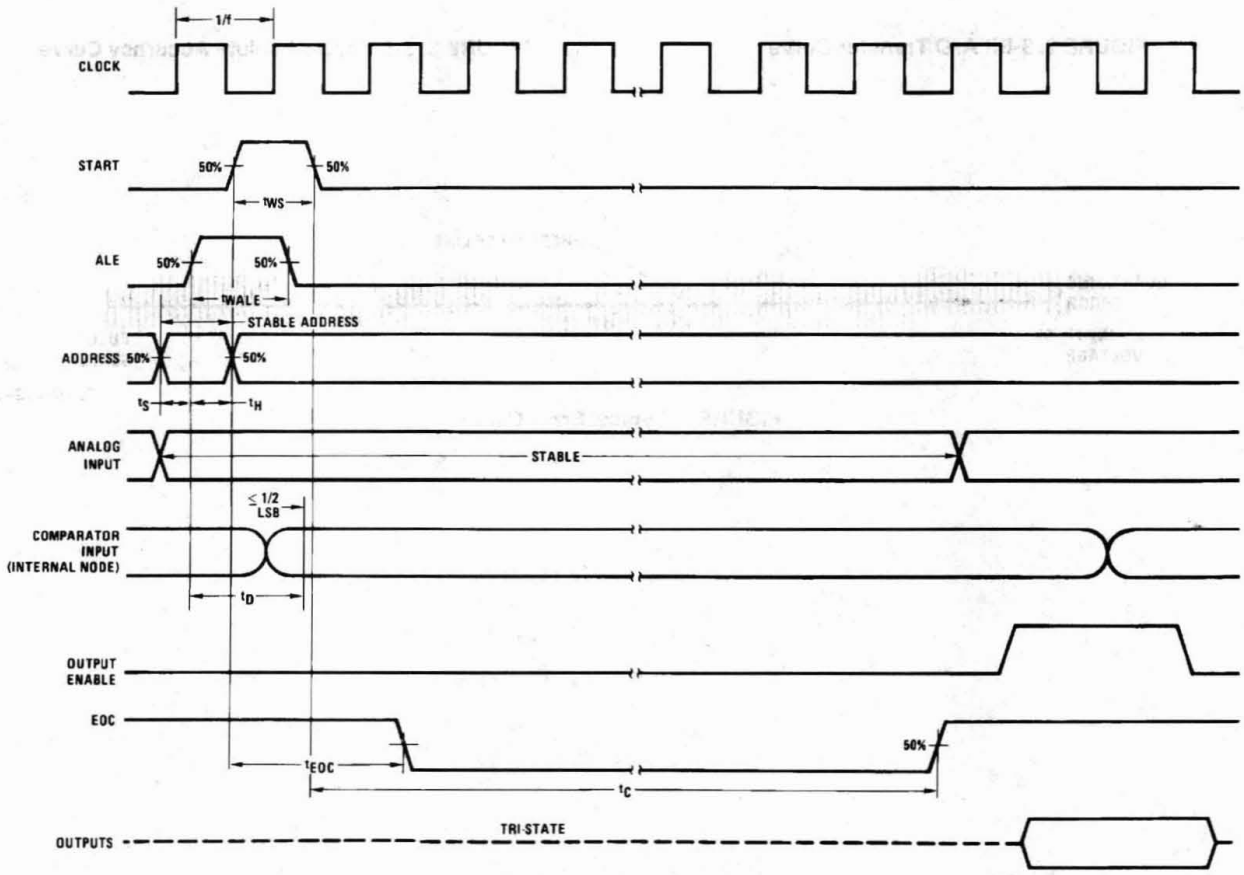
Molded Chip Carrier Package



TL/H/5672–12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Timing Diagram



TL/H/5672–4

FIGURE 5

Typical Performance Characteristics

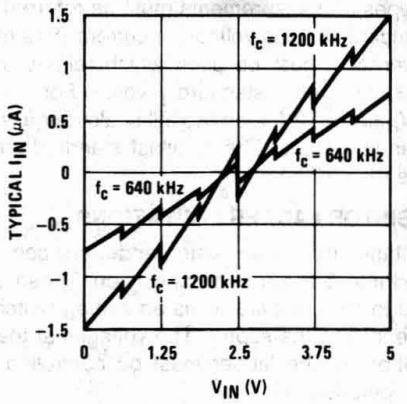
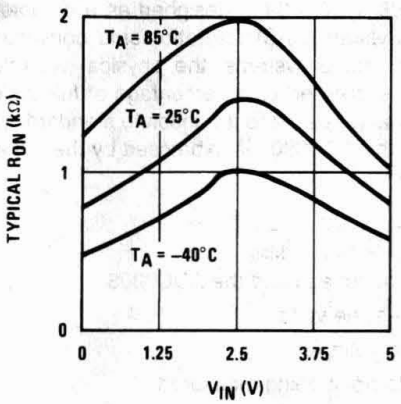


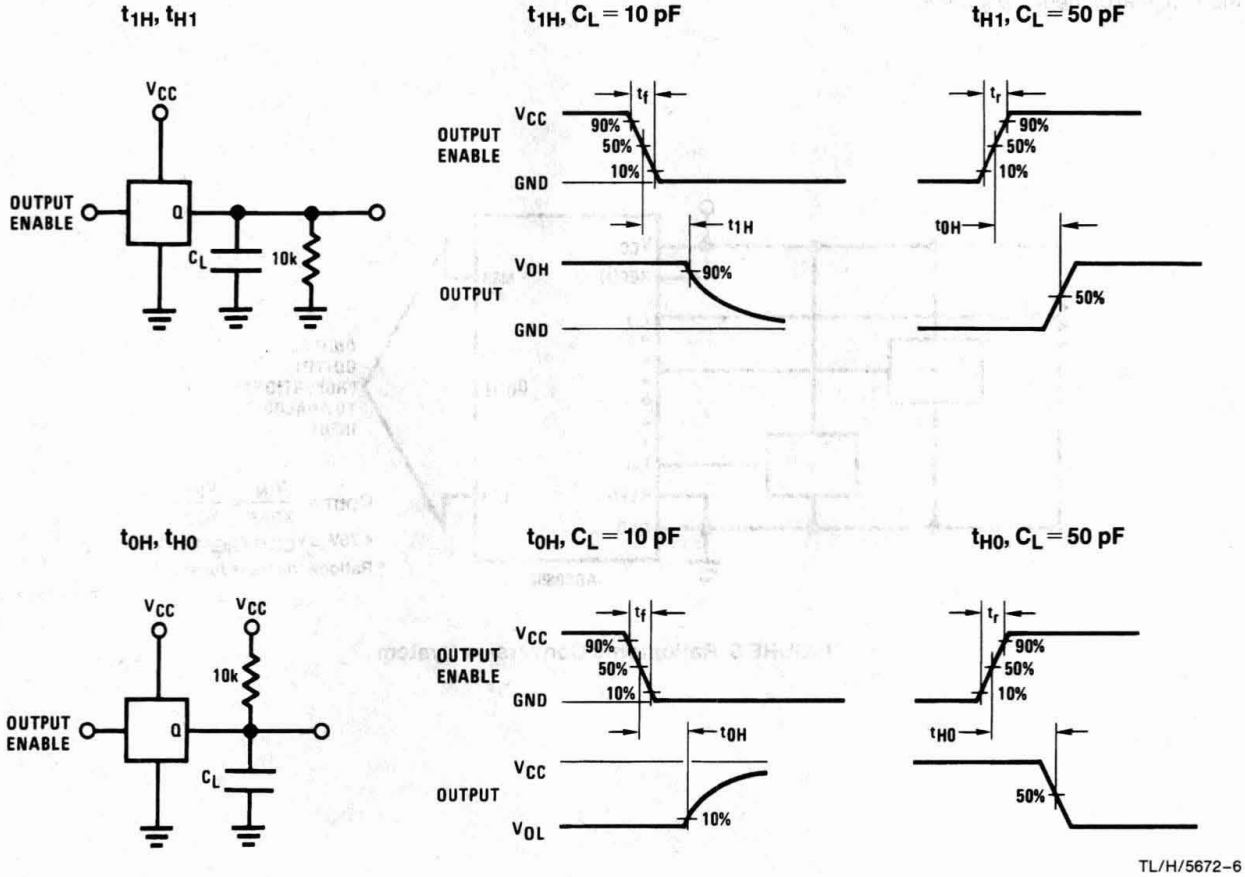
FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)



TL/H/5672-5

FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE Test Circuits and Timing Diagrams



TL/H/5672-6

FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

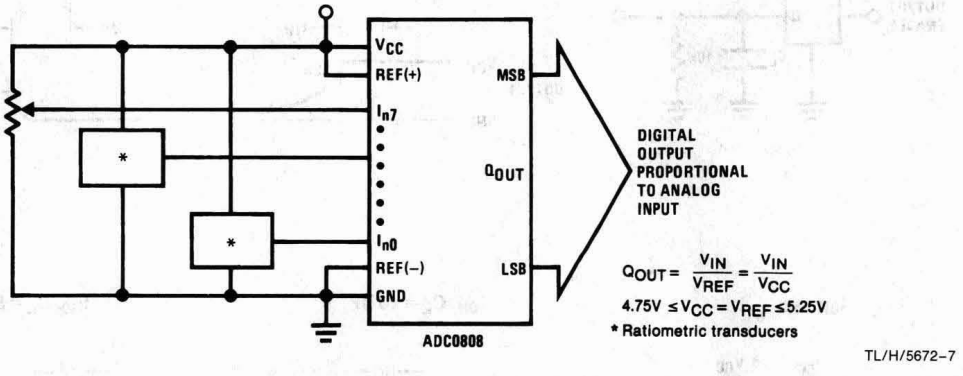


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

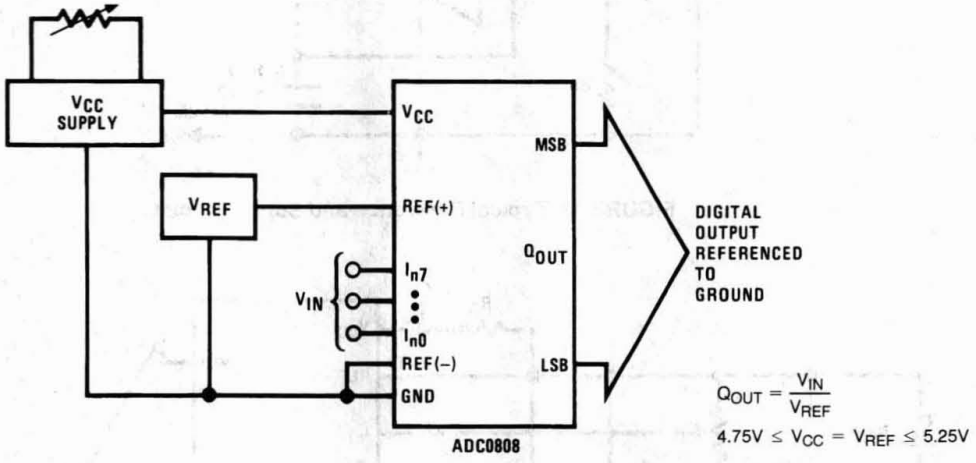


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

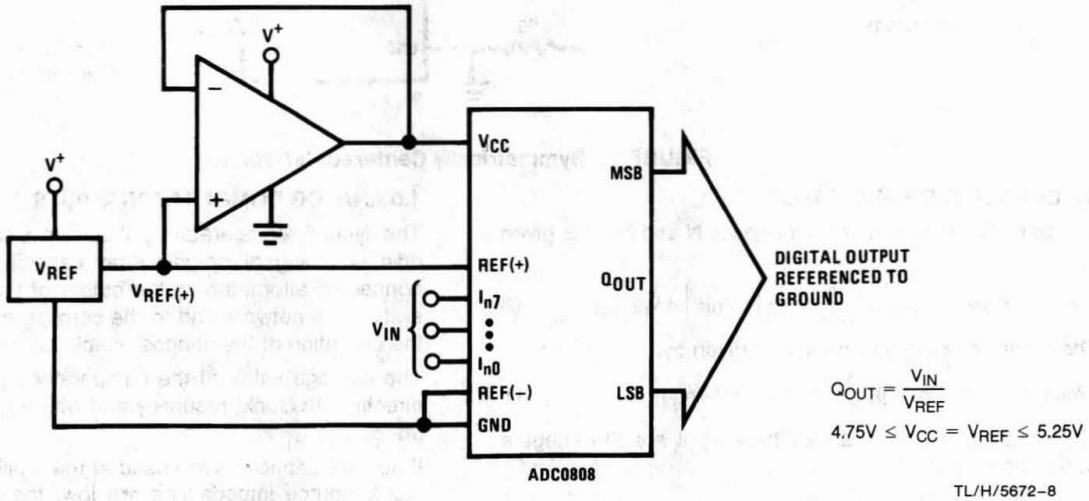


FIGURE 11: Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

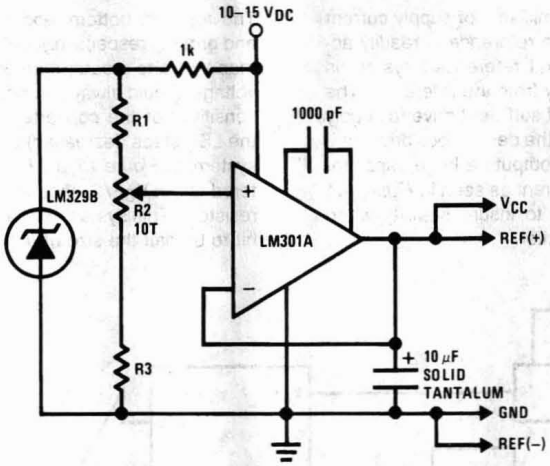
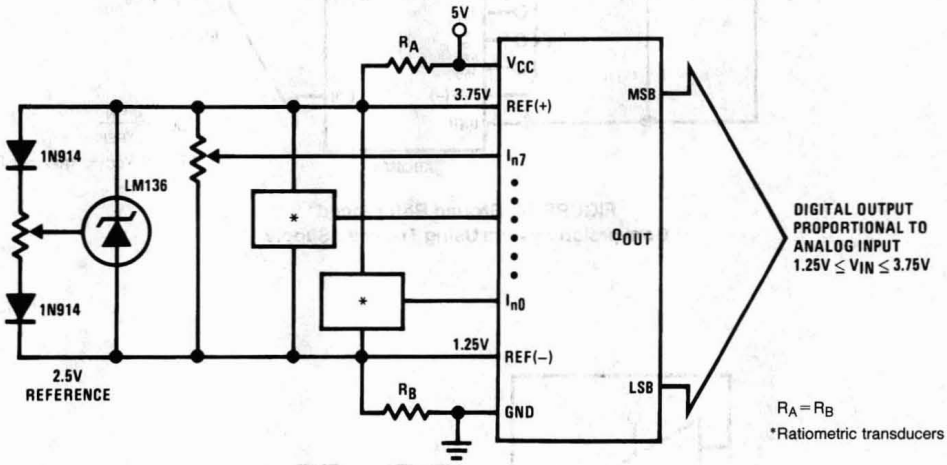


FIGURE 12. Typical Reference and Supply Circuit



TL/H/5672–9

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

$V_{REF(+)}$ = Voltage at Ref(+)

$V_{REF(-)}$ = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 ANALOG COMPARATOR INPUTS

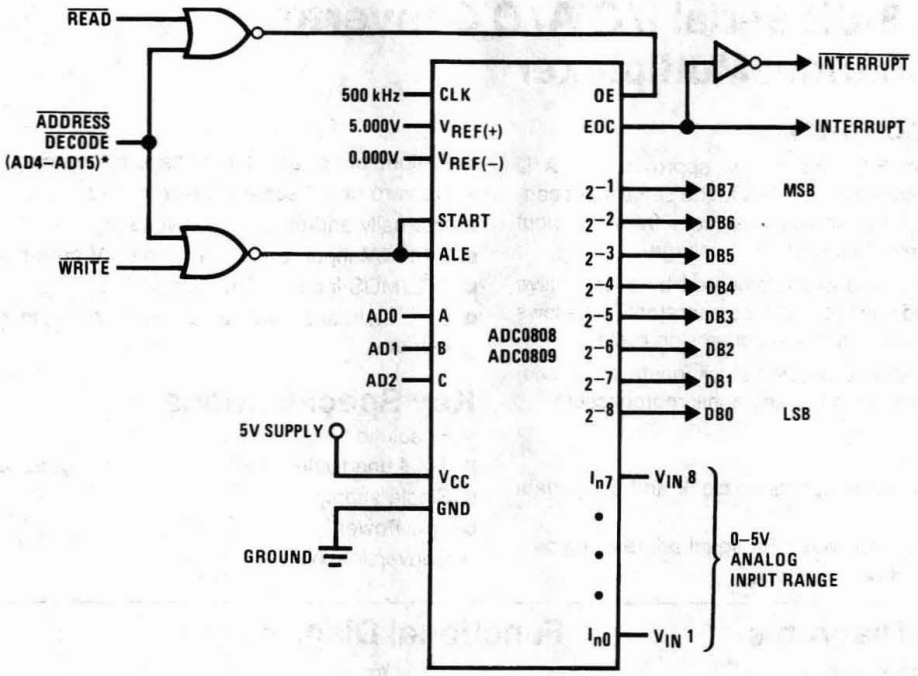
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



TL/H/5672–10

*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ2•R/W	VMA•ϕ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C			−55°C to +125°C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

National Semiconductor

ADC0811 8-Bit Serial I/O A/D Converter With 11-Channel Multiplexer

General Description

The ADC0811 is an 8-Bit successive approximation A/D converter with simultaneous serial I/O. The serial input controls an analog multiplexer which selects from 11 input channels or an internal half scale test voltage.

An input sample-and-hold is implemented by a capacitive reference ladder and sampled data comparator. This allows the input signal to vary during the conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Features

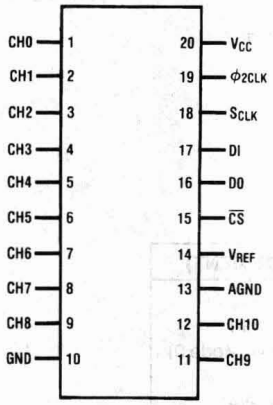
- Separate asynchronous converter clock and serial data I/O clock.
- 11-Channel multiplexer with 4-Bit serial address logic.
- Built-in sample and hold function.
- Ratiometric or absolute voltage referencing.
- No zero or full-scale adjust required.
- Internally addressable test voltage.
- 0V to 5V input range with single 5V power supply.
- TTL/MOS input/output compatible.
- 0.3" standard width 20-pin dip or 20-pin molded chip carrier

Key Specifications

■ Resolution	8-Bits
■ Total unadjusted error	± ½LSB and ± 1LSB
■ Single supply	$5V_{DC}$
■ Low Power	15 mW
■ Conversion Time	32 μS

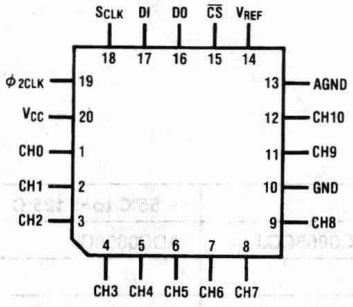
Connection Diagrams

Dual-In-Line Package



Top View TL/H/5587–1

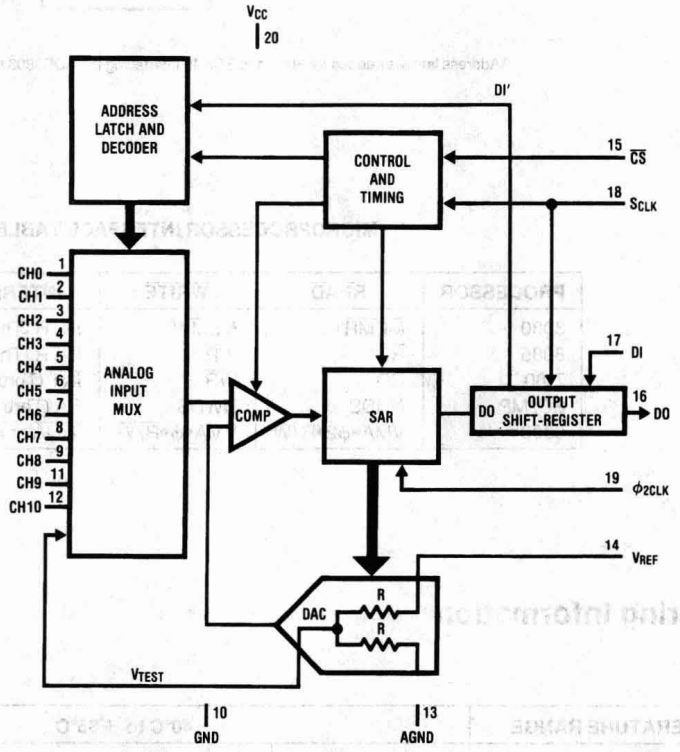
Molded Chip Carrier (PCC) Package



Top View TL/H/5587–2

Order Number ADC0811J,N,V
See NS Packages J20A, N20A, V20A
Use Ordering Information

Functional Diagram



TL/H/5587–3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Inputs and Outputs	−0.3V to V_{CC} +0.3V
Input Current Per Pin (Note 3)	±5mA
Total Package Input Current (Note 3)	±20mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0811BCN, ADC0811CCN	0°C ≤ T_A ≤ 70°C
ADC0811BCV	−40°C ≤ T_A ≤ 85°C
ADC0811CCJ, ADC0811CCV	−40°C ≤ T_A ≤ 85°C

Electrical Characteristics

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + 0.1V), $\phi_{2\ CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Parameter	Conditions	ADC0811CCJ			ADC0811BCN, ADC0811BCV ADC0811CCN, ADC0811CCV			Units
		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	V_{REF} = 5.00 V_{DC} (Note 4)							
ADC0811BCN, ADC0811BCV						±½	**±½**	LSB
ADC0811CCN, ADC0811CCV						±1	**±1**	LSB
ADC0811CCJ			**±1**					LSB
Minimum Reference Input Resistance		8		**5**	8		**5**	kΩ
Maximum Reference Input Resistance		8	**11**		8	11	**11**	kΩ
Maximum Analog Input Range	(Note 5)		**V_{CC} + 0.05**			V_{CC} + 0.05	**V_{CC} + 0.05**	V
Minimum Analog Input Range			**GND − 0.05**			GND − 0.05	**GND − 0.05**	V
On Channel Leakage Current								
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 5V Off Channel = 0V		**1000**			400	**1000**	nA
ADC0811CJ, BJ			**1000**					nA
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 0V Off Channel = 5V		**−1000**			−400	**−1000**	nA
ADC0811BJ, CJ	(Note 9)		**−1000**					nA
Off Channel Leakage Current								
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 5V Off Channel = 0V		**−1000**			−400	**1000**	nA
ADC0811CJ, BJ			**−1000**					nA
ADC0811BCJ, CCJ, BCN, CCN, BCV, CCV	On Channel = 0V Off Channel = 5V		**1000**			400	**1000**	nA
ADC0811BJ, CJ	(Note 9)		**1000**					nA
Minimum V_{TEST} Internal Test Voltage	V_{REF} = V_{CC}, CH 11 Selected		**125**			125	**125**	(Note 10) Counts
Maximum V_{TEST} Internal Test Voltage	V_{REF} = V_{CC}, CH 11 Selected		**130**			130	**130**	(Note 10) Counts

Electrical Characteristics

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + 0.1V), $\phi_{2\,CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Continued)

Parameter	Conditions	ADC0811CCJ			ADC0811BCN, ADC0811BCV ADC0811CCN, ADC0811CCV			Units
		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN} = 5.0V	0.005	**2.5**		0.005	2.5	**2.5**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	**−2.5**		−0.005	2.5	**−2.5**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.5**			2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 5.25V I_{OUT} = 1.6 mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	**−3** **3**		−0.01 0.01	−3 3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−12	**−6.5**		−14	−6.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	18	**8.0**		16	8.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	**2.5**		1	2.5	**2.5**	mA
I_{REF} (Max)	V_{REF} = 5V	**0.7**	**1**		**0.7**	1	**1**	mA

AC CHARACTERISTICS

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
$\phi_{2\,CLK}$, ϕ_2 Clock Frequency	MIN		0.70		**1.0**	MHz
	MAX		3.0	2.0	**2.1**	
S_{CLK}, Serial Data Clock Frequency	MIN				**5.0**	KHz
	MAX		700	525	**525**	
T_C, Conversion Process Time	MIN	Not Including MUX Addressing and Analog Input Sampling Times	48		**48**	ϕ_2 cycles
	MAX		64		**64**	
t_{ACC}, Access Time Delay From $\overline{CS}$	MIN				**1**	ϕ_2 cycles
Falling Edge to DO Data Valid	MAX				**3**	
t_{SET-UP}, Minimum Set-up Time of $\overline{CS}$ Falling Edge to S_{CLK} Rising Edge					$\mathbf{4/\phi_{2CLK} + \frac{1}{2\,S_{CLK}}}$	sec
$t_{H\overline{CS}}$, $\overline{CS}$ Hold Time After the Falling Edge of S_{CLK}					**0**	ns
$t_{\overline{CS}}$, Total $\overline{CS}$ Low Time	MIN				$\mathbf{t_{set\text{-}up} + 8/S_{CLK}}$	sec
	MAX				$\mathbf{t_{\overline{CS}}(min) + 48/\phi_{2CLK}}$	sec
t_{HDI}, Minimum DI Hold Time from S_{CLK} Rising Edge			0		**0**	ns
t_{HDO}, Minimum DO Hold Time from S_{CLK} Falling Edge		R_L = 30k, C_L = 100 pF			**10**	ns

Electrical Characteristics

The following specifications apply for V_{CC} = 4.75V to 5.25V, V_{REF} = +4.6V to (V_{CC} + 0.1V), $\phi_{2\ CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Continued)

Parameter	Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
AC CHARACTERISTICS (Continued)						
t_{SDI}, Minimum DI Set-up Time to S_{CLK} Rising Edge			200		**400**	ns
t_{DDO}, Maximum Delay From S_{CLK} Falling Edge to DO Data Valid	R_L = 30k, C_L = 100 pF		180	400	**400**	ns
t_{TRI}, Maximum DO Hold Time, ($\overline{CS}$ Rising edge to DO TRI-STATE)	R_L = 3k, C_L = 100 pF		90	150	**150**	ns
t_{CA}, Analog Sampling Time	After Address Is Latched $\overline{CS}$ = Low				**4/S_{CLK} + 1 μs**	sec
t_{RDO}, Maximum DO	R_L = 30 kΩ,	"TRI-STATE" to "HIGH" State	75	150	**150**	ns
Rise Time	C_L = 100 pf	"LOW" to "HIGH" State	150	300	**300**	
t_{FDO}, Maximum DO	R_L = 30 kΩ,	"TRI-STATE" to "LOW" State	75	150	**150**	ns
Fall Time	C_L = 100 pf	"HIGH" to "LOW" State	150	300	**300**	
C_{IN}, Maximum Input	Analog Inputs, AN0–AN10 and V_{REF}		11		**55**	pF
Capacitance	All Others		5		**15**	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Under over voltage conditions (V_{IN} < 0V and V_{IN} > V_{CC}) the maximum input current at any one pin is ±5 mA. If the voltage at more than one pin exceeds V_{CC} + .3V the total package current must be limited to 20 mA. For example the maximum number of pins that can be over driven at the maximum current level of ±5 mA is four.

Note 4: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 5: Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% production tested under worst case condition.

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

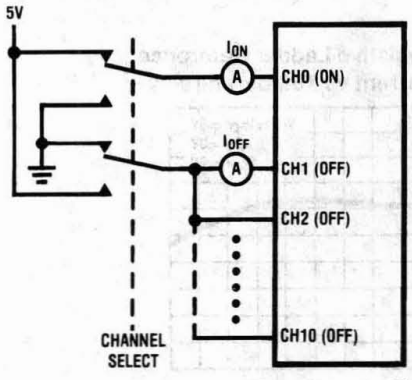
Note 9: Channel leakage current is measured after the channel selection.

Note 10: 1 count = V_{REF}/256.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

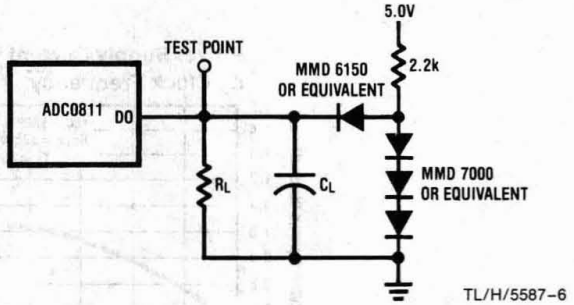
Test Circuits

Leakage Current



TL/H/5587–17

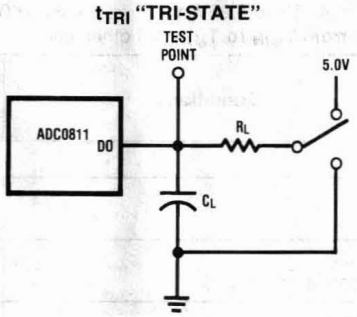
D0 Except "TRI-STATE"



TL/H/5587–6

Test Circuits (Continued)

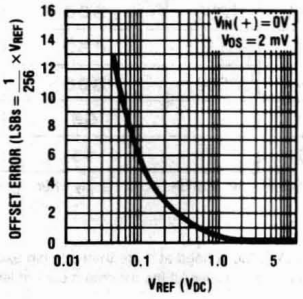
t_{TRI} "TRI-STATE"



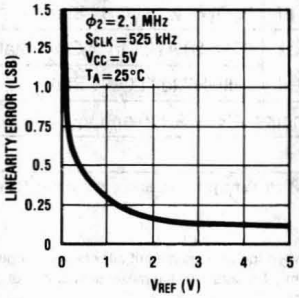
TL/H/5587–22

Typical Performance Characteristics

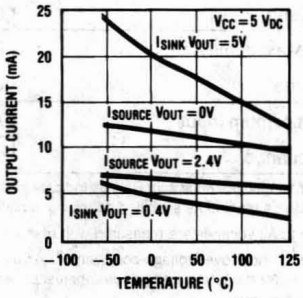
Unadjusted Offset Error vs V_{REF} Voltage



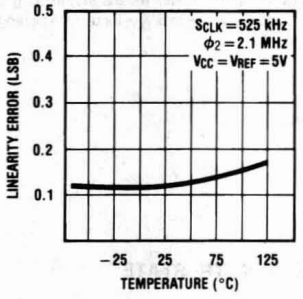
Linearity Error vs V_{REF} Voltage



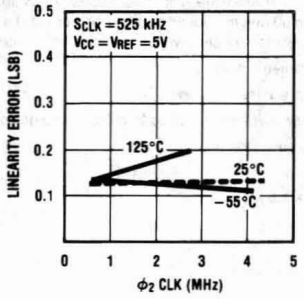
Output Current vs Temperature



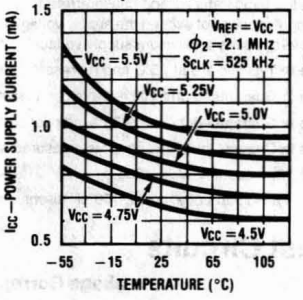
Linearity vs Temperature



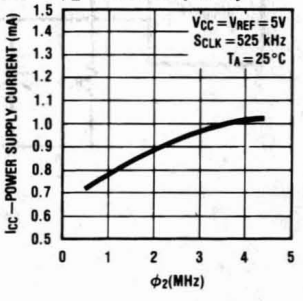
Linearity vs ϕ_2 Clock Frequency



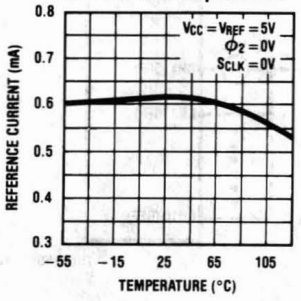
Power Supply Current vs Temperature



Power Supply Current vs ϕ_2 Clock Frequency



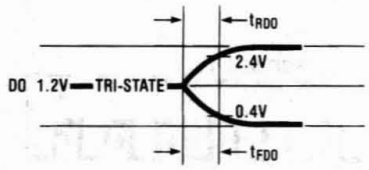
Resistive Ladder Reference Current vs Temperature



TL/H/5587–16

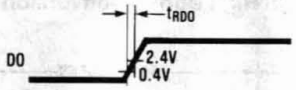
Timing Diagrams

D0 "TRI-STATE" Rise & Fall Times



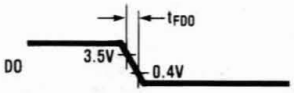
TL/H/5587–13

D0 Low to High State



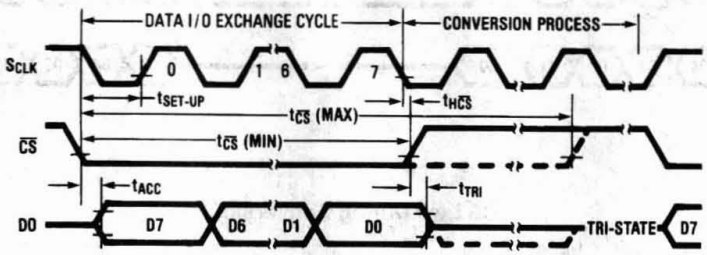
TL/H/5587–14

D0 High to Low State



TL/H/5587–15

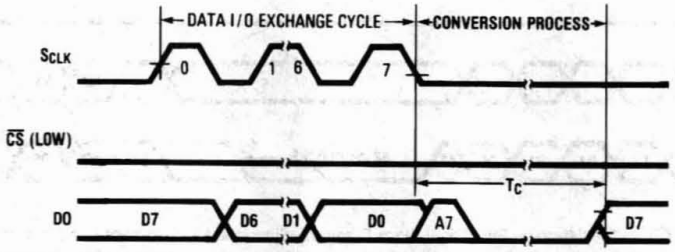
Timing with a continuous S_{CLK}



TL/H/5587–11

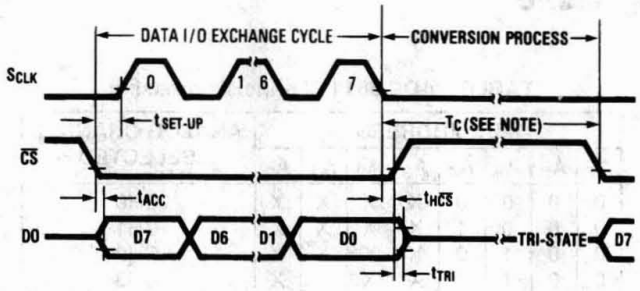
*Strobing $\overline{CS}$ High and Low will abort the present conversion and initiate a new serial I/O exchange.

Timing with a gated S_{CLK} and $\overline{CS}$ Continuously Low



TL/H/5587–9

Using $\overline{CS}$ To TRI-STATE D0

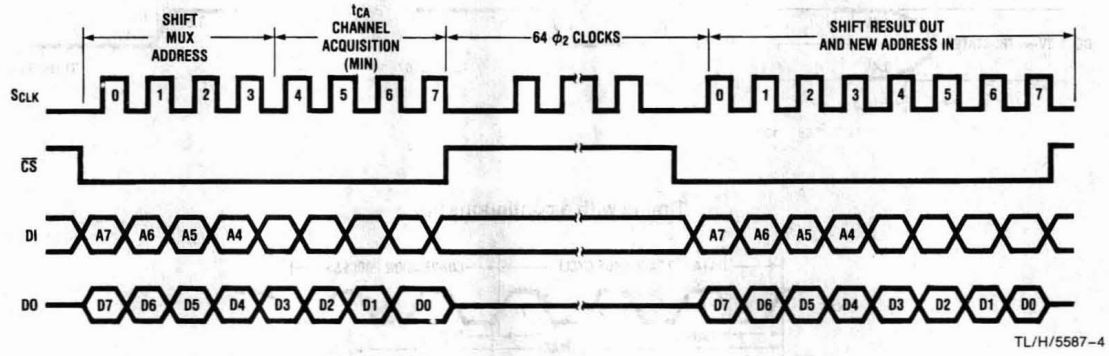


TL/H/5587–10

Note: Strobing $\overline{CS}$ Low during this time interval will abort the conversion in process.

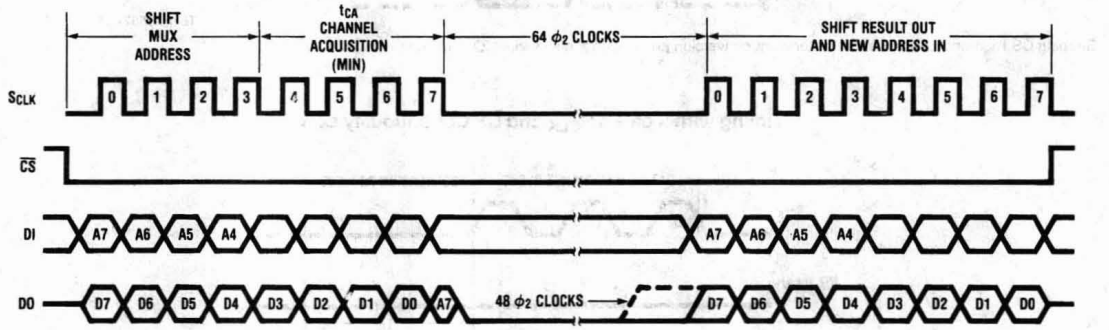
Timing Diagrams (Continued)

$\overline{CS}$ High During Conversion



TL/H/5587–4

$\overline{CS}$ Low During Conversion



TL/H/5587–5

Note: DO and DI lines share the 8-bit I/O shift register(see Functional Block Diagram). Since the MUX address bits are shifted in on S_{CLK} rising edges while S_{CLK} falling edges shift out conversion data on DO, the eighth falling edge of S_{CLK} will shift out the MSB MUX address bit (A7) on DO. Thus, if addressing channels CH8–CH10, a high DO will occur momentarily (one ϕ_2 clock period) until the 8-bit I/O shift register is cleared by the internal EOC signal.

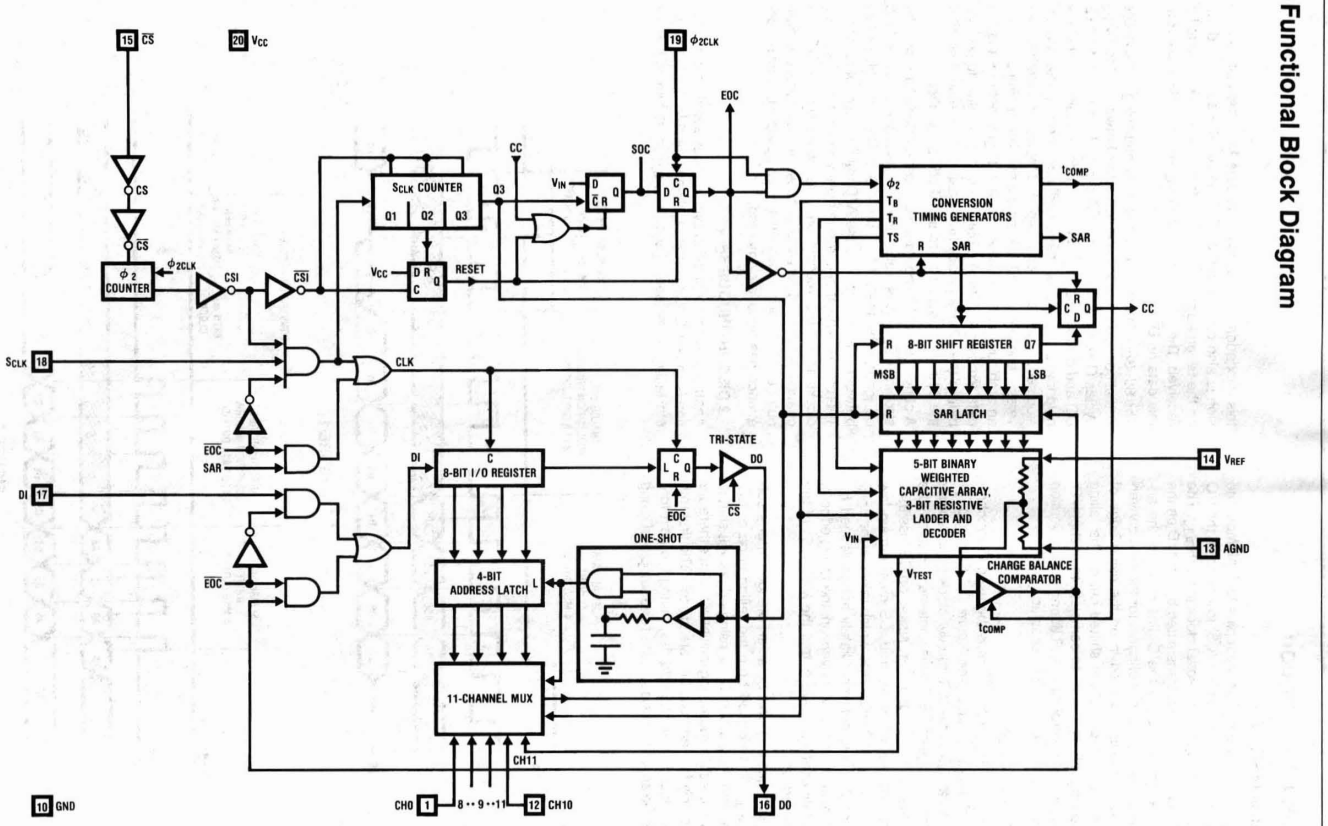
Channel Addressing Table

TABLE I. ADC 0811 Channel Addressing

MUX ADDRESS								ANALOG CHANNEL SELECTED
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	X	X	X	X	CH0
0	0	0	1	X	X	X	X	CH1
0	0	1	0	X	X	X	X	CH2
0	0	1	1	X	X	X	X	CH3
0	1	0	0	X	X	X	X	CH4
0	1	0	1	X	X	X	X	CH5
0	1	1	0	X	X	X	X	CH6
0	1	1	1	X	X	X	X	CH7
1	0	0	0	X	X	X	X	CH8
1	0	0	1	X	X	X	X	CH9
1	0	1	0	X	X	X	X	CH10
1	0	1	1	X	X	X	X	V_{TEST}
1	1	X	X	X	X	X	X	LOGIC TEST MODE*

* Analog channel inputs CH0 thru CH3 are logic outputs

Functional Block Diagram



Functional Description

1.0 DIGITAL INTERFACE

The ADC0811 uses five input/output pins to implement the serial interface. Taking chip select ($\overline{CS}$) low enables the I/O data lines (DO and DI) and the serial clock input (S_{CLK}). The result of the last conversion is transmitted by the A/D on the DO line, while simultaneously the DI line receives the address data that selects the mux channel for the next conversion. The mux address is shifted in on the rising edge of S_{CLK} and the conversion data is shifted out on the falling edge. It takes eight S_{CLK} cycles to complete the serial I/O. A second clock (ϕ_2) controls the SAR during the conversion process and must be continuously enabled.

1.1 CONTINUOUS S_{CLK}

With a continuous S_{CLK} input $\overline{CS}$ must be used to synchronize the serial data exchange (see *Figure 1*). The ADC0811 recognizes a valid $\overline{CS}$ one to three ϕ_2 clock periods after the actual falling edge of $\overline{CS}$. This is implemented to ensure noise immunity of the $\overline{CS}$ signal. Any spikes on $\overline{CS}$ less than one ϕ_2 clock period will be ignored. $\overline{CS}$ must remain low during the complete I/O exchange which takes eight S_{CLK} cycles. Although $\overline{CS}$ is not immediately acknowledged for the purpose of starting a new conversion, the falling edge of $\overline{CS}$ immediately enables DO to output the MSB (D7) of the previous conversion.

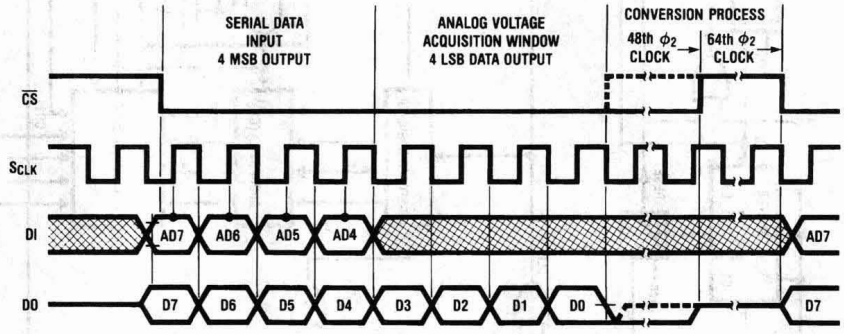
The first S_{CLK} rising edge will be acknowledged after a set-up time ($t_{set\text{-}up}$) has elapsed from the falling edge of $\overline{CS}$. This and the following seven S_{CLK} rising edges will shift in the channel address for the analog multiplexer. Since there are 12 channels only four address bits are utilized. The first four S_{CLK} cycles clock in the mux address, during the next four S_{CLK} cycles the analog input is selected and sampled. During this mux address/sample cycle, data from the last conversion is also clocked out on DO. Since D7 was clocked out on the falling edge of $\overline{CS}$ only data bits D6–D0 remain to be received. The following seven falling edges of S_{CLK} shift out this data on DO.

The 8th S_{CLK} falling edge initiates the beginning of the A/D's actual conversion process which takes between 48 to 64 ϕ_2 cycles (T_C). During this time $\overline{CS}$ can go high to TRI-STATE DO and disable the S_{CLK} input or it can remain low. If $\overline{CS}$ is held low a new I/O exchange will not start until the conversion sequence has been completed, however once the conversion ends serial I/O will immediately begin. Since there is an ambiguity in the conversion time (T_C) synchronizing the data exchange is impossible. Therefore $\overline{CS}$ should go high before the 48th ϕ_2 clock has elasped and return low after the 64th ϕ_2 to synchronize serial communication.

A conversion or I/O operation can be aborted at any time by strobing $\overline{CS}$. If $\overline{CS}$ is high or low less than one ϕ_2 clock it will be ignored by the A/D. If the $\overline{CS}$ is strobed high or low between 1 to 3 ϕ_2 clocks the A/D may or may not respond. Therefore $\overline{CS}$ must be strobed high or low greater than 3 ϕ_2 clocks to ensure recognition. If a conversion or I/O exchange is aborted while in process the consequent data output will be erroneous until a complete conversion sequence has been implemented.

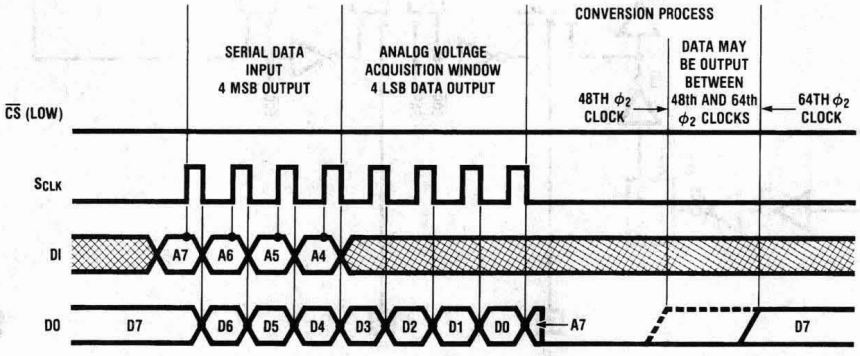
1.2 DISCONTINUOUS S_{CLK}

Another way to accomplish synchronous serial communication is to tie $\overline{CS}$ low continuously and disable S_{CLK} after its 8th falling edge (see *Figure 2*). S_{CLK} must remain low for



TL/H/5587–18

FIGURE 1



TL/H/5587–19

FIGURE 2

Functional Description (Continued)

at least 64 ϕ_2 clocks to insure that the A/D has completed its conversion. If S_{CLK} is enabled sooner, synchronizing to the data output on DO is not possible since an end of conversion signal from the A/D is not available and the actual conversion time is not known. With $\overline{CS}$ low during the conversion time (64 ϕ_2 max) DO will go low after the eighth falling edge of S_{CLK} and remain low until the conversion is completed. Once the conversion is through DO will transmit the MSB. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously.

If $\overline{CS}$ goes high during the conversion sequence DO is tri-stated, and the result is not affected so long as $\overline{CS}$ remains high until the end of the conversion.

1.2 MULTIPLEXER ADDRESSING

The four bit mux address is shifted, MSB first, into DI. Input data corresponds to the channel selected as shown in table 1. Care should be taken not to send an address greater than or equal to twelve (11XX) as this puts the A/D in a digital testing mode. In this mode the analog inputs CH0 thru CH3 become digital outputs, for our use in production testing.

2.0 ANALOG INPUT

2.1 THE INPUT SAMPLE AND HOLD

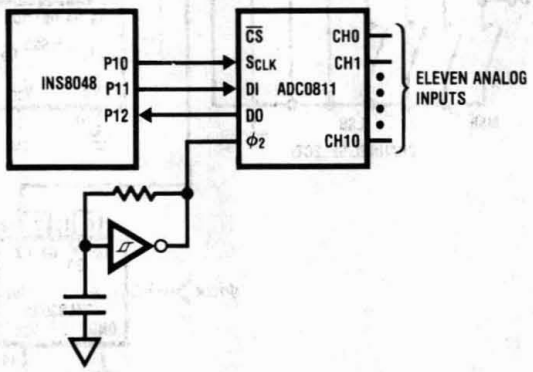
The ADC0811's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for 1 μsec after the eighth S_{CLK} falling edge. The hold mode is initiated with the start of the conversion process. An acquisition window of $4t_{SCLK}+1$ μsec is therefore available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (3K) of the multiplexer switches and the total ladder capacitance (90pf). These values yield an acquisition time of about 2 μsec for a full scale reading. Therefore the analog input must be stable for at least 2 μsec before and 1 μsec after the eighth S_{CLK} falling edge to ensure a proper conversion. External input source resistance and capacitance will lengthen the acquisition time and should be accounted for.

Other conventional sample and hold error specifications are included in the error and timing specs of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC0811's total unadjusted error, while the hold settling time is included in the A/D's max conversion time of 64 ϕ_2 clock periods. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

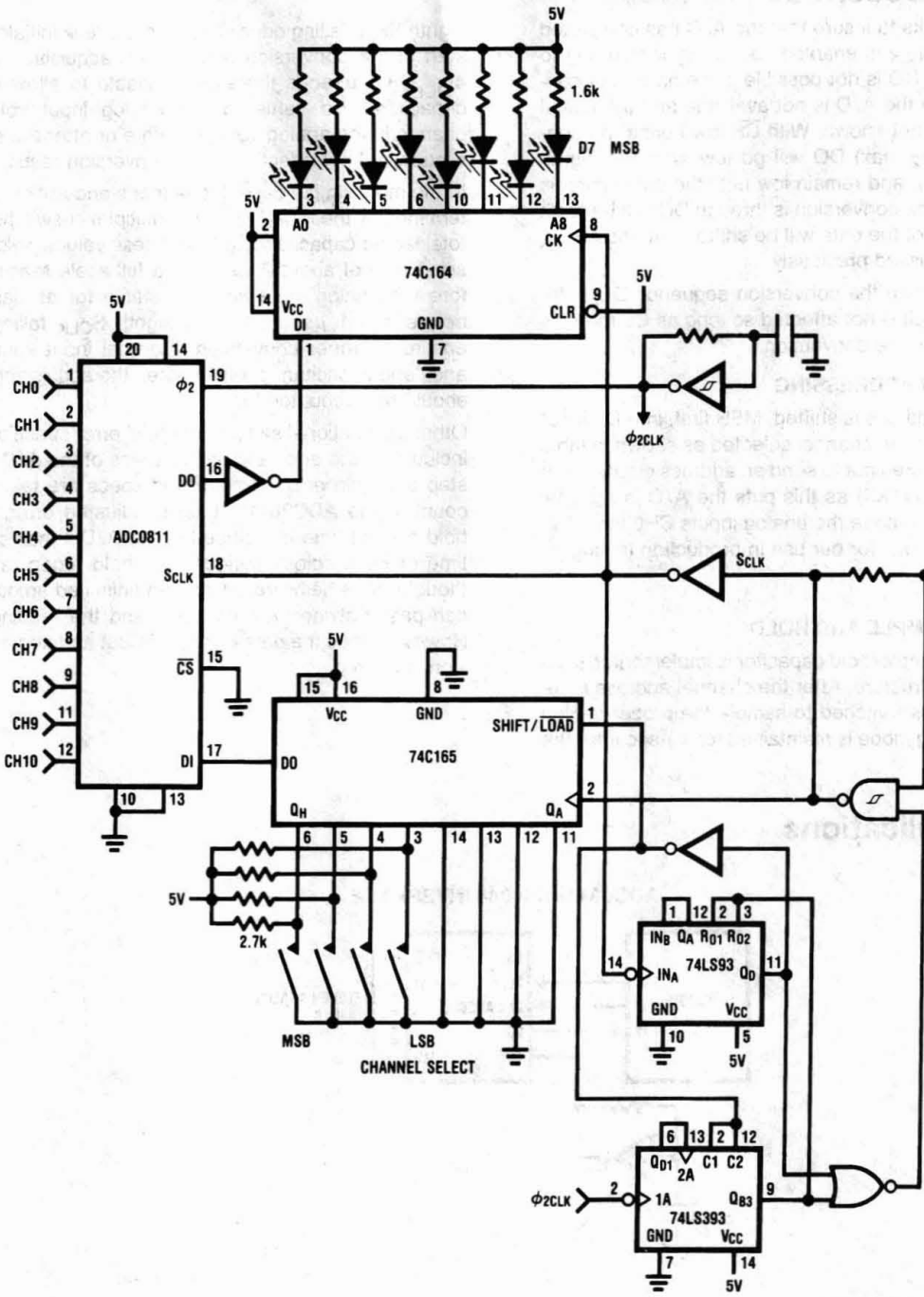
Typical Applications

ADC0811-INS8048 INTERFACE



TL/H/5587–21

ADC0811 FUNCTIONAL CIRCUIT



TL/H/5587–20

Ordering Information

Temperature Range		0°C to 70°C	−40°C to +85°C
Total Unadjusted Error	±½ LSB	ADC0811BCN	ADC0811BCV
	±1 LSB	ADC0811CCN	ADC0811CCJ ADC0811CCV
Package Outline		N20A	J20A, V20A

National Semiconductor

ADC0816/ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

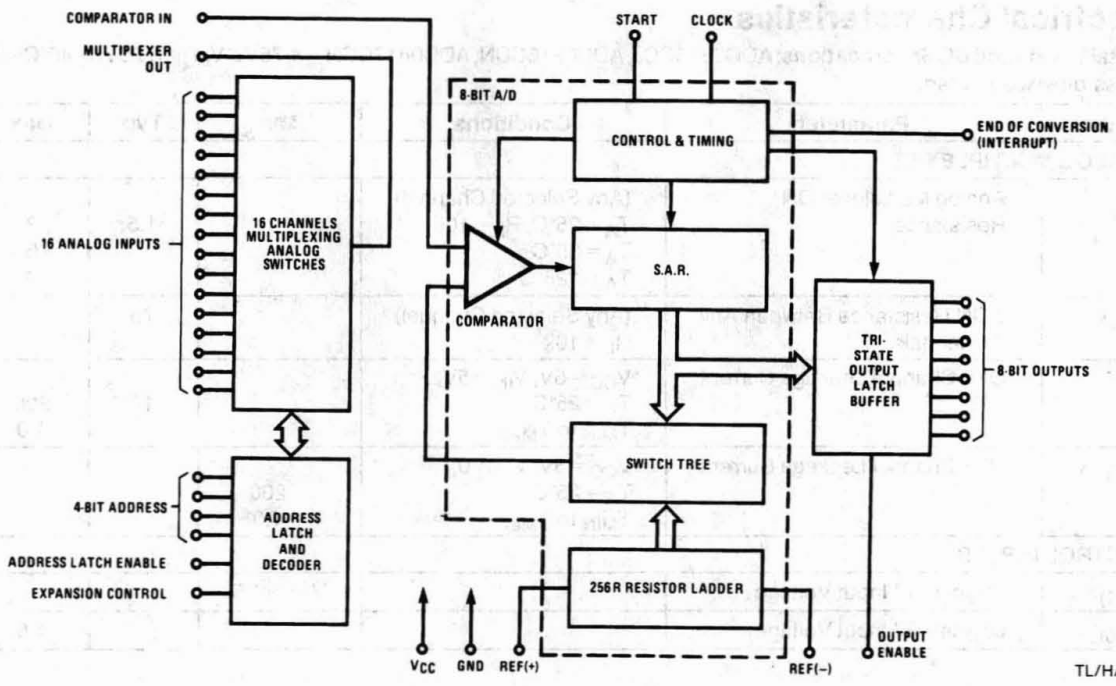
Features

- Easy interface to all microprocessors, or operates "stand alone"
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Outputs meet TTL voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning
- ADC0816 equivalent to MM74C948
- ADC0817 equivalent to MM74C948-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

Block Diagram



TL/H/5277–1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to + 150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 9)	400V

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, V_{IN} = $V_{COMPARATOR\ IN}$, $T_{MIN} \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			±½ ±¾	LSB LSB
	ADC0817 Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			±1 ±1¼	LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CCJ, ADC0816CCN, ADC0817CCN—4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) T_A = 25°C, R_L = 10k T_A = 85°C T_A = 125°C		1.5	3 6 9	kΩ kΩ kΩ
ΔR_{ON}	ΔON Resistance Between Any 2 Channels	(Any Selected Channel) R_L = 10k		75		Ω
I_{OFF+}	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C T_{MIN} to T_{Max}	−200 −1.0			nA μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CCJ, ADC0816CCN, ADC0817CCN—4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS (Continued)						
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O −360 μA, T_A = 85°C I_O = −300 μA, T_A = 125°C	V_{CC} −0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O = V_{CC} V_O = 0	 −3.0		3.0	μA μA

Electrical Characteristics

Timing Specifications: V_{CC} = $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = GND, t_r = t_f = 20 ns and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)* (Note 7)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
T_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time from ALE	R_S = 0Ω *(Figure 5)*		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L = 50 pF, R_L = 10k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L = 10 pF, R_L = 10k *(Figure 8)*		125	250	ns
t_C	Conversion Time	f_c = 640 kHz, *(Figure 5)* (Note 8)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs (Note 8)		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: If start pulse is asynchronous with converter clock or if f_c > 640 kHz, the minimum start pulse width is 8 clock periods plus 2 μs. For synchronous operation at f_c ≤ 640 kHz take start high within 100 ns of clock going low.

Note 8: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 9: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1

Selected Analog Channel	Address Line				Expansion Control
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

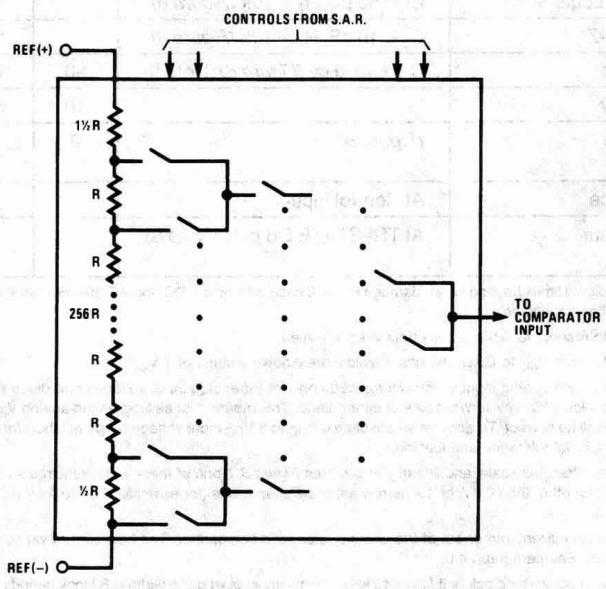
CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

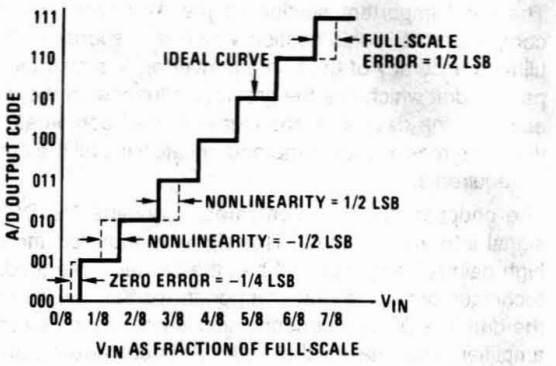
The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + ½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.



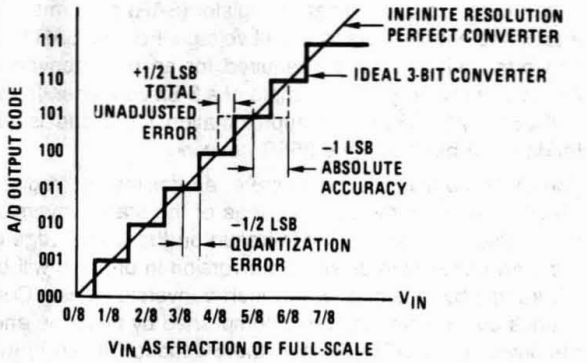
TL/H/5277–2

FIGURE 1. Resistor Ladder and Switch Tree



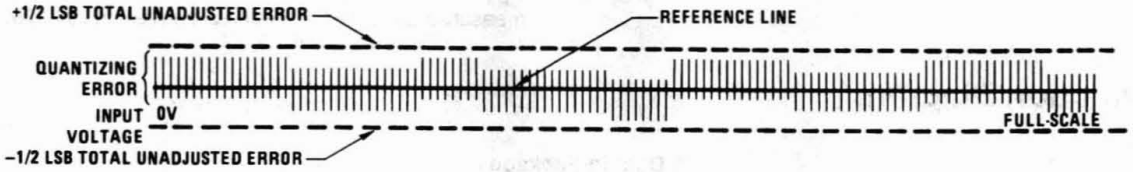
TL/H/5277–3

FIGURE 2. 3-Bit A/D Transfer Curve



TL/H/5277–4

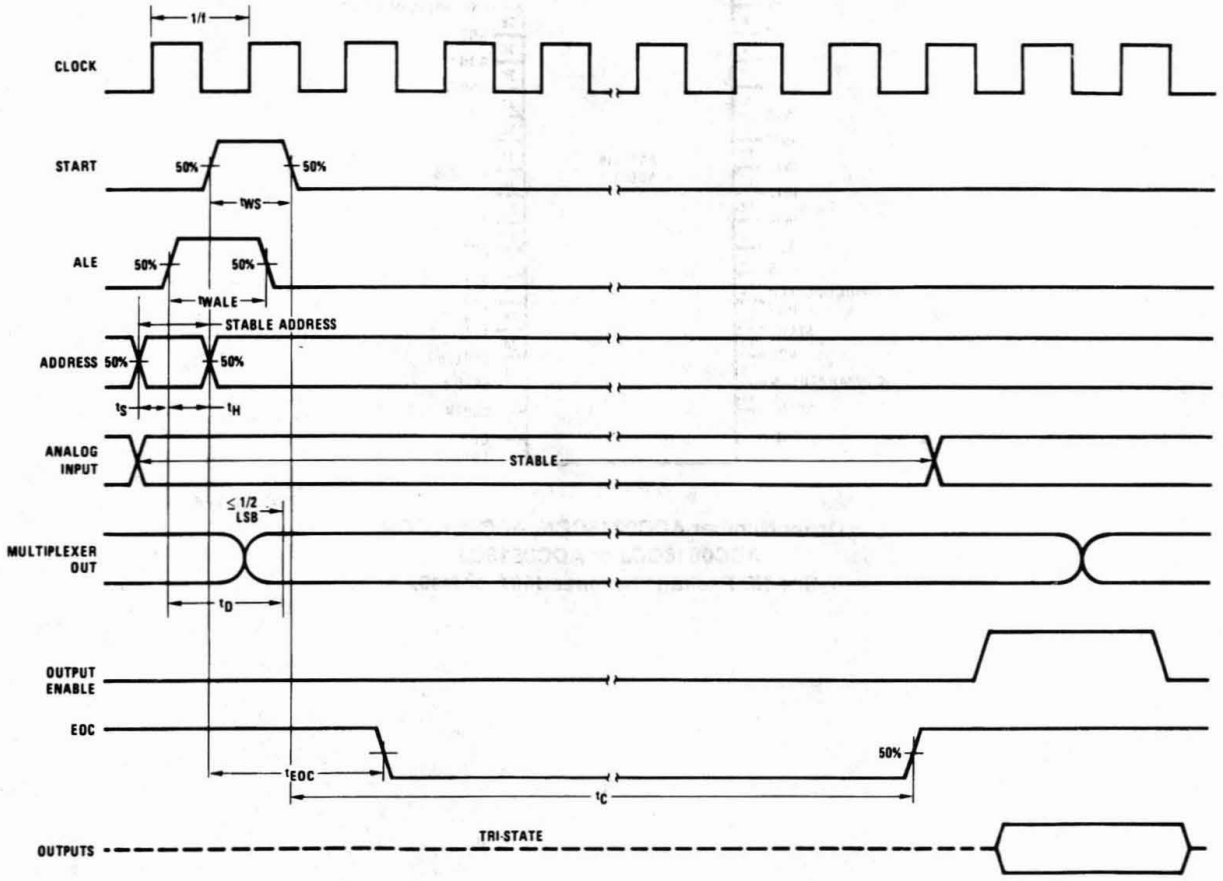
FIGURE 3. 3-Bit A/D Absolute Accuracy Curve



TL/H/5277–5

FIGURE 4. Typical Error Curve

Timing Diagram



TL/H/5277–7

FIGURE 5

2

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

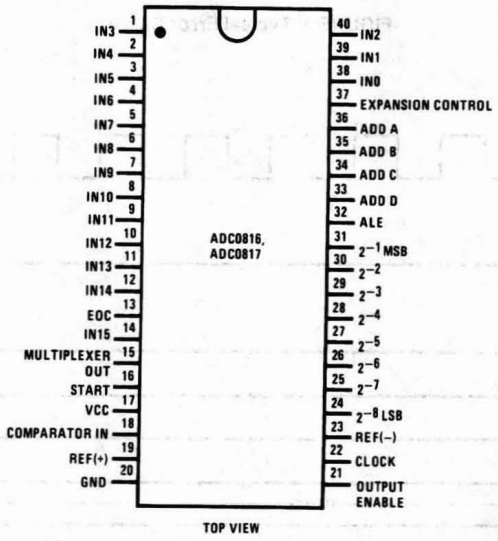
The most important section of the A/D converter is the comparator. It is this section which is responsible for the ulimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

Connection Diagram

Dual-In-Package



TOP VIEW

TL/H/5277–6

Order Number ADC0816CCN, ADC0817CCN, ADC0816CCJ or ADC0816CJ
See NS Package Number J40A or N40A

Typical Performance Characteristics

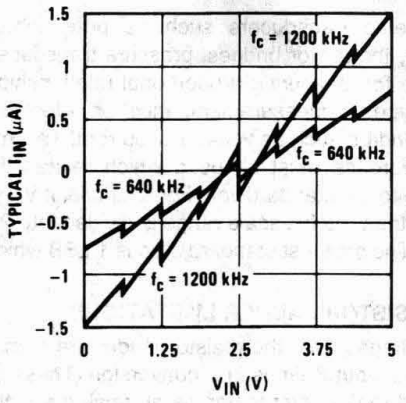
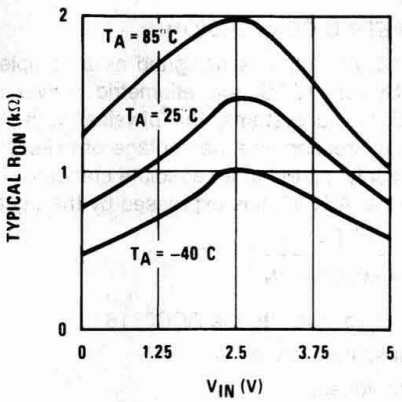


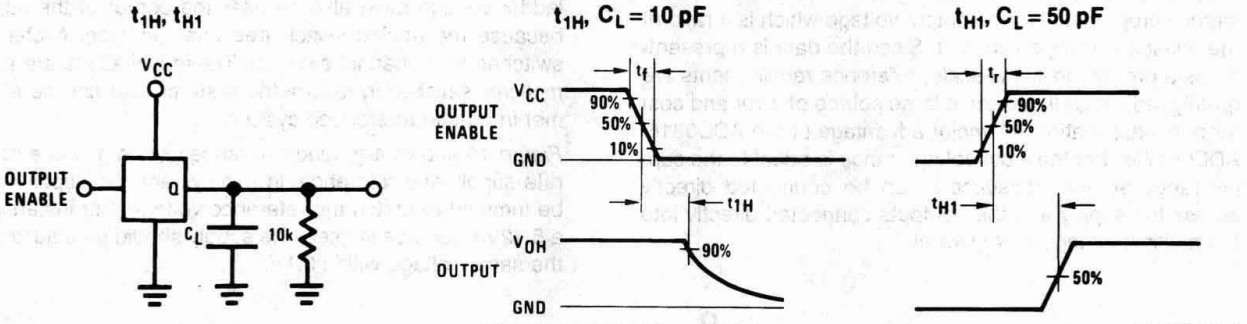
FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)



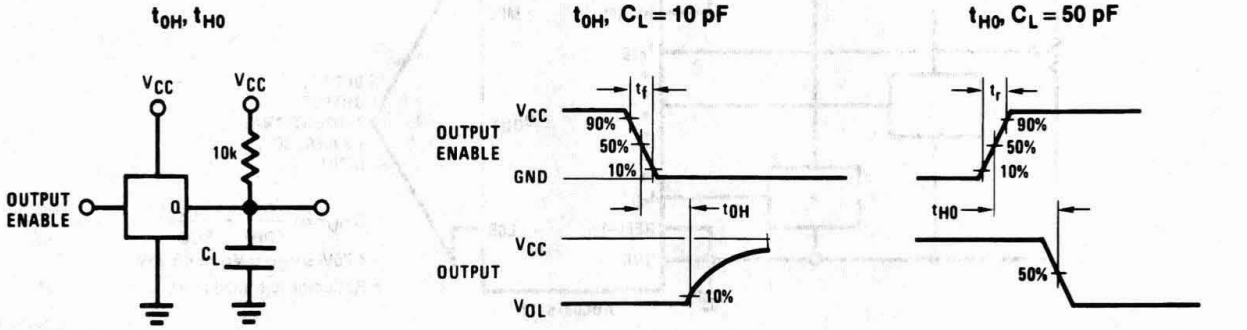
TL/H/5277–8

FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE Test Circuits and Timing Diagrams



TL/H/5277–9



TL/H/5277–10

FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} =$ 5.12V, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches These limitations are automaticaly satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

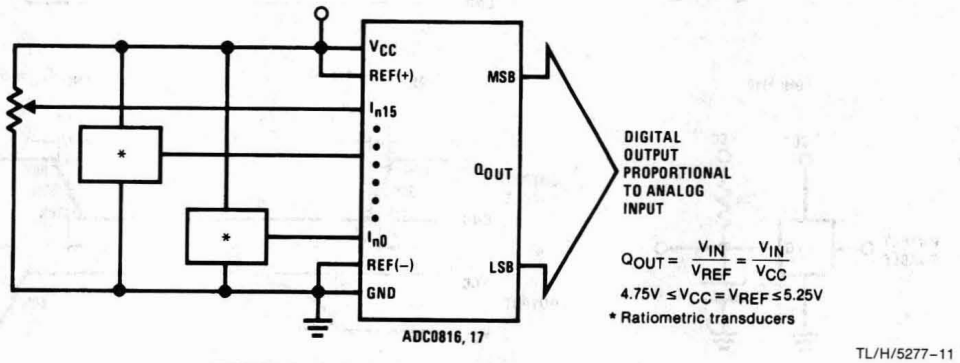


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground references system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the millliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.

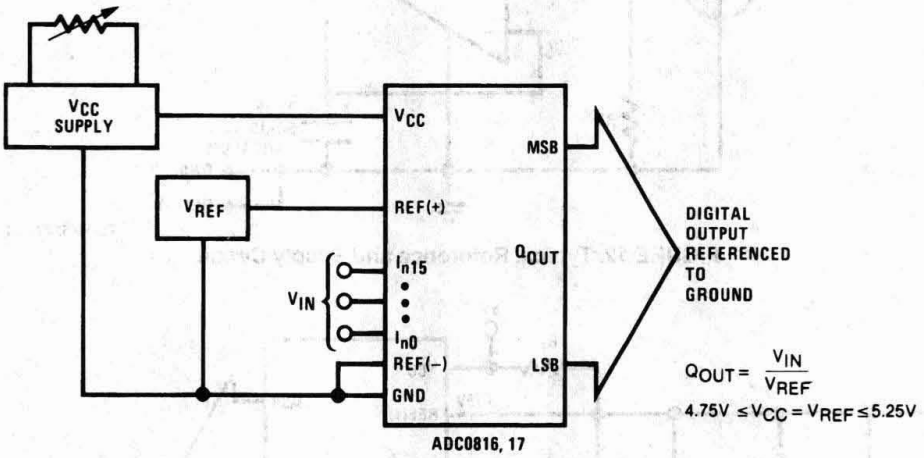


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

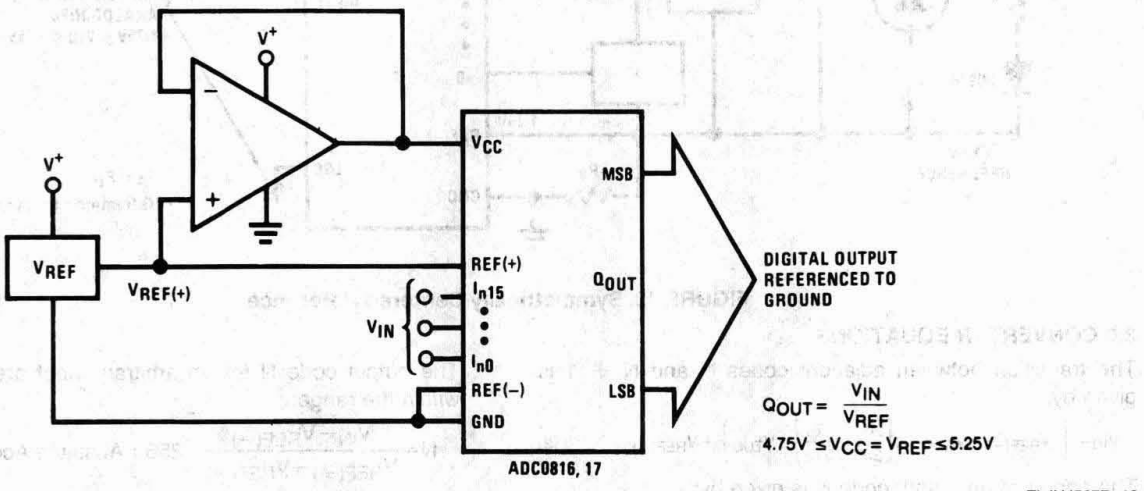
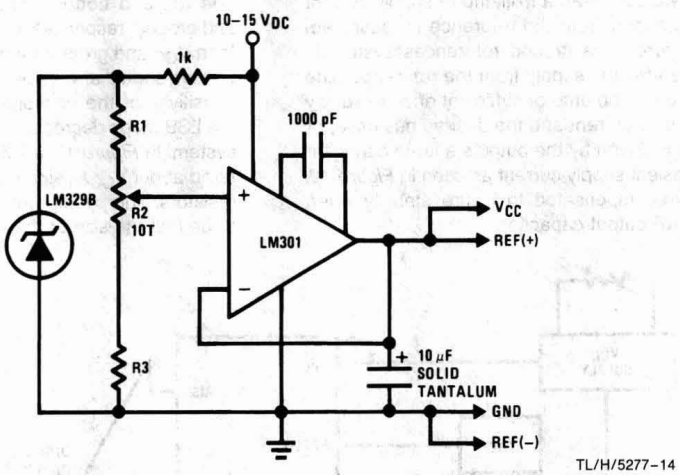


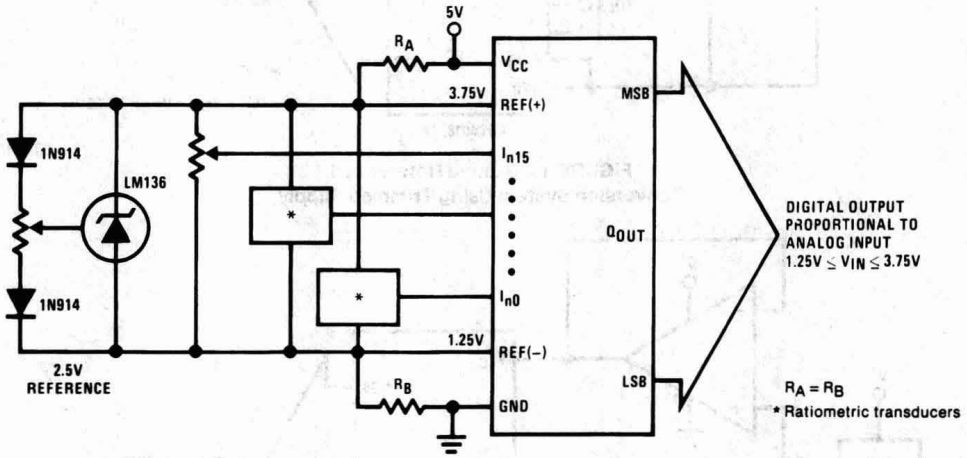
FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)



TL/H/5277–14

FIGURE 12. Typical Reference and Supply Circuit



TL/H/5277–15

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

V_{REF} = Voltage at Ref(+)

V_{REF} = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

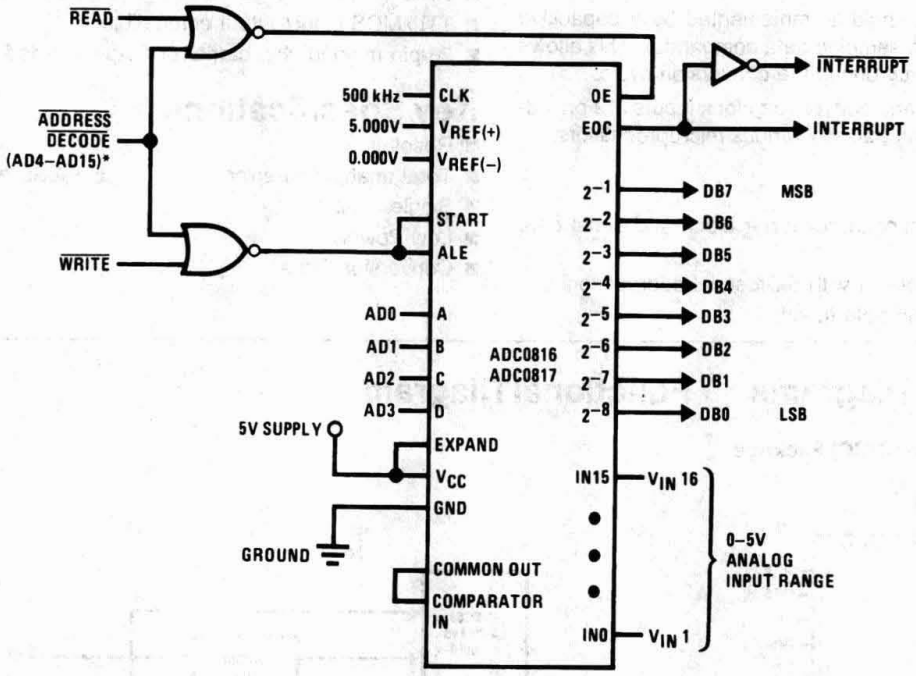
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application



TL/H/5277–16

*Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ 2•R/W	VMA•Q_2•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C	
Error	±½ Bit Unadjusted	ADC0816CCN	ADC0816CCJ
	±1 Bit Unadjusted	ADC0817CCN	
Package Outline		N40A Molded DIP	J40A Hermetic DIP

National Semiconductor

ADC0819 8-Bit Serial I/O A/D Converter with 19-Channel Multiplexer

General Description

The ADC0819 is an 8-Bit successive approximation A/D converter with simultaneous serial I/O. The serial input controls an analog multiplexer which selects from 19 input channels or an internal half scale test voltage.

An input sample-and-hold is implemented by a capacitive reference ladder and sampled data comparator. This allows the input signal to vary during the conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Features

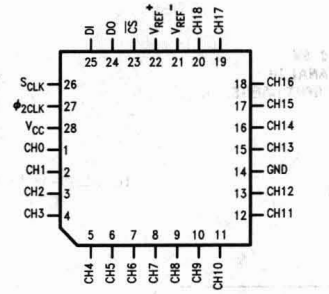
- Separate asynchronous converter clock and serial data I/O clock.
- 19-Channel multiplexer with 5-Bit serial address logic.
- Built-in sample and hold function.
- Ratiometric or absolute voltage referencing.
- No zero or full-scale adjust required.
- Internally addressable test voltage.
- 0V to 5V input range with single 5V power supply.
- TTL/MOS input/output compatible.
- 28-pin molded chip carrier or 28-pin molded DIP

Key Specifications

■ Resolution	8-Bits
■ Total unadjusted error	± ½LSB and ± 1LSB
■ Single supply	$5V_{DC}$
■ Low Power	15 mW
■ Conversion Time	16 μs

Connection Diagrams

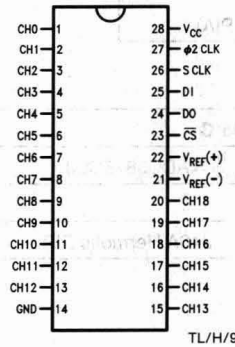
Molded Chip Carrier (PCC) Package



TL/H/9287–1

Top View
Order Number ADC0819BCV, CCV
See NS Package Number V28A

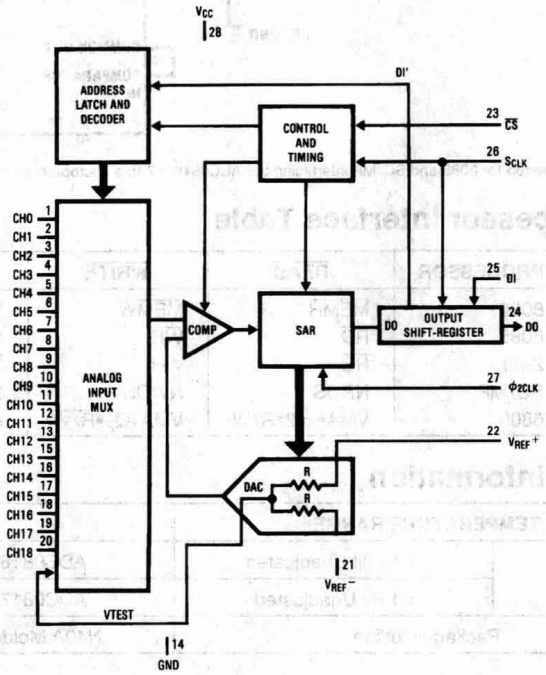
Dual-In-Line Package



TL/H/9287–20

Top View
Order Number ADC0819BCN, CIN
See NS Package Number N28B

Functional Diagram



TL/H/9287–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Inputs and Outputs	−0.3V to V_{CC} +0.3V
Input Current Per Pin (Note 3)	±5mA
Total Package Input Current (Note 3)	±20mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 11)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0819BCV, ADC0819CCV	$-40°C \le T_A \le +85°C$
ADC0819BCN	$0°C \le T_A \le +70°C$
ADC0819CIN	$-40°C \le T_A \le +85°C$

Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, $\phi_{2\,CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Maximum Total Unadjusted Error ADC0819BCV, BCN ADC0819CCV, CIN	V_{REF} = 5.00 V_{DC} (Note 4)		 ±½ ±1	 **±½** **±1**	 LSB LSB
Minimum Reference Input Resistance		8		**5**	kΩ
Maximum Reference Input Resistance		8	11	**11**	kΩ
Maximum Analog Input Range	(Note 5)		V_{CC} + 0.05	**V_{CC} + 0.05**	V
Minimum Analog Input Range			GND − 0.05	**GND − 0.05**	V
On Channel Leakage Current	(Note 9) On Channel = 5V Off Channel = 0V		400	**1000**	nA
	On Channel = 0V Off Channel = 5V (Note 9)		−400	**−1000**	nA
Off Channel Leakage Current	(Note 9) On Channel = 5V Off Channel = 0V		−400	**−1000**	nA
	On Channel = 0V Off Channel = 5V (Note 9)		400	**1000**	nA
Minimum V_{TEST} Internal Test Voltage	V_{REF} = V_{CC}, CH 19 Selected		125	**125**	(Note 10) Counts
Maximum V_{TEST} Internal Test Voltage	V_{REF} = V_{CC}, CH 19 Selected		130	**130**	(Note 10) Counts
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC} = 5.25V		2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC} = 4.75V		0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN} = 5.0V	0.005	2.5	**2.5**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	−2.5	**−2.5**	μA

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, $\phi_{2\,CLK}$ = 2.097 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 μA I_{OUT} = −10 μA		2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 5.25V I_{OUT} = 1.6 mA		0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	−3 3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	−6.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	8.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	2.5	**2.5**	mA
I_{REF} (Max)	V_{REF} = 5V	**0.7**	1	**1**	mA

AC CHARACTERISTICS

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
$\phi_{2\,CLK}$, ϕ_2 Clock Frequency	MIN		0.70		**1.0**	MHz
	MAX		4.0	2.0	**2.1**	
S_{CLK}, Serial Data Clock Frequency	MIN				**5.0**	KHz
	MAX		1000	525	**525**	
T_C, Conversion Process Time	MIN	Not Including MUX Addressing and Analog Input Sampling Times	26		**26**	ϕ_2 cycles
	MAX		32		**32**	
t_{ACC}, Access Time Delay From $\overline{CS}$	MIN				**1**	ϕ_2 cycles
Falling Edge to DO Data Valid	MAX				**3**	
$t_{SET\text{-}UP}$, Minimum Set-up Time of $\overline{CS}$ Falling Edge to S_{CLK} Rising Edge					$4/\phi_{2CLK} + \frac{1}{2\,S_{CLK}}$	sec
$t_{H\overline{CS}}$, $\overline{CS}$ Hold Time After the Falling Edge of S_{CLK}					**0**	ns
$t_{\overline{CS}}$, Total $\overline{CS}$ Low Time	MIN				$t_{set\text{-}up} + 8/S_{CLK}$	sec
	MAX				$t_{\overline{CS}}(min) + 26/\phi_{2CLK}$	sec
t_{HDI}, Minimum DI Hold Time from S_{CLK} Rising Edge			0		**0**	ns
t_{HDO}, Minimum DO Hold Time from S_{CLK} Falling Edge		R_L = 30k, C_L = 100 pF			**10**	ns
t_{SDI}, Minimum DI Set-up Time to S_{CLK} Rising Edge			200		**400**	ns
t_{DDO}, Maximum Delay From S_{CLK} Falling Edge to DO Data Valid		R_L = 30k, C_L = 100 pF	180	200	**250**	ns
t_{TRI}, Maximum DO Hold Time, ($\overline{CS}$ Rising edge to DO TRI-STATE)		R_L = 3k, C_L = 100 pF	90	150	**150**	ns

Electrical Characteristics

The following specifications apply for V_{CC} = 5V, $t_r = t_f = 20$ ns, V_{REF} = 5V, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Parameter	Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
AC CHARACTERISTICS (Continued)						
t_{CA}, Analog Sampling Time	After Address Is Latched $\overline{CS}$ = Low				**$3/S_{CLK} + 1\ \mu s$**	sec
t_{RDO}, Maximum DO Rise Time	R_L = 30 kΩ, C_L = 100 pf	"TRI-STATE" to "HIGH" State	75	150	**150**	ns
		"LOW" to "HIGH" State	150	300	**300**	
t_{FDO}, Maximum DO Fall Time	R_L = 30 kΩ, C_L = 100 pf	"TRI-STATE" to "LOW" State	75	150	**150**	ns
		"HIGH" to "LOW" State	150	300	**300**	
C_{IN}, Maximum Input Capacitance	Analog Inputs, AN0–AN10 and V_{REF}		11		**55**	pF
	All Others		5		**15**	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Under over voltage conditions ($V_{IN} < 0V$ and $V_{IN} > V_{CC}$) the maximum input current at any one pin is ±5 mA. If the voltage at more than one pin exceeds V_{CC} + .3V the total package current must be limited to 20 mA. For example the maximum number of pins that can be over driven at the maximum current level of ±5 mA is four.

Note 4: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 5: Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design Limits are guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

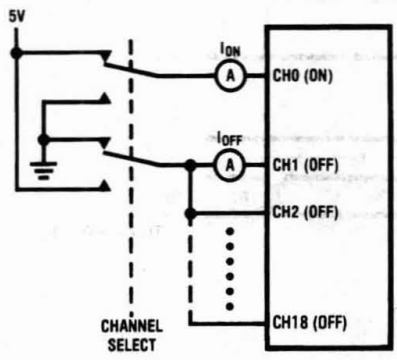
Note 9: Channel leakage current is measured after the channel selection.

Note 10: 1 count = $V_{REF}/256$.

Note 11: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

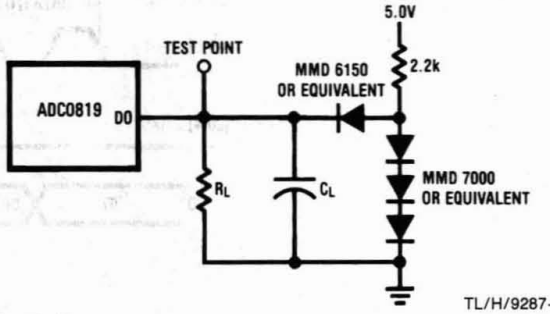
Test Circuits

Leakage Current



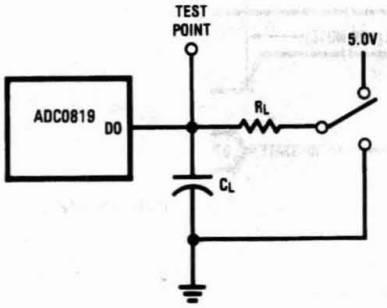
TL/H/9287–3

D0 Except "TRI-STATE"



TL/H/9287–4

t_{TRI} "TRI-STATE"



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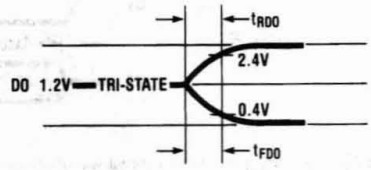
Timing Diagrams

D0 "TRI-STATE" Rise & Fall Times



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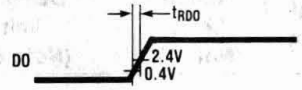
Timing Diagrams (Continued)

D0 Low to High State



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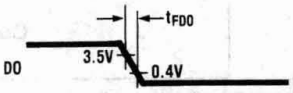
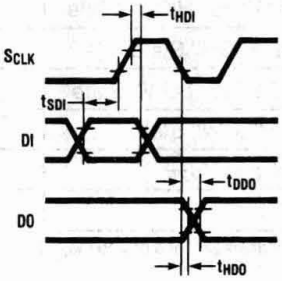
D0 High to Low State



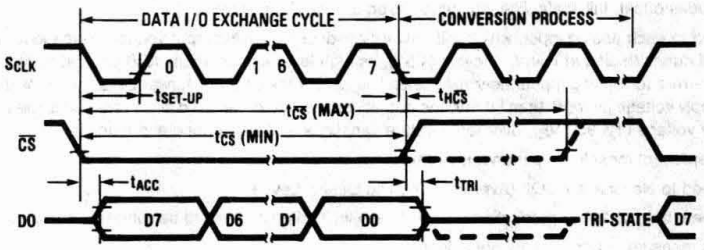
TL/H/9287–8

Data Input and Output Timing



TL/H/9287–9

Timing with a continuous S_{CLK}



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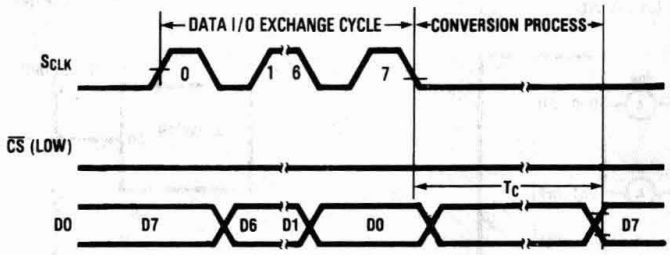
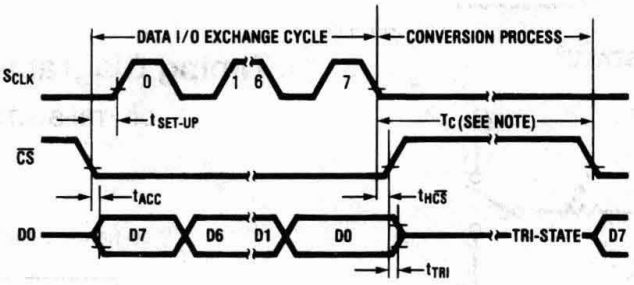
*Strobing $\overline{CS}$ High and Low will abort the present conversion and initiate a new serial I/O exchange.

Timing with a gated S_{CLK} and $\overline{CS}$ Continuously Low



TL/H/9287–11

Using $\overline{CS}$ To TRI-STATE D0

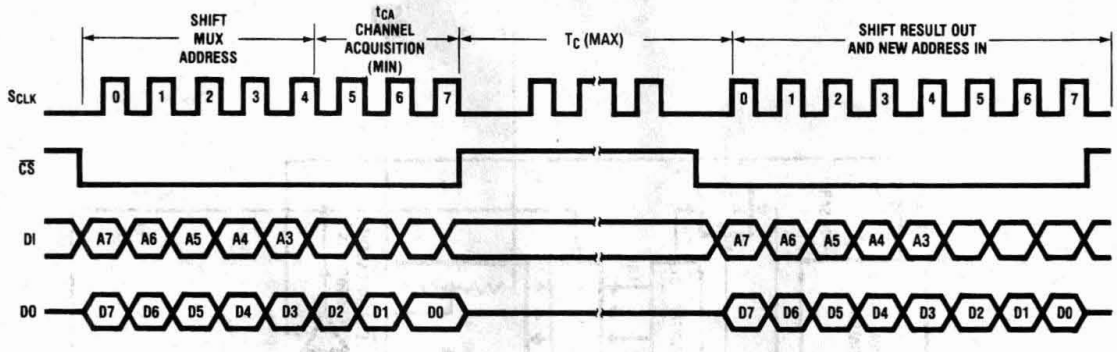


TL/H/9287–12

Note: Strobing $\overline{CS}$ Low during this time interval will abort the conversion in process.

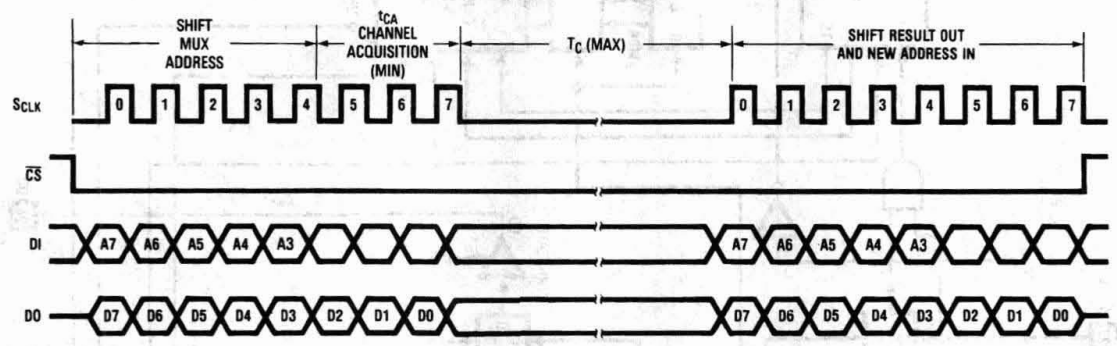
Timing Diagrams (Continued)

$\overline{CS}$ High During Conversion



TL/H/9287–13

$\overline{CS}$ Low During Conversion



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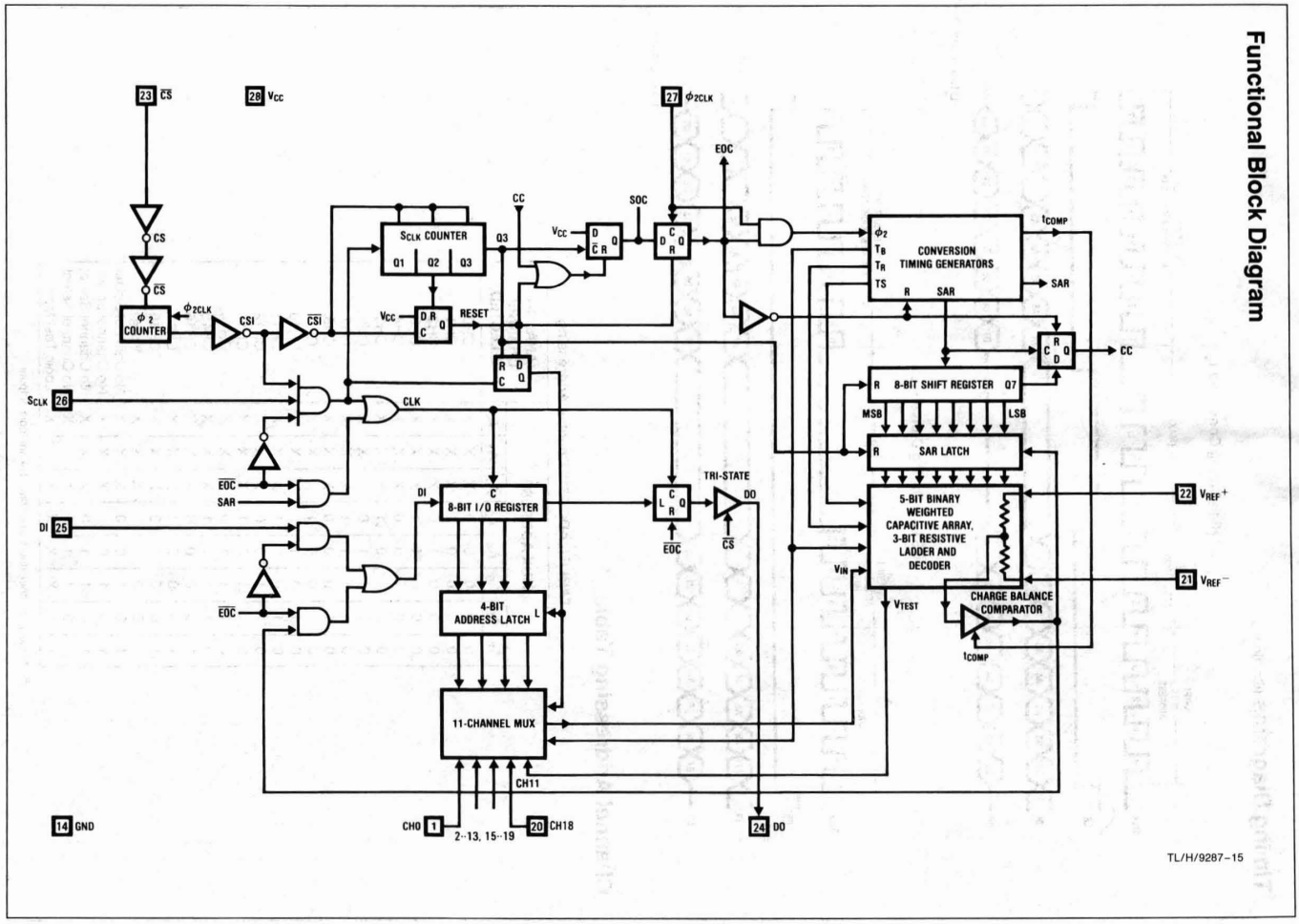
Channel Addressing Table

TABLE I. ADC 0819 Channel Addressing

MUX ADDRESS								ANALOG CHANNEL SELECTED
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	X	X	X	CH0
0	0	0	0	1	X	X	X	CH1
0	0	0	1	0	X	X	X	CH2
0	0	0	1	1	X	X	X	CH3
0	0	1	0	0	X	X	X	CH4
0	0	1	0	1	X	X	X	CH5
0	0	1	1	0	X	X	X	CH6
0	0	1	1	1	X	X	X	CH7
0	1	0	0	0	X	X	X	CH8
0	1	0	0	1	X	X	X	CH9
0	1	0	1	0	X	X	X	CH10
0	1	0	1	1	X	X	X	CH11
0	1	1	0	0	X	X	X	CH12
0	1	1	0	1	X	X	X	CH13
0	1	1	1	0	X	X	X	CH14
0	1	1	1	1	X	X	X	CH15
1	0	0	0	0	X	X	X	CH16
1	0	0	0	1	X	X	X	CH17
1	0	0	1	0	X	X	X	CH18
1	0	0	1	1	X	X	X	V_{TEST}
1	0	1	0	0	X	X	X	No Channel Select
1	0	1	0	1	X	X	X	No Channel Select
1	0	1	1	0	X	X	X	No Channel Select
1	0	1	1	1	X	X	X	No Channel Select
1	1	X	X	X	X	X	X	Logic Test Mode*

*Analog channel inputs CH0 thru CH4 are logic outputs

Functional Block Diagram



TL/H/9287–15

Functional Description

1.0 DIGITAL INTERFACE

The ADC0819 uses five input/output pins to implement the serial interface. Taking chip select ($\overline{CS}$) low enables the I/O data lines (DO and DI) and the serial clock input (S_{CLK}). The result of the last conversion is transmitted by the A/D on the DO line, while simultaneously the DI line receives the address data that selects the mux channel for the next conversion. The mux address is shifted in on the rising edge of S_{CLK} and the conversion data is shifted out on the falling edge. It takes eight S_{CLK} cycles to complete the serial I/O. A second clock (ϕ_2) controls the SAR during the conversion process and must be continuously enabled.

1.1 CONTINUOUS S_{CLK}

With a continuous S_{CLK} input $\overline{CS}$ must be used to synchronize the serial data exchange (see *Figure 1*). The ADC0819 recognizes a valid $\overline{CS}$ one to three ϕ_2 clock periods after the actual falling edge of $\overline{CS}$. This is implemented to ensure noise immunity of the $\overline{CS}$ signal. Any spikes on $\overline{CS}$ less than one ϕ_2 clock period will be ignored. $\overline{CS}$ must remain low during the complete I/O exchange which takes eight S_{CLK} cycles. Although $\overline{CS}$ is not immediately acknowledged for the purpose of starting a new conversion, the falling edge of $\overline{CS}$ immediately enables DO to output the MSB (D7) of the previous conversion.

The first S_{CLK} rising edge will be acknowledged after a set-up time ($t_{set\text{-}up}$) has elapsed from the falling edge of $\overline{CS}$. This and the following seven S_{CLK} rising edges will shift in the channel address for the analog multiplexer. Since there are 19 channels only five address bits are utilized. The first five S_{CLK} cycles clock in the mux address, during the next three S_{CLK} cycles the analog input is selected and sampled. During this mux address/sample cycle, data from the last conversion is also clocked out on DO. Since D7 was clocked out on the falling edge of $\overline{CS}$ only data bits D6–D0 remain to be received. The following seven falling edges of S_{CLK} shift out this data on DO.

The 8th S_{CLK} falling edge initiates the beginning of the A/D's actual conversion process which takes between 26 and 32 ϕ_2 cycles (T_C). During this time $\overline{CS}$ can go high to TRI-STATE DO and disable the S_{CLK} input or it can remain low. If $\overline{CS}$ is held low a new I/O exchange will not start until the conversion sequence has been completed, however once the conversion ends serial I/O will immediately begin. Since there is an ambiguity in the conversion time (T_C) synchronizing the data exchange is impossible. Therefore $\overline{CS}$ should go high before the 26th ϕ_2 clock has elasped and return low after the 32nd ϕ_2 to synchronize serial communication.

A conversion or I/O operation can be aborted at any time by strobing $\overline{CS}$. If $\overline{CS}$ is high or low less than one ϕ_2 clock it will be ignored by the A/D. If the $\overline{CS}$ is strobed high or low between 1 to 3 ϕ_2 clocks the A/D may or may not respond. Therefore $\overline{CS}$ must be strobed high or low greater than 3 ϕ_2 clocks to ensure recognition. If a conversion or I/O exchange is aborted while in process the consequent data output will be erroneous until a complete conversion sequence has been implemented.

1.2 DISCONTINUOUS S_{CLK}

Another way to accomplish synchronous serial communication is to tie $\overline{CS}$ low continuously and disable S_{CLK} after its 8th falling edge (see *Figure 2*). S_{CLK} must remain low for

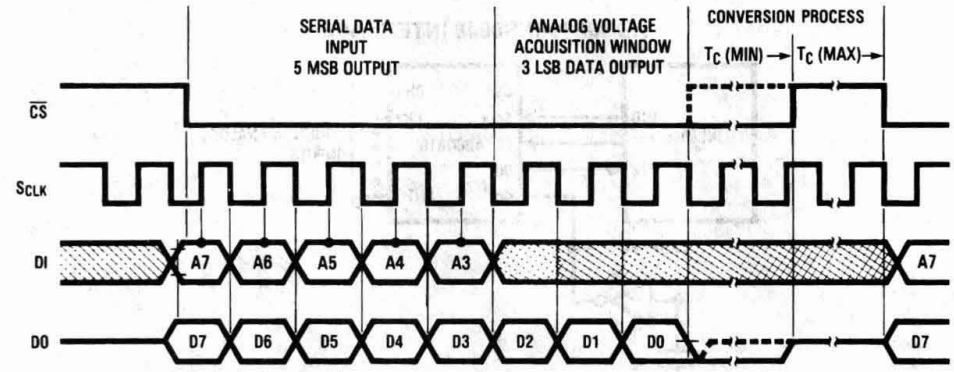


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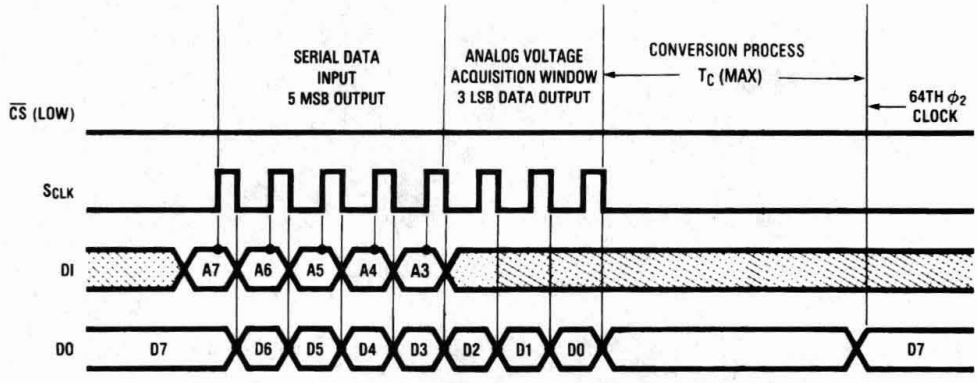
FIGURE 1



TL/H/9287–17

FIGURE 2

Functional Description (Continued)

at least 32 ϕ_2 clocks to ensure that the A/D has completed its conversion. If S_{CLK} is enabled sooner, synchronizing to the data output on DO is not possible since an end of conversion signal from the A/D is not available and the actual conversion time is not known. With $\overline{CS}$ low during the conversion time (32 ϕ_2 max) DO will go high or low after the eighth falling edge of S_{CLK} until the conversion is completed. Once the conversion is through DO will transmit the MSB. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously.

If $\overline{CS}$ goes high during the conversion sequence DO is tri-stated, and the result is not affected so long as $\overline{CS}$ remains high until the end of the conversion.

1.2 MULTIPLEXER ADDRESSING

The five bit mux address is shifted, MSB first, into DI. Input data corresponds to the channel selected as shown in table 1. Care should be taken not to send an address greater than or equal to twenty four (11XXX) as this puts the A/D in a digital testing mode. In this mode the analog inputs CH0 thru CH4 become digital outputs, for our use in production testing.

2.0 ANALOG INPUT

2.1 THE INPUT SAMPLE AND HOLD

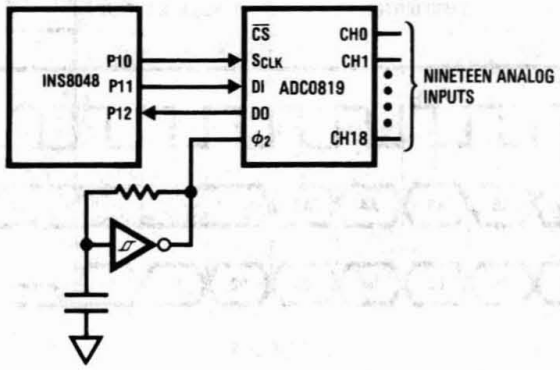
The ADC0819's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for 1 μsec after the eighth S_{CLK} falling edge. The hold mode is initiated with the start of the conversion process. An acquisition window of $3t_{SCLK}+1$ μsec is therefore available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (3K) of the multiplexer switches and the total ladder capacitance (90pf). These values yield an acquisition time of about 2 μsec for a full scale reading. Therefore the analog input must be stable for at least 2 μsec before and 1 μsec after the eighth S_{CLK} falling edge to ensure a proper conversion. External input source resistance and capacitance will lengthen the acquisition time and should be accounted for.

Other conventional sample and hold error specifications are included in the error and timing specs of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC0819's total unadjusted error, while the hold settling time is included in the A/D's max conversion time of 32 ϕ_2 clock periods. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

Typical Applications

ADC0819-INS8048 INTERFACE



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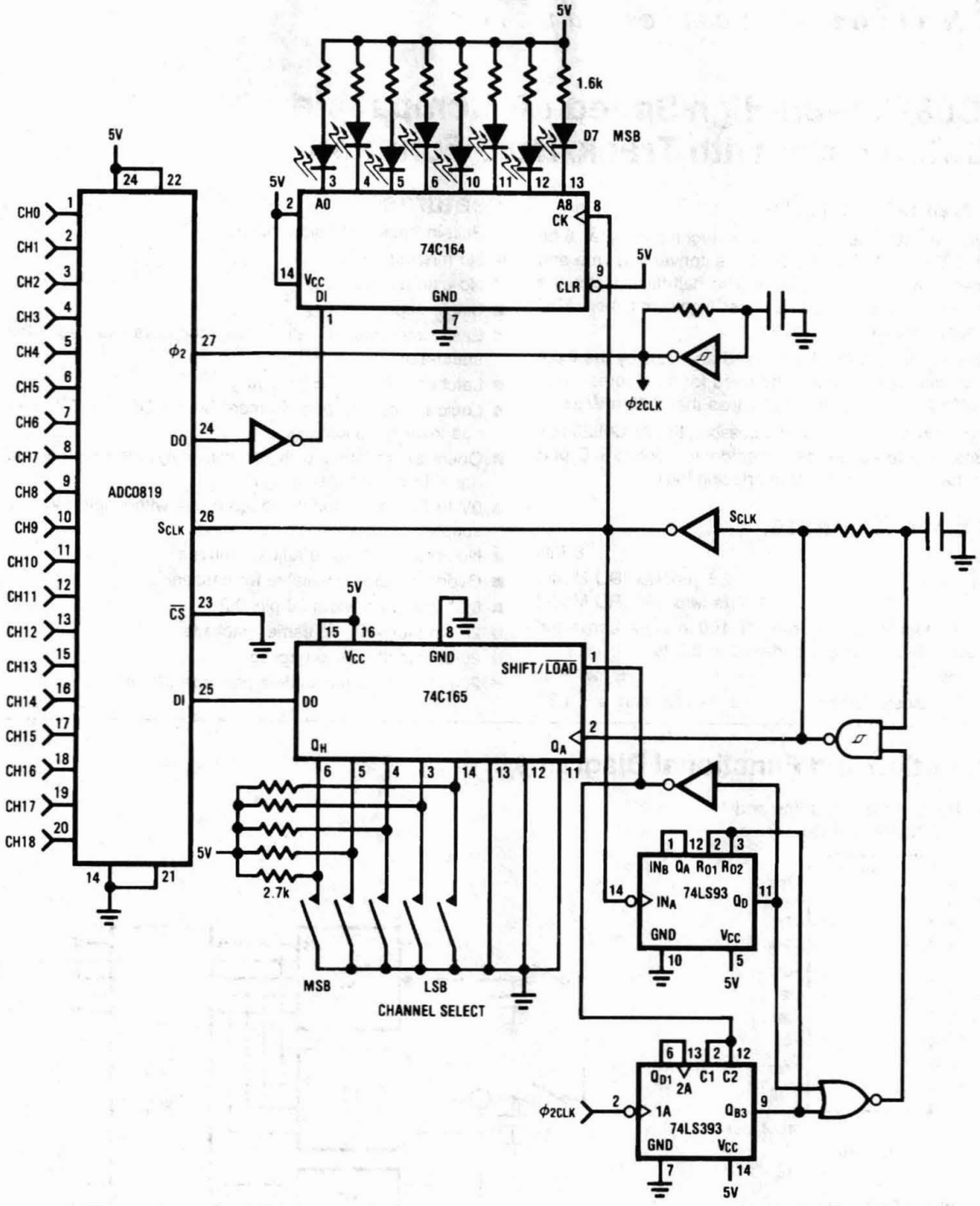
ADC0819 FUNCTIONAL CIRCUIT



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Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	
Total Unadjusted Error	±½ LSB	ADC0819BCN	ADC0819BCV	
	±1 LSB		ADC0819CCV	ADC0819CIN
Package Outline		N28B	V28A	N28B

National Semiconductor

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 μs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

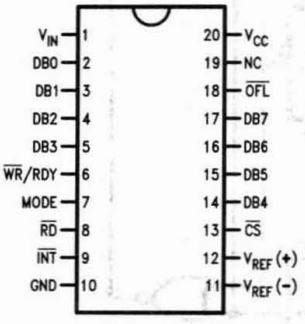
- Resolution — 8 Bits
- Conversion Time — 2.5 μs Max (RD Mode); 1.5 μs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/μs converted without external sample-and-hold to 8 bits
- Low Power — 75 mW Max
- Total Unadjusted Error — ± ½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3″ standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

Connection and Functional Diagrams

Dual-In-Line, Small Outline and SSOP Packages



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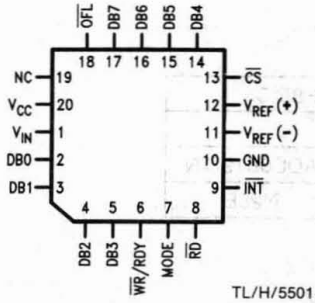
Top View

Molded Chip Carrier Package



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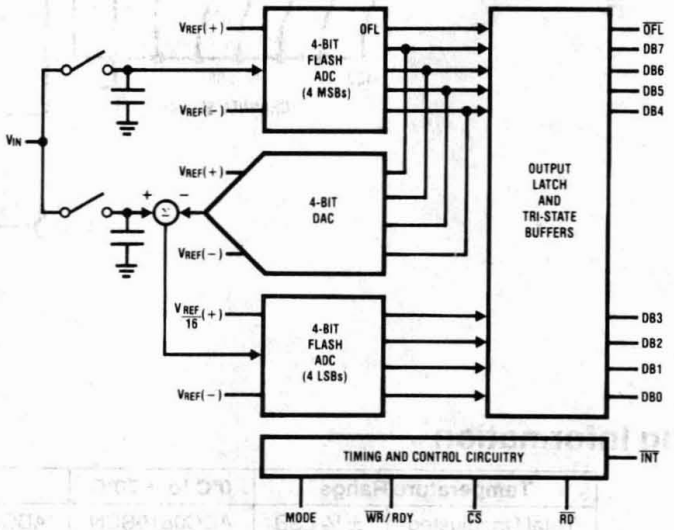


TL/H/5501–2

FIGURE 1

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	10V
Logic Control Inputs	−0.2V to V_{CC} +0.2V
Voltage at Other Inputs and Output	−0.2V to V_{CC} +0.2V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Input Current at Any Pin (Note 5)	1 mA
Package Input Current (Note 5)	4 mA
ESD Susceptability (Note 9)	1200V
Lead Temp. (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0820CCJ	−40°C ≤ T_A ≤ +85°C
ADC0820CIWM	−40°C ≤ T_A ≤ +85°C
ADC0820BCN, ADC0820CCN	0°C ≤ T_A ≤ 70°C
ADC0820BCV, ADC0820CCV	0°C ≤ T_A ≤ 70°C
ADC0820BCWM, ADC0820CCWM	0°C ≤ T_A ≤ 70°C
ADC0820CCMSA	0°C ≤ T_A ≤ 70°C
V_{CC} Range	4.5V to 8V

Converter Characteristics

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = 5V, $V_{REF}(+)$ = 5V, and $V_{REF}(-)$ = GND unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM ADC0820CCMSA, ADC0820CIWM			Limit Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
Resolution			**8**			8	**8**	Bits
Total Unadjusted Error (Note 3)	ADC0820BCN, BCWM					±½	**±½**	LSB
	ADC0820CCJ		**±1**					LSB
	ADC0820CCN, CCWM, CIWM,					±1	**±1**	LSB
	ADC0820CCMSA					±1	**±1**	LSB
Minimum Reference Resistance		2.3	**1.00**		2.3	1.2		kΩ
Maximum Reference Resistance		2.3	**6**		2.3	5.3	**6**	kΩ
Maximum $V_{REF}(+)$ Input Voltage			**V_{CC}**			V_{CC}	**V_{CC}**	V
Minimum $V_{REF}(-)$ Input Voltage			**GND**			GND	**GND**	V
Minimum $V_{REF}(+)$ Input Voltage			**$V_{REF}(-)$**			$V_{REF}(-)$	**$V_{REF}(-)$**	V
Maximum $V_{REF}(-)$ Input Voltage			**$V_{REF}(+)$**			$V_{REF}(+)$	**$V_{REF}(+)$**	V
Maximum V_{IN} Input Voltage			**V_{CC} + 0.1**			V_{CC} + 0.1	**V_{CC} + 0.1**	V
Minimum V_{IN} Input Voltage			**GND − 0.1**			GND − 0.1	**GND − 0.1**	V
Maximum Analog Input Leakage Current	$\overline{CS} = V_{CC}$							
	$V_{IN} = V_{CC}$		**3**			0.3	**3**	µA
	V_{IN} = GND		**−3**			−0.3	**−3**	µA
Power Supply Sensitivity	V_{CC} = 5V ± 5%	±1/16	±¼		±1/16	±¼	±¼	LSB

DC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Parameter	Conditions		ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM ADC0820CCMSA, ADC0820CIWM			Limit Units
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**2.0**			2.0	**2.0**	V
		Mode		**3.5**			3.5	**3.5**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**0.8**			0.8	**0.8**	V
		Mode		**1.5**			1.5	**1.5**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)} = 5V$; $\overline{CS}$, $\overline{RD}$		0.005	**1**		0.005		**1**	μA
	$V_{IN(1)} = 5V$; $\overline{WR}$		0.1	**3**		0.1	0.3	**3**	μA
	$V_{IN(1)} = 5V$; Mode		50	**200**		50	170	**200**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)} = 0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	**−1**		−0.005		**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = -360$ μA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**2.4**			2.8	**2.4**	V
	$V_{CC} = 4.75V$, $I_{OUT} = -10$ μA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 1.6$ mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current	$V_{OUT} = 5V$; DB0–DB7, RDY		0.1	**3**		0.1	0.3	**3**	μA
	$V_{OUT} = 0V$; DB0–DB7, RDY		−0.1	**−3**		−0.1	−0.3	**−3**	μA
I_{SOURCE}, Output Source Current	$V_{OUT} = 0V$; DB0–DB7, $\overline{OFL}$		−12	**−6**		−12	−7.2	**−6**	mA
	$\overline{INT}$		−9	**−4.0**		−9	−5.3	**−4.0**	mA
I_{SINK}, Output Sink Current	$V_{OUT} = 5V$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	**7**		14	8.4	**7**	mA
I_{CC}, Supply Current	$\overline{CS} = \overline{WR} = \overline{RD} = 0$		7.5	**15**		7.5	13	**15**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $V_{REF}(+) = 5V$, $V_{REF}(-) = 0V$ and $T_A = 25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0, *(Figure 2)*	1.6		2.5	μs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0, *(Figure 2)*	$t_{CRD} + 20$		$t_{CRD} + 50$	ns
t_{CWR-RD}, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; t_{WR} = 600 ns, t_{RD} = 600 ns; *(Figures 3a* and *3b)*			1.52	μs
t_{WR}, Write Time	Min	Pin 7 = V_{CC}; *(Figures 3a* and *3b)*		600		ns
	Max	(Note 4) See Graph	50			μs
t_{RD}, Read Time	Min	Pin 7 = V_{CC}; *(Figures 3a* and *3b)* (Note 4) See Graph		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD} < t_l$; *(Figure 3a)* C_L = 15 pF	190		280	ns
		C_L = 100 pF	210		320	ns
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD} > t_l$; *(Figure 3b)* C_L = 15 pF	70		120	ns
		C_L = 100 pF	90		150	ns
t_{ACC3}, Access Time (Delay from Rising Edge of RDY to Output Valid)		R_{PULLUP} = 1k and C_L = 15 pF	30			ns

AC Electrical Characteristics (Continued) The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Ncte 8)	Units
t_I, Internal Comparison Time	Pin 7 = V_{CC}; *(Figures 3b* and *4)* $C_L=50$ pF	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L=1k$, $C_L=10$ pF	100		200	ns
$t_{\overline{INT}L}$, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = V_{CC}, $C_L=50$ pF $t_{RD}>t_I$; *(Figure 3b)* $t_{RD}<t_I$; *(Figure 3a)*	 $t_{RD}+200$		 t_I $t_{RD}+290$	 ns ns
$t_{\overline{INT}H}$, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	*(Figures 2, 3a* and *3b)* $C_L=50$ pF	125		225	ns
$t_{\overline{INT}HWR}$, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	*(Figure 4)*, $C_L=50$ pF	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY	*(Figure 2)*, $C_L=50$ pF, Pin 7 = 0	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid	*(Figure 4)*	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7 = V_{CC}, $t_{RD}<t_I$ *(Figure 3a)*	200		290	ns
t_P, Delay from End of Conversion to Next Conversion	*(Figures 2, 3a, 3b* and *4)* (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/μs
C_{VIN}, Analog Input Capacitance		45			pF
C_{OUT}, Logic Output Capacitance		5			pF
C_{IN}, Logic Input Capacitance		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RD} graphs.

Note 5: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

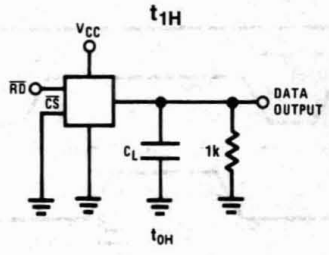
Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: Human body model, 100 pF discharaged through a 1.5 kΩ resistor.

TRI-STATE Test Circuits and Waveforms



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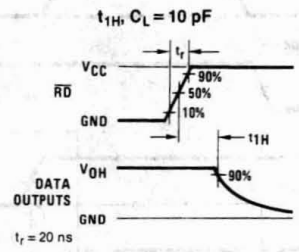
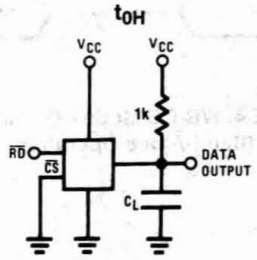
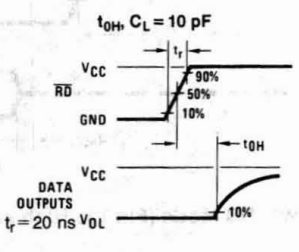


TL/H/5501–4



TL/H/5501–5



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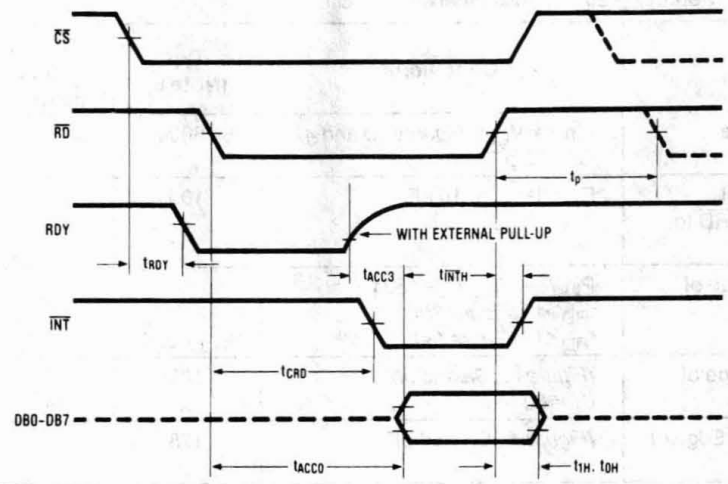
Timing Diagrams



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Note: On power-up the state of $\overline{INT}$ can be high or low.

FIGURE 2. RD Mode (Pin 7 is Low)

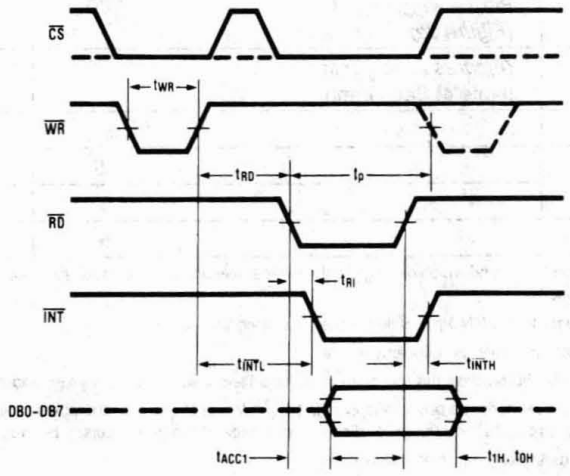

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FIGURE 3a. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)

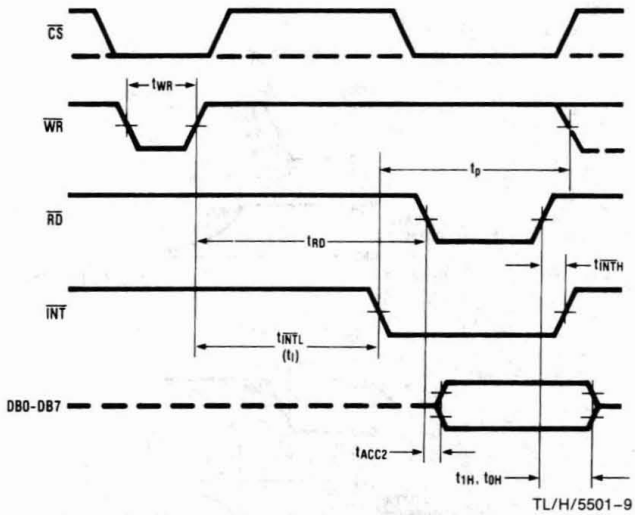

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FIGURE 3b. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

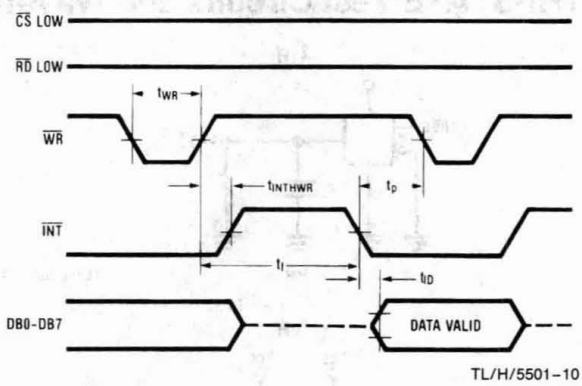

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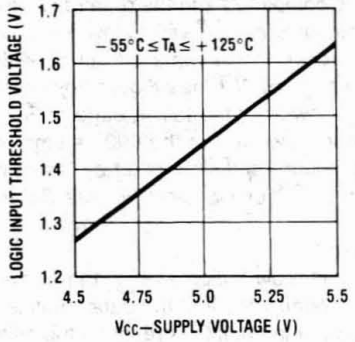
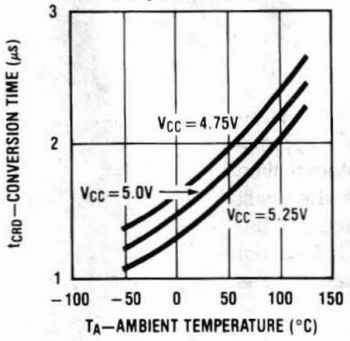
FIGURE 4. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

Typical Performance Characteristics

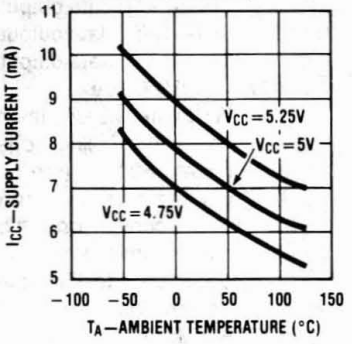
Logic Input Threshold Voltage vs Supply Voltage



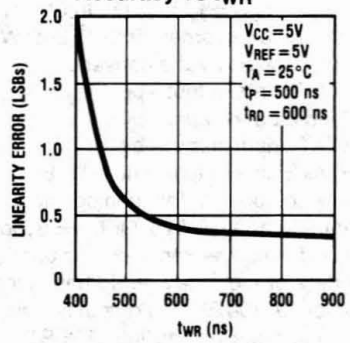
Conversion Time (RD Mode) vs Temperature



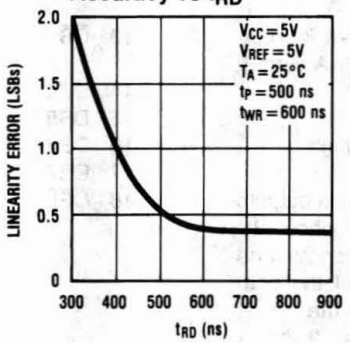
Power Supply Current vs Temperature (not including reference ladder)



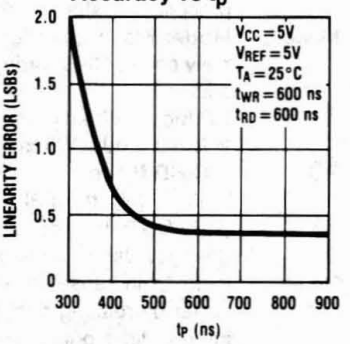
Accuracy vs t_{WR}



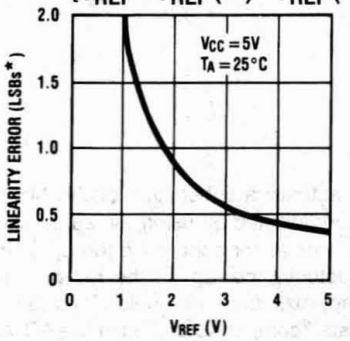
Accuracy vs t_{RD}



Accuracy vs t_p

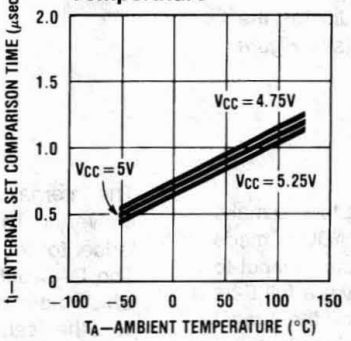


Accuracy vs V_{REF}
[$V_{REF} = V_{REF}(+) - V_{REF}(-)$]

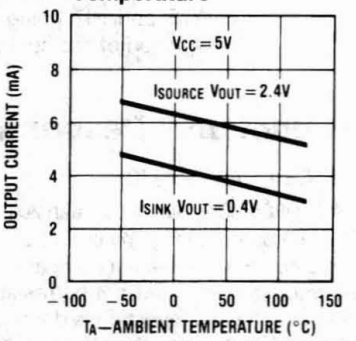


*1 LSB = $\frac{V_{REF}}{256}$

t_I, Internal Time Delay vs Temperature



Output Current vs Temperature



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Description of Pin Functions

Pin	Name	Function
1	V_{IN}	Analog input; range = GND ≤ V_{IN} ≤ V_{CC}
2	DB0	TRI-STATE data output—bit 0 (LSB)
3	DB1	TRI-STATE data output—bit 1
4	DB2	TRI-STATE data output—bit 2
5	DB3	TRI-STATE data output—bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** **$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800 ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see *Figures 3a* and *3b*). **RD Mode** **RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see *Figure 2*).
7	Mode	**Mode:** Mode selection input—it is internally tied to GND through a 50 μA current source. **RD Mode:** When mode is low **WR-RD Mode:** When mode is high
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ low, the TRI-STATE data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes low (see *Figure 4*). $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_I, ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see *Figures 3a* and *3b*). **RD Mode** With $\overline{CS}$ low, the conversion will start with $\overline{RD}$ going low, also $\overline{RD}$ will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and $\overline{INT}$ going low indicates the completion of the conversion (see *Figure 2*).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go low, ~800 ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see *Figure 3b*); or $\overline{INT}$ will go low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes low prior to the 800 ns time out (see *Figure 3a*). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figures 3a* and *3b*). **RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figure 2*).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: GND ≤ $V_{REF}(-)$ ≤ $V_{REF}(+)$ (Note 5)
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-)$ ≤ $V_{REF}(+)$ ≤ V_{CC} (Note 5)
13	$\overline{CS}$	$\overline{CS}$ must be low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	TRI-STATE data output—bit 4
15	DB5	TRI-STATE data output—bit 5
16	DB6	TRI-STATE data output—bit 6
17	DB7	TRI-STATE data output—bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—If the analog input is higher than the $V_{REF}(+)$, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). This output is always active and does not go into TRI-STATE as DB0–DB7 do.
19	NC	No connection
20	V_{CC}	Power supply voltage

1.0 Functional Description

1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (*Figure 1*). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled-data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

1.0 Functional Description (Continued)

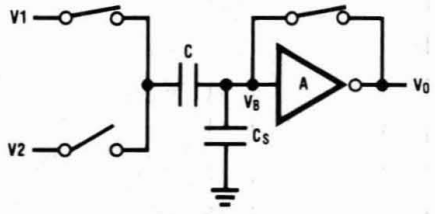
1.2 THE SAMPLED-DATA COMPARATOR

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (*Figure 5*). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (*Figure 5a*) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_B, approximately 1.2V). In the second cycle (*Figure 5b*), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_B') becomes

$$V_B - (V1 - V2)\frac{C}{C + C_S}$$

and the output will go high or low depending on the sign of $V_B' - V_B$.



TL/H/5501–12

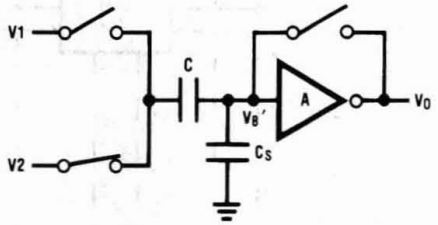
- $V_O = V_B$
- V on C = $V1 - V_B$
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

FIGURE 5a. Zeroing Phase

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (*Figure 6*), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (*Figure 7*). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

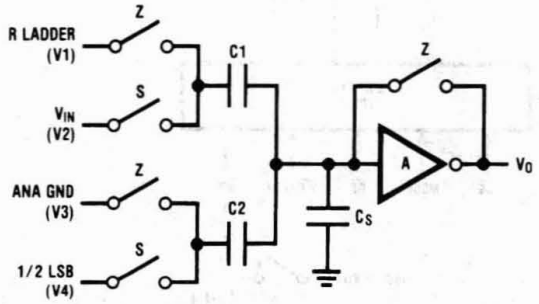


TL/H/5501–13

- $V_B' - V_B = (V2 - V1)\frac{C}{C + C_S}$
- $V_O' = \frac{-A}{C + C_S}[CV2 - CV1]$
- V_O' is dependent on V2 − V1

FIGURE 5b. Compare Phase

FIGURE 5. Sampled-Data Comparator



$$V_O = \frac{-A}{C1 + C2 + C_S}[C1(V2 - V1) + C2(V4 - V3)]$$

$$= \frac{-A}{C1 + C2 + C_S}[\Delta Q_{C1} + \Delta Q_{C2}]$$

TL/H/5501–14

FIGURE 6. ADC0820 Comparator (from MS Flash ADC)

Detailed Block Diagram

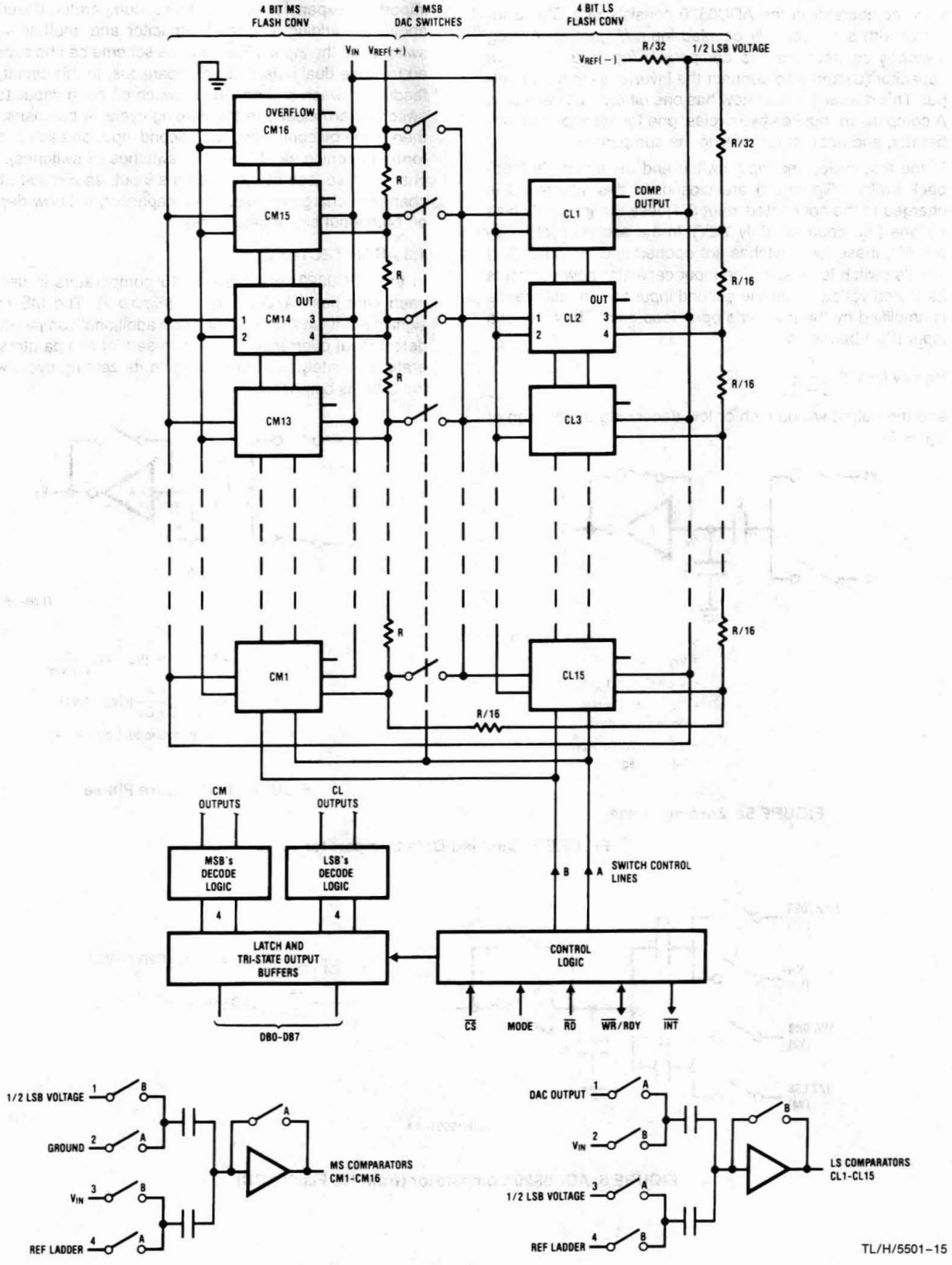


FIGURE 7

1.0 Functional Description (Continued)

When a typical conversion is started, the $\overline{WR}$ line is brought low. At this instant the MS comparators go from zeroing to comparison mode (*Figure 8*). When $\overline{WR}$ is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the $\overline{RD}$ line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When $\overline{RD}$ goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is low. In RD mode, sampling occurs during the first 800 ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

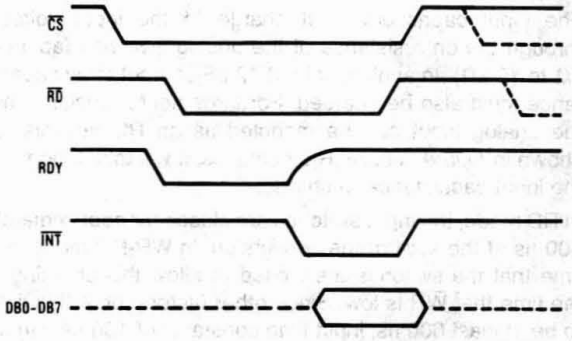
1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ low until output data appears. An $\overline{INT}$ line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

RD Mode (Pin 7 is Low)



TL/H/5501–16

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for $\overline{INT}$ to go low before reading the conversion result (*Figure B*). $\overline{INT}$ will typically go low 800 ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 600 ns (*Figure A*). If this is done, $\overline{INT}$ will immediately go low and data will appear at the outputs.

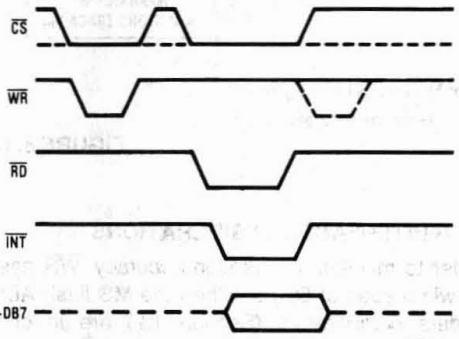


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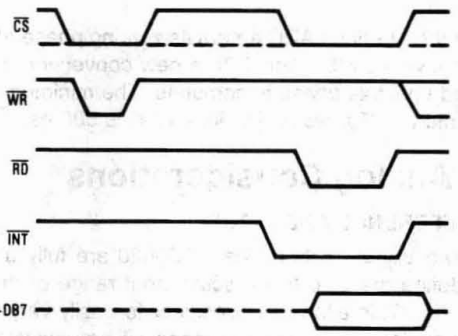
FIGURE A. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)



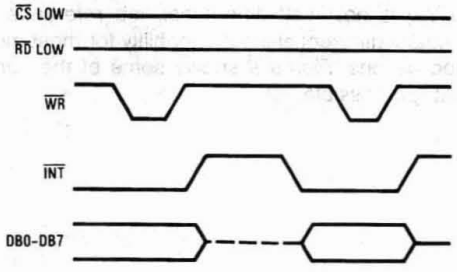
TL/H/5501–18

FIGURE B. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

Stand-Alone

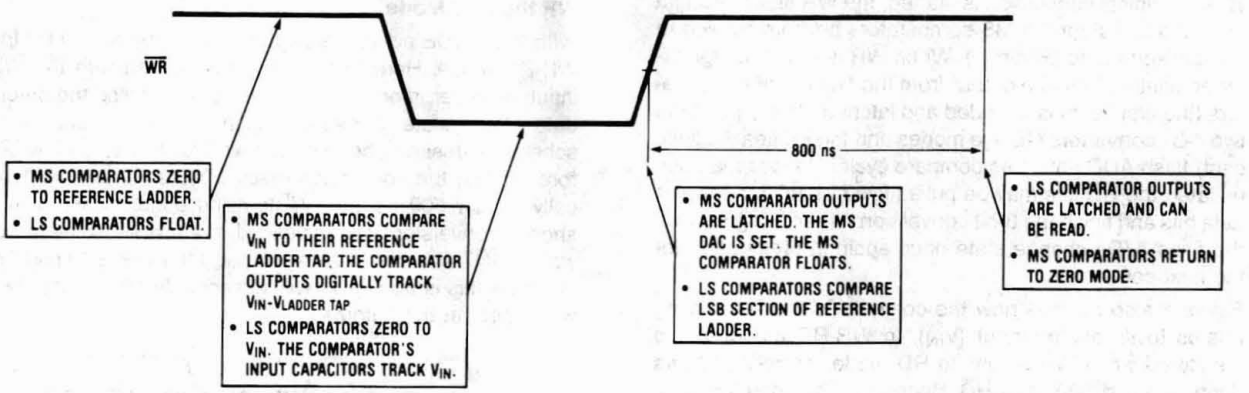
For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800 ns following $\overline{WR}$'s rising edge.

WR-RD Mode (Pin 7 is High) Stand-Alone Operation



TL/H/5501–19

1.0 Functional Description (Continued)


WR
• MS COMPARATORS ZERO TO REFERENCE LADDER.
• LS COMPARATORS FLOAT.
• MS COMPARATORS COMPARE V_{IN} TO THEIR REFERENCE LADDER TAP. THE COMPARATOR OUTPUTS DIGITALLY TRACK V_{IN}-$V_{LADDER\ TAP}$
• LS COMPARATORS ZERO TO V_{IN}. THE COMPARATOR'S INPUT CAPACITORS TRACK V_{IN}.
800 ns
• MS COMPARATOR OUTPUTS ARE LATCHED. THE MS DAC IS SET. THE MS COMPARATOR FLOATS.
• LS COMPARATORS COMPARE LSB SECTION OF REFERENCE LADDER.
• LS COMPARATOR OUTPUTS ARE LATCHED AND CAN BE READ.
• MS COMPARATORS RETURN TO ZERO MODE.

TL/H/5501–20

Note: MS means most significant
LS means least significant

FIGURE 8. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50 μs. When the MS flash ADC's sampled-data comparators (Section 1.2) are in comparison mode ($\overline{WR}$ is low), the input capacitors (C, *Figure 6*) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_P, *Figures 2, 3a, 3b,* and *4*) is 500 ns.

2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing V_{REF}($V_{REF} = V_{REF}(+) - V_{REF}(-)$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF} = 2V$ then 1 LSB = 7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. *Figure 9* shows some of the configurations that are possible.

2.2 INPUT CURRENT

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

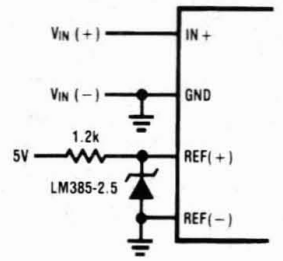
The equivalent input circuit of the ADC0820 is shown in *Figure 10a*. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in *Figure 10b*. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be 1.5 kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

2.0 Analog Considerations (Continued)

External Reference 2.5V Full-Scale



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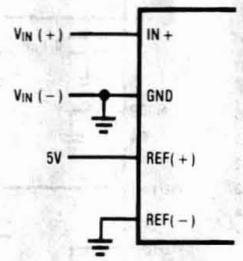
Power Supply as Reference



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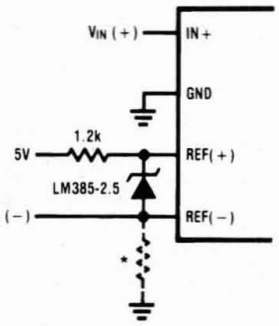
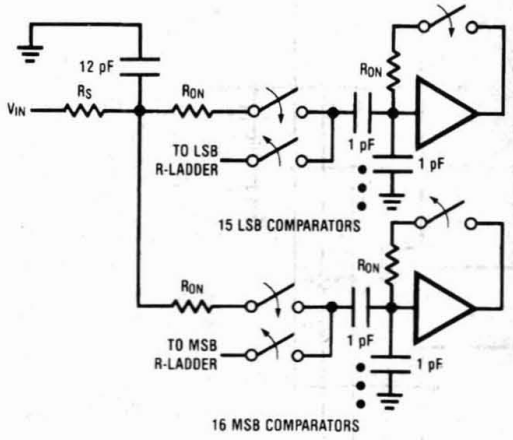
Input Not Referred to GND



*Current path must still exist from $V_{IN}(-)$ to ground

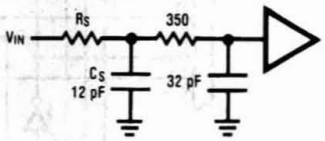
TL/H/5501–23

FIGURE 9. Analog Input Options



TL/H/5501–24

FIGURE 10a



TL/H/5501–25

FIGURE 10b

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

2.4 INHERENT SAMPLE-HOLD

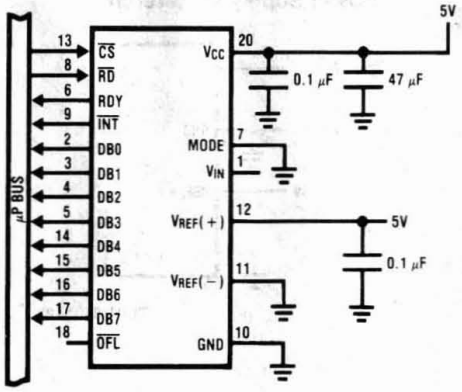
Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 μs, the time through which V_{IN} must be 1/2 LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of $\overline{WR}$ (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 μs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.

3.0 Typical Applications

8-Bit Resolution Configuration



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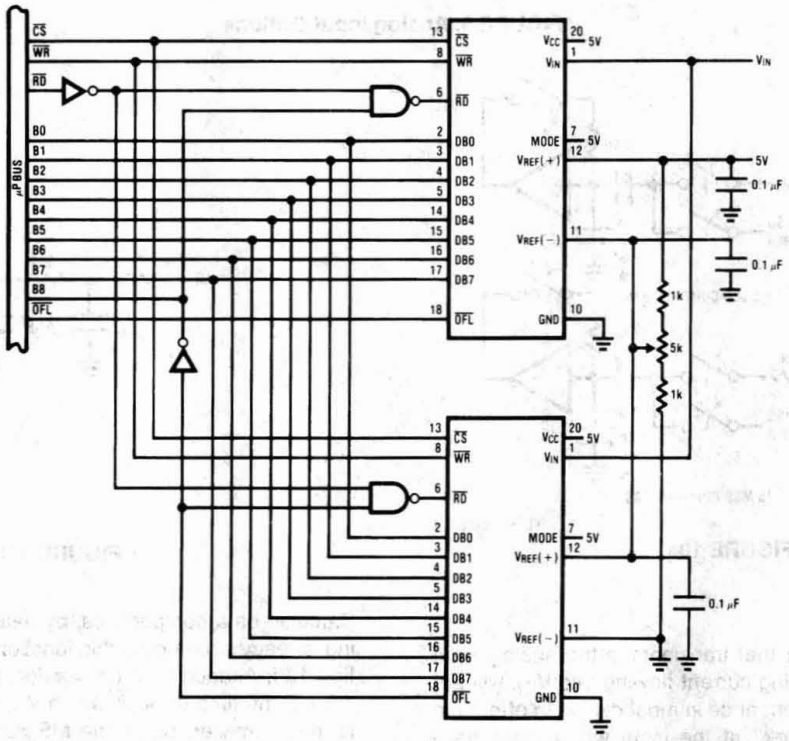
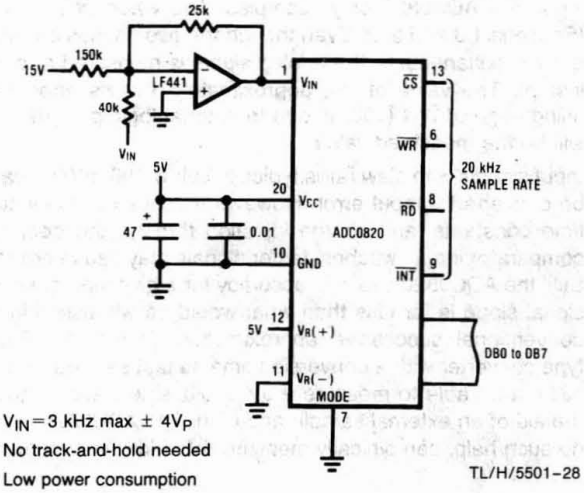
9-Bit Resolution Configuration



TL/H/5501–27

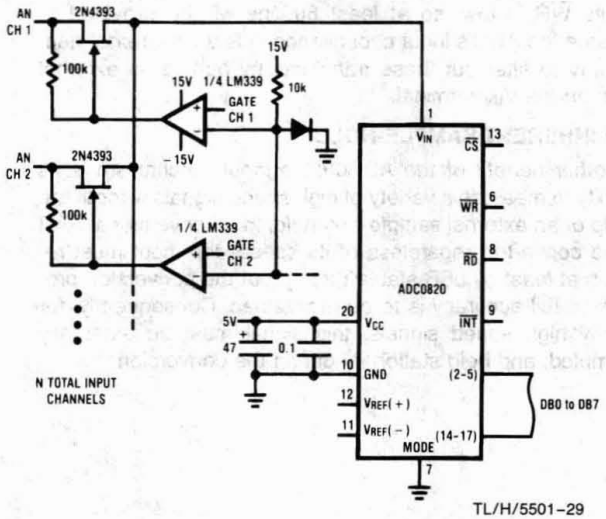
Telecom A/D Converter



- V_{IN} = 3 kHz max ± $4V_P$
- No track-and-hold needed
- Low power consumption

TL/H/5501–28

Multiple Input Channels



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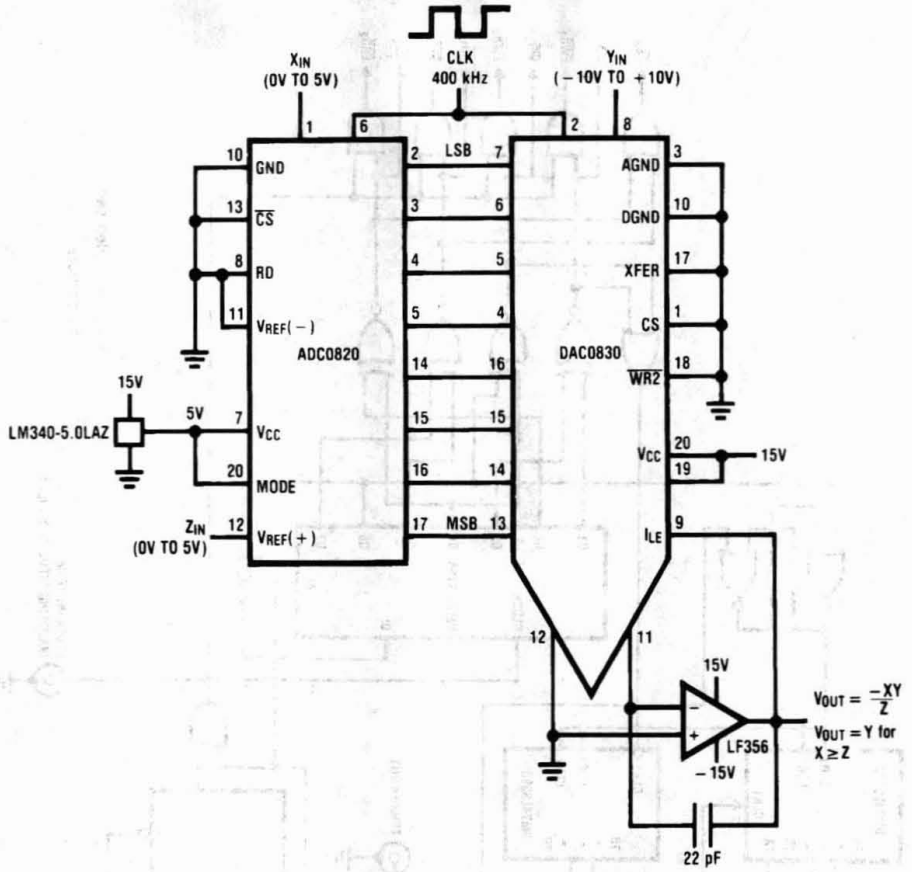
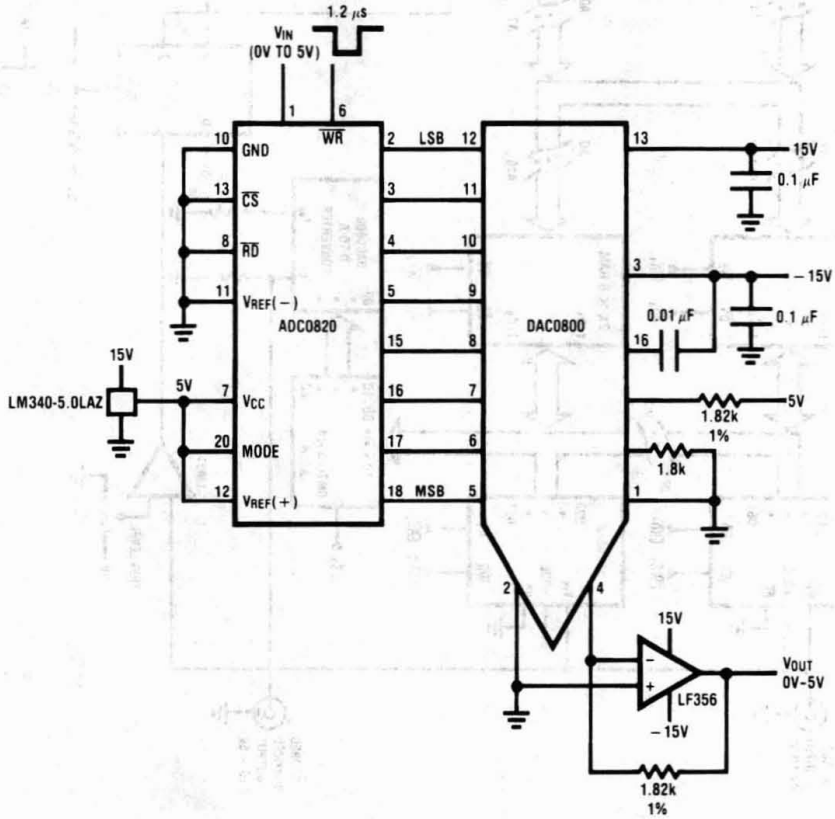
3.0 Typical Applications (Continued)

8-Bit 2-Quadrant Analog Multiplier



TL/H/5501–30

Fast Infinite Sample-and-Hold



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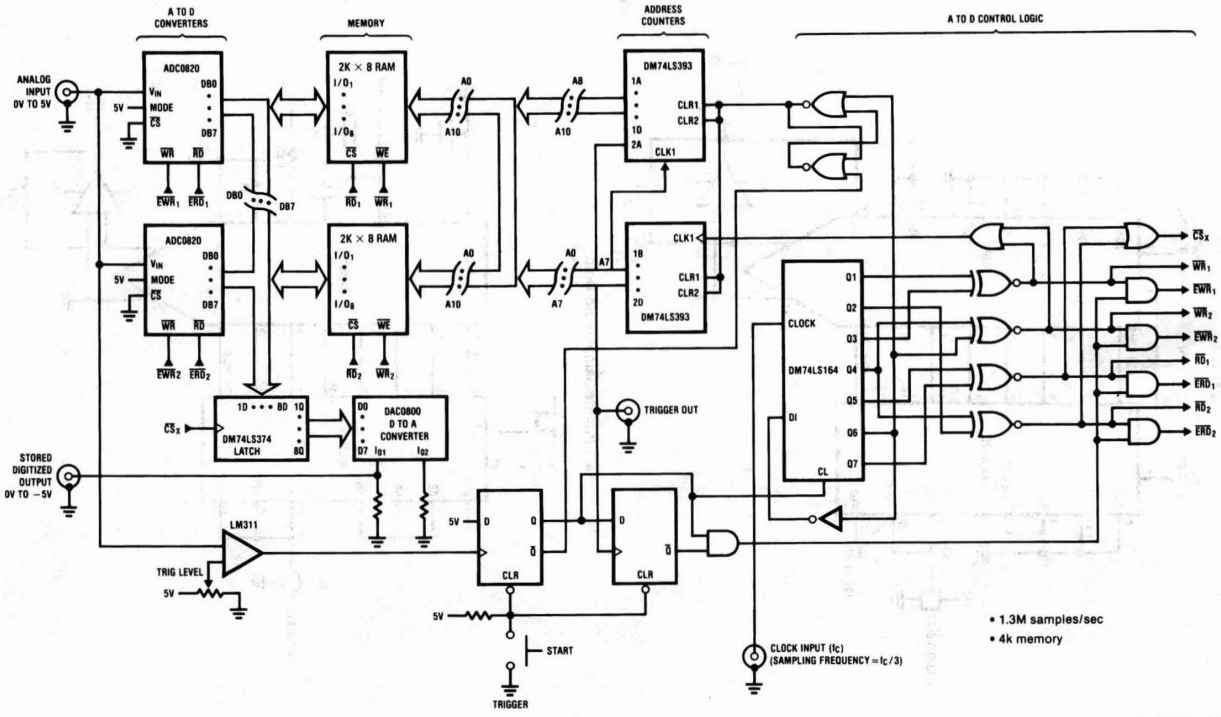
3.0 Typical Applications (Continued)

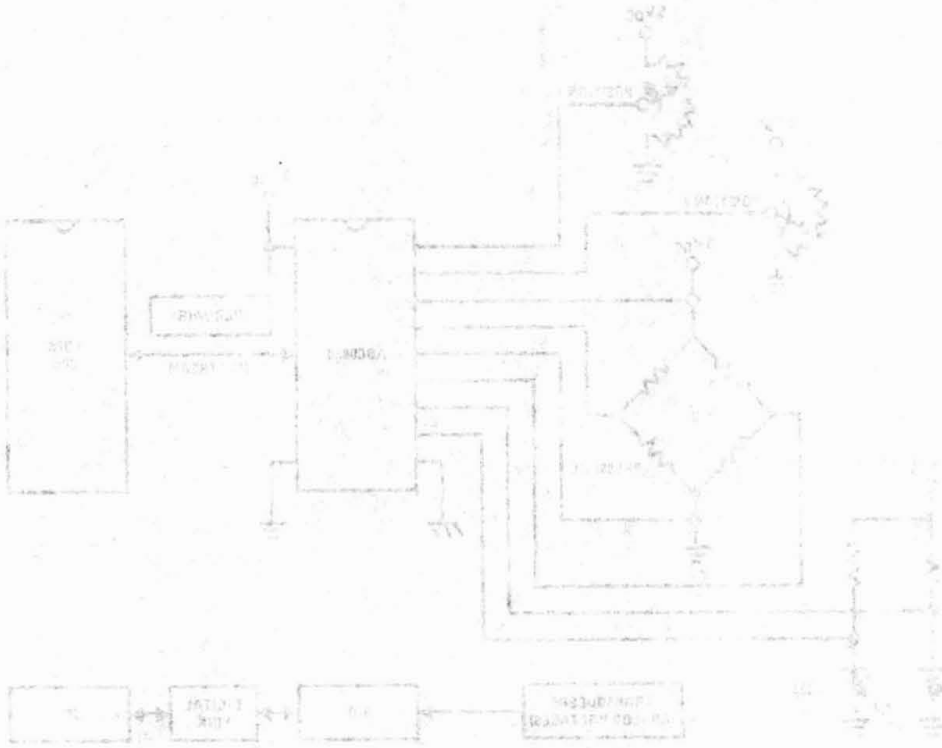
Digital Waveform Recorder



TL/H/5501–32

Ordering Information

Part Number	Total Unadjusted Error	Package	Temperature Range
ADC0820BCV	±½ LSB	V20A—Molded Chip Carrier	0°C to +70°C
ADC0820BCWM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820BCN		N20A—Molded DIP	0°C to +70°C
ADC0820CCJ	±1 LSB	J20A—Cerdip	−40°C to +85°C
ADC0820CCMSA		MSA20— Shrink Small Outline Package	0°C to +70°C
ADC0820CCV		V20A—Molded Chip Carrier	0°C to +70°C
ADC0820CCWM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820CIWM		M20B—Wide Body Small Outline	−40°C to +85°C
ADC0820CCN		N20A—Molded DIP	0°C to +70°C



National Semiconductor

ADC0831/ADC0832/ADC0834 and ADC0838 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

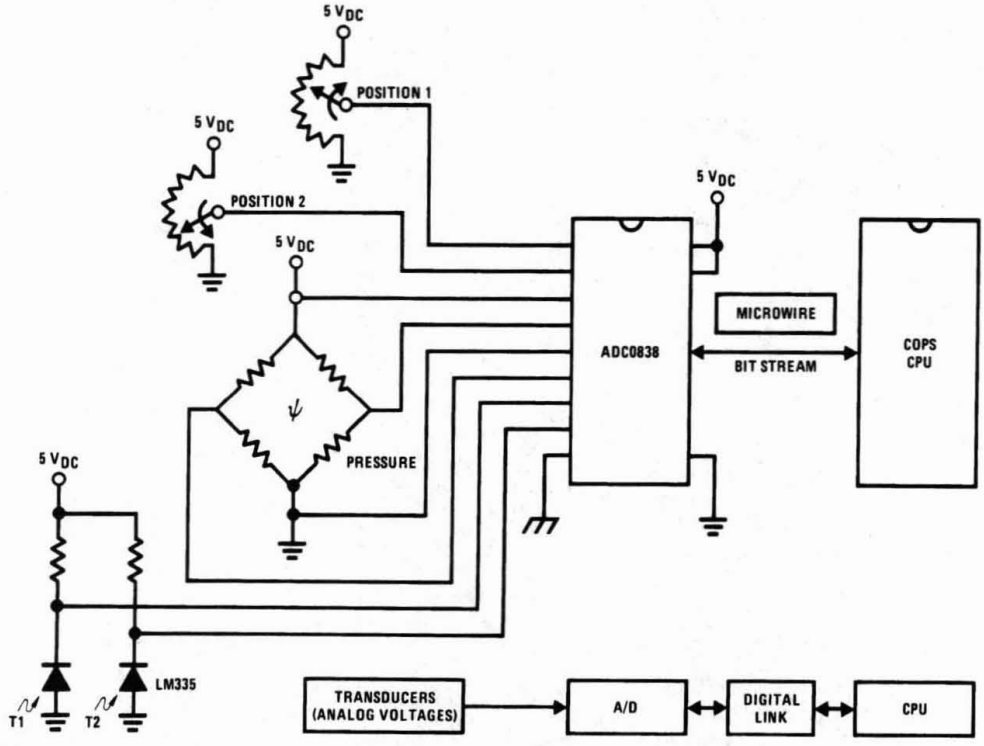
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3" standard width, 8-, 14- or 20-pin DIP package
- 20 Pin Molded Chip Carrier Package (ADC0838 only)
- Surface-Mount Package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 μs

Typical Application



TL/H/5583–1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 5)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0831/8BCJ, ADC0831/4/8CCJ, ADC0832BIWM, ADC0831/2/4/8CIWM ADC0831/2//4/8BCN, ADC0838BCV, ADC0831/2/4/8CCN, ADC0838CCV, ADC0831/2/4/8CCWM	−40°C to +85°C
	0°C to +70°C

Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V+ = V_{REF} = 5V, $V_{REF} \le V_{CC}$ +0.1V, $T_A = T_j$ = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BCJ, BIWM, CIWM and CCJ Devices			BCV, CCV, CCWM, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	V_{REF} = 5.00 V (Note 6)							
ADC0838BCV						±½	±½	
ADC0831/2/4/8BCN						±½	±½	LSB
ADC0831/8BCJ			±½					
ADC0832BIWM			±½					
ADC0838CCV						±1	±1	
ADC0831/2/4/8CCN						±1	±1	
ADC0831/2/4/8CCWM						±1	±1	
ADC0831/4/8CCJ			±1					
ADC0831/2/4/8CIWM			±1					
Minimum Reference Input Resistance (Note 7)		3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Reference Input Resistance (Note 7)		3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Maximum Common-Mode Input Range (Note 8)			**V_{CC} +0.05**			V_{CC} +0.05	**V_{CC} +0.05**	V
Minimum Common-Mode Input Range (Note 8)			**GND −0.05**			GND −0.05	**GND −0.05**	V
DC Common-Mode Error		±1/16	±¼		±1/16	±¼	±¼	LSB

Converter and Multiplexer Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = V+ = 5V, T_A = T_j = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BCJ, BIWM, CIWM and CCJ Devices			BCV, CCV, CCWM, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)								
Change in zero error from V_{CC} = 5V to internal zener operation (Note 3)	15 mA into V+ V_{CC} = N.C. V_{REF} = 5V		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V_+) (Note 3) MIN	15 mA into V+		**6.3**			6.3	**6.3**	V
MAX			**8.5**			8.5	**8.5**	V
Power Supply Sensitivity	V_{CC} = 5V ± 5%	±1/16	**±¼**	±¼	±1/16	±¼	**±¼**	LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**			−0.2	**−1**	µA
	On Channel = 0V, Off Channel = 5V		+0.2 **+1**			+0.2	**+1**	µA
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 0V, Off Channel = 5V		−0.2 **−1**			−0.2	**−1**	µA
	On Channel = 5V, Off Channel = 0V		+0.2 **+1**			+0.2	**+1**	µA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN} = 5.0V	0.005	**1**		0.005	1	**1**	µA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	**−1**		−0.005	−1	**−1**	µA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 µA I_{OUT} = −10 µA		**2.4** **4.5**			2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.1 0.1	**−3** **3**		−0.1 0.1	−3 +3	**−3** **+3**	µA µA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		0.9	**2.5**		0.9	2.5	**2.5**	mA
ADC0832	Includes Ladder Current	2.3	**6.5**		2.3	6.5	**6.5**	mA

AC Characteristics

The following specifications apply for V_{CC} = 5V, $t_r = t_f$ = 20 ns and 25°C unless otherwise specified.

Parameter		Conditions	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Limit Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 10)	Min				40	%
	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 11)		C_L = 100 pF				
		Data MSB First	650		1500	ns
		Data LSB First	250		600	ns
t_{1H}, t_{0H},—Rising Edge of CS to Data Output and SARS Hi-Z		C_L = 10 pF, R_L = 10k (see TRI-STATE® Test Circuits)	125		250	ns
		C_L = 100 pf, R_L = 2k		500		ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground plugs.

Note 3: Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See *Figure 3* in Functional Description Section 6.0)

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 7: Cannot be tested for ADC0832.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 μs. The maximum time the clock can be high is 60 μs. The clock can be stopped when low so long as the analog input voltage remains stable.

Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

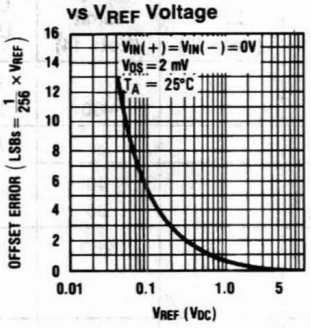
Note 12: Typicals are at 25°C and represent most likely parametric norm.

Note 13: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

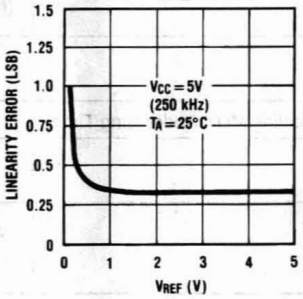
Note 14: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

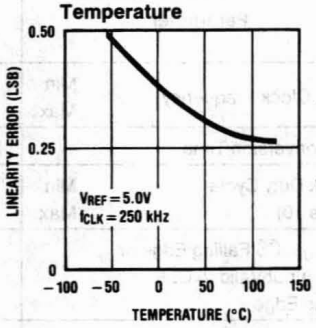
Unadjusted Offset Error vs V_{REF} Voltage



Linearity Error vs V_{REF} Voltage



Linearity Error vs Temperature



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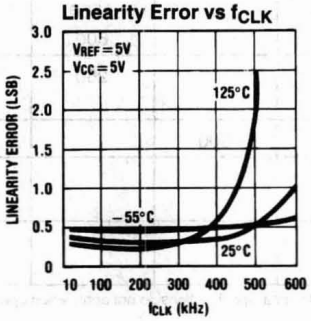
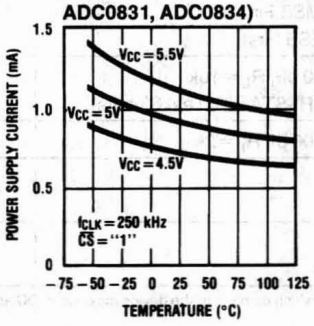
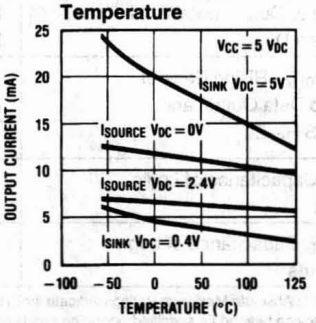
Linearity Error vs f_{CLK}



Power Supply Current vs Temperature (ADC0838, ADC0831, ADC0834)



Output Current vs Temperature



Note: For ADC0832 add I_{REF}.

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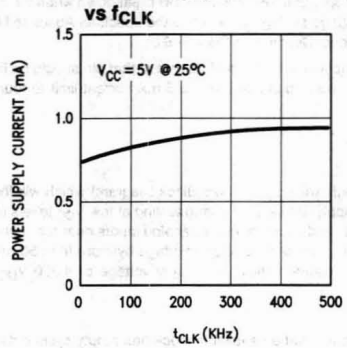
Power Supply Current vs f_{CLK}



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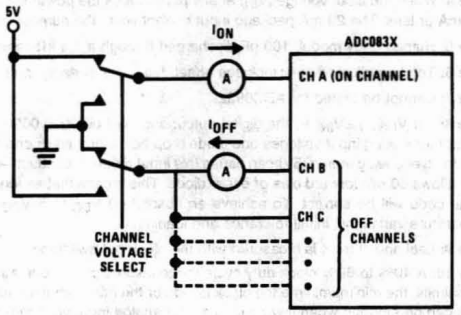
Leakage Current Test Circuit



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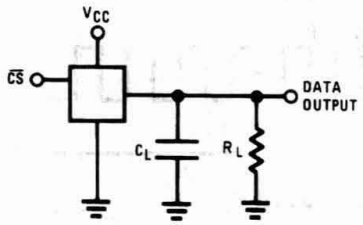
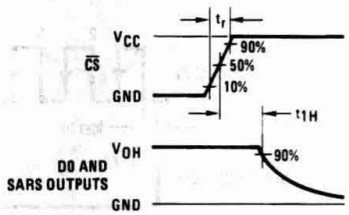
TRI-STATE Test Circuits and Waveforms

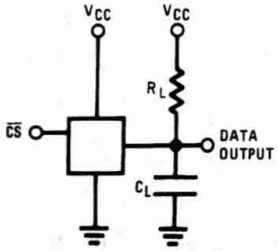
t_{1H}



t_{1H}



t_{OH}



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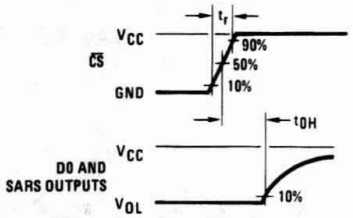
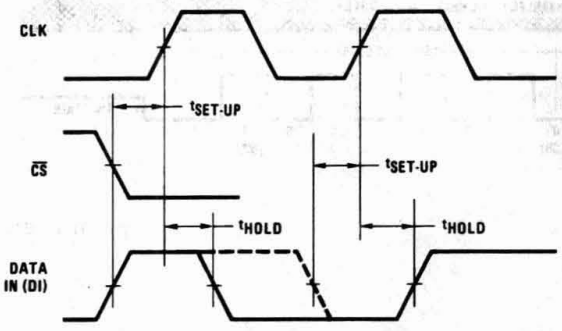
t_{OH}



TL/H/5583–23

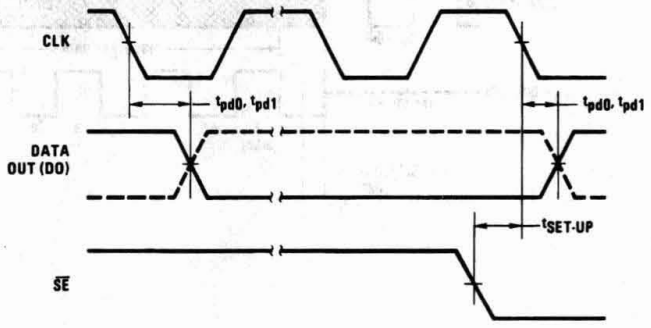
Timing Diagrams

Data Input Timing



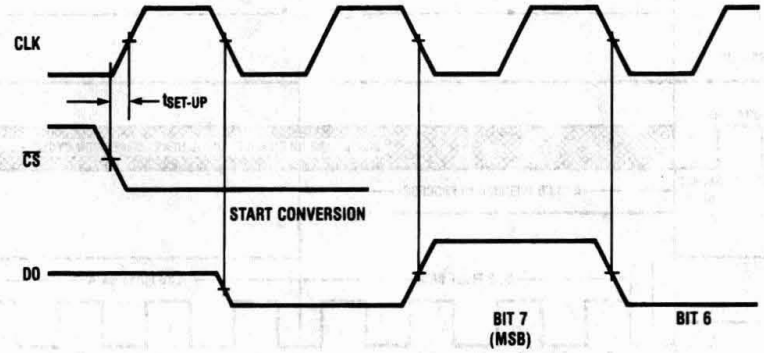
TL/H/5583–24

Data Output Timing



TL/H/5583–25

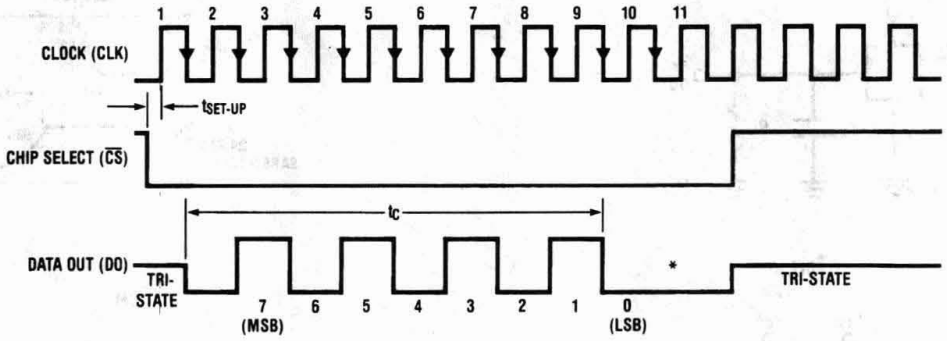
ADC0831 Start Conversion Timing



TL/H/5583–26

Timing Diagrams (Continued)

ADC0831 Timing



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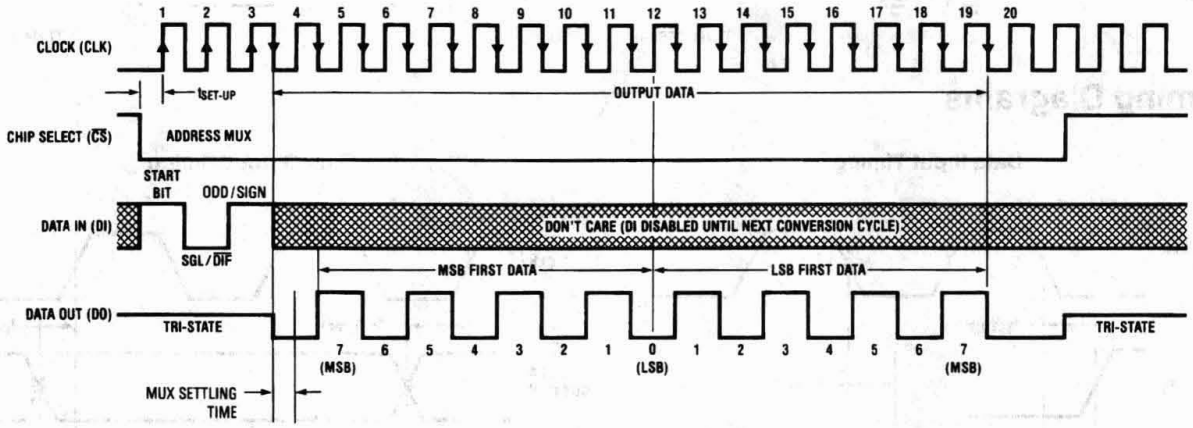
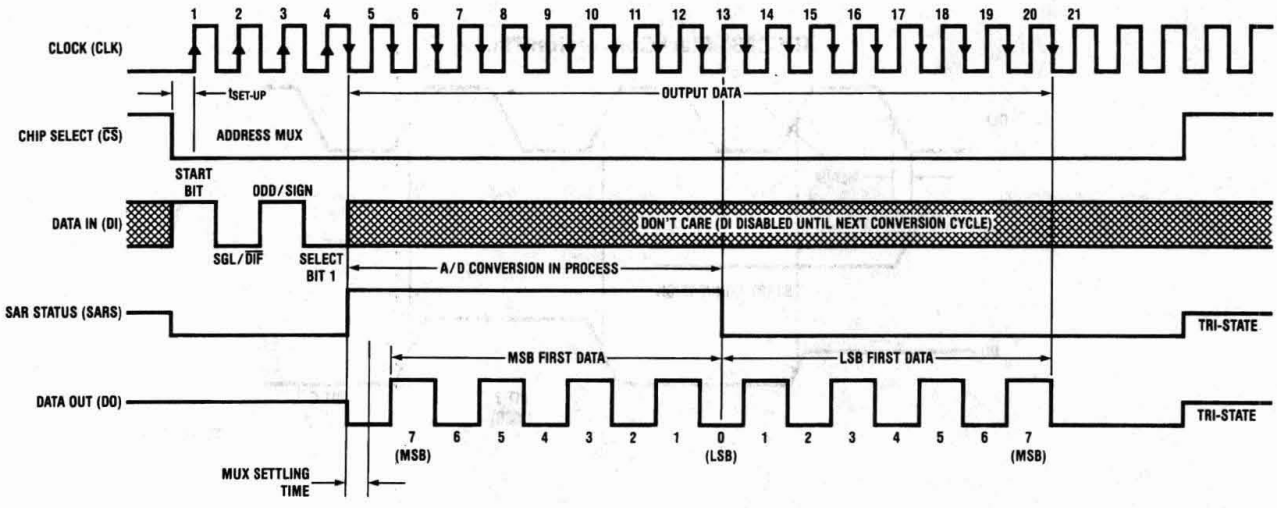
*LSB first output not available on ADC0831.

ADC0832 Timing



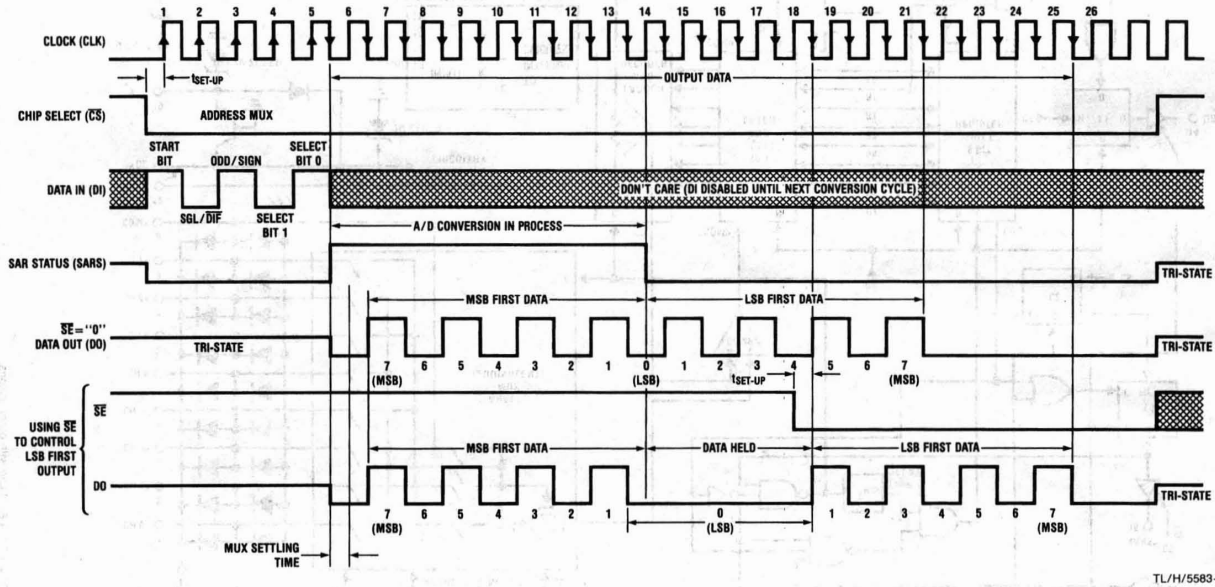
TL/H/5583–28

ADC0834 Timing



TL/H/5583–5

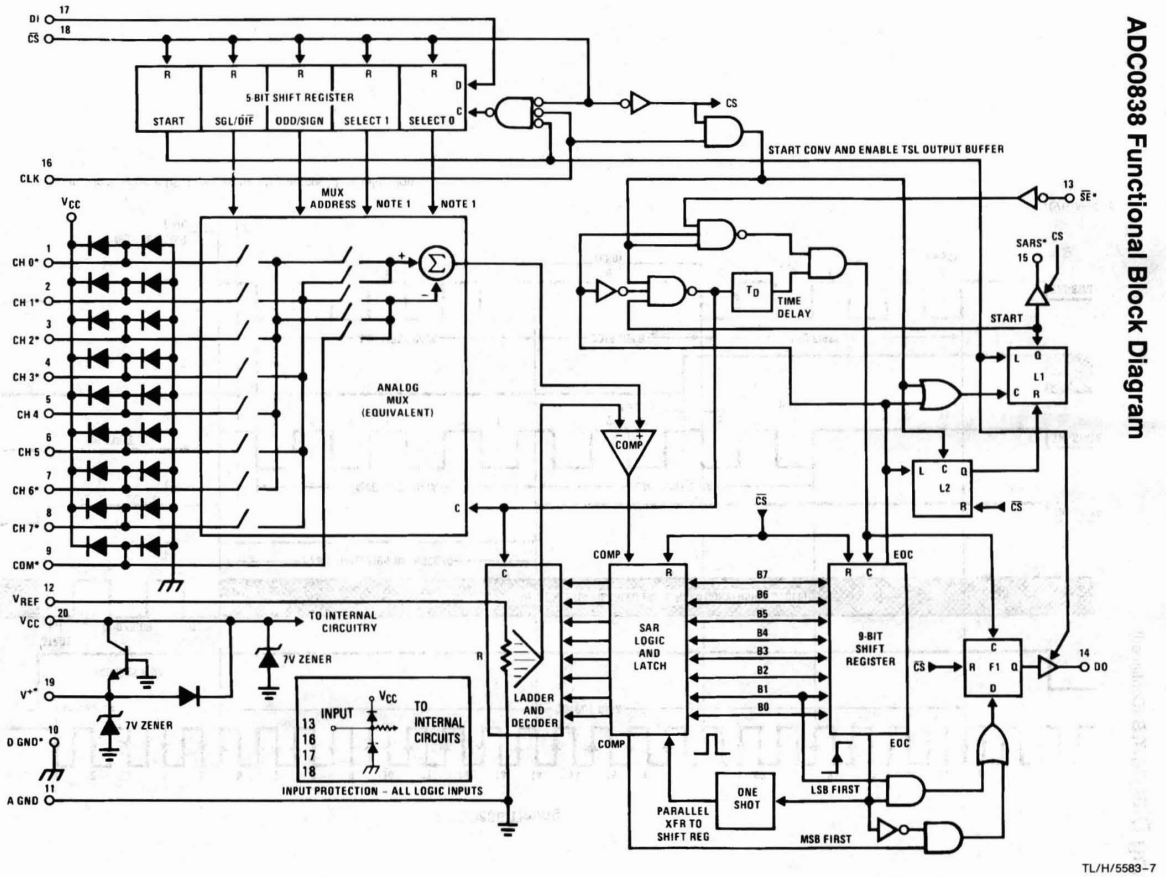
ADC0838 Timing



TL/H/5583–6

* Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC0838 Functional Block Diagram



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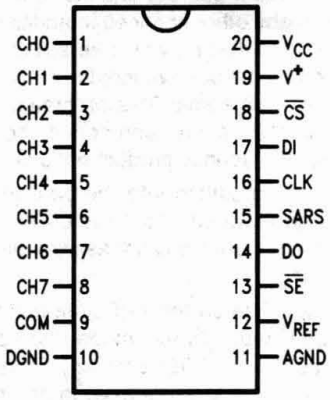
*Some of these functions/pins are not available with other options.

Note 1: For the ADC0834, DI is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832, DI is input directly to the DI input of ODD/SIGN. SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

Connection Diagrams

ADC0838 8-Channel MUX

Small Outline/Dual-In-Line Package (J, M and N)

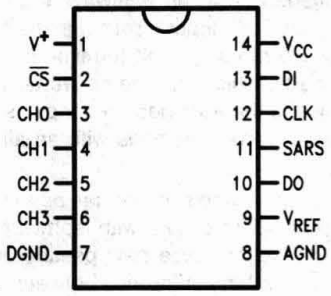


TL/H/5583–8

Top View

ADC0834 4-Channel MUX

Small Outline/Dual-In-Line Package (J, M, and N)



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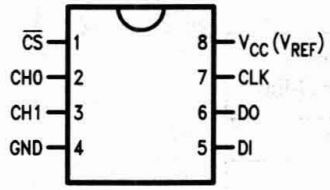
Top View

COM internally connected to A GND

ADC0832 2-Channel MUX

Dual-In-Line Package (J and N)



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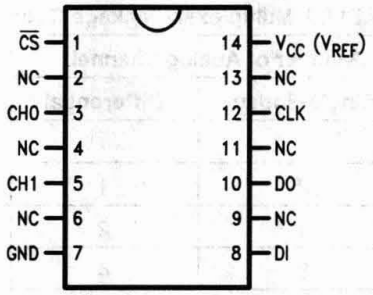
Top View

COM internally connected to GND.

V_{REF} internally connected to V_{CC}.

ADC0832 2-Channel MUX

Small Outline Package (M)

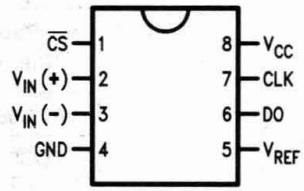


TL/H/5583–41

Top View

ADC0831 Single Differential Input

Dual-In-Line Package (J and N)



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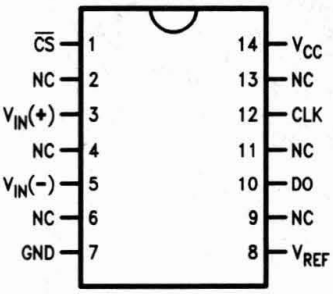
Top View

ADC0831 Single Differential Input

Small Outline Package (M)



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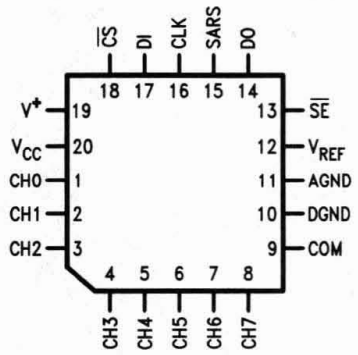
Top View

ADC0838 8-Channel MUX

Molded Chip Carrier (PCC) Package (V)



TL/H/5583–33

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC0831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ADC0838 can be used as a pseudo-differential input. In this mode, the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC0831	1	1	8
ADC0832	2	1	8
ADC0834	4	2	14
ADC0838	8	4	20

Functional Description (Continued)

TABLE II. MUX Addressing: ADC0838

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT		0		1		2		3	
		1	0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

TABLE III. MUX Addressing: ADC0834

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE IV. MUX Addressing: ADC0832

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel #	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.

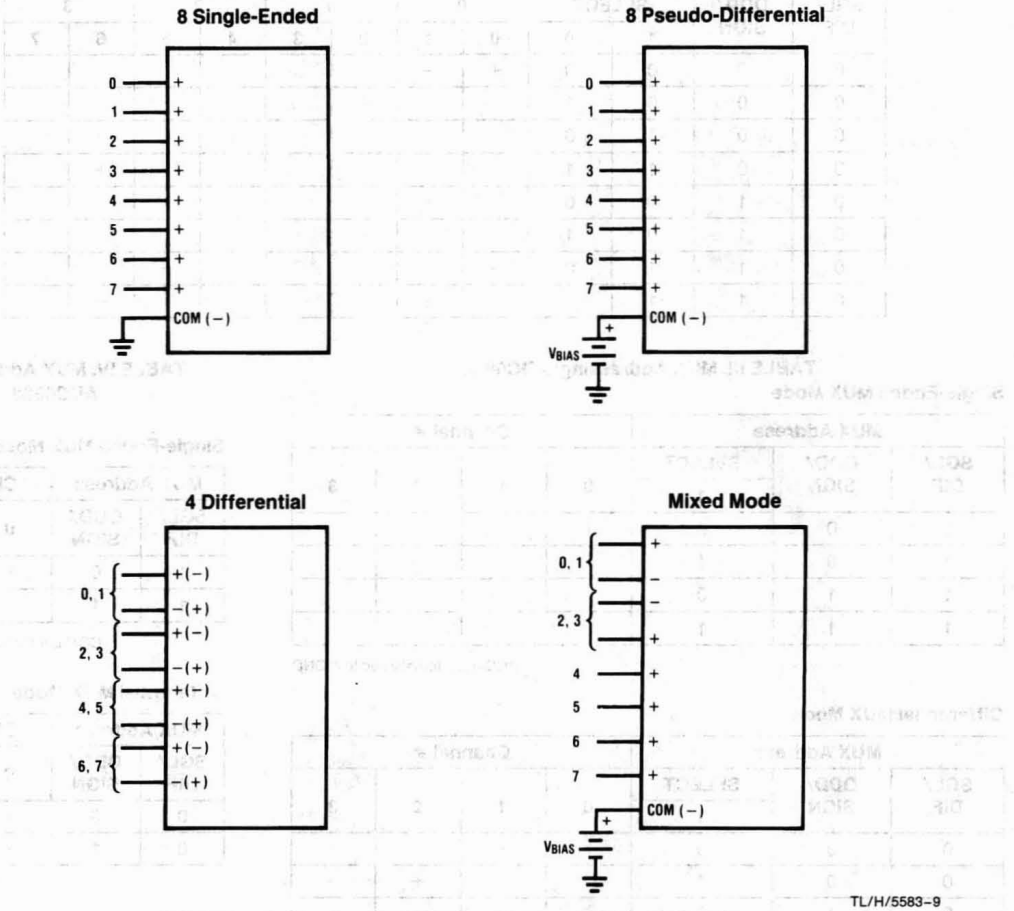


FIGURE 1. Analog Input Multiplexer Options for the ADC0838

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. All 8 bits of the result are stored in an output shift register. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. On the ADC0838 the $\overline{SE}$ line is brought out and if held high, the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low, the data is then clocked out LSB first. The ADC0831 is an exception in that its data is only output in MSB first format.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

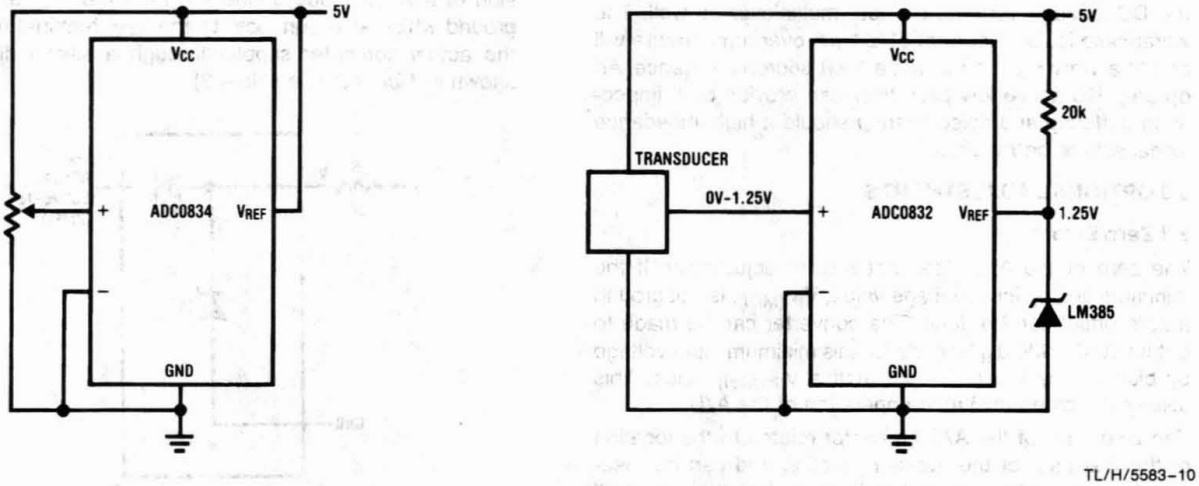
3.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 3.5 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC0832). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/256).



a) Ratiometric

b) Absolute with a Reduced Span

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}} \right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK}, is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input (or V_{CC} for the ADC0832) for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right]$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0838 and ADC0834 is the inclusion of a zener diode connected from the V^+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3*. (See Note 3)

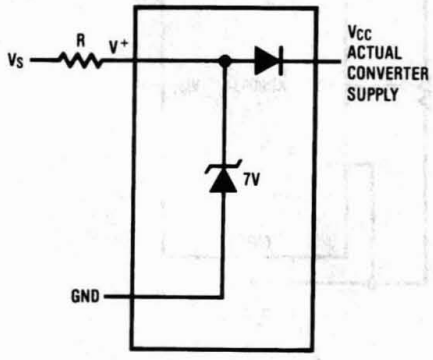


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FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4 and 5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V^+ and V_{CC} is shown in *Figures 6 and 7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D and the relatively high clock frequencies used (typically in the range of 10k–400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under 1/4 of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V^+ pin.

Applications

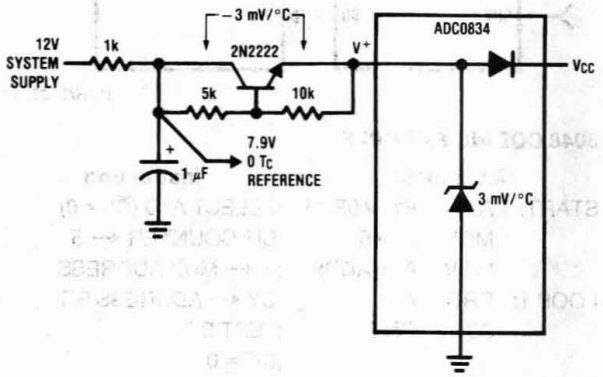

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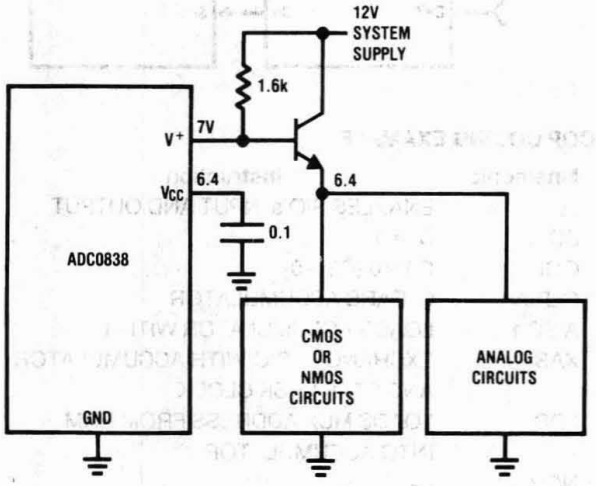
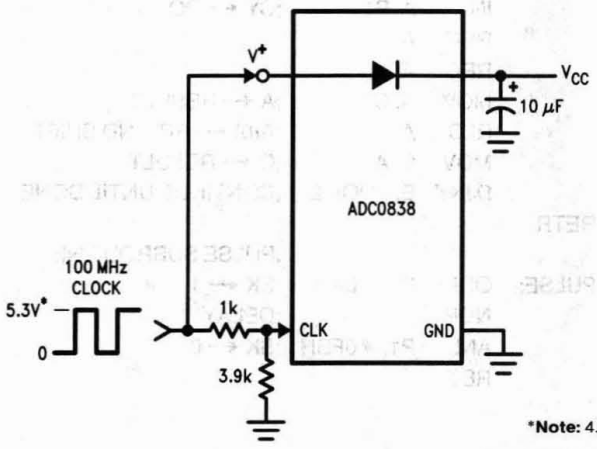
FIGURE 4. Operating with a Temperature Compensated Reference



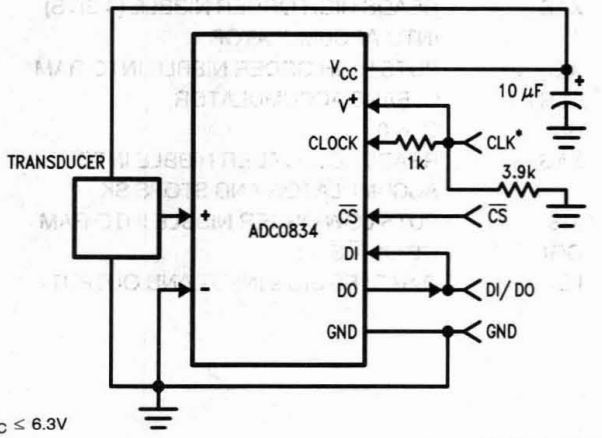
TL/H/5583–34

FIGURE 5. Using the A/D as the System Supply Regulator



TL/H/5583–35

FIGURE 6. Generating V_{CC} from the Converter Clock



***Note:** 4.5V ≤ V_{CC} ≤ 6.3V

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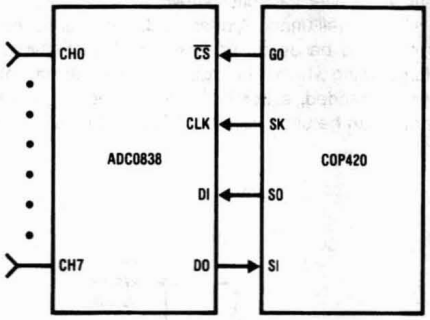
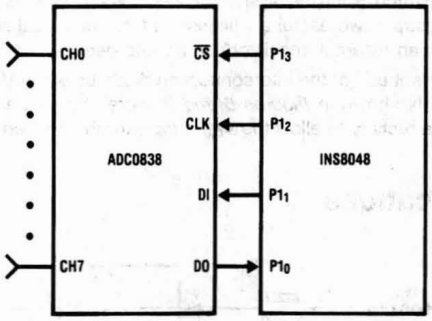
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048





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COP CODING EXAMPLE

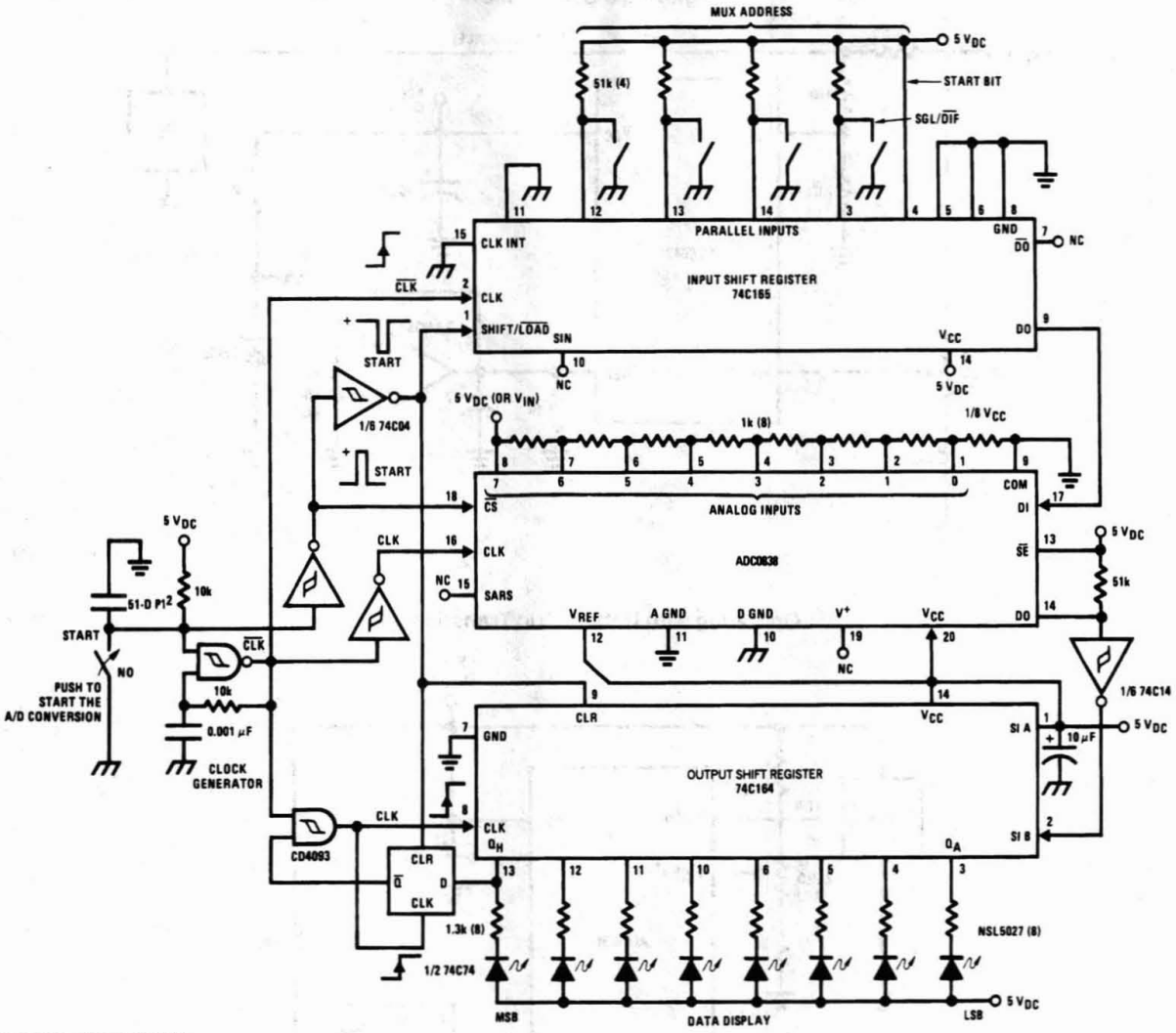
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑	
8 INSTRUCTIONS	
↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

	Mnemonic		Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

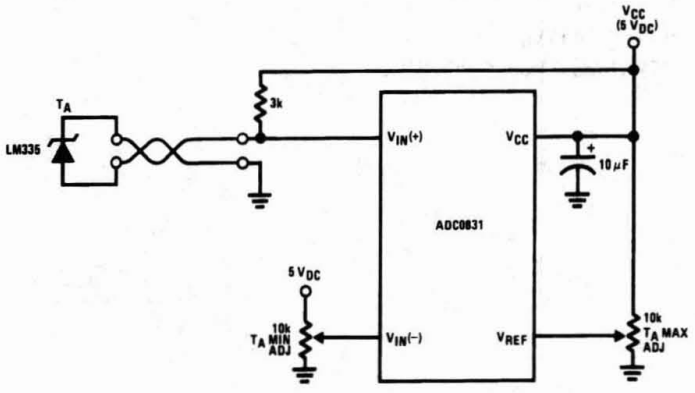
Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0838 Evaluation



*Pinouts shown for ADC0838.
For all other products tie to pin functions as shown.

Low-Cost Remote Temperature Sensor



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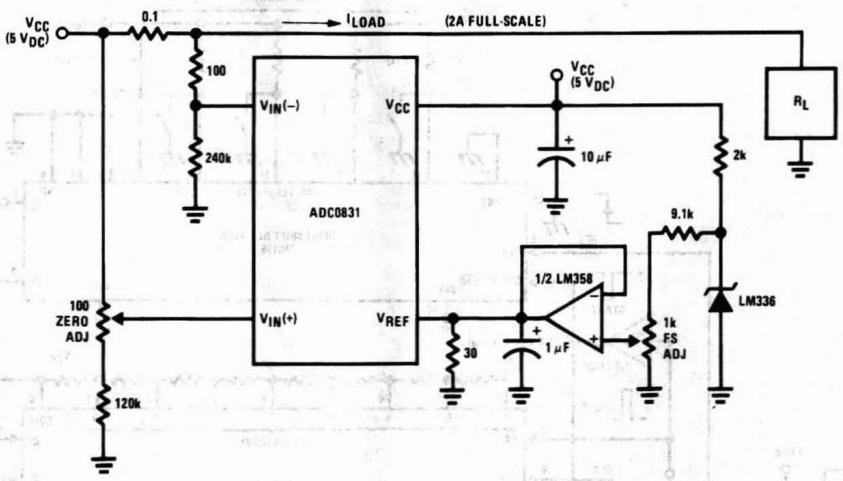
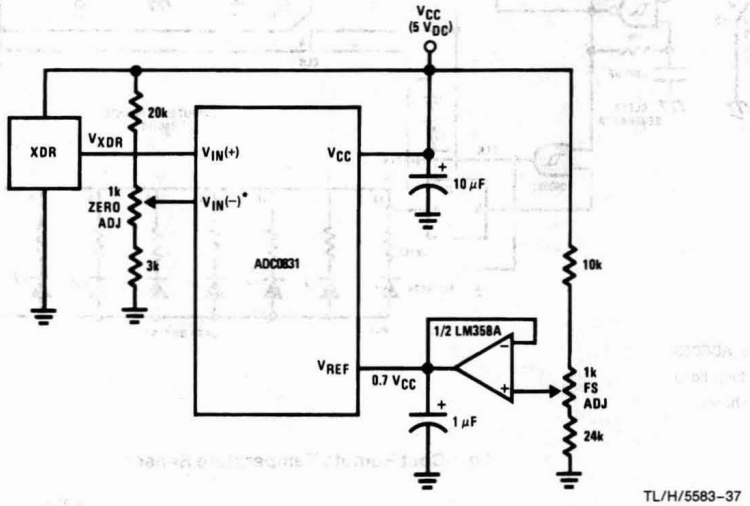
Applications (Continued)

Digitizing a Current Flow



TL/H/5583–15

Operating with Ratiometric Transducers



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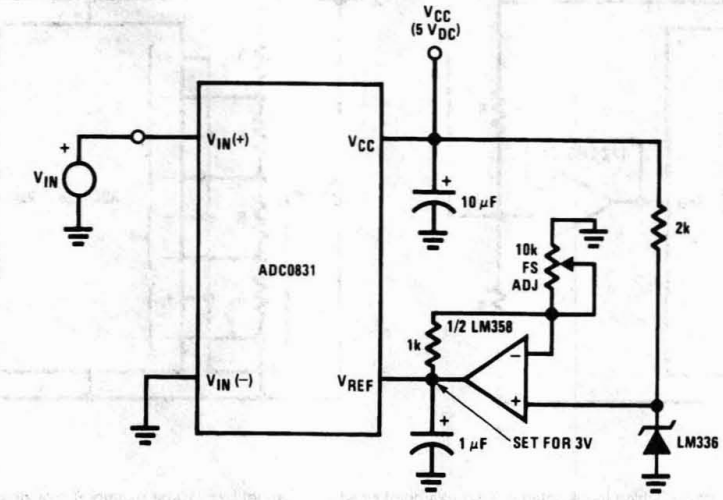
*$V_{IN}(-) = 0.15\ V_{CC}$

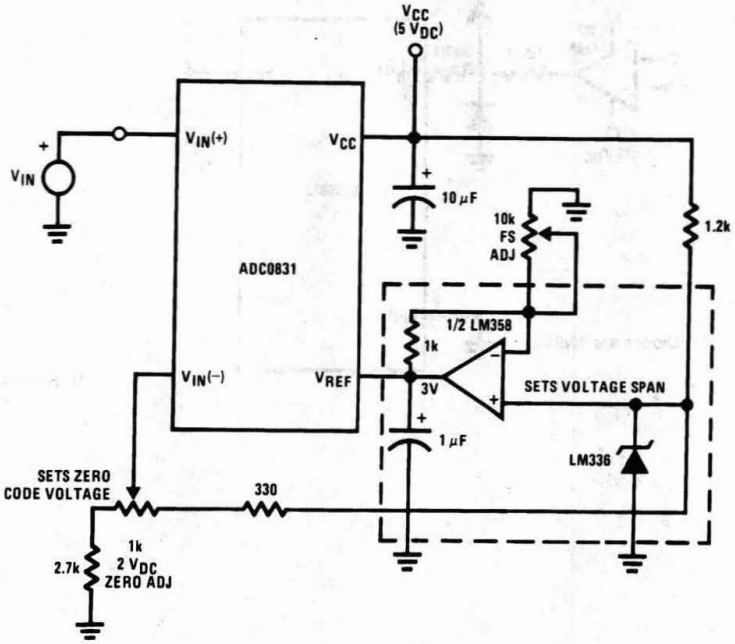
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



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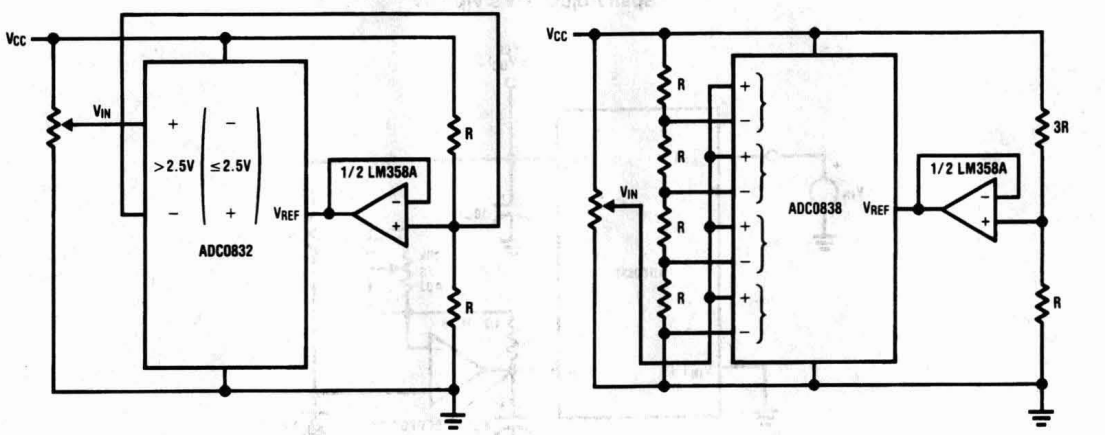
Applications (Continued)

Obtaining Higher Resolution



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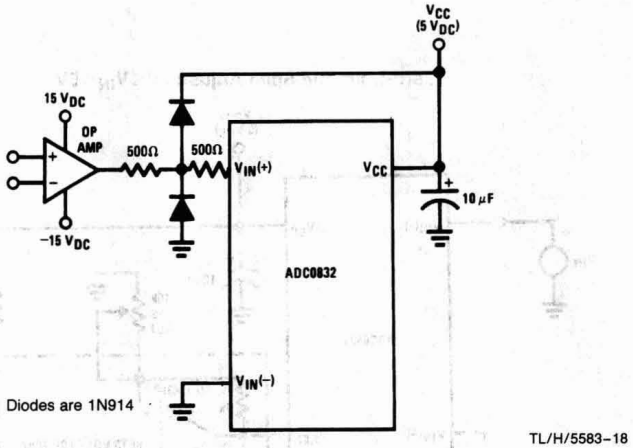
Controller performs a routine to determine which input polarity (9-bit example) or which channel pair (10-bit example) provides a non-zero output code. This information provides the extra bits.

a) 9-Bit A/D **b)10-Bit A/D**

Protecting the Input



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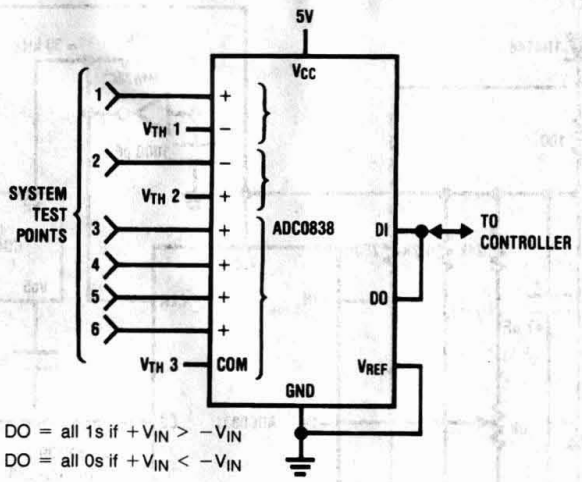
Applications (Continued)

High Accuracy Comparators



DO = all 1s if $+V_{IN} > -V_{IN}$
DO = all 0s if $+V_{IN} < -V_{IN}$

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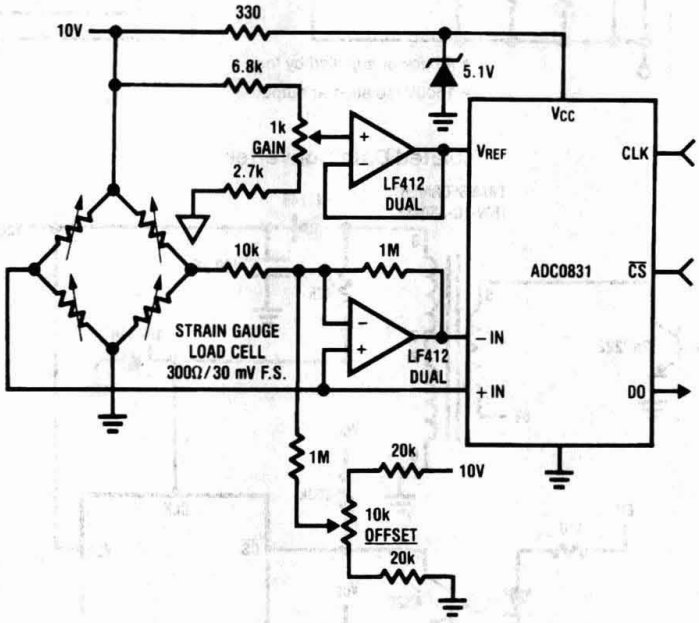
Digital Load Cell



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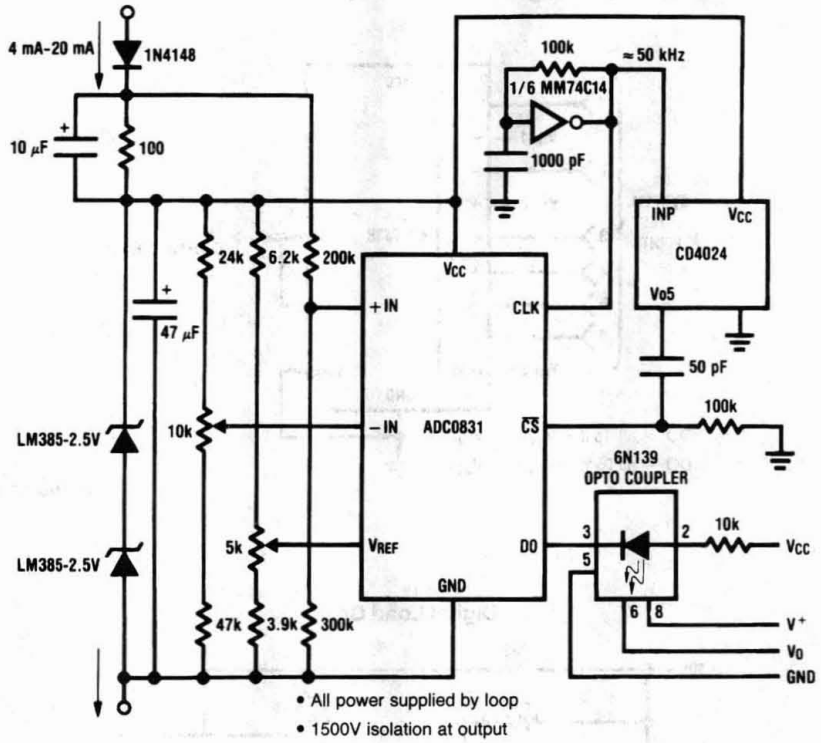
- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

Applications (Continued)

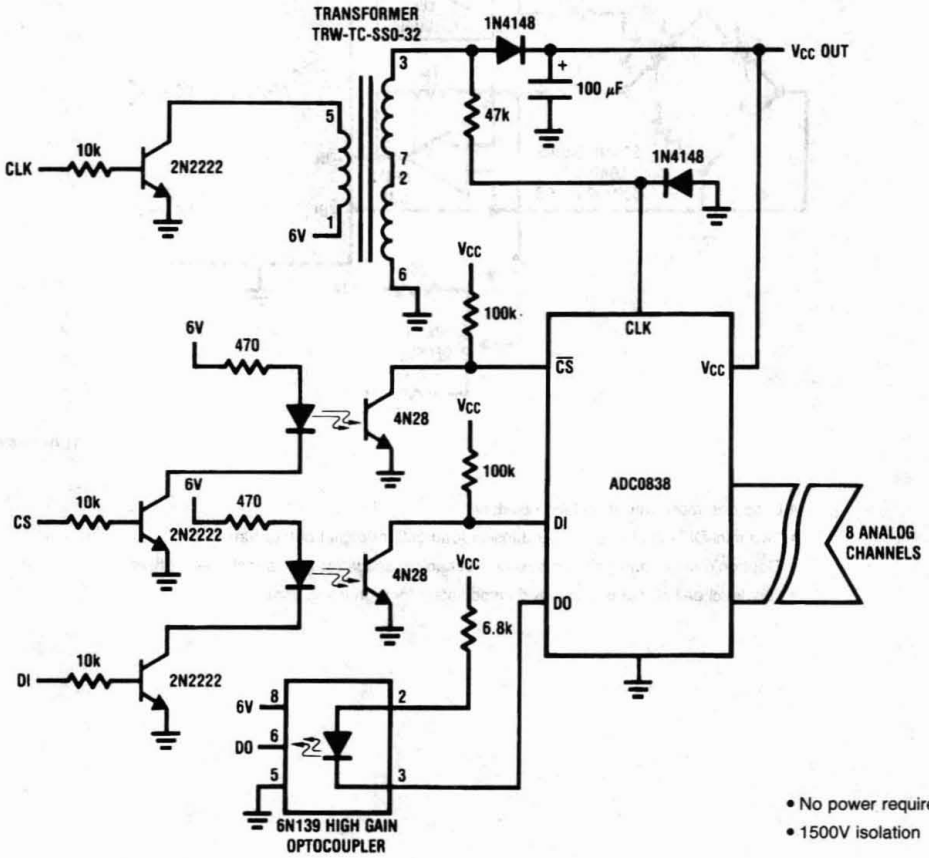
4 mA–20 mA Current Loop Converter



- All power supplied by loop
- 1500V isolation at output

TL/H/5583–20

Isolated Data Converter



- No power required remotely
- 1500V isolation

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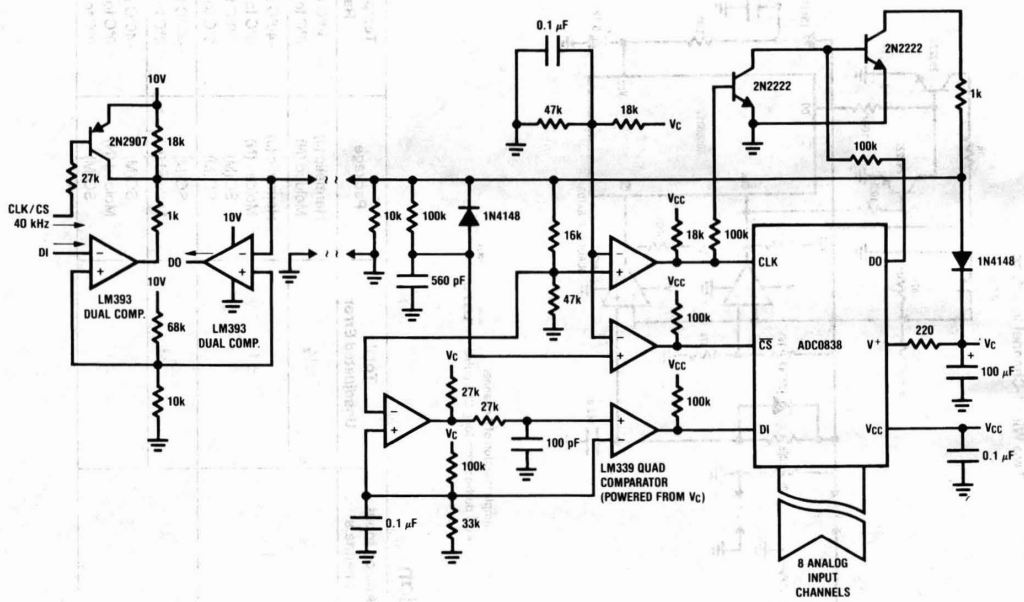
Two Wire Interface for 8 Channels



- No additional connections
- $\overline{CS}$ derived from extended high on CLK line > 100 μs
- Timing arranged for 40 kHz, could be changed up or down by component change
- 10% CLK frequency change without component change OK

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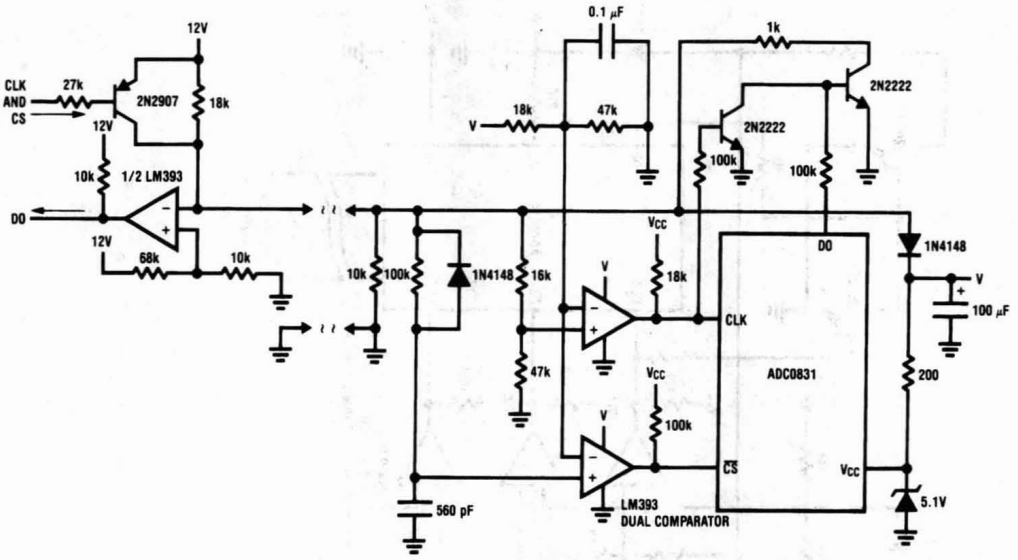
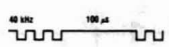
Applications (Continued)

Two Wire 1-Channel Interface



- Simpler version of 8-channel
- $\overline{CS}$ derived from long CLK pulse



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Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831BCJ	1	±½	Hermetic (J)	−40°C to +85°C
ADC0831BCN			Molded (N)	0°C to +70°C
ADC0831CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0831CCN			Molded (N)	0°C to +70°C
ADC0831CIWM			SO(M)	−40°C to +85°C
ADC0831CCWM			SO(M)	0°C to +70°C
ADC0832BIWM	2	±½	SO(M)	−40°C to +85°C
ADC0832BCN			Molded (N)	0°C to +70°C
ADC0832CIWM		±1	SO(M)	−40°C to +85°C
ADC0832CCN			Molded (N)	0°C to +70°C
ADC0832CCWM			SO(M)	0°C to +70°C

Ordering Information (Continued)

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0834BCN	4	±½	Molded (N)	0°C to +70°C
ADC0834CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0834CCN			Molded (N)	0°C to +70°C
ADC0834CCWM			SO(M)	0°C to +70°C
ADC0834CIWM			SO(M)	−40°C to +85°C
ADC0838BCJ	8	±½	Hermetic (J)	−40°C to +85°C
ADC0838BCV			PCC (V)	0°C to +70°C
ADC0838BCN			Molded (N)	0°C to +70°C
ADC0838CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0838CCV			PCC (V)	0°C to +70°C
ADC0838CCN			Molded (N)	0°C to +70°C
ADC0838CIWM			SO(M)	−40°C to +85°C
ADC0838CCWM			SO(M)	0°C to +70°C

See NS Package Number J08A, J14A, J20A, M14B, M20B, N08E, N14A, N20A or V20A

National Semiconductor

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

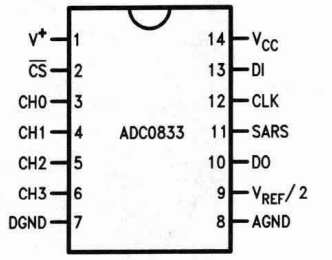
- NSC MICROWIRE compatible–direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3" standard width 14-pin DIP package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	23 mW
■ Conversion Time	32 μs

Connection and Functional Diagrams

Dual-In-Line Package (J and N)



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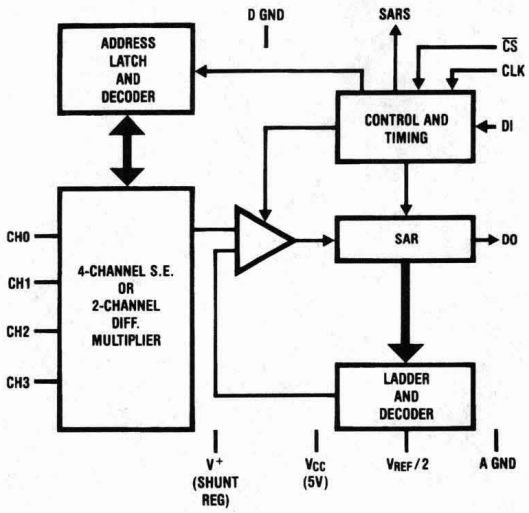
Top View

Order Number ADC0833CCJ, ADC0833BCN or ADC0833CCN
See NS Package Number J14A or N14A



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
ESD Susceptibility (Note 5)	2000V

Operating Conditions (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0833CCJ	$-40°C \le T_A \le 85°C$
ADC0833BCN, ADC0833CCN	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \le (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error	$V_{REF}/2$ Forced to 2.500 V_{DC}				
ADC0833BCN			±½	**±½**	LSB
ADC0833CCN			±1	**±1**	LSB
ADC0833CCJ			**±1**		LSB
Minimum Total Ladder Resistance (Note 9)					
ADC0833CCJ		7.0	**2.6**		kΩ
ADC0833BCN/CCN		7.0	2.6	**2.6**	kΩ
Maximum Total Ladder Resistance (Note 9)					
ADC0833CCJ		7.0	**11.8**		kΩ
ADC0833BCN/CCN		7.0	10.8	**11.8**	kΩ
Minimum Common-Mode Input Range (Note 10)	All MUX Inputs and COM Input				
ADC0833CCJ			**GND−0.05**		V
ADC0833BCN/CCN			GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input Range (Note 10)	All MUX Inputs and COM Input				
ADC0833CCJ			**V_{CC}+0.05**		V
ADC0833BCN/CCN			V_{CC}+0.05	**V_{CC}+0.05**	V
DC Common-Mode Error					
ADC0833CCJ		±1/16	±¼		LSB
ADC0833BCN/CCN		±1/16	±¼	±¼	LSB
Change In Zero Error From V_{CC} = 5V To Internal Zener Operation (Note 3)	15mA Into V+ V_{CC} = N.C. $V_{REF}/2$ = 2.500V				
ADC0833CCJ			**1**		LSB
ADC0833BCN/CCN			1	**1**	LSB

Electrical Characteristics The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \leq (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
V_Z, Minimum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833CCJ			**6.3**		V
ADC0833BCN/CCN			6.3	**6.3**	V
V_Z, Maximum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833CCJ			**8.5**		V
ADC0833BCN/CCN			8.5	**8.5**	V
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$				
ADC0833CCJ		$\pm 1/16$	$\pm$ **¼**		LSB
ADC0833BCN/CCN		$\pm 1/16$	$\pm 1/4$	$\pm$ **¼**	LSB
I_{OFF}, Off Channel Leakage Current (Note 11)	On Channel = 5V, Off Channel = 0V				
ADC0833CCJ			**−1**		μA
			−200		nA
ADC0833BCN/CCN				**−1**	μA
			−200		nA
	On Channel = 0V, Off Channel = 5V				
ADC0833CCJ			**1**		μA
			200		nA
ADC0833BCN/CCN				**1**	μA
			200		nA
I_{ON}, On Channel Leakage Current (Note 11)	On Channel = 5V, Off Channel = 0V				
ADC083CCJ			**1**		μA
			200		nA
ADC0833BCN/CCN				**1**	μA
			200		nA
	On Channel = 0V, Off Channel = 5V				
ADC083CCJ			**−1**		μA
			−200		nA
ADC0833BCN/CCN				**−1**	μA
			−200		nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$				
ADC0833CCJ			**2.0**		V
ADC0833BCN/CCN			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$				
ADC0833CCJ			**0.8**		V
ADC0833BCN/CCN			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$				
ADC0833CCJ		0.005	**1**		μA
ADC0833BCN/CCN		0.005	1	**1**	μA

Electrical Characteristics The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \leq (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$				
ADC0833CCJ		−0.005	**−1**		μA
ADC0833BCN/CCN		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$				
ADC0833CCJ	$I_{OUT} = -360\mu A$		**2.4**		V
ADC0833BCN/CCN			2.4	**2.4**	V
ADC0833CCJ	$I_{OUT} = -10\mu A$		**4.5**		V
ADC0833BCN/CCN			4.5	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6mA$, $V_{CC} = 4.75V$				
ADC0833CCJ			**0.4**		V
ADC0833BCN/CCN			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (DO, SARS)					
ADC0833CCJ	$V_{OUT} = 0.4V$	−0.1	**−3**		μA
ADC0833BCN/CCN		−0.1	−3	**−3**	μA
ADC0833CCJ	$V_{OUT} = 5V$	0.1	**3**		μA
ADC0833BCN/CCN		0.1	3	**3**	μA
I_{SOURCE}	V_{OUT} Short to GND				
ADC0833CCJ		−14	**−6.5**		mA
ADC0833BCN/CCN		−14	−7.5	**−6.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}				
ADC0833CCJ		16	**8.0**		mA
ADC0833BCN/CCN		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Note 3)	$V_{REF}/2$ Open Circuit				
ADC0833CCJ		0.9	**4.5**		mA
ADC0833BCN/CCN		0.9	4.5	**4.5**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$ and $t_r = t_f = 20$ ns unless otherwise specified. These limits apply for $T_A = T_j = 25°C$.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
T_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 12)	Min				40	%
	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 13)		$C_L = 100$ pF				
		Data MSB First	650		1500	ns
		Data LSB First	250		600	ns
t_{1H}, t_{0H}—Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z		$C_L = 10$ pF, $R_L = 10k$	125		250	ns
		$C_L = 100$ pF, $R_L = 2k$		500		ns
		(see TRI-STATE Test Circuits)				
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: Internal zener diodes (approx. 7V) are connected from V^+ to GND and V_{CC} to GND. The zener at V^+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V^+. Functionality is therefore guaranteed for V^+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max. of 6.5V. It is recommended that a resistor be used to limit the max. current into V^+.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: See Applications, section 3.0.

Note 10: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

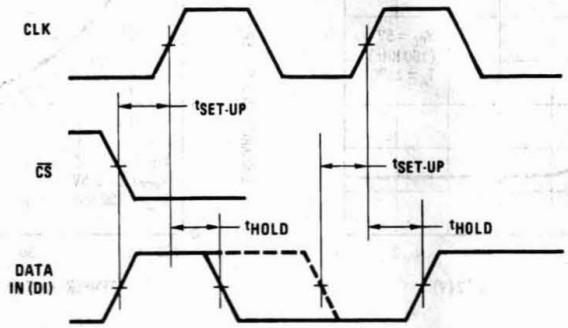
Note 11: Leakage current is measured with the clock not switching.

Note 12: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 1 μs. The maximum time the clock can be high is 60 μs. The clocked can be stopped when low so long as the analog input voltage remains stable.

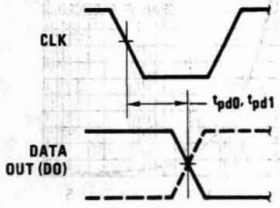
Note 13: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Timing Diagrams

Data Input Timing

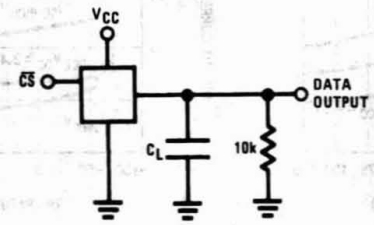


Data Output Timing

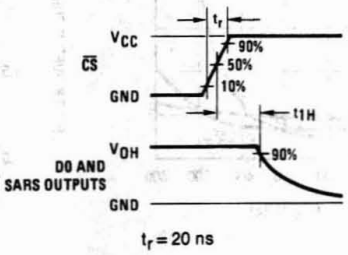


TRI-STATE Test Circuits and Waveforms

t_{1H}

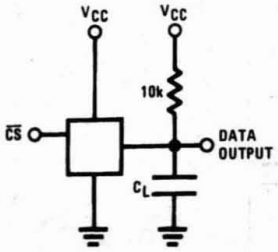


t_{1H}, C_L = 10 pF

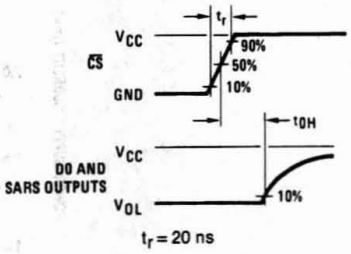


t_r = 20 ns

t_{0H}

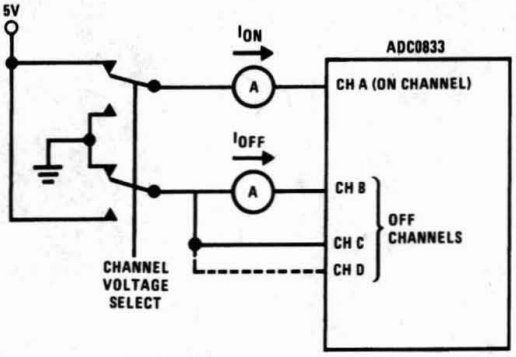


t_{0H}, C_L = 10 pF



t_r = 20 ns

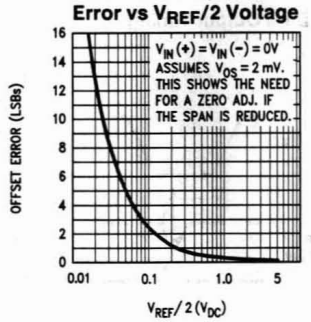
Leakage Current Test Circuit



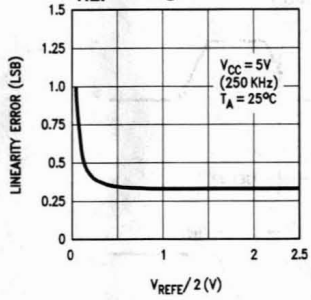
TL/H/5607–2

Typical Performance Characteristics

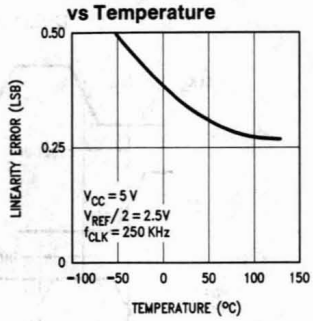
Effect of Unadjusted Offset Error vs $V_{REF}/2$ Voltage



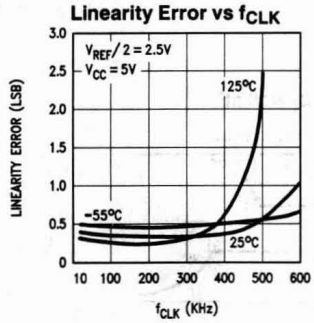
Linearity Error vs V_{REF} Voltage



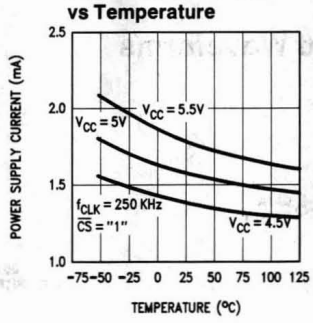
Linearity Error vs Temperature



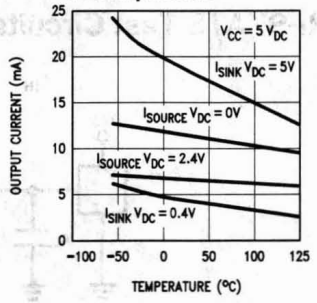
Linearity Error vs f_{CLK}



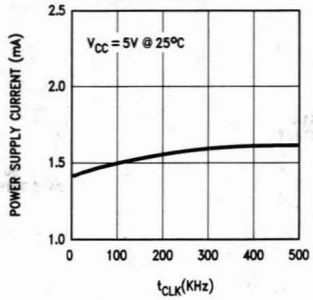
Power Supply Current vs Temperature



Output Current vs Temperature



Power Supply Current vs f_{CLK}



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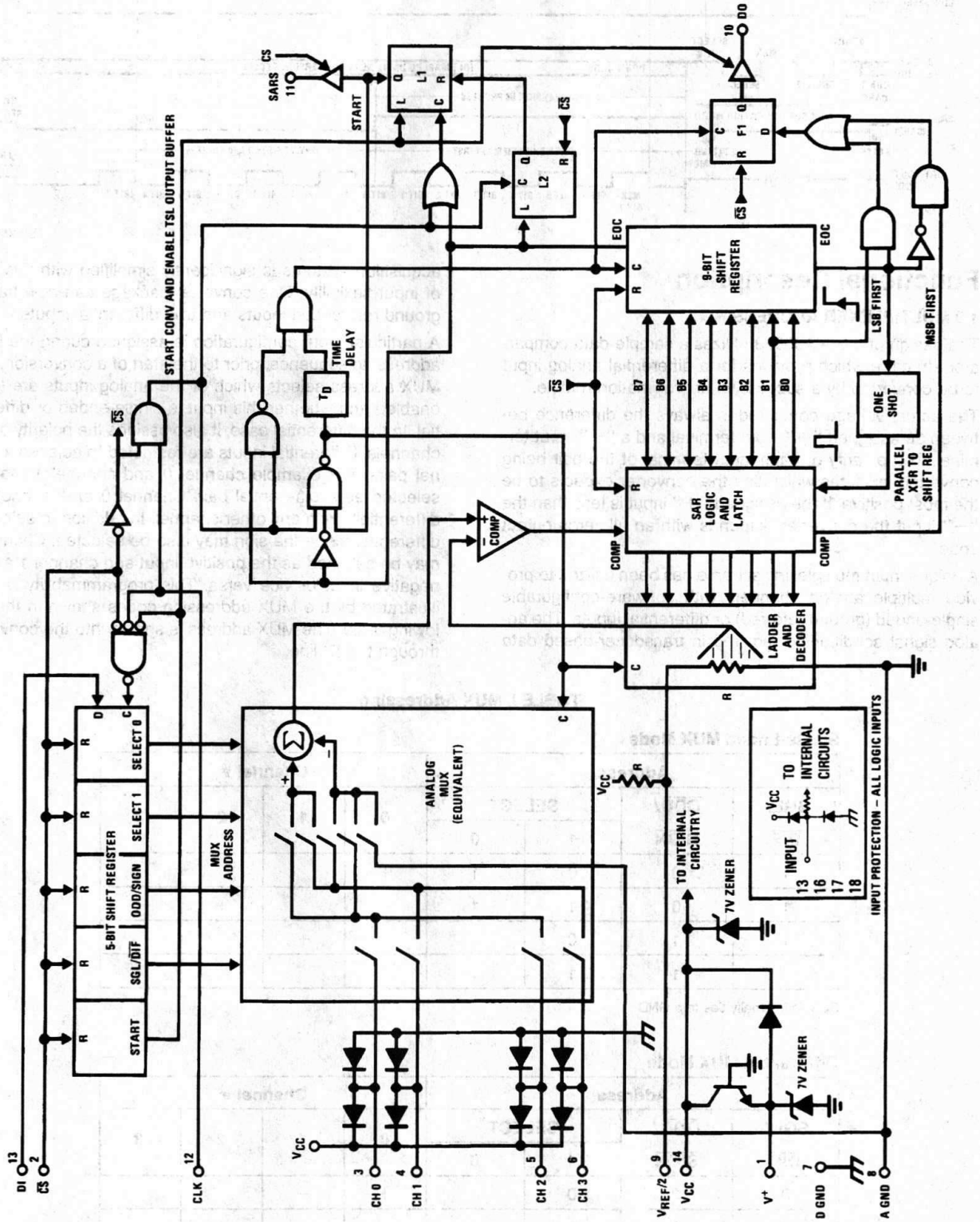
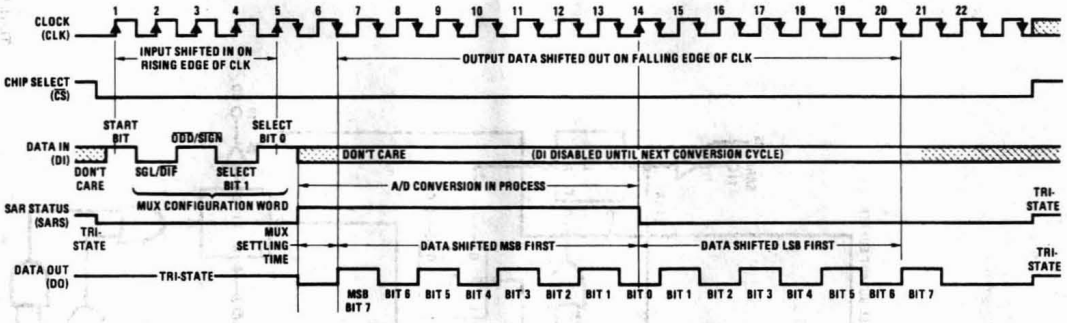
ADC0833 Functional Block Diagram



Timing Diagram



TL/H/5607–5

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of the ADC0833 utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended (ground referred) or differential inputs. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a differential pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following table. The MUX address is shifted into the converter through the DI line.

TABLE I. MUX Addressing

Single-Ended MUX Mode

Address				Channel #			
SGL/ $\overline{\text{DIF}}$	$\overline{\text{ODD}}$/ $\overline{\text{SIGN}}$	SELECT 1	SELECT 0	0	1	2	3
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

COM is internally ties to a GND

Differential MUX Mode

Address				Channel #			
SGL/ $\overline{\text{DIF}}$	$\overline{\text{ODD}}$/ $\overline{\text{SIGN}}$	SELECT 1	SELECT 0	0	1	2	3
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50mV above V_{CC}(typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagram and Functional Block Diagram and to follow a complete conversion sequence.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 4 bits to be the MUX assignment word.

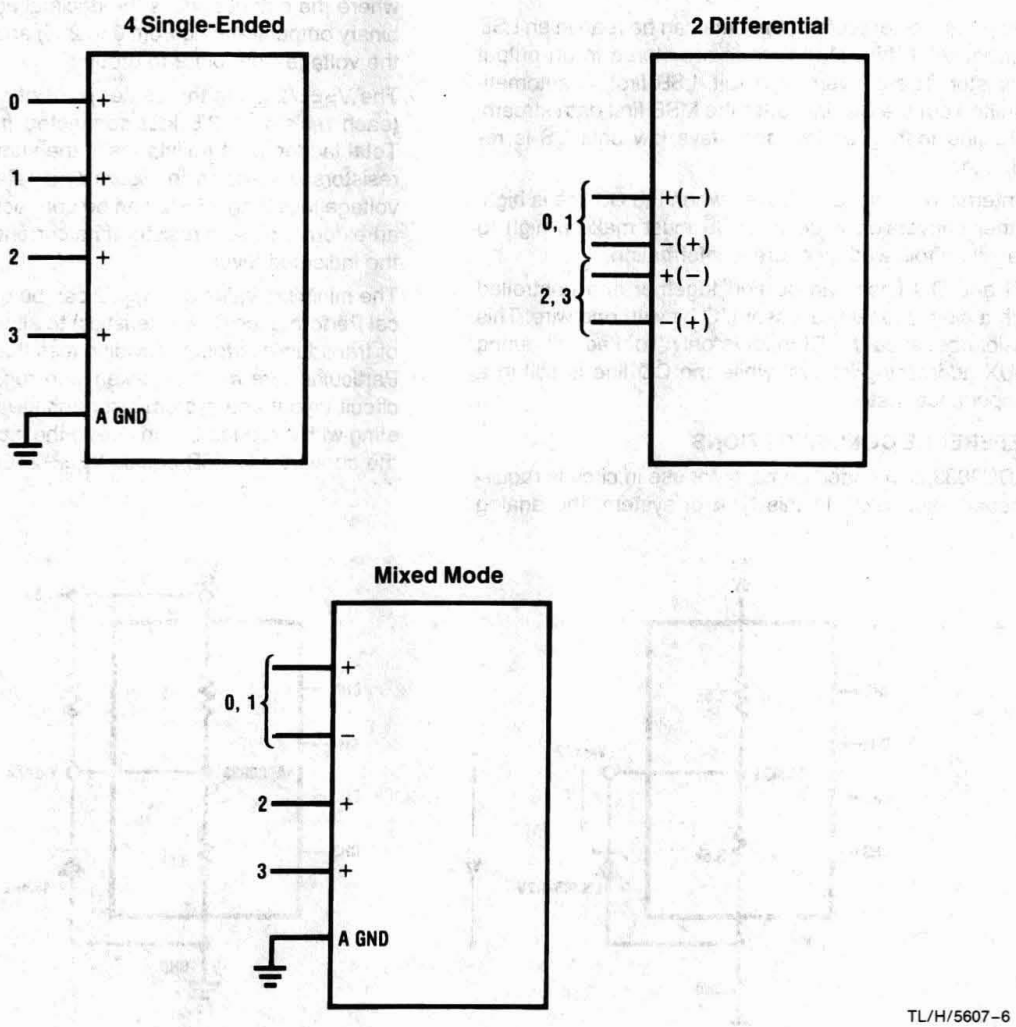


FIGURE 1. Analog Input Multiplexer Options for the ADC0833

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be read in an LSB first format. All 8 bits of the result are stored in an output shift register. The conversion result, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

3.0 REFERENCE CONSIDERATIONS

The ADC0833 is intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, an ADC0834 is a pin-for-pin compatible alternative since it has a V_{REF} input (note the ADC0834 needs one less bit of mux addressing information).

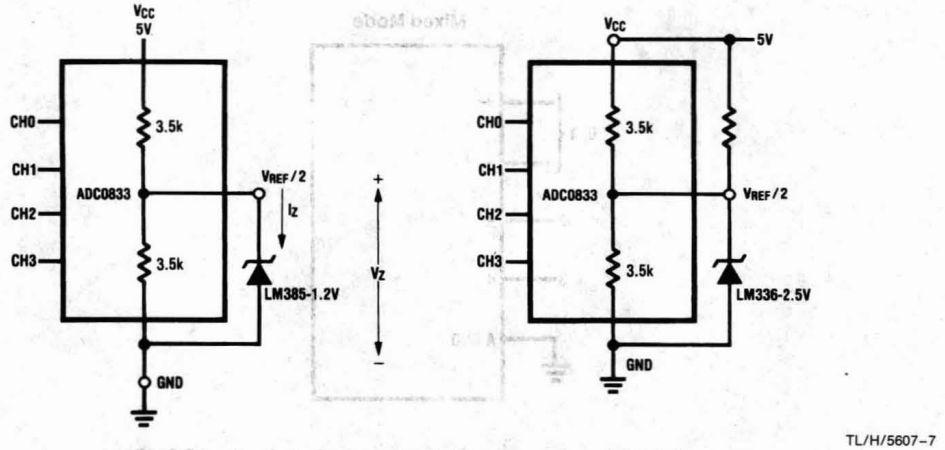
The voltage applied to the $V_{REF}/2$ pin defines the voltage span of the analog input [the difference between $V_{IN}(+)$ and $V_{IN}(-)$] over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+" input and "−" input is approximately *twice* the voltage at the $V_{REF}/2$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The LM385 and LM336 reference diodes are good low current devices to use with these converters. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256 \left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)} \right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF}/2$ is the voltage from pin 9 to ground.

The $V_{REF}/2$ pin is the center point of a two resistor divider (each resistor is 3.5 kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors. As shown in *Figure 2,* a reference diode with a voltage less than $V_{CC}/2$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF}/2$ can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



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$V_{FULL\text{-}SCALE} \cong 2.4V$ $V_{FULL\text{-}SCALE} \cong 5.0V$

Note: No external biasing resistor needed if $V_Z < \frac{V_{CC}}{2}$ and I_Z min $< \frac{V_{CC}/2 - V_Z}{1.75\ k\Omega}$

FIGURE 2. Reference Biasing Examples

...ional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the inputs be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ± 1 μA over temperature will create a 1 mV inut error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{In}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ fs\ adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The $V_{REF}/2$ voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0833 is the inclusion of a 7V zener diode connected from the V^+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3.*

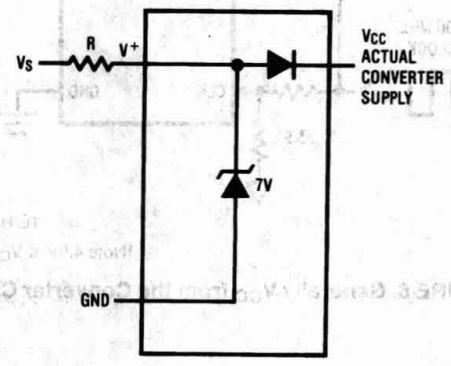

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FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4* and *5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 6* and *7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The of the A/D (~3 mA) and the relativ cies used (typically in the range of 10k ing the small value filter capacitor shown on the V_{CC} line to well under ¼ of an LSB. regulator can also be used in this mode. Th clock voltage swing which is in excess of V_Z. A limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V+ pin.

Applications

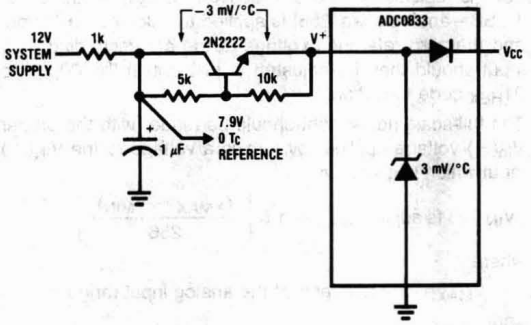

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FIGURE 4. Operating with a Temperature Compensated Reference

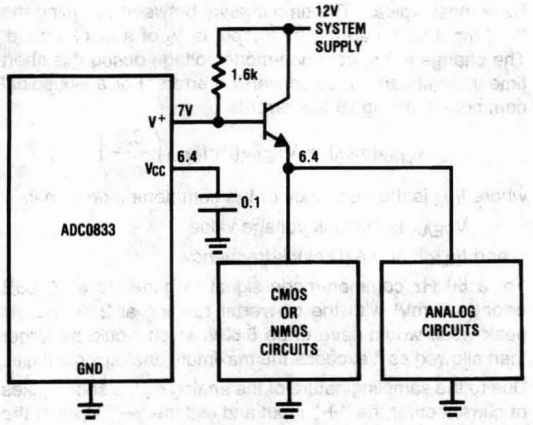

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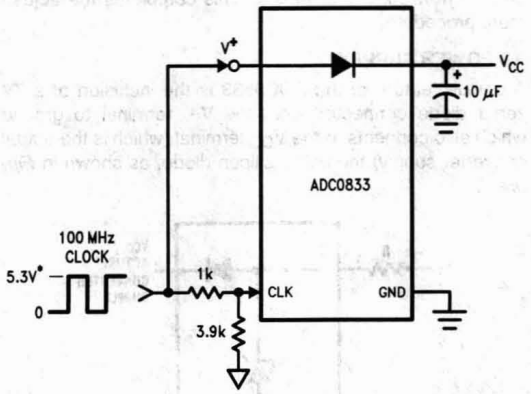
FIGURE 5. Using the A/D as the System Supply Regulator



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*Note 4.5V ≤ V_{CC} ≤ 6.3V

FIGURE 6. Generally V_{CC} from the Converter Clock

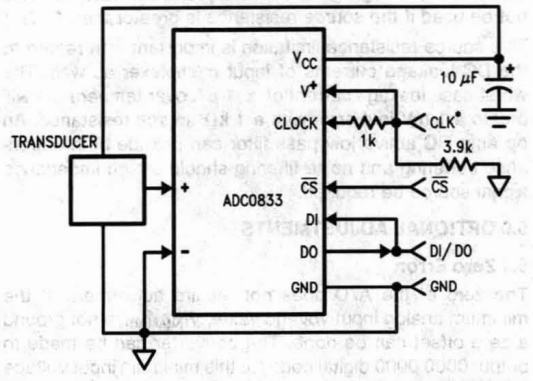

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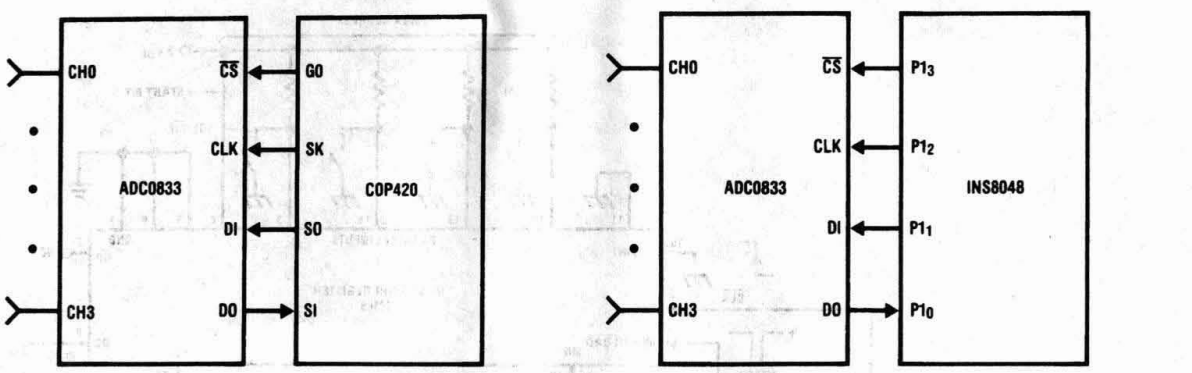
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



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COP CODING EXAMPLE

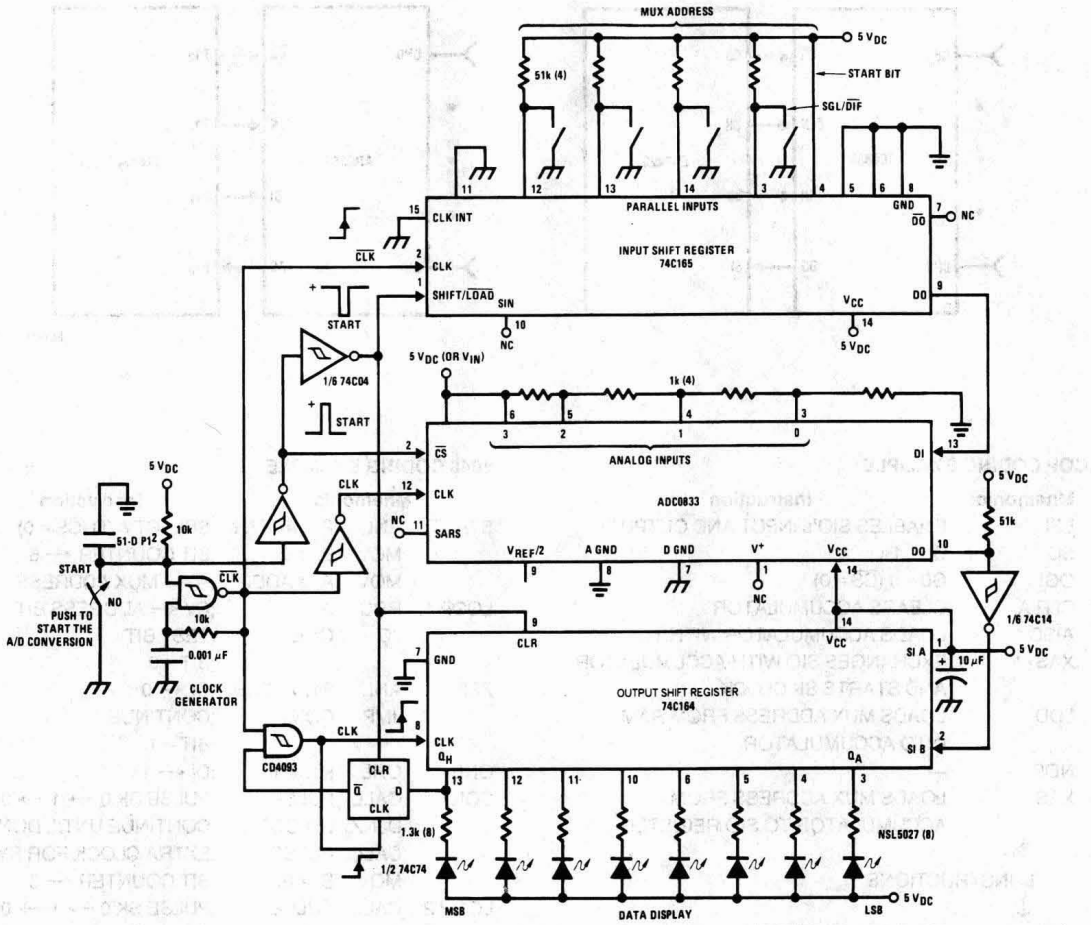
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑	
8 INSTRUCTIONS	
↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

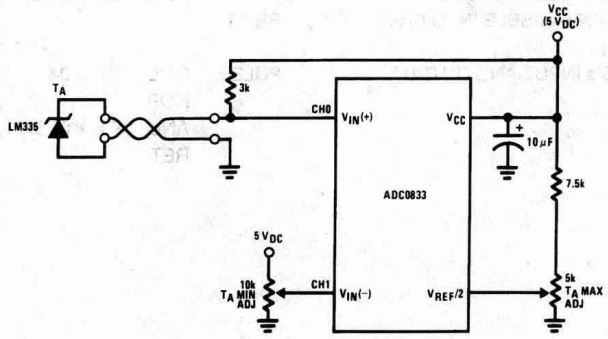
	Mnemonic		Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0833 Evaluation



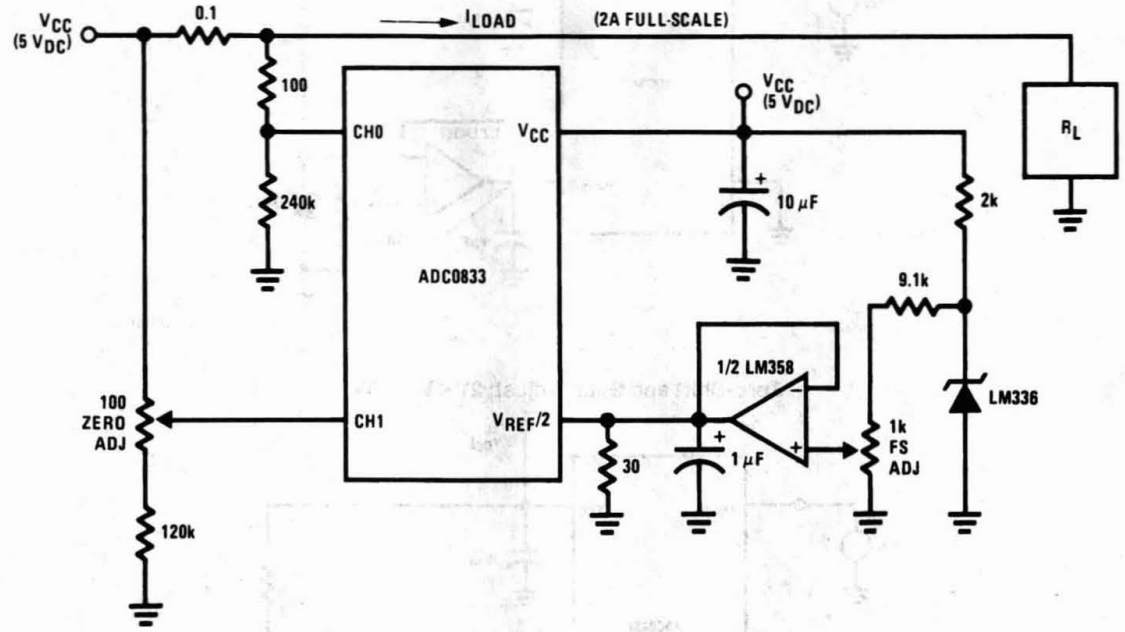
Low Cost Remote Temperature Sensor



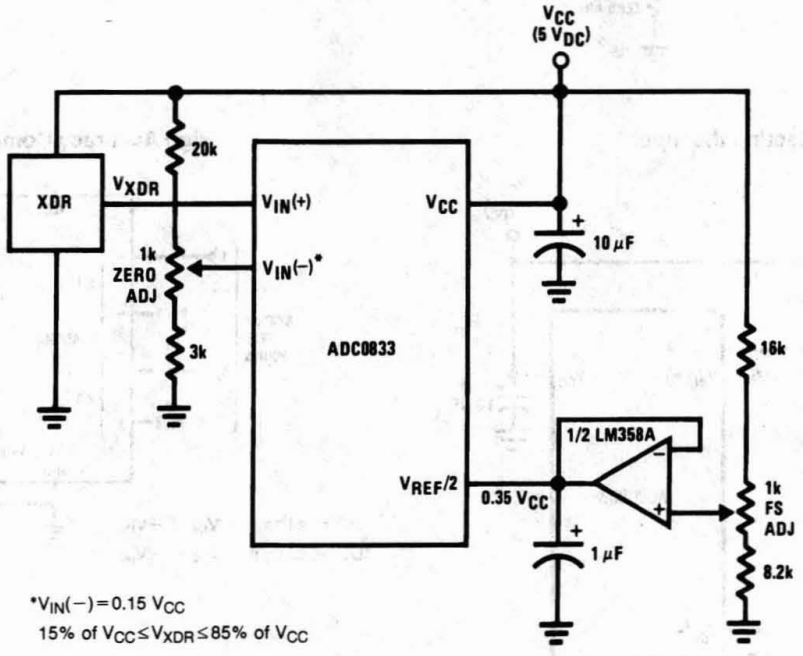
TL/H/5607–11

Applications (Continued)

Digitizing a Current Flow



Operating with Automotive Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

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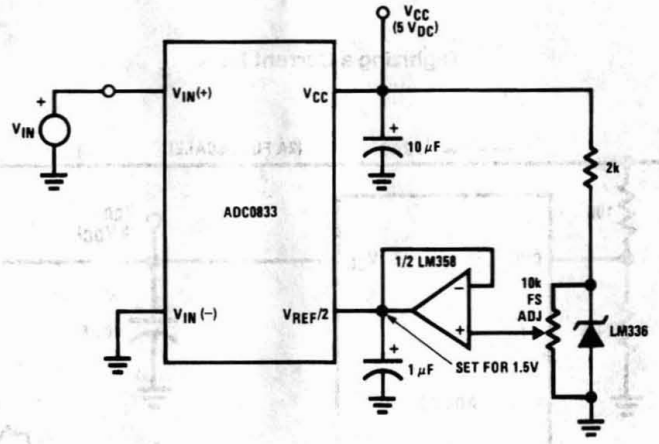
Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$



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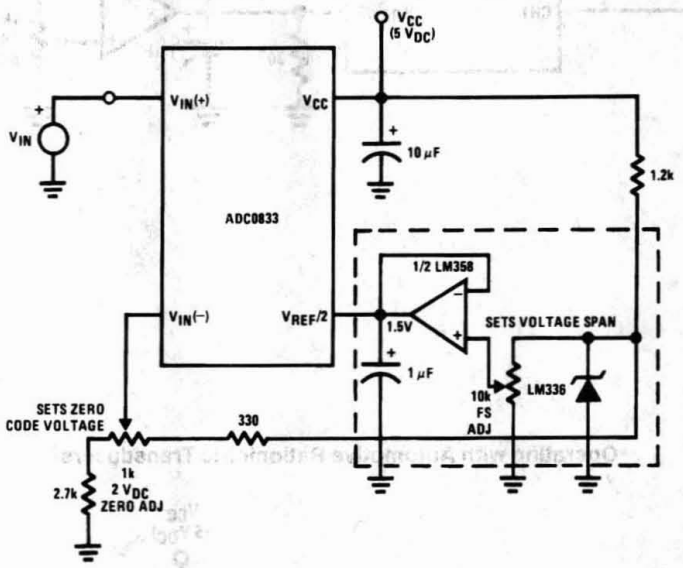
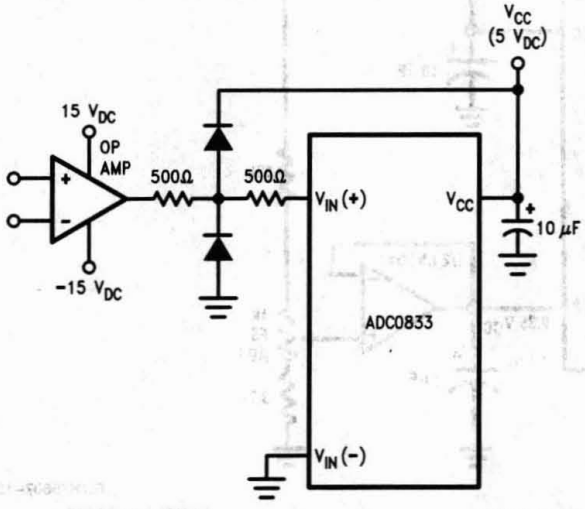
Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



TL/H/5607–19

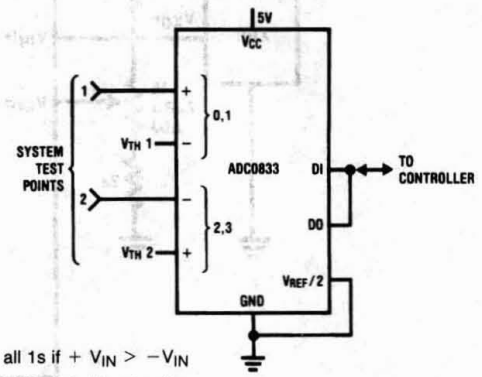
Protecting the Input



Diodes are 1N914

TL/H/5607–20

High Accuracy Comparators



DO = all 1s if $+V_{IN} > -V_{IN}$

DO = all 0s if $+V_{IN} < -V_{IN}$

TL/H/5607–13

For additional application ideas, refer to the data sheet for the ADC0831 family of serial data converters.

Ordering Information

Part Number	Temperature Range	Total Unadjusted Error
ADC0833BCN	0°C to +70°C	±1/2 LSB
ADC0833CCJ	−40°C to +85°C	±1 LSB
ADC0833CCN	0°C to +70°C	

National Semiconductor

ADC08031/ADC08032/ADC08034/ADC08038 8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

General Description

The ADC08031/ADC08032/ADC08034/ADC08038 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

The ADC08034 and ADC08038 provide a 2.6V band-gap derived reference. For devices offering guaranteed voltage reference performance over temperature see ADC08131, ADC08134 and ADC08138.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Applications

- Digitizing automotive sensors
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Test systems
- Embedded diagnostics

Features

- Serial digital data link requires few I/O pins
- Analog input track/hold function
- 2-, 4-, or 8-channel input multiplexer options with address logic
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- On chip 2.6V band-gap reference
- 0.3″ standard width 8-, 14-, or 20-pin DIP package
- 14-, 20-pin small-outline packages

Key Specifications

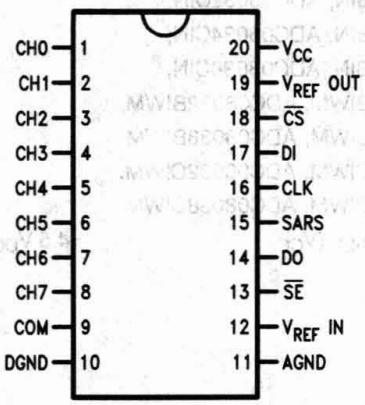
- Resolution — 8 bits
- Conversion time (f_C = 1 MHz) — 8μs (max)
- Power dissipation — 20mW (max)
- Single supply — $5V_{DC}$ (±5%)
- Total unadjusted error — ±½ LSB and ±1LSB
- No missing codes over temperature

Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC08031BIN, ADC08031CIN	N08E
ADC08032BIN, ADC08032CIN	N08E
ADC08034BIN, ADC08034CIN	N14A
ADC08038BIN, ADC08038CIN	N20A
ADC08031BIWM, ADC08031CIWM, ADC08032BIWM, ADC08032CIWM, ADC08034BIWM, ADC08034CIWM	M14B
ADC08038BIWM, ADC08038CIWM	M20B

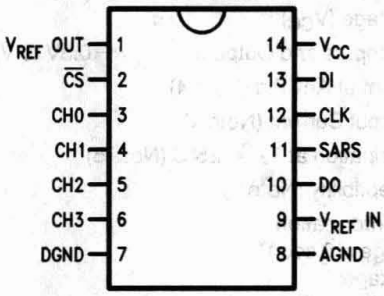
Connection Diagrams

ADC08038



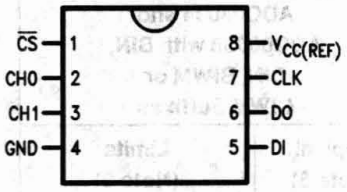
TL/H/10555–2

ADC08034



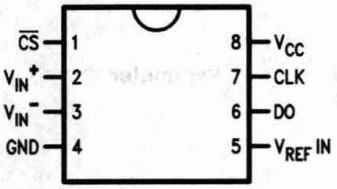
TL/H/10555–3

ADC08032
Dual-In-Line Package



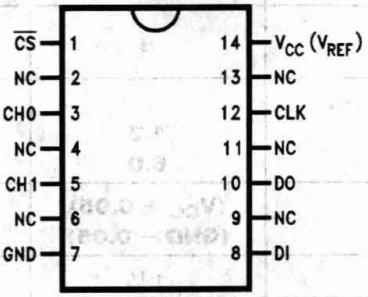
TL/H/10555–4

ADC08031
Dual-In-Line Package



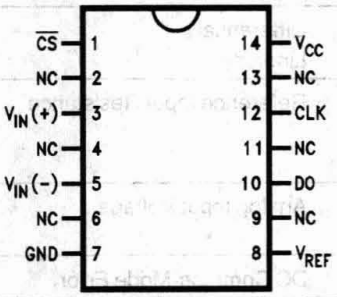
TL/H/10555–5

ADC08032
Small Outline Package



TL/H/10555–30

ADC08031
Small Outline Package



TL/H/10555–31

2

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Power Dissipation at T_A = 25°C (Note 5)	800 mW
ESD Susceptibility (Note 6)	1500V
Soldering Information	
N Package (10 sec.)	260°C
SO Package:	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08031BIN, ADC08031CIN, ADC08032BIN, ADC08032CIN, ADC08034BIN, ADC08034CIN, ADC08038BIN, ADC08038CIN, ADC08031BIWM, ADC08032BIWM, ADC08034BIWM, ADC08038BIWM ADC08031CIWM, ADC08032CIWM, ADC08034CIWM, ADC08038CIWM	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_{CC})	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = V_{REF} = +5 V_{DC}, and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	ADC08031, ADC08032, ADC08034 and ADC08038 with BIN, CIN, BIWM or CIWM Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
	Total Unadjusted Error BIN, BIWM CIN, CIWM	(Note 10)		 **±½** **±1**	 LSB (max) LSB (max)
	Differential Linearity			**8**	Bits (min)
R_{REF}	Reference Input Resistance	(Note 11)	3.5	 **1.3** **6.0**	kΩ kΩ (min) kΩ (max)
V_{IN}	Analog Input Voltage	(Note 12)		**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
	DC Common-Mode Error			±¼	LSB (max)
	Power Supply Sensitivity	V_{CC} = 5V ±5%, V_{REF} = 4.75V		**±¼**	LSB (max)
	On Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		0.2 **1**	μA (max)
		On Channel = 0V, Off Channel = 5V		−0.2 **−1**	μA (max)
	Off Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**	μA (max)
		On Channel = 0V, Off Channel = 5V		0.2 **1**	μA (max)

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V_{REF} = +5\ V_{DC}$, and $f_{CLK} = 1$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08031, ADC08032, ADC08034 and ADC08038 with BIN, CIN, BIWM or CIWM Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.25V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5.0V$		**1**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$		**−1**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$		**−3.0** **3.0**	μA (max) μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		**−6.5**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		**8.0**	mA (min)
I_{CC}	Supply Current ADC08031, ADC08034, and ADC08038 ADC08032 (Note 16)	$\overline{CS}$ = HIGH		 **3.0** **7.0**	 mA (max) mA (max)
REFERENCE CHARACTERISTICS					
$V_{REF}OUT$	Nominal Reference Output	$V_{REF}OUT$ Option Available Only on ADC08034 and ADC08038	2.6		V

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V_{REF} = +5\ V_{DC}$, and $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK}	Clock Frequency		10	 **1**	kHz (min) MHz (max)
	Clock Duty Cycle (Note 14)			**40** **60**	% (min) % (max)
T_C	Conversion Time (Not Including MUX Addressing Time)	$f_{CLK} = 1$ MHz		**8** **8**	$1/f_{CLK}$ (max) μs (max)
t_{CA}	Acquisition Time			**½**	$1/f_{CLK}$(max)
t_{SELECT}	CLK High while $\overline{CS}$ is High		50		ns
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			**25**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 15)	$C_L = 100$ pF: Data MSB First Data LSB First		 **250** **200**	 ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	$C_L = 10$ pF, $R_L = 10$ kΩ (see TRI-STATE Test Circuits)	50		ns
		$C_L = 100$ pF, $R_L = 2$ kΩ		**180**	ns (max)
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to AGND = DGND = 0 V_{DC}, unless otherwise specified.

Note 4: When the input voltage V_{IN} at any pin exceeds the power supplies ($V_{IN} <$ (AGND or DGND) or $V_{IN} > V_{CC}$,) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J_{MAX}}$, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{J_{MAX}} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For devices with suffixes BIN, CIN, BIJ, CIJ, BIWM, and CIWM $T_{J_{MAX}} = 125°C$. For devices with suffix CMJ, $T_{J_{MAX}} = 150°C$. The typical thermal resistances (θ_{JA}) of these parts when board mounted follow: ADC08031 and ADC08032 with BIN and CIN suffixes 120°C/W, ADC08034 with BIN and CIN suffixes 95°C/W, ADC08038 with BIN and CIN suffixes 80°C/W. ADC08031 with BIWM and CIWM suffixes 140°C/W, ADC08032 with BIWM and CIWM suffixes 140°C/W, ADC08034 with BIWM and CIWM suffixes 140°C/W, ADC08038 with BIWM and CIWM suffixes 91°C/W.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or *Linear Data Book* section "Surface Mount" for other methods of soldering surface mount devices.

Note 8: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

Note 9: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Total unadjusted error includes offset, full-scale, linearity, multiplexer.

Note 11: Cannot be tested for the ADC08032.

Note 12: For $V_{IN(-)} \geq V_{IN(+)}$ the digital code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. During testing at low V_{CC} levels (e.g., 4.5V), high level analog inputs (e.g., 5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 13: Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining seven off channels tied low (0 V_{DC}), total current flow through the off channels is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channels is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.

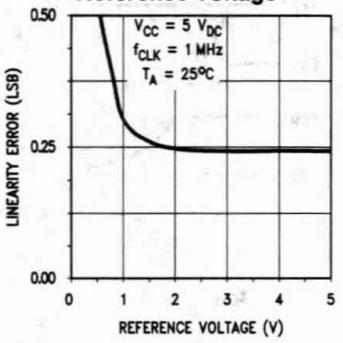
Note 14: A 40% to 60% duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits the minimum time the clock is high or low must be at least 450 ns. The maximum time the clock can be high or low is 100 μs.

Note 15: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

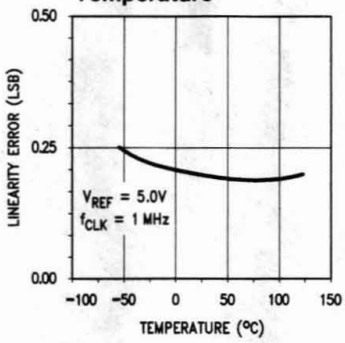
Note 16: For the ADC08032 V_{REF}IN is internally tied to V_{CC}, therefore, for the ADC08032 reference current is included in the supply current.

Typical Performance Characteristics

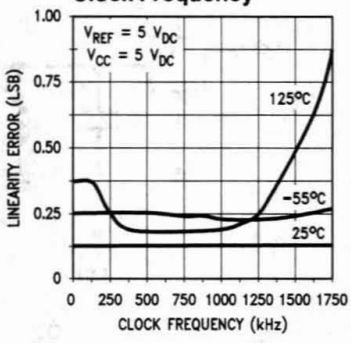
Linearity Error vs Reference Voltage



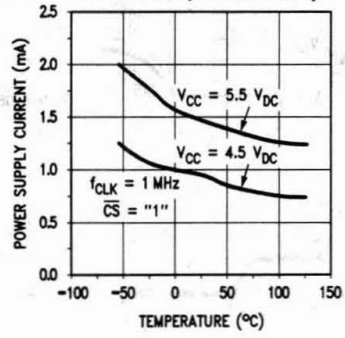
Linearity Error vs Temperature



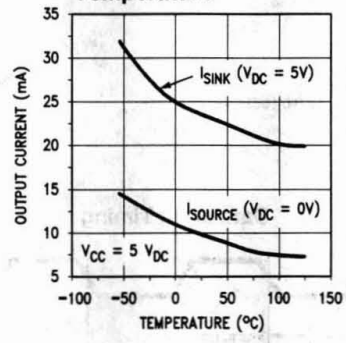
Linearity Error vs Clock Frequency



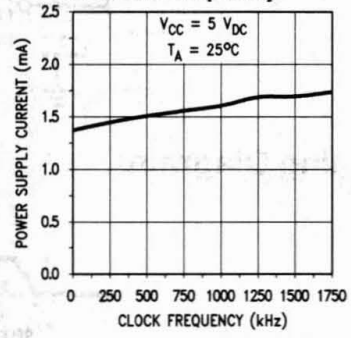
Power Supply Current vs Temperature (ADC08038, ADC08034, ADC08031)



Output Current vs Temperature



Power Supply Current vs Clock Frequency



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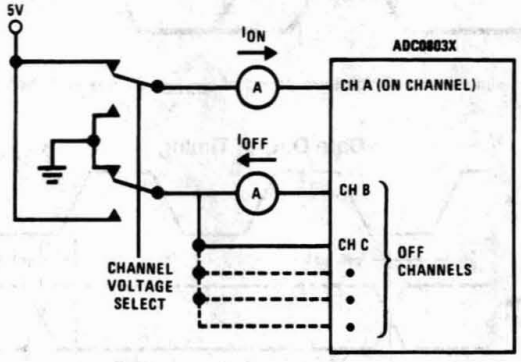
Note: For ADC08032 add I_{REF}

Leakage Current Test Circuit



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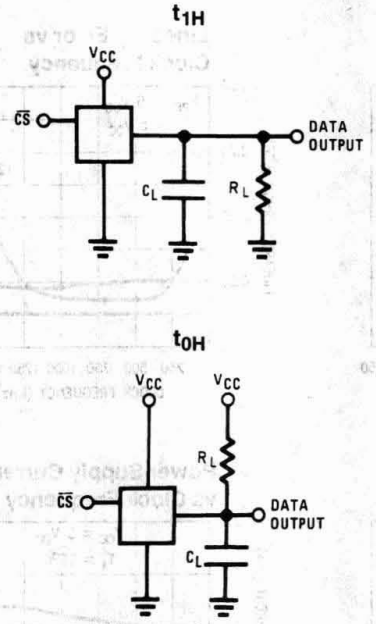
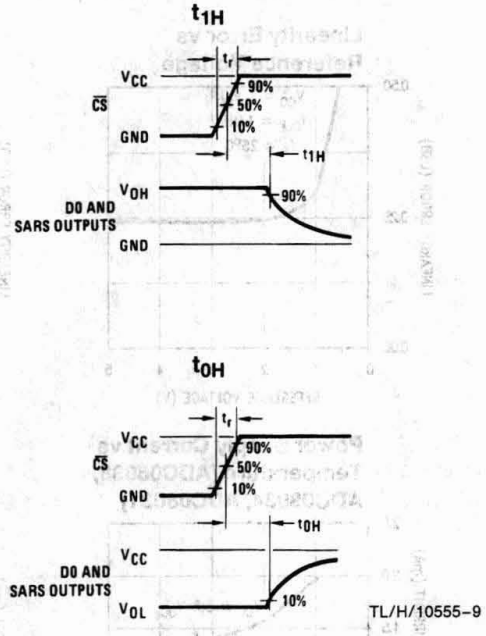
TRI-STATE Test Circuits and Waveforms



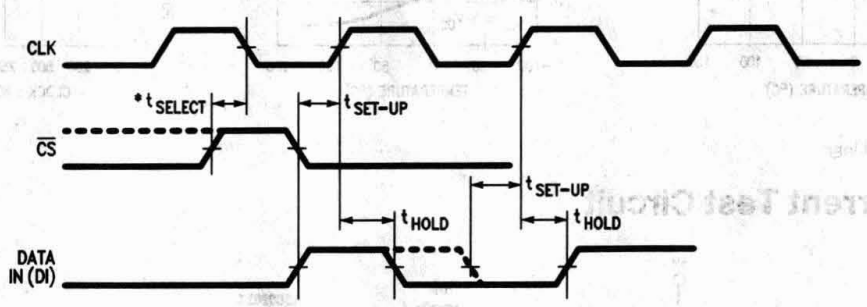


TL/H/10555–8

TL/H/10555–9

Timing Diagrams

Data Input Timing



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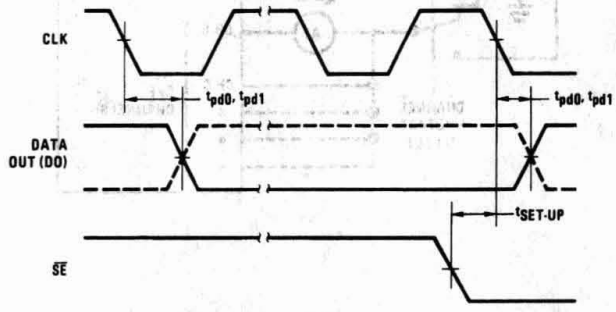
*To reset these devices, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. Otherwise these devices are compatible with industry standards ADC0831/2/4/8.

Data Output Timing



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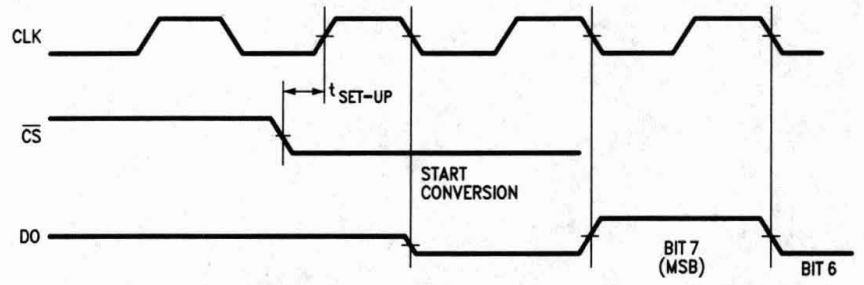
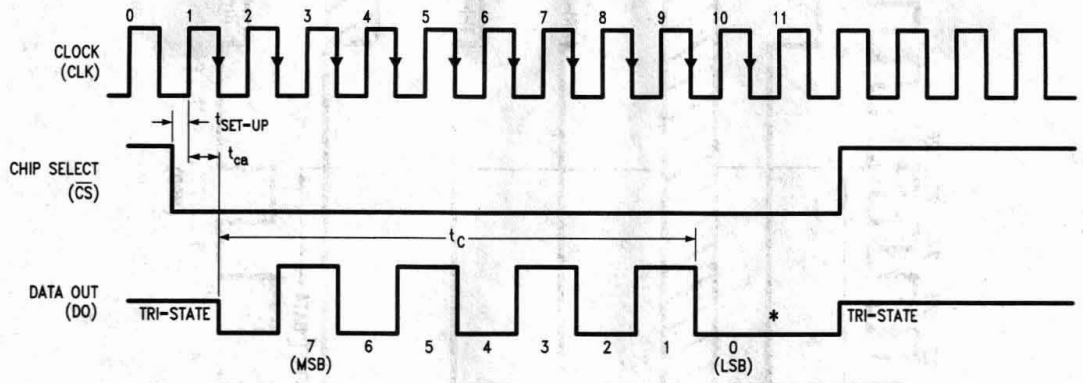
ADC08031 Start Conversion Timing



TL/H/10555–12

Timing Diagrams (Continued)

ADC08031 Timing



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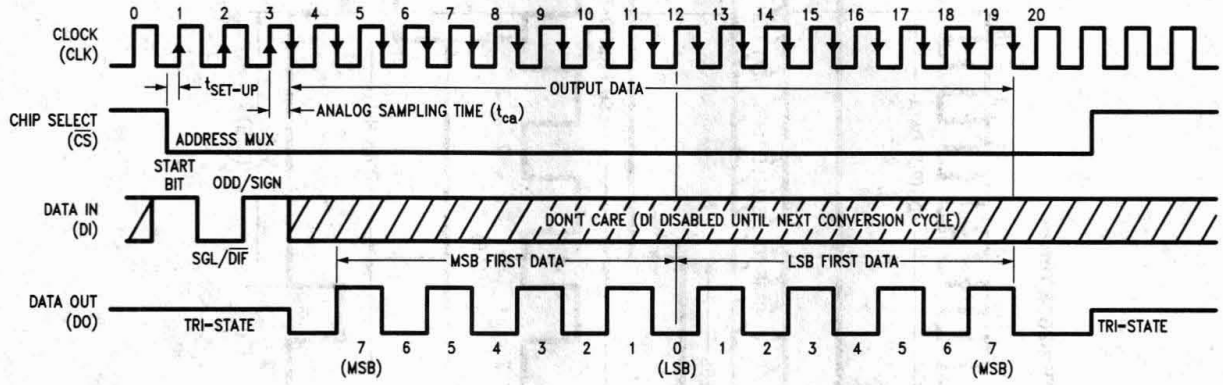
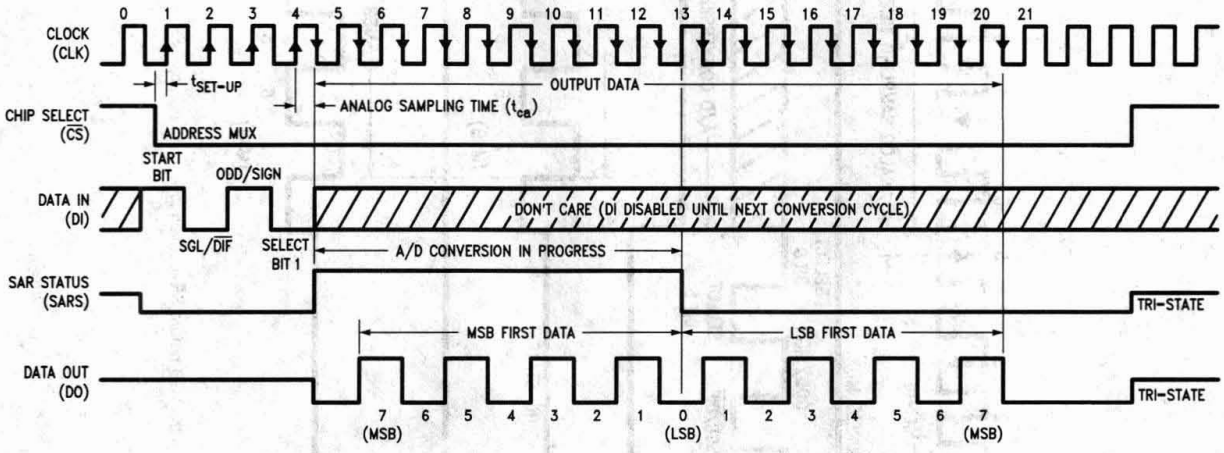
*LSB first output not available on ADC08031.
LSB information is maintained for remainder of clock periods until $\overline{CS}$ goes high.

ADC08032 Timing



TL/H/10555–14

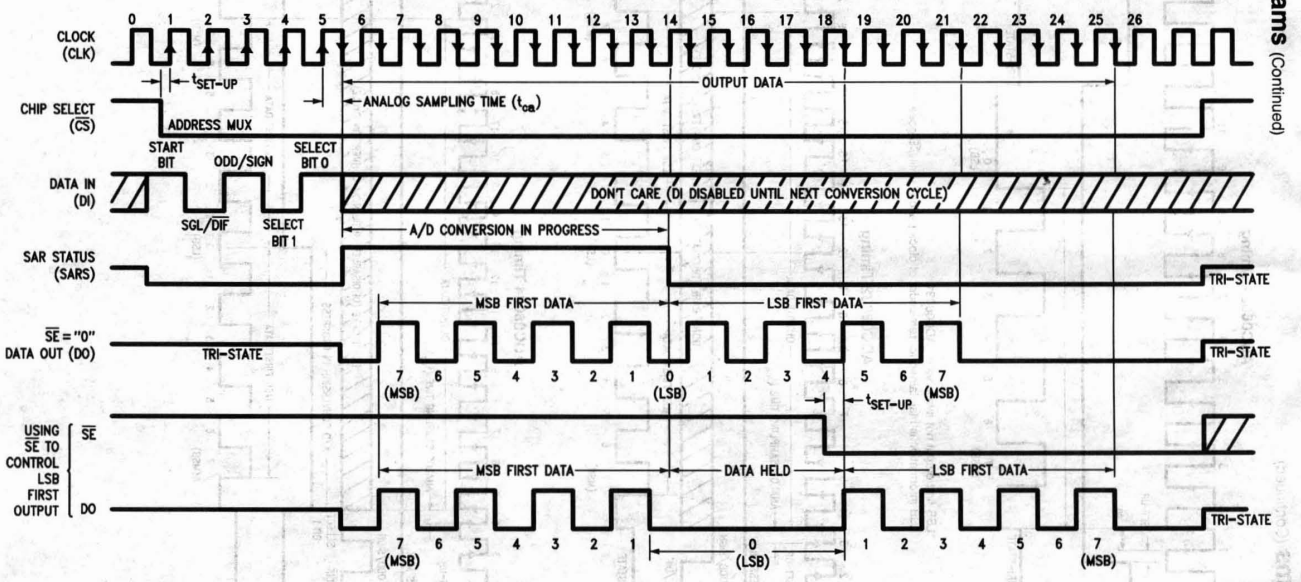
ADC08034 Timing



TL/H/10555–15

Timing Diagrams (Continued)

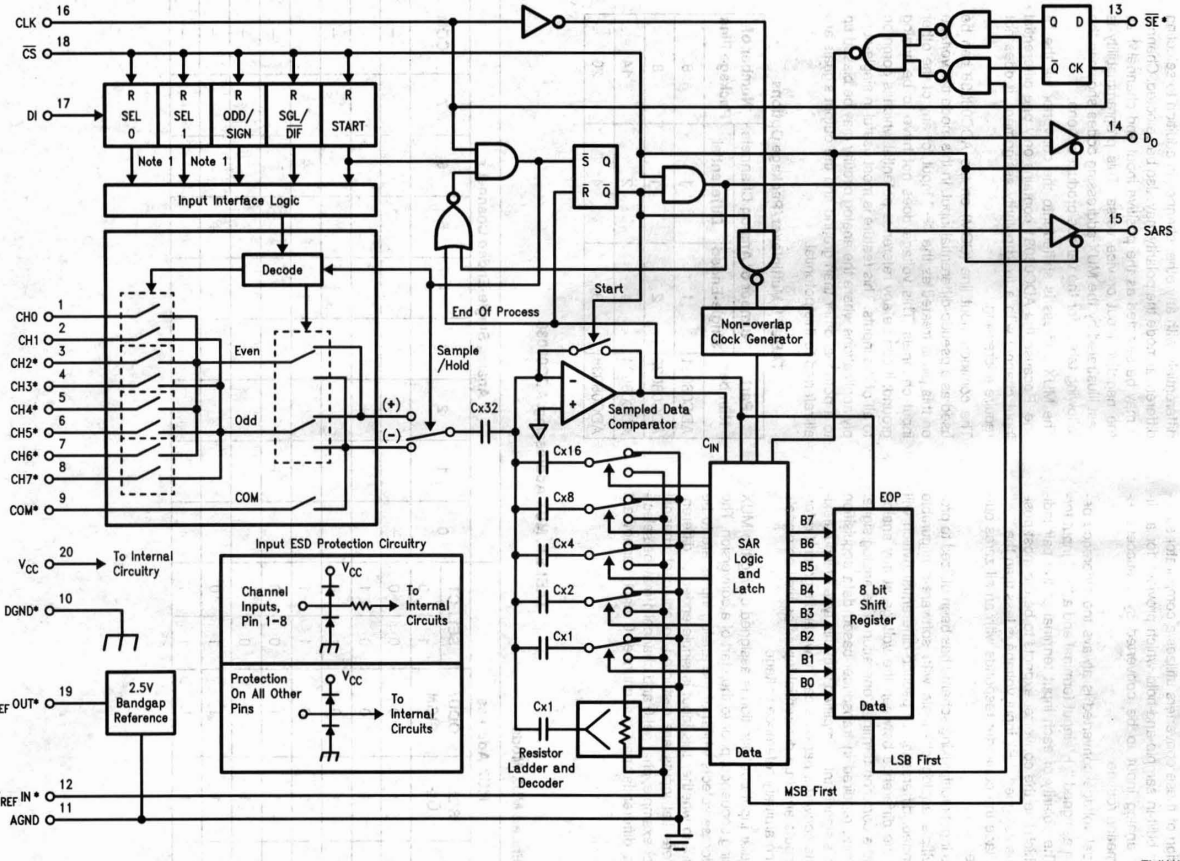
ADC08038 Timing



TL/H/10555–16

*Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC08038 Functional Block Diagram



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*Some of these functions/pins are not available with other options.

Note 1: For the ADC08034, the "SEL 1" Flip-Flop is bypassed, for the ADC08032, both "SEL 0" and "SEL 1" Flip-Flops are bypassed.

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive-approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential (which will convert the difference between the voltage at any analog input and a common terminal) operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC08031 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line (COM) on the ADC08038 can be used as a pseudo-differential input. In this mode the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply applications where the analog circuity may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC08031	1	1	8
ADC08032	2	1	8
ADC08034	4	2	14
ADC08038	8	4	20

TABLE II. MUX Addressing: ADC08038

Single-Ended MUX Mode

MUX Address					Analog Single-Ended Channel #								
START	SGL/$\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0	1	2	3	4	5	6	7	COM
			1	0									
1	1	0	0	0	+								−
1	1	0	0	1			+						−
1	1	0	1	0					+				−
1	1	0	1	1							+		−
1	1	1	0	0		+							−
1	1	1	0	1				+					−
1	1	1	1	0						+			−
1	1	1	1	1								+	−

Functional Description (Continued)

TABLE II. MUX Addressing: ADC08038 (Continued)

Differential MUX Mode

MUX Address					Analog Differential Channel-Pair #							
					0		1		2		3	
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
1	0	0	0	0	+	−						
1	0	0	0	1			+	−				
1	0	0	1	0					+	−		
1	0	0	1	1							+	−
1	0	1	0	0	−	+						
1	0	1	0	1			−	+				
1	0	1	1	0					−	+		
1	0	1	1	1							−	+

TABLE III. MUX Addressing: ADC08034

Single-Ended MUX Mode

MUX Address				Channel #			
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	0	1	2	3
1	1	0	0	+			
1	1	0	1			+	
1	1	1	0		+		
1	1	1	1				+

COM is internally tied to AGND

Differential MUX Mode

MUX Address				Channel #			
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	0	+	−		
1	0	0	1			+	−
1	0	1	0	−	+		
1	0	1	1			−	+

TABLE IV. MUX Addressing: ADC08032

Single-Ended MUX Mode

MUX Address			Channel #	
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	1	0	+	
1	1	1		+

COM is internally tied to AGND

Differential MUX Mode

MUX Address			Channel #	
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	0	0	+	−
1	0	1	−	+

2

Functional Description (Continued)

Since the input configuration is under software control, it can be modified as required before each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

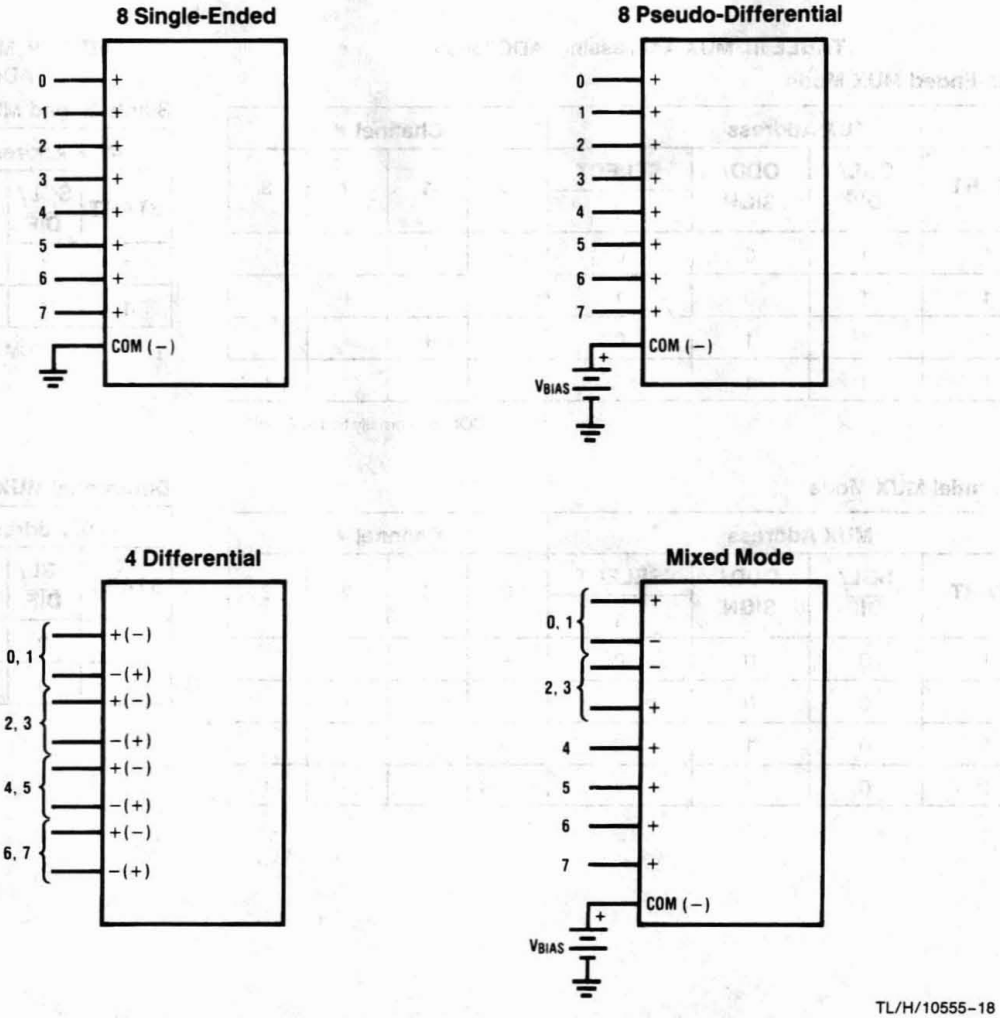
The analog input voltages for each channel can range from 50mV below ground to 50mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows many functions to be included in a small package and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate timing diagram is shown for each device.

1. A conversion is initiated by pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.
2. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.



TL/H/10555–18

FIGURE 1. Analog Input Multiplexer Options for the ADC08038

Functional Description (Continued)

3. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SARS line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).
4. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.
5. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison the comparator's output is shipped to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
6. After 8 clock periods the conversion is completed. The SARS line returns low to indicate this ½ clock cycle later.
7. The stored data in the successive approximation register is loaded into an internal shift register. If the programmer prefers the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. On the ADC08038 the $\overline{SE}$ line is brought out and if held high the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low the data is clocked out LSB first. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. The ADC08031 is an exception in that its data is only output in MSB first format.
8. All internal registers are cleared when the $\overline{CS}$ line is high and the t_{SELECT} requirement is met. See Data Input Timing under Timing Diagrams. If another conversion is desired $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

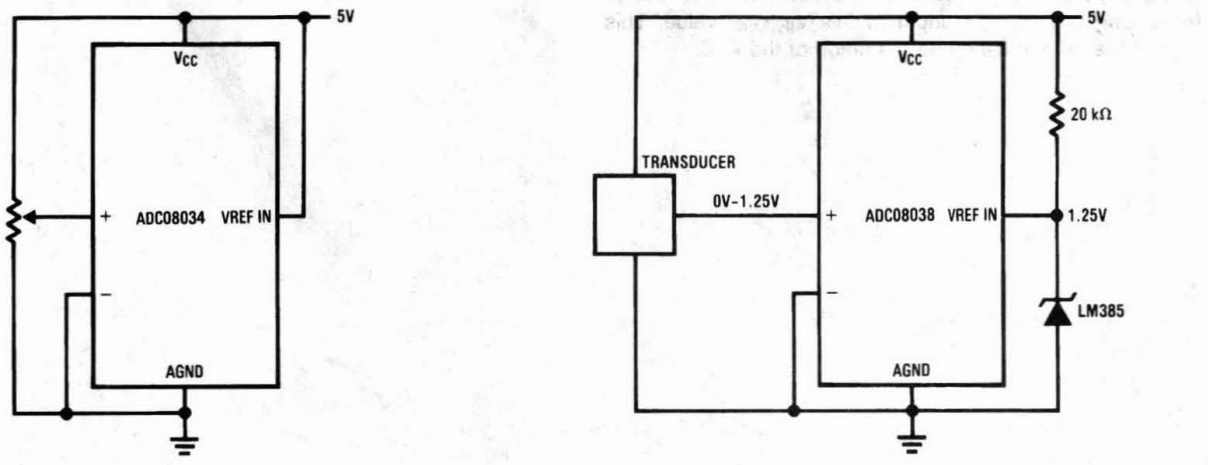
3.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input on these converters, $V_{REF}IN$, defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$ over which the 256 possible output codes apply. The devices can be used either in ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance which can be as low as 1.3kΩ. This pin is the top of a resistor divider string and capacitor array used for the successive approximation conversion.

In a ratiometric system the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $V_{REF}IN$ pin can be tied to V_{CC} (done internally on the ADC08032). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. For the ADC08034 and the ADC08038 a band-gap derived reference voltage of 2.6V (Note 8) is tied to $V_{REF}OUT$. This can be tied back to $V_{REF}IN$. Bypassing $V_{REF}OUT$ with a 100μF capacitor is recommended. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



TL/H/10555–19

a) Ratiometric

b) Absolute with a Reduced Span

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60Hz common-mode signal to generate a ¼ LSB error (≈ 5mV) with the converter running at 250kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. Bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1μA over temperature will create a 1mV input error with a 1kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for V_{REF} = 5.000V_{DC}).

5.2 Full Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF}IN input (or V_{CC} for the ADC08032) for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+)\,fs\,adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

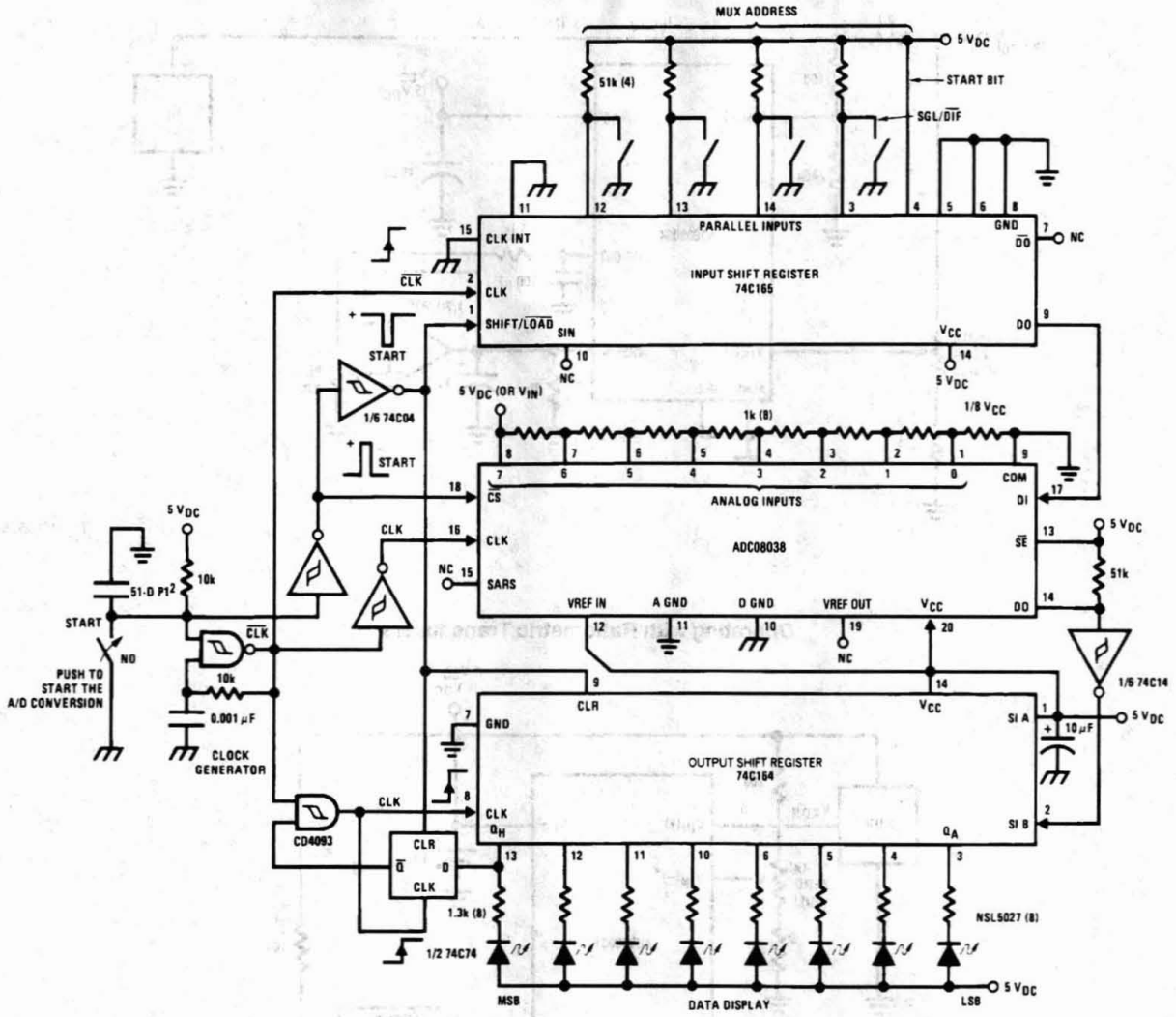
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF}IN (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

Applications

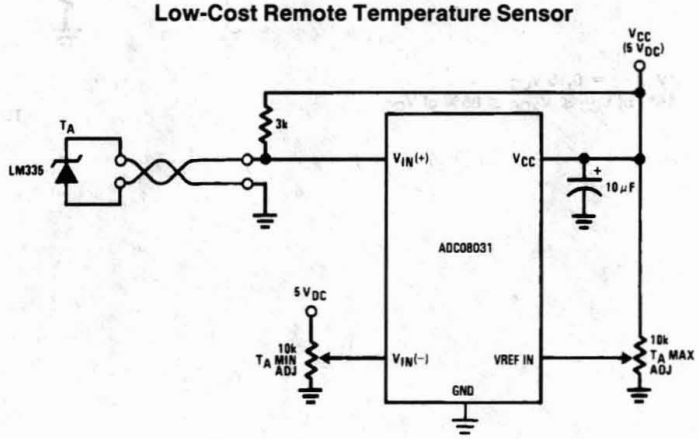
A "Stand-Alone" Hook-Up for ADC08038 Evaluation



*Pinouts shown for ADC08038.

For all other products tie to pin functions as shown.

Low-Cost Remote Temperature Sensor



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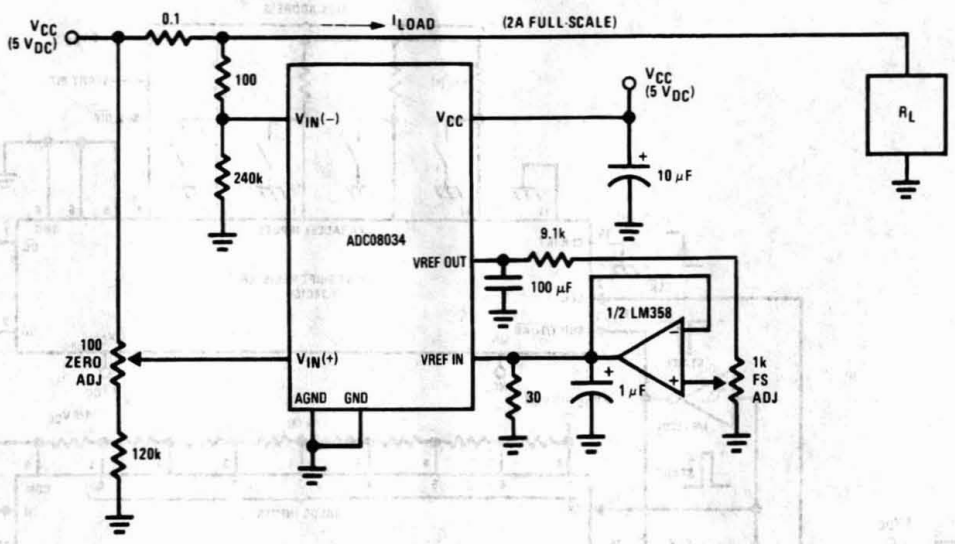
Applications (Continued)

Digitizing a Current Flow



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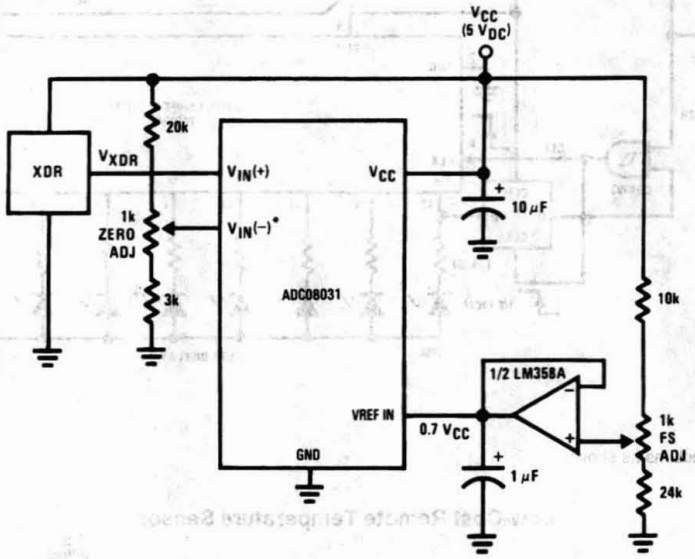
Operating with Ratiometric Transducers



*$V_{IN}(-)$ = 0.15 V_{CC}
15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}

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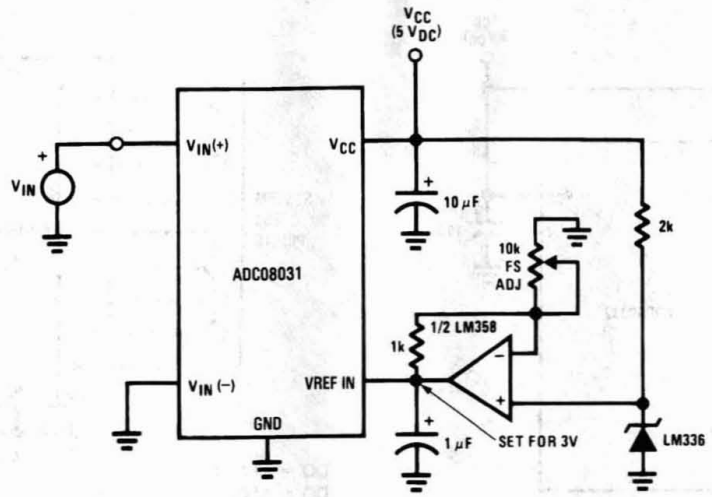
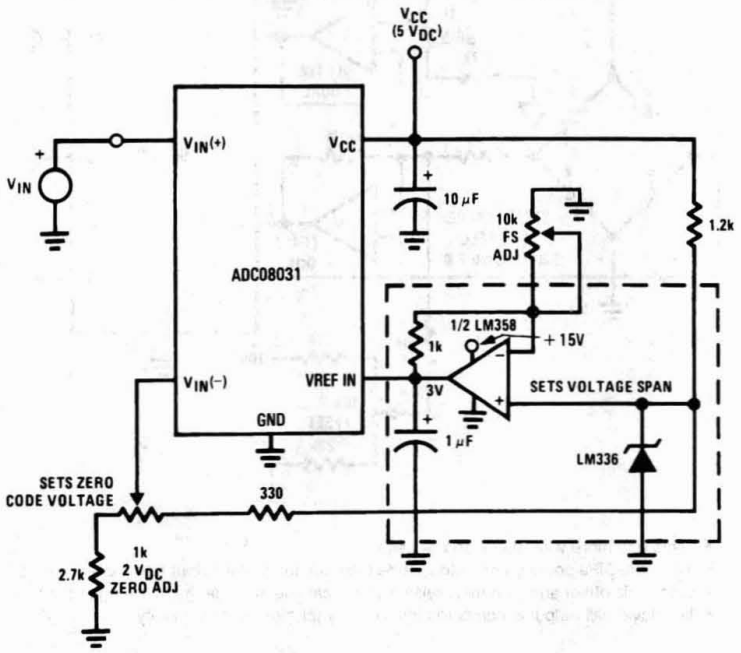
Applications (Continued)

Span Adjust; 0V ≤ V_{IN} ≤ 3V



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



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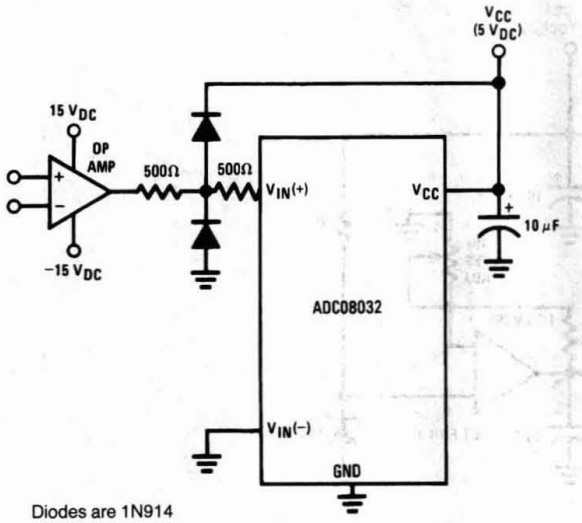
Applications (Continued)

Protecting the Input



Diodes are 1N914

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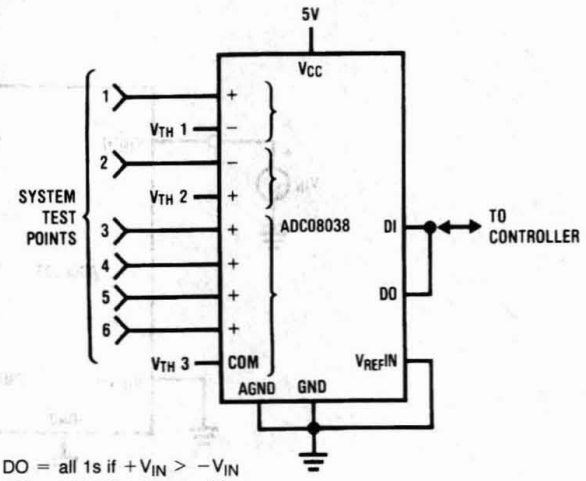
High Accuracy Comparators



DO = all 1s if $+V_{IN} > -V_{IN}$
DO = all 0s if $+V_{IN} < -V_{IN}$

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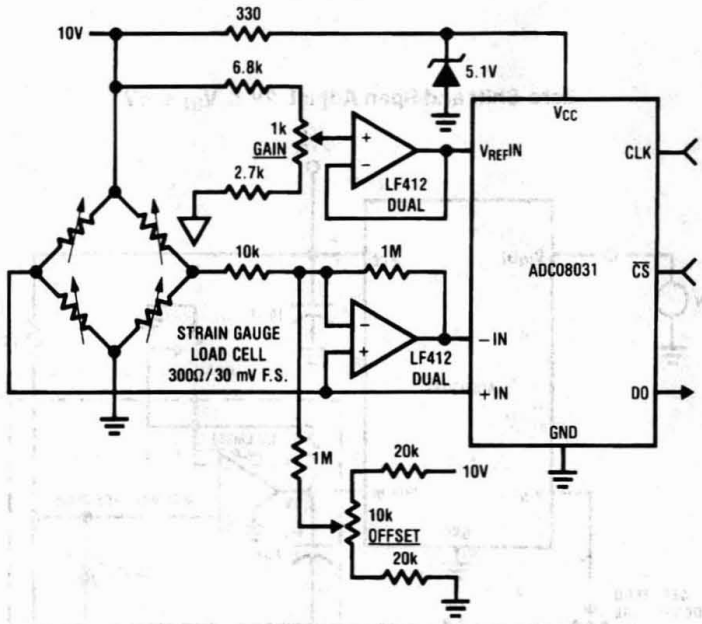
Digital Load Cell



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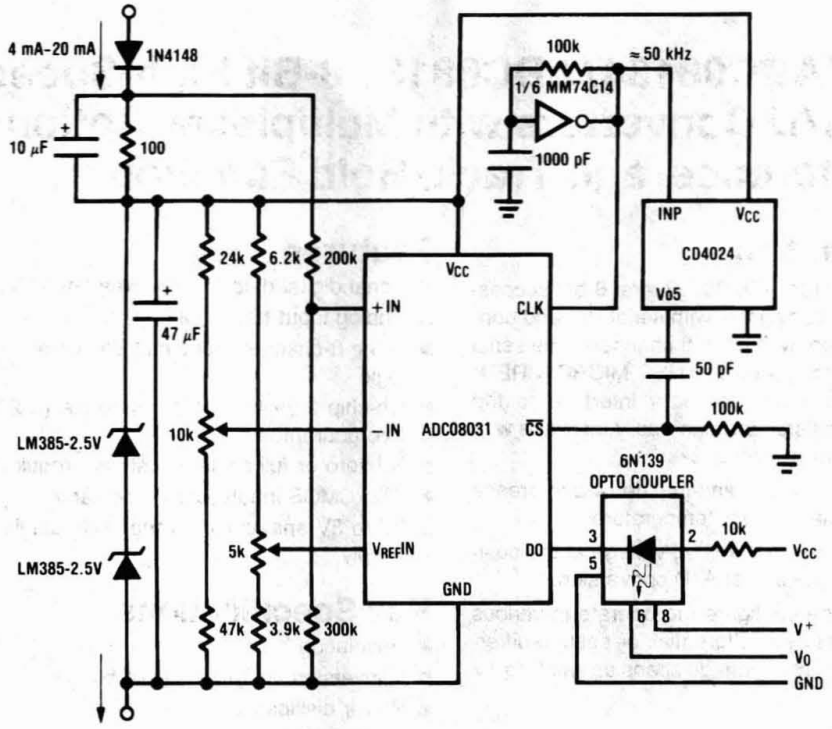
- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

Applications (Continued)

4 mA–20 mA Current Loop Converter



- All power supplied by loop
- 1500V isolation at output

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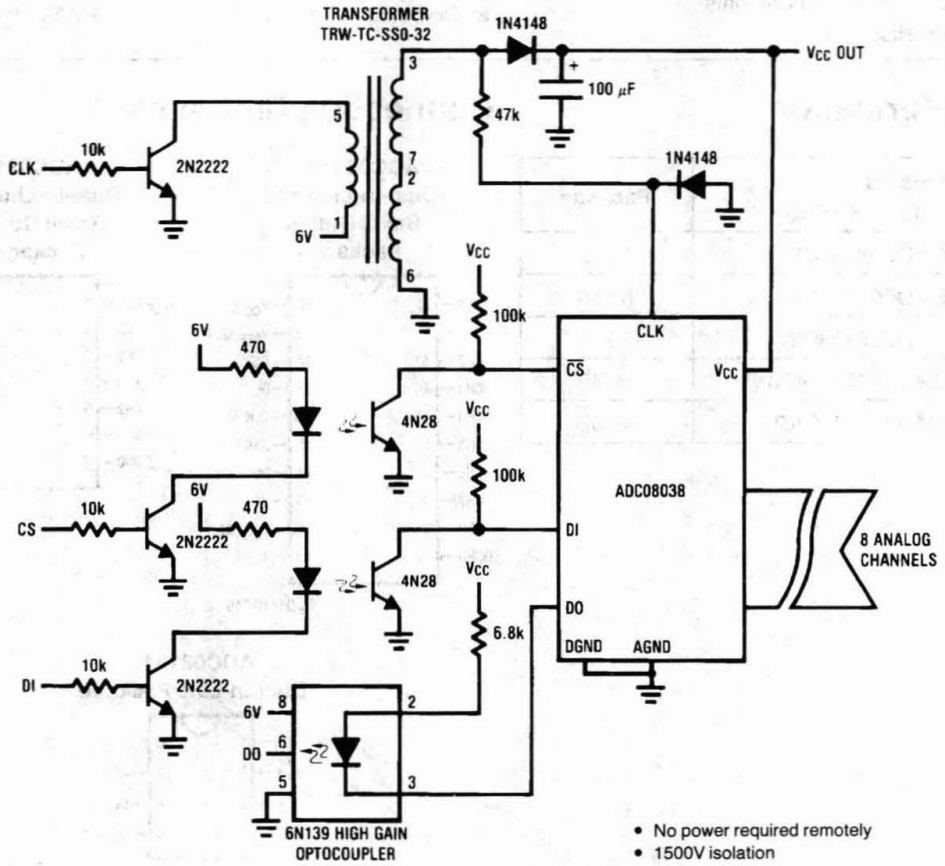
Isolated Data Converter



- No power required remotely
- 1500V isolation

TL/H/10555–29

National Semiconductor

ADC08131/ADC08134/ADC08138 8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

General Description

The ADC08131/ADC08134/ADC08138 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

All three devices provide a 2.5V band-gap derived reference with guaranteed performance over temperature.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Applications

- Digitizing automotive sensors
- Process control/monitoring
- Remote sensing in noisy environments
- Embedded diagnostics

Features

- Serial digital data link requires few I/O pins
- Analog input track/hold function
- 4- or 8-channel input multiplexer options with address logic
- On-chip 2.5V band-gap reference (±2% over temperature guaranteed)
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- 0V to 5V analog input range with single 5V power supply

Key Specifications

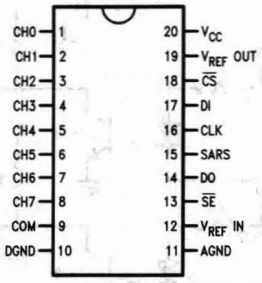
■ Resolution	8 Bits
■ Conversion time (f_C = 1 MHz)	8 μs (Max)
■ Power dissipation	20 mW (Max)
■ Single supply	5 V_{DC} (±5%)
■ Total unadjusted error	±½ LSB and ±1 LSB
■ Linearity Error (V_{REF} = 2.5V)	±½ LSB
■ No missing codes (over temperature)	
■ On-board Reference	+2.5V ±1.5% (Max)

Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC08131BIN, ADC08131CIN	N08E
ADC08134BIN, ADC08134CIN	N14A
ADC08138BIN, ADC08138CIN	N20A
ADC08134BIWM, ADC08134CIWM	M14B
ADC08138BIWM, ADC08138CIWM	M20B

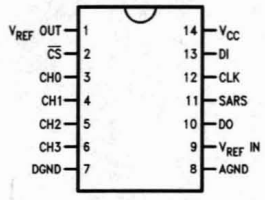
Connection Diagrams

ADC08138 Dual-In-Line and Small Outline Packages



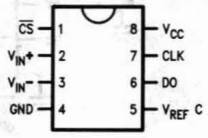
TL/H/10749-2

ADC08134 Dual-In-Line and Small Outline Packages



TL/H/10749-3

ADC08131 Dual-In-Line Package



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Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Power Dissipation at T_A = 25°C (Note 5)	800 mW
ESD Susceptibility (Note 6)	1500V
Soldering Information	
N Package (10 sec.)	260°C
SO Package:	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08131BIN, ADC08131CIN, ADC08134BIN, ADC08134CIN, ADC08138BIN, ADC08138CIN, ADC08134BIWM, ADC08138BIWM, ADC08134CIWM, ADC08138CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage (V_{CC})	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	ADC08131, ADC08134 and ADC08138 with BIN, CIN, BIWM or CIWM Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
	Linearity Error	V_{REF} = +2.5 V_{DC}			
	BIN, BIWM			**±½**	LSB (max)
	CIN, CIWM			**±1**	LSB (max)
	Full Scale Error	V_{REF} = +2.5 V_{DC}			
	BIN, BIWM			**±½**	LSB (max)
	CIN, CIWM			**±1**	LSB (max)
	Zero Error	V_{REF} = +2.5 V_{DC}			
	BIN, BIWM			**±1**	LSB (max)
	CIN, CIWM			**±1**	LSB (max)
	Total Unadjusted Error	V_{REF} = +5 V_{DC}			
	BIN, BIWM	(Note 10)		**±½**	LSB (max)
	CIN, CIWM			**±1**	LSB (max)
	Differential Linearity	V_{REF} = +2.5 V_{DC}		**8**	Bits (min)
R_{REF}	Reference Input Resistance	(Note 11)	3.5		kΩ
				1.3	kΩ (min)
				6.0	kΩ (max)
V_{IN}	Analog Input Voltage	(Note 12)		**(V_{CC} + 0.05)**	V (max)
				(GND − 0.05)	V (min)

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	ADC08131, ADC08134 and ADC08138 with BIN, CIN, BIWM or CIWM Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
	DC Common-Mode Error	V_{REF} = 2.5 V_{DC}		±½	LSB (max)
	Power Supply Sensitivity	V_{CC} = +5V ±5%, V_{REF} = +2.5 V_{DC}		±¼	LSB (max)
	On Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		0.2 **1**	μA (max)
		On Channel = 0V, Off Channel = 5V		−0.2 **−1**	μA (max)
	Off Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**	μA (max)
		On Channel = 0V, Off Channel = 5V		0.2 **1**	μA (max)
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.25V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.0V		**1**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V		**−1**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V: I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.5**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	V_{OUT} = 0V V_{OUT} = 5V		**−3.0** **3.0**	μA (max) μA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V		**−6.5**	mA (min)
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}		**8.0**	mA (min)
I_{CC}	Supply Current ADC08134, ADC08138 ADC08131 (Note 16)	$\overline{CS}$ = HIGH		 **3.0** **6.0**	 mA (max) mA (max)

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = +5\ V_{DC}$ and $f_{CLK} = 1$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08131, ADC08134 and ADC08138 with BIN, CIN, BIWM or CIWM Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
REFERENCE CHARACTERISTICS					
$V_{REF}OUT$	Output Voltage	ADC08134, ADC08138	**2.5 ±2%**	2.5 ±1.5%	V
		ADC08131	**2.5 ±2%**	2.5 ±1.5%	
$\Delta V_{REF}/\Delta T$	Temperature Coefficient		40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation (Note 17)	Sourcing ($0 \le I_L \le +4$ mA) ADC08134, ADC08138	0.003	**0.1**	%/mA (max)
		Sourcing ($0 \le I_L \le +2$ mA) ADC08131	0.003	**0.1**	
		Sinking ($-1 \le I_L \le 0$ mA) ADC08134, ADC08138	0.2	**0.5**	
		Sinking ($-1 \le I_L \le 0$ mA) ADC08131	0.2	**0.5**	
	Line Regulation	$4.75V \le V_{CC} \le 5.25V$	0.5	**6**	mV (max)
I_{SC}	Short Circuit Current	$V_{REF} = 0V$ ADC08134, ADC08138	8	**25**	mA (max)
		$V_{REF} = 0V$ ADC08131	8	**25**	
T_{SU}	Start-Up Time	V_{CC}: 0V → 5V, $C_L = 100\ \mu F$	20		ms
$\Delta V_{REF}/\Delta t$	Long Term Stability		200		ppm/1 kHr

2

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK}	Clock Frequency		10	 **1**	kHz (min) MHz (max)
	Clock Duty Cycle (Note 14)			**40** **60**	% (min) % (max)
T_C	Conversion Time (Not Including MUX Addressing Time)	f_{CLK} = 1 MHz		**8** **8**	$1/f_{CLK}$ (max) μs (max)
t_{CA}	Acquisition Time			**½**	$1/f_{CLK}$(max)
t_{SELECT}	CLK High while $\overline{CS}$ is High		50		ns
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			**25**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 15)	C_L = 100 pF: Data MSB First Data LSB First		 **250** **200**	 ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	C_L = 10 pF, R_L = 10 kΩ (see TRI-STATE Test Circuits)	50		ns
		C_L = 100 pF, R_L = 2 kΩ		**180**	ns (max)
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to AGND = DGND = 0 V_{DC}, unless otherwise specified.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < (AGND or DGND) or V_{IN} > AV_{CC},) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For devices with suffixes BIN, CIN, BIJ, CIJ, BIWM, and CIWM T_{JMAX} = 125°C. For devices with suffix CMJ, T_{JMAX} = 150°C. The typical thermal resistances (θ_{JA}) of these parts when board mounted follow: ADC08131 with BIN and CIN suffixes 120°C/W, ADC08134 with BIN and CIN suffixes 95°C/W, ADC08138 with BIN and CIN suffixes 80°C/W. ADC08134 with BIWM and CIWM suffixes 140°C/W, ADC08138 with BIWM and CIWM suffixes 91°C/W,

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or *Linear Data Book* section "Surface Mount" for other methods of soldering surface mount devices.

Note 8: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 9: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Total unadjusted error includes zero, full-scale, linearity, and multiplexer error. Total unadjusted error with V_{REF} = +5V only applies to the ADC08134 and ADC08138. See Note 16.

Note 11: Cannot be tested for the ADC08131.

Note 12: For $V_{IN(-)} \geq V_{IN(+)}$ the digital code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. During testing at low V_{CC} levels (e.g., 4.5V), high level analog inputs (e.g., 5V) can cause an input diode to conduct, especially at elevated temperatures. This will cause errors for analog inputs near full-scale. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 13: Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining seven off channels tied low (0 V_{DC}), total current flow through the off channels is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channels is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.

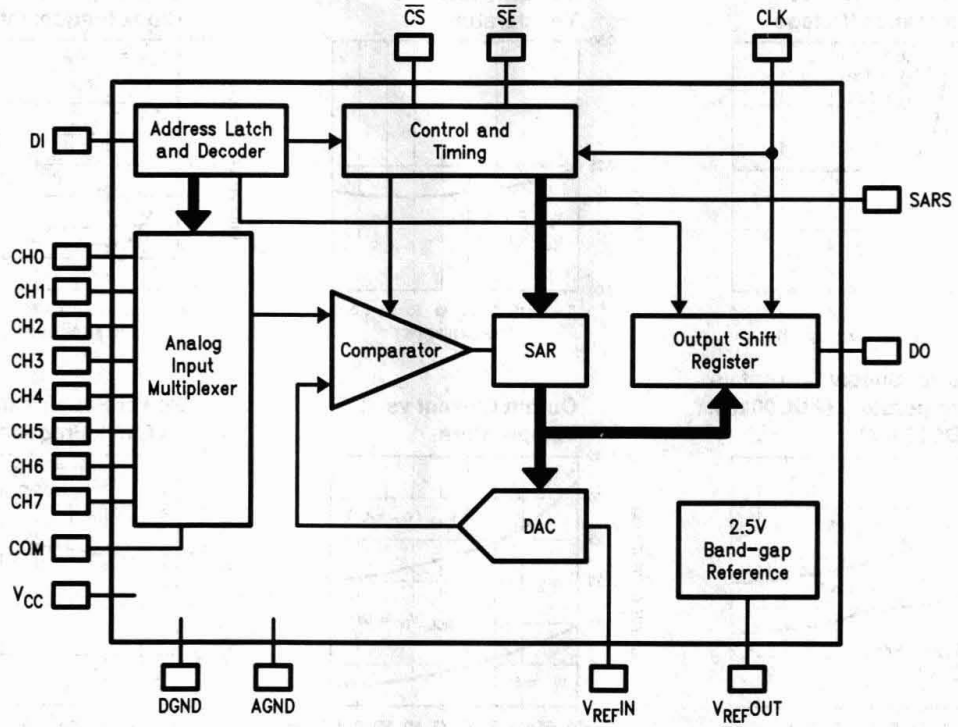
Note 14: A 40% to 60% duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits the minimum time the clock is high or low must be at least 450 ns. The maximum time the clock can be high or low is 100 μs.

Note 15: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Note 16: For the ADC08131 V_{REF}IN is internally tied to the on chip 2.5V band-gap reference output; therefore, the supply current is larger because it includes the reference current (700 μA typical, 2 mA maximum).

Note 17: Load regulation test conditions and specifications for the ADC08131 differ from those of the ADC08134 and ADC08138 because the ADC08131 has the on-board reference as a permanent load.

ADC08138 Simplified Block Diagram



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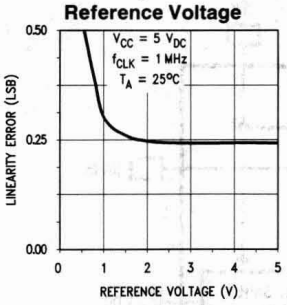
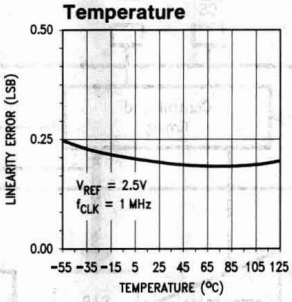
Typical Converter Performance Characteristics

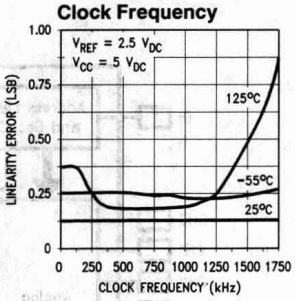
Linearity Error vs Reference Voltage



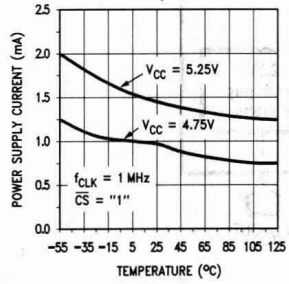
Linearity Error vs Temperature



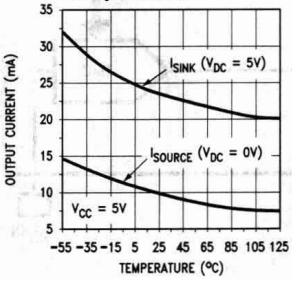
Linearity Error vs Clock Frequency



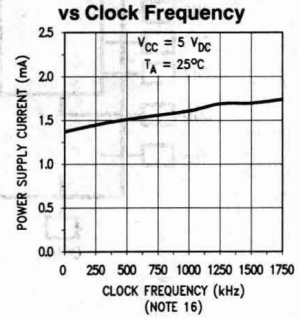
Power Supply Current vs Temperature (ADC08138, ADC08134)



Output Current vs Temperature



Power Supply Current vs Clock Frequency



Note: For ADC08131 add I_{REF} (Note 16)

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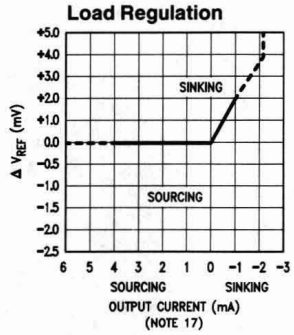
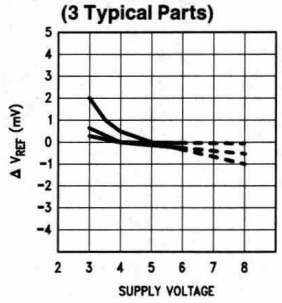
Typical Reference Performance Characteristics

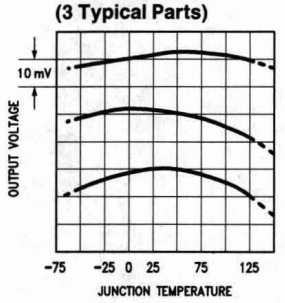
Load Regulation



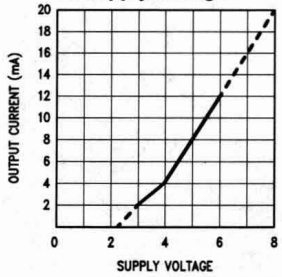
Line Regulation (3 Typical Parts)



Output Drift vs Temperature (3 Typical Parts)



Available Output Current vs Supply Voltage



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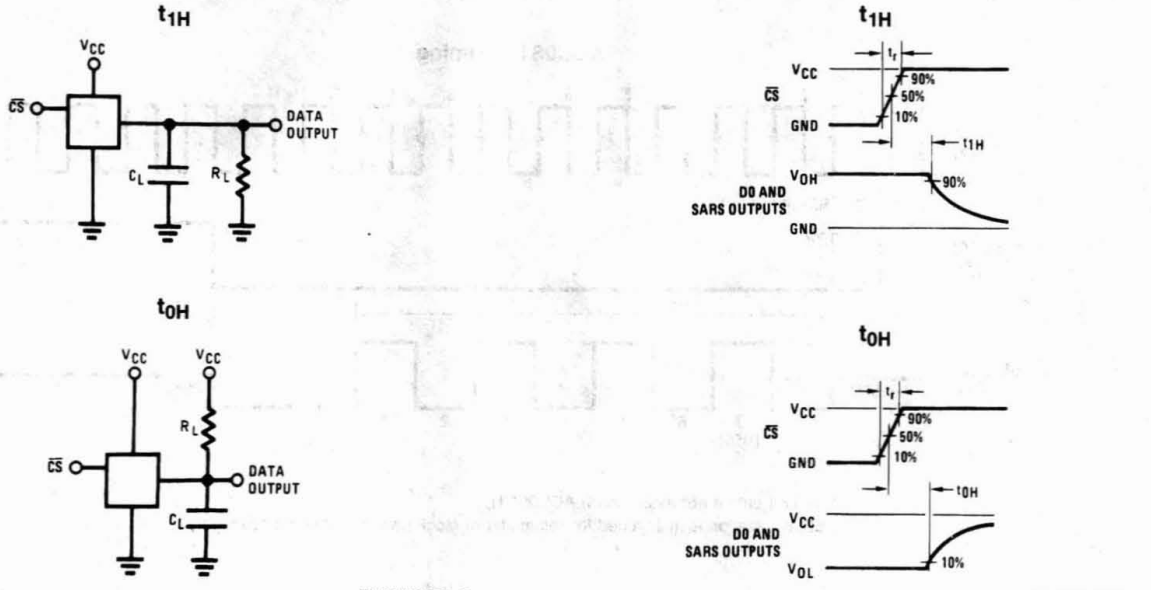
TRI-STATE Test Circuits and Waveforms



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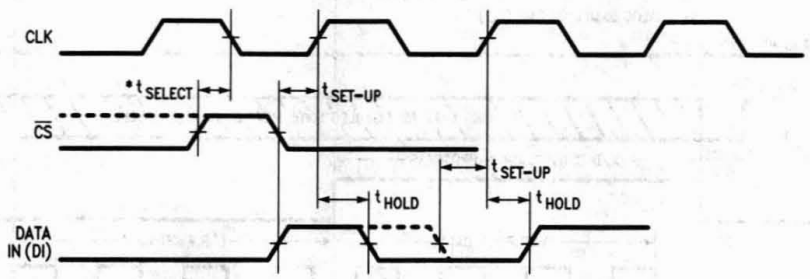
Timing Diagrams

Data Input Timing



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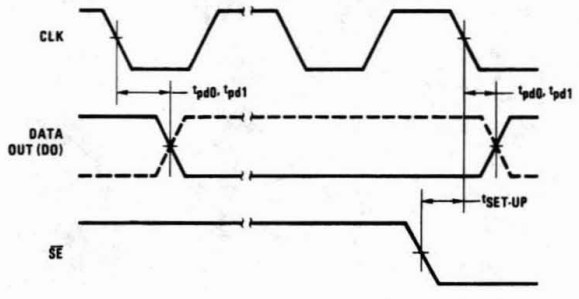
*To reset these devices, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. Otherwise these devices are compatible with industry standards ADC0831/4/8.

Data Output Timing



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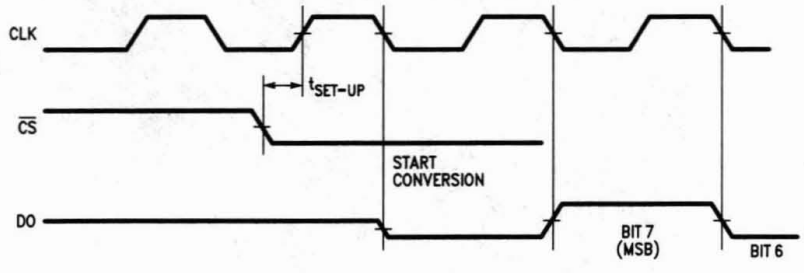
ADC08131 Start Conversion Timing



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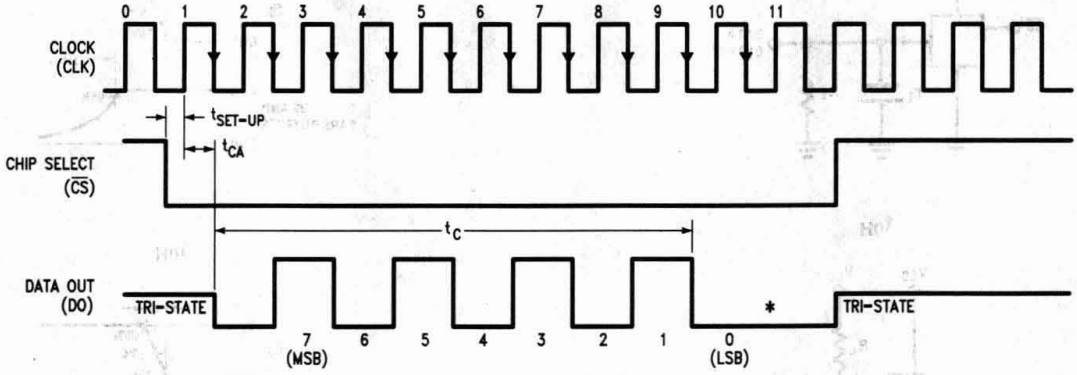
2

Timing Diagrams (Continued)

ADC08131 Timing



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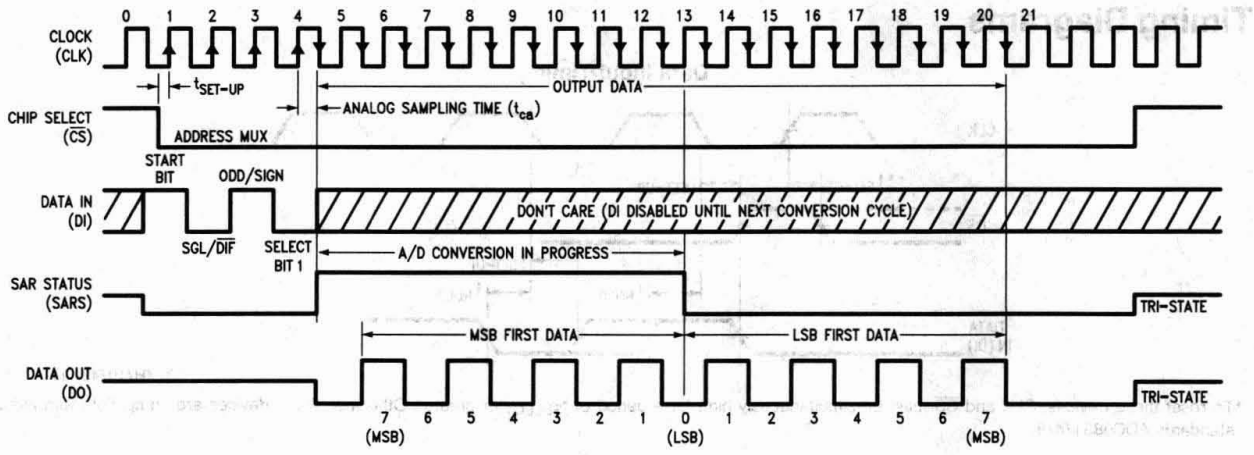
*LSB first output not available on ADC08131.
LSB information is maintained for remainder of clock periods until $\overline{CS}$ goes high.

ADC08134 Timing



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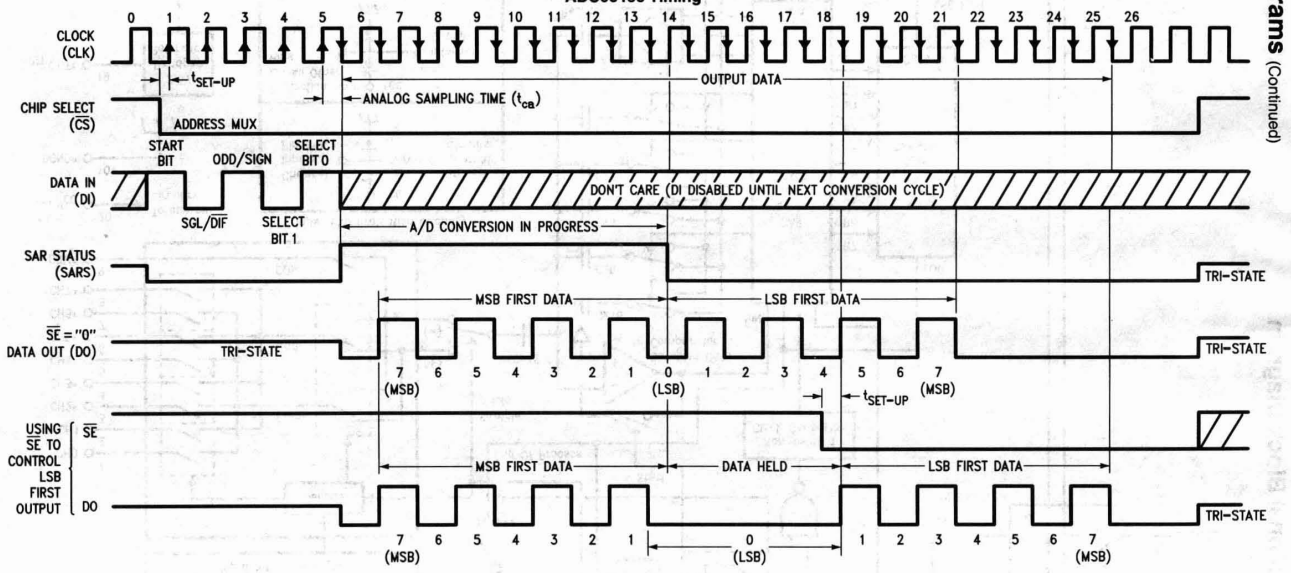
Timing Diagrams (Continued)

ADC08138 Timing



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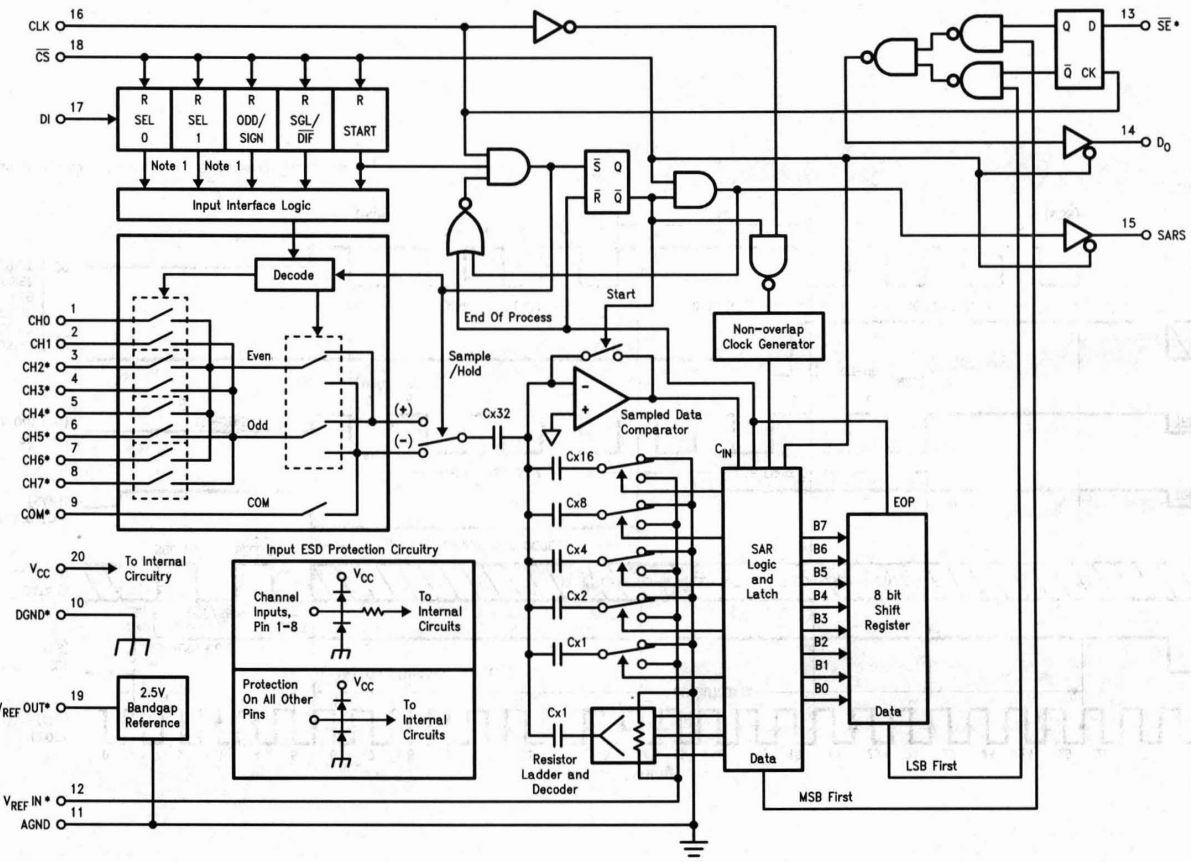
*Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC08138 Functional Block Diagram



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*Some of these functions/pins are not available with other options.

Note 1: For the ADC08134, the "SEL 1" Flip-Flop is bypassed. For the ADC08131, V_{REFOUT} and V_{REFIN} are internally tied together.

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive-approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential (which will convert the difference between the voltage at any analog input and a common terminal) operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC08131 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line (COM) on the ADC08138 can be used as a pseudo-differential input. In this mode the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply applications where the analog circuity may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC08131	1	1	8
ADC08134	4	2	14
ADC08138	8	4	20

TABLE II. MUX Addressing: ADC08138

Single-Ended MUX Mode

MUX Address					Analog Single-Ended Channel #								
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	1	0	0	0	+								−
1	1	0	0	1			+						−
1	1	0	1	0					+				−
1	1	0	1	1							+		−
1	1	1	0	0		+							−
1	1	1	0	1				+					−
1	1	1	1	0						+			−
1	1	1	1	1								+	−

Functional Description (Continued)

TABLE II. MUX Addressing: ADC08138 (Continued)

Differential MUX Mode

MUX Address					Analog Differential Channel-Pair #							
START	SGL/$\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0		1		2		3	
			1	0	0	1	2	3	4	5	6	7
1	0	0	0	0	+	−						
1	0	0	0	1			+	−				
1	0	0	1	0					+	−		
1	0	0	1	1							+	−
1	0	1	0	0	−	+						
1	0	1	0	1			−	+				
1	0	1	1	0					−	+		
1	0	1	1	1							−	+

TABLE III. MUX Addressing: ADC08134

Single-Ended MUX Mode

MUX Address				Channel #			
START	SGL/$\overline{\text{DIF}}$	ODD/ SIGN	SELECT	0	1	2	3
			1				
1	1	0	0	+			
1	1	0	1			+	
1	1	1	0		+		
1	1	1	1				+

COM is internally tied to AGND

Differential MUX Mode

MUX Address				Channel #			
START	SGL/$\overline{\text{DIF}}$	ODD/ SIGN	SELECT	0	1	2	3
			1				
1	0	0	0	+	−		
1	0	0	1			+	−
1	0	1	0	−	+		
1	0	1	1			−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified as required before each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50mV below ground to 50mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows many functions to be included in a small package and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate timing diagram is shown for each device.

1. A conversion is initiated by pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.
2. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.

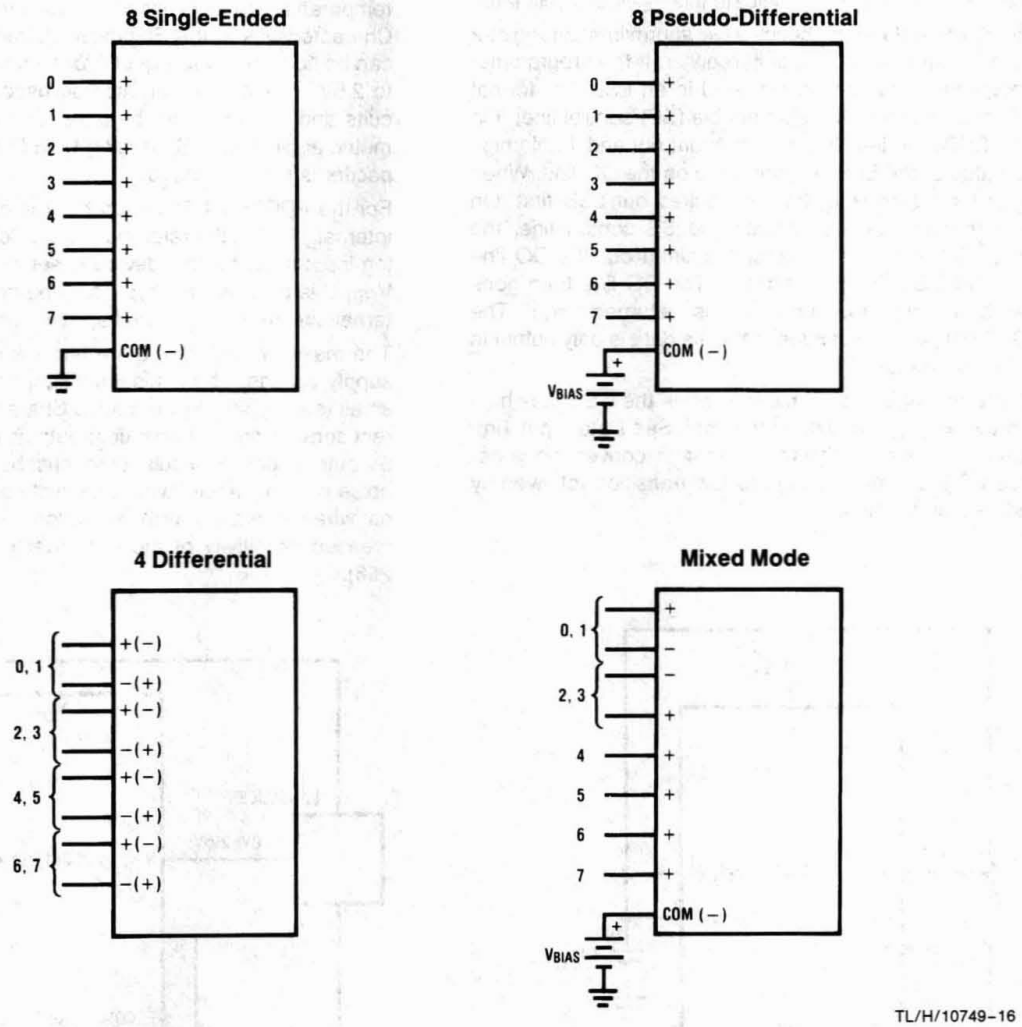

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FIGURE 1. Analog Input Multiplexer Options for the ADC08138

Functional Description (Continued)

3. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period is automatically inserted to allow for sampling the analog input. The SARS line goes high at the end of this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).
4. The data out (DO) line now comes out of TRI-STATE and provides a leading zero.
5. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison the comparator's output is shipped to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
6. After 8 clock periods the conversion is completed. The SARS line returns low to indicate this ½ clock cycle later.
7. The stored data in the successive approximation register is loaded into an internal shift register. If the programmer prefers the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. On the ADC08138 the $\overline{SE}$ line is brought out and if held high the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low the data is clocked out LSB first. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. The ADC08131 is an exception in that its data is only output in MSB first format.
8. All internal registers are cleared when the $\overline{CS}$ line is high and the t_{SELECT} requirement is met. See Data Input Timing under Timing Diagrams. If another conversion is desired $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

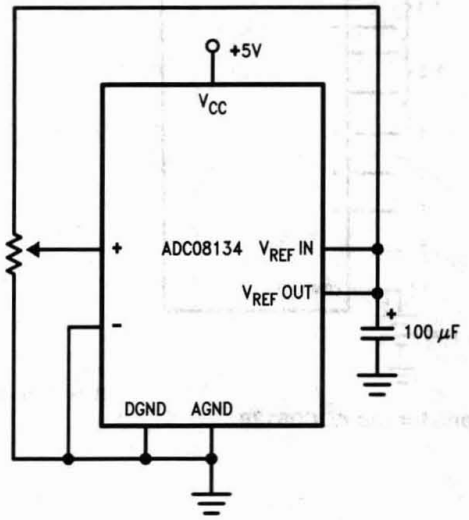
3.0 REFERENCE CONSIDERATIONS

The V_{REF}IN pin on these converters is the top of a resistor divider string and capacitor array used for the successive approximation conversion. The voltage applied to this reference input defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$ over which the 256 possible output codes apply). The reference source must be capable of driving the reference input resistance, which can be as low as 1.3 kΩ.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference input must be biased with a stable voltage source. The ADC08134 and the ADC08138 provide the output of a 2.5V band-gap reference at V_{REF}OUT. This voltage does not vary appreciably with temperature, supply voltage, or load current (see Reference Characteristics in the Electrical Characteristics tables) and can be tied directly to V_{REF}IN for an analog input span of 0V to 2.5V. This output can also be used to bias external circuits and can therefore be used as the reference in ratiometric applications. Bypassing V_{REF}OUT with a 100 μF capacitor is recommended.

For the ADC08131, the output of the on-board reference is internally tied to the reference input. Consequently, the analog input span for this device is set at 0V to 2.5V. The pin V_{REF}C is provided for bypassing purposes and biasing external circuits as suggested above.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/256).



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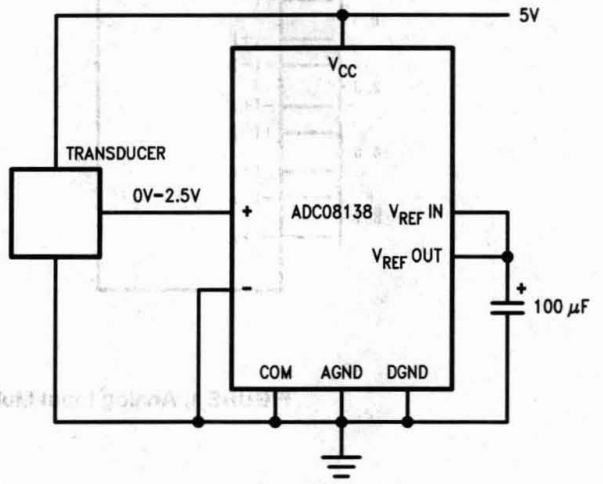
a) Ratiometric



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b) Absolute

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60Hz common-mode signal to generate a ¼ LSB error ($\approx$5mV) with the converter running at 250kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. While operating near or at maximum speed bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1μA over temperature will create a 1mV input error with a 1kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for $V_{REF} = 5.000V_{DC}$).

5.2 Full Scale

A full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF}IN input for a digital output code which is just changing from 1111 1110 to 1111 1111 (See figure entitled "Span Adjust; 0V ≤ V_{IN} ≤ 3V"). This is possible only with the ADC08134 and ADC08138. (The reference is internally connected to V_{REF}IN of the ADC08131).

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+)\,fs\,adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

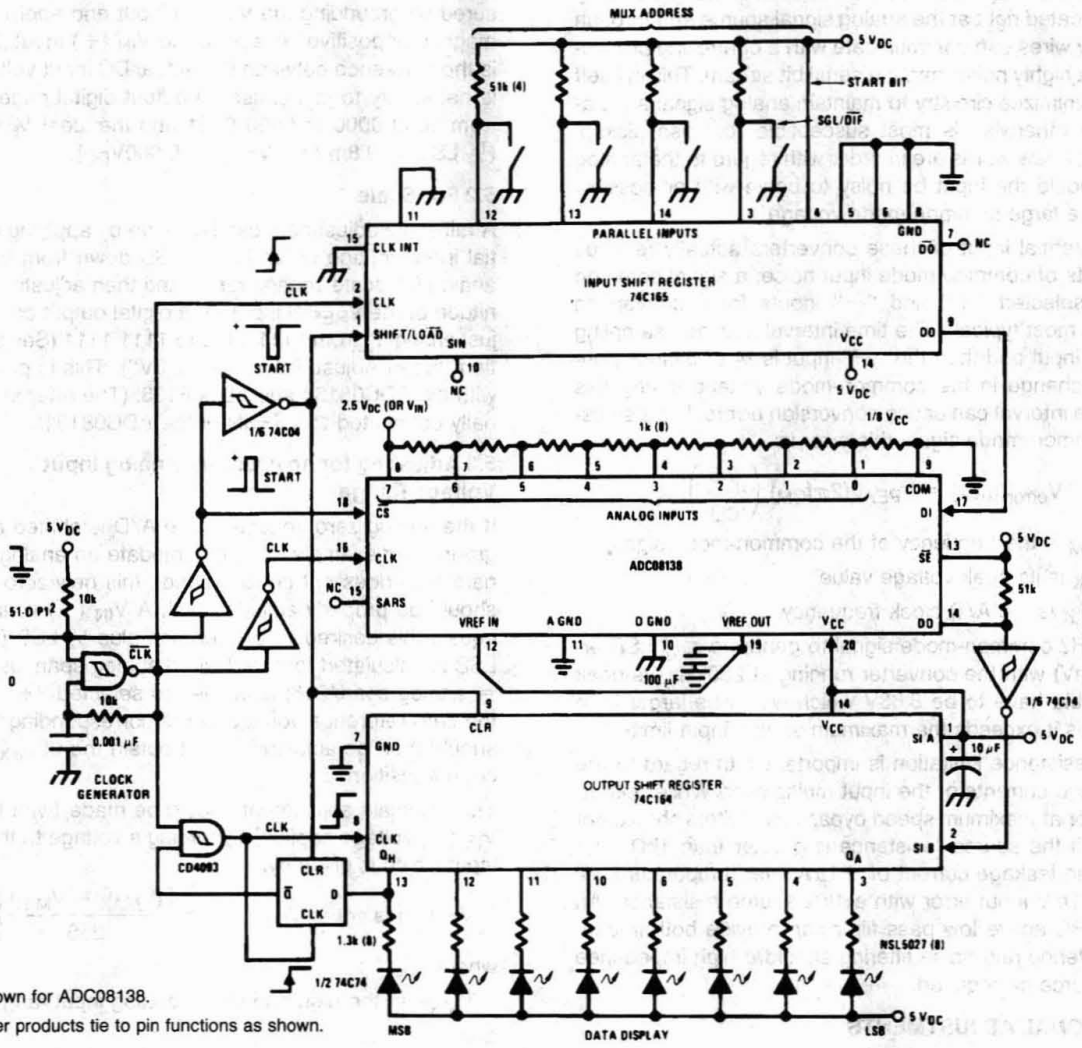
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF}IN (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

Applications

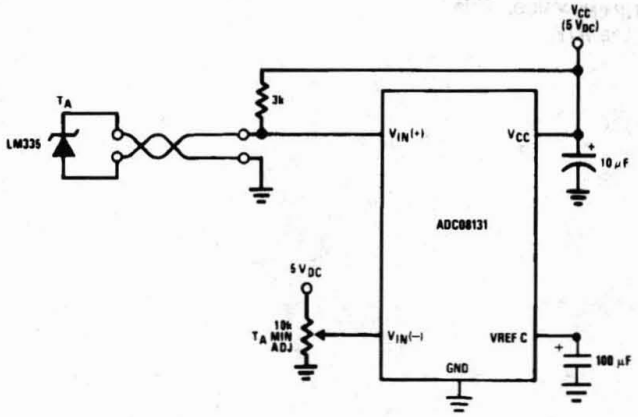
A "Stand-Alone" Hook-Up for ADC08138 Evaluation



*Pinouts shown for ADC08138.

For all other products tie to pin functions as shown.

Low-Cost Remote Temperature Sensor



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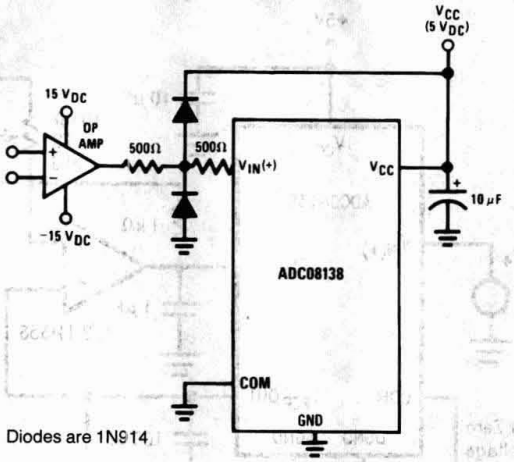
Applications (Continued)

Protecting the Input



Diodes are 1N914

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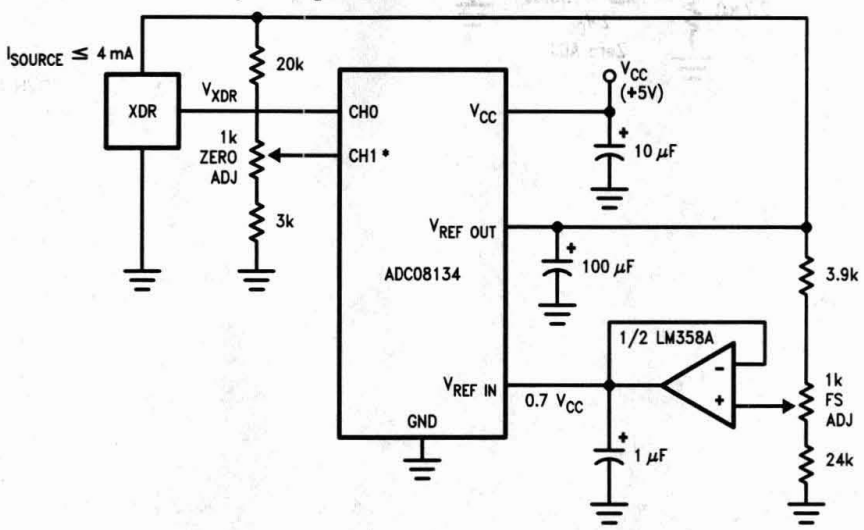
Operating with Ratiometric Transducers



*$V_{IN(-)} = 0.15\ V_{REF}$
15% of $V_{REF} \leq V_{XDR} \leq$ 85% of V_{REF}

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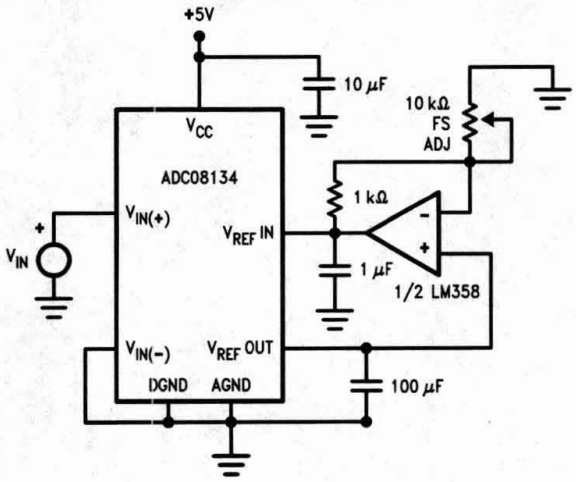
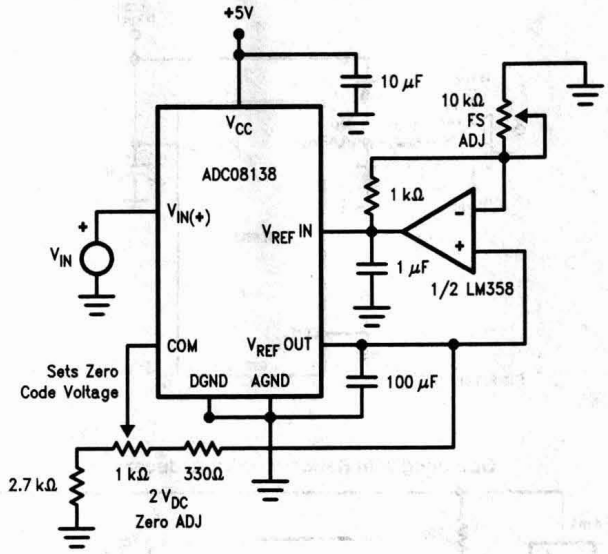
Span Adjust; 0V ≤ V_{IN} ≤ 3V



TL/H/10749–24

Applications (Continued)

Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



TL/H/10749–25

National Semiconductor

ADC08231/ADC08234/ADC08238 8-Bit 2 μs Serial I/O A/D Converters with MUX, Reference, and Track/Hold

General Description

The ADC08231/ADC08234/ADC08238 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

Designed for high-speed/low-power applications, the devices are capable of a fast 2 μs conversion when used with a 4 MHz clock.

All three devices provide a 2.5V band-gap derived reference with guaranteed performance over temperature.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Applications

- High-speed data acquisition
- Digitizing automotive sensors
- Process control/monitoring
- Remote sensing in noisy environments
- Disk drives
- Portable instrumentation
- Test systems

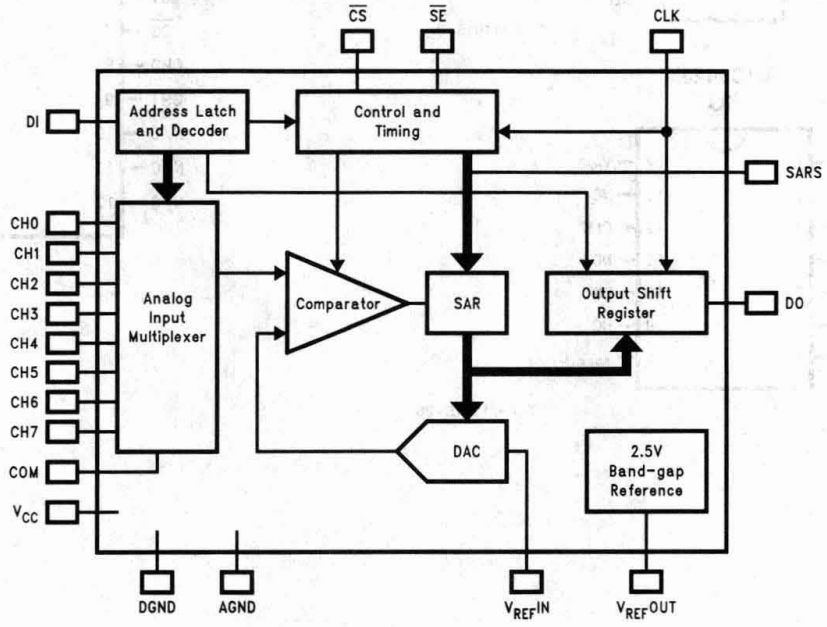
Features

- Serial digital data link requires few I/O pins
- Analog input track/hold function
- 4- or 8-channel input multiplexer options with address logic
- On-chip 2.5V band-gap reference (±2% over temperature guaranteed)
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- 0V to 5V analog input range with single 5V power supply
- Pin compatible with Industry-Standards ADC0831/4/8

Key Specifications

■ Resolution	8 Bits
■ Conversion time (f_C = 4 MHz)	2 μs (Max)
■ Power dissipation	20 mW (Max)
■ Single supply	5 V_{DC} (±5%)
■ Total unadjusted error	±½ LSB and ±1 LSB
■ Linearity Error (V_{REF} = 2.5V)	±½ LSB
■ No missing codes (over temperature)	
■ On-board Reference	+2.5V ±1.5% (Max)

ADC08238 Simplified Block Diagram



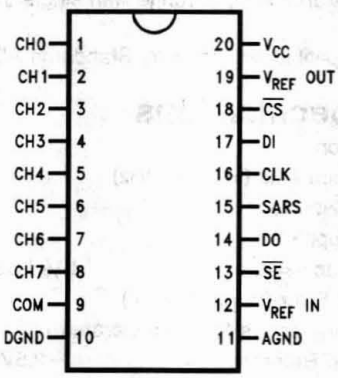
TL/H/11015–4

Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC08231BIN, ADC08231CIN	N08E, DIP
ADC08234BIN, ADC08234CIN	N14A, DIP
ADC08234CIMF	MTB24, TSSOP
ADC08238BIN, ADC08238CIN	N20A, DIP
ADC08231BIWM, ADC08231CIWM	M14B, SO
ADC08234BIWM, ADC08234CIWM	M14B, SO
ADC08238BIWM, ADC08238CIWM	M20B, SO

Connection Diagrams

ADC08238
SO and DIP



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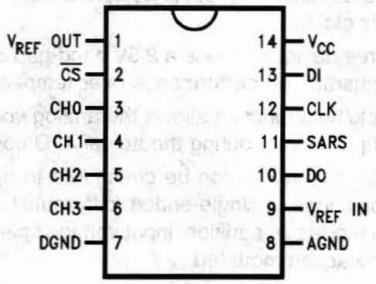
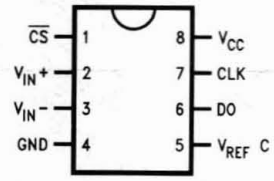
ADC08234
SO and DIP



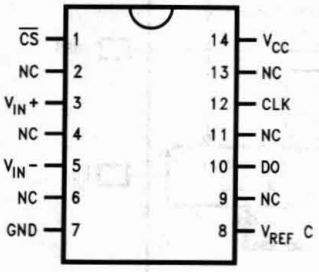
TL/H/11015–2

ADC08231
DIP



TL/H/11015–3

ADC08231
SO



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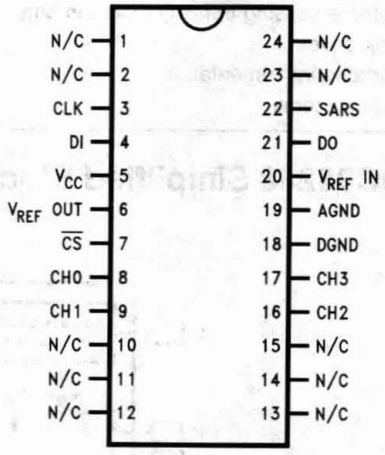
ADC08234
TSSOP



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Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Power Dissipation at T_A = 25°C (Note 5)	800 mW
ESD Susceptibility (Note 6)	1500V
Soldering Information	
N Package (10 sec.)	260°C
TSSOP and SO Package (Note 7):	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08231BIN, ADC08231CIN, ADC08234BIN, ADC08234CIN, ADC08238BIN, ADC08238CIN, ADC08231BIWM, ADC08231CIWM, ADC08234BIWM, ADC08238BIWM, ADC08234CIWM, ADC08238CIWM, ADC08234CIMF	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_{CC})	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and f_{CLK} = 4 MHz, R_{Source} = 50Ω unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	ADC08231, ADC08234 and ADC08238 with BIN, CIN, BIWM, CIWM, or CIMF Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
	Linearity Error	V_{REF} = +2.5 V_{DC}			
	BIN, BIWM			**±½**	LSB (max)
	CIN, CIMF, CIWM			**±1**	LSB (max)
	Gain Error	V_{REF} = +2.5 V_{DC}			
	BIN, BIWM			**±1**	LSB (max)
	CIN, CIMF, CIWM			**±1**	LSB (max)
	Zero Error	V_{REF} = +2.5 V_{DC}			
	BIN, BIWM			**±1**	LSB (max)
	CIN, CIMF, CIWM			**±1**	LSB (max)
	Total Unadjusted Error	V_{REF} = +5 V_{DC}			
	BIN, BIWM	(Note 10)		**±1**	LSB (max)
	CIN, CIMF, CIWM			**±1**	LSB (max)
	Differential Linearity	V_{REF} = +2.5 V_{DC}		**8**	Bits (min)
R_{REF}	Reference Input Resistance	(Note 11)	3.5		kΩ
				1.3	kΩ (min)
				6.0	kΩ (max)
V_{IN}	Analog Input Voltage	(Note 12)		**(V_{CC} + 0.05)**	V (max)
				(GND − 0.05)	V (min)

2

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = +5\ V_{DC}$, $V_{REF} = +2.5\ V_{DC}$ and $f_{CLK} = 4$ MHz, $R_{source} = 50\Omega$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08231, ADC08234 and ADC08238 with BIN, CIN, BIWM, CIWM, or CIMF Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
	DC Common-Mode Error	$V_{REF} = +2.5\ V_{DC}$		±½	LSB (max)
	Power Supply Sensitivity	$V_{CC} = +5V \pm 5\%$, $V_{REF} = +2.5\ V_{DC}$		±¼	LSB (max)
	On Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		0.2 **1**	μA (max)
		On Channel = 0V, Off Channel = 5V		−0.2 **−1**	μA (max)
	Off Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**	μA (max)
		On Channel = 0V, Off Channel = 5V		0.2 **1**	μA (max)
DYNAMIC CHARACTERISTICS (see Typical Converter Performance Characteristics)					
$\frac{S}{N+D}$	Signal-to-(Noise + Distortion) Ratio	$V_{REF} = +5V$, Sample Rate = 286 kHz, $V_{IN} = +5\ V_{p-p}$			
		$f_{IN} = 10$ kHz	48.35		dB
		$f_{IN} = 50$ kHz	48.00		dB
		$f_{IN} = 100$ kHz	47.40		dB
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.25V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5.0V$		**1**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$		**−1**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$		**−3.0** **3.0**	μA (max) μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		**−6.5**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		**8.0**	mA (min)
I_{CC}	Supply Current ADC08234, ADC08238 ADC08231 (Note 16)	$\overline{CS}$ = HIGH		 **3.0** **6.0**	 mA (max) mA (max)

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5 V_{DC} and f_{CLK} = 4 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	ADC08231, ADC08234 and ADC08238 with BIN, CIN, BIWM, CIWM, or CIMF Suffixes		Units (Limits)
			Typical (Note 8)	Limits (Note 9)	
REFERENCE CHARACTERISTICS					
$V_{REF}OUT$	Output Voltage	BIN, BIJ, BIWM	**2.5 ±2%**	2.5 ±1.5%	V
		CIN, CIJ, CIWM, CMJ	**2.5 ±3.5%**	2.5 ±3.0%	
$\Delta V_{REF}/\Delta T$	Temperature Coefficient		40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation (Note 17)	Sourcing ($0 \le I_L \le +4$ mA) ADC08234, ADC08238	0.003	**0.1**	%/mA (max)
		Sourcing ($0 \le I_L \le +2$ mA) ADC08231	0.003	**0.1**	
		Sinking ($-1 \le I_L \le 0$ mA) ADC08234, ADC08238	0.2	**0.5**	
		Sinking ($-1 \le I_L \le 0$ mA) ADC08231	0.2	**0.5**	
	Line Regulation	$4.75V \le V_{CC} \le 5.25V$	0.5	**6**	mV (max)
I_{SC}	Short Circuit Current	V_{REF} = 0V ADC08234, ADC08238	8	**25**	mA (max)
		V_{REF} = 0V ADC08231	8	**25**	
T_{SU}	Start-Up Time	V_{CC}: 0V → 5V C_L = 100 μF	20		ms
$\Delta V_{REF}/\Delta t$	Long Term Stability		200		ppm/1 kHr

2

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5 V_{DC}, V_{REF} = +2.5 V_{DC} and t_r = t_f = 20 ns unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK}	Clock Frequency		10	**4**	kHz (min) MHz (max)
	Clock Duty Cycle (Note 14)			**40** **60**	% (min) % (max)
T_C	Conversion Time (Not Including MUX Addressing Time)	f_{CLK} = 4 MHz		**8** **2**	$1/f_{CLK}$ (max) μs (max)
t_{CA}	Acquisition Time			**1½**	$1/f_{CLK}$(max)
t_{SELECT}	CLK High while $\overline{CS}$ is High		50		ns
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			**25**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 15)	C_L = 100 pF: Data MSB First Data LSB First		 **250** **200**	 ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	C_L = 10 pF, R_L = 10 kΩ (see TRI-STATE Test Circuits)	50		ns
		C_L = 100 pF, R_L = 2 kΩ		**180**	ns (max)
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to AGND = DGND = 0 V_{DC}, unless otherwise specified.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < (AGND or DGND) or V_{IN} > AV_{CC},) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J_{MAX}}$, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{J_{MAX}} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For devices with suffixes BIN, CIN, BIJ, CIJ, BIWM, and CIWM $T_{J_{MAX}}$ = 125°C. For devices with suffix CMJ, $T_{J_{MAX}}$ = 150°C. The typical thermal resistances (θ_{JA}) of these parts when board mounted follow: ADC08231 with BIN and CIN suffixes 120°C/W, ADC08234 with BIN and CIN suffixes 95°C/W, ADC08234 with CIMF suffix 167°C/W, ADC08238 with BIN and CIN suffixes 80°C/W. ADC08231 with BIWM and CIWM suffixes 140°C/W, ADC08234 with BIWM and CIWM suffixes 140°C/W, ADC08238 with BIWM and CIWM suffixes 91°C/W,

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or *Linear Data Book* section "Surface Mount" for other methods of soldering surface mount devices.

Note 8: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 9: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Total unadjusted error includes zero, full-scale, linearity, and multiplexer error. Total unadjusted error with V_{REF} = +5V only applies to the ADC08234 and ADC08238. See Note 16.

Note 11: Cannot be tested for the ADC08231.

Note 12: For $V_{IN(-)} \geq V_{IN(+)}$ the digital code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. During testing at low V_{CC} levels (e.g., 4.5V), high level analog inputs (e.g., 5V) can cause an input diode to conduct, especially at elevated temperatures. This will cause errors for analog inputs near full-scale. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 13: Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining off channels tied low (0 V_{DC}), total current flow through the off channels is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channels is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.

Note 14: A 40% to 60% duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits the minimum time the clock is high or low must be at least 120 ns. The maximum time the clock can be high or low is 100 μs.

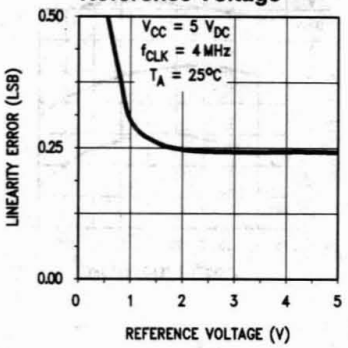
Note 15: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Note 16: For the ADC08231 V_{REF}IN is internally tied to the on chip 2.5V band-gap reference output; therefore, the supply current is larger because it includes the reference current (700 μA typical, 2 mA maximum).

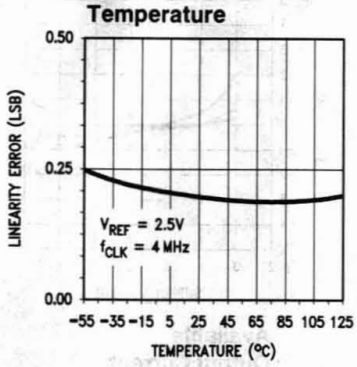
Note 17: Load regulation test conditions and specifications for the ADC08231 differ from those of the ADC08234 and ADC08238 because the ADC08231 has the on-board reference as a permanent load.

Typical Performance Characteristics

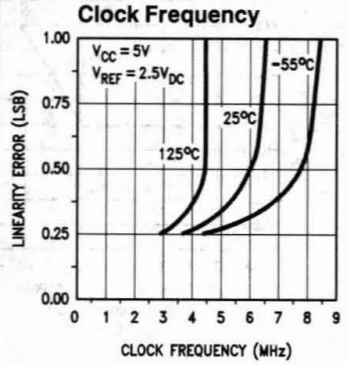
Linearity Error vs Reference Voltage



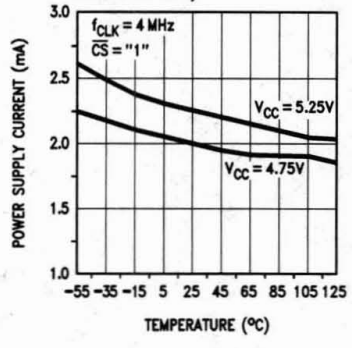
Linearity Error vs Temperature



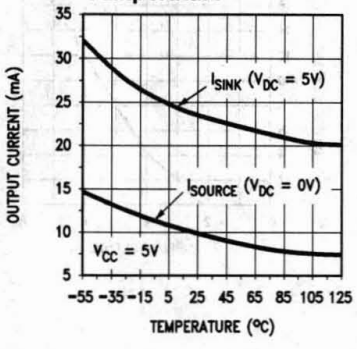
Linearity Error vs Clock Frequency



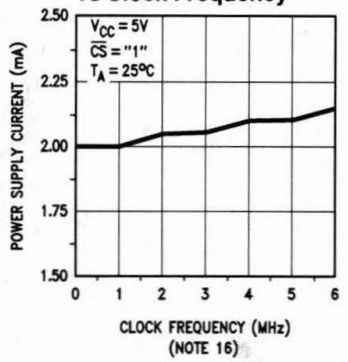
Power Supply Current vs Temperature (ADC08238, ADC08234)



Output Current vs Temperature



Power Supply Current vs Clock Frequency



Note: For ADC08231 add I_{REF} (Note 16)

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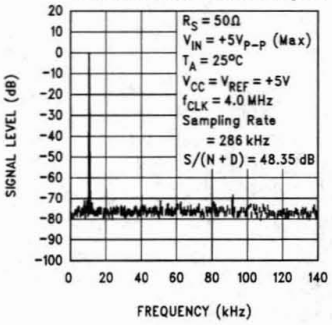
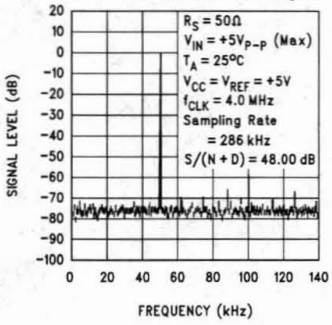
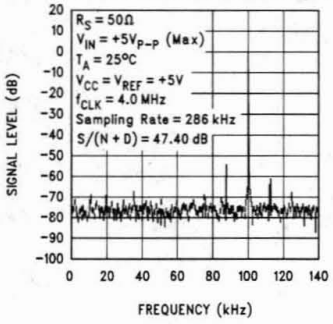
Spectral Response with 10 kHz Sine Wave Input



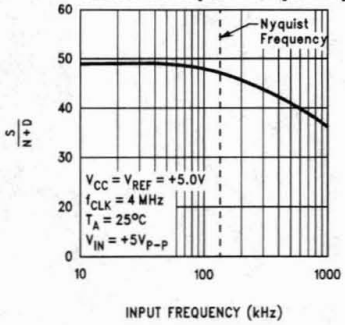
Spectral Response with 50 kHz Sine Wave Input



Spectral Response with 100 kHz Sine Wave Input



Signal-to-Noise + Distortion Ratio vs Input Frequency



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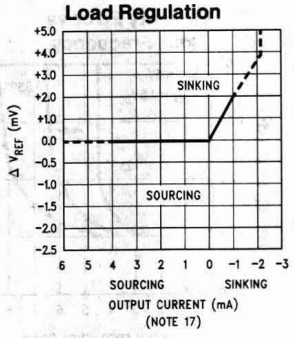
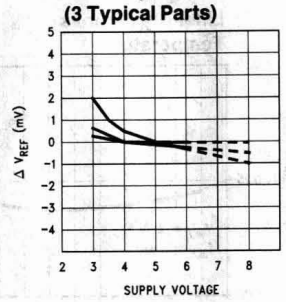
Typical Reference Performance Characteristics

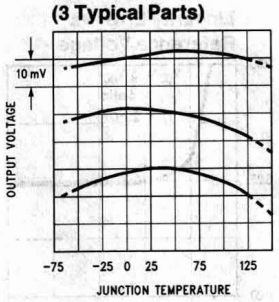
Load Regulation



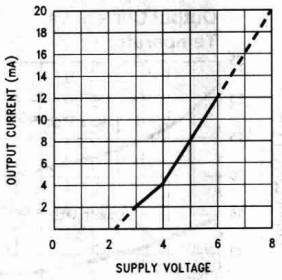
Line Regulation (3 Typical Parts)



Output Drift vs Temperature (3 Typical Parts)



Available Output Current vs Supply Voltage



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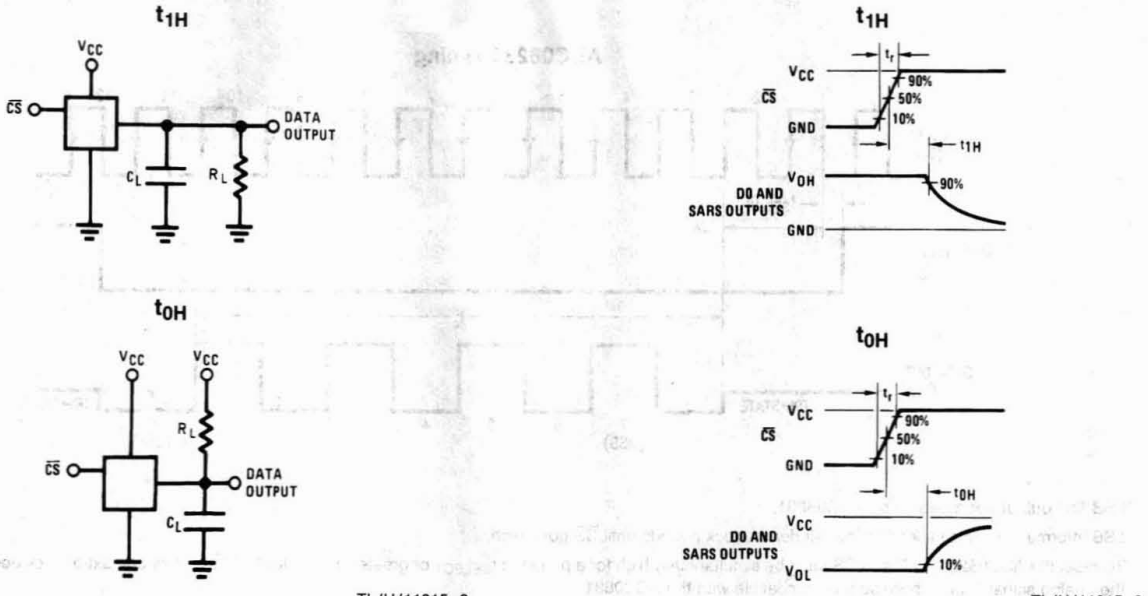
TRI-STATE Test Circuits and Waveforms



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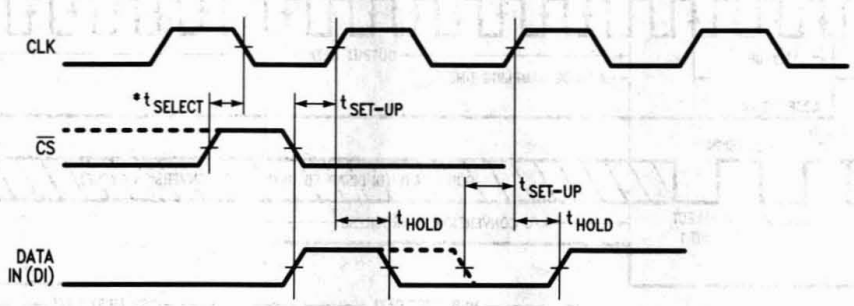
TL/H/11015–9

Timing Diagrams

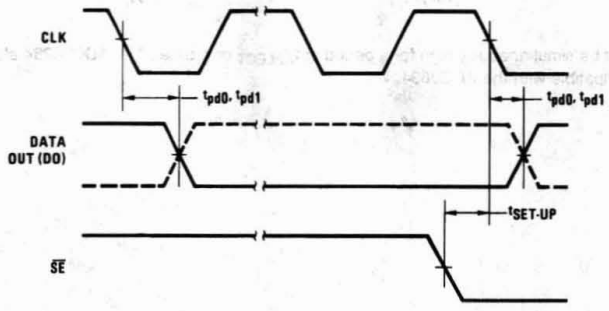
Data Input Timing



TL/H/11015–10

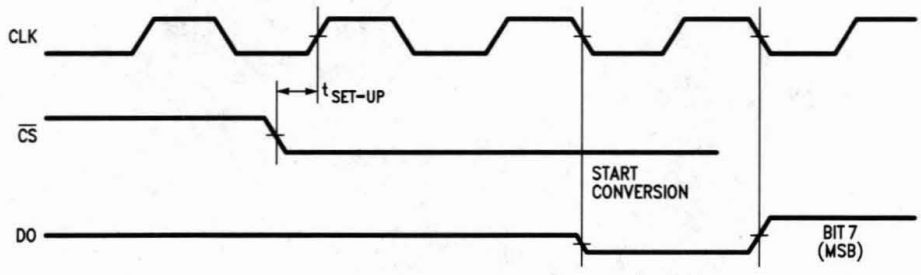
*To reset these devices, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater.

Data Output Timing



TL/H/11015–11

ADC08231 Start Conversion Timing

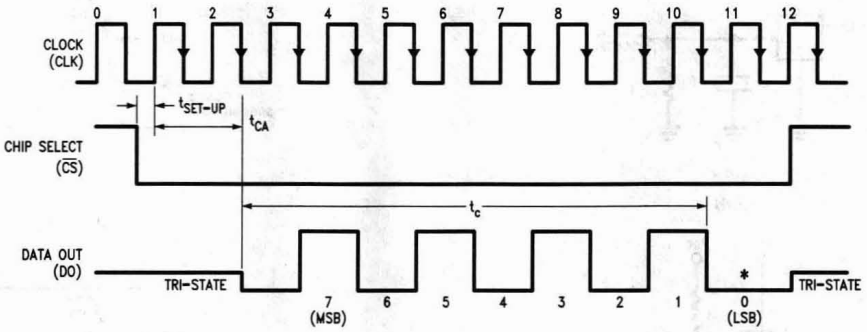


TL/H/11015–12

2

Timing Diagrams (Continued)

ADC08231 Timing



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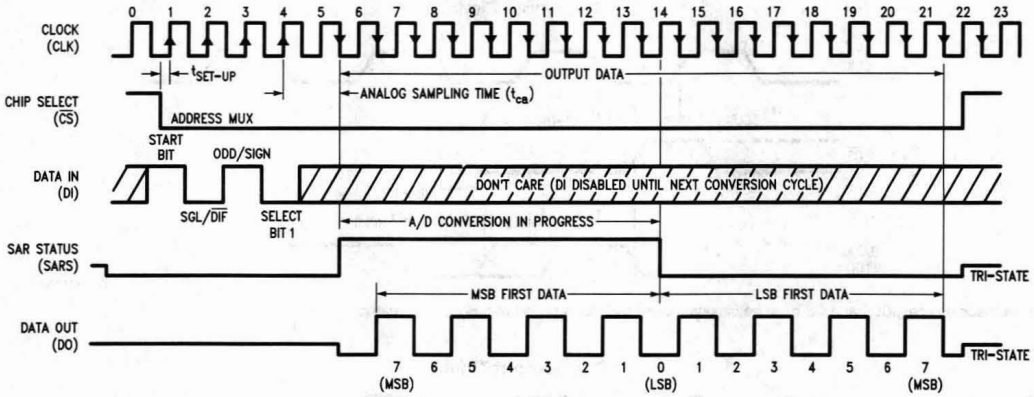
*LSB first output not available on ADC08231.

LSB information is maintained for remainder of clock periods until $\overline{CS}$ goes high.

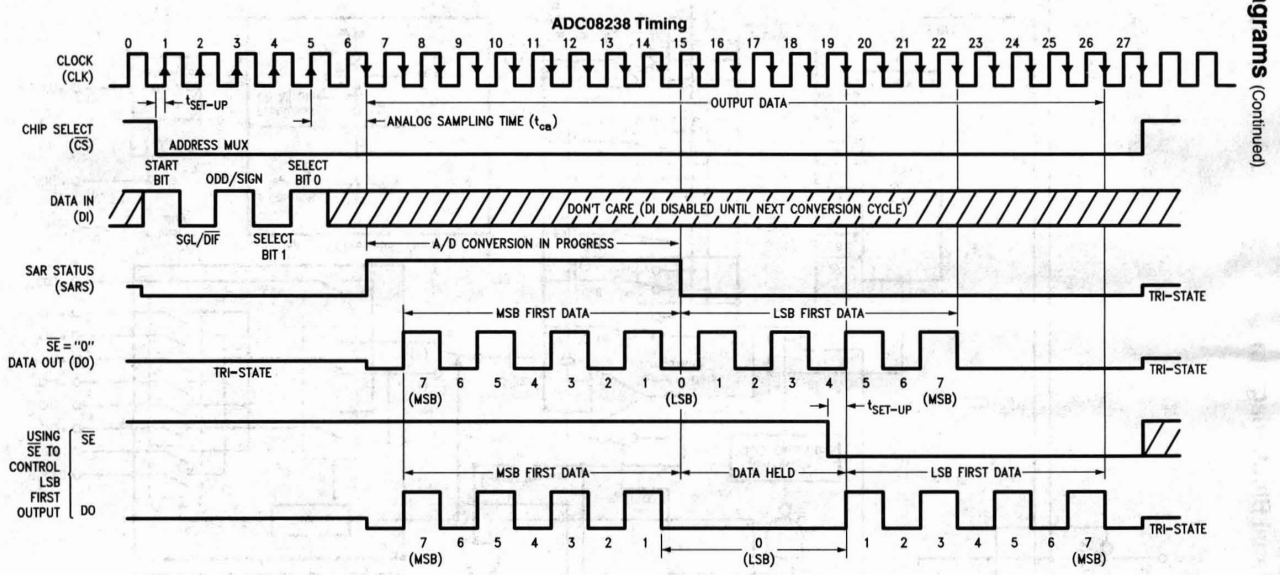
To reset the ADC08231, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. The ADC08231 also has one extra clock period for sampling the analog signal (t_{ca}). Otherwise it is compatible with the ADC0831.

ADC08234 Timing



TL/H/11015–14

To reset the ADC08234, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. The ADC08234 also has one extra clock period for sampling the analog signal (t_{ca}). Otherwise it is compatible with the ADC0834.

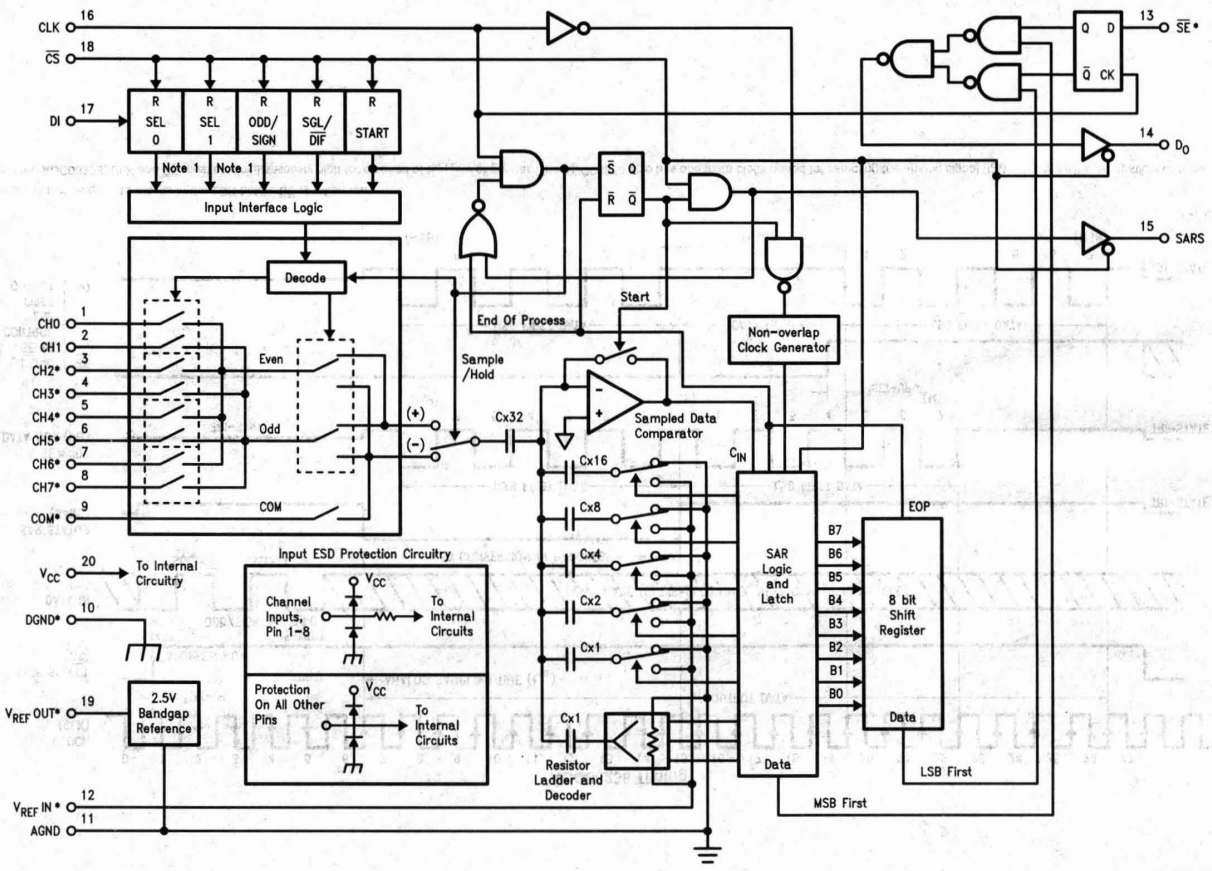


TL/H/11015–15

*Make sure clock edge #19 clocks in the LSB before $\overline{SE}$ is taken low

To reset the ADC08238, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. The ADC08238 also has one extra clock period for sampling the analog signal (t_{ca}). Otherwise it is compatible with the ADC0838.

ADC08238 Functional Block Diagram



TL/H/11015–16

*Some of these functions/pins are not available with other options.

Note 1: For the ADC08234, the "SEL 1" Flip-Flop is bypassed. For the ADC08231, V_{REFOUT} and V_{REFIN} are internally tied together.

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive-approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential (which will convert the difference between the voltage at any analog input and a common terminal) operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC08231 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line (COM) on the ADC08238 can be used as a pseudo-differential input. In this mode the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply applications where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC08231	1	1	8
ADC08234	4	2	14
ADC08238	8	4	20

TABLE II. MUX Addressing: ADC08238

Single-Ended MUX Mode

MUX Address					Analog Single-Ended Channel #								
START	SGL/$\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0	1	2	3	4	5	6	7	COM
			1	0									
1	1	0	0	0	+								−
1	1	0	0	1			+						−
1	1	0	1	0					+				−
1	1	0	1	1							+		−
1	1	1	0	0		+							−
1	1	1	0	1				+					−
1	1	1	1	0						+			−
1	1	1	1	1								+	−

2

Functional Description (Continued)

TABLE II. MUX Addressing: ADC08238 (Continued)

Differential MUX Mode

MUX Address					Analog Differential Channel-Pair #							
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT		0		1		2		3	
			1	0	0	1	2	3	4	5	6	7
1	0	0	0	0	+	−						
1	0	0	0	1			+	−				
1	0	0	1	0					+	−		
1	0	0	1	1							+	−
1	0	1	0	0	−	+						
1	0	1	0	1			−	+				
1	0	1	1	0					−	+		
1	0	1	1	1							−	+

TABLE III. MUX Addressing: ADC08234

Single-Ended MUX Mode

MUX Address				Channel #			
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT	0	1	2	3
			1				
1	1	0	0	+			
1	1	0	1			+	
1	1	1	0		+		
1	1	1	1				+

COM is internally tied to AGND

Differential MUX Mode

MUX Address				Channel #			
START	SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT	0	1	2	3
			1				
1	0	0	0	+	−		
1	0	0	1			+	−
1	0	1	0	−	+		
1	0	1	1			−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified as required before each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

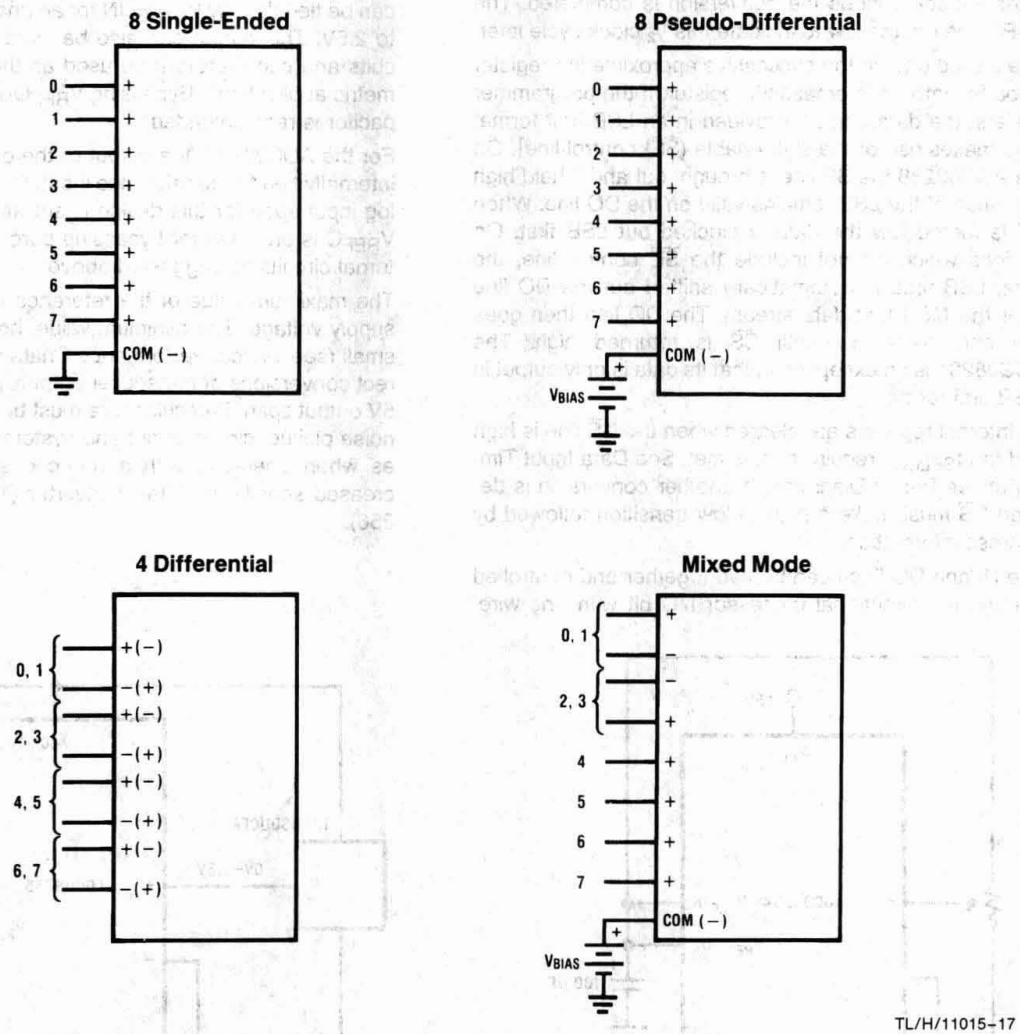
The analog input voltages for each channel can range from 50mV below ground to 50mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows many functions to be included in a small package and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate timing diagram is shown for each device.

1. A conversion is initiated by pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.
2. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.



TL/H/11015–17

FIGURE 1. Analog Input Multiplexer Options for the ADC08238

Functional Description (Continued)

3. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of 1½ clock periods is automatically inserted to allow for sampling the analog input. The SARS line goes high at the end of this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).
4. The data out (DO) line now comes out of TRI-STATE and provides a leading zero.
5. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison the comparator's output is shipped to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
6. After 8 clock periods the conversion is completed. The SARS line returns low to indicate this ½ clock cycle later.
7. The stored data in the successive approximation register is loaded into an internal shift register. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. On the ADC08238 the $\overline{SE}$ line is brought out and if held high the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low the data is clocked out LSB first. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. The ADC08231 is an exception in that its data is only output in MSB first format.
8. All internal registers are cleared when the $\overline{CS}$ line is high and the t_{SELECT} requirement is met. See Data Input Timing under Timing Diagrams. If another conversion is desired $\overline{CS}$ must make a high to low transition followed by address information.

   The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

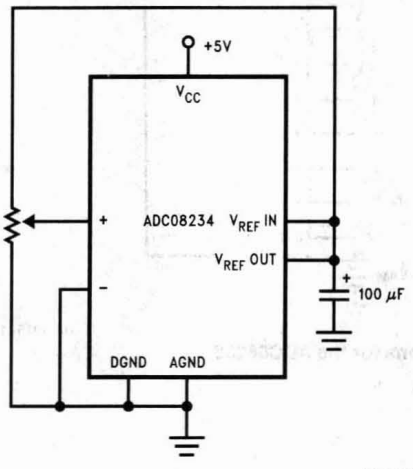
3.0 REFERENCE CONSIDERATIONS

The $V_{REF}IN$ pin on these converters is the top of a resistor divider string and capacitor array used for the successive approximation conversion. The voltage applied to this reference input defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$ over which the 256 possible output codes apply). The reference source must be capable of driving the reference input resistance, which can be as low as 1.3 kΩ.

For absolute accuracy, where the analog input varies between specific voltage limits, the reference input must be biased with a stable voltage source. The ADC08234 and the ADC08238 provide the output of a 2.5V band-gap reference at $V_{REF}OUT$. This voltage does not vary appreciably with temperature, supply voltage, or load current (see Reference Characteristics in the Electrical Characteristics tables) and can be tied directly to $V_{REF}IN$ for an analog input span of 0V to 2.5V. This output can also be used to bias external circuits and can therefore be used as the reference in ratiometric applications. Bypassing $V_{REF}OUT$ with a 100 μF capacitor is recommended.

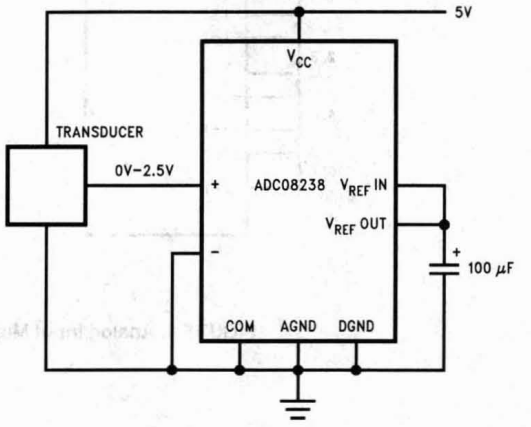
For the ADC08231, the output of the on-board reference is internally tied to the reference input. Consequently, the analog input span for this device is set at 0V to 2.5V. The pin $V_{REF}C$ is provided for bypassing purposes and biasing external circuits as suggested above.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



TL/H/11015–18

a) Ratiometric



TL/H/11015–19

b) Absolute

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60Hz common-mode signal to generate a ¼ LSB error (≈5mV) with the converter running at 250kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. While operating near or at maximum speed, bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1μA over temperature will create a 1mV input error with a 1kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for $V_{REF} = 5.000V_{DC}$).

5.2 Full Scale

A full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF}IN input for a digital output code which is just changing from 1111 1110 to 1111 1111 (See figure entitled "Span Adjust; $0V \leq V_{IN} \leq 3V$"). This is possible only with the ADC08234 and ADC08238. (The reference is internally connected to V_{REF}IN of the ADC08231).

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

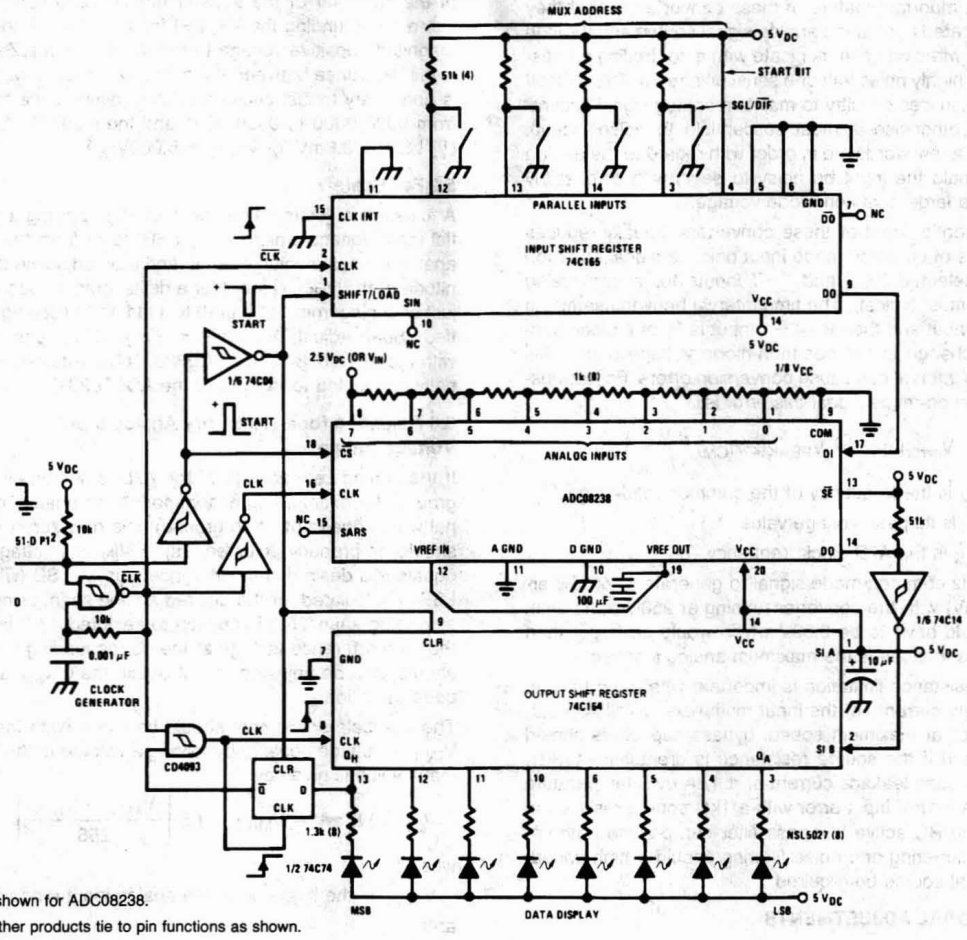
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF}IN (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

Applications

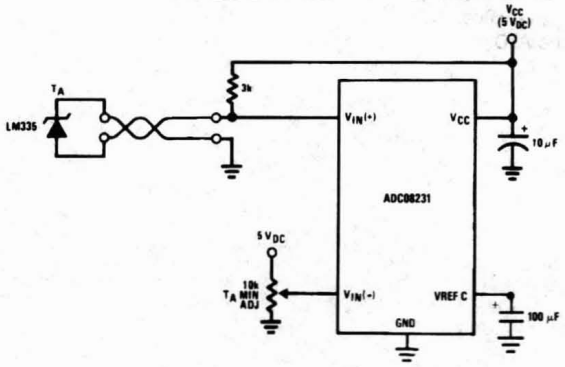
A "Stand-Alone" Hook-Up for ADC08238 Evaluation



*Pinouts shown for ADC08238.

For all other products tie to pin functions as shown.

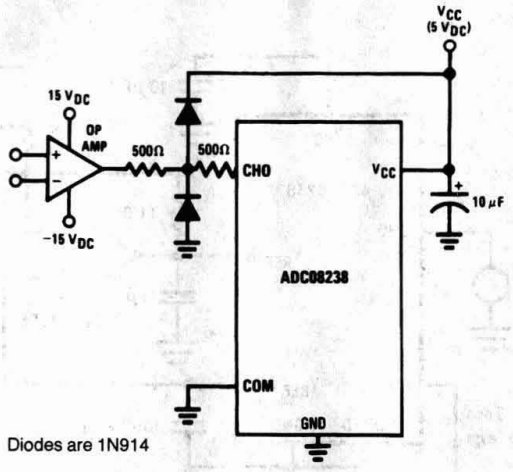
Low-Cost Remote Temperature Sensor



TL/H/11015–21

Applications (Continued)

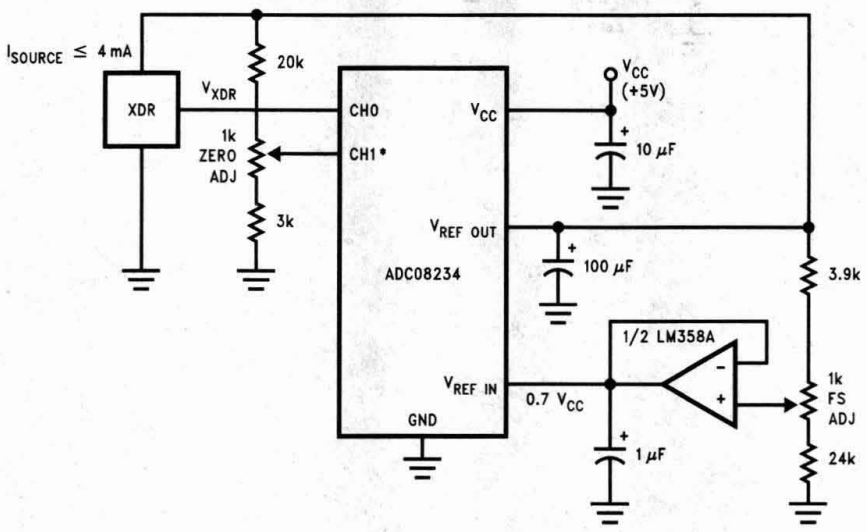
Protecting the Input



Diodes are 1N914

TL/H/11015–22

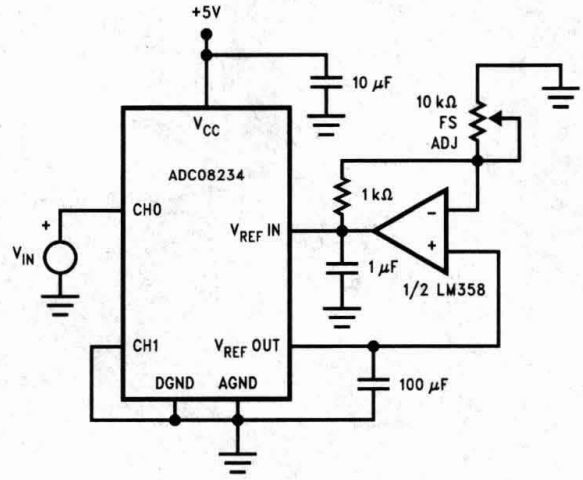
Operating with Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{REF}$
15% of $V_{REF} \leq V_{XDR} \leq$ 85% of V_{REF}

TL/H/11015–23

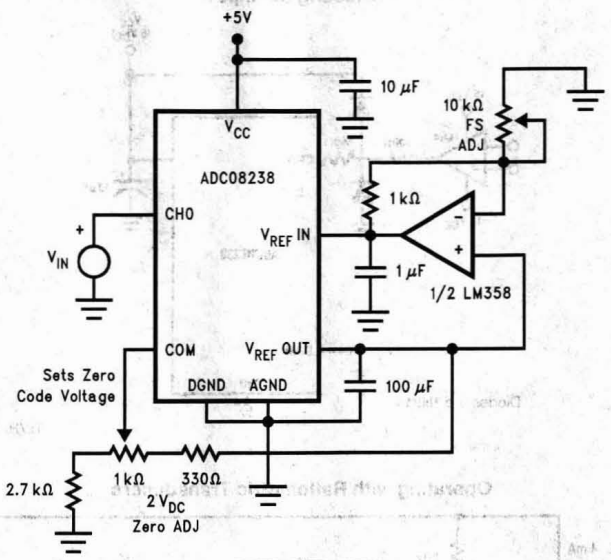
Span Adjust; 0V ≤ V_{IN} ≤ 3V



TL/H/11015–24

Applications (Continued)

Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



TL/H/11015–25

National Semiconductor

ADC0841 8-Bit μP Compatible A/D Converter

General Description

The ADC0841 is a CMOS 8-bit successive approximation A/D converter. Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/D is designed to operate with the control bus of a variety of microprocessors. TRI-STATE® output latches that directly drive the data bus permit the A/D to be configured as a memory location or I/O device to the microprocessor with no interface logic necessary.

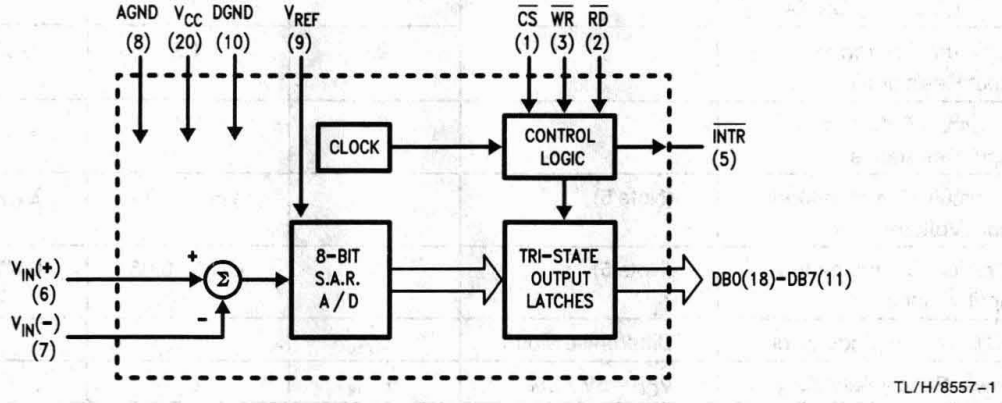
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3" standard width 20-pin package
- 20 Pin Molded Chip Carrier Package

Key Specifications

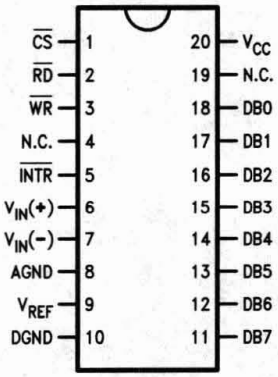
■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	40 μs

Block and Connection Diagrams



TL/H/8557-1

Dual-In-Line Package (N)

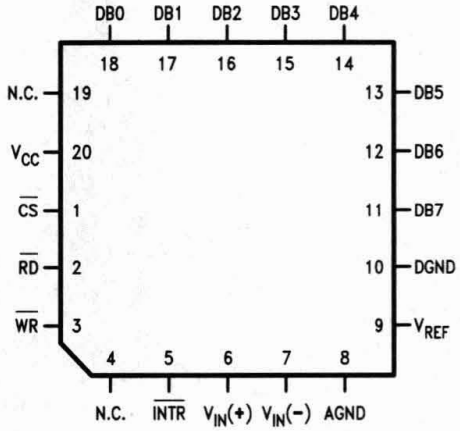


TL/H/8557-2

Top View

(N.C.-No Connection)

Molded Chip Carrier Package (V)



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Top View

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Logic Control Inputs	$-0.3V$ to $V_{CC}+0.3V$
At Other Inputs and Outputs	$-0.3V$ to $V_{CC}+0.3V$
Input Current Per Pin (Note 3)	± 5 mA
Input Current Per Package (Note 3)	± 20 mA
Storage Temperature	$-65°C$ to $+150°C$
Package Dissipation at $T_A = 25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 10)	800V

Operating Conditions (Notes 1 and 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0841BCN, ADC0841CCN	$0°C \le T_A \le 70°C$
ADC0841BCV, ADC0841CCV	$-40°C \le T_A \le 85°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = 5$ V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	ADC0841BCN, ADC0841CCN ADC0841BCV, ADC0841CCV			Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Maximum Total Unadjusted Error	$V_{REF} = 5.00$ V_{DC} (Note 4)				
ADC0841BCN, BCV			$\pm 1/2$	**$\pm 1/2$**	LSB
ADC0841CCN, CCV			± 1	**± 1**	LSB
Minimum Reference Input Resistance		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance		2.4	5.4	**5.9**	kΩ
Maximum Common-Mode Input Voltage	(Note 5)		$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
Minimum Common-Mode Input Voltage	(Note 5)		GND -0.05	**GND -0.05**	V
DC Common-Mode Error	Differential Mode	$\pm 1/16$	$\pm 1/4$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$	$\pm 1/16$	$\pm 1/8$	$\pm 1/8$	LSB

Electrical Characteristics The following specifications apply for $V_{CC}=5\ V_{DC}$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A=T_j=25°C$. (Continued)

Symbol	Parameter	Conditions	ADC0841BCN, ADC0841CCN ADC0841BCV, ADC0841CCV			Units
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
DIGITAL AND DC CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage (Min)	$V_{CC}=5.25V$		2.0	**2.0**	V
$V_{IN(0)}$	Logical "0" Input Voltage (Max)	$V_{CC}=4.75V$		0.8	**0.8**	V
$I_{IN(1)}$	Logical "1" Input Current (Max)	$V_{IN}=5.0V$	0.005		**1**	μA
$I_{IN(0)}$	Logical "0" Input Current (Max)	$V_{IN}=0V$	−0.005		**−1**	μA
$V_{OUT(1)}$	Logical "1" Output Voltage (Min)	$V_{CC}=4.75V$ $I_{OUT}=-360\ \mu A$ $I_{OUT}=-10\ \mu A$		 2.8 4.6	 **2.4** **4.5**	 V V
$V_{OUT(0)}$	Logical "0" Output Voltage (Max)	$V_{CC}=4.75V$ $I_{OUT}=1.6\ mA$		0.34	**0.4**	V
I_{OUT}	TRI-STATE Output Current (Max)	$V_{OUT}=0V$ $V_{OUT}=5V$	−0.01 0.01	−0.3 0.3	**−3** **3**	μA μA
I_{SOURCE}	Output Source Current (Min)	$V_{OUT}=0V$	−14	−7.5	**−6.5**	mA
I_{SINK}	Output Sink Current (Min)	$V_{OUT}=V_{CC}$	16	9.0	**8.0**	mA
I_{CC}	Supply Current (Max)	$\overline{CS}=1$, V_{REF} Open	1	2.3	**2.5**	mA

AC Characteristics

The following specifications apply for $V_{CC} = 5V_{DC}$, $t_r = t_f = 10$ ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_C	Maximum Conversion Time (See Graph)		30	40	**60**	μs
$t_{W(\overline{WR})}$	Minimum $\overline{WR}$ Pulse Width	(Note 9)	50	150		ns
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF (Note 9)	145	225		ns
t_{1H}, t_{0H}	TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L = 10$ pF, $R_L = 10$k, $t_r = 20$ ns (Note 9)	125		200	ns
t_{WI}, t_{RI}	Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$	(Note 9)	200	400		ns
C_{IN}	Capacitance of Logic Inputs		5			pF
C_{OUT}	Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: During over-voltage conditions ($V_{IN} < 0V$ and $V_{IN} > V_{CC}$) the maximum input current at any one pin is ±5 mA. If the current is limited to ±5 mA at all the pins no more than four pins can be in this condition in order to meet the Input Current Per Package (±20 mA) specification.

Note 4: Total undajusted error includes offset, full-scale, and linearity.

Note 5: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

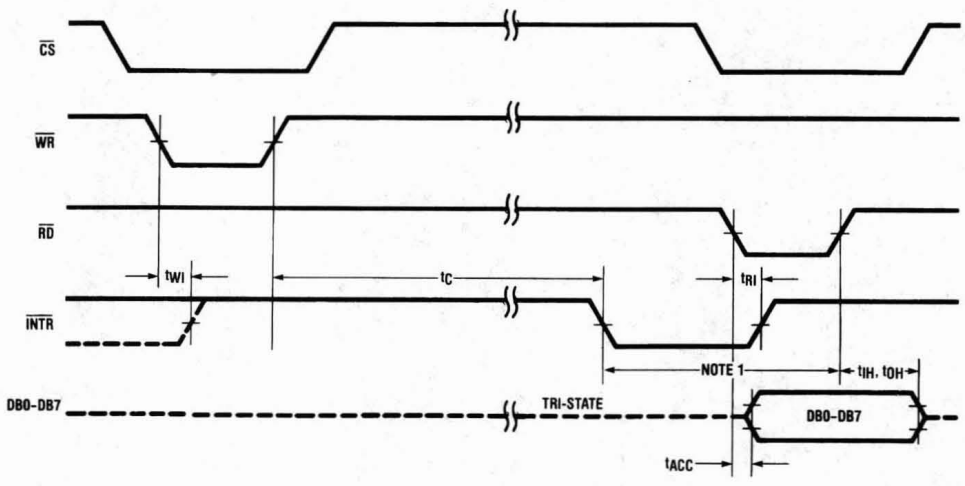
Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 9: The temperature coefficient is 0.3%/°C.

Note 10: Human body model, 100 pF discharged through 1.5 kΩ resistor.

Timing Diagram



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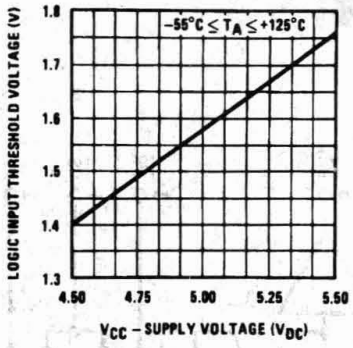
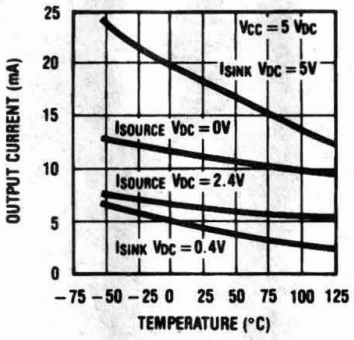
Note 1: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Performance Characteristics

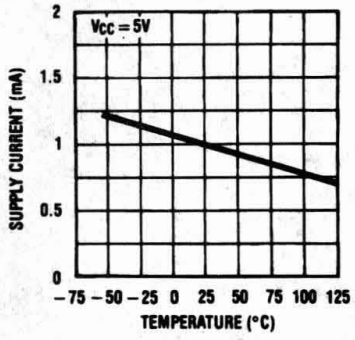
Logic Input Threshold Voltage vs Supply Voltage



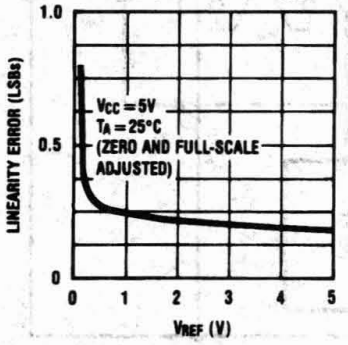
Output Current vs Temperature



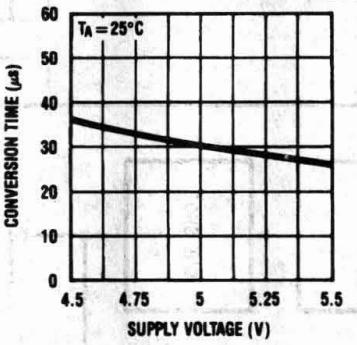
Power Supply Current vs Temperature



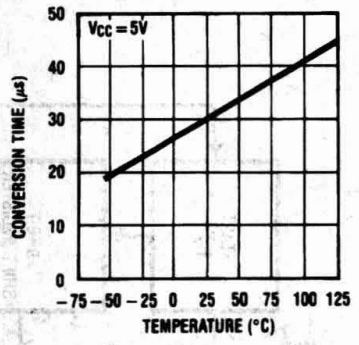
Linearity Error vs V_{REF}



Conversion Time vs V_{SUPPLY}

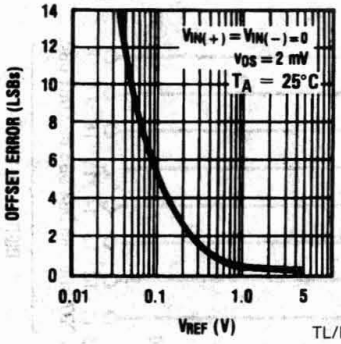


Conversion Time vs Temperature



TL/H/8557–4

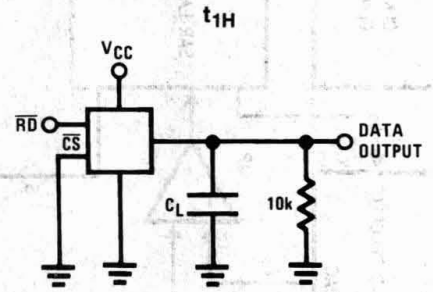
Unadjusted Offset Error vs V_{REF} Voltage



TL/H/8557–22

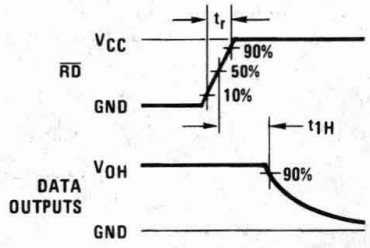
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/8557–5

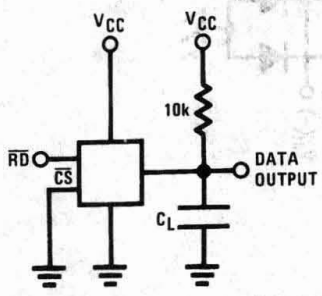
t_{1H}, C_L = 10 pF



TL/H/8557–6

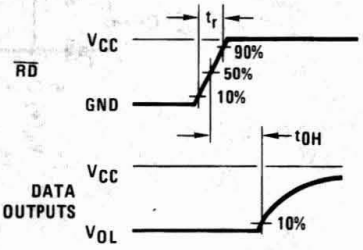
t_r = 20 ns

t_{0H}



TL/H/8557–7

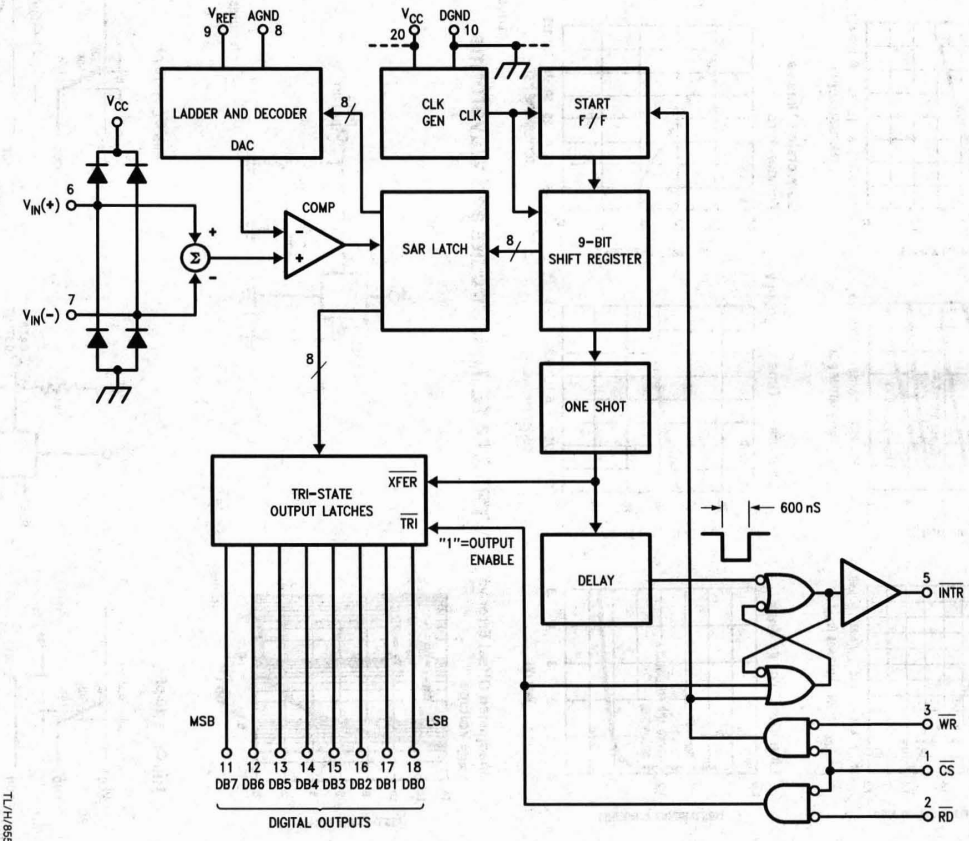
t_{0H}, C_L = 10 pF



TL/H/8557–8

t_r = 20 ns

Functional Block Diagram



TL/H/8557-10

Functional Description

A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$ starts a conversion. After the conversion cycle ($t_C \leq 60$ μsec), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and transfers the conversion result on the output data lines (DB0–DB7).

Applications Information

1.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input of this converter defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The device can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 1a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 1b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with this converter.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

2.0 THE ANALOG INPUTS

2.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of this converter actually reduce the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{ERROR(MAX)} = V_{peak}\,(2\pi\, f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, Vpeak is its peak voltage value and t_C is the conversion time.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈ 5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

2.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

3.0 OPTIONAL ADJUSTMENTS

3.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the V_{IN} (−) input at this $V_{IN(MIN)}$ value.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF} = 5.000\ V_{DC}$).

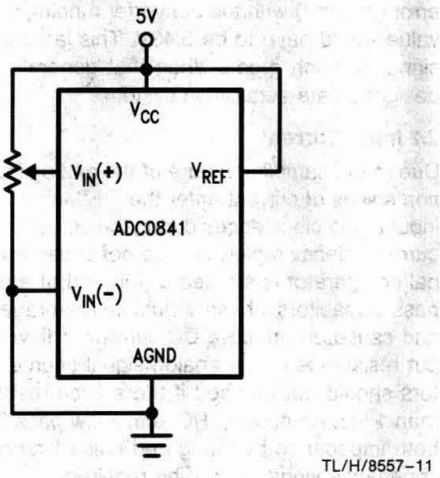
3.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

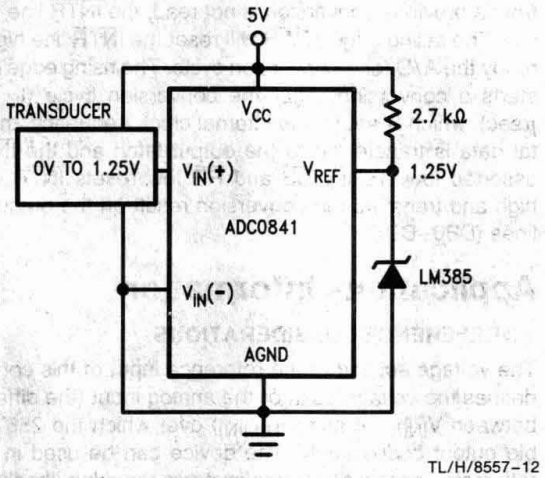
3.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to the "+" input ($V_{IN}(+)$) and the zero reference voltage at the "−" input ($V_{IN}(-)$)should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

Applications Information (Continued)



a) Ratiometric



b) Absolute with a Reduced Span

FIGURE 1. Referencing Examples

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

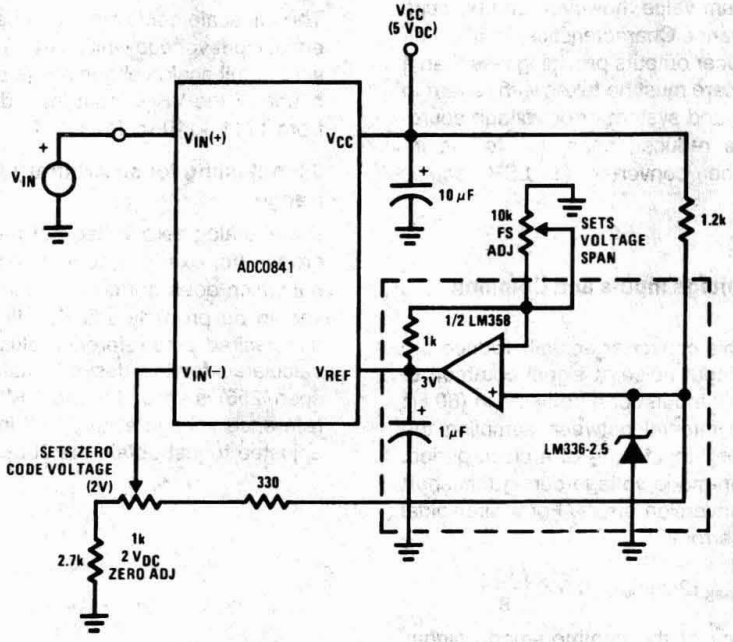
$$V_{IN}(+)\,\text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

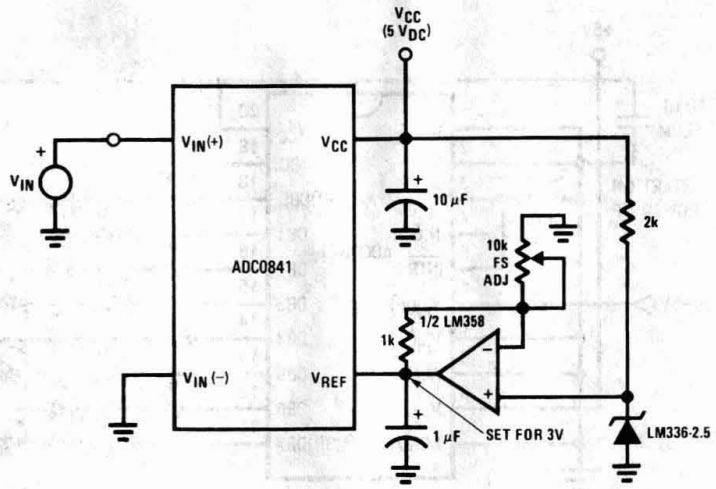
For an example see the Zero-Shift and Span Adjust circuit below.

Zero-Shift and Span Adjust ($2V \leq V_{IN} \leq 5V$)



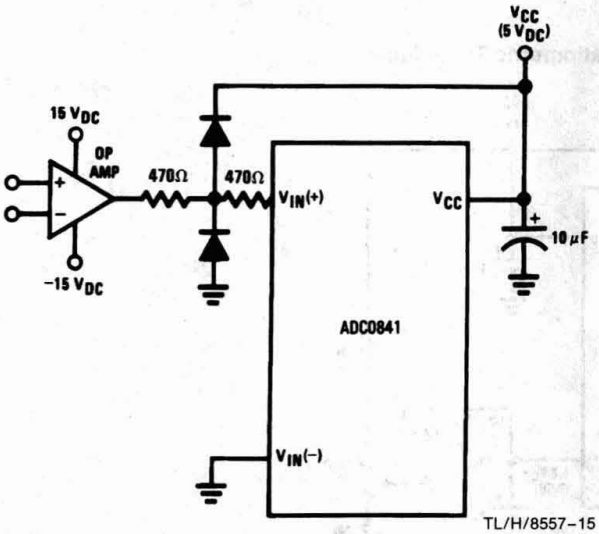
Applications Information (Continued)

Span Adjust $0V \leq V_{IN} \leq 3V$



TL/H/8557–14

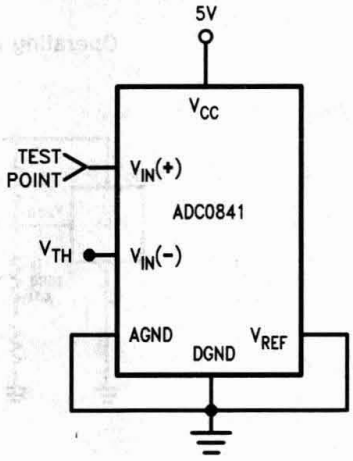
Protecting the Input



TL/H/8557–15

Diodes are 1N914

High Accuracy Comparator

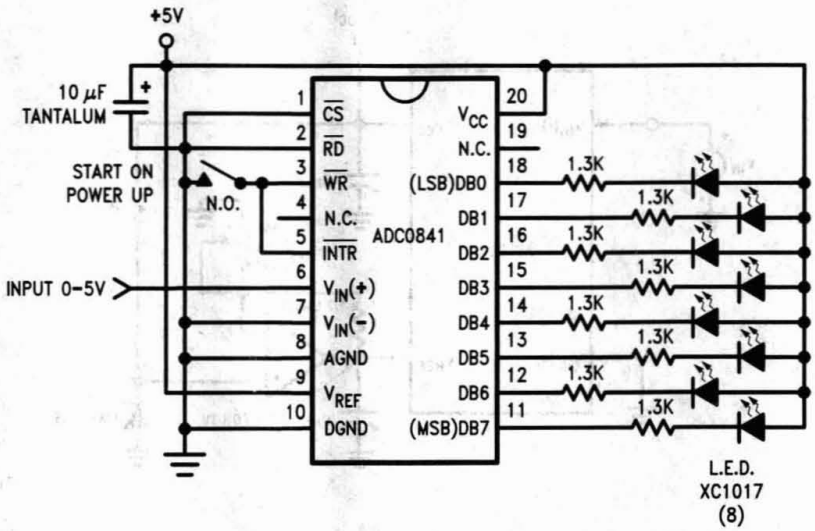


TL/H/8557–16

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$
DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

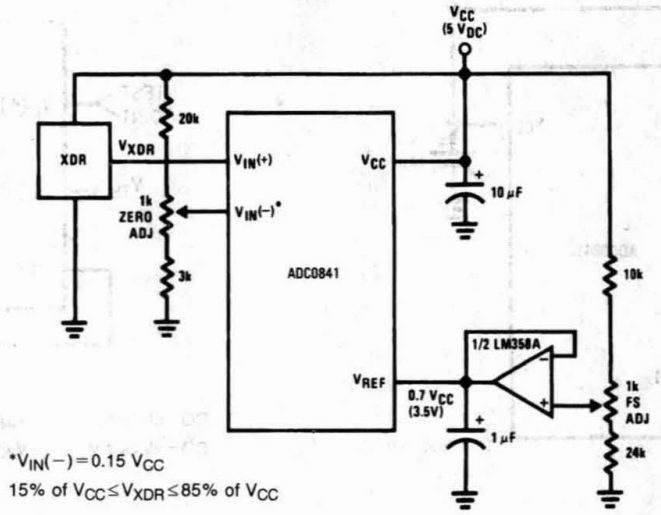
Applications Information (Continued)

Continuous Conversion



TL/H/8557–19

Operating with Automotive Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

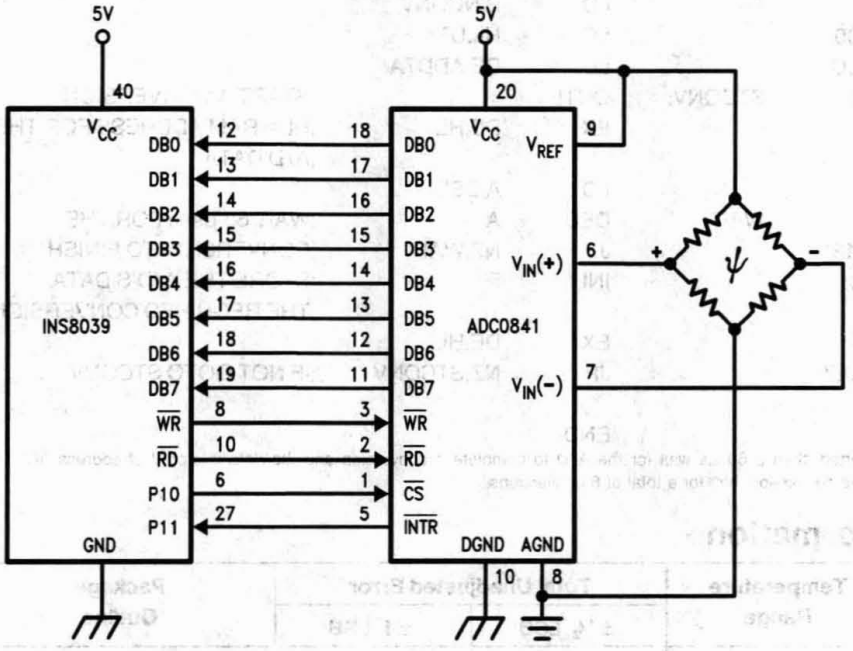
TL/H/8557–17

Applications Information (Continued)

SAMPLE PROGRAM FOR ADC0841—INS8039 INTERFACE
CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

```
                        ORG     0H
0000    04 10           JMP     BEGIN       ;START PROGRAM AT ADDR 10
                        ORG     10H         ;MAIN PROGRAM
0010    B9 FF   BEGIN:  MOV     R1,#0FFH    ;LOAD R1 WITH A UNUSED ADDR
                                            ;LOCATION
0012    B8 20           MOV     R0,#20H     ;A/D DATA ADDRESS
0014    89 FF           ORL     P1,#0FFH    ;SET PORT 1 OUTPUTS HIGH
0016    23 00           MOV     A,00H       ;LOAD THE ACC WITH 00
0018    14 50           CALL    CONV        ;CALL THE CONVERSION SUBROUTINE

                        ;CONTINUE MAIN PROGRAM

                        ;CONVERSION SUBROUTINE
                        ;ENTRY:ACC—A/D MUX DATA
                        ;EXIT: ACC—CONVERTED DATA

                        ORG     50H
0050    99 FE   CONV:   ANL     P1,#0FEH    ;CHIP SELECT THE A/D
0052    91              MOVX    @R1,A       ;START CONVERSION
0053    09      LOOP:   IN      A,P1        ;INPUT INTR STATE
0054    32 53           JB1     LOOP        ;IF INTR = 1 GOTO LOOP
0056    81              MOVX    A,@R1       ;IF INTR = 0 INPUT A/D DATA
0057    89 01           ORL     P1,&01H     ;CLEAR THE A/D CHIP SELECT
0059    A0              MOV     @R0,A       ;STORE THE A/D DATA
005A    83              RET                 ;RETURN TO MAIN PROGRAM
```

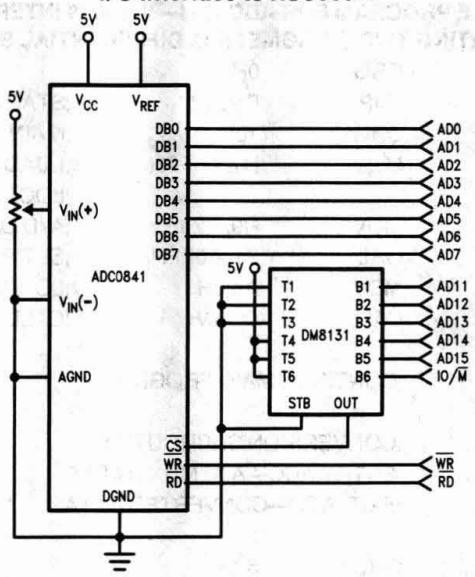
ADC0841—INS8039 Interface



TL/H/8557–20

Applications Information (Continued)

I/O Interface to NSC800™



TL/H/8557–21

SAMPLE PROGRAM FOR ADC0841—NSC800 INTERFACE

```
0010                NCONV   EQU   16        ;TWICE THE NUMBER OF REQUIRED
                                              ;CONVERSIONS
000F                DEL     EQU   15        ;DELAY 60 μsec CONVERSION
001F                CS      EQU   1FH       ;THE BOARD ADDRESS
3C00                ADDTA   EQU   003CH     ;START OF RAM FOR A/D
                                              ;DATA
0000'  00           DTA:    DB    08H       ; DATA
0001'  0E 1F        START:  LD    C,CS
0003'  06 16                LD    B,NCONV
0005'  21 0000'             LD    HL,DTA
0008'  11 003C              LD    DE,ADDTA
000B'  ED A3        STCONV: OUTI                ;START A CONVERSION
000D'  EB                   EX    DE,HL     ;HL = RAM ADDRESS FOR THE
                                              ;A/D DATA
000E'  3E 0F                LD    A,DEL
0010'  3D           WAIT:   DEC   A         ;WAIT 60 μsec FOR THE
0011'  C2 0013'             JP    NZ,WAIT   ;CONVERSION TO FINISH
0014'  ED A2                INI               ;STORE THE A/D'S DATA
                                              ;THE REQUIRED CONVERSIONS COMPLETED?
0016'  EB                   EX    DE,HL
0017'  C2 000E'             JP    NZ,STCONV ;IF NOT GOTO STCONV

                            END
```

Note: A conversion is started, then a 60 μs wait for the A/D to complete a conversion and the data is stored at address ADDTA for the first conversion, ADDTA + 1 for the second conversion, etc. for a total of 8 conversions.

Ordering Information

Temperature Range	Total Unadjusted Error		Package Outline
	±½ LSB	±1 LSB	
0°C to +70°C	ADC0841BCN	ADC0841CCN	N20A Molded Dip
−40°C to +85°C	ADC0841BCV	ADC0841CCV	V20A Molded Chip Carrier

National Semiconductor

ADC0844/ADC0848 8-Bit μP Compatible A/D Converters with Multiplexer Options

General Description

The ADC0844 and ADC0848 are CMOS 8-bit successive approximation A/D converters with versatile analog input multiplexers. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/Ds are designed to operate from the control bus of a wide variety of microprocessors. TRI-STATE® output latches that directly drive the data bus permit the A/Ds to be configured as memory locations or I/O devices to the microprocessor with no interface logic necessary.

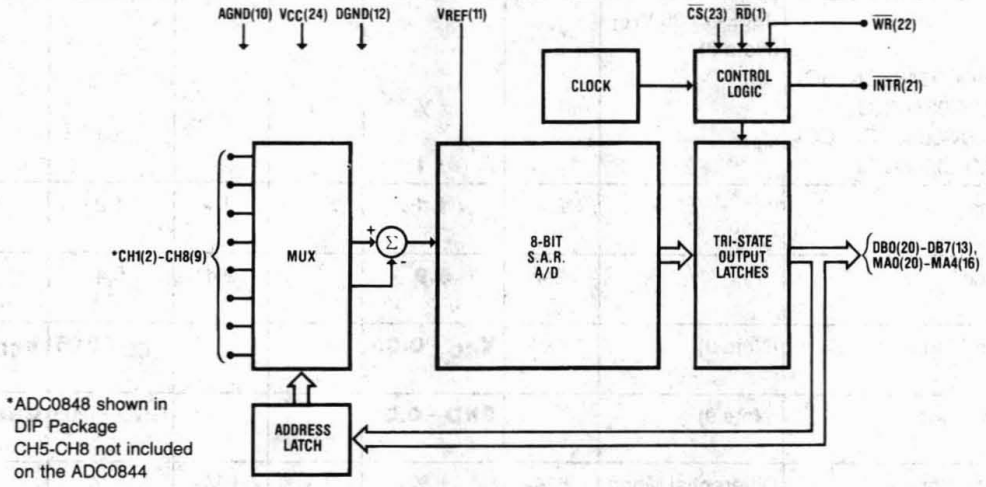
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel or 8-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3" standard width 20-pin or 24-pin DIP
- 28 Pin Molded Chip Carrier Package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	40 μs

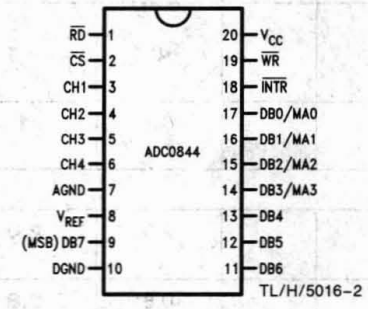
Block and Connection Diagrams



*ADC0848 shown in DIP Package
CH5-CH8 not included on the ADC0844

TL/H/5016-1

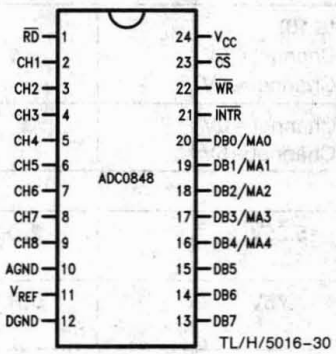
Dual-In-Line Package



TL/H/5016-2

Top View

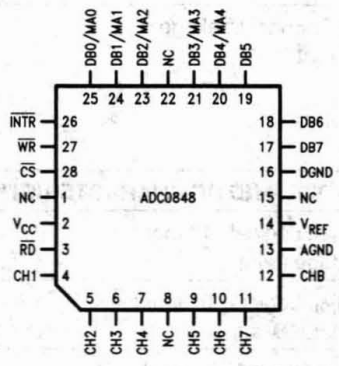
Dual-In-Line Package



TL/H/5016-30

Top View

Molded Chip Carrier Package



TL/H/5016-29

Top View

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage	
Logic Control Inputs	−0.3V to +15V
At Other Inputs and Outputs	−0.3V to V_{CC}+0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 4)	800V
Lead Temperature (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0844BCN, ADC0844CCN, ADC0848BCN, ADC0848CCN	0°C≤T_A≤70°C
ADC0844BCJ, ADC0844CCJ, ADC0848BCJ, ADC0848CCJ ADC0848BCV, ADC0848CCV	−40°C≤T_A≤85°C

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_j = 25°C.

Parameter	Conditions	ADC0844BCJ ADC0844CCJ ADC0848BCJ ADC0848CCJ			ADC0844BCN, ADC0844CCN ADC0848BCN, ADC0848CCN ADC0848BCV, ADC0848CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	V_{REF}=5.00 V_{DC} (Note 8)							
ADC0844BCN, ADC0848BCN, BCV						±½	**±½**	LSB
ADC0844BCJ, ADC0848BCJ			**±½**					LSB
ADC0844CCN, ADC0848CCN, CCV						±1	**±1**	LSB
ADC0844CCJ, ADC0848CCJ			**±1**					LSB
Minimum Reference Input Resistance		2.4	**1.1**		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance		2.4	**5.9**		2.4	5.4	**5.9**	kΩ
Maximum Common-Mode Input Voltage	(Note 9)		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Voltage	(Note 9)		**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Differential Mode	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity	V_{CC}=5V±5%	±1/16	**±⅛**		±1/16	±⅛	**±⅛**	LSB
Off Channel Leakage Current	(Note 10) On Channel=5V, Off Channel=0V		**−1**			−0.1	**−1**	μA
	On Channel=0V, Off Channel=5V		**1**			0.1	**1**	μA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC}=5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC}=4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN}=5.0V	0.005	**1**		0.005		**1**	μA

Electrical Characteristics The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j$ = 25°C. (Continued)

Parameter	Conditions	ADC0844BCJ, ADC0844CCJ, ADC0848BCJ, ADC0848CCJ			ADC0844BCN, ADC0844CCN, ADC0848BCN, ADC0848CCN, ADC0848BCV, ADC0848CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
DIGITAL AND DC CHARACTERISTICS (Continued)								
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	**−1**		−0.005		**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.5**			2.8 4.6	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	**−3** **3**		−0.01 0..01	−0.3 0.3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	**2.5**		1	2.3	**2.5**	mA

AC Electrical Characteristics The following specifications apply for V_{CC} = 5V_{DC}, $t_r = t_f$ = 10 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Units
t_C, Maximum Conversion Time (See Graph)		30	40	**60**	μs
$t_{W(\overline{WR})}$, Minimum $\overline{WR}$ Pulse Width	(Note 11)	50	150		ns
t_{ACC}, Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF (Note 11)	145		225	ns
t_{1H}, t_{0H}, TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (Note 11)	125		200	ns
t_{WI}, t_{RI}, Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$	(Note 11)	200	400		ns
t_{DS}, Minimum Data Set-Up Time	(Note 11)	50	100		ns
t_{DH}, Minimum Data Hold Time	(Note 11)	0	50		ns
C_{IN}, Capacitance of Logic Inputs		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Design limits are guaranteed by not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 8: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

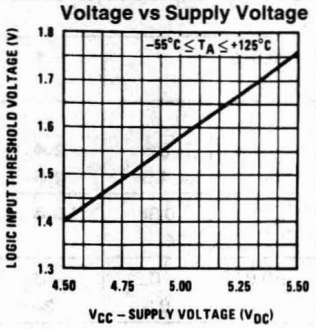
Note 9: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 10: Off channel leakage current is measured after the channel selection.

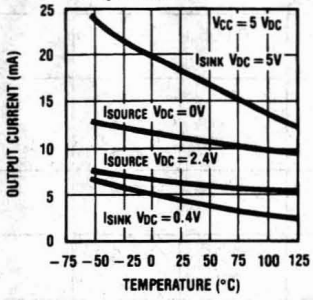
Note 11: The temperature coefficient is 0.3%/°C.

Typical Performance Characteristics

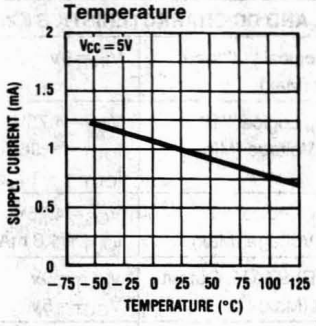
Logic Input Threshold Voltage vs Supply Voltage



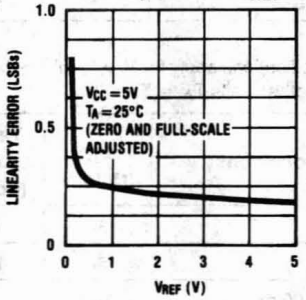
Output Current vs Temperature



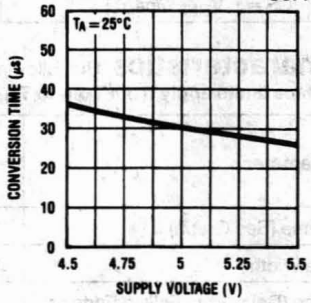
Power Supply Current vs Temperature



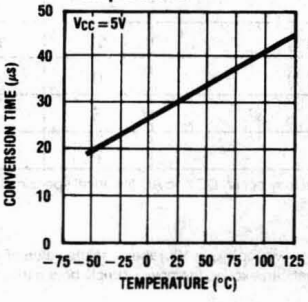
Linearity Error vs V_{REF}



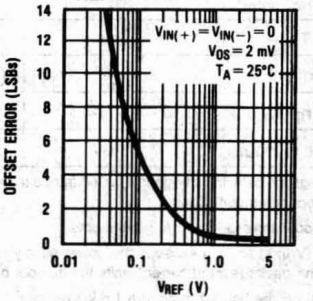
Conversion Time vs V_{SUPPLY}



Conversion Time vs Temperature



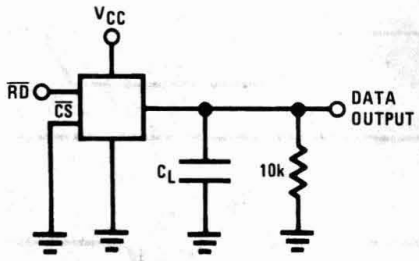
Unadjusted Offset Error vs V_{REF} Voltage



TL/H/5016–3

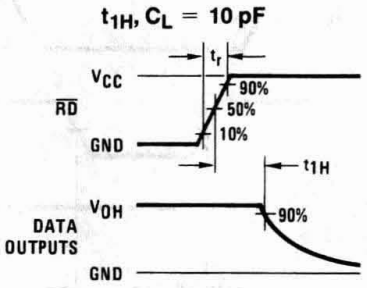
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/5016-4

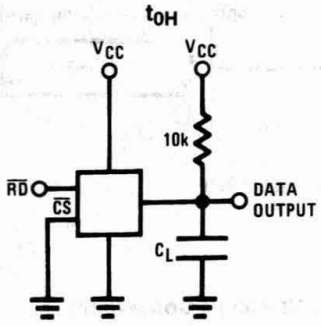
t_{1H}, C_L = 10 pF



TL/H/5016-5

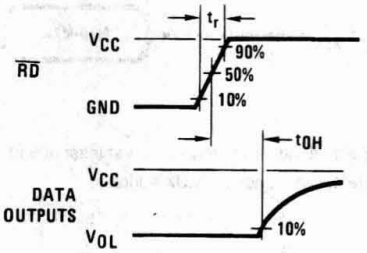
t_r = 20 ns

t_{0H}



TL/H/5016-6

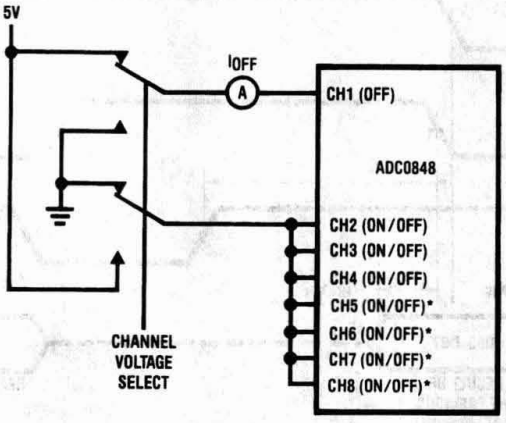
t_{0H}, C_L = 10 pF



TL/H/5016-7

t_r = 20 ns

Leakage Current Test Circuit



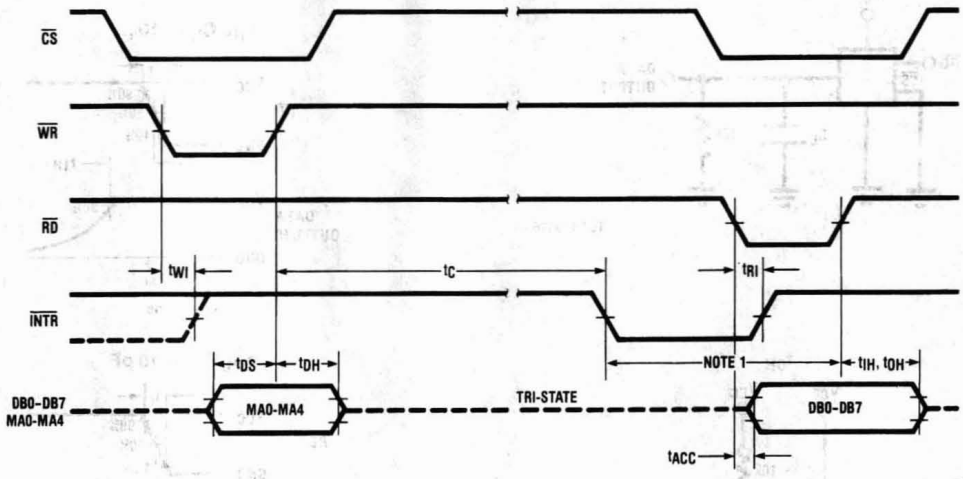
*NOT INCLUDED ON ADC0844

TL/H/5016-8

2

Timing Diagrams

Programming New Channel Configuration and Starting a Conversion

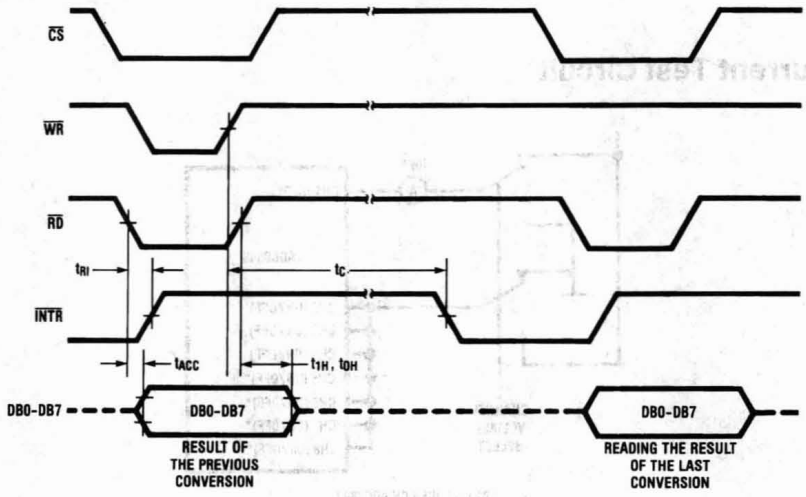


TL/H/5016–9

Note 1: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of $\overline{INTR}$.

Note 2: MA stands for MUX address.

Using the Previously Selected Channel Configuration and Starting a Conversion



TL/H/5016–10

ADC0848 Functional Block Diagram

TL/H/5016–11

Functional Description

The ADC0844 and ADC0848 contain a 4-channel and 8-channel analog input multiplexer (MUX) respectively. Each MUX can be configured into one of three modes of operation differential, pseudo-differential, and single ended. These modes are discussed in the Applications Information Section. The specific mode is selected by loading the MUX address latch with the proper address (see Table I and Table II). Inputs to the MUX address latch (MA0-MA4) are common with data bus lines (DB0-DB4) and are enabled when the $\overline{RD}$ line is high. A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$, with $\overline{RD}$ high, strobes the data on the MA0/DB0-MA4/DB4 inputs into the MUX address latch to select a new input configuration and start a conversion. If the $\overline{RD}$ line is held low during the entire low period of $\overline{WR}$ the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ($t_C \leq 40\ \mu s$), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and outputs the conversion result on the data lines (DB0-DB7).

Applications Information

1.0 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-

TABLE I. ADC0844 MUX ADDRESSING

MUX Address				$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel #					MUX Mode
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND	
X	L	L	L	L	↓	H	+	−				Differential
X	L	L	H	L		H	−	+				
X	L	H	L	L		H			+	−		
X	L	H	H	L		H			−	+		
L	H	L	L	L	↓	H	+				−	Single-Ended
L	H	L	H	L		H		+			−	
L	H	H	L	L		H			+		−	
L	H	H	H	L		H				+	−	
H	H	L	L	L	↓	H	+			−		Pseudo-Differential
H	H	L	H	L		H		+		−		
H	H	H	L	L		H			+	−		
X	X	X	X	L	↓	L	Previous Channel Configuration					

X = don't care

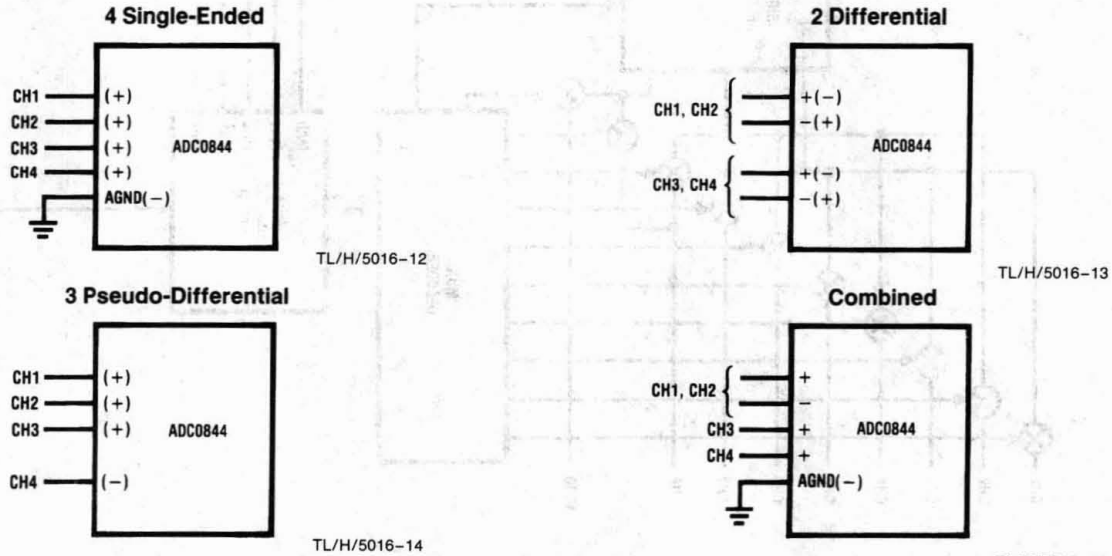


FIGURE 1. Analog Input Multiplexer Options

Applications Information (Continued)

ended, or pseudo-differential. *Figure 1* shows the three modes using the 4-channel MUX ADC0844. The eight inputs of the ADC0848 can also be configured in any of the three modes. In the differential mode, the ADC0844 channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1–CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1–CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 2a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 2b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the

TABLE II. ADC0848 MUX Addressing

MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel									MUX Mode
MA4	MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	AGND	
X	L	L	L	L	L	↓	H	+	−								Differential
X	L	L	L	H	L		H	−	+								
X	L	L	H	L	L		H			+	−						
X	L	L	H	H	L		H			−	+						
X	L	H	L	L	L		H					+	−				
X	L	H	L	H	L		H					−	+				
X	L	H	H	L	L		H							+	−		
X	L	H	H	H	L		H							−	+		
L	H	L	L	L	L	↓	H	+								−	Single-Ended
L	H	L	L	H	L		H		+							−	
L	H	L	H	L	L		H			+						−	
L	H	L	H	H	L		H				+					−	
L	H	H	L	L	L		H					+				−	
L	H	H	L	H	L		H						+			−	
L	H	H	H	L	L		H							+		−	
L	H	H	H	H	L		H								+	−	
H	H	L	L	L	L	↓	H	+							−		Pseudo-Differential
H	H	L	L	H	L		H		+						−		
H	H	L	H	L	L		H			+					−		
H	H	L	H	H	L		H				+				−		
H	H	H	L	L	L		H					+			−		
H	H	H	L	H	L		H						+		−		
H	H	H	H	L	L		H							+	−		
X	X	X	X	X	L	↓	L	Previous Channel Configuration										

Applications Information (Continued)

"+" input and then the "−" inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{ERROR(MAX)} = V_{peak}\,(2\pi\, f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, V_{peak} is its peak voltage value and t_C is the conversion time.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈ 5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

3.3 Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of ± 1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

4.0 OPTIONAL ADJUSTMENTS

4.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This is useful for either differential or pseudo-differential modes of input channel configuration.

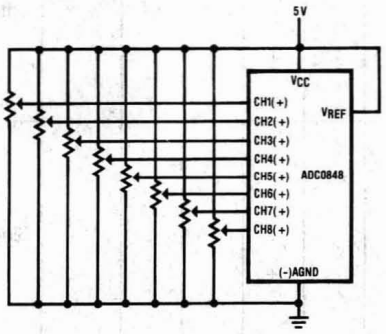
The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF} = 5.000\ V_{DC}$).

4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

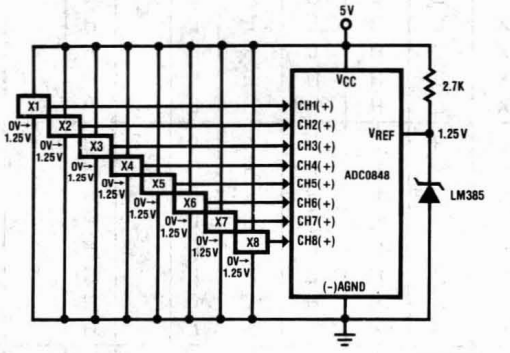
4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.



TL/H/5016–16

a) Ratiometric



TL/H/5016–17

b) Absolute with a Reduced Span

FIGURE 2. Referencing Examples

Applications Information (Continued)

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

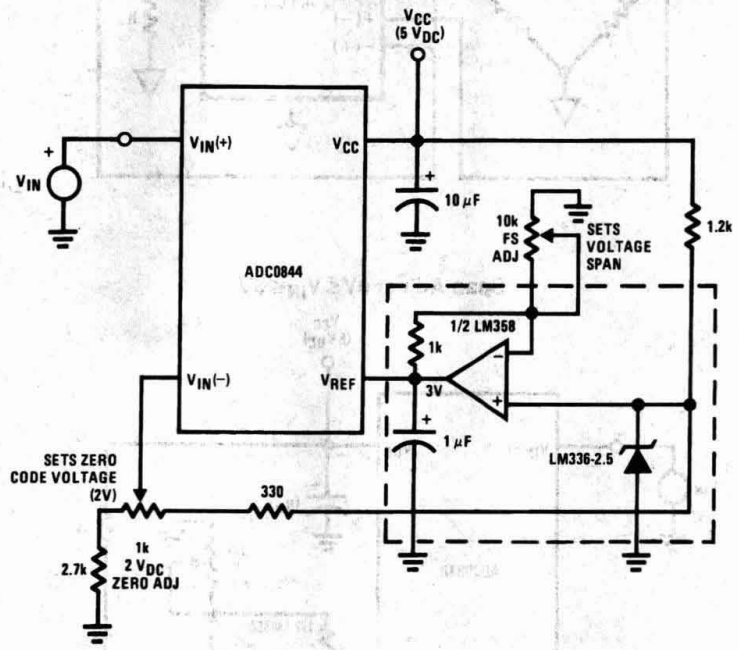
$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX}-V_{MIN})}{256}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

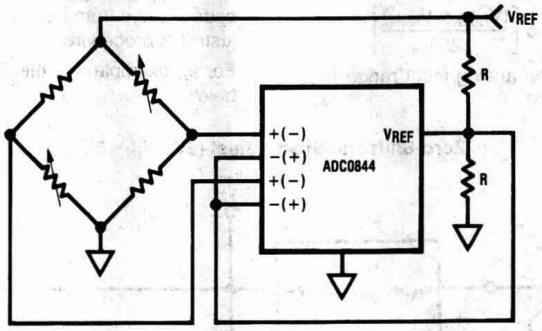
Zero-Shift and Span Adjust ($2V \leq V_{IN} \leq 5V$)



TL/H/5016–18

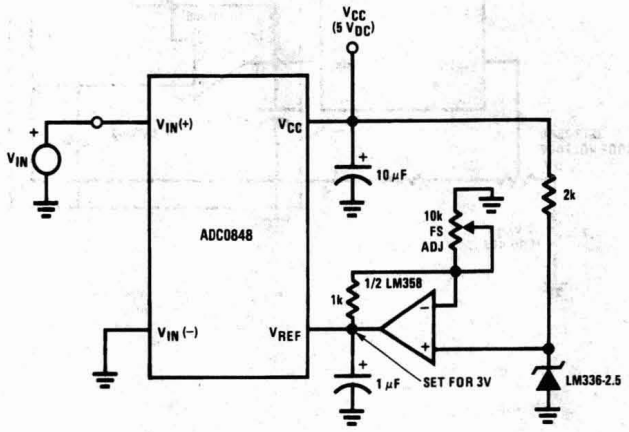
Applications Information (Continued)

Differential Voltage Input 9-Bit A/D



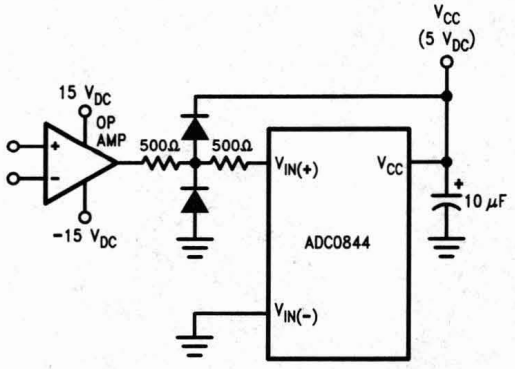
TL/H/5016–19

Span Adjust $0V \leq V_{IN} \leq 3V$



TL/H/5016–20

Protecting the Input

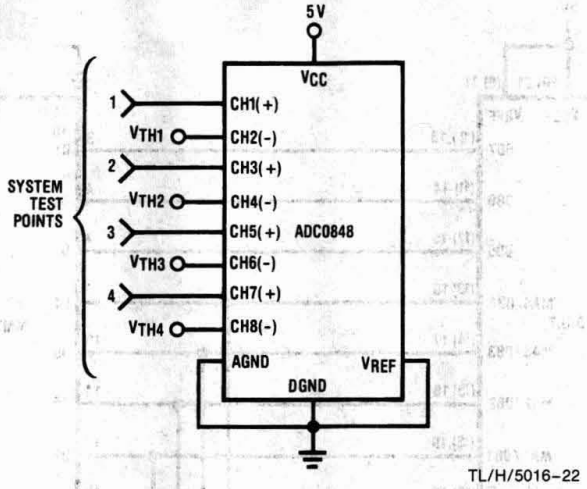


TL/H/5016–21

Diodes are 1N914

Applications Information (Continued)

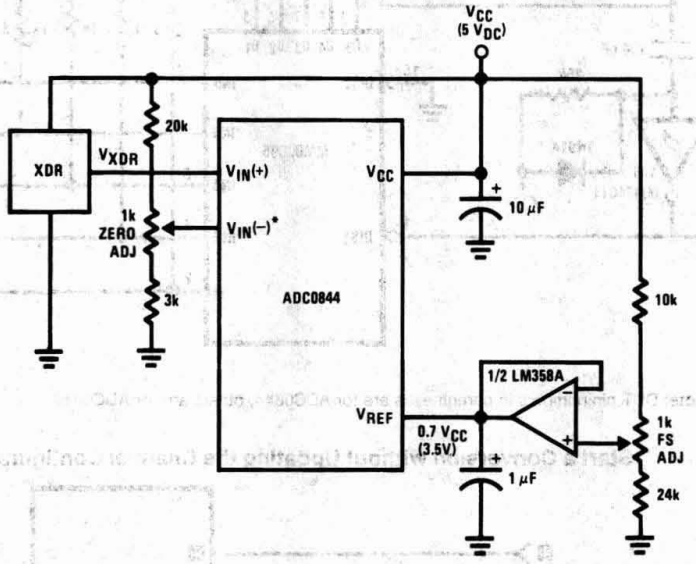
High Accuracy Comparators



TL/H/5016-22

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$
DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

Operating with Automotive Ratiometric Transducers

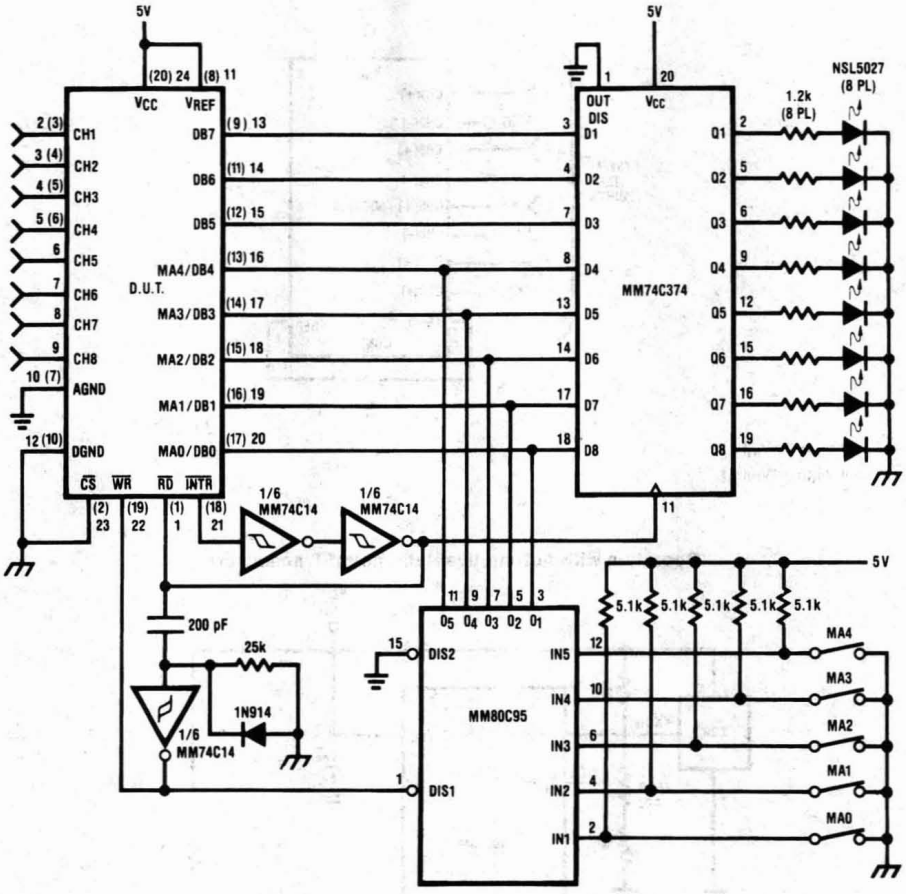


TL/H/5016-23

*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Applications Information (Continued)

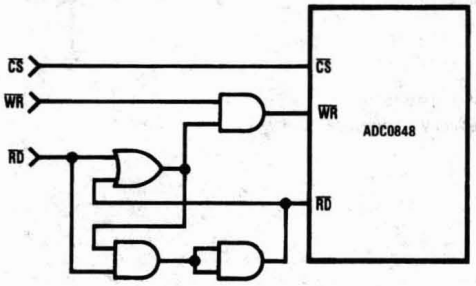
A Stand Alone Circuit



TL/H/5016–25

Note: DUT pin numbers in parentheses are for ADC0844, others are for ADC0848.

Start a Conversion without Updating the Channel Configuration



TL/H/5016–26

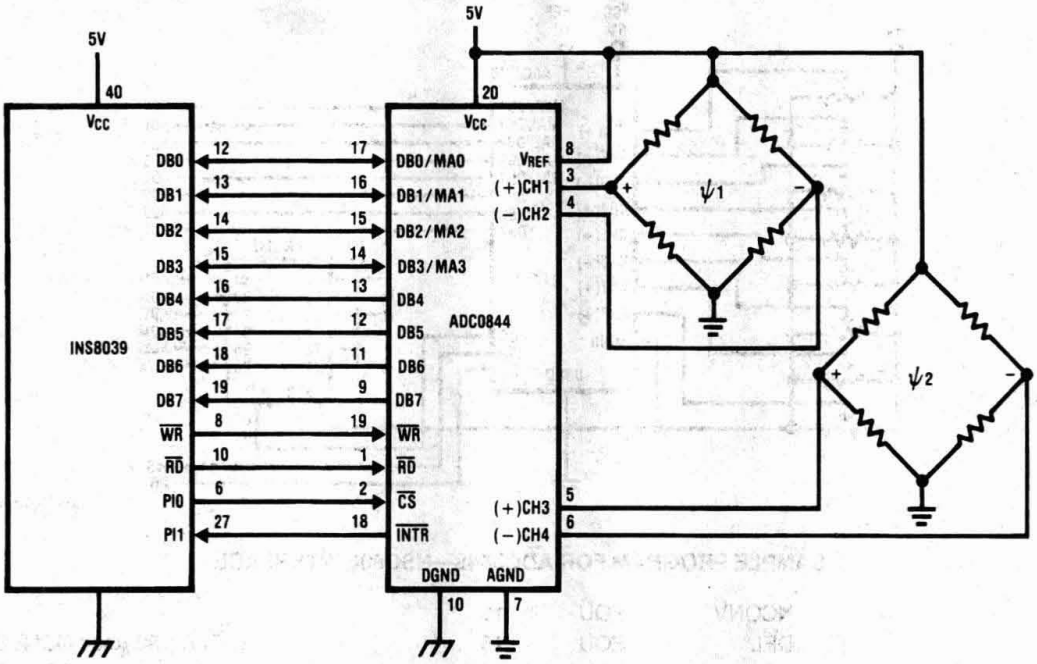
$\overline{CS}$•$\overline{WR}$ will update the channel configuration and start a conversion.

$\overline{CS}$•$\overline{RD}$ will read the conversion data and start a new conversion without updating the channel configuration.

Waiting for the end of this conversion is not necessary. A $\overline{CS}$•$\overline{WR}$ can immediately follow the $\overline{CS}$•$\overline{RD}$.

Applications Information (Continued)

ADC0844—INS8039 Interface



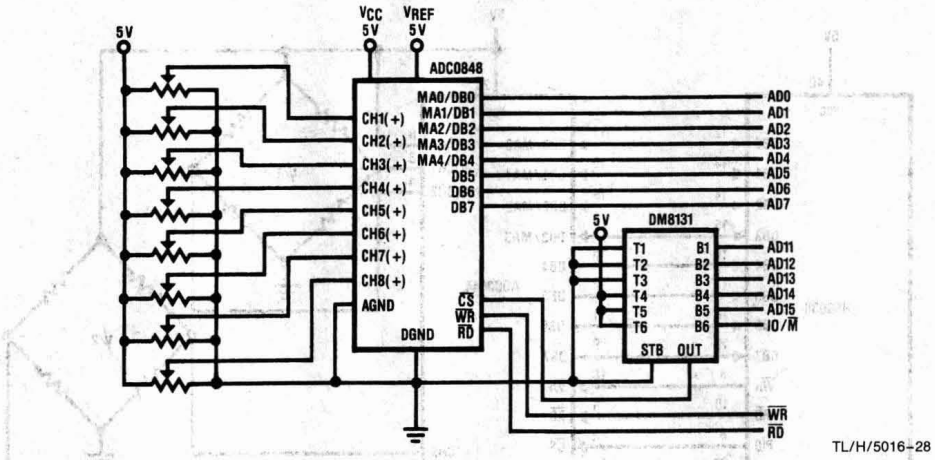
TL/H/5016–27

SAMPLE PROGRAM FOR ADC0844—INS8039 INTERFACE
CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

```
                        ORG     0H
0000    04 10           JMP     BEGIN     ;START PROGRAM AT ADDR 10
                        ORG     10H       ;MAIN PROGRAM
0010    B9 FF   BEGIN:  MOV     R1,#0FFH  ;LOAD R1 WITH A UNUSED ADDR
                                          ;LOCATION
0012    B8 20           MOV     R0,#20H   ;A/D DATA ADDRESS
0014    89 FF           ORL     P1,#0FFH  ;SET PORT 1 OUTPUTS HIGH
0016    23 00           MOV     A,00H     ;LOAD THE ACC WITH A/D MUX DATA
                                          ;CH1 AND CH2 DIFFERENTIAL
0018    14 50           CALL    CONV      ;CALL THE CONVERSION SUBROUTINE
001A    23 02           MOV     A,#02H    ;LOAD THE ACC WITH A/D MUX DATA
                                          ;CH3 AND CH4 DIFFERENTIAL
001C    18              INC     R0        ;INCREMENT THE A/D DATA ADDRESS
001D    14 50           CALL    CONV      ;CALL THE CONVERSION SUBROUTINE

                        ;CONTINUE MAIN PROGRAM

                        ;CONVERSION SUBROUTINE
                        ;ENTRY:ACC—A/D MUX DATA
                        ;EXIT: ACC—CONVERTED DATA

                        ORG     50H
0050    99 FE   CONV:   ANL     P1,#0FEH  ;CHIP SELECT THE A/D
0052    91              MOVX    @R1,A     ;LOAD A/D MUX & START CONVERSION
0053    09      LOOP:   IN      A,P1      ;INPUT INTR STATE
0054    32 53           JB1     LOOP      ;IF INTR = 1 GOTO LOOP
0056    81              MOVX    A,@R1     ;IF INTR = 0 INPUT A/D DATA
0057    89 01           ORL     P1,&01H   ;CLEAR THE A/D CHIP SELECT
0059    A0              MOV     @R0,A     ;STORE THE A/D DATA
005A    83              RET               ;RETURN TO MAIN PROGRAM
```

Applications Information (Continued)

I/O Interface to NSC800



TL/H/5016–28

SAMPLE PROGRAM FOR ADC0848—NSC800 INTERFACE

```
0008                    NCONV   EQU     16
000F                    DEL     EQU     15          ;DELAY 50 μsec CONVERSION
001F                    CS      EQU     1FH         ;THE BOARD ADDRESS
3C00                    ADDTA   EQU     003CH       ;START OF RAM FOR A/D
                                                    ;DATA
0000'  08 09 0A 0B      MUXDTA: DB      08H,09H,0AH,0BH ;MUX DATA
0004'  0C 0D 0E 0F              DB      0CH,0DH,0EH,0FH
0008'  0E 1F            START:  LD      C,CS
000A'  06 16                    LD      B,NCONV
000C'  21 0000'                 LD      HL,MUXDTA
000F'  11 003C                  LD      DE,ADDTA
0012'  ED A3            STCONV: OUTI                ;LOAD A/D'S MUX DATA
                                                    ;AND START A CONVERSION
0014'  EB                       EX      DE,HL       ;HL = RAM ADDRESS FOR THE
                                                    ;A/D DATA
0015'  3E 0F                    LD      A,DEL
0017'  3D               WAIT:   DEC     A           ;WAIT 50 μsec FOR THE
0018'  C2 0013'                 JP      NZ,WAIT     ;CONVERSION TO FINISH
001B'  ED A2                    INI                 ;STORE THE A/D'S DATA
                                                    ;CONVERTED ALL INPUTS?
001D'  EB                       EX      DE,HL
001E'  C2 000E'                 JP      NZ,STCONV   ;IF NOT GOTO STCONV

                                END
```

Note: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH8 a conversion is started, then a 50 μs wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.

Ordering Information

Temperature Range	Total Unadjusted Error		MUX Channels	Package Outline
	±½ LSB	±1 LSB		
0°C to +70°C	ADC0844BCN	ADC0844CCN	4	N20A Molded Dip
	ADC0848BCN	ADC0848CCN	8	N24C Molded Dip
−40°C to +85°C	ADC0844BCJ	ADC0844CCJ	4	J20A Cerdip
	ADC0848BCJ	ADC0848CCJ	8	J24F Cerdip
	ADC0848BCV	ADC0848CCV	8	V28A Molded Chip Carrier

National Semiconductor

ADC0852/ADC0854
Multiplexed Comparator with 8-Bit Reference Divider

General Description

The ADC0852 and ADC0854 are CMOS devices that combine a versatile analog input multiplexer, voltage comparator, and an 8-bit DAC which provides the comparator's threshold voltage (V_{TH}). The comparator provides a "1-bit" output as a result of a comparison between the analog input and the DAC's output. This allows for easy implementation of set-point, on-off or "bang-bang" control systems with several advantages over previous devices.

The ADC0854 has a 4 input multiplexer that can be software configured for single ended, pseudo-differential, and full-differential modes of operation. In addition the DAC's reference input is brought out to allow for reduction of the span.

The ADC0852 has a two input multiplexer that can be configured as 2 single-ended or 1 differential input pair. The DAC reference input is internally tied to V_{CC}.

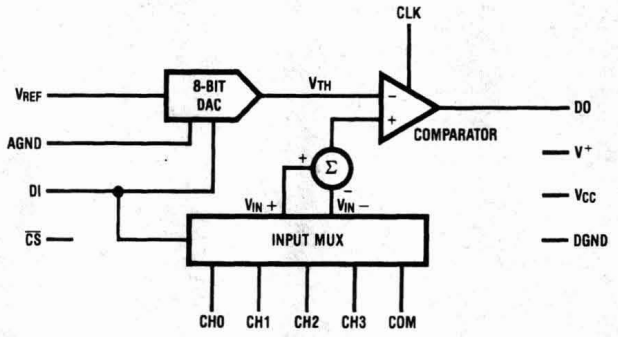
The multiplexer and 8-bit DAC are programmed via a serial data input word. Once programmed the output is updated once each clock cycle up to a maximum clock rate of 400 kHz.

Features

- 2 or 4 channel multiplexer
- Differential or Single-ended input, software controlled
- Serial digital data interface
- 256 programmable reference voltage levels
- Continuous comparison after programming
- Fixed, ratiometric, or reduced span reference capability (ADC 0854)

Key Specifications

- Accuracy, ± ½ LSB or ± 1 LSB of Reference (0.2%)
- Single 5V power supply
- Low Power, 15 mW



TL/H/5521–1

FIGURE 1. ADC0854 Simplified Block Diagram (ADC0852 has 2 input channels, COM tied to GND, V_{REF} tied to V_{CC}, V+ omitted, and one GND connection)

2 Channel and 4 Channel Pin Out

ADC0852 2-CHANNEL MUX
Dual-In-Line Package

TL/H/5521–10

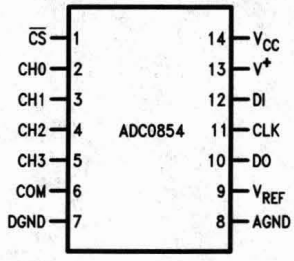
Top View

AGND and COM internally connected to GND

V_{REF} internally connected to V_{CC}

Order Number ADC0852
See NS Package Number N08E

ADC0854 4-CHANNEL MUX
Dual-In-Line Package



TL/H/5521–11

Top View

Order Number ADC0854
See NS Package Number N14A

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic and Analog Inputs	−0.3V to V_{CC} +0.3V
Input Current per Pin	±5 mA
Input Current per Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
ESD Susceptibility (Note 14)	2000V

Operating Conditions

Supply Voltage, V_{CC}	$4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0854CCN, ADC0852CCN	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for V_{CC} = V+ = 5V (no V+ on ADC0852), $V_{REF} \le V_{CC}$ + 0.1V, f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Parameter	Conditions	ADC0852CCN ADC0854CCN			Units
		Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error (Note 7) ADC0852/4/CCN	V_{REF} Forced to 5.000 V_{DC}		±1	**±1**	LSB
Comparator Offset ADC0852/4/CCN		2.5		**20**	mV
Minimum Total Ladder Resistance	ADC0854 (Note 15)	3.5	1.3	**1.3**	kΩ
Maximum Total Ladder Resistance	ADC0854 (Note 15)	3.5	5.4	**5.9**	kΩ
Minimum Common-Mode Input (Note 8)	All MUX Inputs and COM Input		GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input (Note 8)	All MUX Inputs and COM Input		V_{CC} + 0.05	**V_{CC} + 0.05**	V
DC Common-Mode Error		±1/16	±¼	±¼	LSB
Power Supply Sensitivity	V_{CC} = 5V ±5%	±1/16	±¼	±¼	LSB
V_Z, Internal diode breakdown at V+ (Note 3)	15 mA into V+				
MIN			6.3		V
MAX			8.5		V
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		−200	**−1**	µA nA
	On Channel = 0V, Off Channel = 5V		+200	**+1**	µA nA

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V^+ = 5V$ (no V^+ on ADC0852), $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	ADC0852CCN ADC0854CCN			Units
		Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		+200	**+1**	μA nA
	On Channel = 0V, Off Channel = 5V		−200	**−1**	μA nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$		2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$		0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$	0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$	−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 2.4 4.5	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75V$		0.4	**0.4**	V
I_{OUT}, TRI-STATE® Output Current (DO)	$\overline{CS}$ = Logical "1" $V_{OUT} = 0.4V$ $V_{OUT} = 5V$	 −0.1 0.1	 −3 3	 **−3** **3**	 μA μA
I_{SOURCE}	V_{OUT} Short to GND	−14	−7.5	**−6.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}	16	9.0	**8.0**	mA
I_{CC} Supply Current ADC0852	Includes DAC Ladder Current	2.7	6.5	**6.5**	mA
I_{CC} Supply Current ADC0854 (Note 3)	Does not Include DAC Ladder Current	0.9	2.5	**2.5**	mA

AC Characteristics $t_r = t_f = 20$ ns, $T_A = 25°C$

Symbol	Parameter		Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
f_{CLK}	Clock Frequency (Note 12)	MIN MAX			10	 400	kHz kHz
t_{D1}	Rising Edge of Clock to "DO" Enabled		C_L = 100 pF	650		1000	ns
t_r	Comparator Response Time (Note 13)		Not Including Addressing Time			2 + 1 μs	$1/f_{CLK}$
	Clock Duty Cycle (Note 10)	MIN MAX			40 60		% %
t_{SET-UP}	CS Falling Edge or Data Input Valid to CLK Rising Edge	MAX				250	ns
t_{HOLD}	Data Input Valid after CLK Rising Edge	MIN				90	ns
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 11)	MAX	C_L = 100 pF	650		1000	ns
t_{1H}, t_{0H}	Rising Edge of CS to Data Output Hi-Z	MAX	C_L = 10 pF, R_L = 10k C_L = 100 pF, R_L = 2k (see TRI-STATE Test Circuits)	125	 500	250 500	ns ns
C_{IN}	Capacitance of Logic Input			5			pF
C_{OUT}	Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Internal zener diodes (approx. 7V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode ensures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+.

Note 4: Typicals are at 25°C and represent most likely parametric norm.

Note 5: Tested and guaranteed to National AOQL (Average Outgoing Quality Level).

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Total unadjusted error includes comparator offset, DAC linearity, and multiplexer error. It is expressed in LSBs of the threshold DAC's input code.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the output will be 0. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range ensures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits then 1.6 μS ≤ CLK Low ≤ 60 μS and 1.6 μS ≤ CLK HIGH ≤ ∞.

Note 11: With $\overline{CS}$ low and programming complete, D0 is updated on each falling CLK edge. However, each new output is based on the comparison completed 0.5 clock cycles prior (see *Figure 5*).

Note 12: Error specs are not guaranteed at 400 kHz (see graph: Comparator Error vs. f_{CLK}).

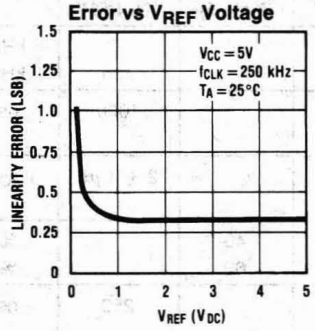
Note 13: See text, section 1.2.

Note 14: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

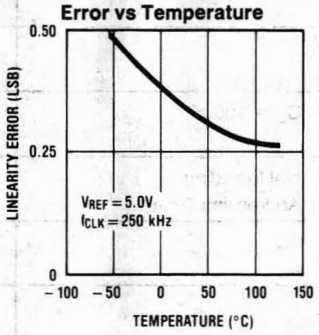
Note 15: Because the reference ladder of the ADC0852 is internally connected to V_{CC}, ladder resistance cannot be directly tested for the ADC0852. Ladder current is included in the ADC0852's supply current specification.

Typical Performance Characteristics

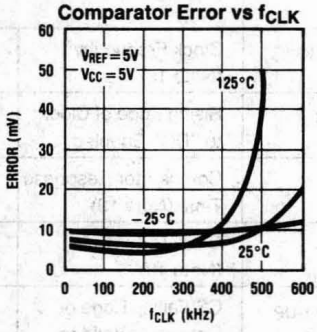
Internal DAC Linearity Error vs V_{REF} Voltage



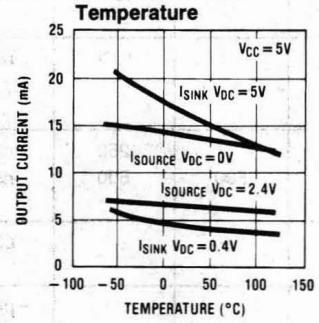
Internal DAC Linearity Error vs Temperature



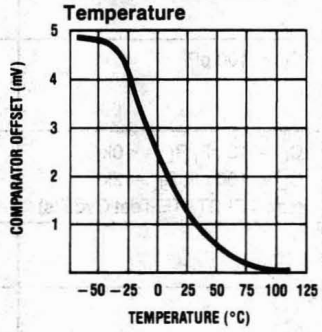
Comparator Error vs f_{CLK}



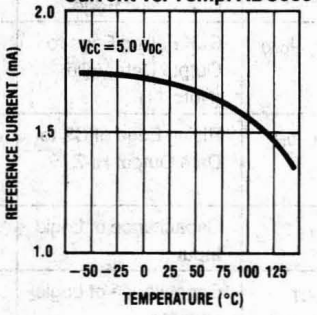
Output Current vs Temperature



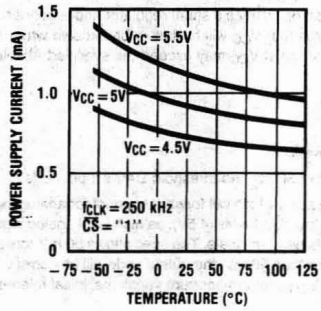
Comparator Offset vs Temperature



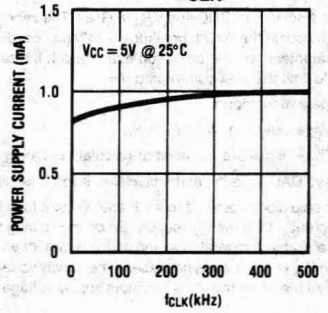
I_{REF}, Reference Current vs. Temp. ADC0854



I_{CC}, Power Supply Current vs. Temperature, ADC0854*



I_{CC}, Power Supply Current vs. f_{CLK}, ADC0854*



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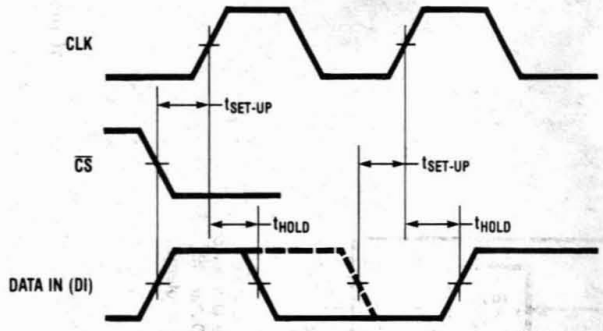
*For ADC0852 add I_{REF}

Timing Diagrams

Data Input Timing



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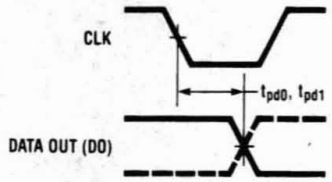
Data Output Timing



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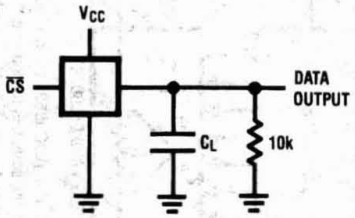
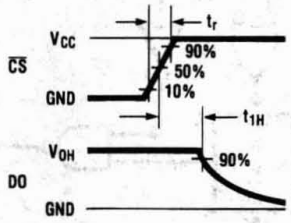
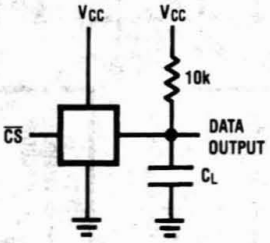
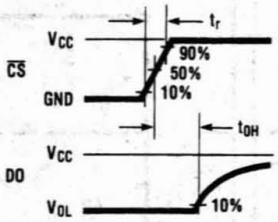
TRI-STATE Test Circuits and Waveforms









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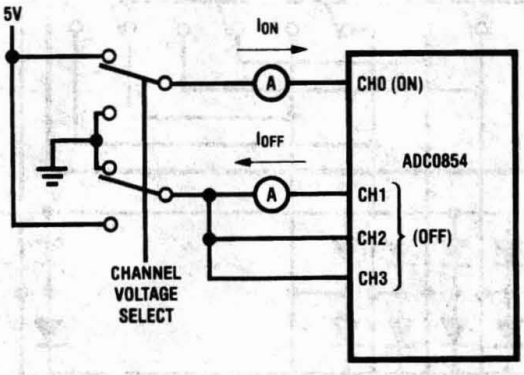
Leakage Test Circuit



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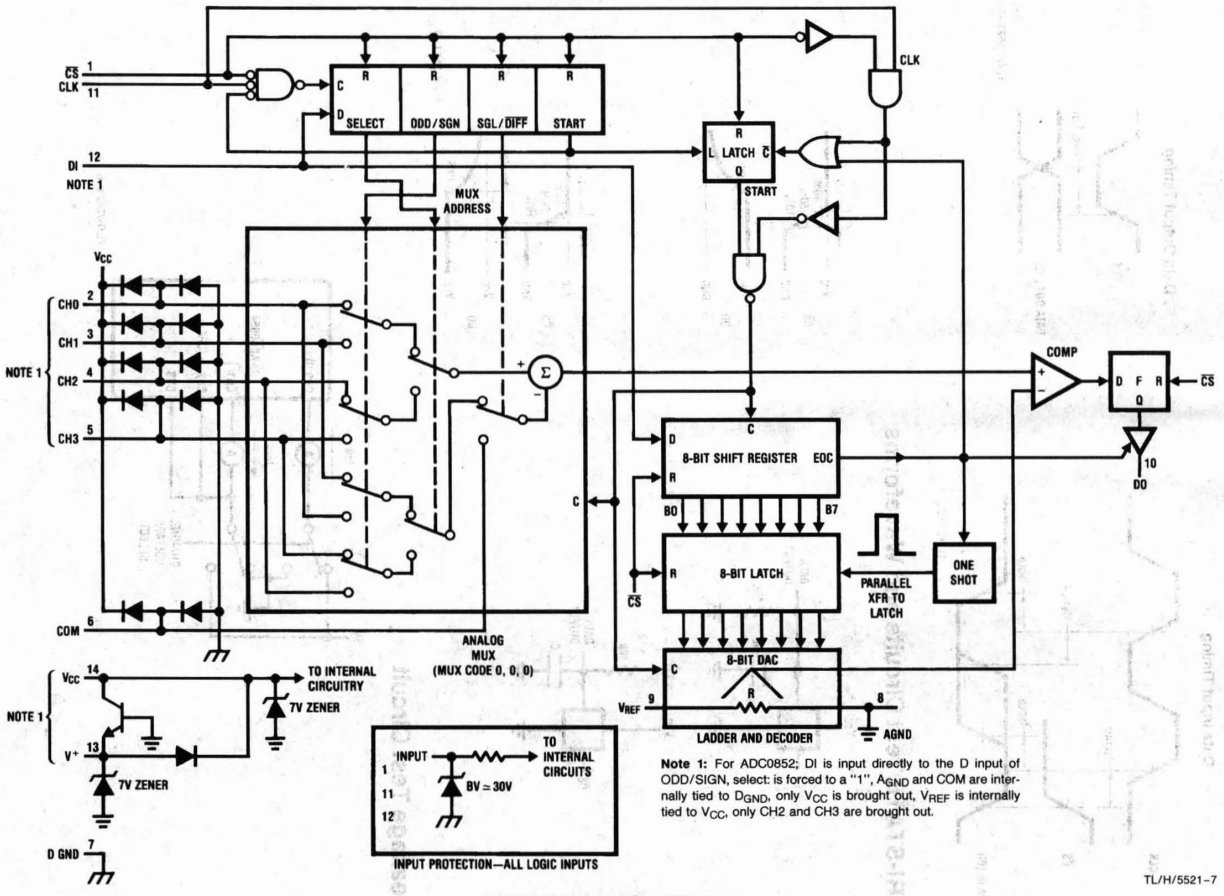

Note 1: For ADC0852; DI is input directly to the D input of ODD/SIGN, select: is forced to a "1", A_{GND} and COM are internally tied to D_{GND}, only V_{CC} is brought out, V_{REF} is internally tied to V_{CC}, only CH2 and CH3 are brought out.

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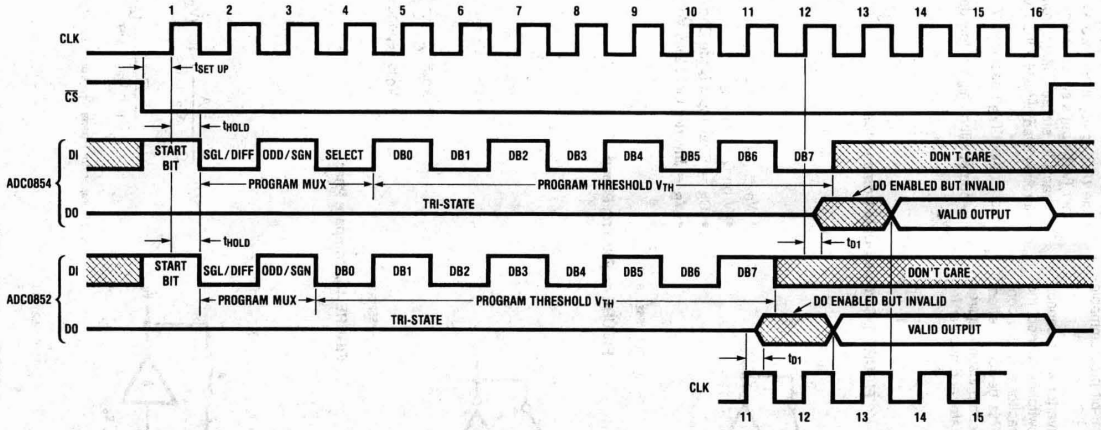
FIGURE 2. Detailed Block Diagram



Note: Valid Output can change only on Falling Edge of CLK.

FIGURE 3. Timing Diagram

Functional Description

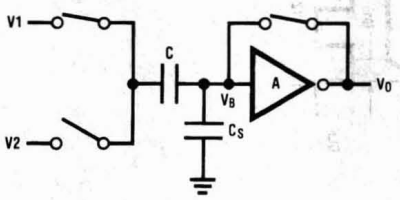
1. 1 The Sampled-data Comparator

The ADC0852 and ADC0854 utilize a sampled-data comparator structure to compare the analog difference between a selected "+" and "−" input to an 8-bit programmable threshold.

This comparator consists of a CMOS inverter with a capacitively coupled input (*Figure 4*). Analog switches connect the two comparator inputs to the input capacitor and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator and another for making the comparison.

In the first cycle (*Figure 4a*), one input switch and the inverter's feedback switch are closed. In this interval, the input capacitor (C) is charged to the connected input (V1) less the inverter's bias voltage (V_B, approx. 1.2 volts). In the second cycle (*Figure 4b*) these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter input (V_B') becomes $V_B - (V1 - V2)\frac{C}{C + C_S}$ and the output will go high or low depending on the sign of V_B'-V_B.

FIGURE 4. Sampled-Data Comparator



- $V_O = V_B$
- V on C = $V_1 - V_B$
- C_S = Stray Input Node Cap.
- V_B = Inverter Input Bias Voltage

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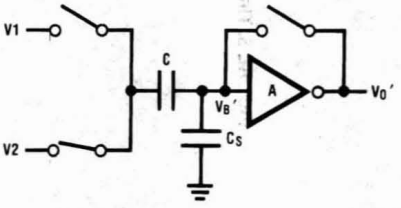
FIGURE 4a. Zeroing Phase



- $V_{B'} - V_B = (V_2 - V_1)\frac{C}{C + C_S}$
- $V_O = \frac{-A}{C + C_S}[CV_2 - CV_1]$
- V_O is dependent on $V_2 - V_1$

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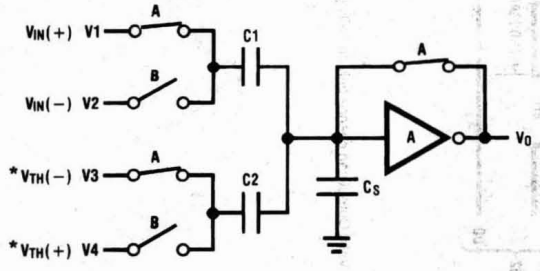
FIGURE 4b. Compare Phase



$$V_O = \frac{-A}{C_1 + C_2 + C_S}[C_1(V_2 - V_1) + C_2(V_4 - V_3)]$$

$$= \frac{-A}{C_1 + C_2 + C_S}[\Delta Q C_1 + \Delta Q C_2]$$

* Comparator Reads V_{TH} from Internal DAC Differentially

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FIGURE 4c. Multiple Differential Inputs

Functional Description (Continued)

In actual practice, the devices used in the ADC0852/4 are a simple but important expansion of the basic comparator described above. As shown in *Figure 4c*, multiple differential comparisons can be made. In this circuit, the feedback switch and one input switch on each capacitor (A switches) are closed in the first cycle. Then the other input on each capacitor is connected while all of the first switches are opened. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor (C1, C2), will now depend on both input signal differences.

1.2 Input Sampling and Response Time

The input phases of the comparator relate to the device clock (CLK) as shown in *Figure 5*. Because the comparator is a sampling device, its response characteristics are somewhat different from those of linear comparators. The $V_{IN}(+)$ input is sampled first (CLK high) followed by $V_{IN}(-)$ (CLK low). The output responds to those inputs, one half cycle later, on CLK's falling edge.

The comparator's response time to an input step is dependent on the step's phase relation to the CLK signal. If an input step occurs too late to influence the most imminent comparator decision, one more CLK cycle will pass before the output is correct. In effect, the response time for the $V_{IN}(+)$ input has a minimum of 1 CLK cycle + 1 μS and a maximum of 2 CLK cycles + 1 μS. The $V_{IN}(-)$ input's delay will range from 1/2 CLK cycle + 1 μS to 1.5 CLK cycles + 1 μS since it is sampled after $V_{IN}(+)$.

The sampled inputs also affect the device's response to pulsed signals. As shown in the shaded areas in *Figure 5*, pulses that rise and/or fall near the latter part of a CLK half-cycle may be ignored.

1.3 Input Multiplexer

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential operation. The analog signal conditioning required in transducer-input and other types of data acquisition systems is significantly simplified with this type of input flexibility. One device package can now handle ground referenced inputs as well as signals with some arbitrary reference voltage.

On the ADC0854, the "common" pin (pin 6) is used as the "−" input for all channels in single-ended mode. Since this input need not be at analog ground, it can be used as the common line for pseudo-differential operation. It may be tied to a reference potential that is common to all inputs and within the input range of the comparator. This feature is especially useful in single-supply applications where the analog circuitry is biased to a potential other than ground.

A particular input configuration is assigned during the MUX addressing sequence which occurs prior to the start of a comparison. The MUX address selects which of the analog channels is to be enabled, what the input mode will be, and the input channel polarity. One limitation is that differential inputs are restricted to adjacent channel pairs. For example, channel 0 and 1 may be selected as a differential pair but they cannot act differentially with any other channel.

The channel and polarity selection is done serially via the DI input. A complete listing of the input configurations and corresponding MUX addresses for the ADC0852 and ADC0854 is shown in tables I and II. *Figure 6* illustrates the analog connections for the various input options.

The analog input voltage for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading accuracy.

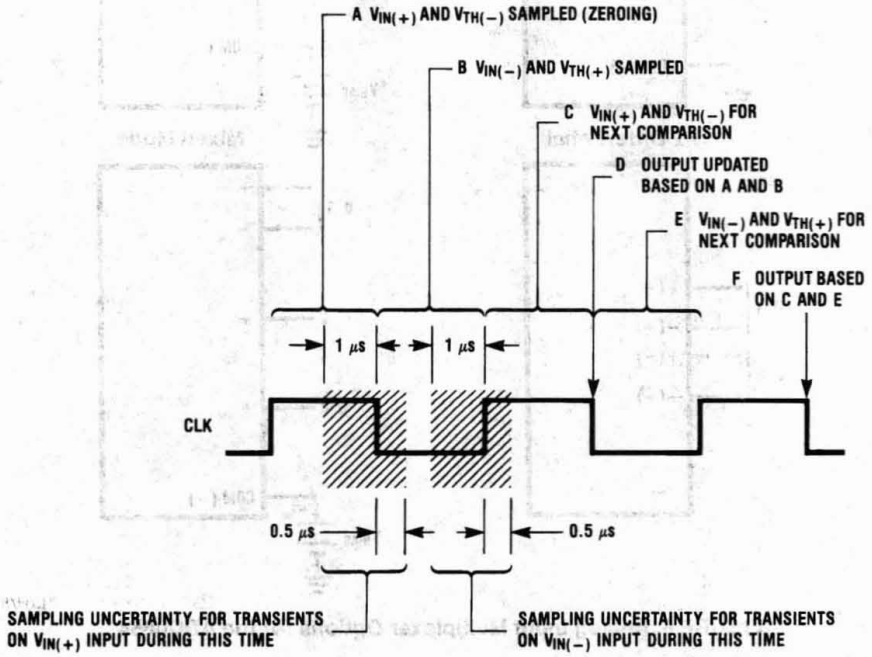
A VIN(+) AND VTH(−) SAMPLED (ZEROING)
B VIN(−) AND VTH(+) SAMPLED
C VIN(+) AND VTH(−) FOR NEXT COMPARISON
D OUTPUT UPDATED BASED ON A AND B
E VIN(−) AND VTH(+) FOR NEXT COMPARISON
F OUTPUT BASED ON C AND E
1 µs
1 µs
CLK
0.5 µs
0.5 µs
SAMPLING UNCERTAINTY FOR TRANSIENTS ON VIN(+) INPUT DURING THIS TIME
SAMPLING UNCERTAINTY FOR TRANSIENTS ON VIN(−) INPUT DURING THIS TIME

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FIGURE 5. Analog Input Timing

Functional Description (Continued)

TABLE I. MUX Addressing: ADC0854
Single-Ended MUX Mode

MUX Address			Channel				
SGL/$\overline{DIF}$	ODD/SIGN	SELECT	0	1	2	3	COM
1	0	0	+				−
1	0	1			+		−
1	1	0		+			−
1	1	1				+	−

Differential MUX Mode

MUX Address			Channel			
SGL/$\overline{DIF}$	ODD/SIGN	SELECT	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE II. MUX Addressing: ADC0852
Single Ended MUX Mode

MUX Address		Channel	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel	
SGL/$\overline{DIF}$	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

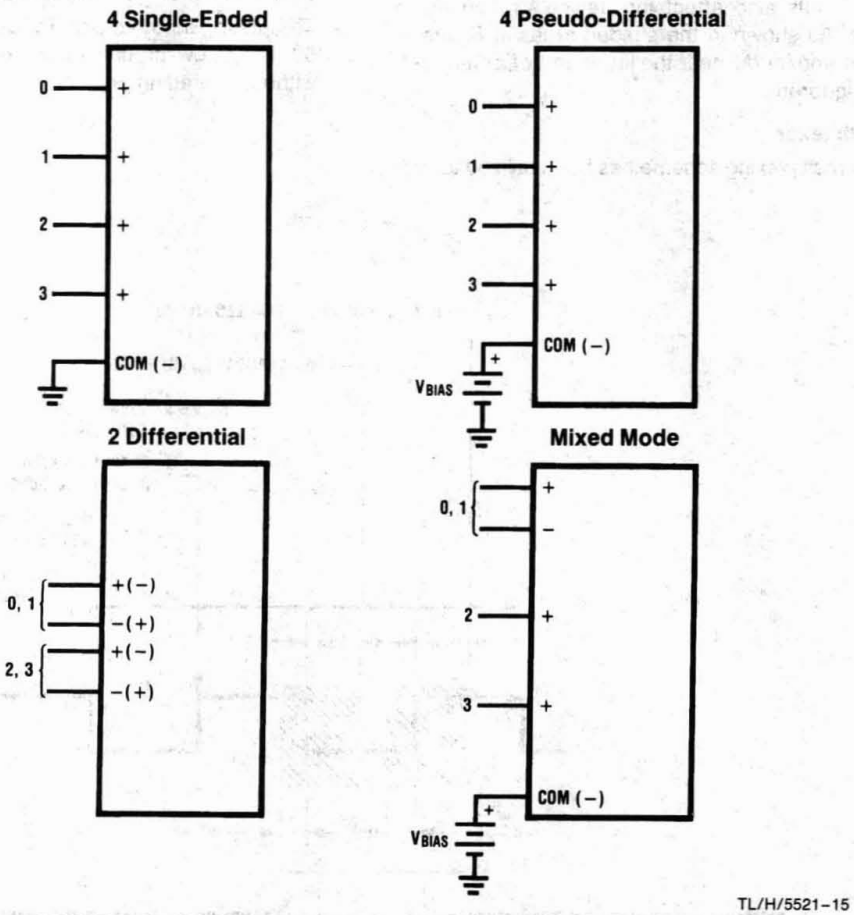

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FIGURE 6. Analog Input Multiplexer Options for the ADC0854

Functional Description (Continued)

2.0 THE DIGITAL INTERFACE

An important characteristic of the ADC0852 and ADC0854 is their serial data link with the controlling processor. A serial communication format eliminates the transmission of low level analog signals by locating the comparator close to the signal source. Thus only highly noise immune digital signals need to be transmitted back to the host processor.

To understand the operation of these devices it is best to refer to the timing diagrams (*Figure 3*) and functional block diagram (*Figure 2*) while following a complete comparison sequence.

1. A comparison is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire addressing sequence and comparison. The comparator then waits for a start bit, its MUX assignment word, and an 8-bit code to set the internal DAC which supplies the comparator's threshold voltage (V_{TH}).

2. An external clock is applied to the CLK input. This clock can be applied continuously and need not be gated on and off.

3. On each rising edge of the clock, the level present on the DI line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line. All leading zeroes are ignored. After the start bit, the ADC0852 expects the next 2 bits to be the MUX assignment word while the ADC0854, with more MUX configurations, looks for 3 bits.

4. Immediately after the MUX assignment word has been clocked in, the shift register then reads the next eight bits as the input code to the internal DAC. This eight bit word is read LSB first and is used to set the voltage applied to the comparator's threshold input (internal).

5. After the rising edge of the 11th or 12th clock (ADC0852 or ADC0854 respectively) following the start bit, the comparator and DAC programming is complete. At this point the DI line is disabled and ignores further inputs. Also at this time the data out (DO) line comes out of TRI-STATE and enters a don't care state (undefined output) for 1.5 clock cycles.

6. The result of the comparison between the programmed threshold voltage and the difference between the two selected inputs ($V_{IN}(+) - V_{IN}(-)$) is output to the DO line on each subsequent high to low clock transition.

7. After programming, continuous comparison on the same selected channel with the same programmed threshold can be done indefinitely, without reprogramming the device, as long as $\overline{CS}$ remains low. Each new comparator decision will be shifted to the output on the falling edge of the clock. However, the output will, in effect, "lag" the analog input by 0.5 to 1.5 clock cycles because of the time required to make the comparison and latch the output (see *Figure 5*).

8. All internal registers are cleared when the $\overline{CS}$ line is brought high. If another comparison is desired $\overline{CS}$ must make a high to low transition followed by new address and threshold programming.

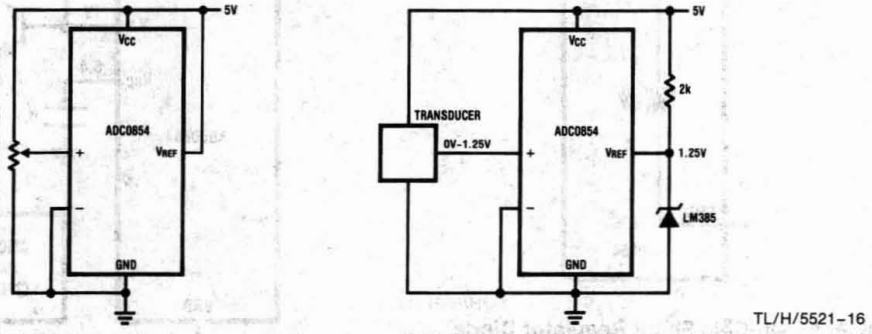
3.0 REFERENCE CONSIDERATIONS / RATIOMETRIC OPERATION

The voltage applied to the "V_{REF}" input of the DAC defines the voltage span that can be programmed to appear at the threshold input of the comparator. The ADC0854 can be used in either ratiometric applications or in systems with absolute references. The V_{REF} pin must be connected to a source capable of driving the DAC ladder resistance (typ. 2.4 kΩ) with a stable voltage.

In ratiometric systems, the analog input voltage is normally a proportion of the DAC's or A/D's reference voltage. For example, a mechanical position servo using a potentiometer to indicate rotation, could use the same voltage to drive the reference as well as the potentiometer. Changes in the value of V_{REF} would not affect system accuracy since only the relative value of these signals to each other is important. This technique relaxes the stability requirements of the system reference since the analog input and DAC reference move together, thus maintaining the same comparator output for a given input condition.

In the absolute case, the V_{REF} input can be driven with a stable voltage source whose output is insensitive to time and temperature changes. The LM385 and LM336 are good low current devices for this purpose.

The maximum value of V_{REF} is limited to the V_{CC} supply voltage. The minimum value can be quite small (see typical performance curves) allowing the effective resolution of the comparator threshold DAC to also be small (V_{REF} = 0.5V, DAC resolution = 2.0 mV). This in turn lets the designer have finer control over the comparator trip point. In such instances however, more care must be taken with regard to noise pickup, grounding, and system error sources.



a) Ratiometric

b) Absolute with a Reduced Span

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FIGURE 7. Referencing Examples

Functional Description (Continued)

4.0 ANALOG INPUTS

4. 1 Differential Inputs

The serial interface of the ADC0852 and ADC0854 allows them to be located right at the analog signal source and to communicate with a controlling processor via a few fairly noise immune digital lines. This feature in itself greatly reduces the analog front end circuitry often needed to maintain signal integrity. Nevertheless, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common mode voltage.

The differential input of the comparator actually reduces the effect of common-mode input noise, i.e. signals common to both selected "+" and "−" inputs such as 60 Hz line noise. The time interval between sampling the "+" input and then the "−" input is ½ of a clock period (see *Figure 5).*

The change in the common-mode voltage during this short time interval can cause comparator errors. For a sinusoidal common-mode signal this error is:

V_{ERROR} (MAX) = V_{PEAK} (2π f_{CM}/2 f_{CLK})

where f_{CM} is the frequency of the common-mode signal, V_{peak} is its peak voltage value, and f_{CLK} is the DAC clock frequency.

For example, 1 V_{PP} 60 Hz noise superimposed on both sides of a differential input signal would cause an error (referred to the input) of 0.75 mV. This amounts to less than 1/25 of an LSB referred to the threshold DAC, (assuming V_{REF} = 5V and f_{CLK} = 250 kHz).

4. 2 Input Currents and Filtering

Due to the sampling nature of the analog inputs, short spikes of current enter the "+" input and leave the "−" at the clock edges during a comparison. These currents decay rapidly and do not cause errors as the comparator is strobed at the end of the clock period (see *Figure 5*).

The source resistance of the analog input is important with regard to the DC leakage currents of the input multiplexer. The worst-case leakage currents of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op-amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance source be required.

4. 3 Arbitrary Analog Input/Reference Range

The total span of the DAC output and hence the comparator's threshold voltage is determined by the DAC reference. For example, if V_{REF} is set to 1 volt then the comparator's threshold can be programmed over a 0 to 1 volt range with 8 bits of resolution. From the analog input's point of view, this span can also be shifted by applying an offset potential to one of the comparator's selected analog input lines (usually "−"). This gives the designer greater control of the ADC0852/4's input range and resolution and can help simplify or eliminate expensive signal conditioning electronics.

An example of this capability is shown in the "Load Cell Limit Comparator" of *Figure 15.* In this circuit, the ADC0852 allows the load-cell signal conditioning to be done with only one dual op-amp and without complex, multiple resistor matching.

5.0 POWER SUPPLY

A unique feature of the ADC0854 is the inclusion of a 7 volt zener diode connected from the "V+" terminal to ground (*Figures 2* and *8*) "V+" also connects to "V_{CC}" via a silicon diode. The zener is intended for use as a shunt voltage regulator to eliminate the need for additional regulating components. This is especially useful if the ADC0854 is to be remotely located from the system power source.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 10* and *11.* Here this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the comparator clock. The low device current requirements and the relatively high clock frequencies used (10 kHz–400 kHz) allows use of the small value filter capacitor shown. The shunt zener regulator can also be used in this mode however this requires a clock voltage swing in excess of 7 volts. Current limiting for the zener is also needed, either built into the clock generator or through a resistor connected from the clock to V+.

Typical Applications

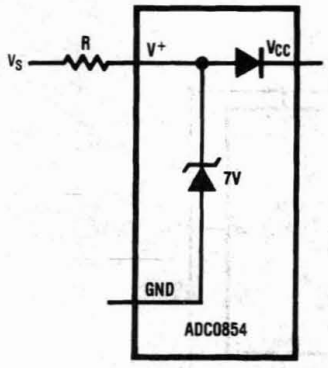

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FIGURE 8. An On-Chip Shunt Regulator Diode

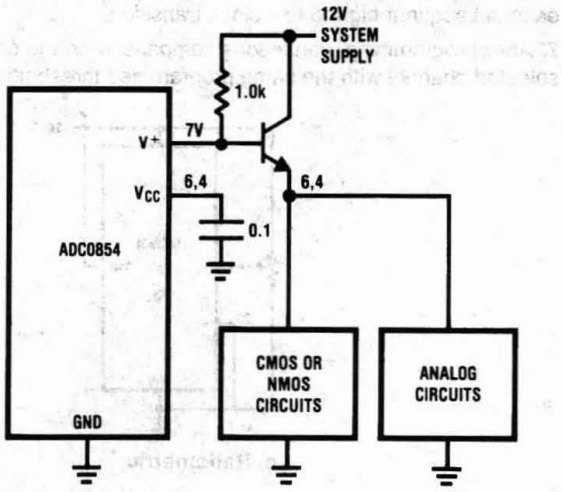

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FIGURE 9. Using the ADC0854 as the System Supply Regulator

Typical Applications (Continued)

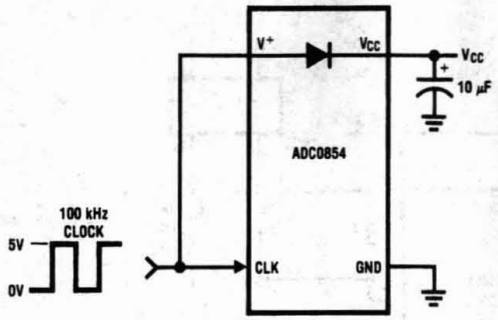

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FIGURE 10. Generating V_{CC} from the Comparator Clock

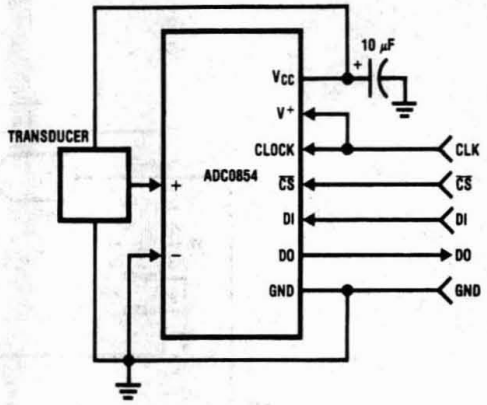

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FIGURE 11. Remote Sensing—Clock and Power on One Wire

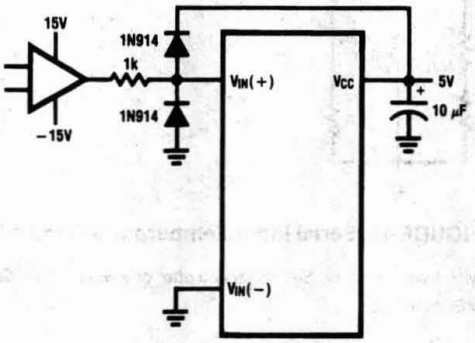

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FIGURE 12. Protecting the Analog Input

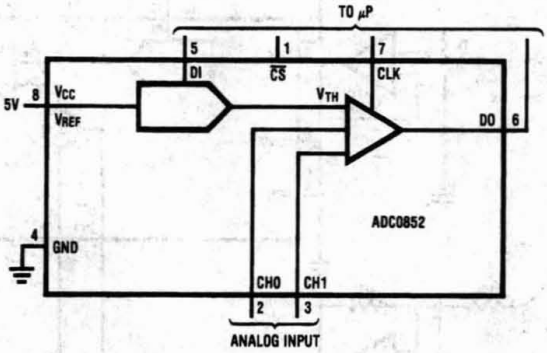

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FIGURE 13. One Component Window Comparator

Requires no additional parts. Window comparisons can be accomplished by inputting the upper and lower window limits into DI on successive comparisons and observing the two outputs:

Two high outputs → input > window

Two low outputs → input < window

One low and one high → input is within window

Typical Applications (Continued)

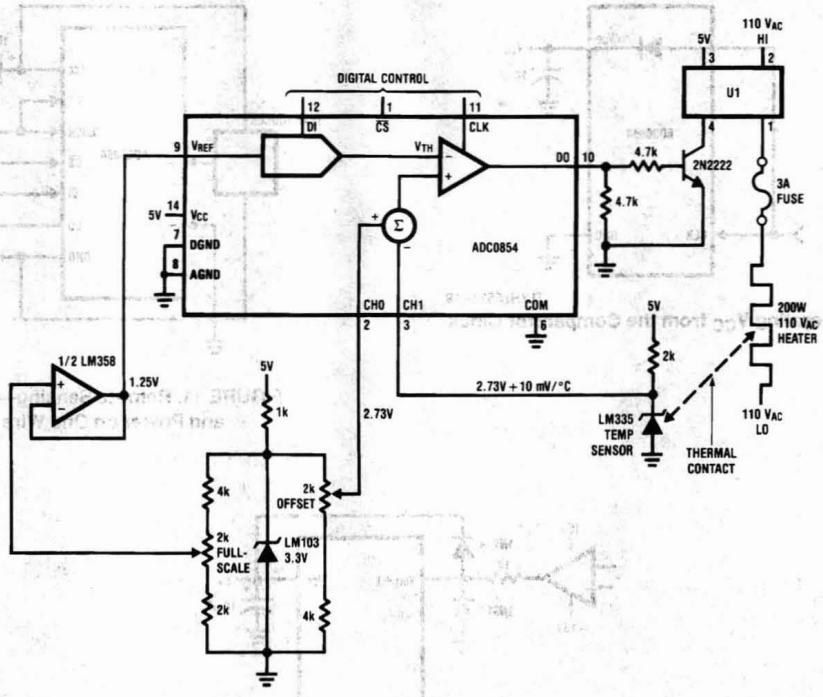

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FIGURE 14. Serial Input Temperature Controller

Note 1: ADC0854 does not require constant service from computer. Self controlled after one write to DI if $\overline{CS}$ remains low.

Note 2: U_1: Solid State Relay, Potter Brumfield #EOM1DB22

Note 3: Set Temp via. DI. Range: 0 to 125°C

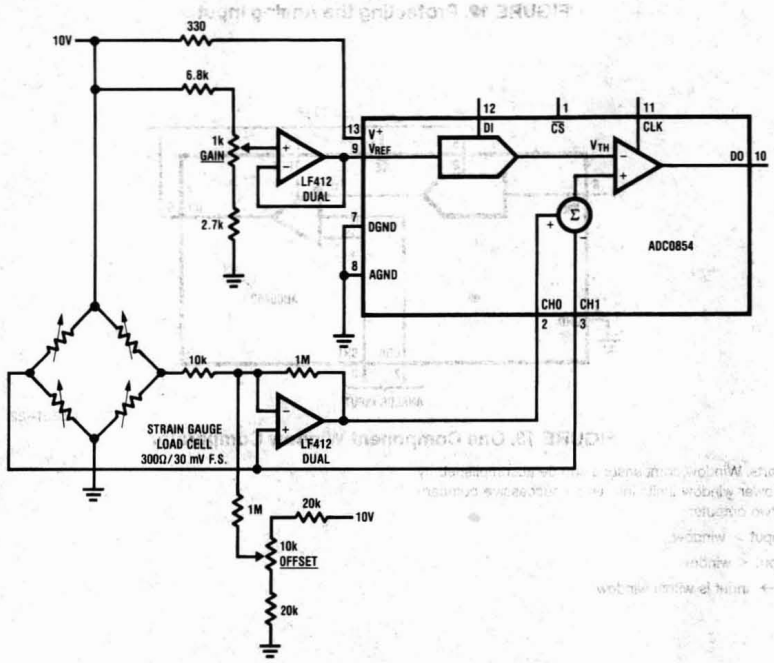

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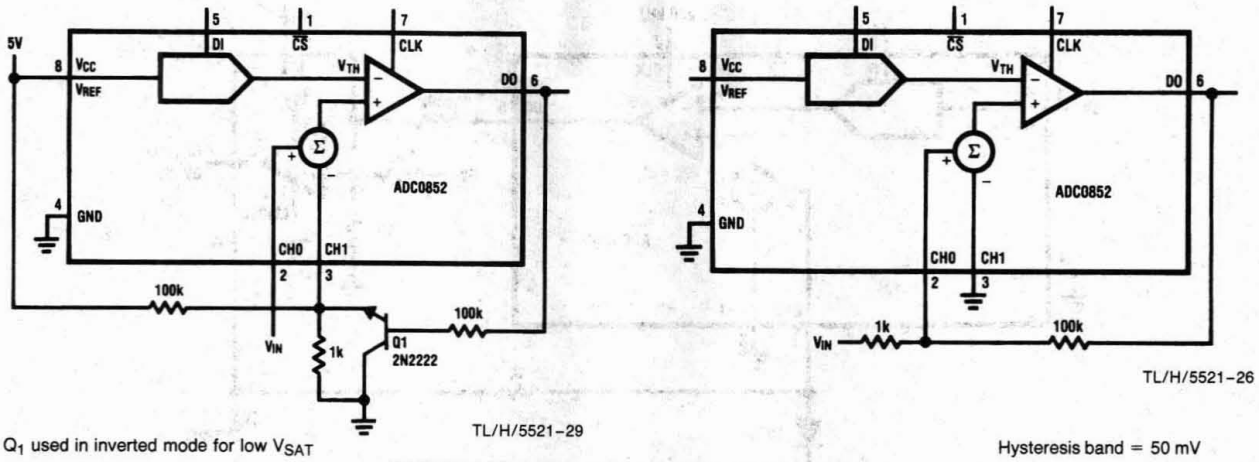
FIGURE 15. Load Cell Limit Comparator

- Differential Input elliminates need for instrumentation amplifier
- A total of 4 load cells can be monitored by ADC0854

Typical Applications (Continued)



* Q_1 used in inverted mode for low V_{SAT}

Hysteresis band = 50 mV

FIGURE 16. Adding Comparator Hysteresis

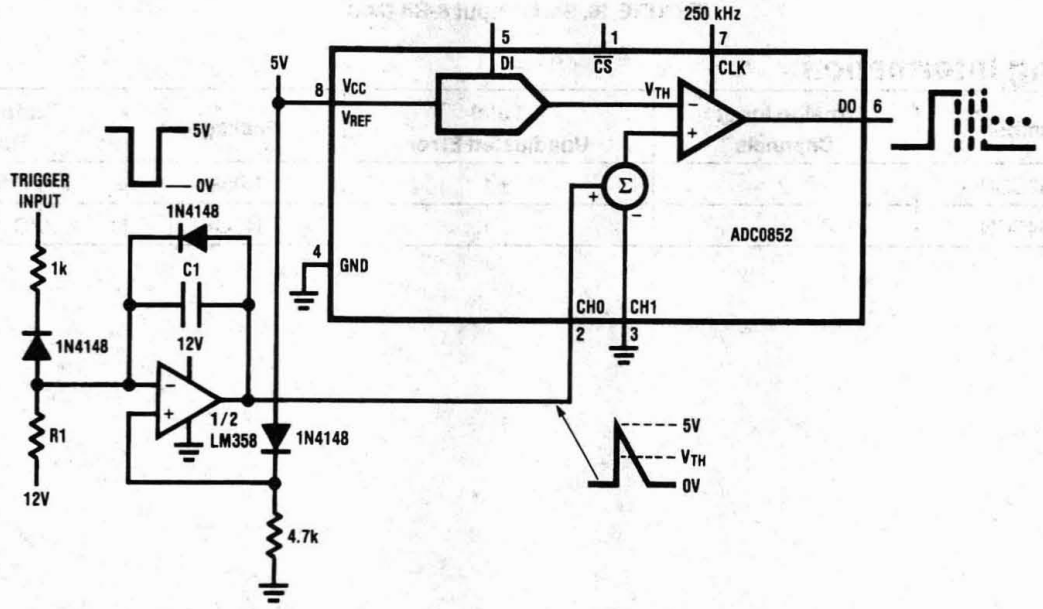


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FIGURE 17. Pulse-Width Modulator

- Range of pulse-widths controlled via R_1, C_1

Typical Applications (Continued)

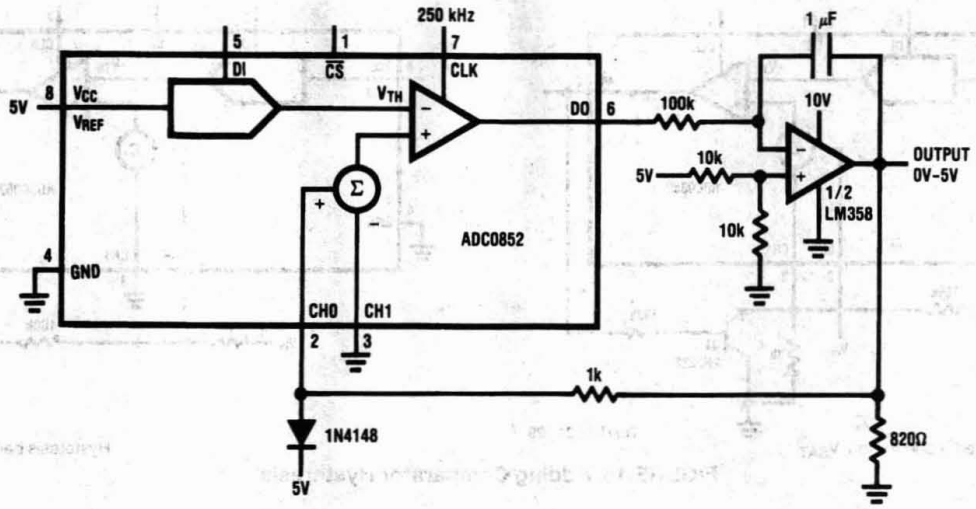

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FIGURE 18. Serial Input 8-Bit DAC

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0852CCN	2	±1	N08E	0°C to 70°C
ADC0854CCN	4	±1	N14A	0°C to 70°C

National Semiconductor

ADC08061/ADC08062
500 ns A/D Converter with S/H Function and Input Multiplexer

General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08061 and ADC08062 CMOS ADCs offer 500 ns (typ) conversion time, internal sample-and-hold (S/H), and dissipate only 125 mW of power. The ADC08062 has a two-channel multiplexer. The ADC08061/2 family performs an 8-bit conversion using a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LSBs.

Input track-and-hold circuitry eliminates the need for an external sample-and-hold. The ADC08061/2 family performs accurate conversions of full-scale input signals that have a frequency range of DC to 300 kHz (full-power bandwidth) without need of an external S/H.

The digital interface has been designed to ease connection to microprocessors and allows the parts to be I/O or memory mapped.

Key Specifications

- Resolution — 8 bits
- Conversion Time — 560 ns max ($\overline{WR}$-$\overline{RD}$ Mode)
- **Full Power Bandwidth — 300 kHz**
- Throughput rate — 1.5 MHz
- Power Dissipation — 125 mW max
- Total Unadjusted Error — ±½ LSB and ±1 LSB

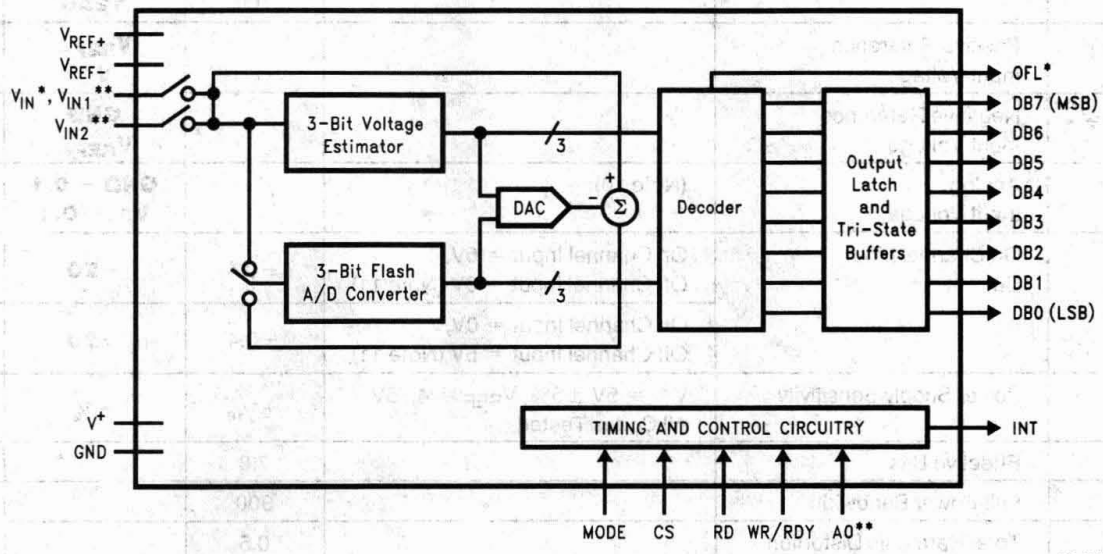
Features

- 1 or 2 input channels
- No external clock required
- Analog input voltage range from GND to V+
- Overflow output available for cascading (ADC08061)
- ADC08061 pin-compatible with the industry standard ADC0820

Applications

- Mobile telecommunications
- Hard disk drives
- Instrumentation
- High-speed data acquisition systems

Block Diagram



*ADC08061
**ADC08062

TL/H/11086–1

2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+)	6V
Logic Control Inputs	−0.3V to V^+ + 0.3V
Voltage at Other Inputs and Outputs	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	
J Package	875 mW
N Package	875 mW
WM Package	875 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Note 5)	
J Package (Soldering, 10 sec.)	+300°C
N Package (Soldering, 10 sec.)	+260°C
WM Package (Vapor Phase, 60 sec.)	+215°C
WM Package (Infrared, 15 sec.)	+220°C
ESD Susceptibility (Note 6)	2 kV

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08061/2BIN, ADC08061/2CIN, ADC08061/2BIWM, ADC08061/2CIWM	$-40°C \le T_A \le 85°C$
ADC08061CMJ, ADC08061CMJ/883	$-55°C \le T_A \le 125°C$
Supply Voltage, (V^+)	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $\overline{RD}$ Mode, $V^+ = 5V$, $V_{REF+} = 5V$, and $V_{REF-} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
INL	Integral Non Linearity	ADC08061/2 BIN, BIWM		**±½**	LSB (max)
		ADC08061/2 CIN, CIWM, CMJ		**±1**	LSB (max)
TUE	Total Unadjusted Error	ADC08061/2 BIN, BIWM		**±½**	LSB (max)
		ADC08061/2 CIN, CIWM, CMJ		**±1**	LSB (max)
	Missing Codes			**0**	Bits (max)
	Reference Input Resistance		700 700	**500** **1250**	Ω(min) Ω (max)
V_{REF+}	Positive Reference Input Voltage			**V_{REF-}** **V^+**	V (min) V (max)
V_{REF-}	Negative Reference Input Voltage			**GND** **V_{REF+}**	V (min) V (max)
V_{IN}	Analog Input Voltage	(Note 10)		**GND − 0.1** **V^+ + 0.1**	V (min) V (max)
	On Channel Input Current	On Channel Input = 5V, Off Channel Input = 0V (Note 11)	−0.4	**−20**	μA (max)
		On Channel Input = 0V, Off Channel Input = 5V (Note 11)	−0.4	**−20**	μA (max)
PSS	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.75V$ All Codes Tested	±1/16	**±½**	LSB (max)
	Effective Bits		7.8		Bits
	Full-Power Bandwidth		300		kHz
THD	Total Harmonic Distortion		0.5		%
S/N	Signal-to-Noise Ratio		50		dB
IMD	Intermodulation Distortion		50		dB

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $t_r = t_f = 10$ ns, $V_{REF+} = 5V$, $V_{REF-} = 0V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
t_{WR}	Write Time	Mode Pin to V^+; (*Figures 2a, 2b,* and *3*)	100	**100**	ns (min)
$t_{\overline{RD}}$	Read Time (Time from Falling Edge of $\overline{WR}$ to Falling Edge of $\overline{RD}$)	Mode Pin to V^+; *(Figure 2a)*	350	**350**	ns (min)
$t_{\overline{RD}W}$	$\overline{RD}$ Width	Mode Pin to GND; *(Figure 4)*	200 400	**250** **400**	ns (min) ns (max)
t_{CONV}	$\overline{WR}$-$\overline{RD}$ Mode Conversion Time ($t_{\overline{WR}} + t_{\overline{RD}} + t_{ACC1}$)	Mode Pin to V^+; *(Figure 2a)*	500	**560**	ns (max)
$t_{C\overline{RD}}$	$\overline{RD}$ Mode Conversion Time	Mode Pin to GND; *(Figure 1)*	655	**900**	ns (max)
t_{ACCO}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 100$ pF Mode Pin to GND; *(Figure 1)*	640	**900**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 10$ pF $C_L = 100$ pF Mode Pin to V^+, $t_{\overline{RD}} \leq t_{\overline{INTL}}$ *(Figure 2a)*	45 50	**110**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 10$ pF $C_L = 100$ pF $t_{\overline{RD}} > t_{\overline{INTL}}$; (*Figures 2b* and *4*)	25 30	**90**	ns (max)
t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$R_L = 3$ kΩ, $C_L = 10$ pF	30	**60**	ns (max)
t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$R_L = 3$ kΩ, $C_L = 10$ pF	30	**70**	ns (max)
$t_{\overline{INTL}}$	Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	(*Figures 2b,* and *3*) Mode Pin = V^+, $C_L = 50$ pF	520	**690**	ns (max)
$t_{\overline{INTH}}$	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF; (*Figures 1, 2a, 2b,* and *4*)	50	**95**	ns (max)
$t_{\overline{INTH}}$	Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF; *(Figure 3)*	45	**95**	ns (max)
t_{RDY}	Delay from $\overline{CS}$ to RDY	Mode Pin = 0V, $C_L = 50$ pF, $R_L = 3$ kΩ *(Figure 1)*	25	**45**	ns (max)
t_{ID}	Delay from $\overline{INT}$ to Output Valid	$R_L = 3$ kΩ, $C_L = 100$ pF; *(Figure 3)*	0	**15**	ns (max)
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$	Mode Pin = V^+, $t_{\overline{RD}} \leq t_{\overline{INTL}}$; *(Figure 2a)*	60	**115**	ns (max)
t_N	Time between End of $\overline{RD}$ and Start of New Conversion	(*Figures 1, 2a, 2b, 3* and *4*)	50	**60**	ns (min)
t_{AH}	Channel Address Hold Time	(*Figures 1, 2a, 2b, 3* and *4*)	10	**60**	ns (min)
t_{AS}	Channel Address Setup Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (max)
$t_{\overline{CSS}}$	$\overline{CS}$ Setup Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (max)
$t_{\overline{CSH}}$	$\overline{CS}$ Hold Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (min)
C_{VIN}	Analog Input Capacitance		25		pF
C_{OUT}	Logic Output Capacitance		5		pF
C_{IN}	Logic Input Capacitance		5		pF

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
V_{IH}	Logic "1" Input Voltage	$V^+ = 5.5V$			
		Mode Pin		**3.5**	V (min)
		ADC08062			
		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0 Pins		**3.0**	V (min)
		ADC08061			
		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ Pins		**2.2**	V (min)
V_{IL}	Logic "0" Input Voltage	$V^+ = 4.5V$			
		Mode Pin		**1.5**	V (max)
		ADC08062			
		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0 Pins		**0.4**	V (max)
		ADC08061			
		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ Pins		**0.7**	V (max)
I_{IH}	Logic "1" Input Current	$V_{IH} = 5V$			
		$\overline{CS}$, $\overline{RD}$, A0 Pins	0.005	**1**	μA (max)
		$\overline{WR}$ Pin	0.1	**3**	μA (max)
		Mode Pin	50	**200**	μA (max)
I_{IL}	Logic "0" Input Current	$V_{IL} = 0V$			
		$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0 Pins	−0.005		μA (max)
		Mode Pin		**−2**	
V_{OH}	Logic "1" Output Voltage	$V^+ = 4.75V$			
		$I_{OUT} = -360\ \mu A$			
		DB0–DB7, $\overline{OFL}$, $\overline{INT}$		**2.4**	V (min)
		$I_{OUT} = -10\ \mu A$			
		DB0–DB7, $\overline{OFL}$, $\overline{INT}$		**4.5**	V (min)
V_{OL}	Logic "0" Output Voltage	$V^+ = 4.75V$			
		$I_{OUT} = 1.6$ mA		**0.4**	V (max)
		DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			
I_O	TRI-STATE Output Current	$V_{OUT} = 5.0V$			
		DB0–DB7, RDY	0.1	**3**	μA (max)
		$V_{OUT} = 0V$			
		DB0–DB7, RDY	−0.1	**−3**	μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			
		DB0–DB7, $\overline{OFL}$, $\overline{INT}$	−26	**−6**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$			
		DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY	24	**7**	mA (min)
I_C	Supply Current	$\overline{CS} = \overline{WR} = \overline{RD} = 0$	11.5	**25**	mA (max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltage ($V_{IN} < GND$ or $V_{IN} > V^+$), the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current specification limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: The power dissipation of this device under normal operation should never exceed 875 mW (Quiescent Power Dissipation + the loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (e.g., when any input or output exceeds the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{JMAX} and θ_{JA} for the various packages and versions of the ADC08061/2.

Part Number	T_{JMAX}	θ_{JA}
ADC08061/2BIN	105	51
ADC08061/2CIN	105	51
ADC08061/2BIWM	105	85
ADC08061/2CIWM	105	85

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at 25°C and represent most likely parametric norm.

Note 8: Limits are guaranteed to National's AOQL (Average Output Quality Level).

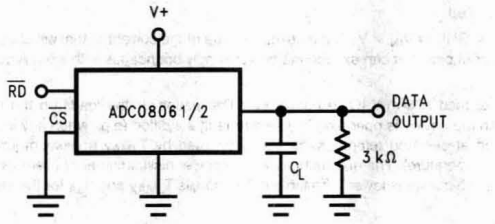
Note 9: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 10: Two on-chip diodes are tied to each analog input and are reversed biased during normal operation. One is connected to V^+ and the other is connected to GND. They will become forward biased and conduct when an analog input voltage is equal to or greater than one diode drop above V^+ or below GND. Therefore, caution should be exercised when testing with $V^+ = 4.5V$. Analog inputs with magnitudes equal to 5V can cause an input diode to conduct, especially at elevated temperatures. This can create conversion errors for analog signals near full-scale. The specification allows 50 mV forward bias on either diode; e.g., the output code will be correct as long as the analog input signal does not exceed the supply voltage by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. An absolute analog input signal voltage range of $0V \leq V_{IN} \leq 5V$ can be achieved by ensuring that the minimum supply voltage applied to V^+ is 4.950V over temperature variations, initial tolerance, and loading.

Note 11: Off-channel leakage current is measured after the on-channel selection.

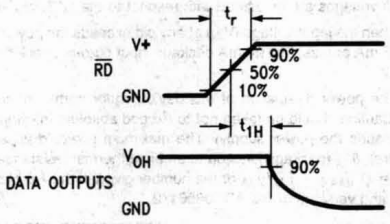
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/11086-2

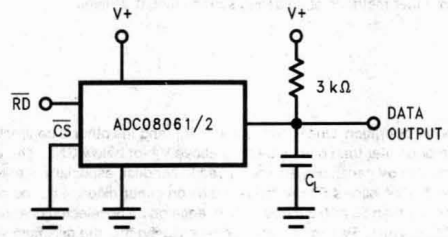
t_{1H}, C_L = 10 pF



TL/H/11086-4

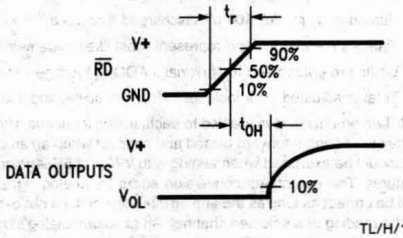
t_r = 10 ns

t_{0H}



TL/H/11086-3

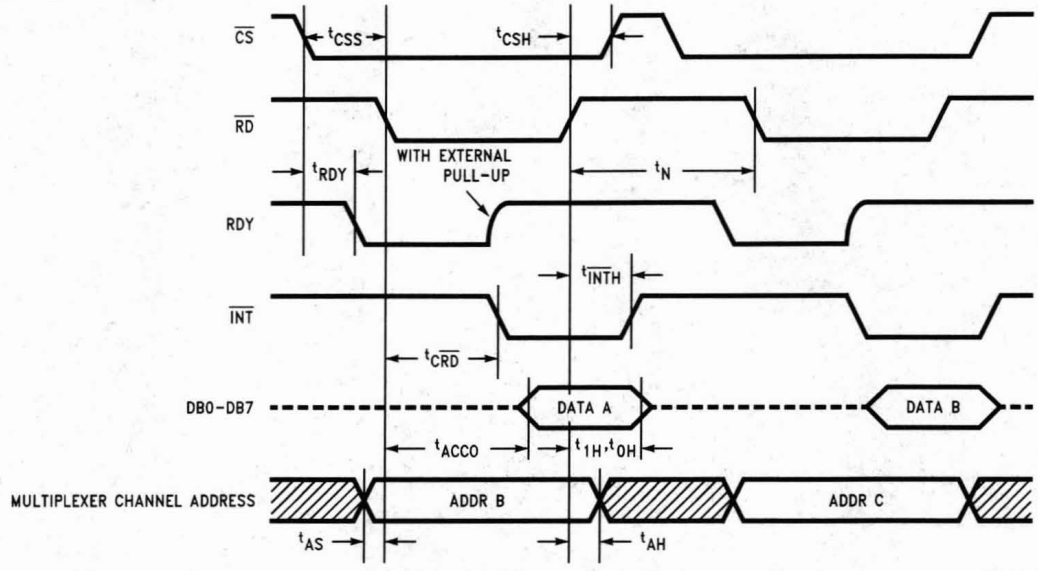
t_{0H}, C_L = 10 pF



TL/H/11086-5

t_r = 10 ns

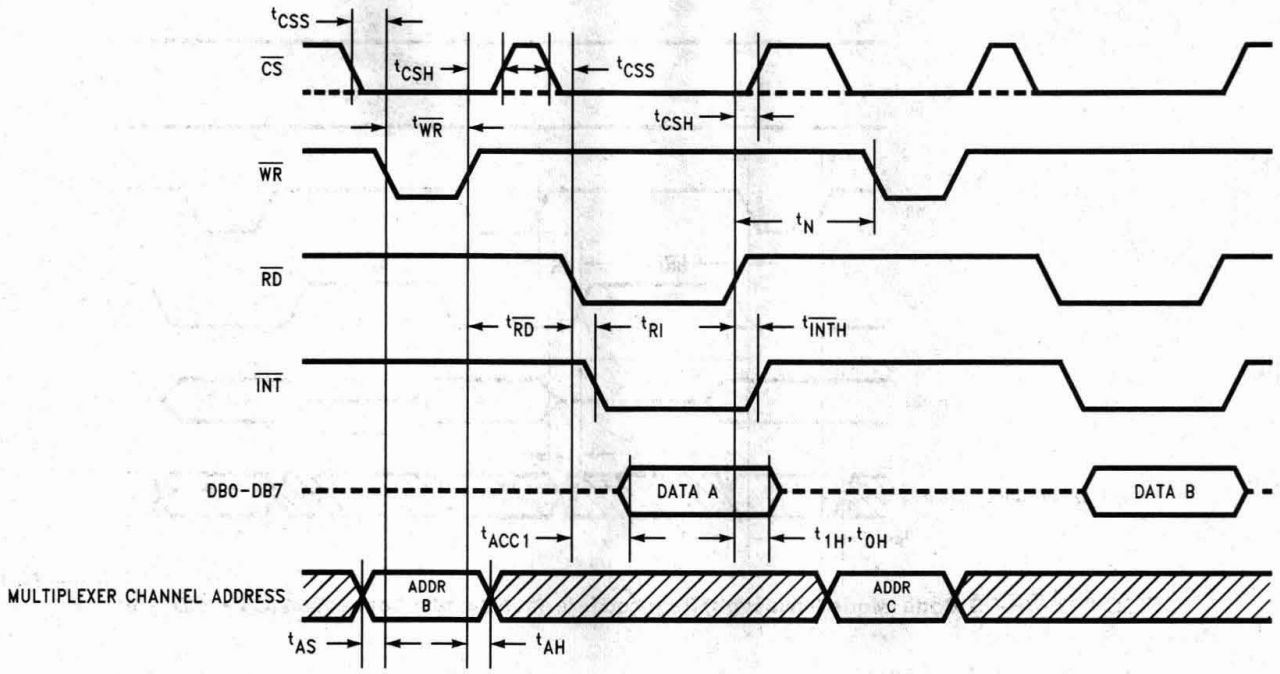
Timing Diagrams



TL/H/11086-6

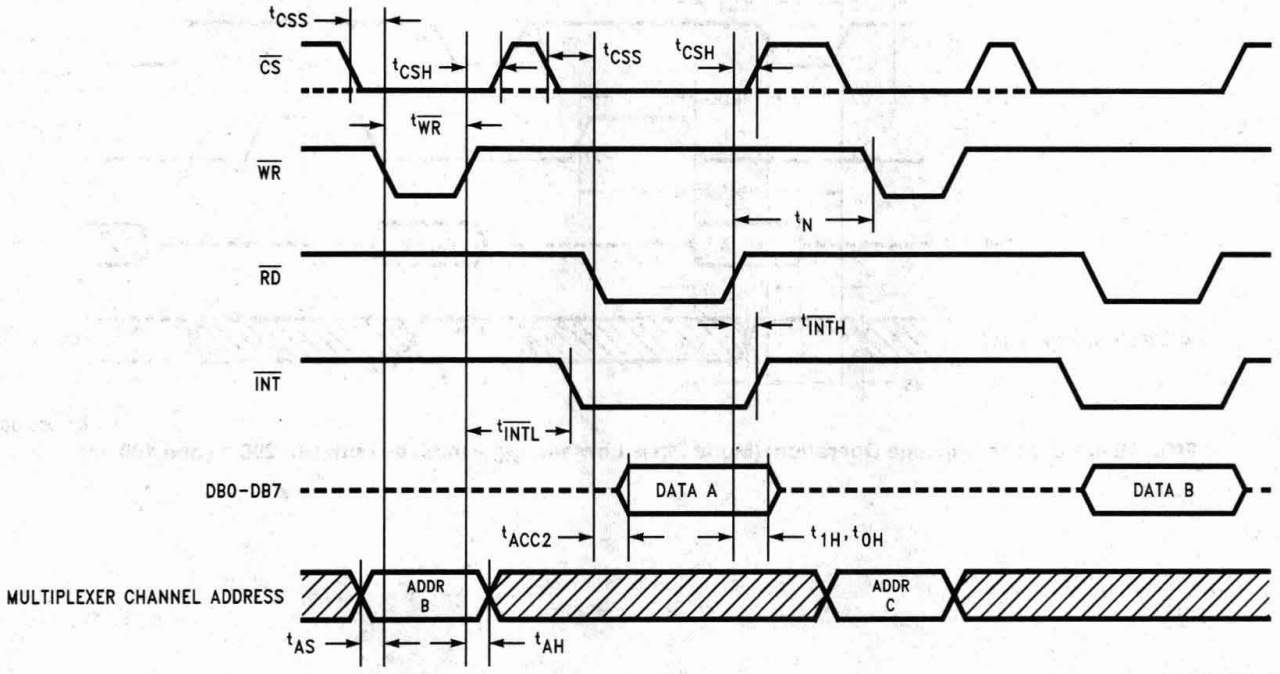
FIGURE 1. $\overline{RD}$ Mode (Mode Pin is Low)

Timing Diagrams (Continued)



TL/H/11086-7

FIGURE 2a. $\overline{WR}$-$\overline{RD}$ Mode (Mode Pin is High and $t_{\overline{RD}} \leq t_{\overline{INTL}}$)

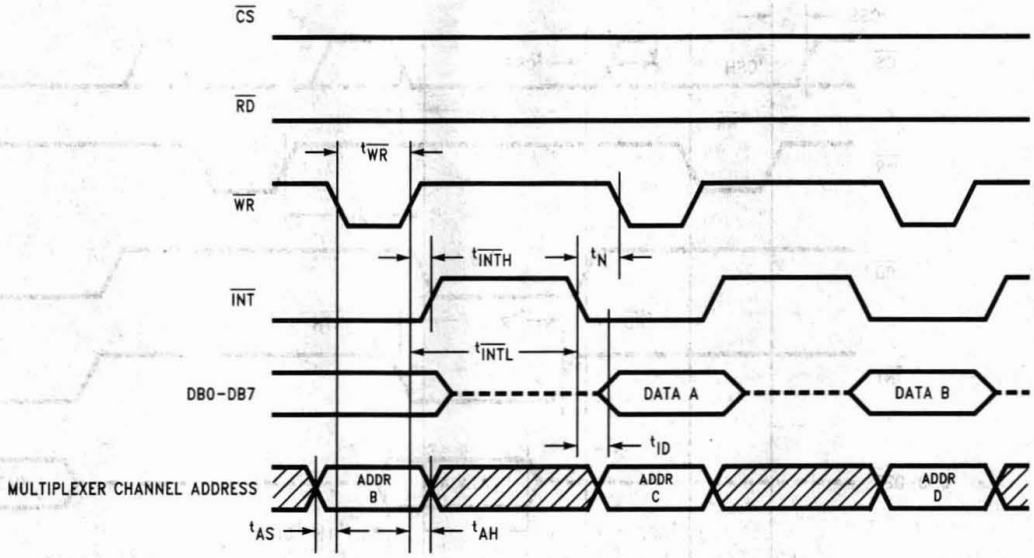


TL/H/11086-8

FIGURE 2b. $\overline{WR}$-$\overline{RD}$ Mode (Mode Pin is High and $t_{\overline{RD}} > t_{\overline{INTL}}$)

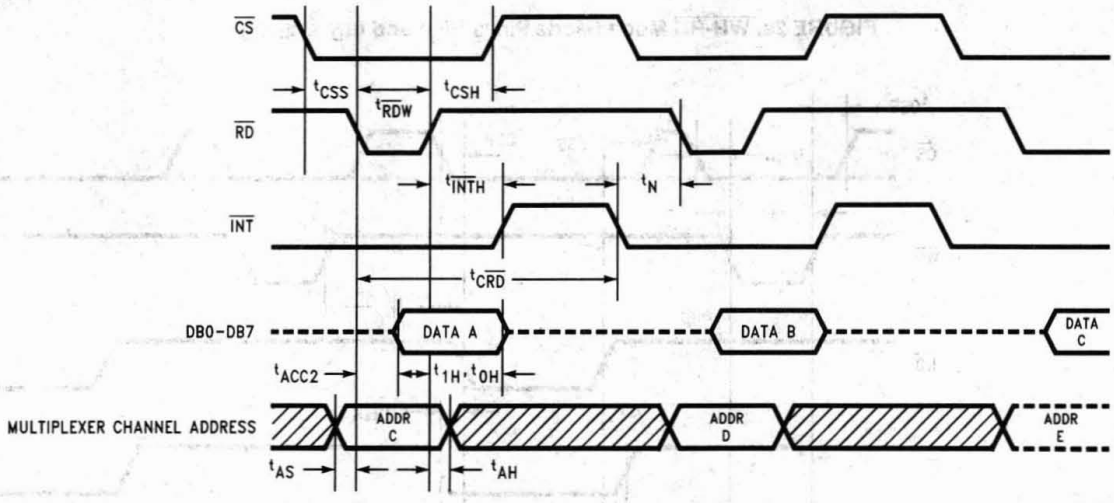
2

Timing Diagrams (Continued)



TL/H/11086–9

FIGURE 3. $\overline{WR}$-$\overline{RD}$ Mode (Mode Pin is High) Reduced Interface System Connection ($\overline{CS}$ = $\overline{RD}$ = 0)

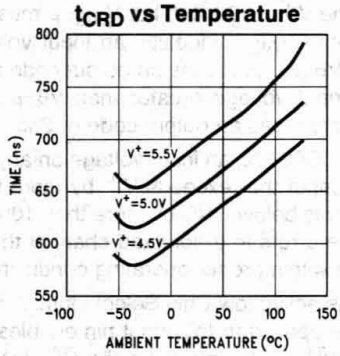


TL/H/11086–10

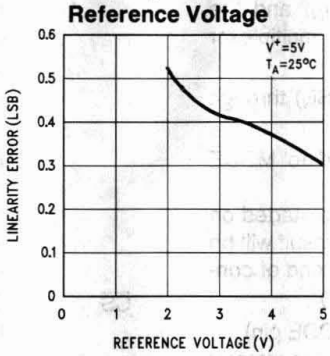
FIGURE 4. $\overline{RD}$ Mode (Pipeline Operation) (Mode Pin is Low and $t_{\overline{RDW}}$ must be between 200 ns and 400 ns)

Typical Performance Characteristics

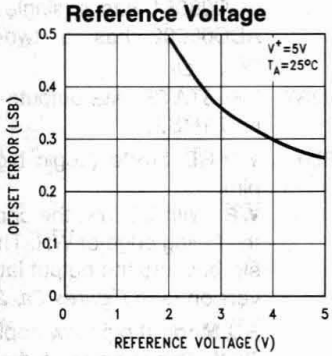
t_{CRD} vs Temperature



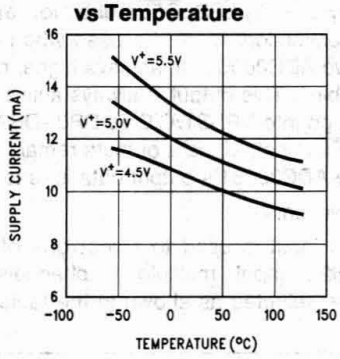
Linearity Error vs Reference Voltage



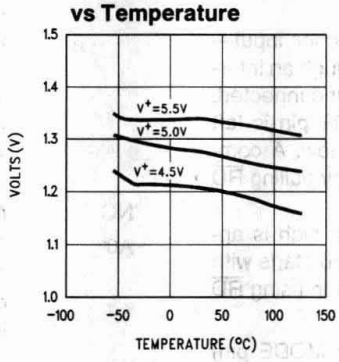
Offset Error vs Reference Voltage



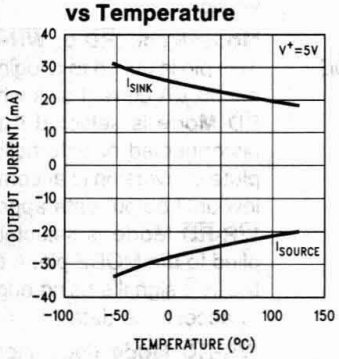
Supply Current vs Temperature



Logic Threshold vs Temperature

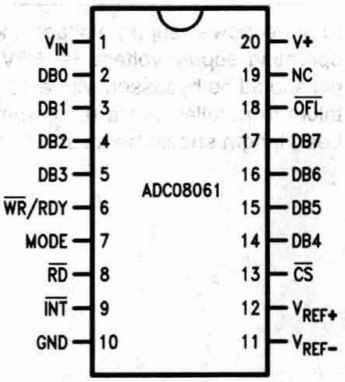


Output Current vs Temperature



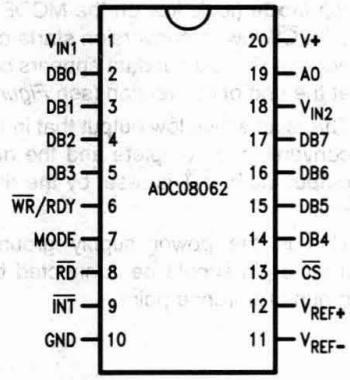
TL/H/11086–24

Connection Diagrams



TL/H/11086–14

Dual-In-Line and Wide-Body Small-Outline Packages J20A, N20A or M20B



TL/H/11086–15

Dual-In-Line and Wide-Body Small-Outline Packages N20A or M20B

Ordering Information

Industrial ($-40°C \leq T_A \leq 85°C$)	Package
ADC08061BIN, ADC08061CIN, ADC08062BIN, ADC08062CIN	N20A
ADC08061BIWM, ADC08061CIWM, ADC08062BIWM, ADC08062CIWM	M20B
ADC08061CMJ, ADC08061CMJ/883, 5962	J20A

2

Pin Description

V_{IN}, V_{IN1-8} These are analog inputs. The input range is GND−50 mV ≤ V_{INPUT} ≤ V^+ + 50 mV. The ADC08061 has a single input (V_{IN}) and the ADC08062 has a two-channel multiplexer (V_{IN1-2}).

DB0–DB7 TRI-STATE data outputs—bit 0 (LSB) through bit 7 (MSB).

$\overline{WR}$/RDY **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)
$\overline{WR}$: With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (see *Figures 2a, 2b,* and *3*).

$\overline{RD}$ Mode (Logic low applied to MODE pin)
RDY: This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and return high at the end of conversion.

MODE **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input—This pin is pulled to a logic low through an internal 50 μA current sink when left unconnected.
$\overline{RD}$ Mode is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.
$\overline{WR}$-$\overline{RD}$ Mode is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.

$\overline{RD}$ **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin)
This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (see *Figures 2a, 2b* and *3*).
$\overline{RD}$ Mode (logic low on the MODE pin)
With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (see *Figures 1* and *4*).

$\overline{INT}$ This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.

GND This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.

V_{REF-}
V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} − 1.5 LSB produces an output code of 255.

For the ADC08062, an input voltage on any unselected input that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create errors in a selected channel that is operating within proper operating conditions.

$\overline{CS}$ This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.

$\overline{OFL}$ Overflow Output. If the analog input is higher than V_{REF+} − ½ LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08061s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.

NC No connection.

A0 This logic input is used to select one of the ADC08062's input multiplexer channels. A channel is selected as shown in the table below.

ADC08062 A0	Channel
0	V_{IN1}
1	V_{IN2}

V^+ Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 μF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

Application Information

1.0 FUNCTIONAL DESCRIPTION

The ADC08061 and ADC08062 perform an 8-bit analog-to-digital conversion using a multi-step flash technique. The first flash generates the five most significant bits (MSBs) and the second flash generates the three least significant bits (LSBs). *Figure 5* shows the major functional blocks of the ADC08061/2's multi-step flash converter. It consists of an over-encoded 2½-bit Voltage Estimator, an internal DAC with two different voltage spans, a 3-bit half-flash converter and a comparator multiplexer.

The resistor string near the center of the block diagram in *Figure 5* forms the internal main DAC. Each of the eight resistors at the bottom of the string is equal to 1/256 of the total string resistance. These resistors form the **LSB Ladder** and have a voltage drop of 1/256 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remaining resistors make up the **MSB Ladder**. They are made up of eight groups of four resistors connected in series. Each MSB Ladder section has ⅛ of the total reference voltage across it. Within a given MSB Ladder section, each of the MSB resistors has 8/256, or 1/32 of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB Ladders. Through the Comparator Multiplexer these tap points can be connected, in groups of eight, to the eight comparators shown at the right of *Figure 5*. This function provides the necessary reference voltages to the comparators during each flash conversion.

The six comparators, seven-resistor string (estimator DAC), and Estimator Decoder at the left of *Figure 5* form the Voltage Estimator. The estimator DAC connected between V_{REF+} and V_{REF-} generates the reference voltages for the six Voltage Estimator comparators. These comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is then used to control the Comparator Multiplexer, connecting the appropriate MSB Ladder section to the eight flash comparators. Only 14 comparators, six in the Voltage Estimator and eight in the flash converter, are needed to achieve the full eight-bit resolution, instead of 32 comparators that would be needed by traditional half-flash methods.

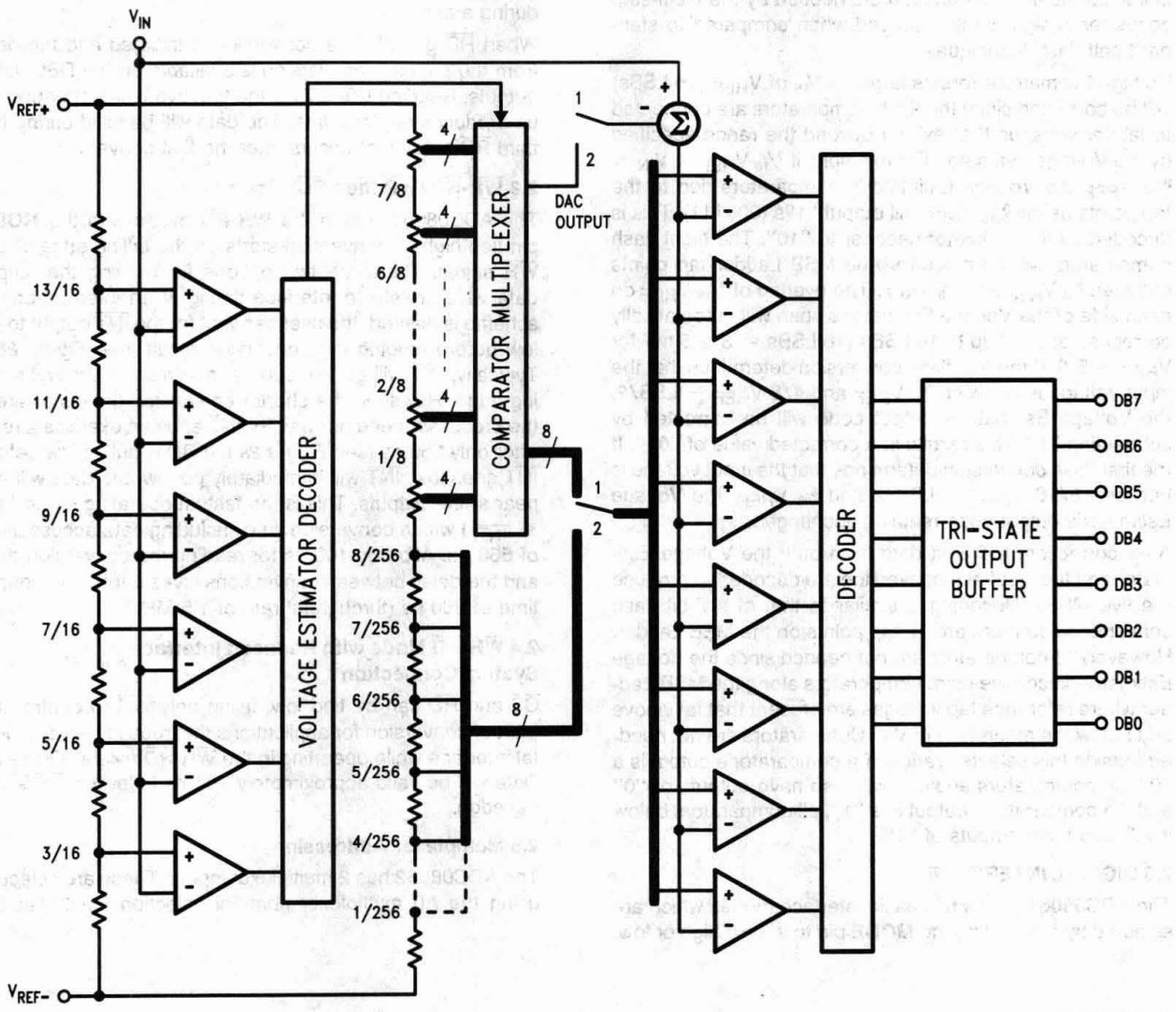


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FIGURE 5. Block Diagram of the ADC08061/2 Multi-Step Flash Architecture

Application Information (Continued)

A conversion begins with the Voltage Estimator comparing the analog input signal against the six tap voltages on the estimator DAC. The estimator decoder then selects one of the groups of tap points along the MSB Ladder. These eight tap points are then connected to the eight flash comparators. For example, if the analog input signal applied to V_{IN} is between 0 and $3/16$ of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the eight tap points between 8/256 and 2/8 of V_{REF} and connects them to the eight flash comparators. The first flash conversion is now performed, producing the five MSBs of data.

The remaining three LSBs are generated next using the same eight comparators that were used for the first flash conversion. As determined by the results of the MSB flash, a voltage from the MSB Ladder equivalent to the magnitude of the five MSBs is subtracted from the analog input voltage as the upper switch is moved from position one to position two. The resulting remainder voltage is applied to the eight flash comparators and, with the lower switch in position two, compared with the eight tap points from the LSB Ladder.

By using the same eight comparators for both flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard half-flash techniques.

Voltage Estimator errors as large as $1/16$ of V_{REF} (16 LSBs) will be corrected since the flash comparators are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if $7/16\ V_{REF} < V_{IN} < 9/16\ V_{REF}$ the Voltage Estimator's comparators tied to the tap points below $9/16\ V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The eight flash comparators will be placed at the MSB Ladder tap points between $3/8\ V_{REF}$ and $5/8\ V_{REF}$. The overlap of $1/16\ V_{REF}$ on each side of the Voltage Estimator's span will automatically correct an error of up to 16 LSBs (16 LSBs = 312.5 mV for $V_{REF} = 5V$). If the first flash conversion determines that the input voltage is between $3/8\ V_{REF}$ and $4/8\ V_{REF} - LSB/2$, the Voltage Estimator's output code will be corrected by subtracting "1". This results in a corrected value of "01". If the first flash conversion determines that the input voltage is between $8/16\ V_{REF} - LSB/2$ and $5/8\ V_{REF}$, the Voltage Estimator's output code remains unchanged.

After correction, the 2-bit data from both the Voltage Estimator and the first flash conversion are decoded to produce the five MSBs. Decoding is similar to that of a 5-bit flash converter since there are 32 tap points on the MSB Ladder. However, 31 comparators are not needed since the Voltage Estimator places the eight comparators along the MSB Ladder where reference tap voltages are present that fall above and below the magnitude of V_{IN}. Comparators are not needed outside this selected range. If a comparator's output is a "0", all comparators above it will also have outputs of "0" and if a comparator's output is a "1", all comparators below it will also have outputs of "1".

2.0 DIGITAL INTERFACE

The ADC08061/2 has two basic interface modes which are selected by connecting the **MODE** pin to a logic high or low.

2.1 $\overline{RD}$ Mode

With a logic low applied to the **MODE** pin, the converter is set to **Read** mode. In this configuration (see *Figure 1*), a complete version is done by pulling $\overline{RD}$ low, and holding low, until the conversion is complete and output data appears. This typically takes 655 ns. The $\overline{INT}$ (interrupt) line goes low at the end of conversion. A typical delay of 50 ns is needed between the rising edge of $\overline{RD}$ (after the end of a conversion) and the start of the next conversion (by pulling $\overline{RD}$ low). The RDY output goes low after the falling edge of $\overline{CS}$ and goes high at the end-of-conversion. It can be used to signal a processor that the converter is busy or serve as a system Transfer Acknowledge signal. For the ADC08062 the data generated by the first conversion cycle after power-up is from an unknown channel.

2.2 $\overline{RD}$ Mode Pipelined Operation

Applications that require shorter $\overline{RD}$ pulse widths than those used in the **Read** mode as described above can be achieved by setting $\overline{RD}$'s width between 200 ns–400 ns *(Figure 4)*. $\overline{RD}$ pulse widths outside this range will create conversion linearity errors. These errors are caused by exercising internal interface logic circuitry using $\overline{CS}$ and/or $\overline{RD}$ during a conversion.

When $\overline{RD}$ goes low, a conversion is initiated and the data from the previous conversion is available on the DB0–DB7 outputs. Reading D0–D7 for the first two times after power-up produces random data. The data will be valid during the third $\overline{RD}$ pulse that occurs after the first conversion.

2.3 $\overline{WR}$-$\overline{RD}$ ($\overline{WR}$ then $\overline{RD}$) Mode

The ADC08061/2 is in the **$\overline{WR}$-$\overline{RD}$ mode** with the **MODE** pin tied high. A conversion starts on the falling edge of the $\overline{WR}$ signal. There are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for the $\overline{INT}$ output to go low before reading the conversion result (see *Figure 2b*). Typically, $\overline{INT}$ will go low 520 ns, maximum, after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 350 ns (see *Figure 2a*). If $\overline{RD}$ is pulled low before $\overline{INT}$ goes low, $\overline{INT}$ will immediately go low and data will appear at the outputs. This is the fastest operating mode ($t_{\overline{RD}} \leq t_{\overline{INTL}}$) with a conversion time, including data access time, of 560 ns. Allowing 100 ns for reading the conversion data and the delay between conversions gives a total throughput time of 660 ns (throughput rate of 1.5 MHz).

2.4 $\overline{WR}$-$\overline{RD}$ Mode with Reduced Interface System Connection

$\overline{CS}$ and $\overline{RD}$ can be tied low, using only $\overline{WR}$ to control the start of conversion for applications that require reduced digital interface while operating in the **$\overline{WR}$-$\overline{RD}$ mode** *(Figure 3)*. Data will be valid approximately 705 ns following $\overline{WR}$'s rising edge.

2.5 Multiplexer Addressing

The ADC08062 has 2 multiplexer inputs. These are selected using the A0 multiplexer channel selection input. Table I

Application Information (Continued)

shows the input code needed to select a given channel. The multiplexer address is latched when received but the multiplexer channel is updated after the completion of the current conversion.

TABLE I. Multiplexer Addressing

ADC08062 A0	Channel
0	V_{IN1}
1	V_{IN2}

The multiplexer address data must be valid at the time of $\overline{RD}$'s falling edge, remain valid during the conversion, and can go high after $\overline{RD}$ goes high when operating in the **Read Mode**.

The multiplexer address data should be valid at or before the time of $\overline{WR}$'s falling edge, remain valid while $\overline{WR}$ is low, and go invalid after $\overline{WR}$ goes high when operating in the **$\overline{WR}$-$\overline{RD}$ Mode**.

3.0 REFERENCE INPUTS

The two V_{REF} inputs of the ADC08061/2 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to vary the span of the analog input since this range will be equivalent to the voltage difference between V_{REF+} and V_{REF-}. Transducers with minimum output voltages above GND can also be compensated by connecting V_{REF-} to a voltage that is equal to this minimum voltage. By reducing V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF} = 2.5V$, then 1 LSB = 9.8 mV). The ADC08061/2's reference arrangement also facilitates ratiometric operation and in many cases the ADC08061/2's power supply can be used for transducer power as well as the V_{REF} source. Ratiometric operation is achieved by connecting V_{REF-} to GND and connecting V_{REF+} and a transducer's power supply input to V^+. The ADC08061/2's linearity degrades when $V_{REF+} - |V_{REF-}|$ is less than 2.0V.

The voltage at V_{REF-} sets the input level that produces a digital output of all zeros. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for some measurement applications. *Figure 6* shows one possible differential configuration.

It should be noted that, while the two V_{REF} inputs are fully differential, the digital output will be zero for any analog input voltage if $V_{REF-} \geq V_{REF+}$.

4.0 ANALOG INPUT AND SOURCE IMPEDANCE

The ADC08061/2's analog input circuitry includes an analog switch with an "on" resistance of 70Ω and capacitance of 1.4 pF and 12 pF (see *Figure 6*). The switch is closed during the A/D's input signal acquisition time (while $\overline{WR}$ is low when using the $\overline{WR}$-$\overline{RD}$ Mode). A small transient current flows into the input pin each time the switch closes. A transient voltage, whose magnitude can increase as the source impedance increases, may be present at the input. So long as the source impedance is less than 500Ω, the input voltage transient will not cause errors and need not be filtered.

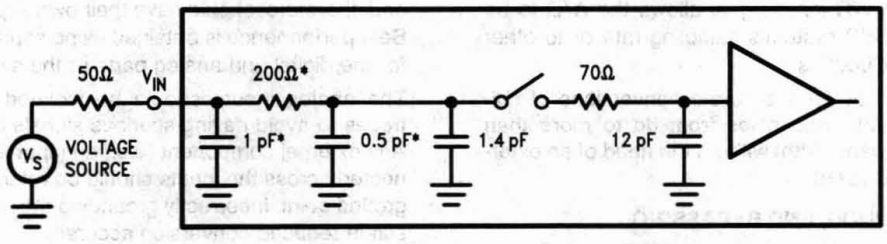
Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (100 ns maximum). A signal source with a high output impedance should have its output buffered with an operational amplifier. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 100 mV and less than V^+ + 100 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than V^+, or more than 300 mV lower than GND. The current flowing through any analog input pin should be limited to 5 mA or less to avoid permanent damage to the IC if an analog input pin is forced beyond these voltages. The sum of all the overdrive currents into all pins must be less than 20 mA. Some sort of protection scheme should be used when the input signal is expected to extend more than 300 mV beyond the power supply limits. A simple protection network using resistors and diodes is shown in *Figure 8*.

6.0 INHERENT SAMPLE-AND-HOLD

An important benefit of the ADC08061/2's input architecture is the inherent sample-and-hold (S/H) and its ability to measure relatively high speed signals without the help of an external S/H. In a non-sampling converter, regardless of its speed, the input must remain stable to at least ½ LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion.

The ADC08061 and ADC08062 are suitable for DSP-based systems because of the direct control of the S/H through

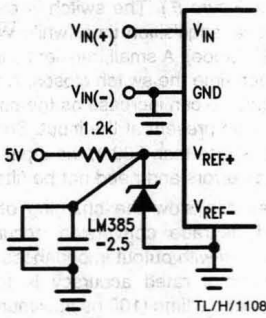


*Represents a multiplexer channel in the ADC08062.

FIGURE 6. ADC08061 and ADC08062 Equivalent Input Circuit Model

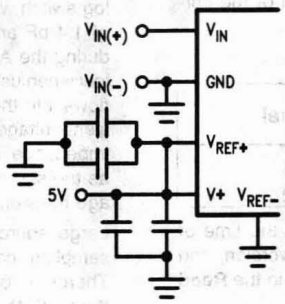
Application Information (Continued)

External Reference 2.5V Full-Scale (Standard Application)



TL/H/11086–20

Power Supply as Reference



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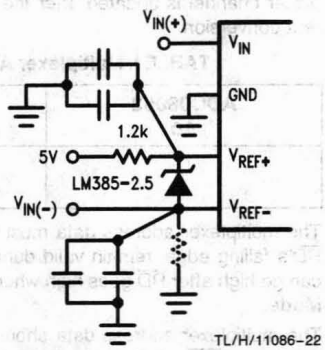
Input Not Referred to GND

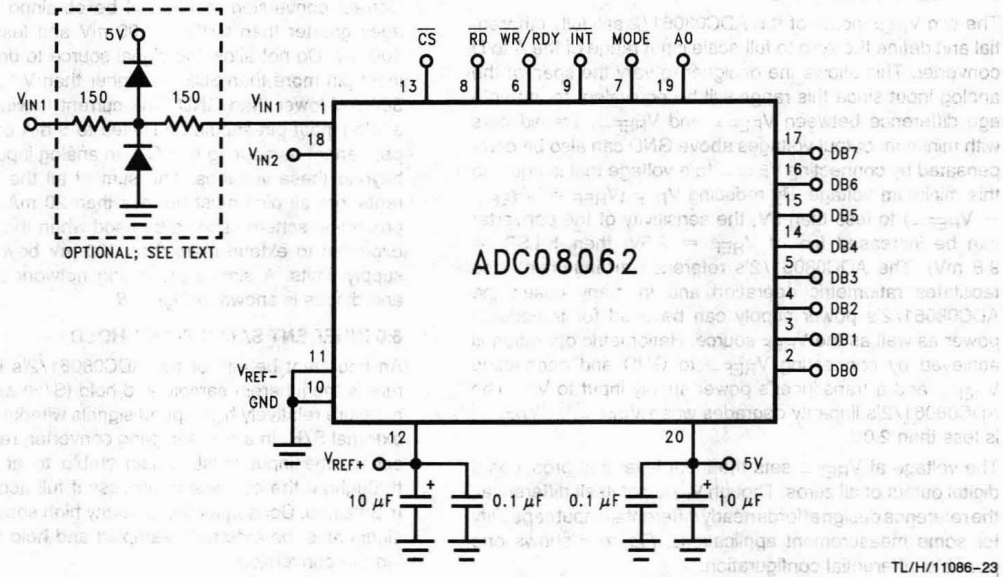


TL/H/11086–22

Note: Bypass capacitors consist of a 0.1 μF ceramic in parallel with a 10 μF bead tantalum.

*Signal source driving $V_{IN}(-)$ must be capable of sinking 5 mA.

FIGURE 7. Analog Input Options



TL/H/11086–23

Note the multiple bypass capacitors on the reference and power supply pins. V_{REF-} should be bypass to analog ground using multiple capacitors if it is not grounded (see Section 7.0 "Layout, Grounds, and Bypassing"). V_{IN1} is shown with an optional input protection network.

FIGURE 8. Typical Connection

the $\overline{WR}$ signal. The $\overline{WR}$ input signal allows the A/D to be synchronized to a DSP system's sampling rate or to other ADC08061 and ADC08062s.

The ADC08061 can perform accurate conversions of full-scale input signals at frequencies from dc to more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

7.0 LAYOUT, GROUNDS, AND BYPASSING

In order to ensure fast, accurate conversions from the ADC08061/2, it is necessary to use appropriate circuit board layout techniques. Ideally, the analog-to-digital converter's ground reference should be low impedance and free of noise from other parts of the system. Digital circuits can produce a great deal of noise on their ground returns and, therefore, should have their own separate ground lines. Best performance is obtained using separate ground planes for the digital and analog parts of the system.

The analog inputs should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., an input filter capacitor) connected across the inputs should be returned to a very clean ground point. Incorrectly grounding the ADC08061/2 will result in reduced conversion accuracy.

The V^+ supply pin, V_{REF+}, and V_{REF-} (if not grounded) should be bypassed with a parallel combination of a 0.1 μF ceramic capacitor and a 10 μF tantalum capacitor placed as close as possible to the supply pin using short circuit board traces. See *Figures 7* and *8*.

National Semiconductor

ADC08161
500 ns A/D Converter with S/H Function and 2.5V Bandgap Reference

General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08161 CMOS A/D converter offers 500 ns conversion time, internal sample-and-hold (S/H), a 2.5V bandgap reference, and dissipates only 100 mW of power. The ADC08161 performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LBSs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, this part has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

- Resolution — 8 Bits
- Conversion time (t_{CONV}) — 560 ns max ($\overline{WR}$-$\overline{RD}$ Mode)
- Full power bandwidth — 300 kHz (typ)
- Throughput rate — 1.5 MHz min
- Power dissipation — 100 mW max
- Total unadjusted error — ±½ LSB and ±1 LSB max

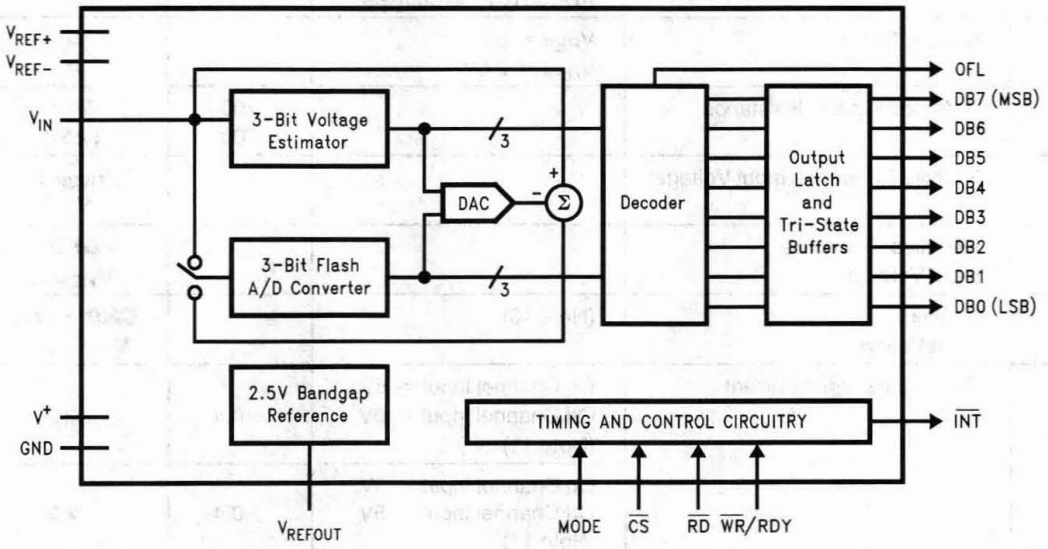
Features

- No external clock required
- Analog input voltage range from GND to V^+
- 2.5V bandgap reference

Applications

- Mobile telecommunications
- Hard-disk drives
- Instrumentation
- High-speed data acquisition systems

Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+)	6V
Logic Control Inputs	−0.3V to V^+ + 0.3V
Voltage at Other Inputs and Outputs	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	
N Package	875 mW
WM Package	875 mW
Lead Temperature (Note 5)	
N Package (Soldering, 10 sec.)	+260°C
WM Package (Vapor Phase, 60 sec.)	+215°C
WM Package (Infrared, 15 sec.)	+220°C
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 6)	750V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08161BIN, ADC08161CIN, ADC08161BIWM, ADC08161CIWM	−40°C ≤ T_A ≤ 85°C
Supply Voltage, (V^+)	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $\overline{RD}$ Mode, $V^+ = 5V$, $V_{REF+} = 5V$, and $V_{REF-} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
INL	Integral Non Linearity	$V_{REF} = 5V$ ADC08161BIN, BIWM		**±½**	LSB (max)
		ADC08161CIN, CIWM		**±1**	LSB (max)
TUE	Total Unadjusted Error (Note 9)	$V_{REF} = 5V$ ADC08161BIN, BIWM		**±½**	LSB (max)
		ADC08161CIN, CIWM,		**±1**	LSB (max)
INL	Integral Non Linearity	$V_{REF} = 2.5V$, All Suffixes		**±1**	LSB (max)
TUE	Total Unadjusted Error	$V_{REF} = 2.5V$ ADC08161, All Suffixes		**±1**	LSB (max)
	Missing Codes	$V_{REF} = 5V$ $V_{REF} = 2.5V$		**0** **0**	Bits (max) Bits (max)
	Reference Input Resistance		700 700	**500** **1250**	Ω (min) Ω (max)
V_{REF+}	Positive Reference Input Voltage			**V_{REF-}** **V^+**	V (min) V (max)
V_{REF-}	Negative Reference Input Voltage			**GND** **V_{REF+}**	V (min) V (max)
V_{IN}	Analog Input Voltage	(Note 10)		**GND − 0.1** **V^+ + 0.1**	V (min) V (max)
	On-Channel Input Current	On Channel Input = 5V, Off Channel Input = 0V (Note 11)	−0.4	**−20**	μA (max)
		On Channel Input = 0V, Off Channel Input = 5V (Note 11)	−0.4	**−20**	μA (max)

Converter Characteristics (Continued)

The following specifications apply for $\overline{RD}$ Mode, $V^+ = 5V$, $V_{REF+} = 5V$, and $V_{REF-} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
PSS	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.75V$ All Codes Tested	$\pm 1/16$	$\pm 1/2$	LSB (max)
	Effective Bits	$V_{IN} = 4.85\ V_{p-p}$ $f_{IN} = 20$ Hz to 20 kHz	7.8		Bits
	Full-Power Bandwidth	$V_{IN} = 4.85\ V_{p-p}$	300		kHz
THD	Total Harmonic Distortion	$V_{IN} = 4.85\ V_{p-p}$ $f_{IN} = 20$ Hz to 20 kHz	0.5		%
S/N	Signal-to-Noise Ratio	$V_{IN} = 4.85\ V_{p-p}$ $f_{IN} = 20$ Hz to 20 kHz	50		dB
IMD	Intermodulation Distortion	$V_{IN} = 4.85\ V_{p-p}$ $f_{IN} = 20$ Hz to 20 kHz	50		dB
C_{VIN}	Analog Input Capacitance		25		pF

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $t_r = t_f = 10$ ns, $V_{REF+} = 5V$, $V_{REF-} = 0V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08161BIN, ADC08161CIN, ADC08161BIWM, ADC08161CIWM		Units (Limit)
			Typical (Note 7)	Limit (Note 8)	
$t_{\overline{WR}}$	Write Time	Mode Pin to V^+ (*Figures 2a, 2b,* and *3*)	100	**100**	ns (min)
$t_{\overline{RD}}$	Read Time (Time from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{RD}$)	Mode Pin to V^+, CMJ Suffix *(Figure 2a)*	350	**350** **515**	ns (min)
t_{RDW}	$\overline{RD}$ Width	Mode Pin to GND *(Figure 4)*	200 400	**250** **400**	ns (min) ns (max)
t_{CONV}	$\overline{WR}$-$\overline{RD}$ Mode Conversion Time ($t_{WR} + t_{RD} + t_{ACC1}$)	Mode Pin to V^+, CMJ Suffix *(Figure 2a)*	500	**560** **790**	ns (max)
t_{CRD}	$\overline{RD}$ Mode Conversion Time	Mode Pin to GND, CMJ Suffix *(Figure 1)*	655	**900** **940**	ns (max)
t_{ACCO}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 100$ pF, Mode Pin to GND CMJ Suffix *(Figure 1)*	640	**900** **940**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 10$ pF $C_L = 100$ pF Mode Pin to V^+, $t_{RD} \leq t_{INTL}$ CMJ Suffix *(Figure 2a)*	45 50	 **110** **175**	ns ns (max) ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	$C_L \leq 10$ pF $C_L = 100$ pF $t_{RD} > t_{INTL}$, CMJ Suffix, (*Figures 2b* and *4*)	25 30	 **55** **60**	ns ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$R_L = 3\ k\Omega$, $C_L = 10$ pF (*Figures 1, 2a, 2b, 3,* and *4*)	30	**60**	ns (max)
$t_{\overline{INTL}}$	Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Mode Pin = V^+, $C_L = 50$ pF (*Figures 2b,* and *3*)	520	**690**	ns (max)

2

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $t_r = t_f = 10$ ns, $V_{REF+} = 5V$, $V_{REF-} = 0V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08161BIN, ADC08161CIN, ADC08161BIWM, ADC08161CIWM		Units (Limit)
			Typical (Note 7)	Limit (Note 8)	
$t_{\overline{INT}H}$	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF, CMJ Suffix (*Figures 1, 2a, 2b,* and *4*)	50	**95** **100**	ns (max)
$t_{\overline{INT}H}$	Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	$C_L = 50$ pF, CMJ Suffix (*Figure 3*)	45	**95** **100**	ns (max)
t_{RDY}	Delay from $\overline{CS}$ to RDY	Mode Pin = 0V, $C_L = 50$ pF, $R_L = 3$ kΩ, CMJ Suffix (*Figure 1*)	25	**45** **50**	ns (max)
t_{ID}	Delay from $\overline{INT}$ to Output Valid	$R_L = 3$ kΩ, $C_L = 100$ pF (*Figure 3*)	0	**15**	ns (max)
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$	Mode Pin = V^+, $t_{RD} \leq t_{INTL}$ CMJ Suffix (*Figure 2a*)	60	**115** **175**	ns (max)
t_N	Time between End of $\overline{RD}$ and Start of New Conversion	(*Figures 1, 2a, 2b, 3* and *4*)	50	**50**	ns (min)
$t_{\overline{CS}S}$	$\overline{CS}$ Setup Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (max)
$t_{\overline{CS}H}$	$\overline{CS}$ Hold Time	(*Figures 1, 2a, 2b, 3* and *4*)	0	**0**	ns (max)

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08161BIN, ADC08161CIN, ADC08161BIWM, ADC08161CIWM		Units (Limit)
			Typical (Note 7)	Limit (Note 8)	
V_{IH}	Logic "1" Input Voltage	$V^+ = 5.5$ V $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins Mode Pin		**2.0** **3.5**	V (min)
V_{IL}	Logic "0" Input Voltage	$V^+ = 4.5$V $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, A0, A1, A2 Pins Mode Pin		**0.8** **1.5**	V (max)
I_{IH}	Logic "1" Input Current	$V_H = 5$V $\overline{CS}$, $\overline{RD}$, A0, A1, A2 Pins $\overline{WR}$ Pin Mode Pin	0.005 0.1 50	**1** **3** **200**	μA (max)
I_{IL}	Logic "0" Input Current	$V_L = 0$V $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, A1, A2 Mode Pins	−0.005	**−2**	μA (max)
V_{OH}	Logic "1" Output Voltage	$V^+ = 4.75$V $I_{OUT} = -360$ μA DB0–DB7, $\overline{OFL}$, $\overline{INT}$ $I_{OUT} = -10$ μA DB0–DB7, $\overline{OFL}$, $\overline{INT}$		**2.4** **4.5**	V (min) V (min)

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	ADC08161BIN, ADC08161CIN, ADC08161BIWM, ADC08161CIWM,		Units (Limit)
			Typical (Note 7)	Limit (Note 8)	
V_{OL}	Logic "0" Output Voltage	$V^+ = 4.75V$ $I_{OUT} = 1.6$ mA DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		**0.4**	V (max)
I_O	TRI-STATE Output Current	$V_{OUT} = 5.0V$ DB0–DB7, RDY	0.1	**3**	μA (max)
		$V_{OUT} = 0V$ DB0–DB7, RDY	−0.1	**−3**	μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$	−26	**−6**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$ DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY	24	**7**	mA (min)
I_C	Supply Current	$\overline{CS} = \overline{WR} = \overline{RD} = 0$	11.5	**20**	mA (max)
C_{OUT}	Logic Output Capacitance		5		pF
C_{IN}	Logic Input Capacitance		5		pF

Bandgap Reference Electrical Characteristics

The following specifications apply for $V^+ = 5V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limits (Note 8)	Units (Limit)
V_{REFOUT}	Internal Reference Output Voltage	"B" Grade "C" Grade	2.5	**2.5 ± 1.5%** **2.5 ± 2.0%**	V (max)
$\Delta V_{REF}/\Delta T$	Internal Reference Temperature Coefficient		40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Internal Reference Load Regulation	Sourcing ($0 \le I_L \le +10$ mA)	0.01	**0.1**	%/mA (max)
	Line Regulation	$4.75V \le V^+ \le 5.25V$	0.5	**6.0**	mV (max)
I_{SC}	Short Circuit Current	$V_{REV} = 0V$	35		mA (max)
$\Delta V_{REF}/\Delta_t$	Long Term Stability		200		ppm/kHr
	Start-Up Time	V^+: 0V ⟶ 5V, $C_L = 220\ \mu F$	40		ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply voltage ($V_{IN} <$ GND or $V_{IN} > V^+$), the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current specification limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 4: The power dissipation of this device under normal operation should never exceed 875 mW (Quiescent Power Dissipation + TTL Loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (e.g., when any input or output exceeds the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{JMAX} and θ_{JA} for the various packages and versions of the ADC08161.

Part Number	T_{JMAX}	θ_{JA}
ADC08161B/CIN	105	51
ADC08161B/CIWM	105	85

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at 25°C and represent most likely parametric norm.

Note 8: Limits are guaranteed to National's AOQL (Average Output Quality Level).

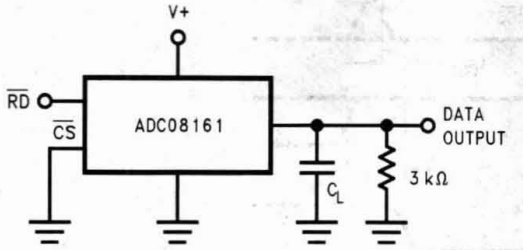
Note 9: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 10: Two on-chip diodes are tied to each analog input and are reversed biased during normal operation. One is connected to V^+ and the other is connected to GND. They will become forward biased and conduct when an analog input voltage is equal to or greater than one diode drop above V^+ or below GND. Therefore, caution should be exercised when testing with $V^+ = 4.5V$. Analog inputs with magnitudes equal to 5V can cause an input diode to conduct, especially at elevated temperatures. This can create conversion errors for analog signals near full-scale. The specification allows 50 mV forward bias on either diode; e.g., the output code will be correct as long as the analog input signal does not exceed the supply voltage by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. An absolute analog input signal voltage range of $0V \le V_{IN} \le 5V$ can be achieved by ensuring that the minimum supply voltage applied to V^+ is 4.950V over temperature variations, initial tolerance, and loading.

Note 11: Off-channel leakage current is measured on the on-channel selection.

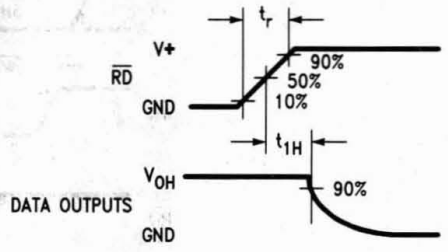
TRI-STATE Test Circuit and Waveforms

t_{1H}



TL/H/11149-2

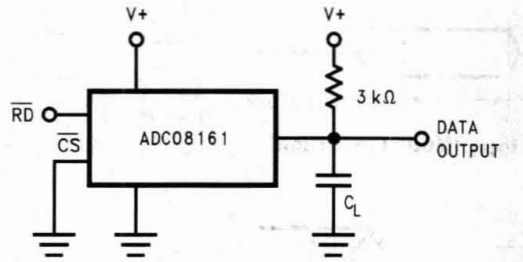
t_{1H}, C_L = 10 pF



TL/H/11149-4

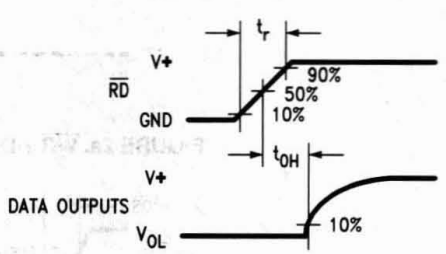
t_r = 10 ns

t_{0H}



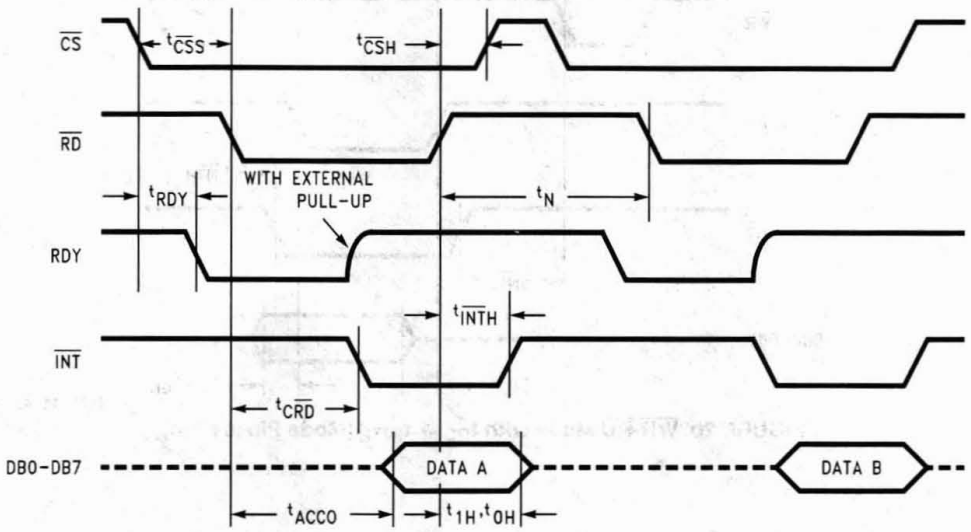
TL/H/11149-3

t_{0H}, C_L = 10 pF



TL/H/11149-5

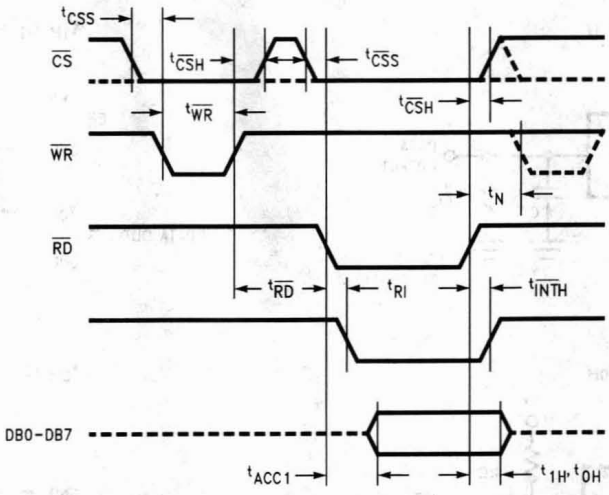
t_r = 10 ns



TL/H/11149-6

FIGURE 1. $\overline{RD}$ Mode (Mode Pin is Low)

TRI-STATE Test Circuit and Waveforms (Continued)



TL/H/11149-7

FIGURE 2a. $\overline{WR}$-$\overline{RD}$ Mode with $t_{RD} \leq t_{INTL}$ (Mode Pin is High)

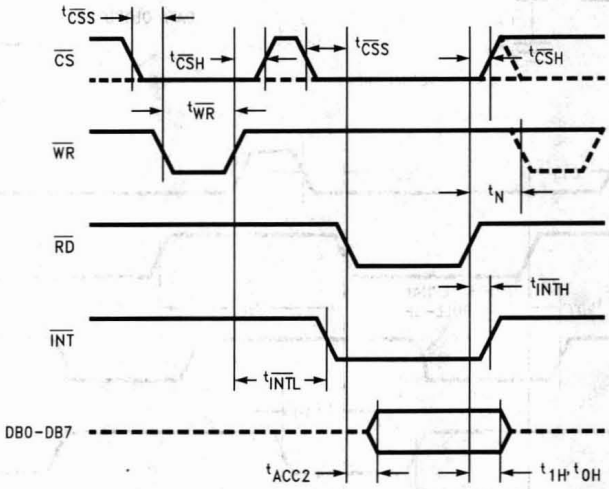


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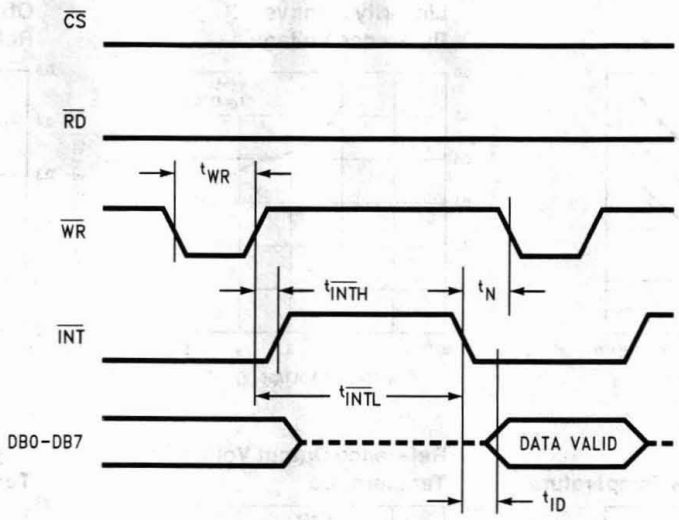
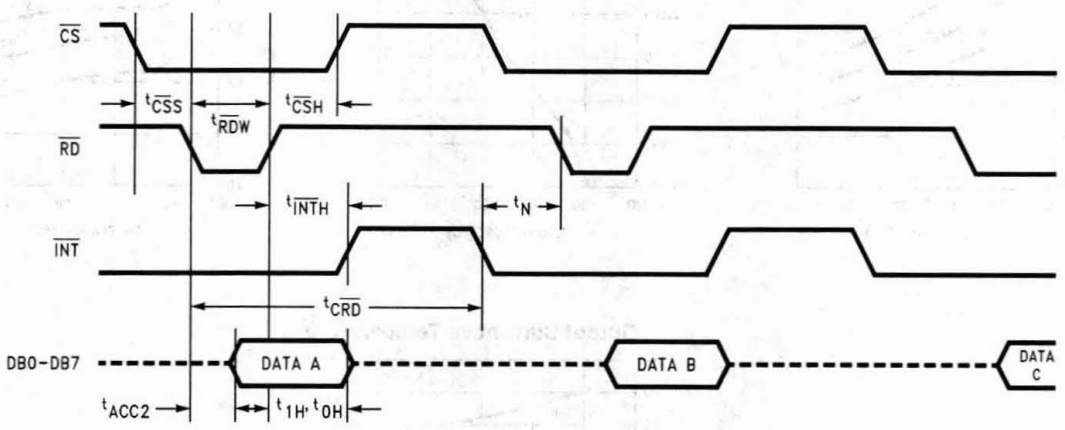
FIGURE 2b. $\overline{WR}$-$\overline{RD}$ Mode with $t_{RD} > t_{INTL}$ (Mode Pin is High)

TRI-STATE Test Circuit and Waveforms (Continued)



TL/H/11149-9

FIGURE 3. WR-RD Mode Reduced Interface System Connection with CS = RD = 0 (Mode Pin is High)



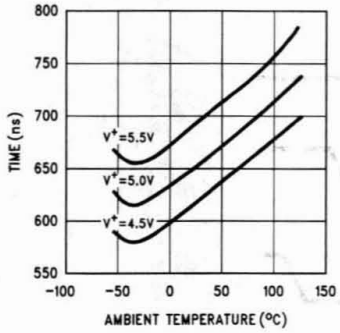
TL/H/11149-10

FIGURE 4. RD Mode (Pipeline Operation); t_{RDW} must be between 200 ns and 400 ns. (Mode Pin is Low)

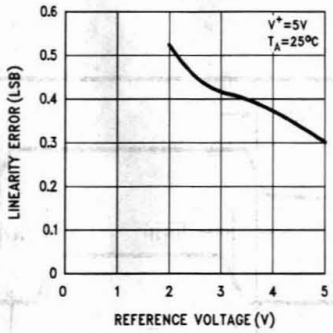
2

Typical Performance Characteristics

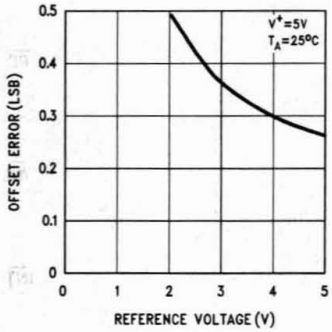
t_{CRD} vs Temperature



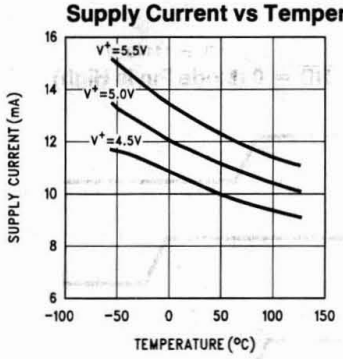
Linearity Error vs Reference Voltage



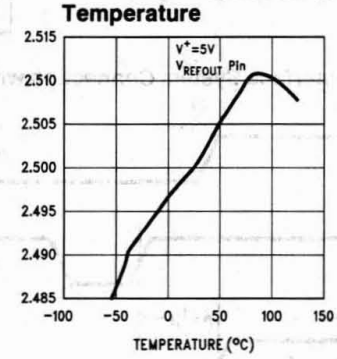
Offset Error vs Reference Voltage



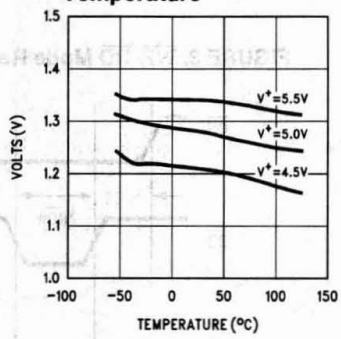
Supply Current vs Temperature



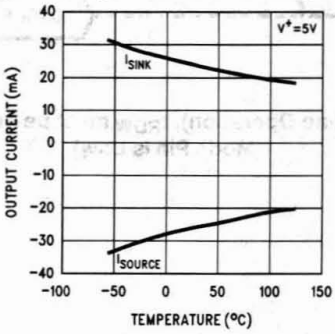
Reference Output Voltage vs Temperature



Logic Threshold vs Temperature



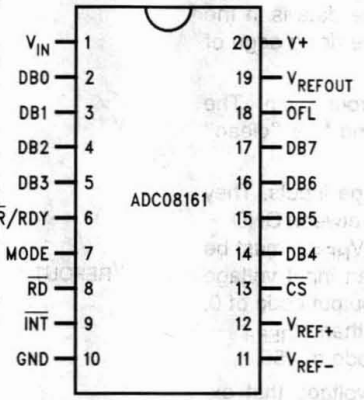
Output Current vs Temperature



TL/H/11149–11

Connection Diagram

Dual-In-Line and Wide-Body Small-Outline Packages



TL/H/11149–14

See NS Package Number N20A or M20A

Ordering Information

Industrial ($-40°C \leq T_A \leq 85°C$)	Package
ADC08161BIN, ADC08161CIN	N20A
ADC08161BIWM, ADC08161CIWM	M20B

Pin Description

V_{IN} This is the analog input. The input range is GND–50 mV $\leq V_{INPUT} \leq V^+ + 50$ mV.

DB0–DB7 TRI-STATE data outputs—bit 0 (LSB) through bit 7 (MSB).

$\overline{WR}$/RDY **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)

$\overline{WR}$: With $\overline{CS}$ low, the conversion is started on the rising edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (see *Figures 2a, 2b,* and *3*).

$\overline{RD}$ Mode (Logic low applied to MODE pin)

RDY: This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and returns high at the end of conversion.

MODE **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input–

This pin is pulled to a logic low through an internal 50 μA current sink when left unconnected.

$\overline{RD}$ Mode is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.

$\overline{WR}$-$\overline{RD}$ Mode is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.

$\overline{RD}$ **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin)

This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (see *Figures 2a, 2b* and *3*).

$\overline{RD}$ Mode (logic low on the MODE pin)

Pin Description (Continued)

With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (see *Figures 1* and *4*).

$\overline{INT}$ This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.

GND This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.

V_{REF-} V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} − 1.5 LSB produces an output code of 255.

For the ADC08161 an input voltage that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create conversion errors.

$\overline{CS}$ This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.

$\overline{OFL}$ Overflow Output. If the analog input is higher than V_{REF+}, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08161s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.

V^+ Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 μF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

V_{REFOUT} The internal bandgap reference's 2.5V output is available on this pin. Use a 220 μF bypass capacitor between this pin and analog ground.

Application Information

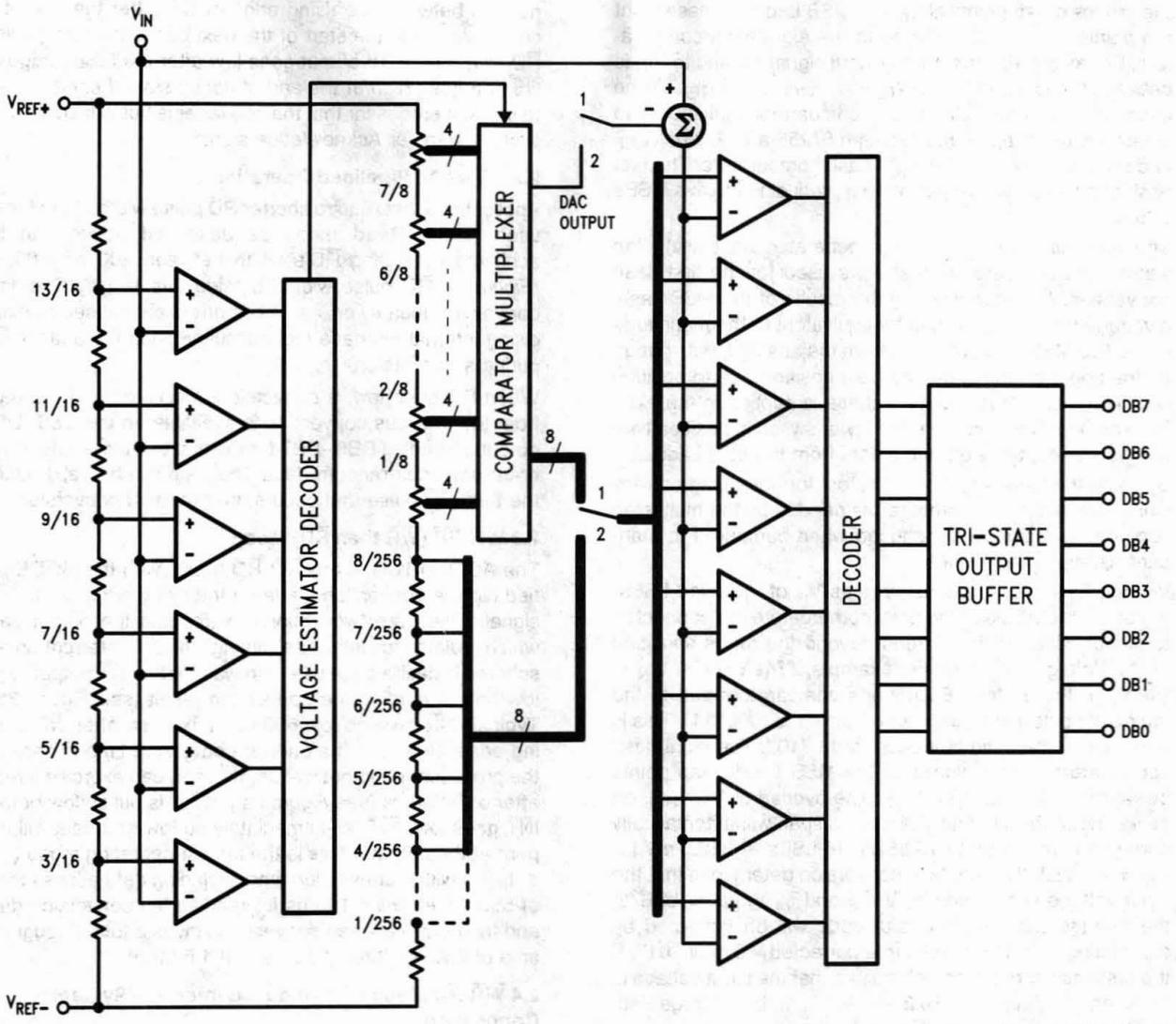


FIGURE 5. Block Diagram of the ADC08161 Multi-Step Flash Architecture

1.0 FUNCTIONAL DESCRIPTION

The ADC08161 performs an 8-bit analog-to-digital conversion using a multi-step flash technique. The first flash generates the five most significant bits (MSBs) and the second flash generates the three least significant bits (LSBs). *Figure 5* shows the major functional blocks of the ADC08161 multi-step flash converter. It consists of an over-encoded 2½-bit Voltage Estimator, an internal DAC with two different voltage spans, a 3-bit half-flash converter and a comparator multiplexer.

The resistor string near the center of the block diagram in *Figure 5* forms the internal main DAC. Each of the eight resistors at the bottom of the string is equal to 1/256 of the total string resistance. These resistors form the **LSB Ladder** and have a voltage drop of 1/256 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remaining resistors make up the **MSB Ladder**. They are made up of eight groups of four resistors connected in series. Each MSB Ladder section has ⅛ of the total reference voltage across it. Within a given MSB Ladder section, each of the MSB resistors has 8/256, or 1/32 of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB Ladders. Through the Comparator Multiplexer these tap points can be connected, in groups of eight, to the eight comparators shown at the right of *Figure 5*. This function provides the necessary reference voltages to the comparators during each flash conversion.

The six comparators, seven-resistor string (estimator DAC), and Estimator Decoder at the left of *Figure 5* form the Voltage Estimator. The estimator DAC connected between V_{REF+} and V_{REF-} generates the reference voltages for the six Voltage Estimator comparators. These comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is then used to control the Comparator Multiplexer, connecting the appropriate MSB Ladder section to the eight flash comparators. Only 14 comparators, six in the Voltage Estimator and eight in the flash converter, are needed to achieve the full eight-bit resolution, instead of 32 comparators that would be needed by traditional half-flash methods.

A conversion begins with the Voltage Estimator comparing the analog input signal against the six tap voltages on the estimator DAC. The estimator decoder then selects one of

Application Information (Continued)

the groups of tap points along the MSB Ladder. These eight tap points are then connected to the eight flash comparators. For example, if the analog input signal applied to V_{IN} is between 0 and $^3/_{16}$ of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the eight tap points between 8/256 and 2/8 of V_{REF} and connects them to the eight flash comparators. The first flash conversion is now performed, producing the five MSBs of data.

The remaining three LSBs are generated next using the same eight comparators that were used for the first flash conversion. As determined by the results of the MSB flash, a voltage from the MSB Ladder equivalent to the magnitude of the five MSBs is subtracted from the analog input voltage as the upper switch is moved from position one to position two. The resulting remainder voltage is applied to the eight flash comparators and, with the lower switch in position two, compared with the eight tap points from the LSB Ladder.

By using the same eight comparators for both flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard half-flash techniques.

Voltage Estimator errors as large as $^1/_{16}$ of V_{REF} (16 LSBs) will be corrected since the flash comparators are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if $^7/_{16}\ V_{REF} < V_{IN} < {}^9/_{16}\ V_{REF}$ the Voltage Estimator's comparators tied to the tap points below $^9/_{16}\ V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The eight flash comparators will be placed at the MSB Ladder tap points between $^3/_8\ V_{REF}$ and $^5/_8\ V_{REF}$. The overlap of $^1/_{16}\ V_{REF}$ on each side of the Voltage Estimator's span will automatically correct an error of up to 16 LSBs (16 LSBs = 312.5 mV for $V_{REF} = 5V$). If the first flash conversion determines that the input voltage is between $^3/_8\ V_{REF}$ and $^4/_8\ V_{REF}$ − LSB/2, the Voltage Estimator's output code will be corrected by subtracting "1". This results in a corrected value of "01". If the first flash conversion determines that the input voltage is between $^8/_{16}\ V_{REF}$ − LSB/2 and $^5/_8\ V_{REF}$, the Voltage Estimator's output code remains unchanged.

After correction, the 2-bit data from both the Voltage Estimator and the first flash conversion are decoded to produce the five MSBs. Decoding is similar to that of a 5-bit flash converter since there are 32 tap points on the MSB Ladder. However, 31 comparators are not needed since the Voltage Estimator places the eight comparators along the MSB Ladder where reference tap voltages are present that fall above and below the magnitude of V_{IN}. Comparators are not needed outside this selected range. If a comparator's output is a "0", all comparators above it will also have outputs of "0" and if a comparator's output is a "1", all comparators below it will also have outputs of "1".

2.0 DIGITAL INTERFACE

The ADC08161 has two basic interface modes which are selected by connecting the **MODE** pin to a logic high or low.

2.1 $\overline{RD}$ Mode

With a logic low applied to the **MODE** pin, the converter is set to **Read** mode. In this configuration (see *Figure 1*), a complete conversion is done by pulling $\overline{RD}$ low, and holding low, until the conversion is complete and output data appears. This typically takes 655 ns. The $\overline{INT}$ (interrupt) line goes low at the end of conversion. A typical delay of 50 ns is needed between the rising edge of $\overline{CS}$ (after the end of a conversion) and the start of the next conversion (by pulling $\overline{RD}$ low). The RDY output goes low after the falling edge of $\overline{CS}$ and goes high at the end-of-conversion. It can be used to signal a processor that the converter is busy or serve as a system Transfer Acknowledge signal.

2.2 $\overline{RD}$ Mode Pipelined Operation

Applications that require shorter $\overline{RD}$ pulse widths than those used in the **Read** mode as described above can be achieved by setting $\overline{RD}$'s width between 200 ns–400 ns *(Figure 4)*. $\overline{RD}$ pulse widths outside this range will create conversion linearity errors. These errors are caused by exercising internal interface logic circuitry using $\overline{CS}$ and/or $\overline{RD}$ during a conversion.

When $\overline{RD}$ goes low, a conversion is initiated and the data from the previous conversion is available on the DB0–DB7 outputs. Reading DB0–DB7 for the first two times after power-up produces random data. The data will be valid during the third $\overline{RD}$ pulse that occurs after the first conversion.

2.3 $\overline{WR}$-$\overline{RD}$ ($\overline{WR}$ then $\overline{RD}$) Mode

The ADC08161 is in the **$\overline{WR}$-$\overline{RD}$ mode** with the **MODE** pin tied high. A conversion starts on the rising edge of the $\overline{WR}$ signal. There are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for the $\overline{INT}$ output to go low before reading the conversion result (see *Figure 2b*). Typically, $\overline{INT}$ will go low 690 ns, maximum, after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 350 ns (see *Figure 2a*). If $\overline{RD}$ is pulled low before $\overline{INT}$ goes low, $\overline{INT}$ will immediately go low and data will appear at the outputs. This is the fastest operating mode ($t_{RD} \leq t_{INTL}$) with a conversion time, including data access time, of 560 ns. Allowing 100 ns for reading the conversion data and the delay between conversions gives a total throughput time of 660 ns (throughput rate of 1.5 MHz).

2.4 $\overline{WR}$-$\overline{RD}$ Mode with Reduced Interface System Connection

$\overline{CS}$ and $\overline{RD}$ can be tied low, using only $\overline{WR}$ to control the start of conversion for applications that require reduced digital interface while operating in the **$\overline{WR}$-$\overline{RD}$ mode** *(Figure 3)*. Data will be valid approximately 705 ns following $\overline{WR}$'s rising edge.

Application Information (Continued)

3.0 REFERENCE INPUTS

The ADC08161's two V_{REF} inputs are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to vary the span of the analog input since this range will be equivalent to the voltage difference between V_{REF+} and V_{REF-}. Transducers that have outputs that minimum output voltages above GND can also be compensated by connecting V_{REF-} to a voltage that is equal to this minimum voltage. By reducing V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF} = 2.5V$, then 1 LSB = 9.8 mV). The reference arrangement also facilitates ratiometric operation and in may cases the power supply can be used for transducer power as well as the V_{REF} source. Ratiometric operation is achieved by connecting V_{REF-} to GND and connecting V_{REF+} and a transducer's power supply input to V^+. The ADC08161s accuracy degrades when $V_{REF+} - |V_{REF-}|$ is less than 2.0V.

The voltage at V_{REF-} sets the input level that produces a digital output of all zeroes. Through V_{IN} is not itself differential, the reference design affords nearly differential-input capability for some measurement applications. *Figure 6* shows one possible differential configuration.

It should be noted that, while the two V_{REF} inputs are fully differential, the digital output will be zero for any analog input voltage if $V_{REF-} \geq V_{REF+}$.

4.0 ANALOG INPUT AND SOURCE IMPEDANCE

The ADC08161's analog input circuitry includes an analog switch with an "on" resistance of 70Ω and a 1.4 pF capacitor (see *Figure 6*). The switch is closed during the A/D's input signal acquisition time (while $\overline{WR}$ is low when using the $\overline{WR}$-$\overline{RD}$ Mode). A small transient current flows into the input pin each time the switch closes. A transient voltage, whose magnitude can increase as the source impedance increases, may be present at the input. So long as the source impedance is less than 500Ω, the input voltage transient will not cause errors and need not be filtered.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (100 ns maximum). A signal source with a high output impedance should have its output buffered with an operational amplifier. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Some suggested input configurations using the internal 2.5V reference, an external reference, and adjusting the input span are shown in *Figure 7*.

Correct conversion results will be obtained for input voltages greater than GND − 100 mV and less than V^+ + 100 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than V^+, or more than 300 mV lower than GND. The current flowing through any analog input pin should be limited to 5 mA or less to avoid permanent damage to the IC if an analog input pin is forced beyond these voltages. The sum of all the overdrive currents into all pins must be less than 20 mA. Some sort of protection scheme should be used when the input signal is expected to extend more than 300 mV beyond the power supply limits. A simple protection network using resistors and diodes is shown in *Figure 8*.

5.0 INHERENT SAMPLE-AND-HOLD

An important benefit of the ADC08161's input architecture is the inherent sample-and-hold (S/H) and its ability to measure relatively high speed signals without the help of an external S/H. In a non-sampling converter, regardless of its speed, the input must remain stable to at least ½ LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion.

The ADC08161 is suitable for DSP-based systems because of the direct control of the S/H through the $\overline{WR}$ signal. The $\overline{WR}$ input signal allows the A/D to be synchronized to a DSP system's sampling rate or to other ADC08161s.

The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

6.0 INTERNAL BANDGAP REFERENCE

The ADC08161 has an internal bandgap 2.5V reference that can be used as the V_{REF+} input. A parallel combination of a 0.1 μF ceramic capacitor and a 220 μF tantalum capacitor should be used to bypass the V_{REFOUT} pin. This reduces possible noise pickup that could cause conversion errors.

7.0 LAYOUT, GROUNDS, AND BYPASSING

In order to ensure fast, accurate conversions from the ADC08161, it is necessary to use appropriate circuit board layout techniques. Ideally, the analog-to-digital converter's ground reference should be low impedance and free of noise from other parts of the system. Digital circuits can produce a great deal of noise on their ground returns and, therefore, should have their own separate ground lines. Best performance is obtained using separate ground planes should be provided for the digital and analog parts of the system.

The analog inputs should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., an input filter capacitor) connected across the inputs should be returned to a very clean ground point. Incorrectly grounding the ADC08161 may result in reduced conversion accuracy.

The V^+ supply pin, V_{REF+}, and V_{REF-} (if not grounded) should be bypassed with a parallel combination of a 0.1 μF ceramic capacitor and a 10 μF tantalum capacitor placed as close as possible to the pins using short circuit board traces. See *Figures 7* and *8*.

Application Information (Continued)

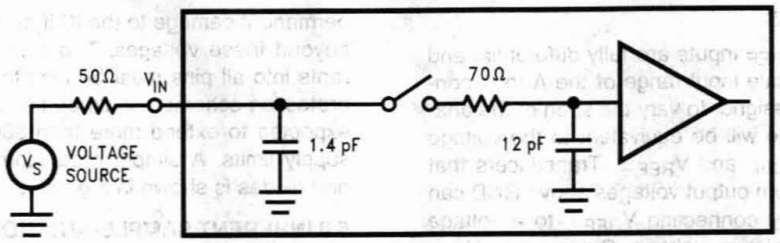
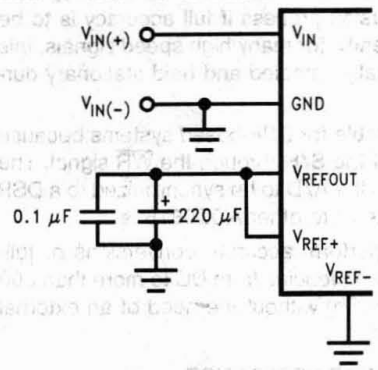
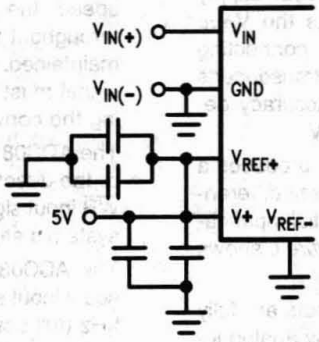


FIGURE 6. ADC08161 Equivalent Input Circuit Model

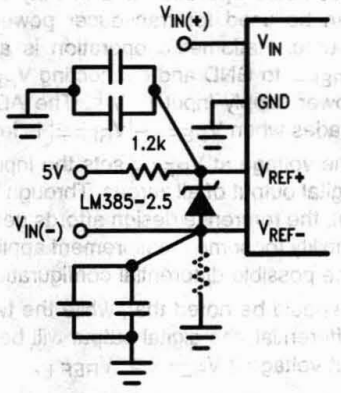
Internal Reference 2.5V Full-Scale (Standard Application)



Power Supply as Reference



Input Not Referred to GND



*Signal source driving $V_{IN}(-)$ must be capable of sinking 5 mA.

Note: Bypass capacitors consist of a 0.1 μF ceramic in parallel with a 10 μF bead tantalum, unless otherwise specified.

FIGURE 7. Analog Input Options

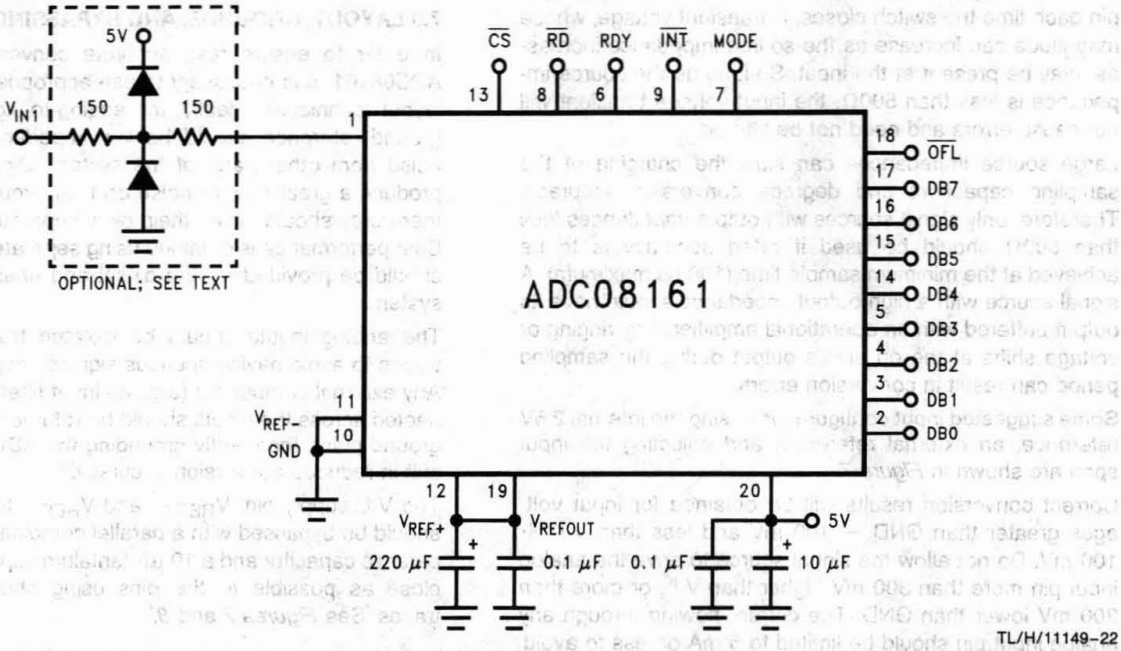


FIGURE 8. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. $V_{REF}-$ should be bypassed to analog ground using multiple capacitors if it is not grounded (See Section 7.0 "LAYOUT, GROUNDS, and BYPASSING"). V_{IN1} is shown with an optional input protection network.

National Semiconductor

ADC1001 10-Bit μP Compatible A/D Converter

General Description

The ADC1001 is a CMOS, 10-bit successive approximation A/D converter. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 10-bit resolution.

Features

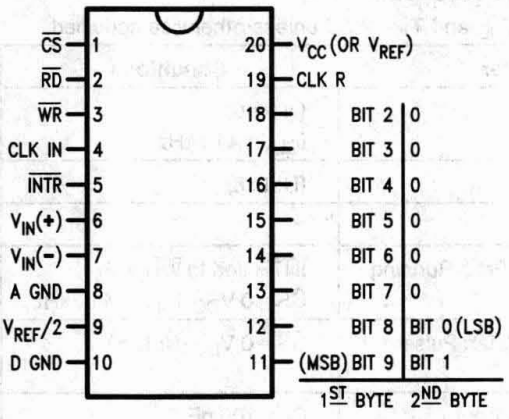
- ADC1001 is pin compatible with ADC0801 series 8-bit A/D converters
- Compatible with NSC800 and 8080 μP derivatives—no interfacing logic needed
- Easily interfaced to 6800 μP derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3″ standard width 20-pin DIP package

Key Specifications

■ Resolution	10 bits
■ Linearity error	±1 LSB
■ Conversion time	200μS

Connection Diagram

ADC1001 (for an 8-bit data bus)
Dual-In-Line Package



TL/H/5675–11

Top View

Ordering Information

Temperature Range	0°C to +70°C	−40°C to +85°C
Order Number	ADC1001CCJ-1	ADC1001CCJ
Package Outline	J20A	J20A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Logic Control Inputs	−0.3V to +18V
Voltage at Other Inputs and Outputs	−0.3V to (V_{CC} + 0.3V)
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 10)	800V

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1001CCJ	$-40°C \le T_A \le +85°C$
ADC1001CCJ-1	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Converter Characteristics

Converter Specifications: V_{CC} = 5 V_{DC}, $V_{REF}/2$ = 2.500 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 410 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Linearity Error Zero Error Full-Scale Error				±1 ±2 ±2	LSB LSB LSB
Total Ladder Resistance (Note 9)	Input Resistance at Pin 9	2.2	4.8		KΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.05		V_{CC} + 0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/8		LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ± 5% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/8		LSB

AC Electrical Characteristics

Timing Specifications: V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_c	Conversion Time	(Note 5) f_{CLK} = 410 kHz	80 195		90 220	$1/f_{CLK}$ μs
f_{CLK}	Clock Frequency	(Note 8)	100		1260	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 410 kHz			4600	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 6)	150			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		170	300	ns
t_{1H}, t_{0H}	TRI-STATE® Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
t_{1rs}	$\overline{INTR}$ to 1st Read Set-Up Time		550	400		ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5\ V_{DC}$ and $T_{MIN}\leq T_A\leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except CLK IN)	$V_{CC}=5.25\ V_{DC}$	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except CLK IN)	$V_{CC}=4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN}=5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" input Current (All Inputs)	$V_{IN}=0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN						
V_T+	CLK IN Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
OUTPUTS AND $\overline{\text{INTR}}$						
$V_{OUT}(0)$	Logical "0" Output Voltage	$I_{OUT}=1.6$ mA, $V_{CC}=4.75\ V_{DC}$			0.4	V_{DC}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-360\ \mu A$, $V_{CC}=4.75\ V_{DC}$ $I_O=-10\ \mu A$, $V_{CC}=4.75\ V_{DC}$	2.4 4.5			V_{DC} V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT}=0.4\ V_{DC}$ $V_{OUT}=5\ V_{DC}$		0.1 0.1	−100 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to GND, $T_A=25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A=25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	$f_{CLK}=410$ kHz, $V_{REF}/2=$ NC, $T_A=25°C$ and $\overline{CS}=1$		2.5	5.0	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-)\geq V_{IN}(+)$ the digital output code will be all zeros. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near fullscale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 1*.

Note 6: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).

Note 7: All typical values are for $T_A=25°C$.

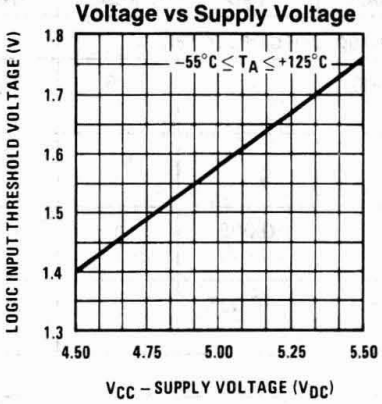
Note 8: Accuracy is guaranteed at $f_{CLK}=410$ kHz. At higher clock frequencies accuracy can degrade.

Note 9: The $V_{REF/2}$ pin is the center point of a two resistor divider (each resistor is 2.4kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors.

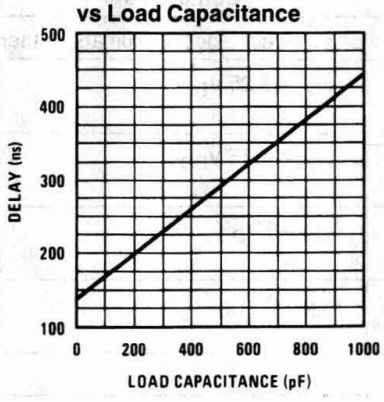
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

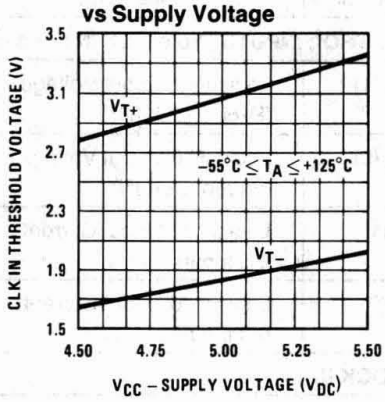
Logic Input Threshold Voltage vs Supply Voltage



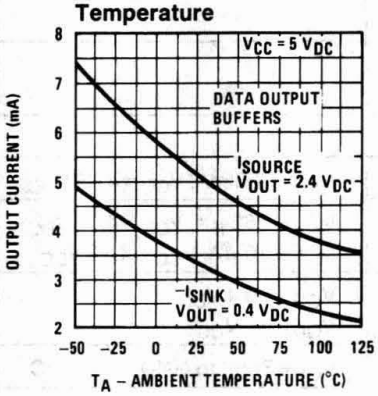
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



CLK IN Schmitt Trip Levels vs Supply Voltage



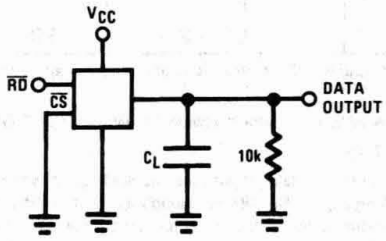
Output Current vs Temperature



TL/H/5675–2

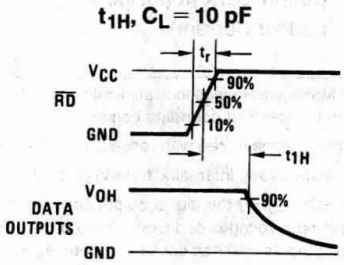
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/5675–3

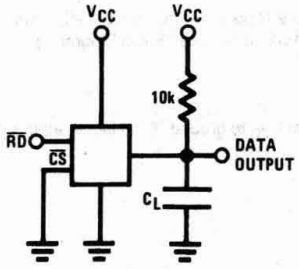
t_{1H}, $C_L = 10$ pF



TL/H/5675–4

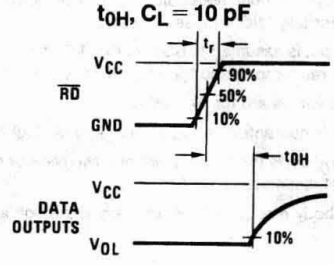
$t_r = 20$ ns

t_{0H}



TL/H/5675–5

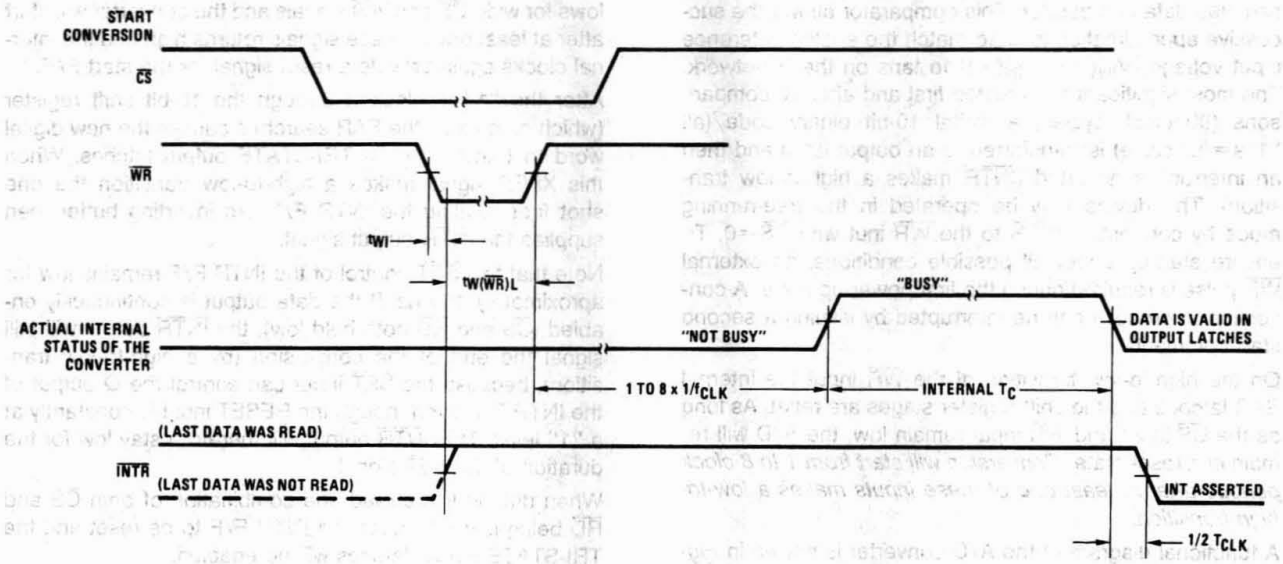
t_{0H}, $C_L = 10$ pF



TL/H/5675–6

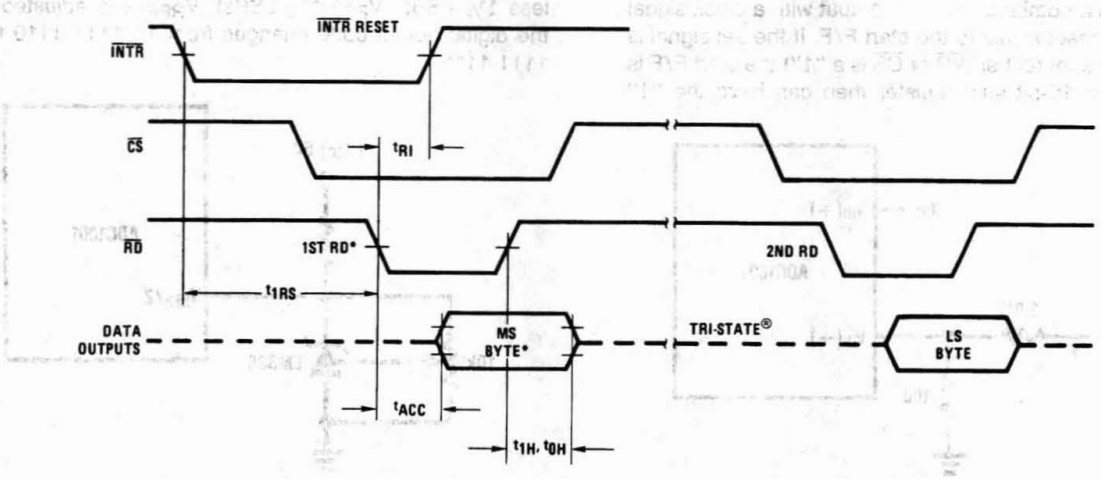
$t_r = 20$ ns

Timing Diagrams



TL/H/5675–7

Output Enable and Reset INTR



TL/H/5675–8

Note: All timing is measured from the 50% voltage points.

BYTE SEQUENCING FOR THE 20-PIN ADC1001

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Functional Description

The ADC1001 uses an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network, are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ inut with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion in process can be interrupted by issuing a second start command.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 1*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, which allows the conversion process to continue. If the set signal were to still be present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When this XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

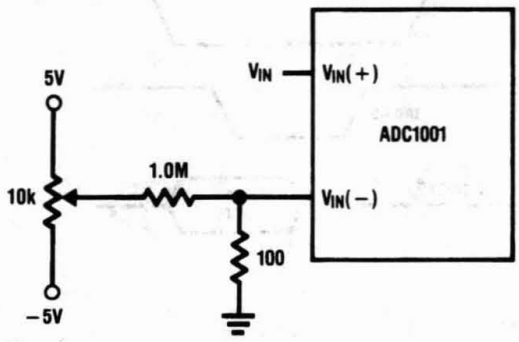
Note that this $\overline{SET}$ control of the INTR F/F remains low for aproximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

Zero and Full-Scale Adjustment

Zero error can be adjusted as shown in *Figure 2*. $V_{IN}(+)$ is forced to +2.5 mV (+½ LSB) and the potentiometer is adjusted until the digital output code changes from 00 0000 0000 to 00 0000 0001.

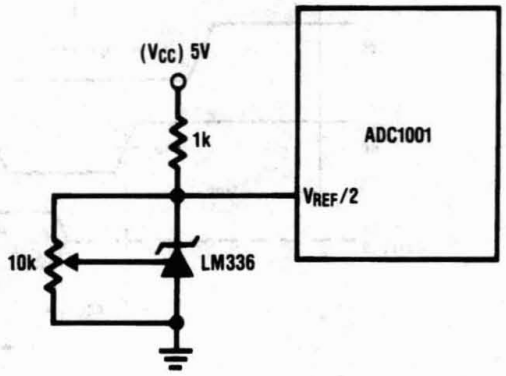
Full-scale is adjusted as shown in *Figure 3*, with the $V_{REF}/2$ input. With V_{IN} (+) forced to the desired full-scale voltage less 1½ LSBs ($V_{FS} - 1½$ LSBs), $V_{REF}/2$ is adjusted until the digital output code changes from 11 1111 1110 to 11 1111 1111.



TL/H/5675–9

NOTE: $V_{IN}(-)$ should be biased so that $V_{IN}(-) \geq -0.05V$ when potentiometer wiper is set at most negative voltage position.

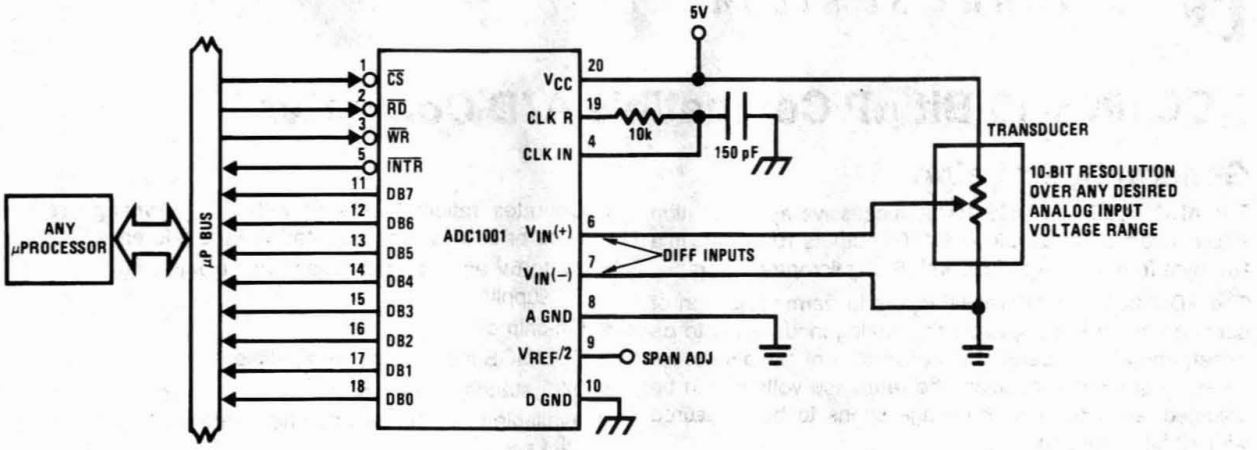
FIGURE 2. Zero Adjust Circuit



TL/H/5675–10

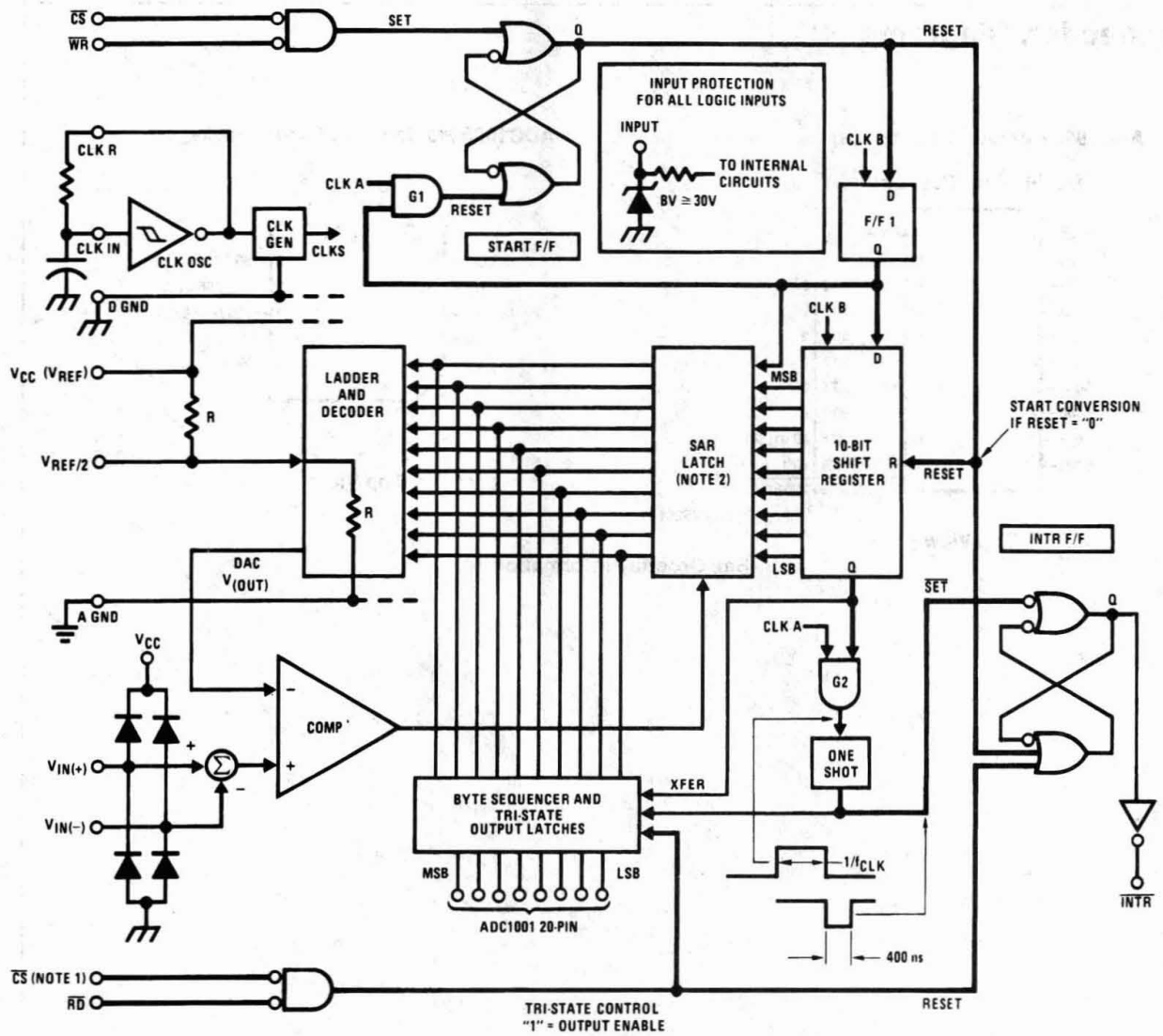
FIGURE 3. Full-Scale Adjust

Typical Application



TL/H/5675–1

Block Diagram



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

TL/H/5675–13

FIGURE 1

National Semiconductor

ADC1005 10-Bit μP Compatible A/D Converter

General Description

The ADC1005 is a CMOS 10-bit successive approximation A/D converter. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The ADC1005 has differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.

Features

- Easy interface to all microprocessors
- Differential analog voltage inputs
- Operates ratiometrically or with 5 V_{DC} voltage reference or analog span adjusted voltage reference
- 0V to 5V analog input voltage range with single 5V supply
- On-chip clock generator
- TLL/MOS input/output compatible
- 0.3" standard width 20-pin DIP
- Available in 20-pin molded chip carrier package

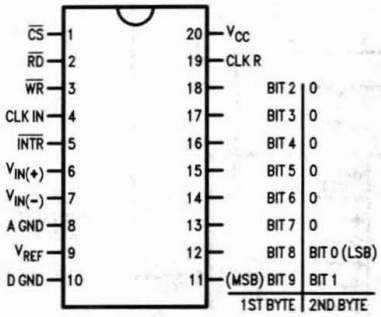
Key Specifications

■ Resolution	10 bits
■ Linearity Error	±½ LSB and ±1 LSB
■ Conversion Time	50 μs

Connection Diagrams

ADC1005 (for an 8-bit data bus)

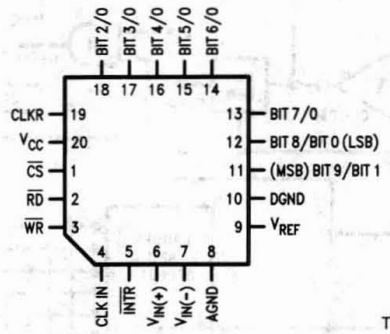
Dual-In-Line Package



TL/H/5261–1

Top View

ADC1005 Molded Chip Carrier Package



TL/H/5261–19

Top View

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Logic Control Inputs	−0.3V to +15V
Voltage at Other Inputs and Outputs	−0.3V to V_{CC} +0.3V
Input Current Per Pin	±5 mA
Input Current Per Package	±20 mA
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature	
(Soldering, 10 seconds)	
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	800V

Operating Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5V to 6.0V
Temperature Range	$T_{MN} \le T_A \le T_{MAX}$
ADC1005BCJ, ADC1005CCJ	$-40°C \le T_A \le +85°C$
ADC1005BCJ-1, ADC1005CCJ-1, ADC1005CCV	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 1.8 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC1005BCJ ADC1005CCJ			ADC1005BCJ-1, ADC1005CCJ-1 ADC1005CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
Converter Characteristics								
Linearity Error (Note 3)								
ADC1005BCJ			**±0.5**					LSB
ADC1005BCJ-1						±0.5	**±0.5**	LSB
ADC1005CCJ			**±1**					LSB
ADC1005CCJ-1, CCV						±1	**±1**	LSB
Zero Error								
ADC1005BCJ			**±0.5**					LSB
ADC1005BCJ-1						±0.5	**±0.5**	LSB
ADC1005CCJ			**±1**					LSB
ADC1005CCJ-1, CCV						±1	**±1**	LSB
Fullscale Error								
ADC1005BCJ			**±0.5**					LSB
ADC1005BCJ-1						±0.5	**±0.5**	LSB
ADC1005CCJ			**±1**					LSB
ADC1005CCJ-1, CCV						±1	**±1**	LSB
Reference Input Resistance MIN		4.8	**2.2**		4.8	2.4	**2.2**	kΩ
Reference Input Resistance MAX		4.8	**8.3**		4.8	7.6	**8.3**	kΩ
Common-Mode Input (Note 4) MIN	$V_{IN}(+)$ or $V_{IN}(-)$		**V_{CC} + 0.05**			V_{CC} + 0.05	**V_{CC} + 0.05**	V
Common-Mode Input (Note 4) MAX	$V_{IN}(+)$ or $V_{IN}(-)$		**GND − 0.05**			GND − 0.05	**GND − 0.05**	V
DC Common-Mode Error	Over Common-Mode Input Range	±1/8	±1/4		±1/8	±1/4	±1/4	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±5% V_{REF} = 4.75V	±1/8	±1/4		±1/8	±1/4	±1/4	LSB

Electrical Characteristics (Continued) The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = 1.8 MHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC1005BCJ ADC1005CCJ			ADC1005BCJ-1, ADC1005CCJ-1 ADC1005CCV			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
DC Characteristics								
$V_{IN(1)}$ Logical "1" Input Voltage MIN	V_{CC} = 5.25V (except CLK_{IN})		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage MAX	V_{CC} = 4.75V (Except CLK_{IN})		**0.8**			0.8	**0.8**	V
I_{IN}, Logical "1" Input Current MAX	V_{IN} = 5.0V	0.005	**1**		0.005	1	**1**	μA
I_{IN}, Logical "0" Input Current MAX	V_{IN} = 0V	−0.005	**−1**		−0.005	−1	**−1**	μA
$V_{T+(MIN)}$, Minimum CLK_{IN} Positive going Threshold Voltage		3.1	**2.7**		3.1	2.7	**2.7**	V
$V_{T(MAX)}$, Maximum CLK_{IN} Positive going Threshold Voltage		3.1	**3.5**		3.1	3.5	**3.5**	V
$V_{T-(MIN)}$, Minimum CLK_{IN} Negative going Threshold Voltage		1.8	**1.5**		1.8	1.5	**1.5**	V
$V_{T-(MAX)}$, Maximum CLK_{IN} Negative going Threshold Voltage		1.8	**2.1**		1.8	2.1	**2.1**	V
$V_{H(MIN)}$, Minimum CLK_{IN} Hysteresis (V_{T+}-V_{T-})		1.3	**0.6**		1.3	0.6	**0.6**	V
$V_{H(MAX)}$, Maximum CLK_{IN} Hysteresis (V_{T+}-V_{T-})		1.3	**2.0**		1.3	2.0	**2.0**	V
$V_{OUT(1)}$, Logical "1" Output Voltage MIN	V_{CC} = 4.75V I_{OUT} = −360 μA I_{OUT} = −10 μA		**2.4** **4.5**			2.8 4.6	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage MAX	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current MAX	V_{OUT} = 0V V_{OUT} = 5V	−0.01 0.01	**−3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current MIN	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current MIN	V_{OUT} = 5V	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current MAX	f_{CLK} = 1.8 MHz $\overline{CS}$ = "1"	1.5	**3**		1.5	2.5	**3**	mA

AC Electrical Characteristics The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
f_{CLK}, Clock Frequency MIN			0.2	0.2	MHz
MAX			2.6	2.6	MHz
Clock Duty Cycle MIN			40	40	%
MAX			60	60	%

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{REF} = 5V, $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** All other limits $T_A = T_j$ = 25°C. (Continued)

Parameter		Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
t_C, Conversion Time	MIN			80	80	$1/f_{CLK}$
	MAX			90	90	$1/f_{CLK}$
	MIN	f_{CLK} = 1.8 MHz		45	45	μs
	MAX	f_{CLK} = 1.8 MHz		50	50	μs
$t_{W(\overline{WR})L}$, Minimum $\overline{WR}$ Pulse Width		$\overline{CS}$ = 0	100	150	150	ns
t_{ACC}, Access Time (Delay from falling edge of $\overline{RD}$ to Output Data Valid)		$\overline{CS}$ = 0 C_L = 100 pF, R_L = 2k	170	300	300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)		R_L = 10k, C_L = 10 pF R_L = 2k, C_L = 100 pF	125 145	 230	200 230	ns ns
t_{WI}, t_{RI}, Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	450	ns
t_{IRS}, $\overline{INTR}$ to 1st Read Set-up Time			400	550	550	ns
C_{IN}, Capacitance of Logic Inputs			5		7.5	pF
C_{OUT}, Capacitance of Logic Outputs			5		7.5	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through the end points of the transfer characteristic.

Note 4: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 00 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

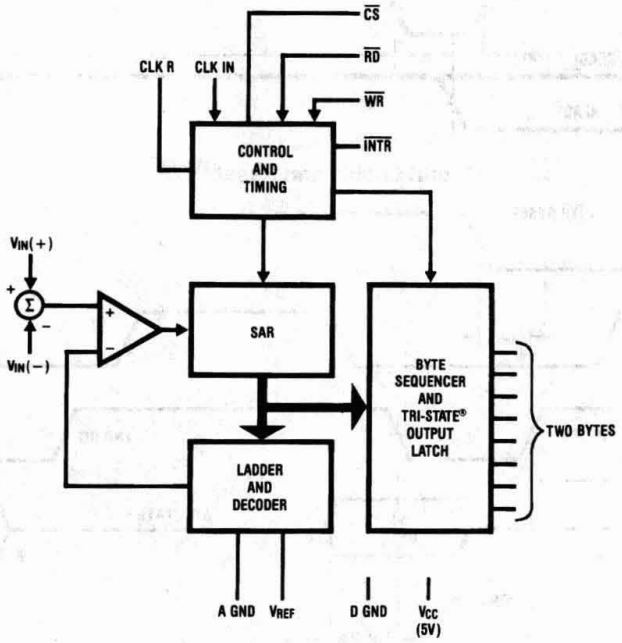
Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Diagram



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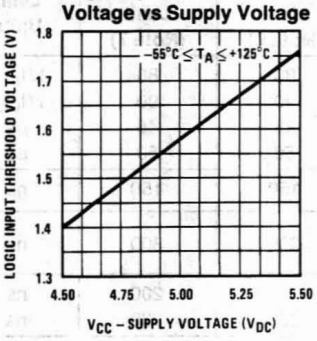
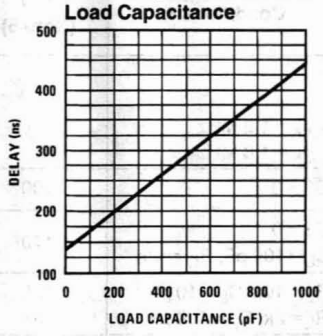
Typical Performance Characteristics

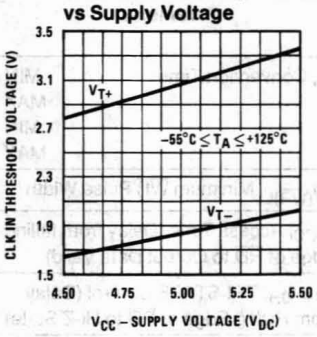
Logic Input Threshold Voltage vs Supply Voltage



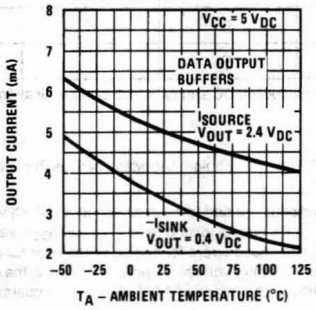
Delay from Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



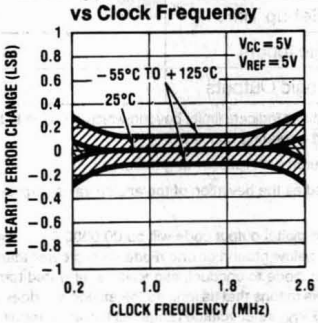
CLK IN Schmitt Trip Levels vs Supply Voltage



Output Current vs Temperature



Typical Linearity Error vs Clock Frequency



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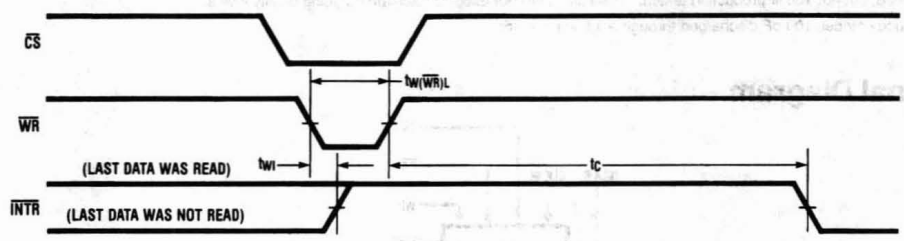
Timing Diagrams

Start Conversion



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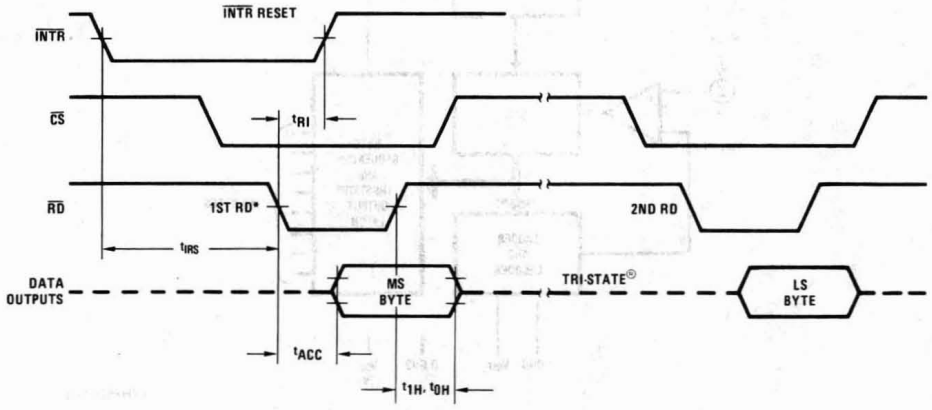
Output Enable and Reset $\overline{INTR}$



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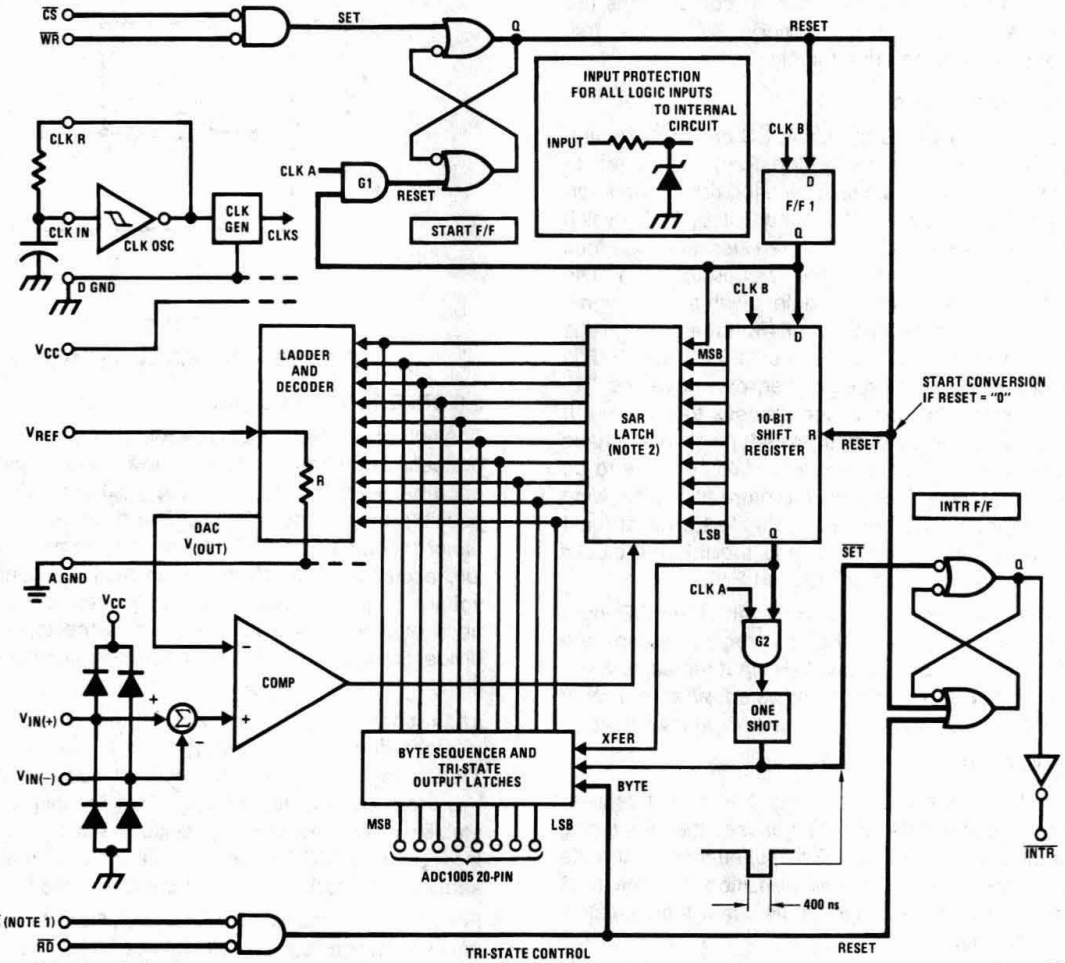
Note: All timing is measured from the 50% voltage points.

Timing Diagrams (Continued)

Byte Sequencing for ADC1005

Byte Order	8-Bit Data Bus Connection							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1st	MSB Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2
2nd	Bit 1	LSB Bit 0	0	0	0	0	0	0

Block Diagram



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

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FIGURE 1.

Functional Description

1.0 GENERAL OPERATION

A block diagram of the A/D converter is shown in *Figure 1* All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

1.1 Converter Operation

The ADC1005 uses an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog input voltage [$V_{IN}(+) - V_{IN}(-)$] to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch.

1.2 Starting a Conversion

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 10-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q ouput of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, allowing the conversion process to continue. If the set signal were still present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals. The converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

To summarize, on the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start after at least one of these inputs makes a low-to-high transition.*

1.3 Output Control

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When the XFER signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal.

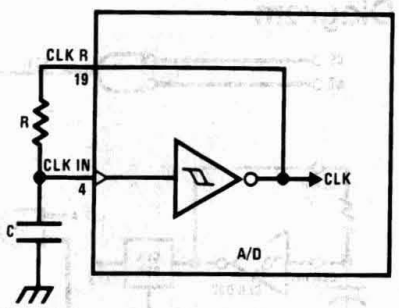
Note that this $\overline{SET}$ control of the INTR F/F remains low for approximately 400 ns. If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low) the $\overline{INTR}$ output will still signal the end of the conversion (by a high-to-low transition). This is because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

1.4 Free-Running and Self-Clocking Modes

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to ensure start up.

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN makes use of a Schmitt trigger as shown in *Figure 2.*



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$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

FIGURE 2. Self-Clocking the A/D

2.0 REFERENCE VOLTAGE

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 1024 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 4.8 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 3a*) the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system references as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 3b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be small to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout, and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/1024$).

Functional Description (Continued)

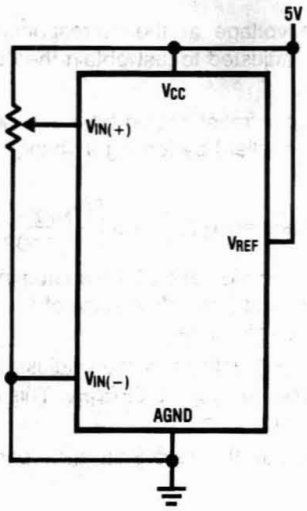

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FIGURE 3a. Ratiometric

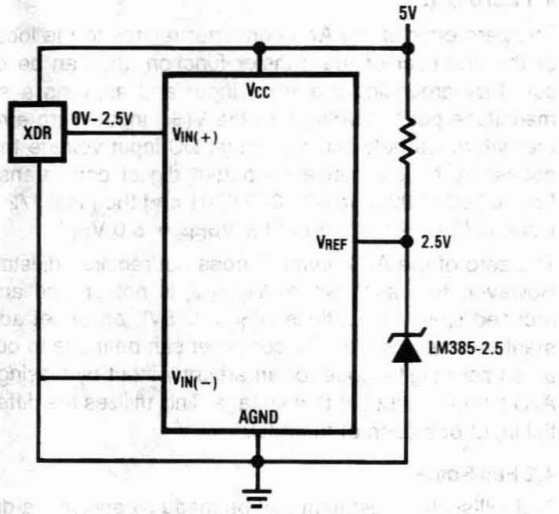

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FIGURE 3b. Absolute with a Reduced Span

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of these converters reduce the effects of common-mode input noise, which is defined as noise common to both selected "+" and "−" inputs (60 Hz is most typical). The time interval between sampling the "+" input and the "−" input is half of an internal clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal, this error is:

$$V_{ERROR(MAX)} = V_{PEAK}\,(2\pi\, f_{CM}) \times \frac{4}{f_{CLK}}$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the clock frequency at the CLK IN pin.

For a 60 Hz common-mode signal to generate a 1/4 LSB error (1.2 mV) with the converter running at 1.8 MHz, its peak value would have to be 1.46V. A common-mode signal this large is much greater than that generally found in data aquisition systems.

3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock rising edges during the conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

3.3 Input Bypass Capacitors

Bypass capacitors at the inputs will average the current spikes noted in 3.2 and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full scale. For continuous conversions with a 1.8 MHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the V_{REF} pin* for high resistance sources (>1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a linear function of the differential input voltage.

3.4 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* if the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications (≤0.1 kΩ) a 4700 pF bypass capacitor at the inputs will prevent pickup due to series lead induction of a long wire. A 100Ω series resistor can be used to isolate this capacitor – both the R and the C are placed outside the feedback loop – from the output of an op amp, if used.

3.5 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 1 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, can reduce system noise pickup but can create analog scale errors. See section 3.2, 3.3, and 3.4 if input filtering is to be used.

Functional Description (Continued)

4.0 OFFSET AND REFERENCE ADJUSTMENT

4.1 Zero Offset

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V(−) input and applying a small magnitude positive voltage to the V(+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 00 0000 0000 to 00 0000 0001 and the ideal 1/2 LSB value (1/2 LSB = 2.45 mV for V_{REF} = 5.0 V_{DC}).

The zero of the A/D normally does not require adjustment. However, for cases where $V_{IN(MIN)}$ is not ground and in reduced span applications (V_{REF} < 5V), an offset adjustment may be desired. The converter can be made to output an all zero digital code for an arbitrary input by biasing the A/D's $V_{IN}(-)$ input at that voltage. This utilizes the differential input operation of the A/D.

4.2 Full Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code that is just changing from 11 1111 1110 to 11 1111 1111.

4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus 1/2 LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/1024) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 000_{HEX} 001_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input given by:

$$V_{IN}(+) \text{ FS adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{1024}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced).

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from $3FF_{HEX}$ to $3FE_{HEX}$. This completes the adjustment procedure.

For an example see the Zero-Shift and Span-Adjust circuit below.

5.0 POWER SUPPLIES

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and the other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to the digital ground. Any V_{REF} bypass capacitors, analog input filters capacitors, or input signal shielding should be returned to the analog ground point.

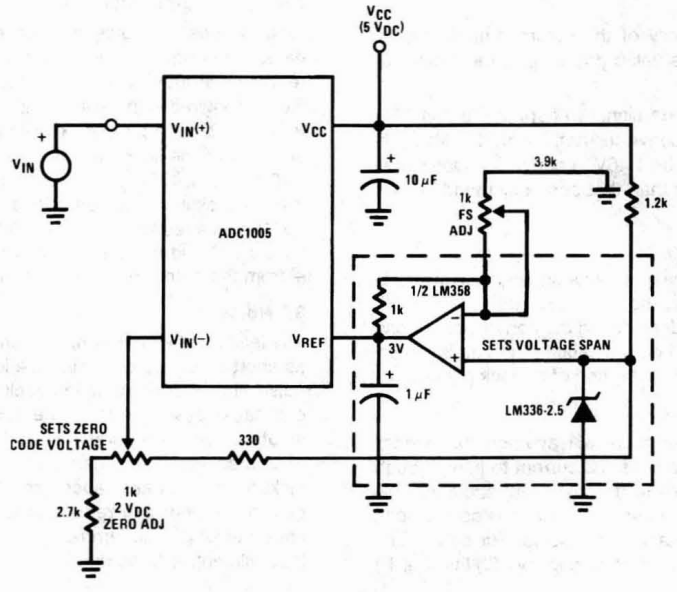

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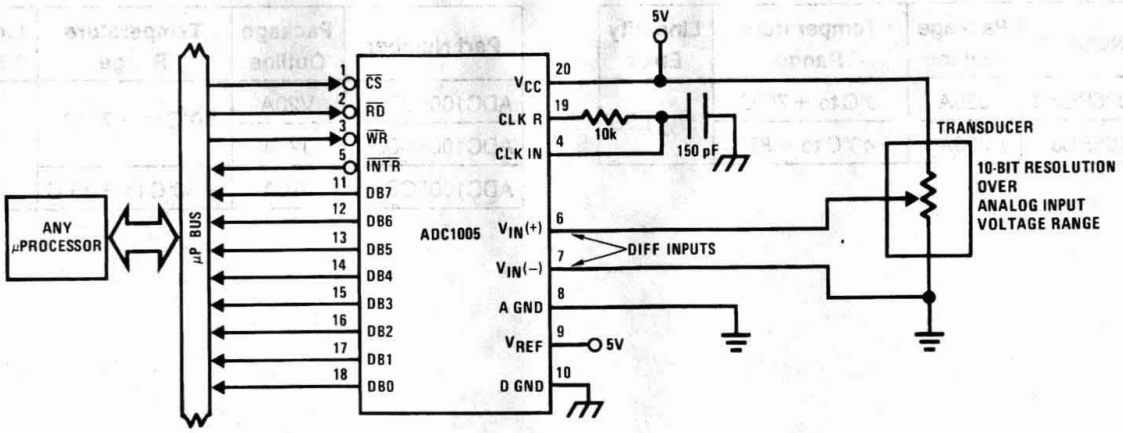
Figure 4. Zero-Shift and Span-Adjust (2V ≤ V_{IN} ≤ 5V)

Typical Applications



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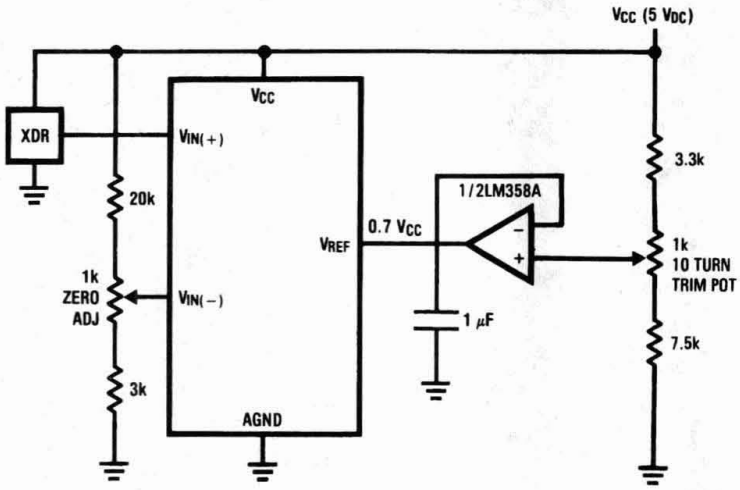
Operating with Ratiometric Transducers



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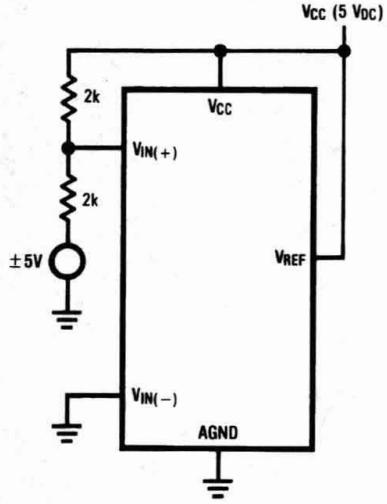
$V_{IN}(-) = 0.15\ V_{CC}$

$15\%\ \text{of}\ V_{CC} \leq V_{XDR} \leq 85\%\ \text{of}\ V_{CC}$

Handling ±5V Analog Inputs



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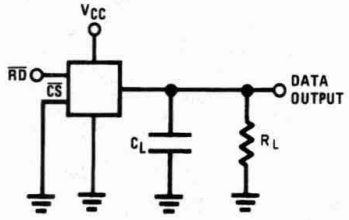
TRI-STATE Test Circuits and Waveforms

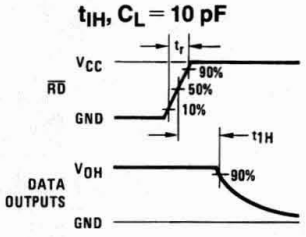
t_{1H}



TL/H/5261–7

$t_r = 20$ ns

t_{1H}, $C_L = 10$ pF



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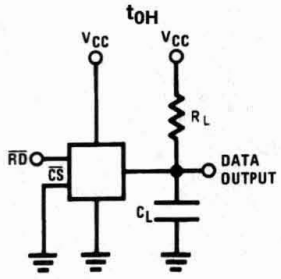
t_{OH}



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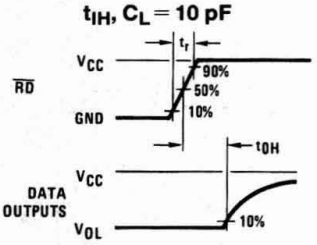
$t_r = 20$ ns

t_{1H}, $C_L = 10$ pF



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Ordering Information

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005BCJ-1	J20A	0°C to +70°C	±½ LSB
ADC1005BCJ	J20A	−40°C to +85°C	

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005CCV	V20A	0°C to +70°C	±1 LSB
ADC1005CCJ-1	J20A		
ADC1005CCJ	J20A	−40°C to +85°C	

National Semiconductor

ADC10154, ADC10158 10-Bit Plus Sign 4 μs ADCs with 4- or 8-Channel MUX, Track/Hold and Reference

General Description

The ADC10154 and ADC10158 are CMOS 10-bit plus sign successive approximation A/D converters with versatile analog input multiplexers, track/hold function and a 2.5V band-gap reference. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The input track/hold is implemented using a capacitive array and sampled-data comparator.

Resolution can be programmed to be 8-bit, 8-bit plus sign, 10-bit or 10-bit plus sign. Lower-resolution conversions can be performed faster.

The variable resolution output data word is read in two bytes, and can be formatted left justified or right justified, high byte first.

Applications

- Process control
- Instrumentation
- Test equipment

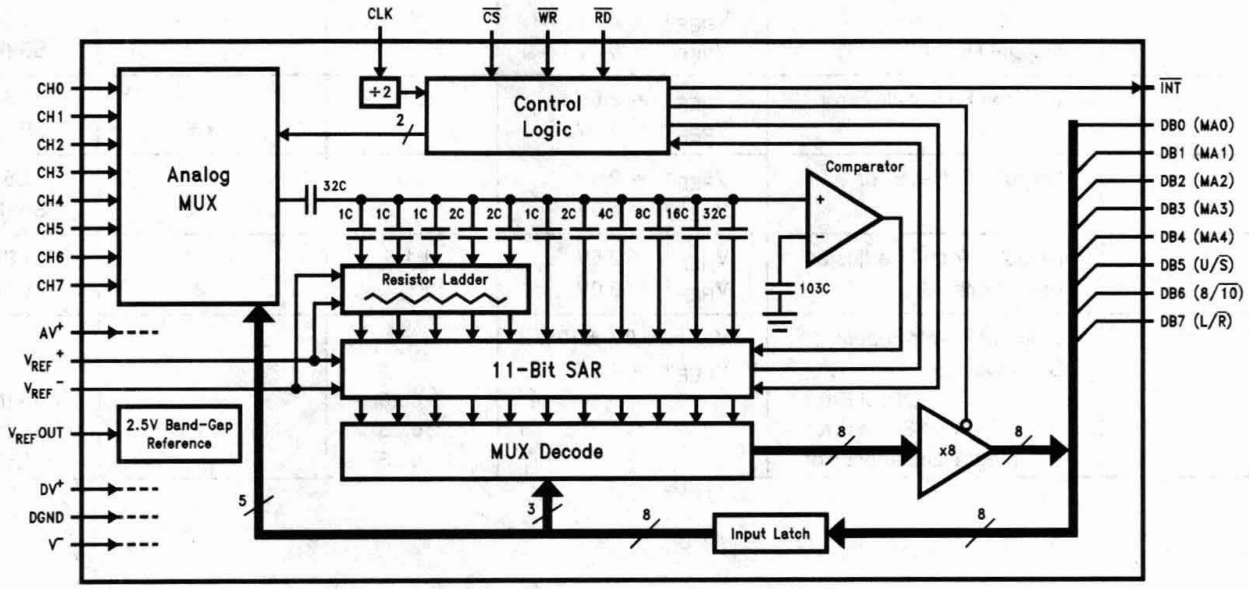
Features

- 4- or 8- channel configurable multiplexer
- Analog input track/hold function
- 0V to 5V analog input range with single +5V power supply
- −5V to +5V analog input voltage range with ±5V supplies
- Fully tested in unipolar (single +5V supply) and bipolar (dual ±5V supplies) operation
- Programmable resolution/speed and output data format
- Ratiometric or Absolute voltage reference operation
- No zero or full scale adjustment required
- No missing codes over temperature
- Easy microprocessor interface

Key Specifications

Resolution	10-bit plus sign
Integral linearity error	±1 LSB (max)
Unipolar power dissipation	33 mW (max)
Conversion time (10-bit + sign)	4.4 μs (max)
Conversion time (8-bit)	3.2 μs (max)
Sampling rate (10-bit + sign)	166 kHz
Sampling rate (8-bit)	207 kHz
Band-gap reference	2.5V ±2.0% (max)

ADC10158 Simplified Block Diagram



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Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage ($V^+ = AV^+ = DV^+$)	6.5V
Negative Supply Voltage (V^-)	−6.5V
Total Supply Voltage ($V^+ - V^-$)	13V
Total Reference Voltage ($V_{REF}^+ - V_{REF}^-$)	6.6V
Voltage at Inputs and Outputs	V^- − 0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Package Dissipation at T_A = 25°C (Note 5)	500 mW
ESD Susceptibility (Note 6)	2000V
Soldering Information	
N Packages (10 Sec)	260°C
J Packages (10 Sec)	300°C
SO Package (Note 7):	
Vapor Phase (60 Sec)	215°C
Infrared (15 Sec)	220°C
Storage Temperature	
Ceramic DIP Packages	−65°C to +150°C
Plastic DIP and SO Packages	−40°C to +150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10154CIN, ADC10154CIWM, ADC10158CIN, ADC10158CIWM	−40°C ≤ T_A ≤ +85°C
Positive Supply Voltage ($V^+ = AV^+ = DV^+$)	4.5 V_{DC} to 5.5 V_{DC}
Unipolar Negative Supply Voltage (V^-)	DGND
Bipolar Negative Supply Voltage (V^-)	−4.5V to −5.5V
$V^+ - V^-$	11V
V_{REF}^+	AV^+ + 0.05 V_{DC} to V^- − 0.05 V_{DC}
V_{REF}^-	AV^+ + 0.05 V_{DC} to V^- − 0.05 V_{DC}
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	0.5 V_{DC} to V^+

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+$ = + 5.0 V_{DC}, V_{REF}^+ = 5.000 V_{DC}, V_{REF}^- = GND, V^- = GND for unipolar operation or V^- = −5.0 V_{DC} for bipolar operation, and f_{CLK} = 5.0 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Notes 8, 9, and 12)

Symbol	Parameter	Conditions	Typical (Note 10)	CIN and CIWM Suffixes Limits (Note 11)	Units (Limit)
UNIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Resolution			**10 + Sign**	Bits
	Unipolar Integral Linearity Error	V_{REF}^+ = 2.5V V_{REF}^+ = 5.0V	±0.5	 **±1**	LSB LSB (Max)
	Unipolar Full-Scale Error	V_{REF}^+ = 2.5V V_{REF}^+ = 5.0V	±0.5	 **±1.5**	LSB LSB (Max)
	Unipoiar Offset Error	V_{REF}^+ = 2.5V V_{REF}^+ = 5.0V	±1	 **±1.5**	LSB LSB (Max)
	Unipolar Total Unadjusted Error (Note 13)	V_{REF}^+ = 2.5V V_{REF}^+ = 5.0V	±1.5	 **±2**	LSB LSB (Max)
	Unipolar Power Supply Sensitivity	V^+ = +5V ±10% V_{REF}^+ = 4.5V			
	Offset Error		±0.25	**±1**	LSB (Max)
	Full-Scale Error		±0.25	**±1**	LSB (Max)
	Integral Linearity Error		±0.25		LSB

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 8, 9, and 12) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	CIN and CIWM Suffixes Limits (Note 11)	Units (Limit)
BIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Resolution			**10 + Sign**	Bits
	Bipolar Integral Linearity Error	$V_{REF}^+ = 5.0V$		**±1**	LSB (Max)
	Bipolar Full-Scale Error	$V_{REF}^+ = 5.0V$		**±1.25**	LSB (Max)
	Bipolar Negative Full-Scale Error with Positive-Full Scale Adjusted	$V_{REF}^+ = 5.0V$		**±1.25**	LSB (Max)
	Bipolar Offset Error	$V_{REF}^+ = 5.0V$		**±2.5**	LSB (Max)
	Bipolar Total Unadjusted Error (Note 13)	$V_{REF}^+ = 5.0V$		**±3**	LSB (Max)
	Bipolar Power Supply Sensitivity				
	Offset Error	$V^+ = +5V \pm 10\%$	±0.5	**±2.5**	LSB (Max)
	Full-Scale Error	$V_{REF}^+ = 4.5V$	±0.5	**±1.5**	LSB (Max)
	Integral Linearity Error		±0.25		LSB
	Offset Error	$V^- = -5V \pm 10\%$	±0.25	**±0.75**	LSB (Max)
	Full-Scale Error	$V_{REF}^+ = 4.5V$	±0.25	**±0.75**	LSB (Max)
	Integral Linearity Error		±0.25		LSB
UNIPOLAR AND BIPOLAR CONVERTER AND MULTIPLEXER STATIC CHARACTERISTICS					
	Missing Codes			**0**	
	DC Common Mode Error (Note 14)	$V_{IN}^+ = V_{IN}^- = V_{IN}$ where			
	Bipolar	$+5.0V \geq V_{IN} \geq -5.0V$	±0.25	**±0.75**	LSB (Max)
	Unipolar	$+5.0V \geq V_{IN} \geq 0V$	±0.25	**±0.5**	LSB (Max)
R_{REF}	Reference Input Resistance		7	**4.5**	kΩ (Max)
				9.5	kΩ (Max)
C_{REF}	Reference Input Capacitance		70		pF
V_{AI}	Analog Input Voltage			**($V^+ + 0.05$)**	V (Max)
				($V^- - 0.05$)	V (Min)
C_{AI}	Analog Input Capacitance		30		pF
	Off Channel Leakage Current (Note 15)	On Channel = 5V, Off Channel = 0V	−400	**−1000**	nA (Max)
		On Channel = 0V, Off Channel = 5V	400	**1000**	nA (Max)

2

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 5.000\ V_{DC}$, $V_{REF}^- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 8, 9, and 12) (Continued)

Symbol	Parameter		Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
DYNAMIC CONVERTER AND MULTIPLEXER CHARACTERISTICS						
S/(N+D)	Unipolar Signal-to-Noise+ Distortion Ratio		$f_{IN} = 10$ kHz, $V_{IN} = 4.85\ V_{p-p}$ $f_{IN} = 150$ kHz, $V_{IN} = 4.85\ V_{p-p}$	60 58		dB dB
S/(N+D)	Bipolar Signal-to-Noise+ Distortion Ratio		$f_{IN} = 10$ kHz, $V_{IN} = \pm 4.85V$ $f_{IN} = 150$ kHz, $V_{IN} = \pm 4.85V$	60 58		dB dB
	−3 dB Unipolar Full Power Bandwidth		$V_{IN} = 4.85\ V_{p-p}$	200		kHz
	−3 dB Bipolar Full Power Bandwidth		$V_{IN} = \pm 4.85V$	200		kHz
REFERENCE CHARACTERISTICS (Unipolar Operation $V^- = GND$ Only)						
$V_{REF}Out$	Reference Output Voltage			2.5 ±1%	**2.5 ± 2%**	V (Max)
$\Delta V_{REF}/\Delta t$	$V_{REF}Out$ Temperature Coefficient			40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation	Sourcing	$0\ mA \le I_L \le +4\ mA$	0.003	**0.1**	%/mA (Max)
		Sinking	$0\ mA \ge I_L \ge -1\ mA$	0.2	**0.6**	%/mA (Max)
	Line Regulation		$4.5V \le V^+ \le 5.5V$	0.5	**6**	mV (Max)
I_{SC}	Short Circuit Current		$V_{REF}Out = 0V$	14	**25**	mA (Max)
$\Delta V_{REF}/\Delta t$	Long-Term Stability			200		ppm/1 kHr
t_{SU}	Start-Up Time		$C_L = 330\ \mu F$	20		ms
DIGITAL AND DC CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V^+ = 5.5V$		**2.0**	V (Min)
$V_{IN(0)}$	Logical "0" Input Voltage		$V^+ = 4.5V$		**0.8**	V (Max)
$I_{IN(1)}$	Logical "1" Input Current		$V_{IN} = 5.0V$	0.005	**2.5**	μA (Max)
$I_{IN(0)}$	Logical "0" Input Current		$V_{IN} = 0V$	−0.005	**−2.5**	μA (Max)
$V_{OUT(1)}$	Logical "1" Output Voltage		$V^+ = 4.5V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.25**	 V (Min) V (Min)
$V_{OUT(0)}$	Logical "0" Output Voltage		$V^+ = 4.5V$ $I_{OUT} = 1.6$ mA		**0.4**	V (Max)
I_{OUT}	TRI-STATE® Output Current		$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3** **3**	μA (Max) μA (Max)
$+I_{SC}$	Output Short Circuit Source Current		$V_{OUT} = 0V$	−40	**−10**	mA (Min)
$-I_{SC}$	Output Short Circuit Sink Current		$V_{OUT} = DV^+$	30	**10**	mA (Min)
DI+	Digital Supply Current		$\overline{CS}$ = HIGH	0.75	**2**	mA (Max)
			$\overline{CS}$ = HIGH, $f_{CLK} = 0$ Hz	0.15		mA (Max)
AI+	Analog Supply Current		$\overline{CS}$ = HIGH	3	**4.5**	mA (Max)
			$\overline{CS}$ = HIGH, $f_{CLK} = 0$ Hz	3		mA (Max)
I−	Negative Supply Current		$\overline{CS}$ = HIGH	3.5	**4.5**	mA (Max)
			$\overline{CS}$ = HIGH, $f_{CLK} = 0$ Hz	3.5		mA (Max)
I_{REF}	Reference Input Current		$V_{REF}^+ = 5V$	0.7	**1.1**	mA (Max)

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}+ = 5.000\ V_{DC}$, $V_{REF}- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, $t_r = t_f = 3$ ns and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 16) (Continued)

Symbol	Parameter		Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
AC CHARACTERISTICS						
f_{CLK}	Clock Frequency			8 10	**5.0**	MHz (Max) kHz (Min)
	Clock Duty Cycle				**20** **80**	% (Min) % (Max)
t_C	Conversion Time	8-Bit Unipolar Mode			**16**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**3.2**	μs (Max)
		8-Bit Bipolar Mode			**18**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**3.6**	μs (Max)
		10-Bit Unipolar Mode			**20**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**4.0**	μs (Max)
		10-Bit Bipolar Mode			**22**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**4.4**	μs (Max)
t_A	Acquisition Time				**6**	$1/f_{CLK}$
			$f_{CLK} = 5.0$ MHz		**1.2**	μs
t_{CR}	Delay between Falling Edge of $\overline{CS}$ and Falling Edge of $\overline{RD}$			0	**5**	ns (Min)
t_{RC}	Delay betwee Rising Edge $\overline{RD}$ and Rising Edge of $\overline{CS}$			0	**5**	ns (Min)
t_{CW}	Delay between Falling Edge of $\overline{CS}$ and Falling Edge of $\overline{WR}$			0	**5**	ns (Min)
t_{WC}	Delay between Rising Edge of $\overline{WR}$ and Rising Edge of $\overline{CS}$			0	**5**	ns (Min)
t_{RW}	Delay between Falling Edge of $\overline{RD}$ and Falling Edge of $\overline{WR}$			0	**5**	ns (Min)
$t_{W(\overline{WR})}$	$\overline{WR}$ Pulse Width			25	**50**	ns (Min)
t_{WS}	$\overline{WR}$ High to CLK ÷ 2 Low Set-Up Time				**5**	ns (Max)
t_{DS}	Data Set-Up Time			6	**15**	ns (Max)
t_{DH}	Data Hold Time			0	**5**	ns (Max)
$t_{\overline{WR}}$	Delay from Rising Edge of $\overline{WR}$ to Rising Edge $\overline{RD}$			0	**5**	ns (Min)
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)		$C_L = 100$ pF	25	**45**	ns (Max)
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of INT		$C_L = 100$ pF	25	**40**	ns (Max)
$t_{\overline{INTL}}$	Delay from Falling Edge of CLK ÷ 2 to Falling Edge of $\overline{INT}$			40		ns

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}+ = 5.000\ V_{DC}$, $V_{REF}- = GND$, $V^- = GND$ for unipolar operation or $V^- = -5.0\ V_{DC}$ for bipolar operation, $t_r = t_f = 3$ ns and $f_{CLK} = 5.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 16) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
AC CHARACTERISTICS (Continued)					
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L = 10$ pF, $R_L = 1$ kΩ	20	**35**	ns (Max)
t_{RR}	Delay between Successive $\overline{RD}$ Pulses		25	**50**	ns (Min)
t_P	Delay between Last Rising Edge of $\overline{RD}$ and the Next Falling Edge of $\overline{WR}$		20	**50**	ns (Min)
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

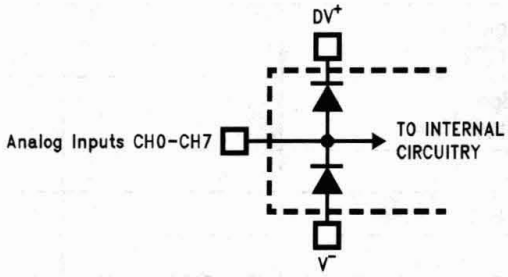
Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > AV^+$ or DV^+), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: ADC10154 with BIN and CIN suffixes 65°C/W, ADC10154 with BIJ, CIJ and CMJ suffixes 49°C/W, ADC10154 with BIWM and CIWM suffixes 72°C/W, ADC10158 with BIN and CIN suffixes 59°C/W, ADC10158 with BIJ, CIJ, and CMJ suffixes 46°C/W, ADC10158 with BIWM and CIWM suffixes 68°C/W.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post-1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 8: Two on-chip diodes are tied to each analog input as shown below. They will forward-conduct for analog input voltages one diode drop below V^- supply or



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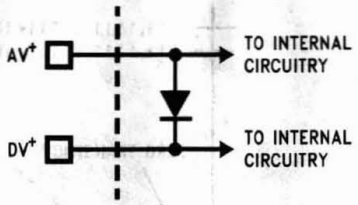
one diode drop greater than V^+ supply. Be careful during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. This means that if AV^+ and DV^+ are minimum (4.5 V_{DC}) and V^- is a maximum ($-4.5\ V_{DC}$) full scale must be $\leq \pm 4.55\ V_{DC}$.

Electrical Characteristics (Continued)

Note 9: A diode exists between AV^+ and DV^+ as shown below.



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To guarantee accuracy, it is required that the AV^+ and DV^+ be connected together to a power supply with separate bypass filter at each V^+ pin.

Note 10: Typicals are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: One LSB is referenced to 10 bits of resolution.

Note 13: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 14: For DC Common Mode Error the only specification that is measured is offset error.

Note 15: Channel leakage current is measured after the channel selection.

Note 16: All the timing specifications are tested at the TTL logic levels, $V_{IL} = 0.8V$ for a falling edge and $V_{IH} = 2.0V$ for a rising.

Ordering Information

Industrial $-40°C \leq T_A \leq 85°C$	Package
ADC10154CIN	N24A
ADC10154CIWM	M24B
ADC10158CIN	N28B
ADC10158CIWM	M28B

Electrical Characteristics (Continued)

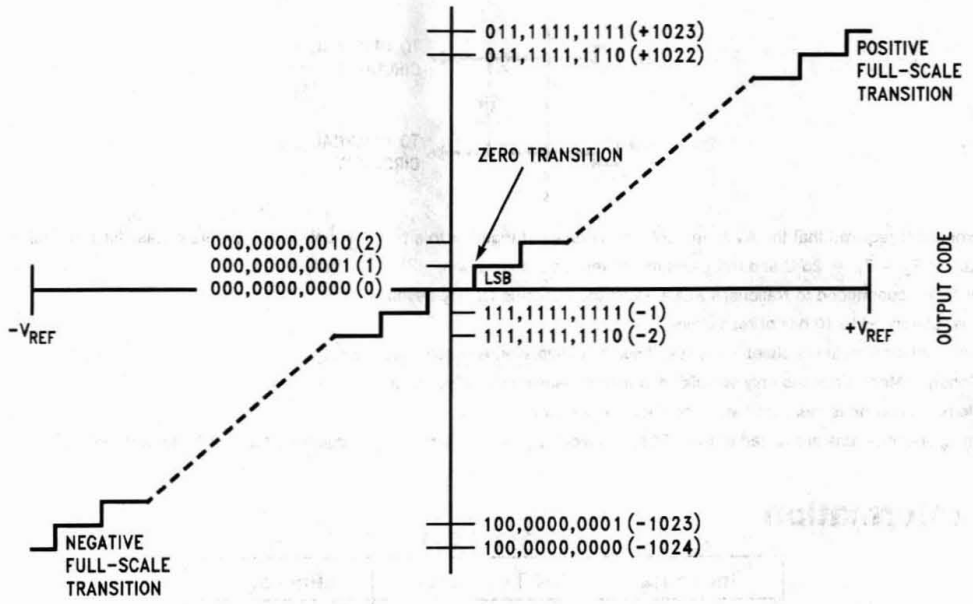

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FIGURE 1A. Transfer Characteristic

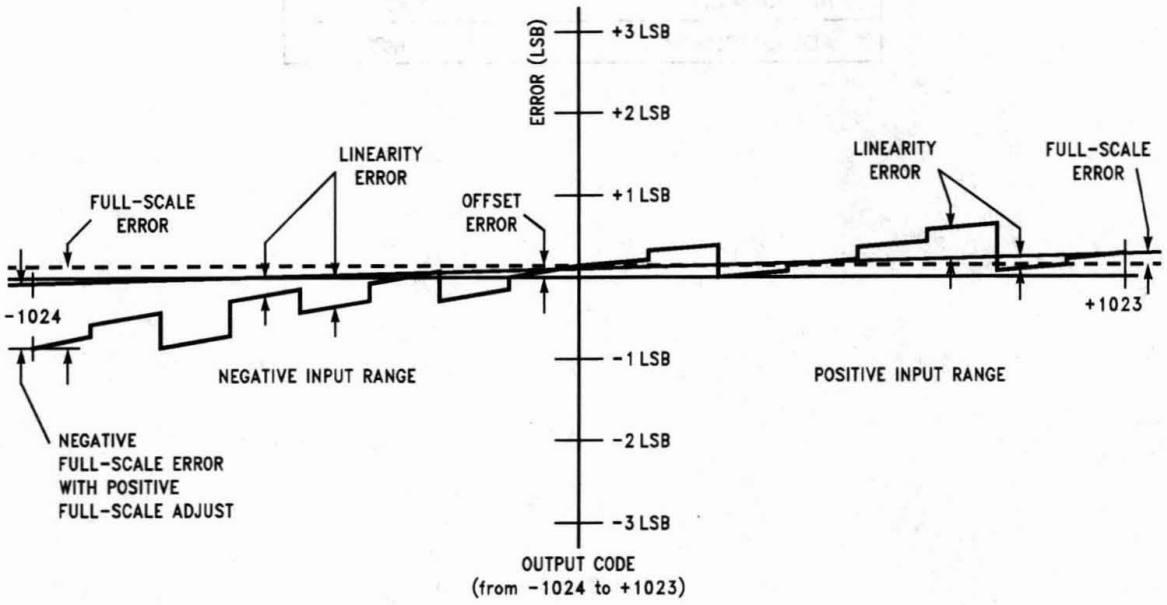

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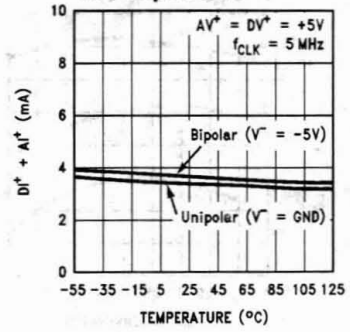
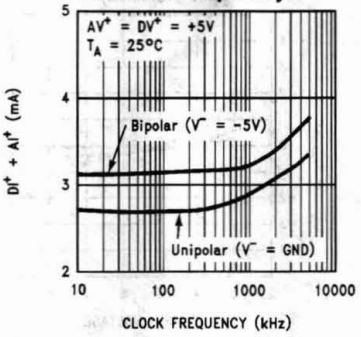
FIGURE 1B. Simplified Error Curve vs Output Code

Typical Converter Performance Characteristics

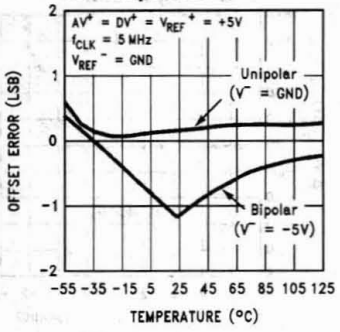
Total Positive Supply Current ($DI^+ + AI^+$) vs Temperature



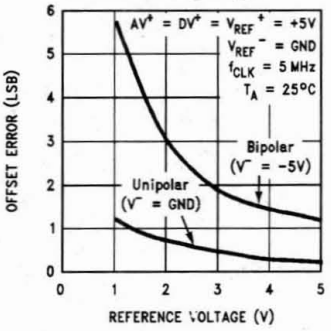
Total Positive Power Supply Current ($DI^+ + AI^+$) vs Clock Frequency



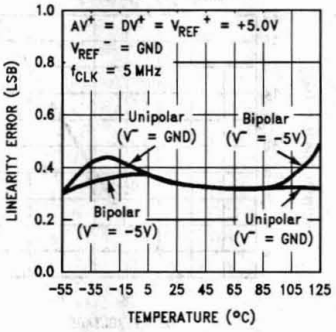
Offset Error vs Temperature



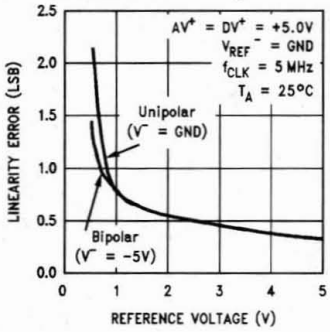
Offset Error vs Reference Voltage



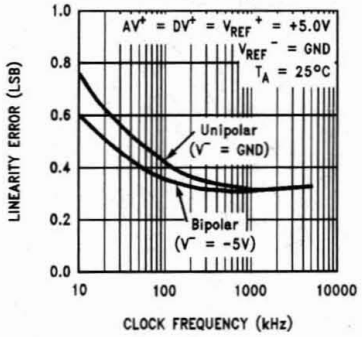
Linearity Error vs Temperature



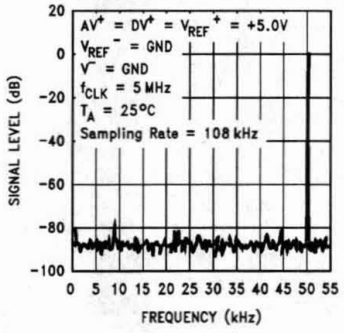
Linearity Error vs Reference Voltage



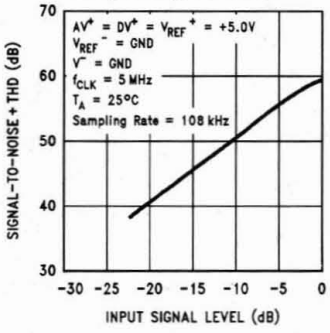
Linearity Error vs Clock Frequency



Spectral Response with 50 kHz Sine Wave



10-Bit Unsigned Signal-to-Noise + THD Ratio vs Input Signal Level



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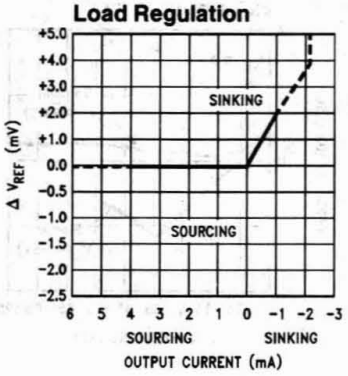
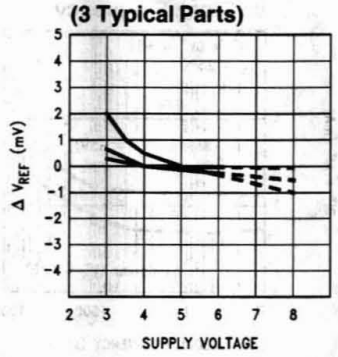
2

Typical Reference Performance Characteristics

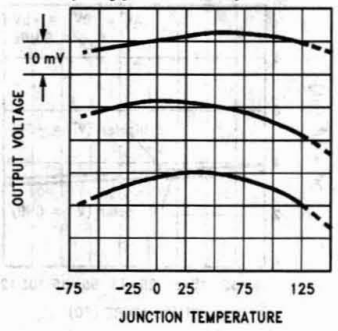
Load Regulation



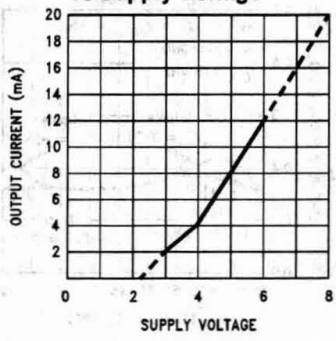
Line Regulation (3 Typical Parts)



Output Drift vs Temperature (3 Typical Parts)



Available Output Current vs Supply Voltage



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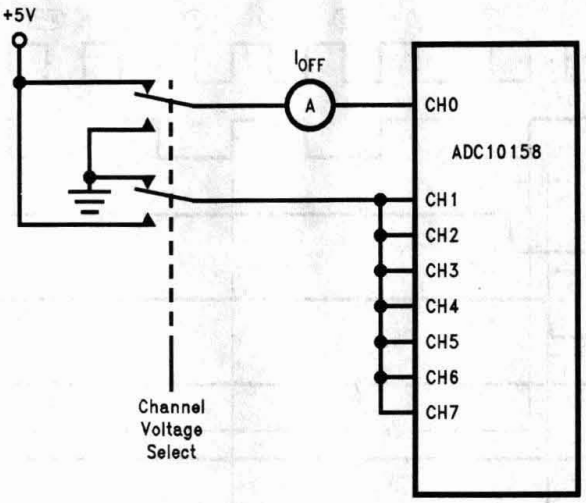
Leakage Current Test Circuit



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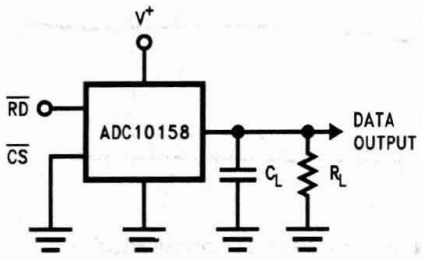
TRI-STATE Test Circuits and Waveforms



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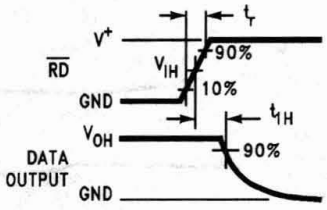

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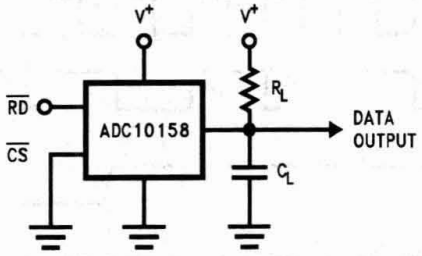

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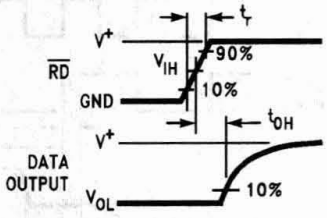

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2

Timing Diagrams

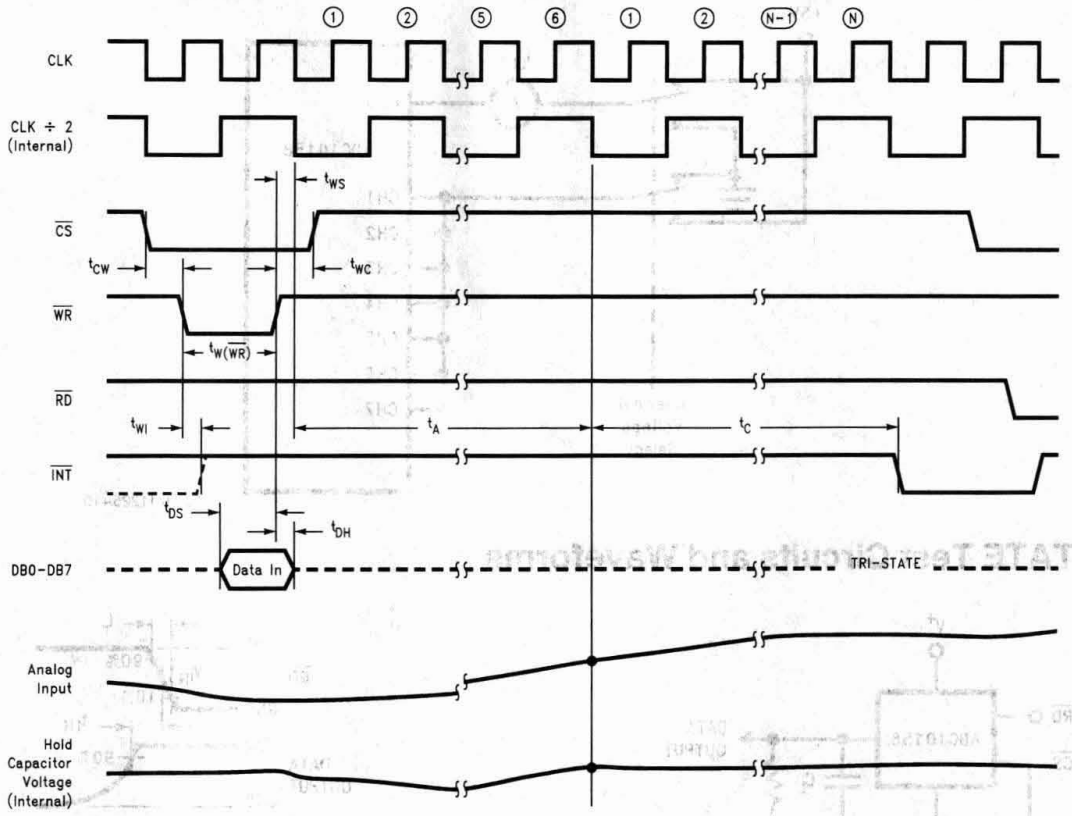

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DIAGRAM 1. Starting a Conversion with New MUX Channel and Output Configuration

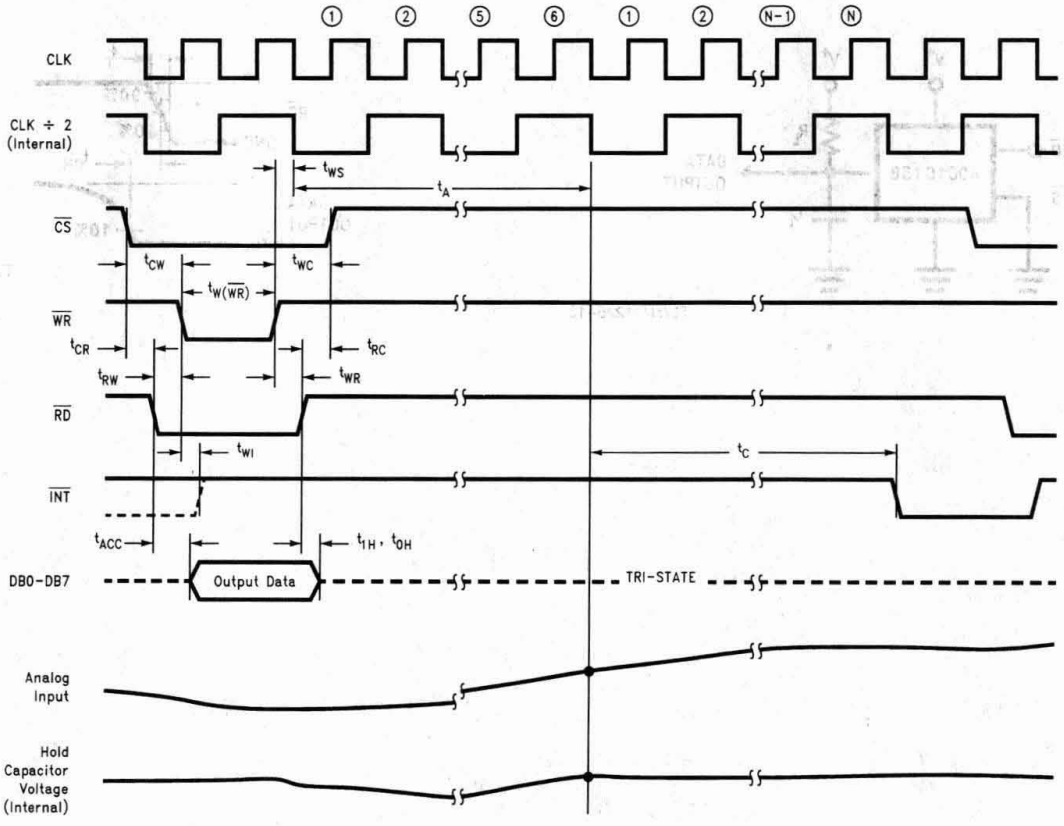

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DIAGRAM 2. Starting a Conversion without Changing the MUX Channel or Output Configuration

Timing Diagrams (Continued)

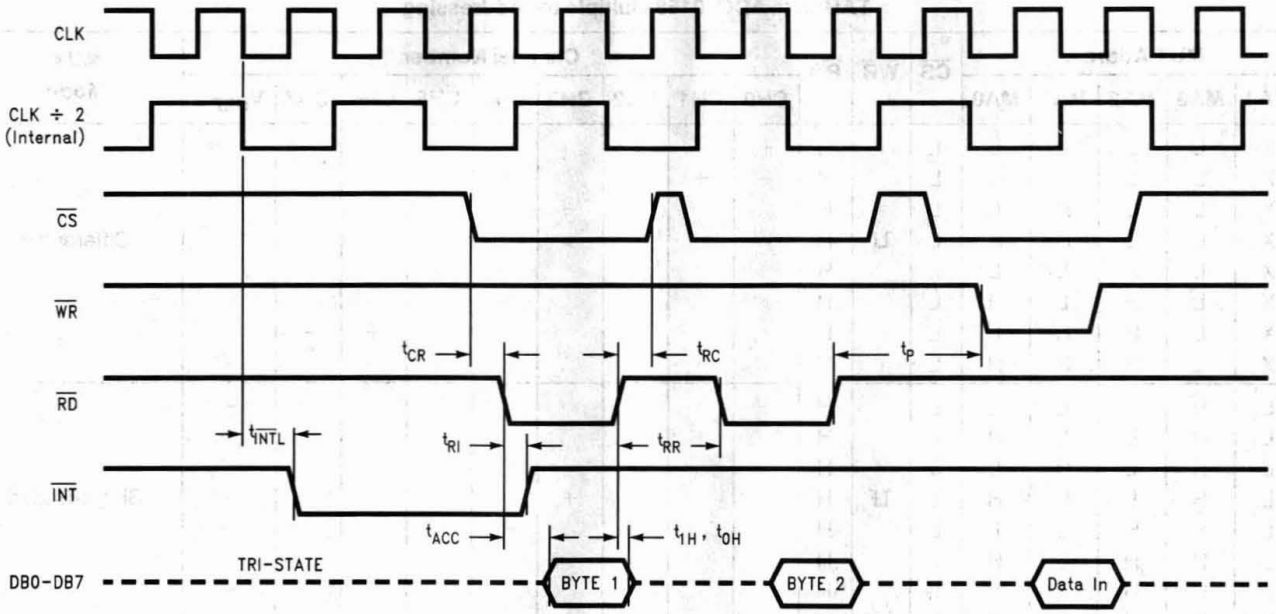

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DIAGRAM 3. Reading the Conversion Result

Multiplexer Addressing and Output Data Configuration Tables

TABLE I. ADC10154 and ADC10158 Output Data Configuration

Resolution	Output Data Format	Control Input Data			Data Bus Output Assignment								
		8/$\overline{10}$	U/$\overline{S}$	L/$\overline{R}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
10-Bits + Sign	Right-Justified	L	L	L	Sign 8	Sign 7	Sign 6	Sign 5	Sign 4	Sign 3	MSB 2	9 LSB	First Byte Read Second Byte Read
10-Bits + Sign	Left-Justified	L	L	H	Sign 3	MSB 2	9 LSB	8 L	7 L	6 L	5 L	4 L	First Byte Read Second Byte Read
10-Bits	Right-Justified	L	H	L	L 8	L 7	L 6	L 5	L 4	L 3	MSB 2	9 LSB	First Byte Read Second Byte Read
10-Bits	Left-Justified	L	H	H	MSB 2	9 LSB	8 L	7 L	6 L	5 L	4 L	3 L	First Byte Read Second Byte Read
8-Bits + Sign	Right-Justified	H	L	L	Sign MSB	Sign 7	Sign 6	Sign 5	Sign 4	Sign 3	Sign 2	Sign LSB	First Byte Read Second Byte Read
8-Bits + Sign	Left-Justified	H	L	H	Sign LSB	MSB L	7 L	6 L	5 L	4 L	3 L	2 L	First Byte Read Second Byte Read
8-Bits	Right-Justified	H	H	L	L MSB	L 7	L 6	L 5	L 4	L 3	L 2	L LSB	First Byte Read Second Byte Read
8-Bits	Left-Justified	H	H	H	MSB L	7 L	6 L	5 L	4 L	3 L	2 L	LSB L	First Byte Read Second Byte Read

Multiplexer Addressing and Output Data Configuration Tables (Continued)

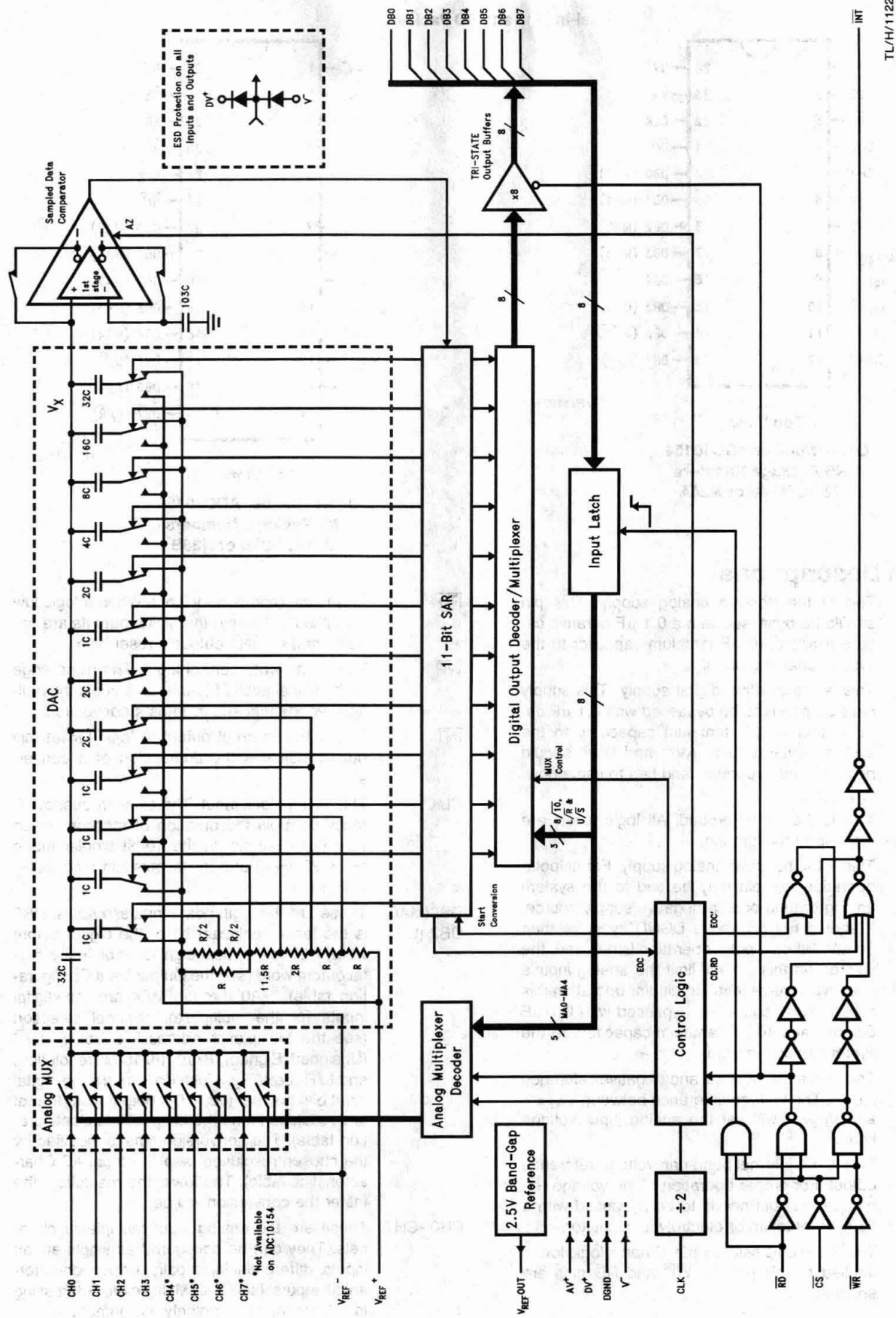
TABLE II. ADC10158 Multiplexer Addressing

MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel Number								MUX Mode
MA4	MA3	MA2	MA1	MA0				CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	V_{REF}^-	
X	L	L	L	L	L		H	+	−								Differential
X	L	L	L	H	L		H	−	+								
X	L	L	H	L	L		H			+	−						
X	L	L	H	H	L	⊓	H			−	+						
X	L	H	L	L	L		H					+	−				
X	L	H	L	H	L		H					−	+				
X	L	H	H	L	L		H							+	−		
X	L	H	H	H	L		H							−	+		
L	H	L	L	L	L		H	+								−	Single-Ended
L	H	L	L	H	L		H		+							−	
L	H	L	H	L	L		H			+						−	
L	H	L	H	H	L	⊓	H				+					−	
L	H	H	L	L	L		H					+				−	
L	H	H	L	H	L		H						+			−	
L	H	H	H	L	L		H							+		−	
L	H	H	H	H	L		H								+	−	
H	H	L	L	L	L		H	+							−		Pseudo-Differential
H	H	L	L	H	L		H		+						−		
H	H	L	H	L	L		H			+					−		
H	H	L	H	H	L	⊓	H				+				−		
H	H	H	L	L	L		H					+			−		
H	H	H	L	H	L		H						+		−		
H	H	H	H	L	L		H							+	−		
X	X	X	X	X	L	⊓	L	Previous Channel Configuration									

TABLE III. ADC10154 Multiplexer Addressing

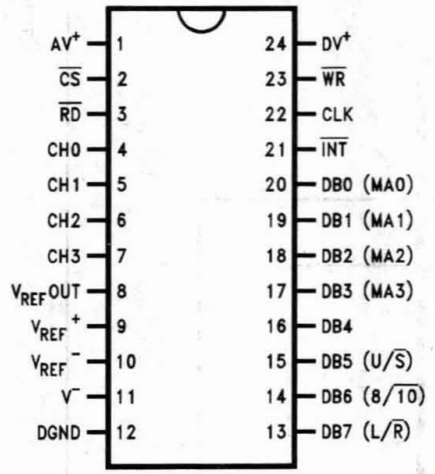
MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel Number					MUX Mode
MA4	MA3	MA2	MA1	MA0				CH0	CH1	CH2	CH3	V_{REF}^-	
X	X	L	L	L	L		H	+	−				Differential
X	X	L	L	H	L		H	−	+				
X	X	L	H	L	L	⊓	H			+	−		
X	X	L	H	H	L		H			−	+		
X	L	H	L	L	L		H	+				−	Single-Ended
X	L	H	L	H	L		H		+			−	
X	L	H	H	L	L	⊓	H			+		−	
X	L	H	H	H	L		H				+	−	
X	H	H	L	L	L		H	+			−		Pseudo-Differential
X	H	H	L	H	L	⊓	H		+		−		
X	H	H	H	L	L		H			+	−		
X	X	X	X	X	L	⊓	L	Previous Channel Configuration					

Detailed Block Diagram



Connection Diagrams

Dual-In Line and SO Packages



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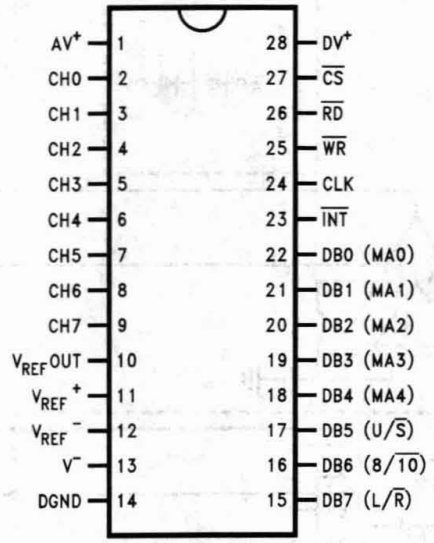
Top View

Order Number ADC10154
NS Package Numbers
J24A, M24B or N24A



TL/H/11225–3

Top View

Order Number ADC10158
NS Package Numbers
J28A, M28B or N28B

1.0 Pin Descriptions

AV^+ This is the positive analog supply. This pin should be bypassed with a 0.1 μF ceramic capacitor and a 10 μF tantalum capacitor to the system analog ground.

DV^+ This is the positive digital supply. This supply pin also needs to be bypassed with 0.1 μF ceramic and 10 μF tantalum capacitors to the system digital ground. AV^+ and DV^+ should be bypassed separately and tied to same power supply.

DGND This is the digital ground. All logic levels are referred to this ground.

V^- This is the negative analog supply. For unipolar operation this pin may be tied to the system analog ground or to a negative supply source. It should not go above DGND by more than 50 mV. When bipolar operation is required, the voltage on this pin will limit the analog input's negative voltage level. In bipolar operation this supply pin needs to be bypassed with 0.1 μF ceramic and 10 μF tantalum capacitors to the system analog ground.

V_{REF}^+, V_{REF}^- These are the positive and negative reference inputs. The voltage difference between V_{REF}^+ and V_{REF}^- will set the analog input voltage span.

V_{REF}Out This is the internal band-gap voltage reference output. For proper operation of the voltage reference, this pin needs to be bypassed with a 330 μF tantalum or electrolytic capacitor.

$\overline{CS}$ This is the chip select input. When a logic low is applied to this pin the $\overline{WR}$ and $\overline{RD}$ pins are enabled.

$\overline{RD}$ This is the read control input. When a logic low is applied to this pin the digital outputs are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ This is the write control input. The rising edge of the signal applied to this pin selects the multiplexer channel and initiates a conversion.

$\overline{INT}$ This is the interrupt output. A logic low at this output indicates the completion of a conversion.

CLK This is the clock input. The clock frequency directly controls the duration of the conversion time (for example, in the 10-bit bipolar mode $t_C = 22/f_{CLK}$) and the acquisition time ($t_A = 6/f_{CLK}$).

DB0(MA0)–DB7 (L/$\overline{R}$) These are the digital data inputs/outputs. DB0 is the least significant bit of the digital output word; DB7 is the most significant bit in the digital output word (see the Output Data Configuration table). MA0 through MA4 are the digital inputs for the multiplexer channel selection (see the Multiplexer Addressing tables). U/$\overline{S}$ (Unsigned/Signed), 8/$\overline{10}$, (8/10-bit resolution) and L/$\overline{R}$ (Left/Right justification) are the digital input bits that set the A/D's output word format and resolution (see the Output Data Configuration table). The conversion time is modified by the chosen resolution (see Electrical AC Characteristics table). The lower the resolution, the faster the conversion will be.

CH0–CH7 These are the analog input multiplexer channels. They can be configured as single-ended inputs, differential input pairs, or pseudo-differential inputs (see the Multiplexer Addressing tables for the input polarity assignments).

2.0 Functional Description

The ADC10154 and ADC10158 use successive approximation to digitize an analog input voltage. Additional logic has been incorporated in the devices to allow for the programmability of the resolution, conversion time and digital output format. A capacitive array and a resistive ladder structure are used in the DAC portion of the A/D converters. The structure of the DAC allows a very simple switching scheme to provide a very versatile analog input multiplexer. Also, inherent in this structure is a sample/hold. A 2.5V CMOS band-gap reference is also provided on the ADC10154 and ADC10158.

2.1 DIGITAL INTERFACE

The ADC10154 and ADC10158 have eight digital outputs (DB0–DB8) and can be easily interfaced to an 8-bit data bus. Taking $\overline{CS}$ and $\overline{WR}$ low simultaneously will strobe the data word on the data-bus into the input latch. This word will be decoded to determine the multiplexer channel selection, the A/D conversion resolution and the output data format. The following table shows the input word data-bit assignment.

DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
MA0	MA1	MA2	MA3	MA4	U/$\overline{S}$	8/$\overline{10}$	L/$\overline{R}$
MUX Address					Control Input Data		

DB0 through DB4 are assigned to the multiplexer address data bits zero through four (MA0–MA4). Tables II and III describe the multiplexer address assignment. DB5 selects unsigned or signed (U/$\overline{S}$) operation. DB6 selects 8- or 10-bit resolution. DB7 selects left or right justification of the output data. Refer to Table I for the effect the Control Input Data has on the digital output word.

The conversion process is started by the rising edge of $\overline{WR}$, which sets the "start conversion" bit inside the ADC. If this bit is set, the converter will start acquiring the input voltage on the next falling edge of the internal CLK÷2 signal. The acquisition period is 3 CLK÷2 periods, or 6 CLK periods. Immediately after the acquisition period the input signal is held and the actual conversion begins. The number of clocks required for a conversion is given in the following table:

Conversion Type	CLK÷2 Cycles	CLK Cycles (N)
8-Bit	8	16
8-Bit + Sign	9	18
10-Bit	10	20
10-Bit + Sign	11	22

Since the CLK÷2 signal is internal to the ADC, it is initially impossible to know which falling edge of CLK corresponds to the falling edge of CLK÷2. For the first conversion, the rising edge of $\overline{WR}$ should occur at least t_{WS} ns before any falling edge of CLK. If this edge happens to be on the rising edge of CLK÷2, this will add 2 CLK cycles to the total conversion time. The phase of the CLK÷2 signal can be determined at the end of the first conversion, when $\overline{INT}$ goes low. $\overline{INT}$ always goes low on the falling edge of the CLK÷2 signal. From the first falling edge of $\overline{INT}$ onward, every other falling edge of CLK will correspond to the falling edge of CLK÷2. With the phase of CLK÷2 now known, the conversion time can be minimized by taking $\overline{WR}$ high at least t_{WS} ns before the falling edge of CLK÷2.

Upon completion of the conversion, $\overline{INT}$ goes low to signal the A/D conversion result is ready to be read. Taking $\overline{CS}$ and $\overline{RD}$ low will enable the digital output buffer and put byte 1 of the conversion result on DB0 through DB7. The falling edge of $\overline{RD}$ resets the $\overline{INT}$ output high. Taking $\overline{CS}$ and $\overline{RD}$ low a second time will put byte 2 of the conversion result on DB7–DB0. Table I defines the DB0–DB7 assignement for different Control Input Data. The second read does not have to be completed before a new conversion is started.

Taking $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ low simultaneously will start a conversion without changing the multiplexer channel assignment or output configuration and resolution. The timing diagram in *Figure 2* shows the sequence of events that implement this function. Refer to Diagrams 1, 2, and 3 in the Timing Diagrams section for the timing constraints that must be met.

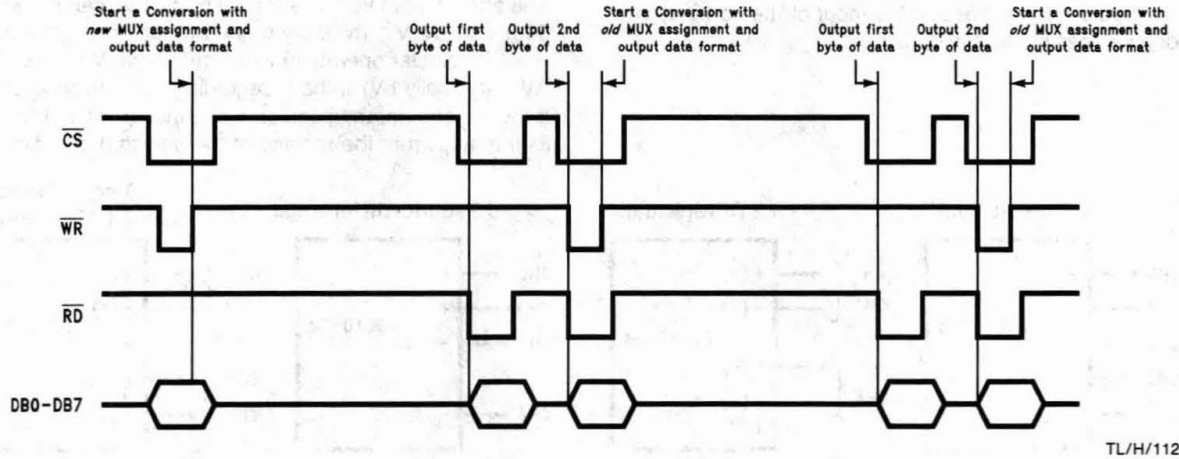

Start a Conversion with new MUX assignment and output data format
Output first byte of data
Output 2nd byte of data
Start a Conversion with old MUX assignment and output data format
Output first byte of data
Output 2nd byte of data
Start a Conversion with old MUX assignment and output data format
CS
WR
RD
DB0-DB7

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FIGURE 2. Starting a Conversion without Updating the Channel Configuration, Resolution, or Data Format

2.0 Functional Description (Continued)

Digital Interface Hints:

- Reads and writes can be completely asynchronous to CLK.
- In addition to the timing indicated in Diagrams 1–3, $\overline{CS}$ can be tied low permanently or taken low for entire conversions, eliminating all the $\overline{CS}$ guardbands (t_{CR}, t_{RC}, t_{CW}, t_{WC}).
- If $\overline{CS}$ is used as shown in Diagrams 1–3, the $\overline{CS}$ guardbands (t_{CR}, t_{RC}, t_{CW}, t_{WC}) between $\overline{CS}$ and the $\overline{RD}$ and $\overline{WR}$ signals can safely be ignored as long as the following two conditions are met:
  1) When initiating a write, $\overline{CS}$ and $\overline{WR}$ must be simultaneously low for at least $t_{W(\overline{WR})}$ ns (see Diagram 1). The "start" conversion" bit will be set on the rising edge of $\overline{WR}$ or $\overline{CS}$, whichever is first.
  2) When reading data, understand that data will not be valid until t_{ACC} ns after *both* $\overline{CS}$ and $\overline{RD}$ go low. The output data will enter TRI-STATE t_{1H} ns or t_{0H} ns after *either* $\overline{CS}$ or $\overline{RD}$ goes high (see Diagrams 2 and 3).

2.2 ARCHITECTURE

Before a conversion is started, during the analog input sampling period, the sampled data comparator is zeroed. As the comparator is being zeroed the channel assigned to be the positive input is connected to the A/D's input capacitor. (See the Digital Interface section for a description of the assignment procedure.) This charges the input 32C capacitor of the DAC to the positive analog input voltage. The switches shown in the DAC portion of the detailed block diagram are set for this zeroing/acquisition period. The voltage at the input and output of the comparator are at equilibrium at this point in time. When the conversion is started the comparator feedback switches are opened and the 32C input capacitor is then switched to the assigned negative input voltage. When the comparator feedback switch opens a fixed amount of charge is trapped on the common plates of the capacitors. The voltage at the input of the comparator moves away from equilibrium when the 32C capacitor is switched to the assigned negative input voltage, causing the output of the comparator to go high ("1") or low ("0"). The SAR next goes through an algorithm, controlled by the output state of the comparator, that redistributes the charge on the capacitor array by switching the voltage on one side of the capacitors in the array. The objective of the SAR algorithm is to return the voltage at the input of the comparator as close as possible to equilibrium.

The switch position information at the completion of the successive approximation routine is a direct representation of the digital output. This information is then manipulated by the Digital Output decoder to the programmed format. The reformatted data is then available to be strobed onto the data bus (DB0–DB7) via the digital output buffers by taking $\overline{CS}$ and $\overline{RD}$ low.

3.0 Applications Information

3.1 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by the successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal or pair of input terminals being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code when configured for unsigned operation. When configured for signed operation the A/D responds with the appropriate output digital code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-ended, or pseudo-differential. *Figure 3* shows the three modes using the 4-channel MUX of the ADC10154. The eight inputs of the ADC10158 can also be configured in any of the three modes. The single-ended mode has CH0–CH3 assigned as the positive input with the negative input being the V_{REF}^- of the device. In the differential mode, the ADC10154 channel inputs are grouped in pairs, CH0 with CH1 and CH2 with CH3. The polarity assignment of each channel in the pair is interchangeable. Finally, in the pseudo-differential mode CH0–CH2 are positive inputs referred to CH3 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground-referred inputs and true differential inputs as well as signals referred to a specific voltage.

The analog input voltages for each channel can range from 50 mV below V^- (typically ground for unipolar operation or −5V for bipolar operation) to 50 mV above $V^+ = DV^+ = AV^+$ (typically 5V) without degrading conversion accuracy. If the voltage on an unselected channel exceeds these limits it may corrupt the reading of the selected channel.

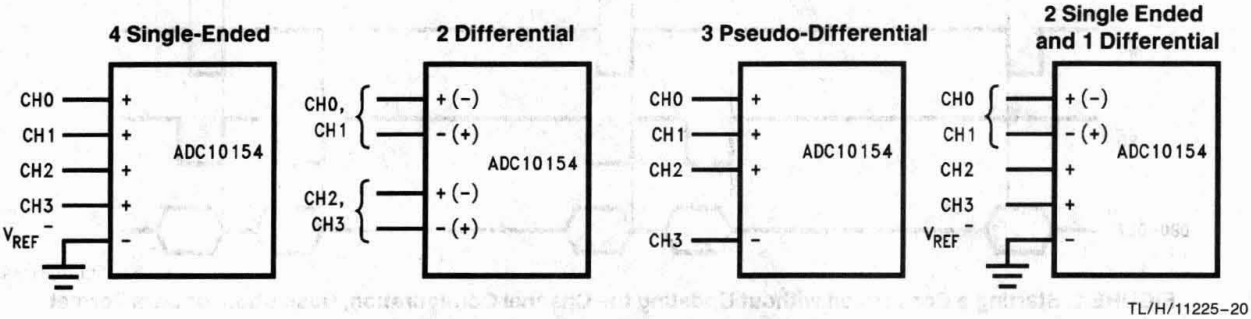

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FIGURE 3. Analog Input Multiplexer Options

3.0 Applications Information (Continued)

3.2 REFERENCE CONSIDERATIONS

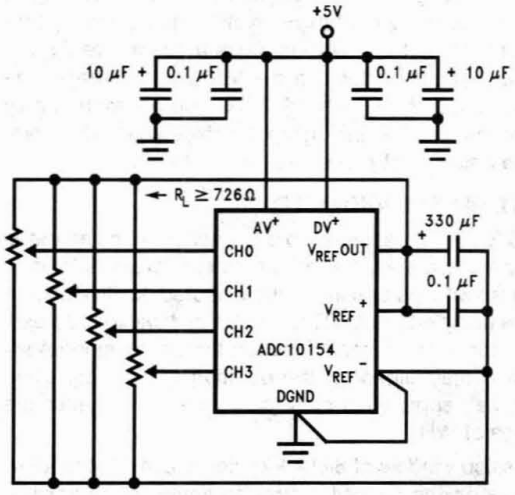
The voltage difference between the V_{REF}^+ and V_{REF}^- inputs defines the analog input voltage span (the difference between V_{IN}(Max) and V_{IN}(Min)) over which the 2^n (where n is the programmed resolution) possible output codes apply. In the pseudo-differential and differential modes the actual voltage applied to V_{REF}^+ and V_{REF}^- can lie anywhere between the AV^+ and V^-. Only the difference voltage is of importance. When using the single-ended multiplexer mode the voltage at V_{REF}^- has a dual function. It simultaneously determines the "zero" reference voltage and, with V_{REF}^+, the analog voltage span.

The value of the voltage on the V_{REF}^+ or V_{REF}^- inputs can be anywhere between $AV^+ + 50$ mV and $V^- - 50$ mV, so long as V_{REF}^+ is greater than V_{REF}^-. The ADC10154 and ADC10158 can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the minimum reference input resistance of 4.5 kΩ.

The internal 2.5V bandgap reference in the ADC10154 and ADC10158 is available as an output on the V_{REF}Out pin. To ensure optimum performance this output needs to be bypassed to ground with 330 μF aluminum electrolytic or tantalum capacitor. The reference output is unstable with capacitive loads greater than 100 pF and less than 100 μF. Any capacitive loads ≤100 pF or ≥100 μF will not cause the reference to oscillate. Lower output noise can be obtained by increasing the output capacitance. The 330 μF capacitor will yield a typical noise floor of 200 nVrms/$\sqrt{\text{Hz}}$. The 2.5V reference output is referred to the negative supply pin (V^-). Therefore, **the voltage at V_{REF}Out will always be 2.5V greater than the voltage applied to V^-.** Applying this voltage to V_{REF}^+ with V_{REF}^- tied to V^- will yield an analog voltage span of 2.5V. In bipolar operation the voltage at V_{REF}Out will be at −2.5V when V^- is tied to −5V. For the single-ended multiplexer mode the analog input voltage range will be from −5V to −2.5V. The pseudo-differential and differential multiplexer modes allow for more flexibility in the analog input voltage range since the "zero" reference voltage is set by the actual voltage applied to the assigned negative input pin. The drawback of using the internal reference in the bipolar mode is that any noise on the −5V tied to the V^- pin will affect the conversion result. The bandgap reference is specified and tested in unipolar operation with V^- tied to the system ground.

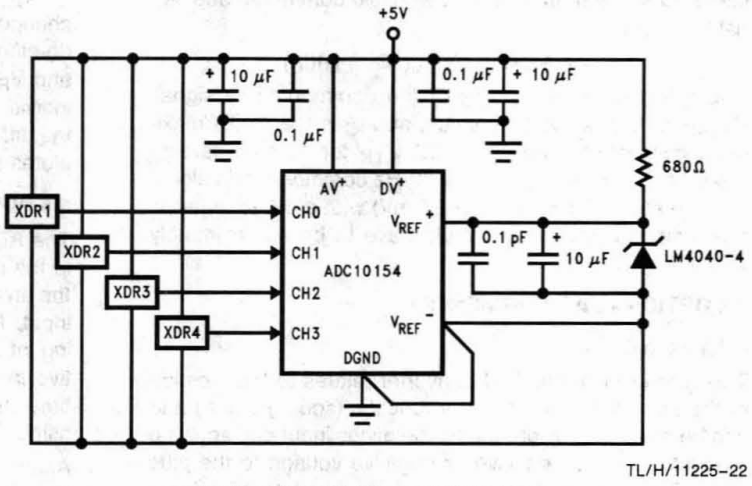
In a ratiometric system *(Figure 4a)*, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage may also be the system power supply, so V_{REF}^+ can also be tied to AV^+. This technique relaxes the stablity requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy *(Figure 4b)*, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time- and temperature-stable voltage source that has excellent initial accuracy. The LM4040 and LM185 references are suitable for use with the ADC10154 and ADC10158.



TL/H/11225-21

a. Ratiometric Using the Internal Reference



TL/H/11225-22

b. Absolute Using a 4.096V Span

FIGURE 4. Different Reference Configurations

3.0 Applications Information (Continued)

The minimum value of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) can be quite small (see Typical Performance Characteristics) to allow direct conversion of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/2^n$).

3.3 THE ANALOG INPUTS

Due to the sampling nature of the analog inputs, at the clock edges short duration spikes of current will be seen on the selected assigned negative input. Input bypass capacitors should not be used if the source resistance is greater than 1 kΩ since they will average the AC current and cause an effective DC current to flow through the analog input source resistance. An op amp RC active lowpass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required. Bypass capacitors may be used when the source impedance is very low without any degradation in performance.

In a true differential input stage, a signal that is common to both "+" and "−" inputs is cancelled. For the ADC10154 and ADC10158, the positive input of a selected channel pair is only sampled once before the start of a conversion during the acquisition time (t_A). The negative input needs to be stable during the complete conversion sequence because it is sampled before each decision in the SAR sequence. Therefore, any AC common-mode signal present on the analog inputs will not be completely cancelled and will cause some conversion errors. For a sinusoid common-mode signal this error is:

$$V_{error}(Max) = V_{PEAK}(2\pi f_{CM})(t_C)$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value, and t_C is the A/D's maximum conversion time ($t_C = 22/f_{CLK}$ for 10-bit plus sign resolution). For example, for a 60 Hz common-mode signal to generate a ¼ LSB error (1.24 mV) with a 4.5 μs conversion time, its peak value would have to be approximately 731 mV.

3.4 OPTIONAL ADJUSTMENTS

3.4.1 Zero Error

The zero error of the A/D converter relates to the location of the first riser of the transfer function (see *Figure 1*) and can be measured by grounding the minus input and applying a small magnitude positive or negative voltage to the plus input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 000 0000 0000 to 000 0000 0001 (10-bits plus sign) and the ideal ½ LSB value (½ LSB = 2.44 mV for V_{REF} = + 5.000V and 10-bit plus sign resolution).

The zero error of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN}(Min)$, is not ground, the effetive "zero" voltage can be adjusted to a convenient value. The converter can be made to output an all zeros digital code for this minimum input voltage by biasing any minus input to $V_{IN}(Min)$. This is useful for either the differential or pseudo-differential input channel configurations.

3.4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the V_{REF} voltage ($V_{REF} = V_{REF}^+ - V_{REF}^-$) for a digital output code changing from 011 1111 1110 to 011 1111 1111. In bipolar signed operation this only adjusts the positive full scale error. The negative full-scale error will be as specified in the Electrical Characteristics after a positive full-scale adjustment.

3.4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A plus input voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/2^n, n being the programmed resolution) is applied to selected plus input and the zero reference voltage at the corresponding minus input should then be adjusted to just obtain the 000_{HEX} to 001_{HEX} code transition.

The full-scale adjustment should be made [with the proper minus input voltage applied] by forcing a voltage to the plus input which is given by:

$$V_{IN}(+)\,fs\,adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{2^n}\right]$$

where V_{MAX} equals the high end of the ananlog input range, V_{MIN} equals the low end (the offset zero) of the analog range and n equals the programmed resolution. Both V_{MAX} and V_{MIN} are ground referred. The V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) voltage is then adjusted to provide a code change from $3FE_{HEX}$ to $3FF_{HEX}$. Note, when using a pseudo-differential or differential multiplexer mode where V_{REF}^+ and V_{REF}^- are placed within the V^+ and V^- range, the individual values of V_{REF}^+ and V_{REF}^- do not matter, only the difference sets the analog input voltage span. This completes the adjustment procedure.

3.5 INPUT SAMPLE-AND-HOLD

The ADC10154/8's sample/hold capacitor is implemented in the capacitor array. After the channel address is loaded, the array is switched to sample the selected positive analog input. The rising edge of $\overline{WR}$ loads the multiplexer addressing information. The sampling period for the assigned positive input is maintained for the duration of the acquisition time (t_A), i.e., approximately 6 to 8 clock cycles after the rising edge of $\overline{WR}$.

An acquisition window of 6 clock cycles is available to allow the voltage on the capacitor array to settle to the positive analog input voltage. Any change in the analog voltage on a selected positive input before or after the acquisition window will not effect the A/D conversion result.

In the simplest case, the array's acquisition time is determined by the R_{ON} (9 kΩ) of the multiplexer switches, the stray input capacitance C_{S1} (3.5 pF) and the total array (C_L) and stray (C_{S2}) capacitance ($C_L + C_{S2}$ = 48 pF). For a large source resistance the analog input can be modeled as an RC network as shown in *Figure 5*. The values shown yield an acquisition time of about 1.1 μs for 10-bit unipolar or 10-bit plus sign bipolar accuracy with a zero-to-full-scale change in the input voltage. External source resistance and capacitance will lengthen the acquisition time and should be accounted for. Slowing the clock will lengthen the acquisition time, thereby allowing a larger external source resistance.

3.0 Applications Information (Continued)

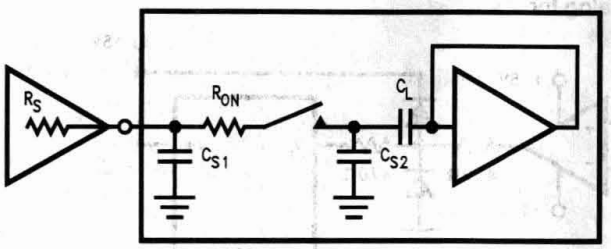


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FIGURE 5. Analog Input Model

The curve "Signal to Noise Ratio vs. Output Frequency" *(Figure 6)* gives an indication of the usable bandwidth of the ADC10154/ADC10158. The signal-to-noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the A/D. An ideal 10-bit plus sign A/D converter with a total unadjusted error of 0 LSB would have a signal-to-noise ratio of about 68 dB, which can be derived from the equation:

$$S/N = 6.02(n) + 1.8$$

where S/N is in dB and n is the number of bits. *Figure 2* shows the signal-to-noise ratio vs. input frequency of a typical ADC10154/ADC10158 with ½ LSB total unadjusted error. The dotted lines show signal-to-noise ratios for an ideal (noiseless) 10-bit A/D with 0 LSB error and an A/D with a 1 LSB error.

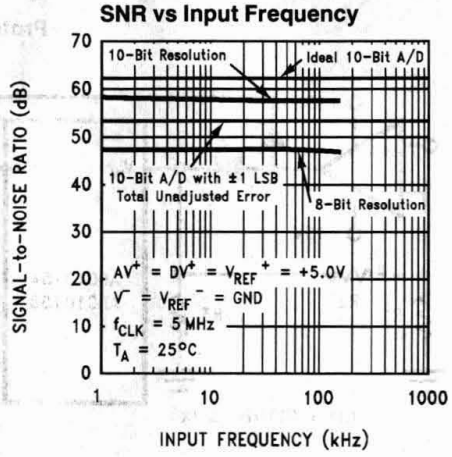

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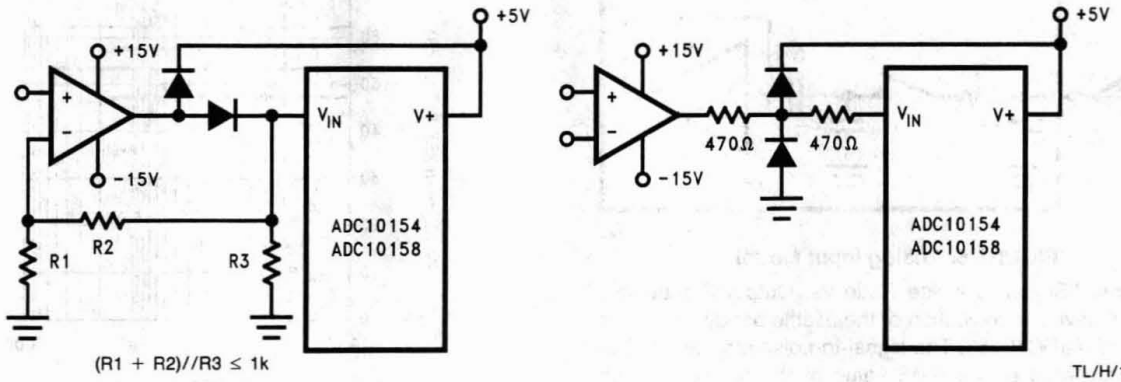
FIGURE 6. ADC10154/ADC10158
Signal-to-Noise Ratio vs Input Frequency

The sample-and-hold error specifications are included in the error and timing specifications of the A/D. The hold step and gain error sample/hold specs are included in the ADC10154/ADC10158's total unadjusted, linearity, gain and offset error specifications, while the hold settling time is included in the A/D's maximum conversion time specification. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. The data is lost after a new conversion has been completed.

3.0 Applications Information (Continued)

Protecting the Analog Inputs



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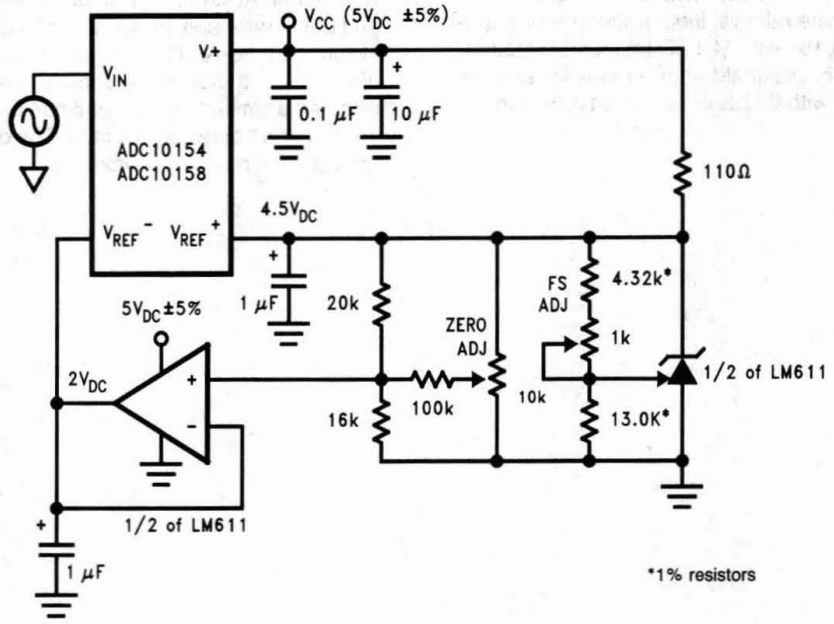
Note 1: Diodes are 1N914.

Note 2: The protection diodes should be able to withstand the output current of the op amp under current limit.

Zero-Shift and Span-Adjust for Signed or Unsigned, Unipolar, Single-Ended Multiplexer Assignment, Analog Input Range of 2V ≤ V_{IN} ≤ 4.5V



TL/H/11225–26

National Semiconductor

ADC1031/ADC1034/ADC1038 10-Bit Serial I/O A/D Converters with Analog Multiplexer and Track/Hold Function

General Description

The ADC1031, ADC1034 and ADC1038 are 10-bit successive approximation A/D converters with serial I/O. The serial input, for the ADC1034 and ADC1038, controls a single-ended analog multiplexer that selects one of 4 input channels (ADC1034) or one of 8 input channels (ADC1038). The ADC1034 and ADC1038 serial output data can be configured into a left- or right-justified format.

An input track/hold is implemented by a capacitive reference ladder and sampled-data comparator. This allows the analog input to vary during the A/D conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Applications

- Engine control
- Process control
- Instrumentation
- Test equipment

Features

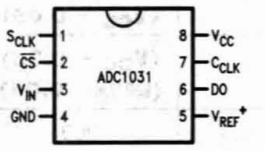
- Serial I/O (MICROWIRE™ compatible)
- Separate asynchronous converter clock and serial data I/O clock
- Analog input track/hold function
- Ratiometric or absolute voltage referencing
- No zero or full scale adjustment required
- 0V to 5V analog input range with single 5V power supply
- TTL/MOS input/output compatible
- No missing codes

Key Specifications

■ Resolution	10 bits
■ Total unadjusted error	±1 LSB (max)
■ Single supply	5V ±5%
■ Power dissipation	20 mW (max)
■ Max. conversion time (f_C = 3 MHz)	13.7 μs (max)
■ Serial data exchange time (f_S = 1 MHz)	10 μs (max)

Connection Diagrams

Dual-In-Line and SO Packages



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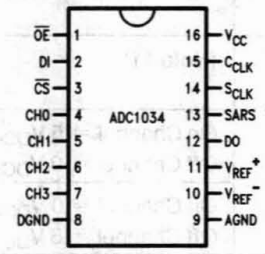
Top View

ADC1031 In NS Package N08E



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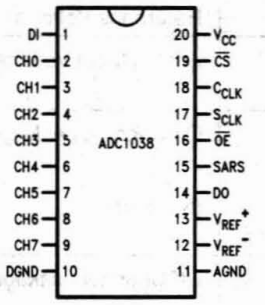
Top View

ADC1034 In NS Packages J16A, M16B or N16E



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Top View

ADC1038 In NS Packages J20A, M20B or N20A

Ordering Information

Industrial $-40°C \leq T_A \leq +85°C$	Package
ADC1031CIN	N08E
ADC1034CIN	N16E
ADC1034CIWM	M16B
ADC1038CIN	N20A
ADC1038CIWM	M20B
Military $-55°C \leq T_A \leq +125°C$	**Package**
ADC1034CMJ	J16A
ADC1038CMJ	J20A

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	$-0.3V$ to $V_{CC} + 0.3V$
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Package Dissipation at $T_A = 25°C$ (Note 5)	500 mW
ESD Susceptability (Note 6)	2000V
Soldering Information	
N Package (10 sec.)	260°C
J Package (10 sec.)	300°C
SO Package (Note 7):	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Storage Temperature	$-65°C$ to $+150°C$

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1031CIN, ADC1034CIN, ADC1034CIWM, ADC1038CIN, ADC1038CIWM	$-40°C \le T_A \le +85°C$
ADC1034CMJ, ADC1038CMJ	$-55°C \le T_A \le +125°C$
Supply Voltage (V_{CC})	4.75 V_{DC} to 5.25 V_{DC}
Reference Voltage ($V_{REF} = V_{REF}^+ - V_{REF}^-$)	2.0 V_{DC} to $V_{CC} + 0.05V$

Electrical Characteristics

The following specifications apply for $V_{CC} = +5.0V$, $V_{REF} = +4.6V$, $f_S = 700$ kHz, and $f_C = 3$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
CONVERTER AND MULTIPLEXER CHARACTERISTICS						
	Total Unadjusted Error	CIN, CIWM, CMJ	(Note 10)		±**1**	LSB (max)
	Differential Linearity				**10**	Bits (min)
R_{REF}	Reference Input Resistance			8	 **5** **11**	kΩ kΩ (min) kΩ (max)
V_{REF}	Reference Voltage				**(V_{CC} + 0.05)**	V (max)
V_{IN}	Analog Input Voltage		(Note 11)		**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
	On Channel Leakage Current		On Channel = 5 V_{DC}, Off Channel = 0 V_{DC}	5.0	200 **500**	nA (max) nA (max)
	(Note 12)		On Channel = 0 V_{DC}, Off Channel = 5 V_{DC}	5.0	−200 **−500**	nA (max) nA (max)
	Off Channel Leakage Current		On Channel = 5 V_{DC}, Off Channel = 0 V_{DC}	5.0	−200 **−500**	nA (max) nA (max)
	(Note 12)		On Channel = 0 V_{DC}, Off Channel = 5 V_{DC}	5.0	200 **500**	nA (max) nA (max)
	Power Supply Sensitivity	Zero Error	4.75 $V_{DC} \le V_{CC} \le 5.25$ V_{DC}		±**1/4**	LSB (max)
		Full Scale Error			±**1/4**	LSB (max)

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5.0V, V_{REF} = +4.6V, f_S = 700 kHz, and f_C = 3 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.25 V_{DC}		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75 V_{DC}		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.0 V_{DC}	0.005	**2.5**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0 V_{DC}	−0.005	**−2.5**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75 V_{DC} I_{OUT} = −360 μA I_{OUT} = −10 μA		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75 V_{DC} I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V	−0.01	**−3**	μA (max)
		V_{OUT} = 5V	0.01	**3**	μA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V	−14	**−6.5**	mA (min)
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}	16	**8.0**	mA (min)
I_{CC}	Supply Current	$\overline{CS}$ = HIGH, V_{REF} Open	1.5	**3**	mA (max)
AC CHARACTERISTICS					
f_C	Conversion Clock (C_{CLK}) Frequency		0.7 4.0	 **3.0**	MHz (min) MHz (max)
f_S	Serial Data Clock (S_{CLK}) Frequency (Note 13)	f_C = 3 MHz, R/$\overline{L}$ = "0"	183		kHz (min)
		f_C = 3 MHz, R/$\overline{L}$ = "1"	622		kHz (min)
		f_C = 3 MHz, R/$\overline{L}$ = "0" or R/$\overline{L}$ = "1"	2	**1.0**	MHz (max)
T_C	Conversion Time	Not Including MUX Addressing and Analog Input Sampling Times		**41 (1/f_C) + 200 ns**	(max)
t_{CA}	Analog Sampling Time	After Address is Latched, $\overline{CS}$ = Low		**4.5 (1/f_S) + 200 ns**	(max)
t_{ACC}	Access Time Delay from $\overline{CS}$ or $\overline{OE}$ Falling Edge to DO Data Valid	$\overline{OE}$ = "0"	100	**200**	ns (max)
t_{SET-UP}	Set-up Time of $\overline{CS}$ Falling Edge to S_{CLK} Rising Edge		75	**150**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{OE}$ or $\overline{CS}$ Rising Edge to DO TRI-STATE	R_L = 3 kΩ, C_L = 100 pF	100	**120**	ns (max)
t_{HDI}	DI Hold Time from S_{CLK} Rising Edge		0	**50**	ns (min)
t_{SDI}	DI Set-up Time to S_{CLK} Rising Edge		50	**100**	ns (min)

2

Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +5.0V, V_{REF} = +4.6V, f_S = 700 kHz, and f_C = 3 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions		Typical (Note 8)	Limit (Note 9)	Units (Limits)
AC CHARACTERISTICS (Continued)						
t_{HDO}	DO Hold Time from S_{CLK} Falling Edge	R_L = 30 kΩ, C_L = 100 pF		70	**10**	ns (min)
t_{DDO}	Delay from S_{CLK} Falling Edge to DO Data Valid	R_L = 30 kΩ, C_L = 100 pF		150	**250**	ns (max)
t_{RDO}	DO Rise Time	R_L = 30 kΩ, C_L = 100 pF	TRI-STATE to High	35	**75**	ns (max)
			Low to High	75	**150**	ns (max)
t_{FDO}	DO Fall Time	R_L = 30 kΩ, C_L = 100 pF	TRI-STATE to Low	35	**75**	ns (max)
			High to Low	75	**150**	ns (max)
C_{IN}	Input Capacitance	Analog Inputs (CH0–CH7)		50		pF
		All Other Inputs		7.5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < DGND, or V_{IN} > V_{CC}) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{Jmax} = 125°C. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow: ADC1031 with CIN suffixes 71°C/W, ADC1034 with CMJ suffixes 52°C/W, ADC1034 with CIN suffixes 54°C/W, ADC1034 with CIWM suffixes 70°C/W, ADC1038 with CMJ suffixes 53°C/W, ADC1038 with CIN suffixes 46°C/W, ADC1038 with CIWM suffixes 64°C/W.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or *Linear Databook* section "Surface Mount" for other methods of soldering surface mount devices.

Note 8: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 11: Two on-chip diodes are tied to each analog input. They will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

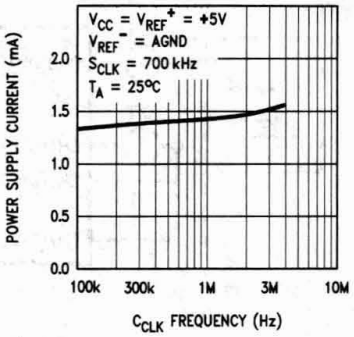
Note 12: Channel leakage current is measured after the channel selection.

Note 13: In order to synchronize the serial data exchange properly, SARS needs to go low after completion of the serial I/O data exchange. If this does not occur the output shift register will be reset and the correct output data lost. The minimum limit for S_{CLK} will depend on C_{CLK} frequency and whether right-justified or left-justified, and can be determined by the following equations:

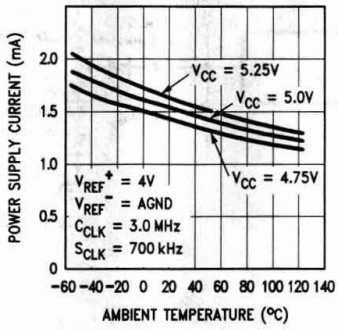
$f_S > (8.5/41)\ (f_C)$ with right-justification (R/$\overline{L}$ = "1") and $f_S > (2.5/41)\ (f_C)$ with left-justification (R/$\overline{L}$ = "0").

Typical Performance Characteristics

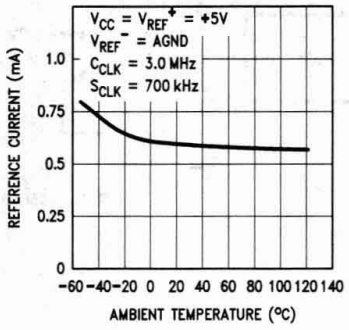
Power Supply Current (I_{CC}) vs C_{CLK}



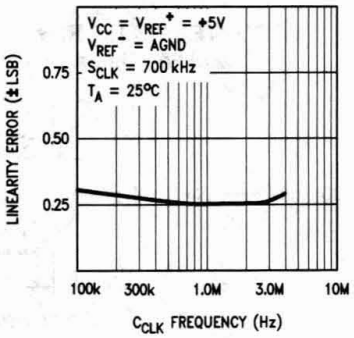
Power Supply Current (I_{CC}) vs Ambient Temperature



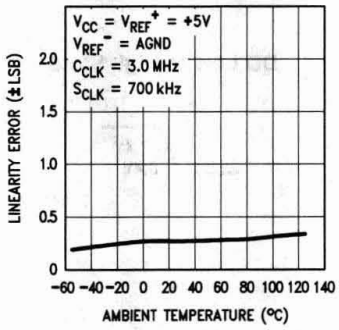
Reference Current (I_{REF}) vs Ambient Temperature



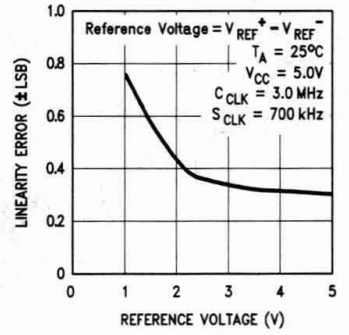
Linearity Error vs C_{CLK} Frequency



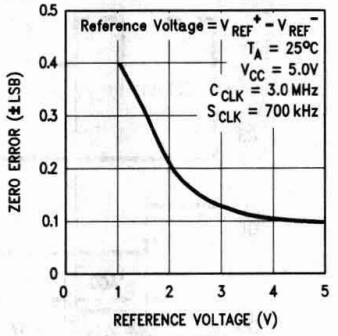
Linearity Error vs Ambient Temperature



Linearity Error vs Reference Voltage



Zero Error vs Reference Voltage



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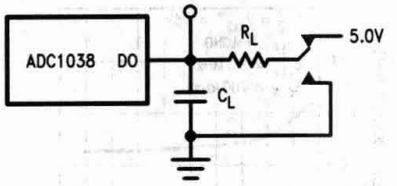
2

Test Circuits

t_{1H}, t_{0H}



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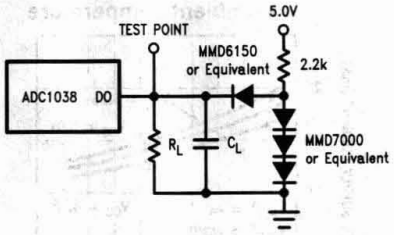
DO except "TRI-STATE"



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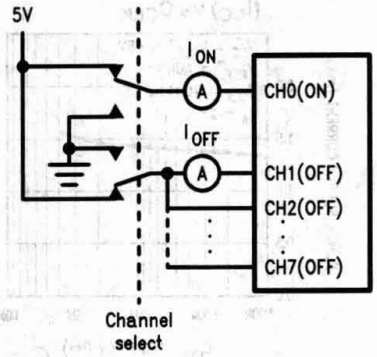
Leakage Current



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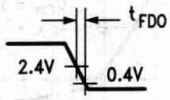
Timing Diagrams

DO High to Low State



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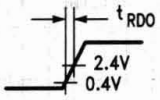
DO Low to High State



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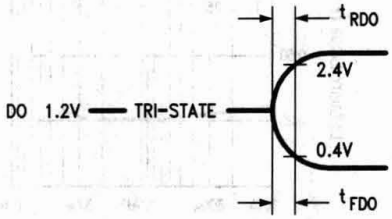
DO "TRI-STATE" Rise and Fall Times



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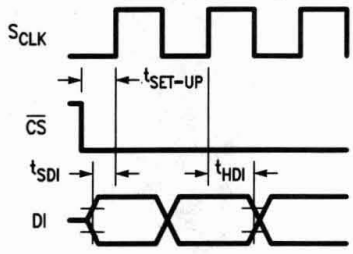
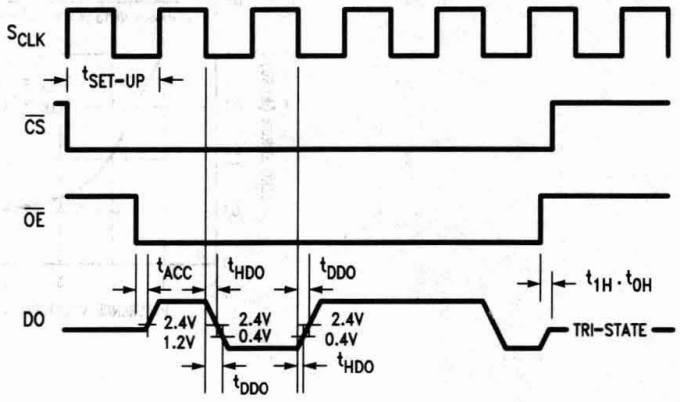
DI Data Input Timing



TL/H/10556-12

DO Data Output Timing



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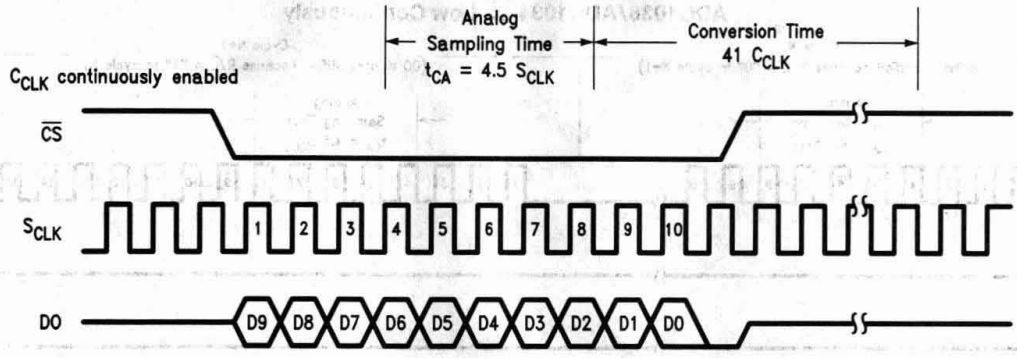
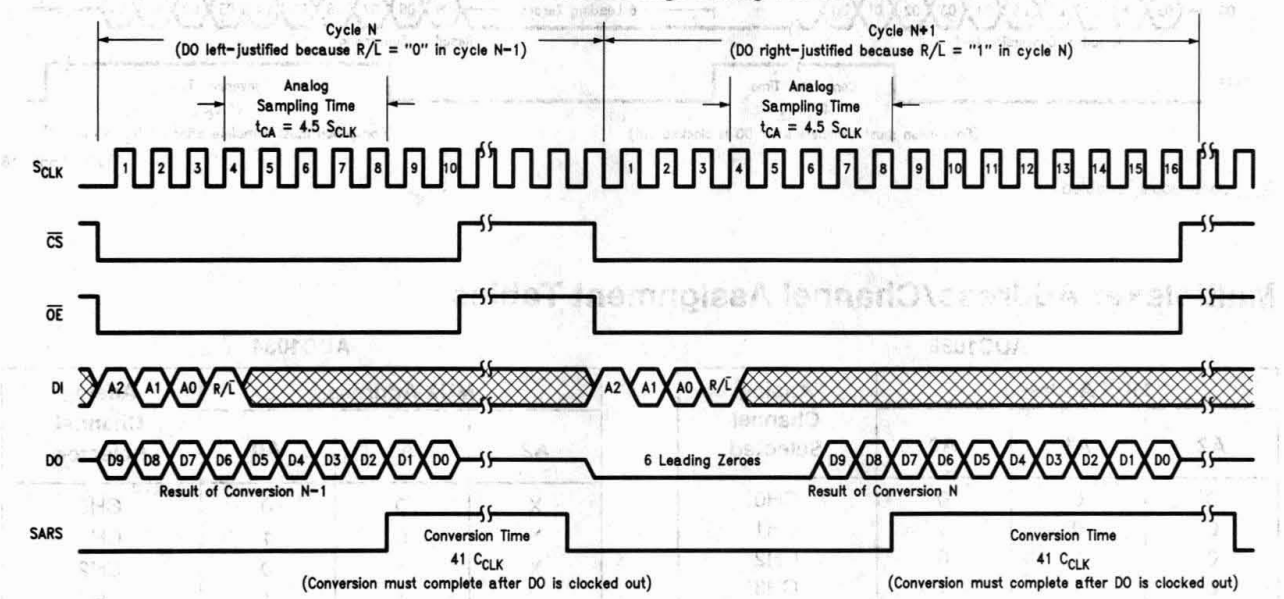
Timing Diagrams (Continued)

ADC1031 $\overline{CS}$ High during Conversion



TL/H/10556–14

ADC1038/ADC1034 $\overline{CS}$ High during Conversion


Cycle N
(DO left-justified because R/$\overline{L}$ = "0" in cycle N–1)
Cycle N+1
(DO right-justified because R/$\overline{L}$ = "1" in cycle N)
Analog
Sampling Time
t_{CA} = 4.5 S_{CLK}
Analog
Sampling Time
t_{CA} = 4.5 S_{CLK}
S_{CLK}
1 2 3 4 5 6 7 8 9 10
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
$\overline{CS}$
$\overline{OE}$
DI
A2 A1 A0 R/$\overline{L}$
A2 A1 A0 R/$\overline{L}$
DO
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
6 Leading Zeroes
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
Result of Conversion N–1
Result of Conversion N
SARS
Conversion Time
41 C_{CLK}
(Conversion must complete after DO is clocked out)
Conversion Time
41 C_{CLK}
(Conversion must complete after DO is clocked out)

C_{CLK} continuously enabled

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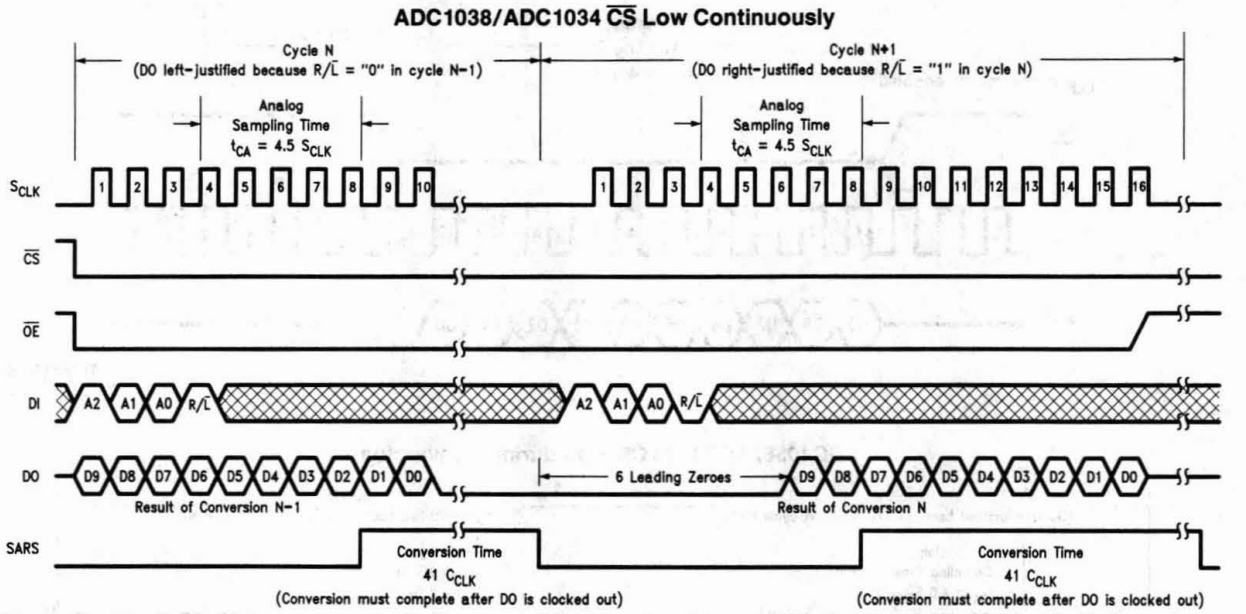
2

Timing Diagrams (Continued)



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C_{CLK} continuously enabled

Multiplexer Address/Channel Assignment Tables

ADC1038

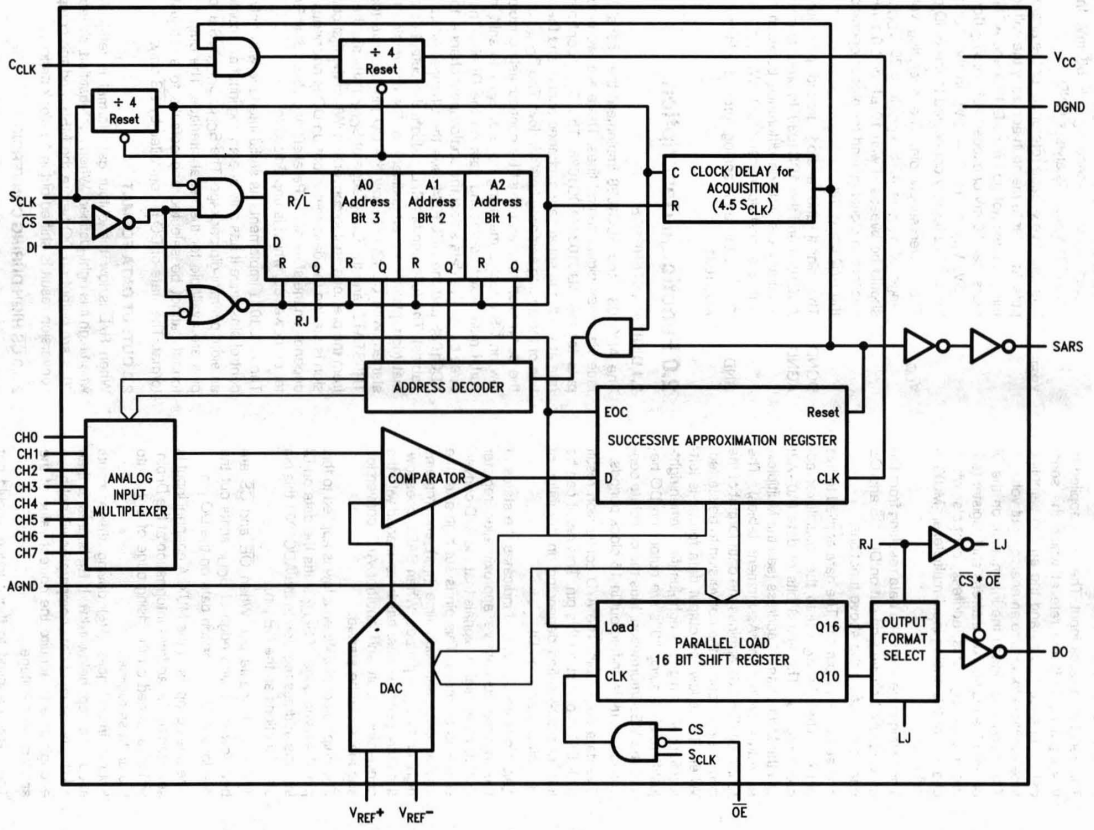
MUX Address			Analog Channel Selected
A2	A1	A0	
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

ADC1034

MUX Address			Analog Channel Selected
A2	A1	A0	
X	0	0	CH0
X	0	1	CH1
X	1	0	CH2
X	1	1	CH3

Note: "X" = don't care

ADC1038 Functional Block Diagram



1.0 Pin Descriptions

C_{CLK} The clock applied to this input controls the successive approximation conversion time interval. The clock frequency applied to this input can be between 700 kHz and 4 MHz.

S_{CLK} The serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs and the analog sampling time available to acquire an analog input voltage. The rising edge loads the information on the DI pin into the multiplexer address shift register (address register). This address controls which channel of the analog input multiplexer (MUX) is selected.

The falling edge shifts the data resulting from the previous A/D conversion out on DO. $\overline{CS}$ and $\overline{OE}$ enable or disable the above functions.

DI The serial data input pin. The data applied to this pin is shifted by S_{CLK} into the multiplexer address register. The first 3 bits of data (A0–A2) are the MUX channel address (see the Multiplexer Address/Channel Assignment tables). The fourth bit (R/$\overline{L}$) determines the data format of the conversion result in the conversion to be started. When R/$\overline{L}$ is low the output data format is left-justified; when high it is right-justified. When right-justified, six leading "0"s are output on DO before the MSB information; thus the complete conversion result is shifted out in 16 clock periods.

DO The data output pin. The A/D conversion result (D0–D9) is output on this pin. This result can be left- or right-justified depending on the value of R/$\overline{L}$ bit shifted in on DI.

SARS This pin is an output and indicates the status of the internal successive approximation register (SAR). When high, it signals that the A/D conversion is in progress. This pin is set high after the analog input sampling time (t_{CA}) and remains high for 41 C_{CLK} periods. When SARS goes low, the output shift register has been loaded with the conversion result and another A/D conversion sequence can be started.

$\overline{CS}$ The chip select pin. When a low is applied to this pin, the rising edge of S_{CLK} shifts the data on DI into the address register. In the ADC1031 this pin also functions as the $\overline{OE}$ pin.

$\overline{OE}$ The output enable pin. When $\overline{OE}$ and $\overline{CS}$ are both low the falling edge of S_{CLK} shifts out the previous A/D conversion data on the DO pin.

CH0–CH7 The analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of S_{CLK} into the address register.

Source impedances (R_S) driving these inputs should be kept below 1 kΩ. If R_S is greater than 1 kΩ, the sampled data comparator will not have enough time to acquire the correct value of the applied input voltage.

The voltage applied to these inputs should not exceed V_{CC} or go below DGND or AGND by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

V_{REF}^+ The positive analog voltage reference for the analog inputs. In order to maintain accuracy the voltage range of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) is 2.5 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF}^+ cannot exceed V_{CC} + 50 mV. In the ADC1031 V_{REF}^- is always GND.

V_{REF}^- The negative voltage reference for the analog inputs. In order to maintain accuracy the voltage at this pin must not go below DGND and AGND by more than 50 mV or exceed 40% of V_{CC} (for V_{CC} = 5V, V_{REF}^- (max) = 2V). In the ADC1031 V_{REF}^- is internally connected to the GND pin.

V_{CC} The power supply pin. The operating voltage range of V_{CC} is 4.75 V_{DC} to 5.25 V_{DC}. V_{CC} should be bypassed with 10 μF and 0.1 μF capacitors to digital ground for proper operation of the A/D converter.

DGND, AGND The digital and analog ground pins for the ADC1034 and the ADC1038. In order to maintain accuracy the voltage difference between these two pins must not exceed 300 mV.

GND The digital and analog ground pin for the ADC1031.

2.0 Functional Description

2.1 DIGITAL INTERFACE

The ADC1034 and ADC1038 implement their serial interface via seven digital control lines. There are two clock inputs for the ADC1034/ADC1038. The S_{CLK} controls the rate at which the serial data exchange occurs and the duration of the analog sampling time window. The C_{CLK} controls the conversion time and must be continuously enabled. A low on $\overline{CS}$ enables the rising edge of S_{CLK} to shift in the serial multiplexer addressing data on the DI pin. The first three bits of this data select the analog input channel for the ADC1038 and the ADC1034 (see the Channel Addressing Tables). The following bit, R/$\overline{L}$, selects the output data format (right-justified or left-justified) for the conversion to be started. With $\overline{CS}$ and $\overline{OE}$ low the DO pin is active (out of TRI-STATE) and the falling edge of S_{CLK} shifts out the data from the previous analog conversion. When the first conversion is started the data shifted out on DO is erroneous as it depends on the state of the Parallel Load 16-Bit Shift Register on power up, which is unpredictable.

The ADC1031 implements its serial interface with only four control pins since it has only one analog input and comes in an eight pin mini-dip package. The S_{CLK}, C_{CLK}, $\overline{CS}$ and $\overline{DO}$ pins are available for the serial interface. The output data format cannot be selected and defaults to a left-justified format. The state of DO is controlled by $\overline{CS}$ only.

2.2 OUTPUT DATA FORMAT

When R/$\overline{L}$ is low the output data format is left-justified; when high it is right-justified. When right-justified, six leading "0"s are output on DO before the MSB, and the complete conversion result is shifted out in 16 clock periods.

2.3.0 $\overline{CS}$ HIGH DURING CONVERSION

With a continuous S_{CLK} input, $\overline{CS}$ must be used to synchronize the serial data exchange. A valid $\overline{CS}$ is recognized if it occurs at least 100 ns (t_{SET-UP}) before the rising edge of S_{CLK}, thus causing data to be input on DI. If this does not

2.0 Functional Description (Continued)

occur there will be an uncertainty as to which S_{CLK} rising edge will clock in the first bit of data. $\overline{CS}$ must remain low during the complete I/O exchange. Also, $\overline{OE}$ needs to be low if data from the previous conversion needs to be accessed.

2.3.1 $\overline{CS}$ LOW CONTINUOUSLY

Another way to accomplish synchronous serial communication is to tie $\overline{CS}$ low continuously and use SARS and S_{CLK} to synchronize the serial data exchange. S_{CLK} can be disabled low during the conversion time and enabled after SARS goes low. With $\overline{CS}$ low during the conversion time a zero will remain on DO until the conversion is completed. Once the conversion is complete, the falling edge of SARS will shift out on DO the MSB before S_{CLK} is enabled. This MSB would be a leading zero if right-justified or D9 if left-justified. The rest of the data will be shifted out once S_{CLK} is enabled as discussed previously. If $\overline{CS}$ goes high during the conversion sequence DO is put into TRI-STATE, and the conversion result is not affected so long as $\overline{CS}$ remains high until the end of the conversion.

2.4 TYING S_{CLK} and C_{CLK} TOGETHER

S_{CLK} and C_{CLK} can be tied together. The total conversion time will increase because the maximum clock frequency is now 1 MHz. The timing diagrams and the serial I/O exchange time (10 S_{CLK} cycles) remain the same, but the conversion time (T_C = 41 C_{CLK} cycles) lengthens from a minimum of 14 μs to a minimum of 41 μs. In the case where $\overline{CS}$ is low continuously, since the applied clock cannot be disabled, SARS must be used to synchronize the data output on DO and initiate a new conversion. The falling edge of SARS sends the MSB information out on DO. The next rising edge of the clock shifts in MUX address bit A2 on DI. The following clock falling edge will clock the next data bit of information out on DO. A conversion will be started after MUX addressing information has been loaded in (3 more clocks) and the analog sampling time (4.5 clocks) has elapsed. The ADC1031 does not have SARS. Therefore, $\overline{CS}$ cannot be left low continuously on the ADC1031.

3.0 Analog Considerations

3.1 THE INPUT SAMPLE AND HOLD

The ADC1031/4/8's sample/hold capacitor is implemented in its capacitive ladder structure. After the channel address is received, the ladder is switched to sample the proper analog input. This sampling mode is maintained for 4.5 S_{CLK} cycles after the multiplexer addressing information is loaded in. For the ADC1031/4/8, the sampling of the analog input starts on S_{CLK}'s 4th rising edge.

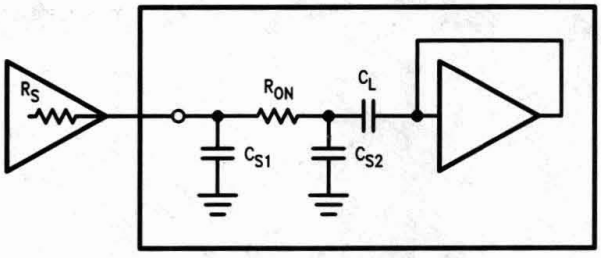


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FIGURE 1. Analog Input Model

An acquisition window of 4.5 S_{CLK} cycles is available to allow the ladder capacitance to settle to the analog input voltage. Any change in the analog voltage before or after the acquisition window will not effect the A/D conversion result.

In the most simple case, the ladder's acquisition time is determined by the R_{on} (9 kΩ) of the multiplexer switches, the C_{S1} (3.5 pF) and the total ladder (C_L) and stray (C_{S2}) capacitance (48 pF). For large source resistance the analog input can be modeled as an RC network as shown in *Figure 1*. The values shown yield an acquisition time of about 3 μs for 10 bit accuracy with a zero to a full scale change in the reading. External source resistance and capacitance will lengthen the acquisition time and should be accounted for.

The curve "Signal to Noise Ratio vs Output Frequency" *(Figure 2)* gives an indication of the usable bandwidth of the ADC1031/ADC1034/ADC1038. The signal to noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the A/D. An ideal 10 bit A/D converter with a total unadjusted error of 0 LSB would have a signal to noise ratio of about 62 dB, which can be derived from the equation:

$$S/N = 6.02(N) + 1.8$$

where S/N is in dB and N is the number of bits. *Figure 2* shows the signal to noise ratio vs. input frequency of a typical ADC1031/4/8 with ½ LSB total unadjusted error. The dotted lines show signal-to-noise ratios for an ideal (noiseless) 10 bit A/D with 0 LSB error and an A/D with a 1 LSB error.

The sample-and-hold error specifications are included in the error and timing specifications of the A/D. The hold step and gain error sample/hold specs are taken into account in the ADC1031/4/8's total unadjusted error specification, while the hold settling time is included in the A/D's maximum conversion time specification. The hold droop rate can be thought of as being zero since an unlimited amount of time can pass between a conversion and the reading of data. However, once the data is read it is lost and another conversion is started.

3.2 INPUT FILTERING

Due to the sampling nature of the analog input, transients will appear on the input pins. They are caused by the ladder capacitance and internal stray capacitance charging current flowing into V_{IN}. These transients will not degrade the A/D's performance if they settle out within the sampling window. This will occur if external source resistance is kept to a minimum.

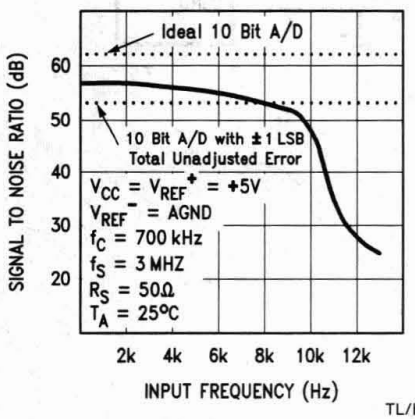

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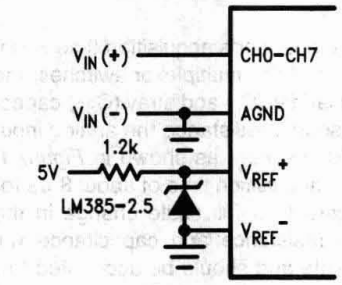
FIGURE 2. ADC1031/4/8 Signal to Noise Ratio vs Input Frequency

2

3.0 Analog Considerations (Continued)

External Reference 2.5V Full Scale



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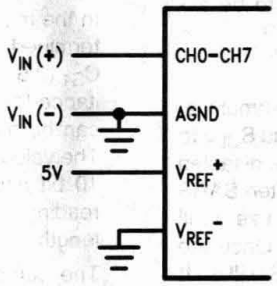
Power Supply as Reference



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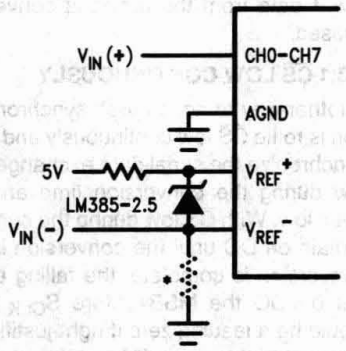
Input Not Referred to GND



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*Current path must still exist from $V_{IN}(-)$ to ground

FIGURE 3. Analog Input Options

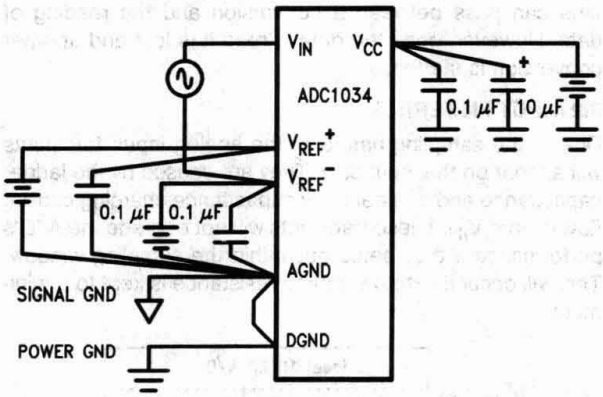
3.3 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC1031/4/8 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{REF}+$ and $V_{REF}-$. By reducing V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF} = 2V then 1 LSB = 1.95 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

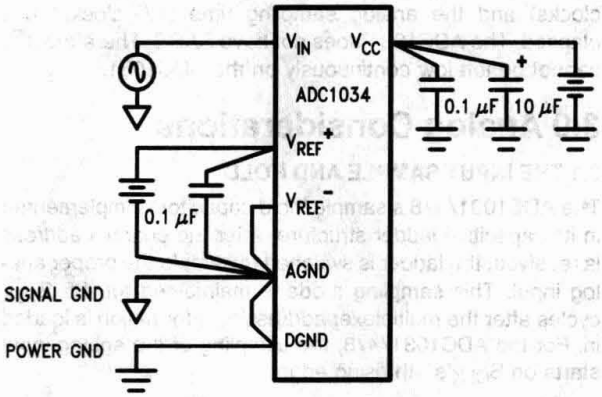
This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}-$ sets the input level which produces a digital output of all zeros. Though V_{IN} is not itself differential, the reference design allows nearly differential-input capability for many measurement applications. *Figure 3* shows some of the configurations that are possible.

The ADC1031 has no $V_{REF}-$ pin. $V_{REF}-$ is internally tied to GND.

Power Supply Bypassing



TL/H/10556–23



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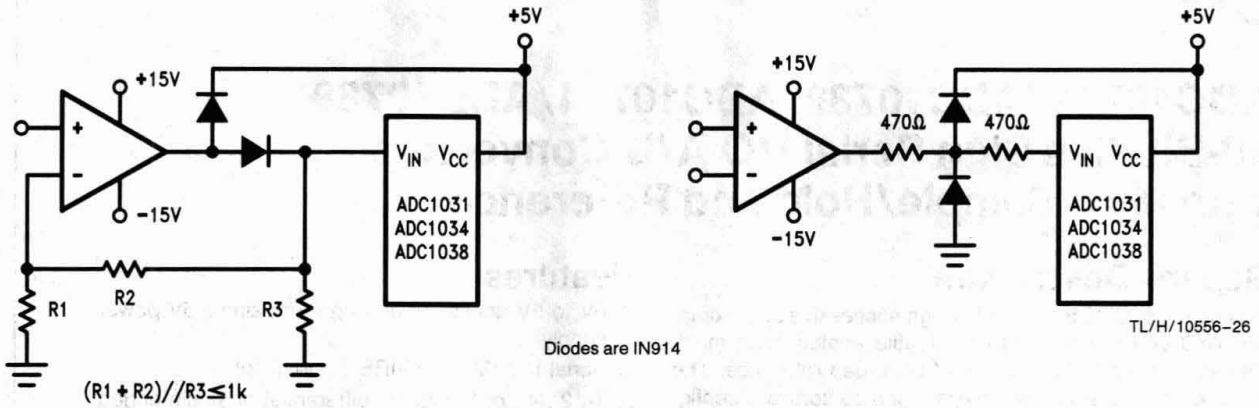
Protecting the Analog Inputs

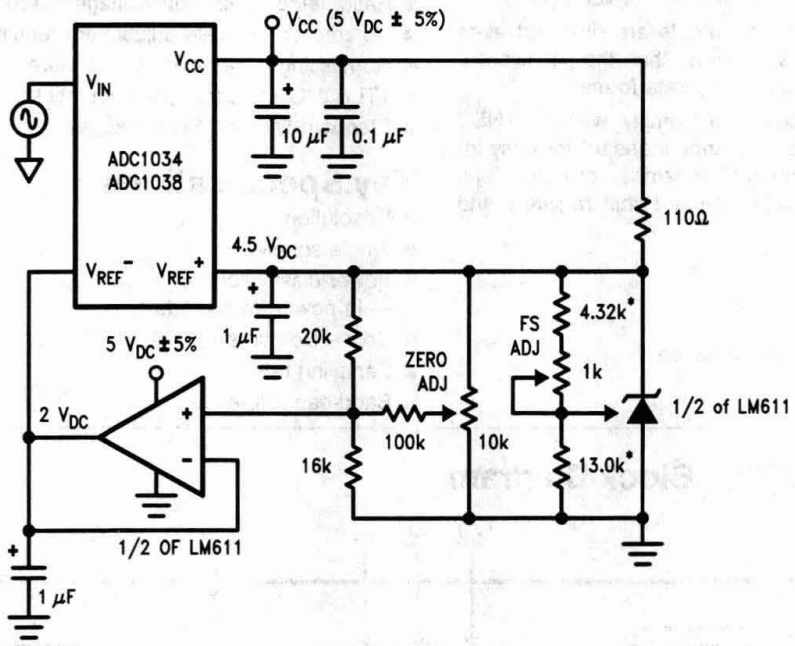


Diodes are IN914

TL/H/10556–26

TL/H/10556–25

Zero-Shift and Span-Adjust (2V ≤ V_{IN} ≤ 4.5V)



*1% resistors

TL/H/10556–27

National Semiconductor

ADC10731/ADC10732/ADC10734/ADC10738 10-Bit Plus Sign Serial I/O A/D Converters with Mux, Sample/Hold and Reference

General Description

This series of CMOS 10-bit plus sign successive approximation A/D converters features versatile analog input multiplexers, sample/hold and a 2.5V band-gap reference. The 1-, 2-, 4-, or 8-channel multiplexers can be software configured for single-ended or differential mode of operation.

An input sample/hold is implemented by a capacitive reference ladder and sampled-data comparator. This allows the analog input to vary during the A/D conversion cycle.

In the differential mode, valid outputs are obtained even when the negative inputs are greater than the positive because of the 10-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC™ families of controllers, and can easily interface with standard shift registers and microprocessors.

Applications

- Medical instruments
- Portable and remote instrumentation
- Test equipment

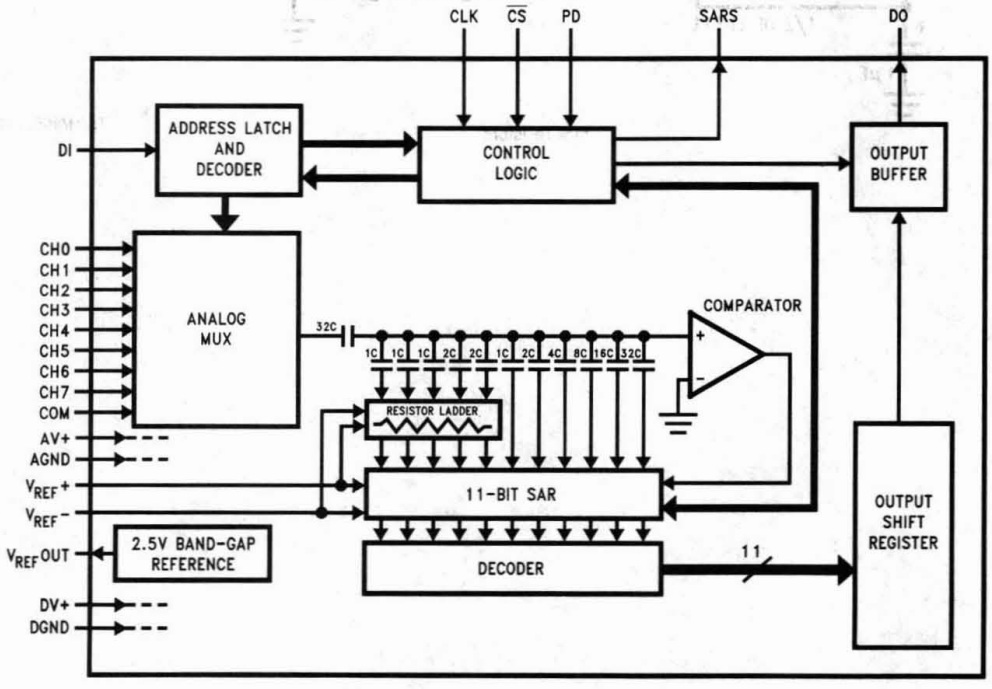
Features

- 0V to 5V analog input range with single 5V power supply
- Serial I/O (MICROWIRE compatible)
- 1-, 2-, 4-, or 8-channel differential or single-ended multiplexer
- Software or hardware power down
- Analog input sample/hold function
- Ratiometric or absolute voltage referencing
- No zero or full scale adjustment required
- No missing codes over temperature
- TTL/CMOS input/output compatible
- Standard DIP and SO packages

Key Specifications

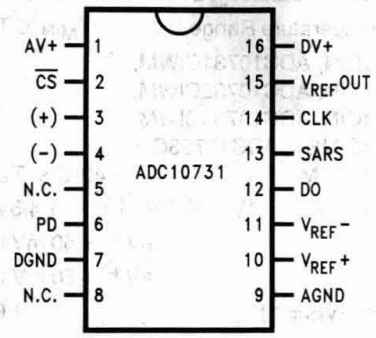
■ Resolution	10 bits plus sign
■ Single supply	5V
■ Power dissipation	37 mW (Max)
— In powerdown mode	18 μW
■ Conversion time	5 μs (Max)
■ Sampling rate	74 kHz (Max)
■ Band-gap reference	2.5V ±2% (Max)

ADC10738 Simplified Block Diagram



TL/H/11390–1

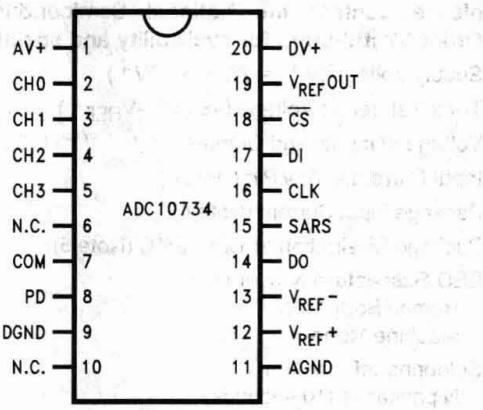
Connection Diagrams for Dual-In-Line and SO Packages



TL/H/11390–2

Top View

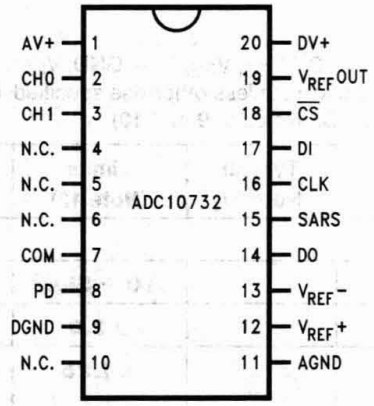
See NS Package Number N16E or M16B



TL/H/11390–4

Top View

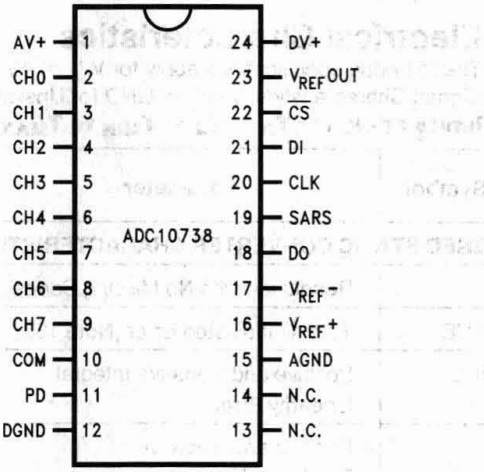
See NS Package Number N20A or M20B



TL/H/11390–3

Top View

See NS Package Number N20A or M20B

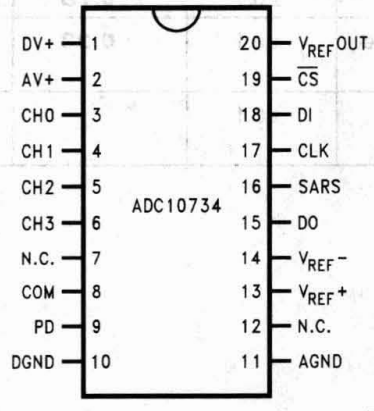


TL/H/11390–5

Top View

See NS Package Number N24A or M24B

Connection Diagram for the SSOP Package



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See NS Package Number MSA20

Ordering Information

Industrial Temperature Range $-40°C \leq T_A \leq +85°C$	Package
ADC10731CIN	N16E
ADC10731CIWM	M16B
ADC10732CIN	N20A
ADC10732CIWM	M20B
ADC10734CIMSA	MSA20
ADC10734CIN	N20A
ADC10734CIWM	M20B
ADC10738CIN	N24A
ADC10738CIWM	M24B

2

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ = AV^+ = DV^+$)	6.5V
Total Reference Voltage ($V_{REF}^+ - V_{REF}^-$)	6.5V
Voltage at Inputs and Outputs	$V^+ + 0.3V$ to $-0.3V$
Input Current at Any Pin (Note 4)	30 mA
Package Input Current (Note 4)	120 mA
Package Dissipation at $T_A = 25°C$ (Note 5)	500 mW
ESD Susceptability (Note 6)	
Human Body Model	2500V
Machine Model	150V
Soldering Information	
N packages (10 seconds)	260°C
SO Package (Note 7)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	$-40°C$ to $+150°C$

Operating Ratings (Notes 2 and 3)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10731CIN, ADC10731CIWM, ADC10732CIN, ADC10732CIWM, ADC10734CIN, ADC10734CIWM, ADC10734CIMSA, ADC10738CIN, ADC10738CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage ($V^+ = AV^+ = DV^+$)	$+4.5V$ to $+5.5V$
V_{REF}^+	$AV^+ + 50$ mV to -50 mV
V_{REF}^-	$AV^+ + 50$ mV to -50 mV
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	$+0.5V$ to V^+

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 2.5\ V_{DC}$, $V_{REF}^- = GND$, $V_{IN}^- = 2.5V$ for Signed Characteristics, $V_{IN}^- = GND$ for Unsigned Characteristics and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
SIGNED STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10 + Sign**	Bits
TUE	Total Unadjusted Error (Note 13)			**±2.0**	LSB(max)
INL	Positive and Negative Integral Linearity Error			**±1.25**	LSB(max)
	Positive and Negative Full-Scale Error			**±1.5**	LSB(max)
	Offset Error			**±1.5**	LSB(max)
	Power Supply Sensitivity				
	Offset Error	$V^+ = +5.0V \pm 10\%$	±0.2	**±1.0**	LSB(max)
	+ Full-Scale Error		±0.2	**±1.0**	LSB(max)
	− Full-Scale Error		±0.1	**±0.75**	LSB(max)
	DC Common Mode Error (Note 14)	$V_{IN}^+ = V_{IN}^- = V_{IN}$ where $5.0V \ge V_{IN} \ge 0V$	±0.1	**±0.33**	LSB(max)
	Multiplexer Channel to Channel Matching		±0.1		LSB

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 2.5\ V_{DC}$, $V_{REF}^- = GND$, $V_{IN}^- = 2.5V$ for Signed Characteristics, $V_{IN}^- = GND$ for Unsigned Characteristics and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10) (Continued)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
UNSIGNED STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10**	Bits
TUE	Total Unadjusted Error (Note 13)	$V_{REF}^+ = 4.096V$	±0.75		LSB
INL	Integral Linearity Error	$V_{REF}^+ = 4.096V$	±0.50		LSB
	Full-Scale Error	$V_{REF}^+ = 4.096V$		**±1.25**	LSB(max)
	Offset Error	$V_{REF}^+ = 4.096V$		**±1.25**	LSB(max)
	Power Supply Sensitivity Offset Error Full-Scale Error	 $V^+ = +5.0V \pm 10\%$ $V_{REF}^+ = 4.096V$	 ±0.1 ±0.1		 LSB LSB
	DC Common Mode Error (Note 14)	$V_{IN}^+ = V_{IN}^- = V_{IN}$ where $+5.0V \geq V_{IN} \geq 0V$	±0.1		LSB
	Multiplexer Channel to Channel Matching	$V_{REF}^+ = 4.096V$	±0.1		LSB
DYNAMIC SIGNED CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	67		dB
ENOB	Effective Number of Bits	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	10.8		Bits
THD	Total Harmonic Distortion	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	−78		dB
IMD	Intermodulation Distortion	$V_{IN} = 4.85\ V_{PP}$, and f_{IN} = 1 kHz to 15 kHz	−85		dB
	Full-Power Bandwidth	$V_{IN} = 4.85\ V_{PP}$, where S/(N + D) Decreases 3 dB	380		kHz
	Multiplexer Channel to Channel Crosstalk	f_{IN} = 15 kHz	−80		dB

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 2.5\ V_{DC}$, $V_{REF}^- = GND$, $V_{IN}^- = 2.5V$ for Signed Characteristics, $V_{IN}^- = GND$ for Unsigned Characteristics and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10) (Continued)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
DYNAMIC UNSIGNED CONVERTER CHARACTERISTIC					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$V_{REF}^+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and $f_{IN} = 1$ kHz to 15 kHz	60		dB
	Effective Bits	$V_{REF}^+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and $f_{IN} = 1$ kHz to 15 kHz	9.8		Bits
THD	Total Harmonic Distortion	$V_{REF}^+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and $f_{IN} = 1$ kHz to 15 kHz	−70		dB
IMD	Intermodulation Distortion	$V_{REF}^+ = 4.096V$, $V_{IN} = 4.0\ V_{PP}$, and $f_{IN} = 1$ kHz to 15 kHz	−73		dB
	Full-Power Bandwidth	$V_{IN} = 4.0\ V_{PP}$, $V_{REF}^+ = 4.096V$, where S/(N+D) decreases 3 dB	380		kHz
	Multiplexer Channel to Channel Crosstalk	$f_{IN} = 15$ kHz, $V_{REF}^+ = 4.096V$	−80		dB
REFERENCE INPUT AND MULTIPLEXER CHARACTERISTICS					
	Reference Input Resistance		7	**5.0** **9.5**	kΩ kΩ(min) kΩ(max)
C_{REF}	Reference Input Capacitance		70		pF
	MUX Input Voltage			**−50** **$AV^+ + 50$ mV**	mV(min) (max)
C_{IM}	MUX Input Capacitance		47		pF
	Off Channel Leakage Current (Note 15)	On Channel = 5V and Off Channel = 0V	−0.4	**−3.0**	µA(max)
		On Channel = 0V and Off Channel = 5V	0.4	**3.0**	µA(max)
	On Channel Leakage Current (Note 15)	On Channel = 5V and Off Channel = 0V	0.4	**3.0**	µA(max)
		On Channel = 0V and Off Channel = 5V	−0.4	**−3.0**	µA(max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 2.5\ V_{DC}$, $V_{REF}^- = GND$, $V_{IN}^- = 2.5V$ for Signed Characteristics, $V_{IN}^- = GND$ for Unsigned Characteristics and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10) (Continued)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
REFERENCE CHARACTERISTICS					
$V_{REF}Out$	Reference Output Voltage		2.5V ±0.5%	**2.5V ±2%**	V(max)
$\Delta V_{REF}/\Delta T$	$V_{REF}Out$ Temperature Coefficient		±40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation, Sourcing	0 mA ≤ I_L ≤ +4 mA	±0.003	±**0.05**	%/mA(max)
$\Delta V_{REF}/\Delta I_L$	Load Regulation, Sinking	0 mA ≤ I_L ≤ −1 mA	±0.2	±**0.6**	%/mA(max)
	Line Regulation	5V ±10%	±0.3	±**2.5**	mV(max)
I_{SC}	Short Circuit Current	$V_{REF}Out$ = 0V	13	**22**	mA(max)
	Noise Voltage	10 Hz to 10 kHz, C_L = 100 μF	5		μV
$\Delta V_{REF}/\Delta t$	Long-term Stability		±120		ppm/kHr
t_{SU}	Start-Up Time	C_L = 100 μF	100		ms
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V^+ = 5.5V		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage	V^+ = 4.5V		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.0V	0.005	+**2.5**	μA(max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−0.005	−**2.5**	μA(max)
$V_{OUT(1)}$	Logical "1" Output Voltage	V^+ = 4.5V, I_{OUT} = −360 μA V^+ = 4.5V, I_{OUT} = −10 μA		**2.4** **4.5**	V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V^+ = 4.5V, I_{OUT} = 1.6 mA		**0.4**	V(min)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V V_{OUT} = 5V	−0.1 +0.1	−**3.0** +**3.0**	μA(max) μA(max)
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V, V^+ = 4.5V	−30	−**15**	mA(min)
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V^+ = 4.5V	30	**15**	mA(min)
I_D^+	Digital Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up $\overline{CS}$ = HIGH, Power Down $\overline{CS}$ = HIGH, Power Down, and CLK Off	0.9 0.2 0.5	**1.3** **0.4** **50**	mA(max) mA(max) μA(max)
I_A^+	Analog Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up $\overline{CS}$ = HIGH, Power Down	2.7 3	**6.0** **15**	mA(max) μA(max)
I_{REF}	Reference Input Current	V_{REF}^+ = +2.5V and $\overline{CS}$ = HIGH, Power Up		**0.6**	mA(max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = 2.5\ V_{DC}$, V_{REF}^- = GND, V_{IN}^- = 2.5V for Signed Characteristics, V_{IN}^- = GND for Unsigned Characteristics and f_{CLK} = 2.5 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Note 16)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
AC CHARACTERISTICS					
f_{CLK}	Clock Frequency		3.0 5	**2.5**	MHz(max) kHz(min)
	Clock Duty Cycle			**40** **60**	%(min) %(max)
t_C	Conversion Time		12 5	**12** **5**	Clock Cycles μs(max)
t_A	Acquisition Time		4.5 2	**4.5** **2**	Clock Cycles μs(max)
t_{SCS}	$\overline{CS}$ Set-Up Time, Set-Up Time from Falling Edge of CS to Rising Edge of Clock		14 (1 t_{CLK} − 14 ns)	**30** **(1 t_{CLK} −30 ns)**	ns(min) (max)
t_{SDI}	DI Set-Up Time, Set-Up Time from Data Valid on DI to Rising Edge of Clock		16	**25**	ns(min)
t_{HDI}	DI Hold Time, Hold Time of DI Data from Rising Edge of Clock to Data not Valid on DI		2	**25**	ns(min)
t_{AT}	DO Access Time from Rising Edge of CLK When $\overline{CS}$ is "Low" during a Conversion		30	**50**	ns(min)
t_{AC}	DO or SARS Access Time from $\overline{CS}$, Delay from Falling Edge of $\overline{CS}$ to Data Valid on DO or SARS		30	**70**	ns(max)
t_{DSARS}	Delay from Rising Edge of Clock to Falling Edge of SARS when $\overline{CS}$ is "Low"		100	**200**	ns(max)
t_{HDO}	DO Hold Time, Hold Time of Data on DO after Falling Edge of Clock		20	**35**	ns(max)
t_{AD}	DO Access Time from Clock, Delay from Falling Edge of Clock to Valid Data of DO		40	**80**	ns(max)
t_{1H}, t_{0H}	Delay from Rising Edge of $\overline{CS}$ to DO or SARS TRI-STATE		40	**50**	ns(max)
t_{DCS}	Delay from Falling Edge of Clock to Falling Edge of $\overline{CS}$		20	**30**	ns(min)
$t_{CS(H)}$	$\overline{CS}$ "HIGH" Time for A/D Reset after Reading of Conversion Result		1 CLK	**1 CLK**	cycle(min)
$t_{CS(L)}$	ADC10731 Minimum $\overline{CS}$ "Low" Time to Start a Conversion		1 CLK	**1 CLK**	cycle(min)
t_{SC}	Time from End of Conversion to $\overline{CS}$ Going "Low"		5 CLK	**5 CLK**	cycle(min)
t_{PD}	Delay from Power-Down command to 10% of Operating Current		1		μs
t_{PC}	Delay from Power-Up Command to Ready to Start a New Conversion		10		μs
C_{IN}	Capacitance of Logic Inputs		7		pF
C_{OUT}	Capacitance of Logic Outputs		12		pF

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifcations and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > AV^+$ or DV^+), the current at that pln should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.

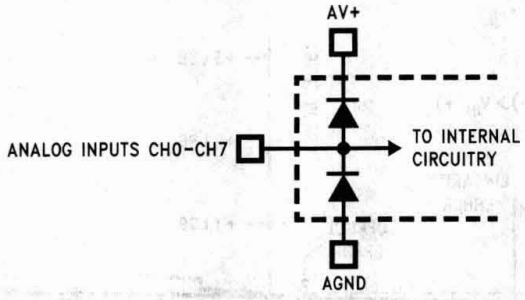
Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given In the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$. The typical thermal resistance (θ_{JA}) of these Paris when board mounted can be found in the following table:

Part Number	Thermal Resistance	Package Type
ADC10731CIN	82°C/W	N16E
ADC10731CIWM	90°C/W	M16B
ADC10732CIN	47°C/W	N20A
ADC10732CIWM	80°C/W	M20B
ADC10734CIMSA	134°C/W	MSA20
ADC10734CIN	47°C/W	N20A
ADC10734CIWM	80°C/W	M20B
ADC10738CIN	60°C/W	N24A
ADC10738CIWM	75°C/W	M24B

Note 6: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 7: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titied "Surtace Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surtace mount devices.

Note 8: Two on-ohip diodes are tied to each analog input as shown below. They will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V^+ supply. Be careful during testing at low V^+ levels (+4.5V), as high level analog inputs (+5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors In the conversion result. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be oorrect. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. If AV^+ and DV^+ are minimum (4.5 V_{DC}) and full scale must be $\leq +4.55$ V_{DC}.



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Note 9: No connection exists between AV^+ and DV^+ on the chip.

To guarantee accuracy, it is required that the AV^+ and DV^+ be connected together to a power supply with separate bypass filter at eacn V^+ pin.

Note 10: One LSB is referenced to 10 bits of resolution.

Note 11: Typicals are at $T_J = T_A = 25°C$ and represent most likely pararmetric norm.

Note 12: Tested limits are guaranteed to National's AOQL (Average Outgolng Quality Level).

Note 13: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 14: The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.

Note 15: Channel leakage current is measured after the channel selection.

Note 16: All the timing specifications are tested at the TTL logic levels, $V_{IL} = 0.8V$ for a falling edge and $V_{IH} = 2.0V$ for a rising. TRI-STATE voltage level is forced to 1.4V.

Note 17: The voltage applied to the digital inputs will affect the current drain during power down. These devices are tested with CMOS logic levels (logic Low = 0V and logic High = 5V). TTL levels increase the current, during power down, to about 300 μA.

Electrical Characteristics (Continued)

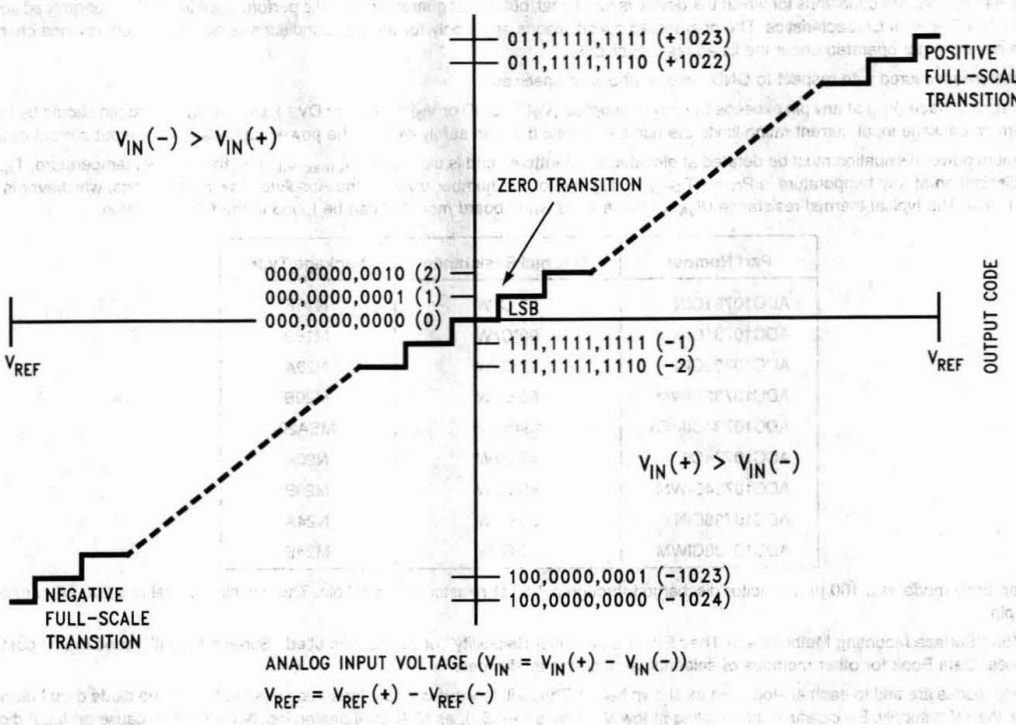

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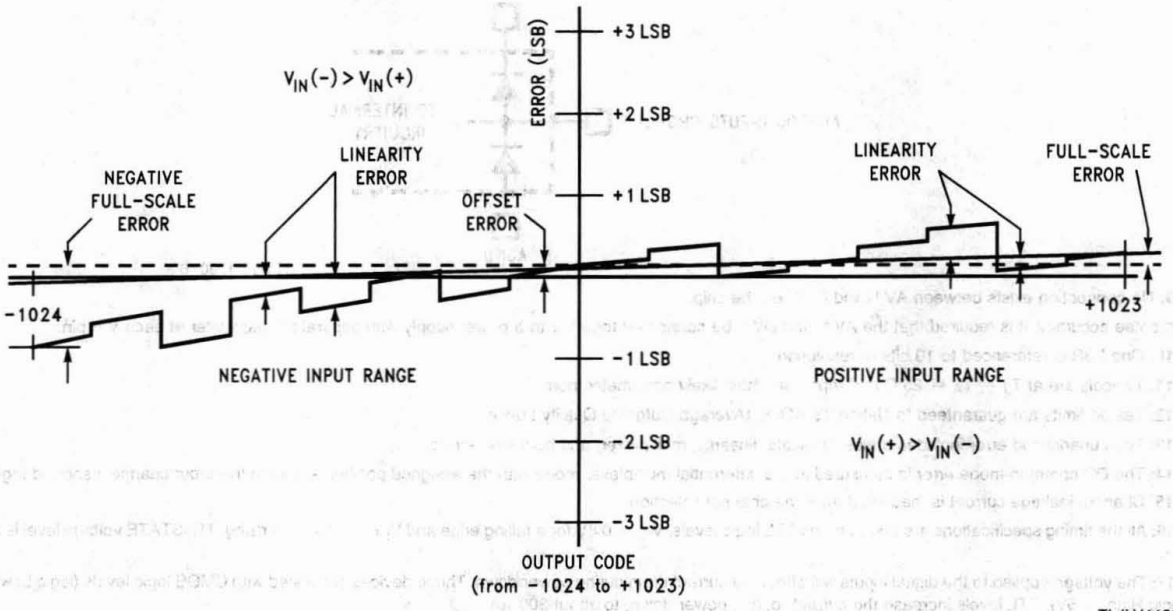
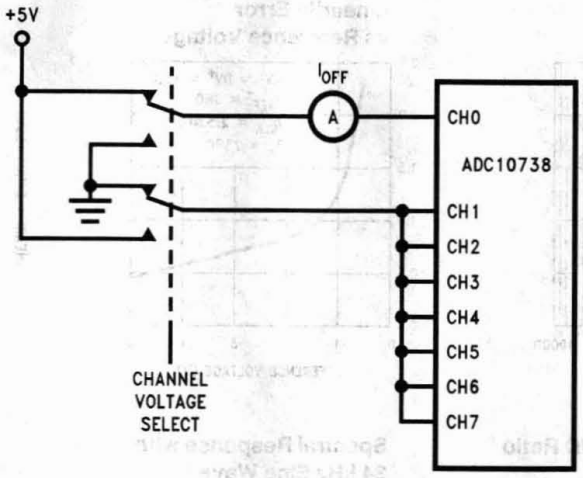
FIGURE 1A. Transter Characteristic



TL/H/11390-26

FIGURE 1B. Simplified Error Curve vs Output Code

Leakage Current Test Circuit



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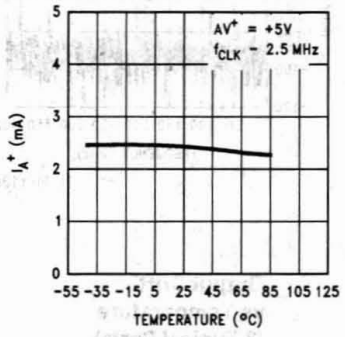
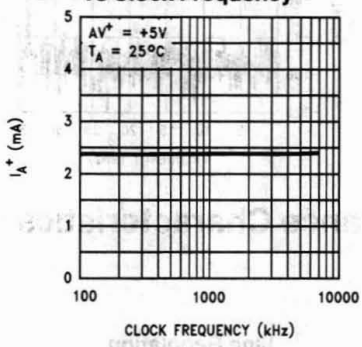
Typical Performance Characteristics

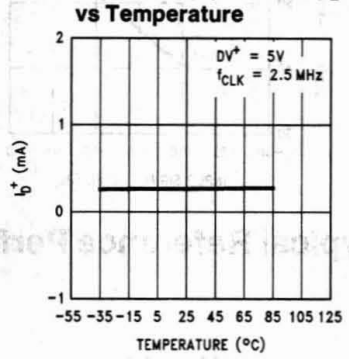
Analog Supply Current (I_A+) vs Temperature



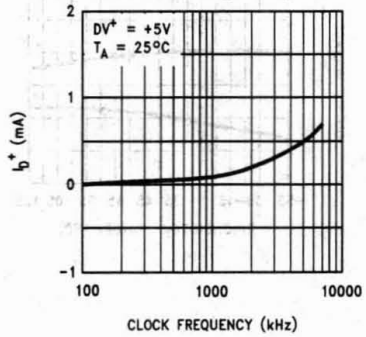
Analog Supply Current (I_A+) vs Clock Frequency



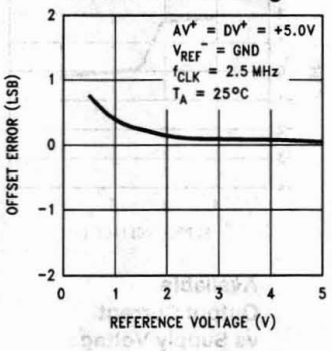
Digital Supply Current (I_D+) vs Temperature



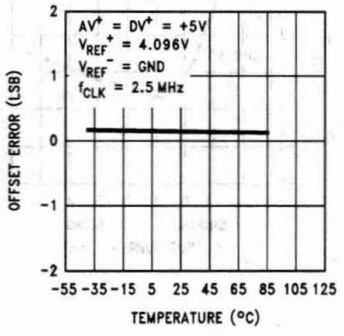
Digital Supply Current (I_D+) vs Clock Frequency



Offset Error vs Reference Voltage



Offset Error vs Temperature



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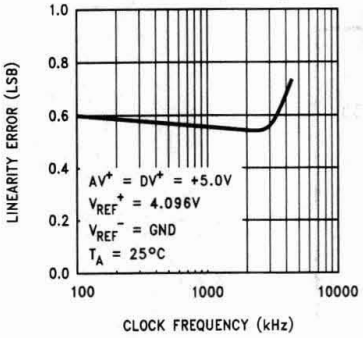
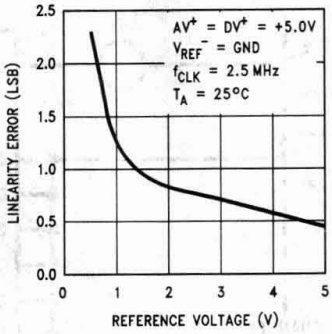
2

Typical Performance Characteristics (Continued)

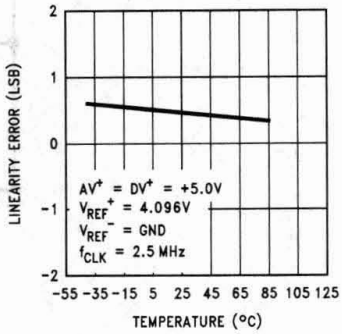
Linearity Error vs Clock Frequency



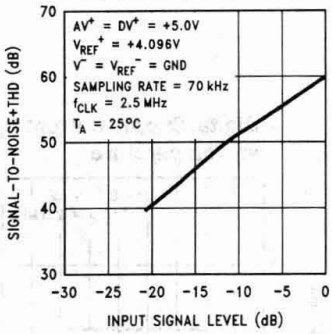
Linearity Error vs Reference Voltage



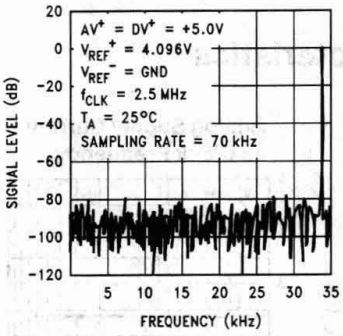
Linearity Error vs Temperature



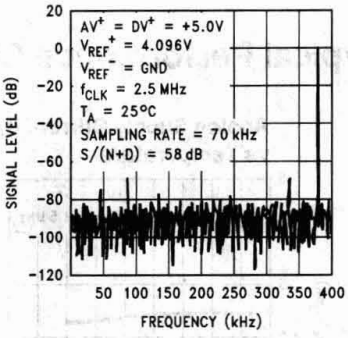
10-Bit Unsigned Signal-to-Noise + THD Ratio vs Input Signal Level



Spectral Response with 34 kHz Sine Wave



Power Bandwidth Response with 380 kHz Sine Wave



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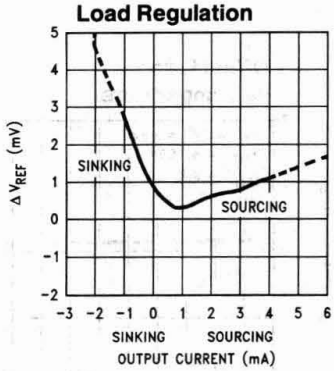
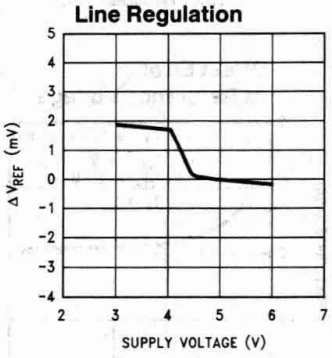
Typical Reference Performance Characteristics

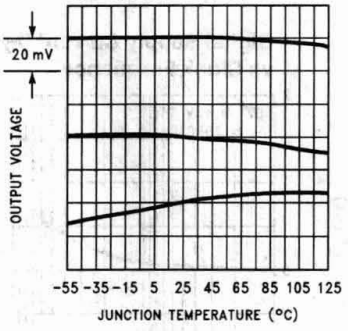
Load Regulation



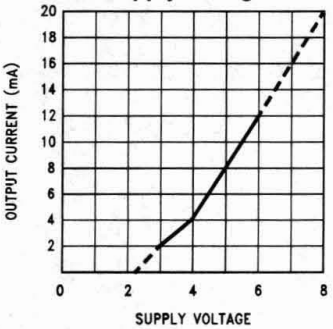
Line Regulation



Output Drift vs Temperature (3 Typical Parts)



Available Output Current vs Supply Voltage



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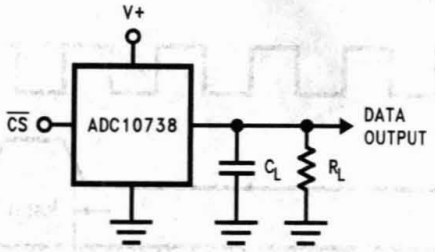
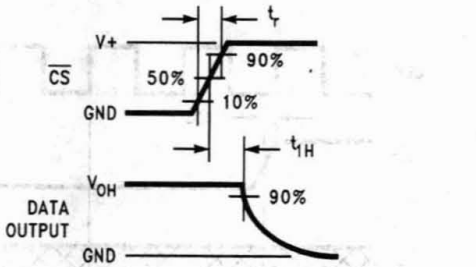
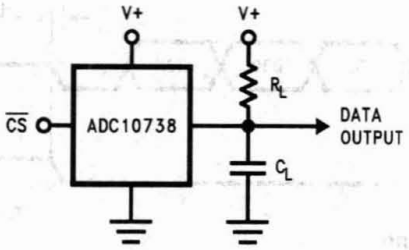
TRI-STATE Test Circuits and Waveforms



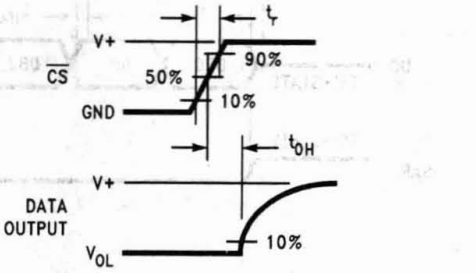
TL/H/11390-10



TL/H/11390-11

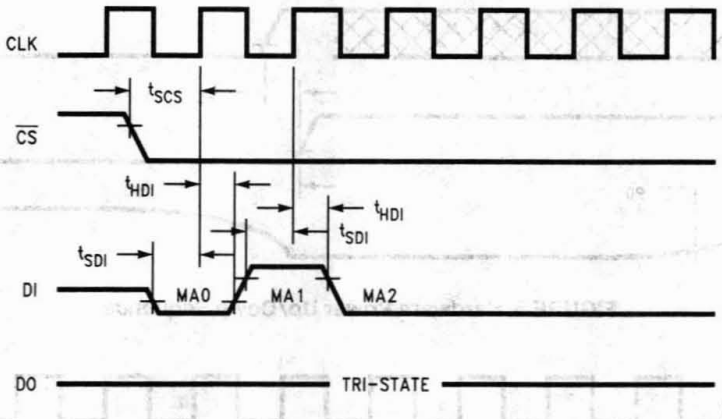


TL/H/11390-12



TL/H/11390-13

Timing Diagrams



TL/H/11390-14

FIGURE 2. DI Timing

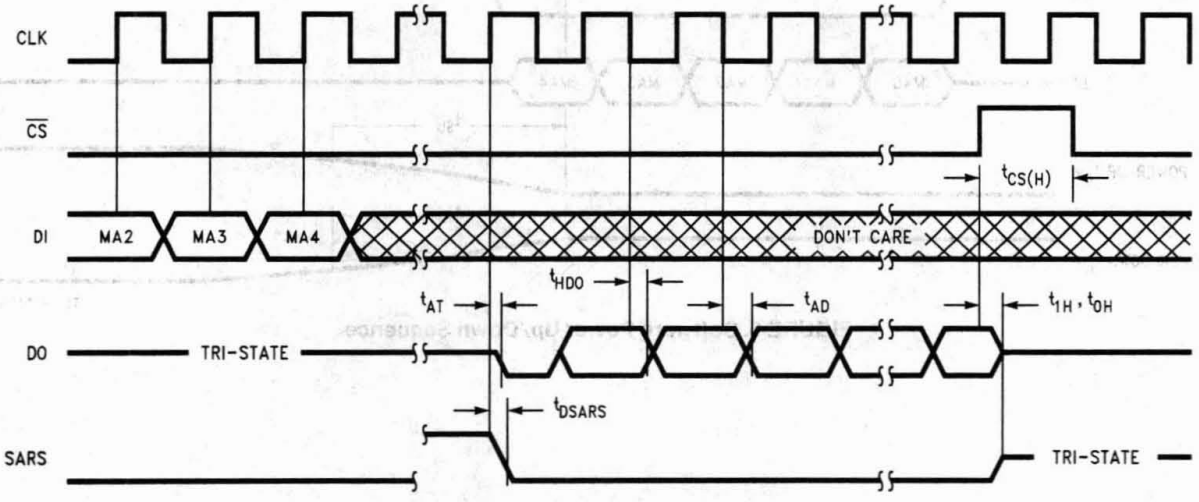


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FIGURE 3. DO Timing

2

Timing Diagrams (Continued)

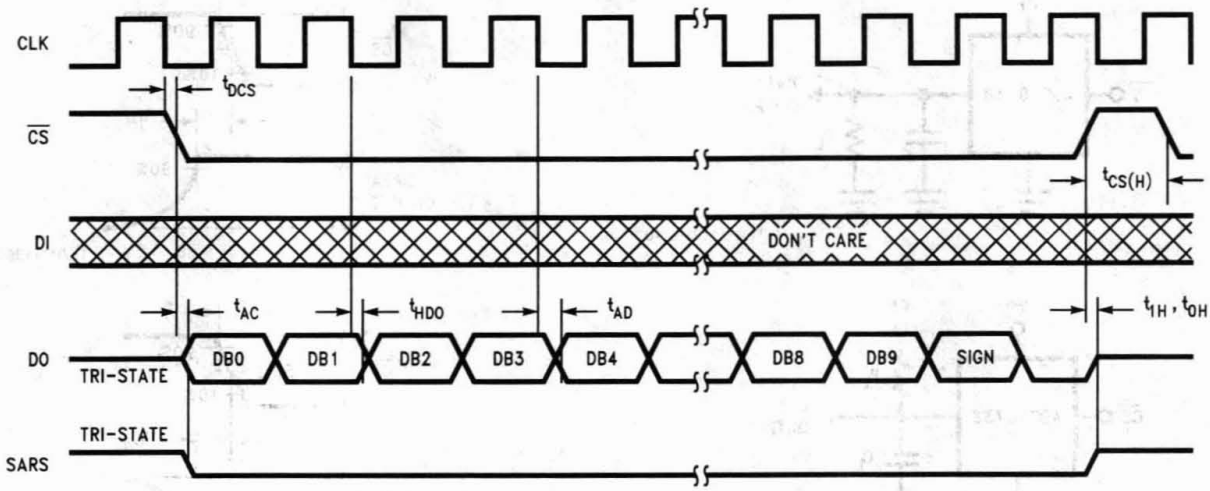

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FIGURE 4. Delayed DO Timing

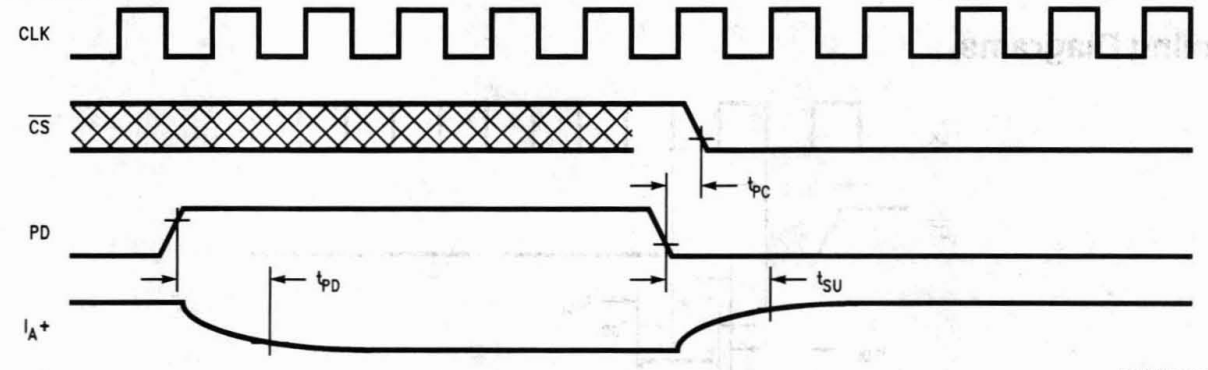

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FIGURE 5. Hardware Power Up/Down Sequence

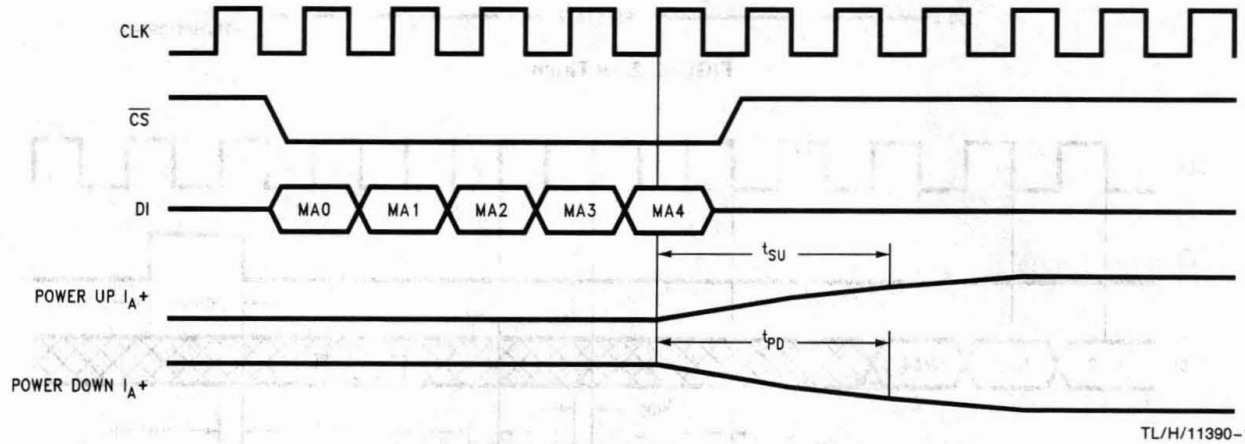

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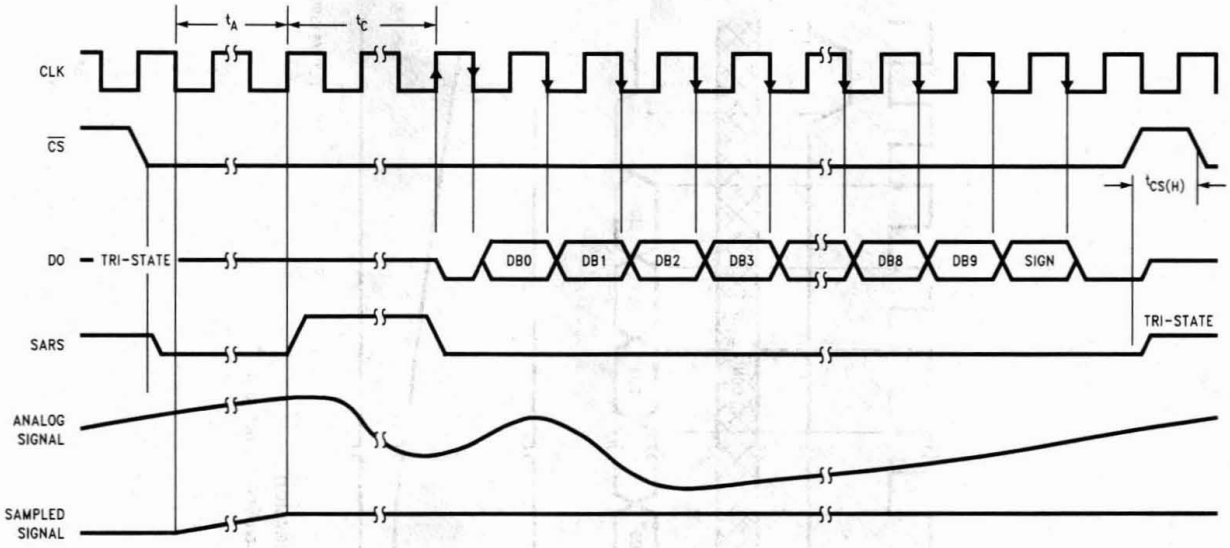
FIGURE 6. Software Power Up/Down Sequence

Timing Diagrams (Continued)



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Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is invalid.

FIGURE 7. ADC10731 $\overline{CS}$ Low during Conversion

Timing Diagrams (Continued)

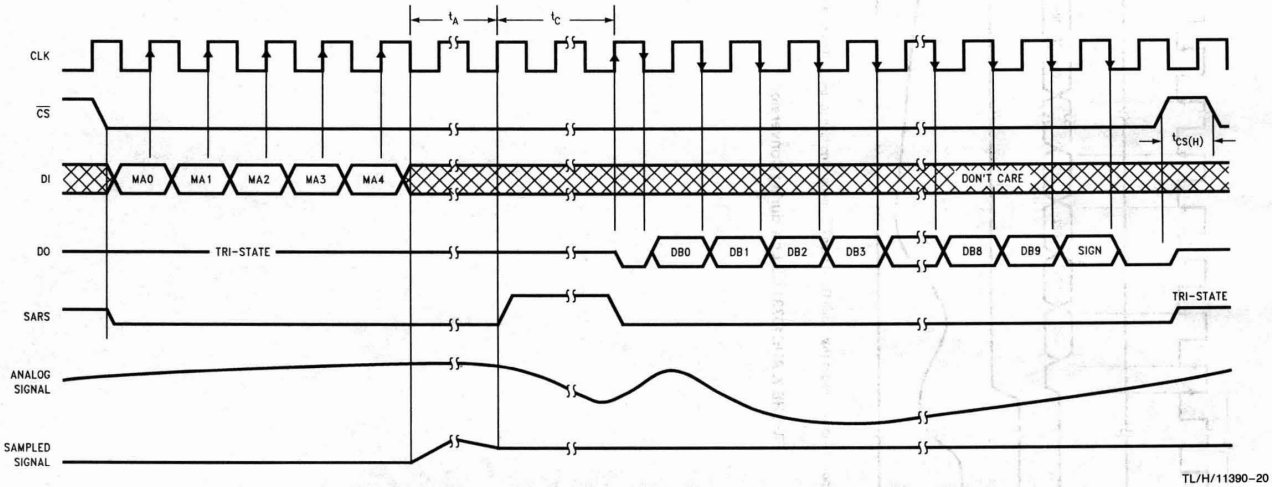

FIGURE 8. ADC10732, ADC10734 and ADC10738 $\overline{CS}$ Low during Conversion

Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

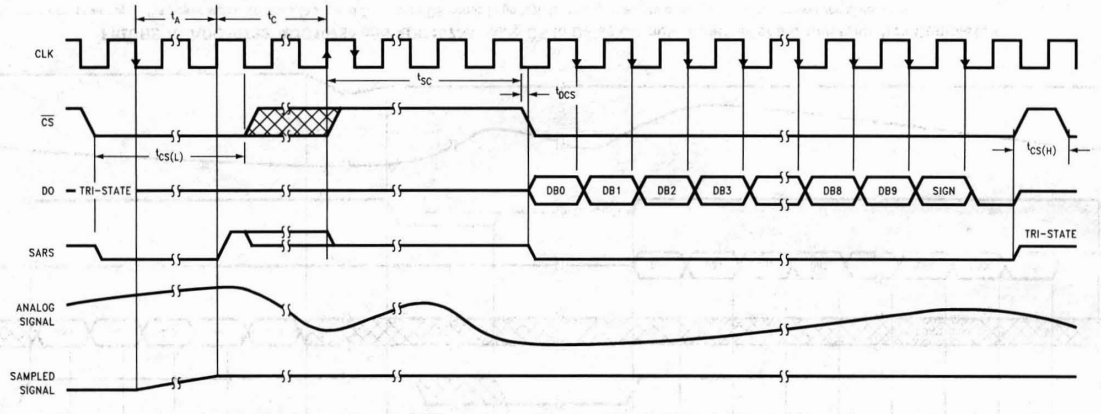

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FIGURE 9. ADC10731 Using $\overline{CS}$ to Delay Output of Data afer a Conversion has Completed

Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

Timing Diagrams (Continued)

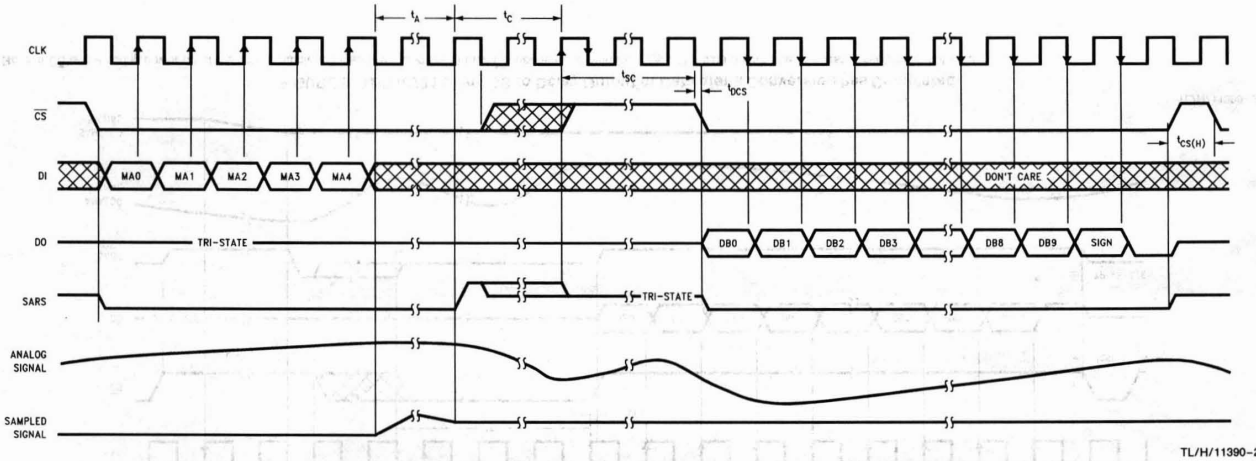

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FIGURE 10. ADC10732, ADC10734 and ADC10738 Using $\overline{CS}$ to Delay Output of Data after a Conversion has Completed

Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

TABLE I. ADC10738 Multiplexer Address Assignment

MUX Address					Channel Number								MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0										
1	1	0	0	0	+								−	Single-Ended
1	1	0	0	1			+						−	
1	1	0	1	0					+				−	
1	1	0	1	1							+		−	
1	1	1	0	0		+							−	
1	1	1	0	1				+					−	
1	1	1	1	0						+			−	
1	1	1	1	1								+	−	
1	0	0	0	0	+	−								Differential
1	0	0	0	1			+	−						
1	0	0	1	0					+	−				
1	0	0	1	1							+	−		
1	0	1	0	0	−	+								
1	0	1	0	1			−	+						
1	0	1	1	0					−	+				
1	0	1	1	1							−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)									

TABLE II. ADC10734 Multiplexer Address Assignment

MUX Address					Channel Number					MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	CH2	CH3	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0						
1	1	0	0	0	+				−	Single-Ended
1	1	0	0	1			+		−	
1	1	1	0	0		+			−	
1	1	1	0	1				+	−	
1	0	0	0	0	+	−				Differential
1	0	0	0	1			+	−		
1	0	1	0	0	−	+				
1	0	1	0	1			−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)					

TABLE III. ADC10732 Multiplexer Address Assignment

MUX Address					Channel Number			MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0				
1	1	0	0	0	+		−	Single-Ended
1	1	1	0	0		+	−	
1	0	0	0	0	+	−		Differential
1	0	1	0	0	−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)			

2

Pin Descriptions

CLK — The clock applied to this input controls the successive approximation conversion time interval, the acquisition time and the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address shift register. This address controls which channel of the analog input multiplexer (MUX) is selected. The falling edge shifts the data resulting from the A/D conversion out on DO. $\overline{CS}$ enables or disables the above functions. The clock frequency applied to this input can be between 5 kHz and 3 MHz.

DI — This is the serial data input pin. The data applied to this pln is shifted by CLK into the multiplexer address register. Tables I through III show the multiplexer address assignment.

DO — The data output pin. The A/D conversion result (DB0-SIGN) are clocked out by the failing edge of CLK on this pin.

$\overline{CS}$ — This is the chip select input pin. When a logic low is applied to this pin, the rising edge of CLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE after a conversion has been completed.

PD — This is the power down input pin. When a logic high is applied to this pin the A/D is powered down. When a low is applied the A/D is powered up.

SARS — This is the successive approximation register status output pin. When $\overline{CS}$ is high this pin is in TRI-STATE. With $\overline{CS}$ low this pin is active high when a conversion is in progress and active low at all other times.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of CLK into the address register (see Tables I–III).

The voltage applied to these inputs should not exceed AV^+ or go below GND by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input pln. It can be used as a "pseudo ground" when the analog multiplexer is single-ended.

V_{REF}^+ — This is the positive analog voltage reference input. In order to malntaln accuracy, the voltage range V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) is 0.5 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF}^+ cannot exceed $AV^+ + 50$ mV.

V_{REF}^- — The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND − 50 mV or exceed $AV^+ + 50$ mV.

AV^+, DV^+ — These are the analog and digital power supply pins. These pins should be tied to the same power supply and bypassed separately. The operating voltage range of AV^+ and DV^+ is 4.5 V_{DC} to 5.5 V_{DC}.

DGND — This is the digital ground pin.

AGND — This is the analog ground pin.

Applications Hints

The ADC10731/2/4/8 use successive approximation to digitize an analog input voltage. The DAC portion of the A/D converters uses a capacitive array and a resistive ladder structure. The structure of the DAC allows a very simple switching scheme to provide a versatile analog input multiplexer. This structure also provides a sample/hold. The ADC10731/2/4/8 have a 2.5V CMOS bandgap reference. The serial digital I/O interfaces to MICROWIRE and MICROWIRE+.

1.0 DIGITAL INTERFACE

There are two modes of operation. The fastest throughput rate is obtained when $\overline{CS}$ is kept low during a conversion. The timing diagrams in *Figures 7* and *8* show the operation of the devices in this mode. $\overline{CS}$ must be taken high for at least $t_{CS(H)}$ (1 CLK) between conversions. This is necessary to reset the internal logic. *Figures 9* and *10* show the operation of the devices when $\overline{CS}$ is taken high while the ADC10731/2/4/8 is converting. $\overline{CS}$ may be taken high during the conversion and kept high indefinitely to delay the output data. This mode simplifies the interface to other devices while the ADC10731/2/4/8 is busy converting.

1.1 Getting Started with a Conversion

The ADC10731/2/4/8 need to be initialized after the power supply voltage is applied. If $\overline{CS}$ is low when the supply voltage is applied then $\overline{CS}$ needs to be taken high for at least $t_{CS(H)}$ (1 clock period). The data output after the first conversion is not valid.

1.2 Software and Hardware Power Up/Down

These devices have the capability of software or hardware power down. *Figures 5* and *6* show the timing diagrams for hardware and software power up/down. In the case of hardware power down note that $\overline{CS}$ needs to be high for t_{PC} after PD is taken low. When PD is high the device is powered down. The total quiescent current, when powered down, is typically 200 μA with the clock at 2.5 MHz and 3 μA with the clock off. The actual voltage level applied to a digital input will effect the power consumption of the device during power down. CMOS logic levels will give the least amount of current drain (3 μA). TTL logic levels will increase the total current drain to 200 μA.

These devices have resistive reference ladders which draw 600 μA with a 2.5V reference voltage. The internal band gap reference voltage shuts down when power down is activated. If an external reference voltage is used, it will have to be shut down to minimize the total current drain of the device.

2.0 ARCHITECTURE

Before a conversion is started, during the analog input sampling period, (t_A), the sampled data comparator is zeroed. As the comparator is being zeroed the channel assigned to be the positive input is connected to the A/D's input capacitor. (The assignment procedure is explained in the Pin Descriptions section.) This charges the input 32C capacitor of the DAC to the positive analog input voltage. The switches shown in the DAC portion of *Figure 11* are set for this zeroing/acquisition period. The voltage at the input and output of the comparator are at equilibrium at this time. When the conversion is started, the comparator feedback switches are opened and the 32C input capacitor is then switched to the assigned negative input voltage. When the comparator feedback switch opens, a fixed amount of charge is trapped on the common plates of the capacitors. The voltage at the input of the comparator moves away from equilibrium when the 32C capacitor is switched to the assigned negative input voltage, causing the output of the comparator to go high ("1") or low ("0"). The SAR next goes through an algorithm, controlled by the output state of the comparator, that redistributes the charge on the capacitor array by switching the voltage on one side of the capacitors in the array. The objective of the SAR algorithm is to return the voltage at the input of the comparator as close as possible to equilibrium.

The switch position information at the completion of the successive approximation routine is a direct representation of the digital output. This data is then available to be shifted on the DO pin.

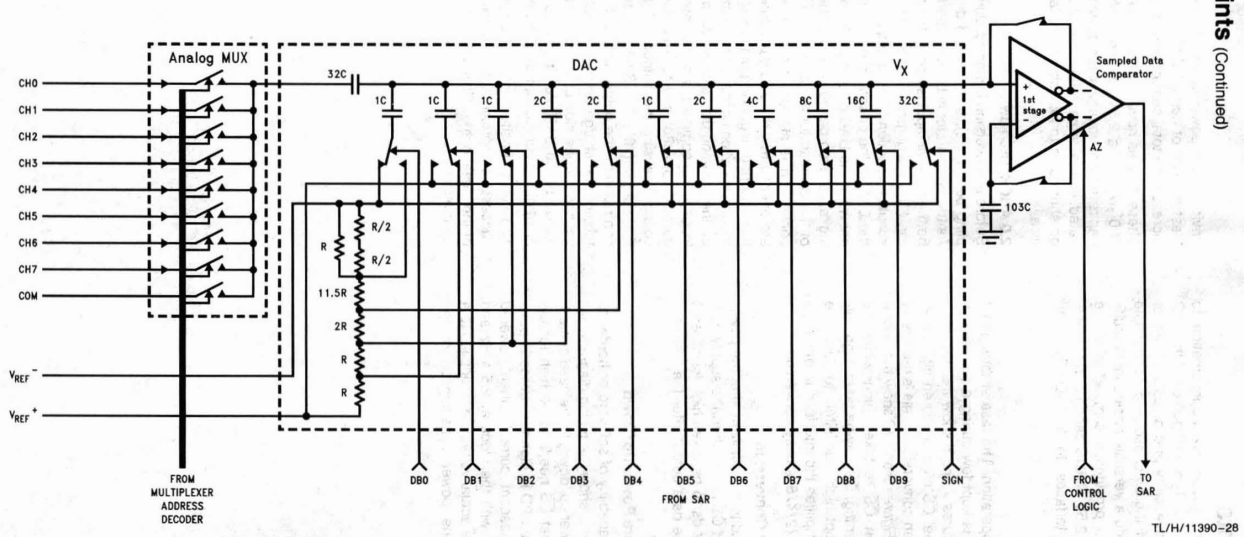

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FIGURE 11. Detailed Diagram of the ADC10738 DAC and Analog Multiplexer Stages

Applications Hints (Continued)

3.0 APPLICATIONS INFORMATION

3.1 Multiplexer Configuration

The design of these converters utilizes a sampled-data comparator structure, which allows a differential analog input to be converted by the successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal or pair of input terminals being converted indicates which line the converter expects to be the most positive.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-ended, or pseudo-differential. *Figure 12* illustrates the three modes using the 4-channel MUX of the ADC10734. The eight inputs of the ADC10738 can also be configured in any of the three modes. The single-ended mode has CH0–CH3 assigned as the positive input with COM serving as the negative input. In the differential mode, the ADC10734 channel inputs are grouped in pairs, CH0 with CH1 and CH2 with CH3. The polarity assignment of each channel in the pair is interchangeable. Finally, in the pseudo-differential mode CH0–CH3 are positive inputs referred to COM which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground-referred inputs and true differential inputs as well as signals referred to a specific voltage.

The analog input voltages for each channel can range from 50 mV below GND to 50 mV above $V^+ = DV^+ = AV^+$ without degrading conversion accuracy. If the voltage on an unselected channel exceeds these limits it may corrupt the reading of the selected channel.

3.2 Reference Considerations

The voltage difference between the V_{REF}^+ and V_{REF}^- inputs defines the analog input voltage span (the difference between V_{IN}(Max) and V_{IN}(Min)) over which 1023 positive and 1024 negative possible output codes apply.

The value of the voltage on the V_{REF}^+ or V_{REF}^- inputs can be anywhere between $AV^+ + 50$ mV and -50 mV, so long as V_{REF}^+ is greater than V_{REF}^-. The ADC10731/2/4/8 can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the minimum reference input resistance of 5 kΩ.

The internal 2.5V bandgap reference in the ADC10731/2/4/8 is available as an output on the V_{REF}Out pin. To ensure optimum performance this output needs to be bypassed to ground with 100 μF aluminum electrolytic or tantalum capacitor. The reference output can be unstable with capacitive loads greater than 100 pF and less than 100 μF. Any capacitive loading less than 100 pF and greater than 100 μF will not cause oscillation. Lower output noise can be obtained by increasing the output capacitance. A 100 μF capacitor will yield a typical noise floor of 200 nV/$\sqrt{\text{Hz}}$. The pseudo-differential and differential multiplexer modes allow for more flexibility in the analog input voltage range since the "zero" reference voltage is set by the actual voltage applied to the assigned negative input pin.

In a ratiometric system *(Figure 13a)*, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage may also be the system power supply, so V_{REF}^+ can also be tied to AV^+. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy *(Figure 13b)*, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time- and temperature-stable voltage source that has excellent initial accuracy. The LM4040, LM4041 and LM185 references are suitable for use with the ADC10731/2/4/8.

The minimum value of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) can be quite small (see Typical Performance Characteristics) to allow direct conversion of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/1024).

3.3 The Analog Inputs

Due to the sampling nature of the analog inputs, at the clock edges short duration spikes of current will be seen on the selected assigned negative input. Input bypass capacitors should not be used if the source resistance is greater than 1 kΩ since they will average the AC current and cause an effective DC current to flow through the analog input source resistance. An op amp RC active lowpass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required. Bypass capacitors may be used when the source impedance is very low without any degradation in performance.

In a true differential input stage, a signal that is common to both "+" and "−" inputs is canceled. For the ADC10731/2/4/8, the positive input of a selected channel pair is only sampled once before the start of a conversion during the acquisition time (t_A). The negative input needs to be stable during the complete conversion sequence because it is sampled before each decision in the SAR sequence. Therefore, any AC common-mode signal present on the analog inputs will not be completely canceled and will cause some conversion errors. For a sinusoid common-mode signal this error is:

$$V_{ERROR}(\text{max}) = V_{PEAK} (2 \pi f_{CM}) (t_C)$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value, and t_C is the A/D's conversion time ($t_C = 12/f_{CLK}$). For example, for a 60 Hz common-mode signal to generate a ¼ LSB error (0.61 mV) with a 4.8 μs conversion time, its peak value would have to be approximately 337 mV.

Applications Hints (Continued)

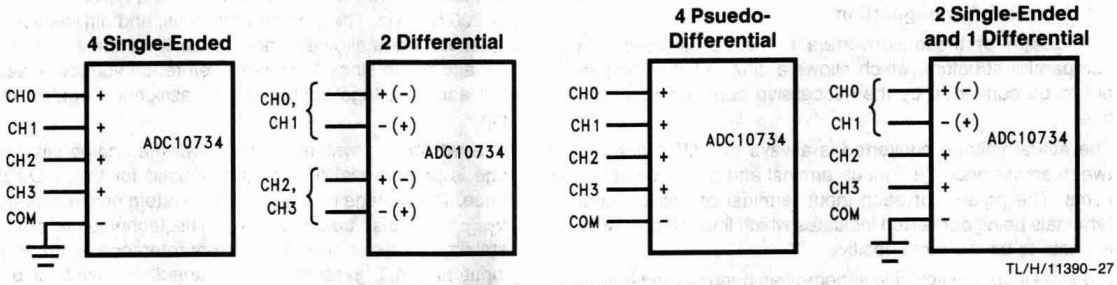
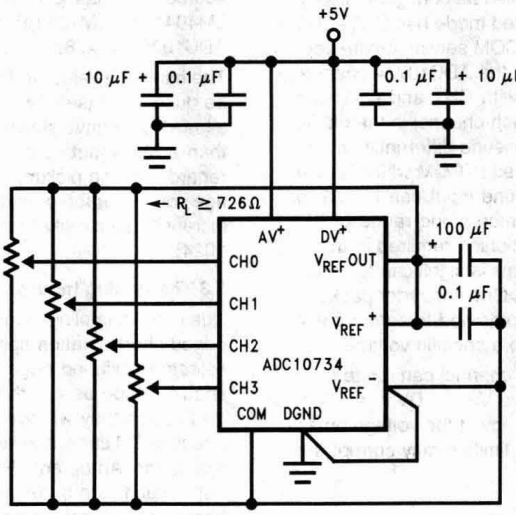


FIGURE 12. Analog Input Multiplexer Options

a. Ratiometric Using the Internal Reference



b. Absolute Using a 4.096V Span

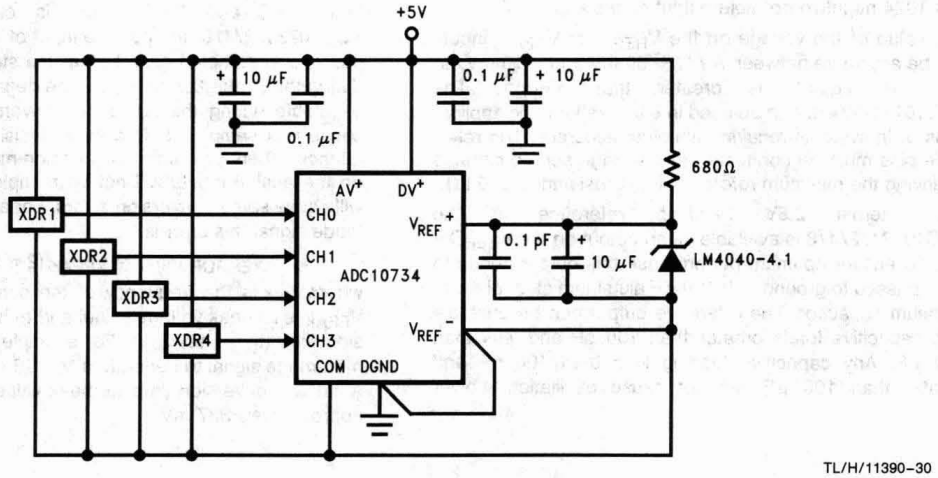


FIGURE 13. Different Reference Configurations

Applications Hints (Continued)

3.4 Optional Adjustments

3.4.1 Zero Error

The zero error of the A/D converter relates to the location of the first riser of the transfer function (see *Figure 1*) and can be measured by grounding the minus input and applying a small magnitude voltage to the plus input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 000 0000 0000 to 000 0000 0001 and the ideal ½ LSB value (½ LSB = 1.22 mV for V_{REF} = + 2.500V).

The zero error of the A/D does not require adjustment. If the minimum analog input voltage value, V_{IN}(Min), is not ground, the effective "zero" voltage can be adjusted to a convenient value. The converter can be made to output an all zeros digital code for this minimum input voltage by biasing any minus input to V_{IN}(Min). This is useful for either the differential or pseudo-differential input channel configurations.

3.4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the V_{REF} voltage ($V_{REF} = V_{REF}^+ - V_{REF}^-$) for a digital output code changing from 011 1111 1110 to 011 1111 1111. In bipolar signed operation this only adjusts the positive full scale error.

3.4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A plus input voltage which equals this desired zero reference plus ½ LSB is applied to selected plus input and the zero reference voltage at the corresponding minus input should then be adjusted to just obtain the 000 0000 0000 to 000 0000 0001 code transition.

The full-scale adjustment should be made [with the proper minus input voltage applied] by forcing a voltage to the plus input which is given by:

$$V_{IN}(+)\, f_s\, adj = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{2^n} \right]$$

where V_{MAX} equals the high end of the analog input range, V_{MIN} equals the low end (the offset zero) of the analog range. Both V_{MAX} and V_{MIN} are ground referred. The V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) voltage is then adjusted to provide a code change from 011 1111 1110 to 011 1111 1111. Note, when using a pseudo-differential or differential multiplexer mode where V_{REF}^+ and V_{REF}^- are placed within the V^+ and GND range, the individual values of V_{REF} and V_{REF}^- do not matter, only the difference sets the analog input voltage span. This completes the adjustment procedure.

3.5 The Input Sample and Hold

The ADC10731/2/4/8's sample/hold capacitor is implemented in the capacitor array. After the channel address is loaded, the array is switched to sample the selected positive analog input. The sampling period for the assigned positive input is maintained for the duration of the acquisition time (t_A) 4.5 clock cycles.

This acquisition window of 4.5 clock cycles is available to allow the voltage on the capacitor array to settle to the positive analog input voltage. Any change in the analog voltage on a selected positive input before or after the acquisition window will not effect the A/D conversion result.

In the simplest case, the array's acquisition time is determined by the R_{ON} (3 kΩ) of the multiplexer switches, the stray input capacitance C_{S1} (3.5 pF) and the total array (C_L) and stray (C_{S2}) capacitance (48 pF). For a large source resistance the analog input can be modeled as an RC network as shown in *Figure 14*. The values shown yield an acquisition time of about 1.1 μs for 10-bit unipolar or 10-bit plus sign accuracy with a zero-to-full-scale change in the input voltage. External source resistance and capacitance will lengthen the acquisition time and should be accounted for. Slowing the clock will lengthen the acquisition time, thereby allowing a larger external source resistance.

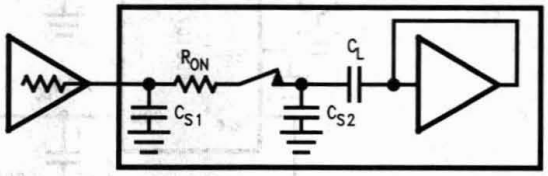


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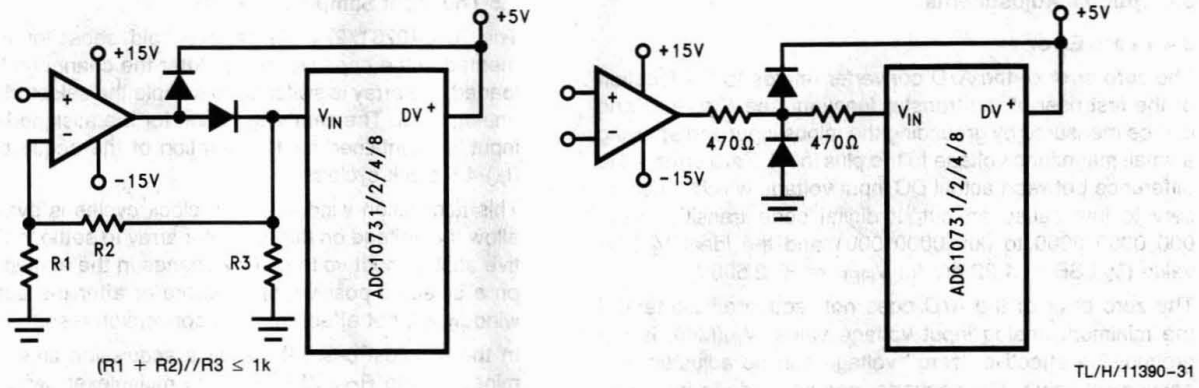
FIGURE 14. Analog Input Model

The signal-to-noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the ideal A/D. An ideal 10-bit plus sign A/D converter with a total unadjusted error of 0 LSB would have a signal-to-(noise + distortion) ratio of about 68 dB, which can be derived from the equation:

$$S/(N + D) = 6.02(n) + 1.8$$

where S/(N + D) is in dB and n is the number of bits.

Applications Hints (Continued)



Note 1: Diodes are 1N914.

Note 2: The protection diodes should be able to withstand the output current of the op amp under current limit.

FIGURE 15. Protecting the Analog Inputs

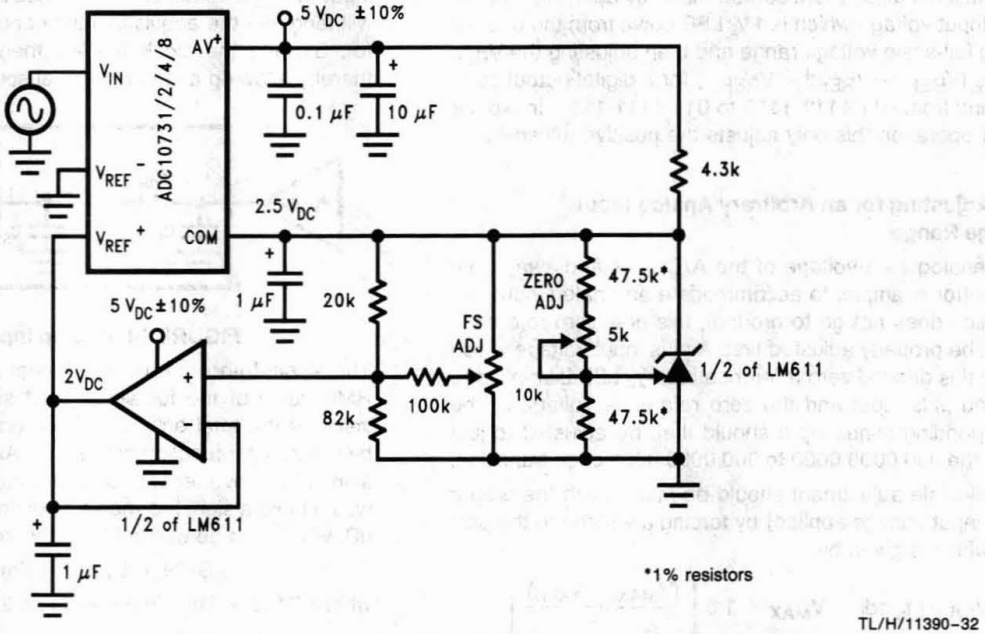


FIGURE 16. Zero-Shift and Span-Adjust for Signed or Unsigned, Single-Ended Multiplexer Assignment, Signed Analog Input Range of 0.5V ≤ V_{IN} ≤ 4.5V

National Semiconductor

ADC10831, ADC10832, ADC10834, ADC10838 10-Bit Plus Sign Serial I/O A/D Converters with MUX, Sample/Hold and Reference

General Description

This series of CMOS 10-bit plus sign successive approximation A/D converters features versatile analog input multiplexers, sample/hold and a 2.5V band-gap reference. The 1, 2, 4 or 8-channel multiplexers can be software configured for single-ended or differential mode of operation.

An input sample/hold is implemented by a capacitive reference ladder and sampled-data comparator. This allows the analog input to vary during the A/D conversion cycle.

In the differential mode, valid outputs are obtained even when the negative inputs are greater than the positive because of the 10-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC™ families of controllers, and can easily interface with standard shift registers and microprocessors.

Applications

- Medical instruments
- Remote instrumentation
- Test equipment

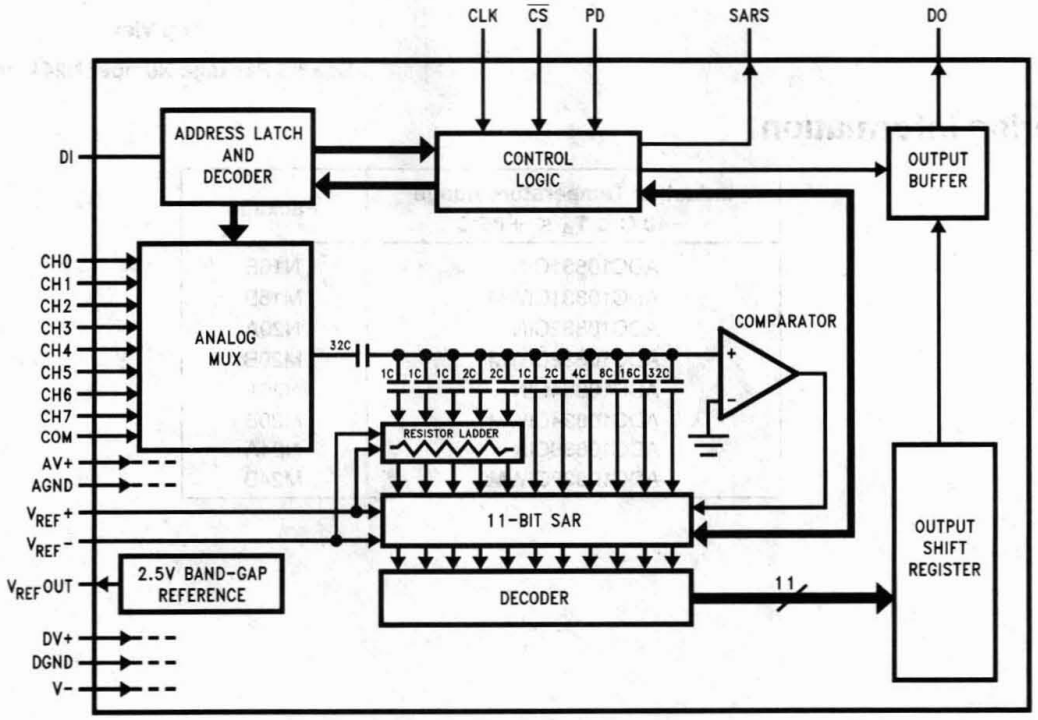
Features

- −5V to +5V analog voltage range with ±5V supplies
- Serial I/O (MICROWIRE compatible)
- 1, 2, 4, or 8-channel differential or single-ended multiplexer
- Software or hardware power down
- Analog input sample/hold function
- Ratiometric or Absolute voltage referencing
- No zero or full scale adjustment required
- No missing codes over temperature
- TTL/MOS input/output compatible
- Standard DIP and SO packages

Key Specifications

■ Resolution	10 bits plus sign
■ Dual supply	±5V
■ Power dissipation	59 mW (Max)
■ In power down mode	33 μW
■ Conversion time	5 μs (Max)
■ Sampling rate	74 kHz (Max)
■ Band-gap reference	2.5V ±2% (Max)

ADC10838 Simplified Block Diagram



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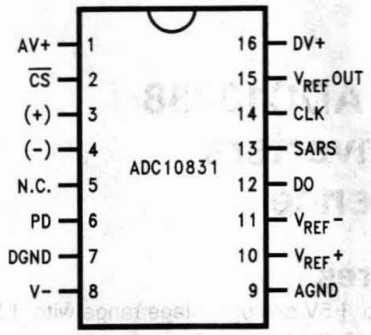
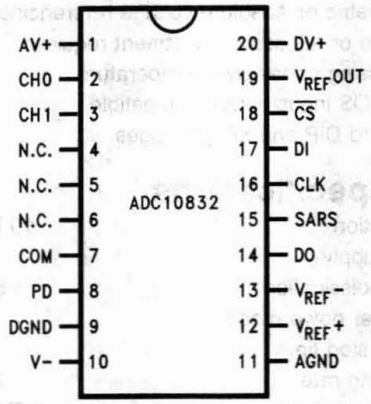
Connection Diagrams for Dual-In-Line and SO Packages



TL/H/11391-2

Top View

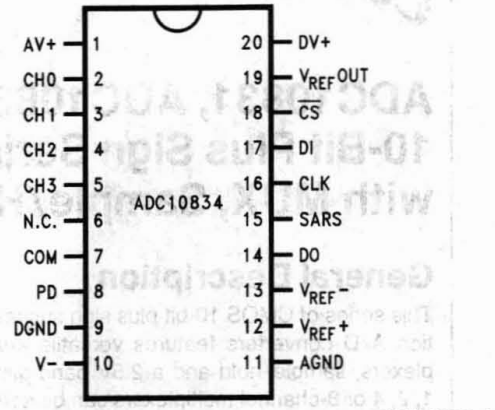
See NS Package Number N16E or M16B



TL/H/11391-3

Top View

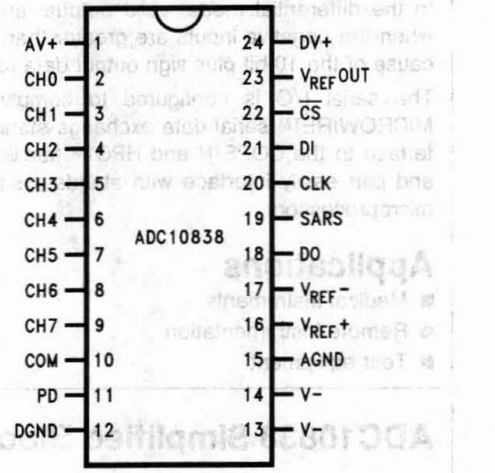
See NS Package Number N20A or M20B



TL/H/11391-4

Top View

See NS Package Number N20A or M20B



TL/H/11391-5

Top View

See NS Package Number N24A or M24B

Ordering Information

Industrial Temperature Range $-40°C \leq T_A \leq +85°C$	Package
ADC10831CIN	N16E
ADC10831CIWM	M16B
ADC10832CIN	N20A
ADC10832CIWM	M20B
ADC10834CIN	N20A
ADC10834CIWM	M20B
ADC10838CIN	N24A
ADC10838CIWM	M24B

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage ($V^+ = AV^+ = DV^+$)	+6.0V
Negative Supply Voltage (V^-)	−6.0V
Total Supply Voltage ($V^+ - V^-$)	12V
Total Reference Voltage ($V_{REF}^+ - V_{REF}^-$)	+6.0V
Voltage at Analog Inputs (CH0-CH7 and COM)	$V^+ + 0.3V$ to $V^- - 0.3V$
Voltage at other Inputs and Outputs	$V^+ + 0.3V$ to −0.3V
Input Current at Any Pin (Note 4)	30 mA
Package Input Current (Note 4)	120 mA
Package Dissipation at $T_A = 25°C$ (Note 5)	500 mW
ESD Susceptability (Note 6)	
Human Body Model	2500V
Machine Model	150V
Soldering Information	
N packages (10 seconds)	260°C
SO Package (Note 7)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	−40°C to +150°C

Operating Ratings (Notes 2 and 3)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10831CIN, ADC10831CIWM, ADC10832CIN, ADC10832CIWM, ADC10834CIN, ADC10834CIWM, ADC10838CIN, ADC10838CIWM	$-40°C \le T_A \le +85°C$
Positive Supply Voltage ($V^+ = AV^+ = DV^+$)	+4.5V to +5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
V_{REF}^+	$AV^+ + 50$ mV to −50 mV
V_{REF}^-	$AV^+ + 50$ mV to −50 mV
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	+0.5V to V^+

Electrical Characteristics

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = V_{IN}^- = GND$, $V^- = -5.0V_{DC}$, and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10 + Sign**	Bits
TUE	Total Unadjusted Error (Note 13)			**±2.0**	LSB(max)
INL	Positive and Negative Integral Linearity Error			**±1.25**	LSB(max)
	Positive and Negative Full-Scale Error			**±1.5**	LSB(max)
	Offset Error			**±1.5**	LSB(max)
	Power Supply Sensitivity				
	Offset Error	$V^+ = +5.0V \pm 10\%$	±0.2	**±1.0**	LSB(max)
	+ Full-Scale Error	or $V^- = -5.0 \pm 10\%$	±0.2	**±1.0**	LSB(max)
	− Full-Scale Error		±0.1	**±0.75**	LSB(max)
	DC Common Mode Error (Note 14)	$V_{IN}^+ = V_{IN}^- = V_{IN}$ where $+5.0V \ge V_{IN} \ge -5V$	±0.15	**±0.6**	LSB(max)
	Multiplexer Channel to Channel Matching		±0.1		LSB

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = V_{IN}^- = GND$, $V^- = -5.0\ V_{DC}$, and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10) (Continued)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$V_{IN} = 8.0\ V_{PP}$, Sampling Rate = 74 kHz and f_{IN} = 1 kHz to 15 kHz	67		dB
ENOB	Effective Number of Bits	$V_{IN} = 8.0\ V_{PP}$, Sampling Rate = 74 kHz and f_{IN} = 1 kHz to 15 kHz	10.8		Bits
THD	Total Harmonic Distortion	$V_{IN} = 8.0\ V_{PP}$, Sampling Rate = 74 kHz and f_{IN} = 1 kHz to 15 kHz	−78		dB
IMD	Intermodulation Distortion	$V_{IN} = 8.0\ V_{PP}$, Sampling Rate = 74 kHz and f_{IN} = 1 kHz to 15 kHz	−85		dB
	Full-Power Bandwidth	$V_{IN} = 8.0\ V_{PP}$, where S/(N + D) Decreases 3 dB Sampling Rate = 74 kHz	380		kHz
	Multiplexer Channel to Channel Crosstalk	f_{IN} = 15 kHz Sampling Rate = 74 kHz	−80		dB
REFERENCE INPUT AND MULTIPLEXER CHARACTERISTICS					
	Reference Input Resistance		7	**5.0** **9.5**	kΩ kΩ(min) kΩ(max)
C_{REF}	Reference Input Capacitance		70		pF
	MUX Input Voltage			**V^- −50 mV** **AV^+ +50 mV**	(min) (max)
C_{IM}	MUX Input Capacitance		47		pF
	Off Channel Leakage Current (Note 15)	On Channel = +5V and Off Channel = −5V	−0.4	**−3.0**	µA(max)
		On Channel = −5V and Off Channel = +5V	0.4	**3.0**	µA(max)
	On Channel Leakage Current (Note 15)	On Channel = +5V and Off Channel = +5V	0.4	**3.0**	µA(max)
		On Channel = −5V and Off Channel = +5V	−0.4	**−3.0**	µA(max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = V_{IN}^- = GND$, $V^- = -5.0\ V_{DC}$, and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = +25°C$. (Notes 8, 9 and 10) (Continued)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
REFERENCE CHARACTERISTICS					
$V_{REF}Out$	Reference Output Voltage		2.5V ±0.5%	**2.5V ±2%**	V(max)
$\Delta V_{REF}/\Delta T$	$V_{REF}Out$ Temperature Coefficient		±40		ppm/°C
$\Delta V_{REF}/\Delta I_L$	Load Regulation, Sourcing	0 mA ≤ I_L ≤ +4 mA	±0.003	**±0.05**	%/mA(max)
$\Delta V_{REF}/\Delta I_L$	Load Regulation, Sinking	0 mA ≤ I_L ≤ −1 mA	±0.2	**±0.6**	%/mA(max)
	Line Regulation	5V ±10%	±0.3	**±2.5**	mV(max)
I_{SC}	Short Circuit Current	$V_{REF}Out$ = 0V	13	**22**	mA(max)
	Noise Voltage	10 Hz to 10 kHz, C_L = 100 µF	5		µV
$\Delta V_{REF}/\Delta t$	Long-term Stability		±120		ppm/kHr
t_{SU}	Start-Up Time	C_L = 100 µF	100		ms
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	V^+ = 5.5V		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage	V^+ = 4.5V		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.0V	0.005	**+2.5**	µA(max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−0.005	**−2.5**	µA(min)
$V_{OUT(1)}$	Logical "1" Output Voltage	V^+ = 4.5V, I_{OUT} = −360 µA V^+ = 4.5V, I_{OUT} = −10 µA		**2.4** **4.5**	V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V^+ = 4.5V, I_{OUT} = 1.6 mA		**0.4**	V(min)
I_{OUT}	TRI-STATE Output Current	V_{OUT} = 0V V_{OUT} = 5V	−0.1 +0.1	**−3.0** **+3.0**	µA(min) µA(max)
$+I_{SC}$	Output Short-Circuit Source Current	V_{OUT} = 0V, V^+ = 4.5V	−30	**−15**	mA(max)
$-I_{SC}$	Output Short-Circuit Sink Current	V_{OUT} = V^+ = 4.5V	30	**15**	mA(min)
I_D^+	Digital Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up $\overline{CS}$ = HIGH, Power Down $\overline{CS}$ = HIGH, Power Down, and CLK Off	0.9 0.2 0.5	**1.3** **0.4** **50**	mA(max) mA(max) µA(max)
I_A^+	Positive Analog Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up $\overline{CS}$ = HIGH, Power Down	2.7 3.0	**6.0** **15**	mA(max) µA(max)
I_A^-	Negative Analog Supply Current (Note 17)	$\overline{CS}$ = HIGH, Power Up $\overline{CS}$ = HIGH, Power Down	−2.7 −3.0	−4.5 −15	mA(min) µA(min)
I_{REF}	Reference Input Current	V_{REF}^+ = +2.5V and $\overline{CS}$ = HIGH, Power Up		**0.6**	mA(max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = AV^+ = DV^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = V_{IN} = GND$, $V^- = -5.0\ V_{DC}$, and $f_{CLK} = 2.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$. (Note 16)

Symbol	Parameter	Conditions	Typical (Note 11)	Limits (Note 12)	Units (Limits)
AC CHARACTERISTICS					
f_{CLK}	Clock Frequency		3.0 5	**2.5**	MHz(max) kHz(min)
	Clock Duty Cycle			**40** **60**	%(min) %(max)
t_C	Conversion Time		12 5	**12** **5**	Clock Cycles μs(max)
t_A	Acquisition Time		4.5 2	**4.5** **2**	Clock Cycles μs(max)
t_{SCS}	$\overline{CS}$ Set-Up Time, Set-Up Time from Falling Edge of CS to Rising Edge of Clock		14 (1 t_{CLK} − 14 ns)	**30** **(1 t_{CLK} −30 ns)**	ns(min) (max)
t_{SDI}	DI Set-Up Time, Set-Up Time from Data Valid on DI to Rising Edge of Clock		16	**25**	ns(min)
t_{HDI}	DI Hold Time, Hold Time of DI Data from Rising Edge of Clock to Data not Valid on DI		2	**25**	ns(min)
t_{AT}	DO Access Time from Rising Edge of CLK When $\overline{CS}$ is "Low" during a Conversion		30	**50**	ns(min)
t_{AC}	DO or SARS Access Time from $\overline{CS}$, Delay from Falling Edge of $\overline{CS}$ to Data Valid on DO or SARS		30	**70**	ns(max)
t_{DSARS}	Delay from Rising Edge of Clock to Falling Edge of SARS when $\overline{CS}$ is "Low"		100	**200**	ns(max)
t_{HDO}	DO Hold Time, Hold Time of Data on DO after Falling Edge of Clock		20	**45**	ns(max)
t_{AD}	DO Access Time from Clock, Delay from Falling Edge of Clock to Valid Data of DO		40	**80**	ns(max)
t_{1H}, t_{0H}	Delay from Rising Edge of $\overline{CS}$ to DO or SARS TRI-STATE		40	**50**	ns(max)
t_{DCS}	Delay from Falling Edge of Clock to Falling Edge of $\overline{CS}$		20	**30**	ns(min)
$t_{CS(H)}$	$\overline{CS}$ "HIGH" Time for A/D Reset after Reading of Conversion Result		1 CLK	**1 CLK**	cycle(min)
$t_{CS(L)}$	ADC10731 Minimum $\overline{CS}$ "Low" Time to Start a Conversion		1 CLK	**1 CLK**	cycle(min)
t_{SC}	Time from End of Conversion to $\overline{CS}$ Going "Low"		5 CLK	**5 CLK**	cycle(min)
t_{PD}	Delay from Power-Down command to 10% of Operating Current		1		μs
t_{PC}	Delay from Power-Up Command to Ready to Start a New Conversion		10		μs
C_{IN}	Capacitance of Logic Inputs		7		pF
C_{OUT}	Capacitance of Logic Outputs		12		pF

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifcations and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > AV^+$ or DV^+), the current at that pln should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.

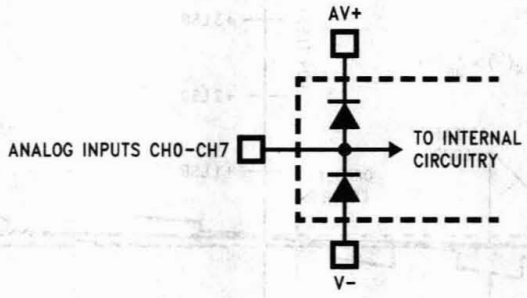
Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given In the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$. The typical thermal resistance (θ_{JA}) of these Paris when board mounted can be found in the following table:

Part Number	Thermal Resistance	Package Type
ADC10831CIN	82°C/W	N16E
ADC10831CIWM	90°C/W	M16B
ADC10832CIN	47°C/W	N20A
ADC10832CIWM	80°C/W	M20B
ADC10834CIN	47°C/W	N20A
ADC10834CIWM	80°C/W	M20B
ADC10838CIN	60°C/W	N24A
ADC10838CIWM	75°C/W	M24B

Note 6: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 7: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titied "Surtace Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surtace mount devices.

Note 8: Two on-ohip diodes are tied to each analog input as shown below. They will forward-conduct for analog input voltages one diode drop below V^- or one diode drop greater than V^+ supply. Be careful during testing at low V^+ and V^- levels ($\pm 4.5V$), as high level analog inputs ($\pm 5V$) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors In the conversion result. The specification allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be oorrect. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. If AV^+ and DV^+ are minimum (4.5 V_{DC}) and V^- is a maximum (-4.5 V_{DC}) full scale must be $\leq \pm 4.55$ V_{DC}.



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Note 9: No connection exists between AV^+ and DV^+ on the chip.

To guarantee accuracy, it is required that the AV^+ and DV^+ be connected together to a power supply with separate bypass filter at eacn V^+ pin.

Note 10: One LSB is referenced to 10 bits of resolution.

Note 11: Typicals are at $T_J = T_A = 25°C$ and represent most likely pararmetric norm.

Note 12: Tested limits are guaranteed to National's AOQL (Average Outgolng Quality Level).

Note 13: Total unadjusted error includes offset, full-scale, linearity, multiplexer, and hold step errors.

Note 14: The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.

Note 15: Channel leakage current is measured after the channel selection.

Note 16: All the timing specifications are tested at the TTL logic levels, $V_{IL} = 0.8V$ for a falling edge and $V_{IH} = 2.0V$ for a rising. TRI-STATE voltage level is forced to 1.4V.

Note 17: The voltage applied to the digital inputs will affect the current drain during power down. These devices are tested with CMOS logic levels (logic Low = 0V and logic High = 5V). TTL levels increase the power down current to about 300 μA.

Electrical Characteristics (Continued)

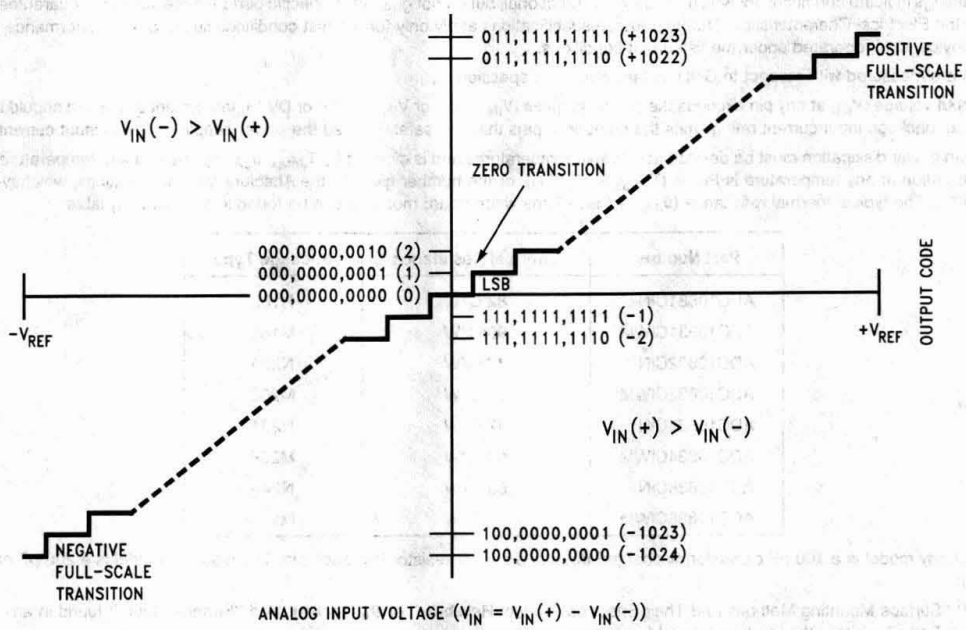

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FIGURE 1A. Transfer Characteristic

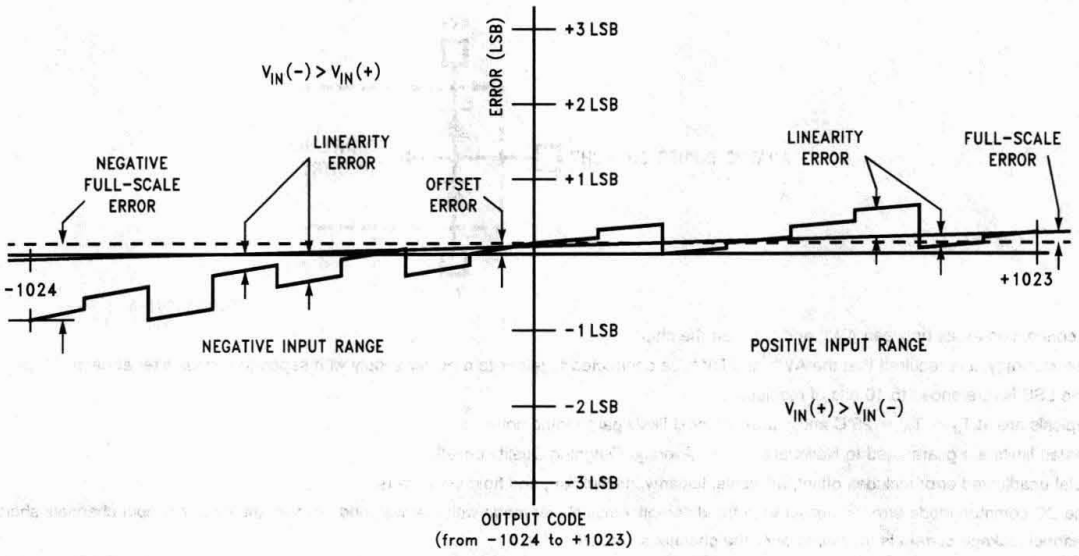

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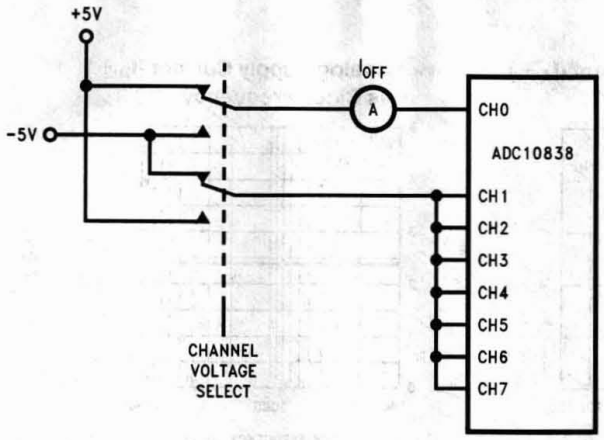
FIGURE 1B. Simplified Error Curve vs Output Code

Leakage Current Test Circuit



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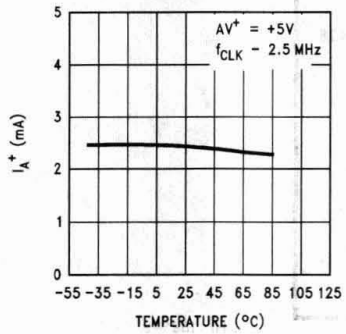
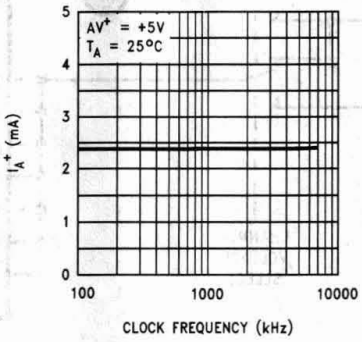
Typical Performance Characteristics

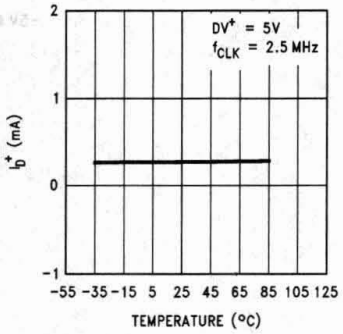
Analog Supply Current (I_A+) vs Temperature



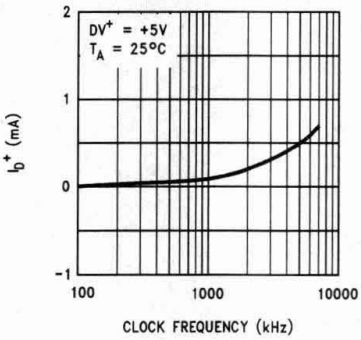
Analog Supply Current (I_A+) vs Clock Frequency



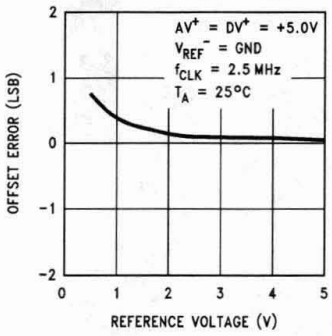
Digital Supply Current (I_D+) vs Temperature



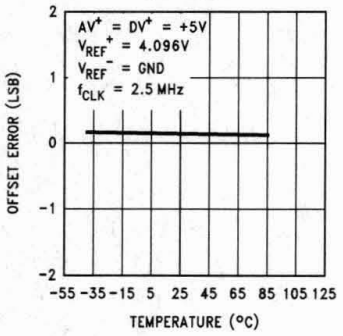
Digital Supply Current (I_D+) vs Clock Frequency



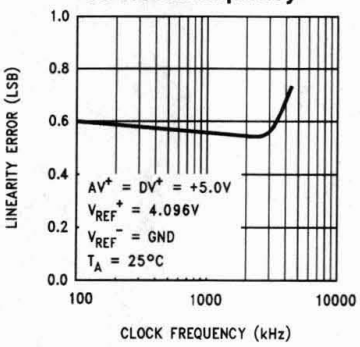
Offset Error vs Reference Voltage



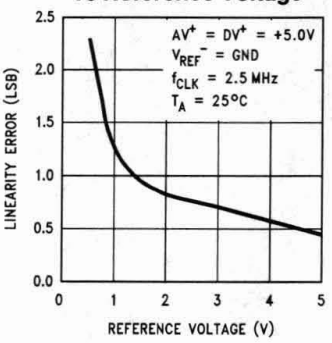
Offset Error vs Temperature



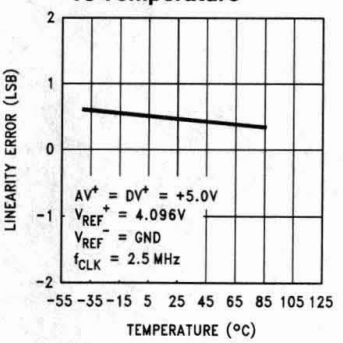
Linearity Error vs Clock Frequency



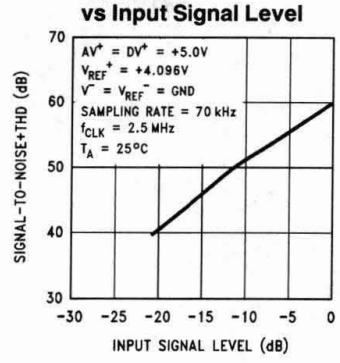
Linearity Error vs Reference Voltage



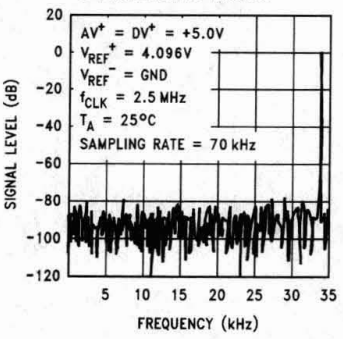
Linearity Error vs Temperature



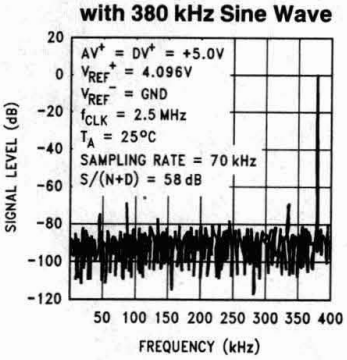
10-Bit Unsigned Signal-to-Noise + THD Ratio vs Input Signal Level



Spectral Response with 34 kHz Sine Wave



Power Bandwidth Response with 380 kHz Sine Wave



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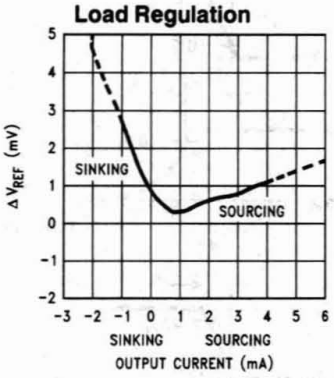
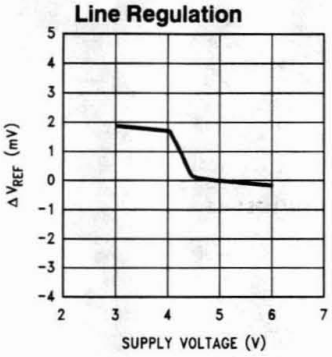
Typical Reference Performance Characteristics

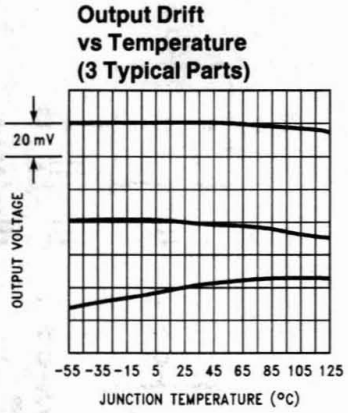
Load Regulation



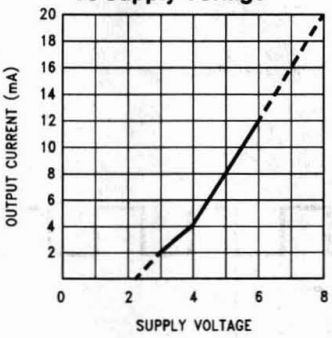
Line Regulation



Output Drift vs Temperature (3 Typical Parts)



Available Output Current vs Supply Voltage



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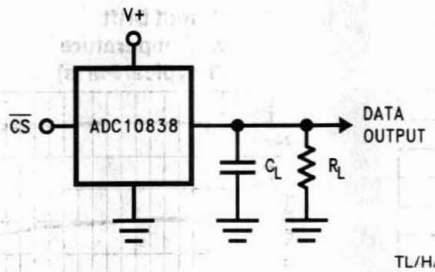
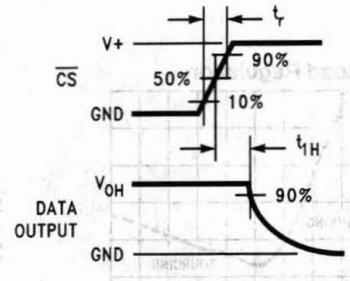
2

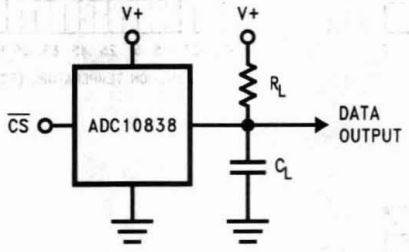
TRI-STATE Test Circuits and Waveforms



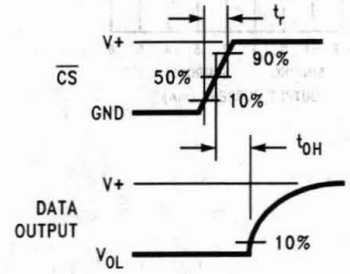
TL/H/11391–12



TL/H/11391–13



TL/H/11391–14



TL/H/11391–15

Timing Diagrams

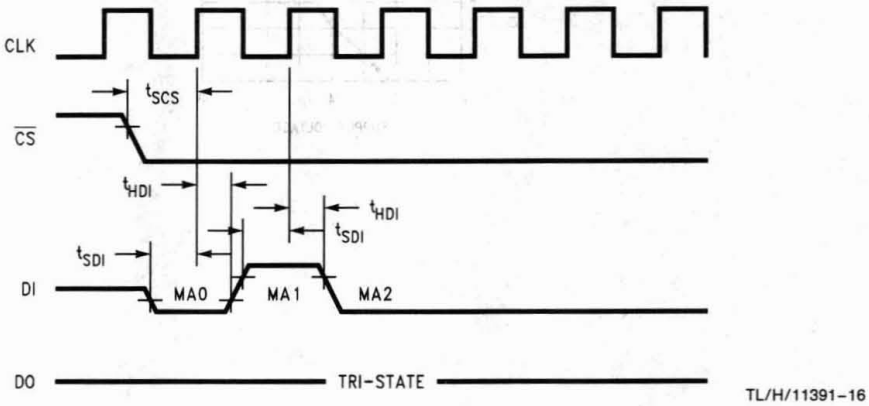


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FIGURE 2. DI Timing

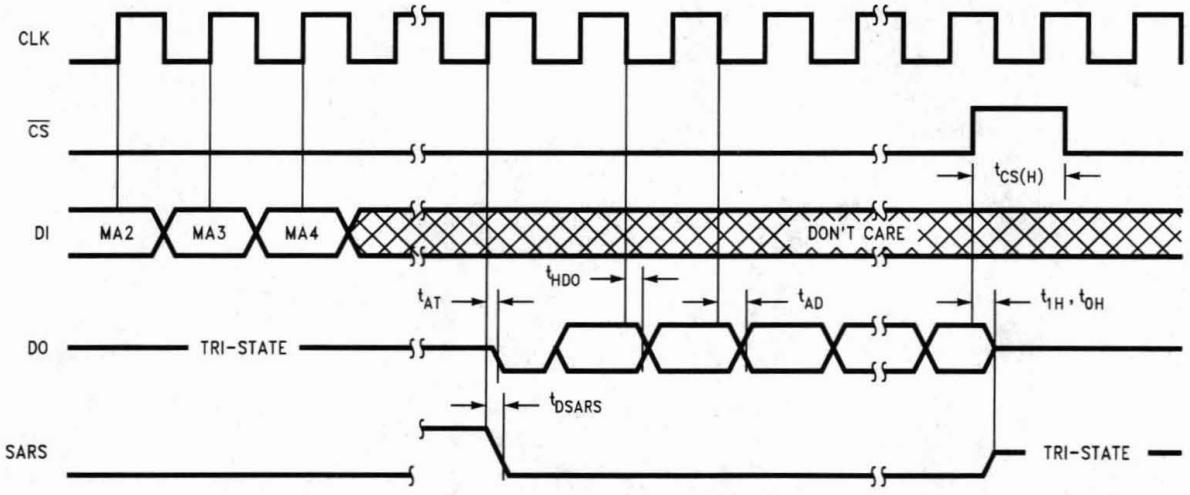

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FIGURE 3. DO Timing

Timing Diagrams (Continued)

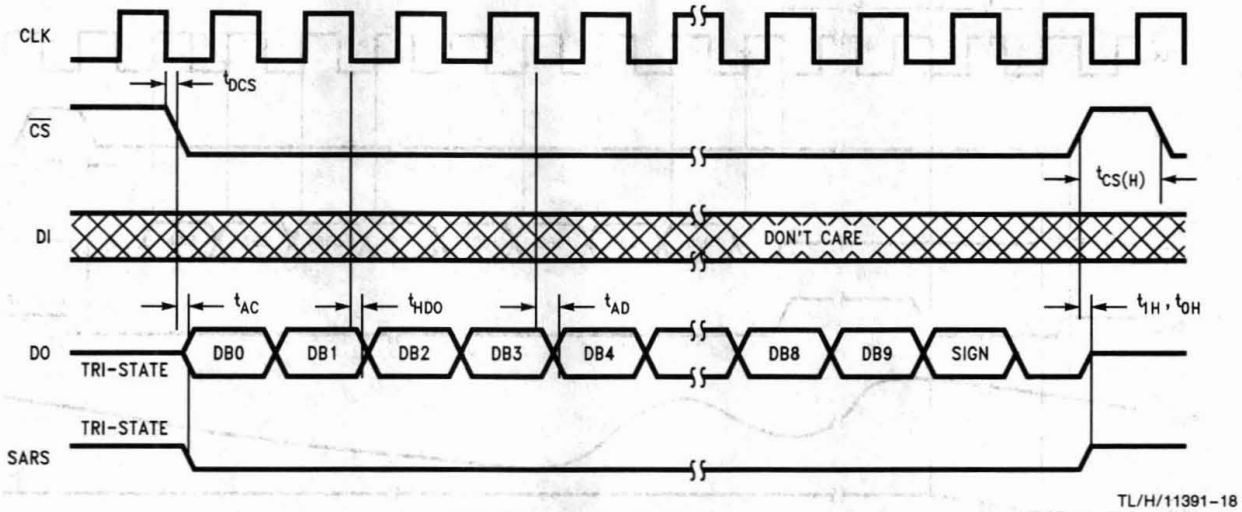

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FIGURE 4. Delayed DO Timing

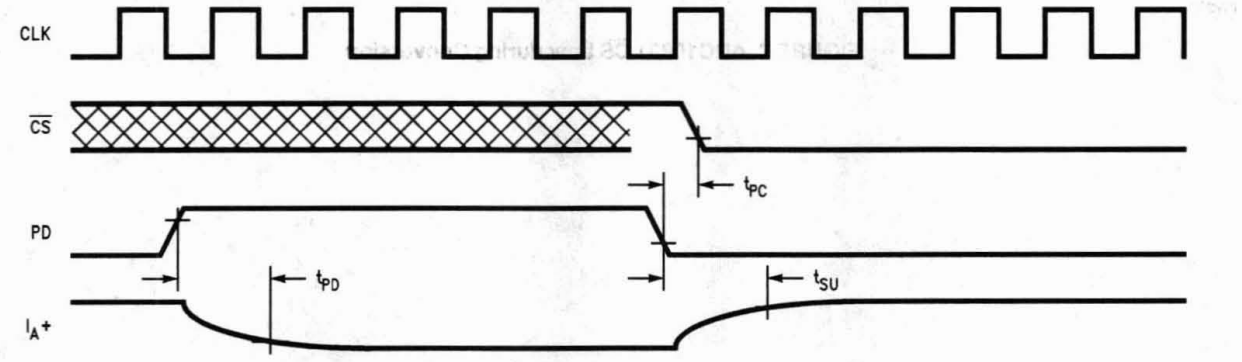

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FIGURE 5. Hardware Power Up/Down Sequence

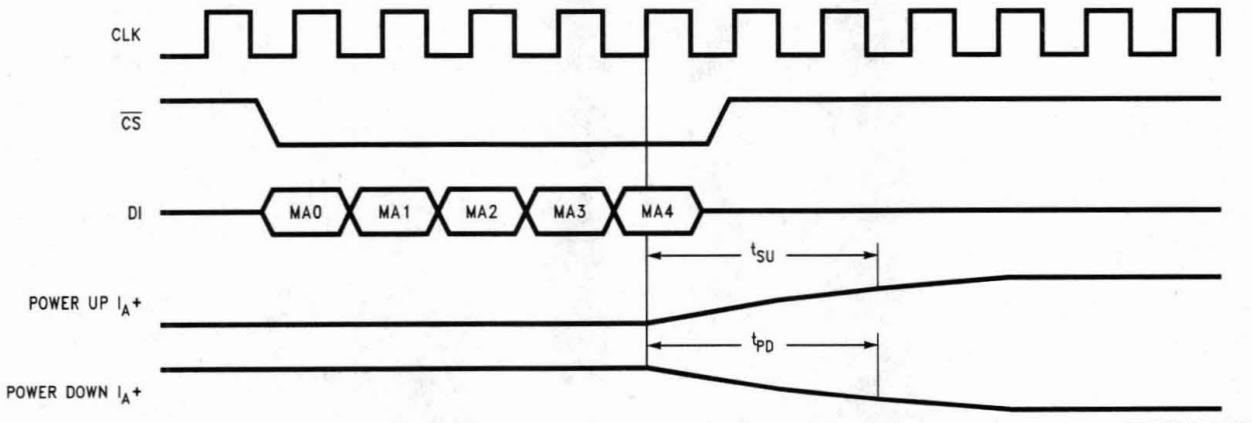

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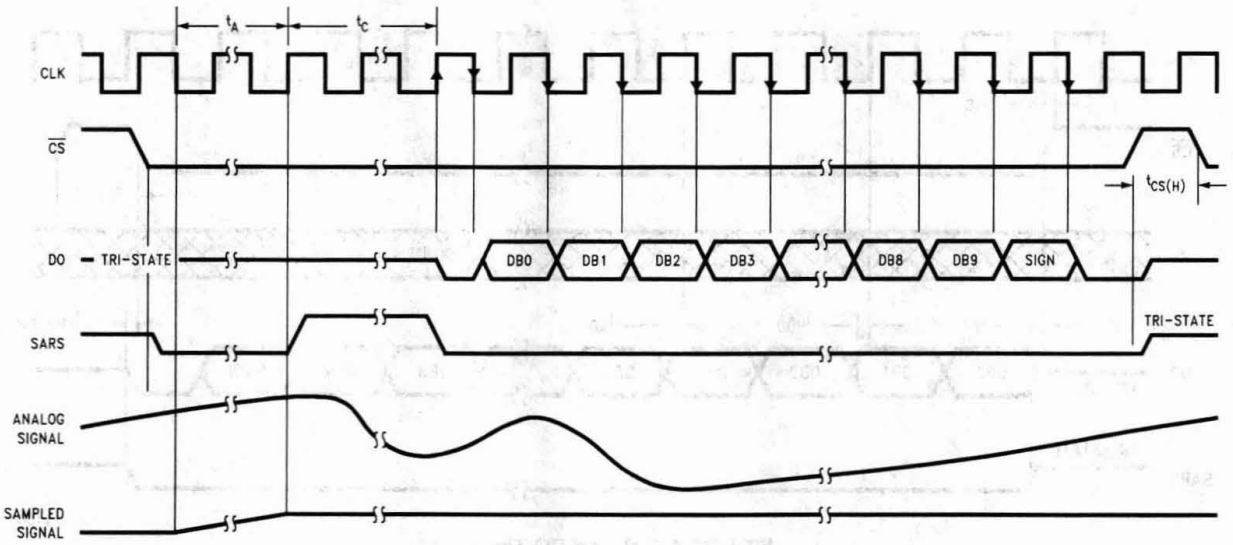
FIGURE 6. Software Power Up/Down Sequence

2

Timing Diagrams (Continued)



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Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is invalid.

FIGURE 7. ADC10831 $\overline{CS}$ Low during Conversion

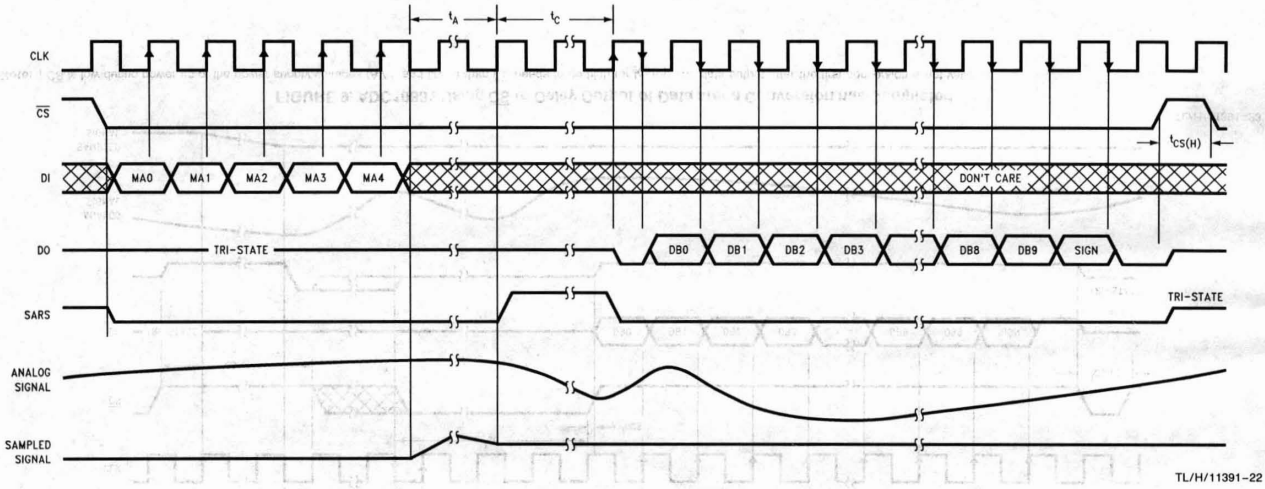

FIGURE 8. ADC10832, ADC10834 and ADC10838 $\overline{CS}$ Low during Conversion

Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

Timing Diagrams (Continued)

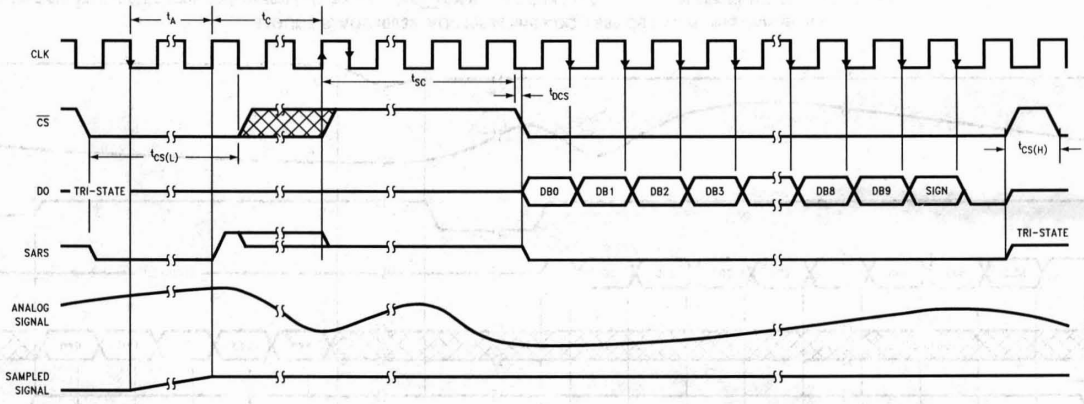

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FIGURE 9. ADC10831 Using $\overline{CS}$ to Delay Output of Data afer a Conversion has Completed

Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

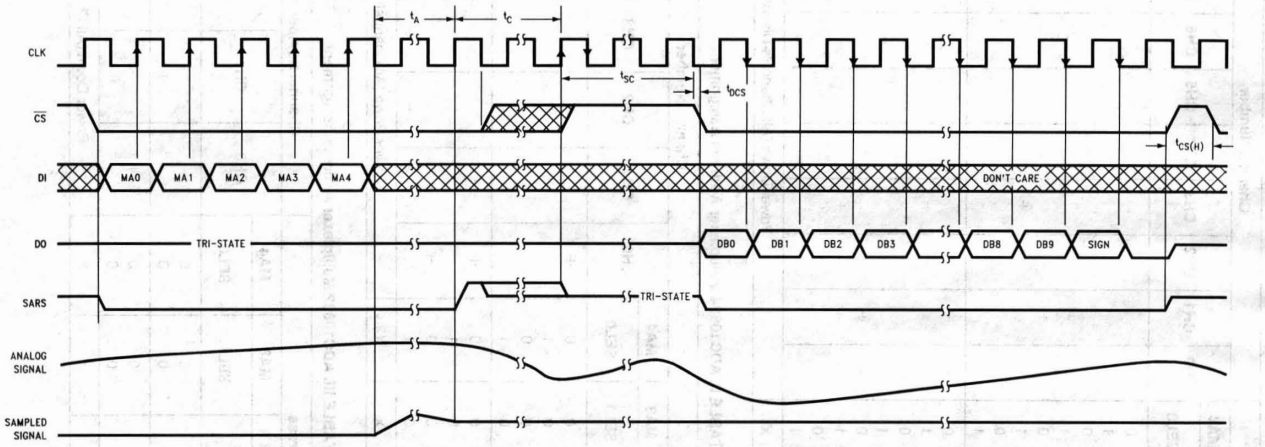

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FIGURE 10. ADC10832, ADC10834 and ADC10838 Using $\overline{CS}$ to Delay Output of Data after a Conversion has Completed

Note: If $\overline{CS}$ is low during power up of the power supply voltages (AV^+ and DV^+) then $\overline{CS}$ needs to go high for $t_{CS(H)}$. The data output after the first conversion is not valid.

TABLE I. ADC10838 Multiplexer Address Assignment

MUX Address					Channel Number									MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0										
1	1	0	0	0	+								−	Single-Ended
1	1	0	0	1			+						−	
1	1	0	1	0					+				−	
1	1	0	1	1							+		−	
1	1	1	0	0		+							−	
1	1	1	0	1				+					−	
1	1	1	1	0						+			−	
1	1	1	1	1								+	−	
1	0	0	0	0	+	−								Differential
1	0	0	0	1			+	−						
1	0	0	1	0					+	−				
1	0	0	1	1							+	−		
1	0	1	0	0	−	+								
1	0	1	0	1			−	+						
1	0	1	1	0					−	+				
1	0	1	1	1							−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)									

TABLE II. ADC10834 Multiplexer Address Assignment

MUX Address					Channel Number					MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	CH2	CH3	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0						
1	1	0	0	0	+				−	Single-Ended
1	1	0	0	1			+		−	
1	1	1	0	0		+			−	
1	1	1	0	1				+	−	
1	0	0	0	0	+	−				Differential
1	0	0	0	1			+	−		
1	0	1	0	0	−	+				
1	0	1	0	1			−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)					

TABLE III. ADC10832 Multiplexer Address Assignment

MUX Address					Channel Number			MUX MODE
MA0	MA1	MA2	MA3	MA4	CH0	CH1	COM	
PU	SING/ DIFF	ODD/ SIGN	SEL1	SEL0				
1	1	0	0	0	+		−	Single-Ended
1	1	1	0	0		+	−	
1	0	0	0	0	+	−		Differential
1	0	1	0	0	−	+		
0	X	X	X	X	Power Down (All Channels Disconnected)			

Pin Descriptions

CLK — The clock applied to this input controls the successive approximation conversion time interval, the acquisition time and the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address shift register. This address controls which channel of the analog input multiplexer (MUX) is selected. The falling edge shifts the data resulting from the A/D conversion out on DO. $\overline{CS}$ enables or disables the above functions. The clock frequency applied to this input can be between 5 kHz and 3 MHz.

DI — This is the serial data input pin. The data applied to this pln is shifted by CLK into the multiplexer address register. Tables I through III show the multiplexer address assignment.

DO — The data output pin. The A/D conversion result (DB0-SIGN) are clocked out by the falling edge of CLK on this pin.

$\overline{CS}$ — This is the chip select input pin. When a logic low is applied to this pin, the rising edge of CLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE after a conversion has been completed.

PD — This is the power down input pin. When a logic high is applied to this pin the A/D is powered down. When a low is applied the A/D is powered up.

SARS — This is the successive approximation register status output pin. When $\overline{CS}$ is high this pin is in TRI-STATE. With $\overline{CS}$ low this pin is active high when a conversion is in progress and active low at all other times.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of CLK into the address register (see Tables I–III).

The voltage applied to these inputs should not exceed AV^+ or go below V^- by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input. When the analog multiplexer is single ended this input serves as the zero reference level for inputs CH0–CH7 (see Tables I-III). COM can serve as a "pseudo ground" that has an input voltage range of $AV^+ + 50$ mV to $V^- - 50$ mV. In most cases, COM will be grounded. When the MUX is set in the differential pairs mode, COM is not used and may be grounded.

V_{REF}^+ — This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) is 0.5 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF}^+ cannot exceed $AV^+ + 50$ mV.

V_{REF}^- — The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND − 50 mV or exceed $AV^+ + 50$ mV. V_{REF}^- must always be less than V_{REF}^+.

AV^+, DV^+ — These are the analog and digital positive power supply pins. These pins should be tied to the same power supply and bypassed separately. The operating voltage range of AV^+ and DV^+ is 4.5 V_{DC} to 5.5 V_{DC}.

V^- — This is the negative analog supply pin. The operating voltage range of V^- is −4.5V to −5.5V. This supply pin needs to be bypassed with 0.1 μF ceramic and 10 μF tantalum capacitors to the system analog ground.

DGND — This is the digital ground pin.

AGND — This is the analog ground pin.

Applications Hints

The ADC10831/2/4/8 use successive approximation to digitize an analog input voltage. The DAC portion of the A/D converters uses a capacitive array and a resistive ladder structure. The structure of the DAC allows a very simple switching scheme to provide a versatile analog input multiplexer. This structure also provides a sample/hold. The ADC10831/2/4/8 have a 2.5V CMOS bandgap reference. The serial digital I/O interfaces to MICROWIRE and MICROWIRE+.

1.0 DIGITAL INTERFACE

There are two modes of operation. The fastest throughput rate is obtained when $\overline{CS}$ is kept low during a conversion. The timing diagrams in *Figures 7* and *8* show the operation of the devices in this mode. $\overline{CS}$ must be taken high for at least $t_{CS(H)}$ (1 CLK) between conversions. This is necessary to reset the internal logic. *Figures 9* and *10* show the operation of the devices when $\overline{CS}$ is taken high while the ADC10831/2/4/8 is converting. $\overline{CS}$ may be taken high during the conversion and kept high indefinitely to delay the output data. This mode simplifies the interface to other devices while the ADC10831/2/4/8 is busy converting.

1.1 Getting Started with a Conversion

The ADC10831/2/4/8 need to be initialized after the power supply voltage is applied. If $\overline{CS}$ is low when the supply voltage is applied then $\overline{CS}$ needs to be taken high for at least $t_{CS(H)}$ (1 clock period). The data output after the first conversion is not valid.

1.2 Software and Hardware Power Up/Down

These devices have the capability of software or hardware power down. *Figures 5* and *6* show the timing diagrams for hardware and software power up/down. In the case of hardware power down note that $\overline{CS}$ needs to be high for t_{PC} after PD is taken low. When PD is high the device is powered down. The total quiescent current, when powered down, is typically 200 μA with the clock at 2.5 MHz and 3 μA with the clock off. The actual voltage level applied to a digital input will affect the power consumption of the device during power down. CMOS logic levels will give the least amount of current drain (3 μA). TTL logic levels will increase the total power down current drain to 300 μA.

These devices have resistive reference ladders which draw 600 μA with a 2.5V reference voltage. The internal band gap reference voltage shuts down when power down is activated. If an external reference voltage is used, it will have to be shut down to minimize the total current drain of the device.

2.0 ARCHITECTURE

Before a conversion is started, during the analog input sampling period, (t_A), the sampled data comparator is zeroed. As the comparator is being zeroed the channel assigned to be the positive input is connected to the A/D's input capacitor. (The assignment procedure is explained in the Pin Descriptions section.) This charges the input 32C capacitor of the DAC to the positive analog input voltage. The switches shown in the DAC portion of *Figure 11* are set for this zeroing/acquisition period. The voltage at the input and output of the comparator are at equilibrium at this time. When the conversion is started, the comparator feedback switches are opened and the 32C input capacitor is then switched to the assigned negative input voltage. When the comparator feedback switch opens, a fixed amount of charge is trapped on the common plates of the capacitors. The voltage at the input of the comparator moves away from equilibrium when the 32C capacitor is switched to the assigned negative input voltage, causing the output of the comparator to go high ("1") or low ("0"). The SAR next goes through an algorithm, controlled by the output state of the comparator, that redistributes the charge on the capacitor array by switching the voltage on one side of the capacitors in the array. The objective of the SAR algorithm is to return the voltage at the input of the comparator as close as possible to equilibrium.

The switch position information at the completion of the successive approximation routine is a direct representation of the digital output. This data is then available to be shifted on the D0 pin.

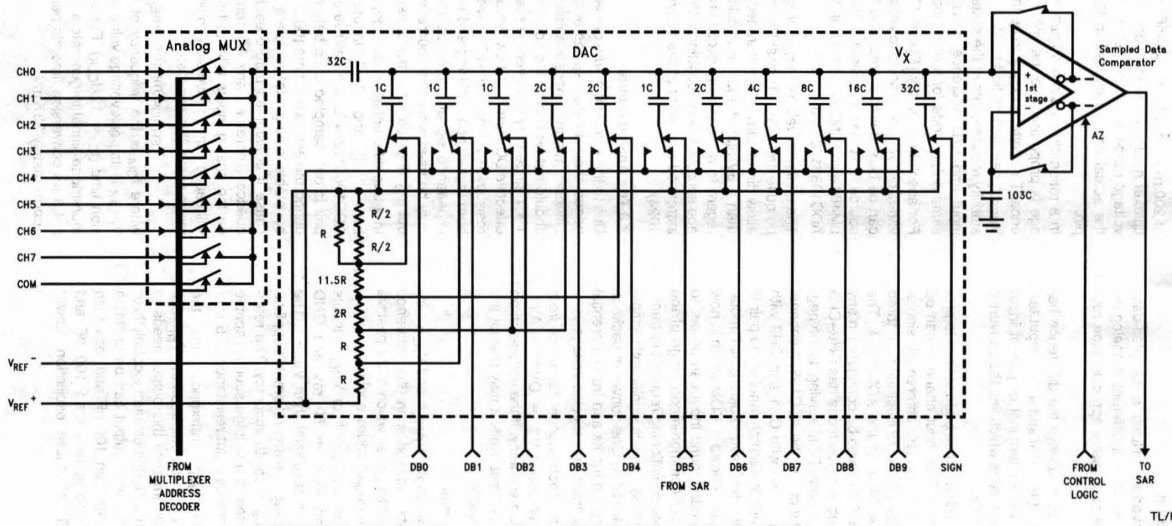


FIGURE 11. Detailed Diagram of the ADC10838 DAC and Analog Multiplexer Stages

Applications Hints (Continued)

3.0 APPLICATIONS INFORMATION

3.1 Multiplexer Configuration

The design of these converters utilizes a sampled-data comparator structure, which allows a differential analog input to be converted by the successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal or pair of input terminals being converted indicates which line the converter expects to be the most positive.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-ended, or pseudo-differential. *Figure 12* illustrates the three modes using the 4-channel MUX of the ADC10834. The eight inputs of the ADC10838 can also be configured in any of the three modes. The single-ended mode has CH0–CH3 assigned as the positive input with COM serving as the negative input. In the differential mode, the ADC10834 channel inputs are grouped in pairs, CH0 with CH1 and CH2 with CH3. The polarity assignment of each channel in the pair is interchangeable. Finally, in the pseudo-differential mode CH0–CH3 are positive inputs referred to COM which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground-referred inputs and true differential inputs as well as signals referred to a specific voltage.

The analog input voltages for each channel can range from 50 mV below V^- to 50 mV above $V^+ = DV^+ = AV^+$ without degrading conversion accuracy. If the voltage on an unselected channel exceeds these limits it may corrupt the reading of the selected channel.

3.2 Reference Considerations

The voltage difference between the V_{REF}^+ and V_{REF}^- inputs defines the analog input voltage span (the difference between V_{IN}(Max) and V_{IN}(Min)) over which 1023 positive and 1024 negative possible output codes apply.

The value of the voltage on the V_{REF}^+ or V_{REF}^- inputs can be anywhere between $AV^+ + 50$ mV and GND −50 mV, so long as V_{REF}^+ is greater than V_{REF}^-. The ADC10831/2/4/8 can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pins must be connected to a voltage source capable of driving the minimum reference input resistance of 5 kΩ.

The internal 2.5V bandgap reference in the ADC10831/2/4/8 is available as an output on the V_{REF}Out pin. To ensure optimum performance this output needs to be bypassed to ground with 100 μF aluminum electrolytic or tantalum capacitor. The reference output can be unstable with capacitive loads greater than 100 pF and less than 100 μF. Any capacitive loading less than 100 pF and greater than 100 μF will not cause oscillation. Lower output noise can be obtained by increasing the output capacitance. A 100 μF capacitor will yield a typical noise floor of 200 nV/$\sqrt{\text{Hz}}$. The pseudo-differential and differential multiplexer modes allow for more flexibility in the analog input voltage range since the "zero" reference voltage is set by the actual voltage applied to the assigned negative input pin.

In a ratiometric system *(Figure 13a)*, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage may also be the system power supply, so V_{REF}^+ can also be tied to AV^+. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy *(Figure 13b)*, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time- and temperature-stable voltage source that has excellent initial accuracy. The LM4040, LM4041 and LM185 references are suitable for use with the ADC10831/2/4/8.

The minimum value of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) can be quite small (see Typical Performance Characteristics) to allow direct conversion of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/1024).

3.3 The Analog Inputs

Due to the sampling nature of the analog inputs, at the clock edges short duration spikes of current will be seen on the selected assigned negative input. Input bypass capacitors should not be used if the source resistance is greater than 1 kΩ since they will average the AC current and cause an effective DC current to flow through the analog input source resistance. An op amp RC active lowpass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required. Bypass capacitors may be used when the source impedance is very low without any degradation in performance.

In a true differential input stage, a signal that is common to both "+" and "−" inputs is canceled. For the ADC10831/2/4/8, the positive input of a selected channel pair is only sampled once before the start of a conversion during the acquisition time (t_A). The negative input needs to be stable during the complete conversion sequence because it is sampled before each decision in the SAR sequence. Therefore, any AC common-mode signal present on the analog inputs will not be completely canceled and will cause some conversion errors. For a sinusoid common-mode signal this error is:

$$V_{ERROR}(\text{max}) = V_{PEAK}\,(2\,\pi\,f_{CM})\,(t_C)$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value, and t_C is the A/D's conversion time ($t_C = 12/f_{CLK}$). For example, for a 60 Hz common-mode signal to generate a ¼ LSB error (0.61 mV) with a 4.8 μs conversion time, its peak value would have to be approximately 337 mV.

Applications Hints (Continued)

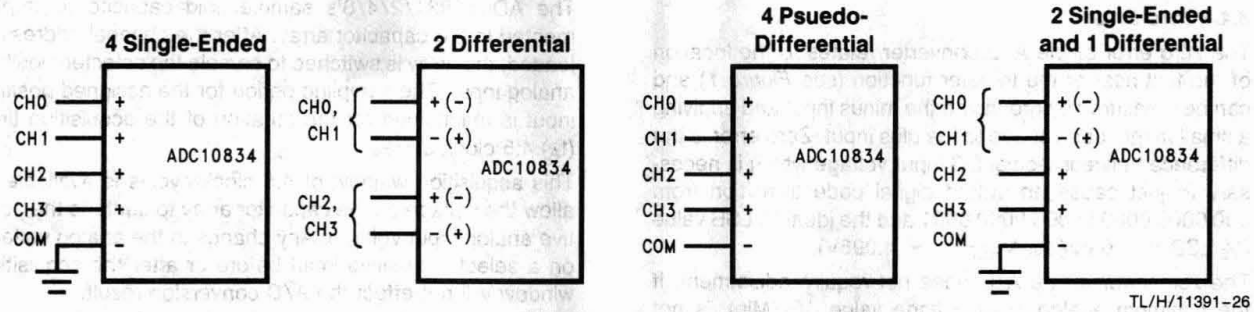
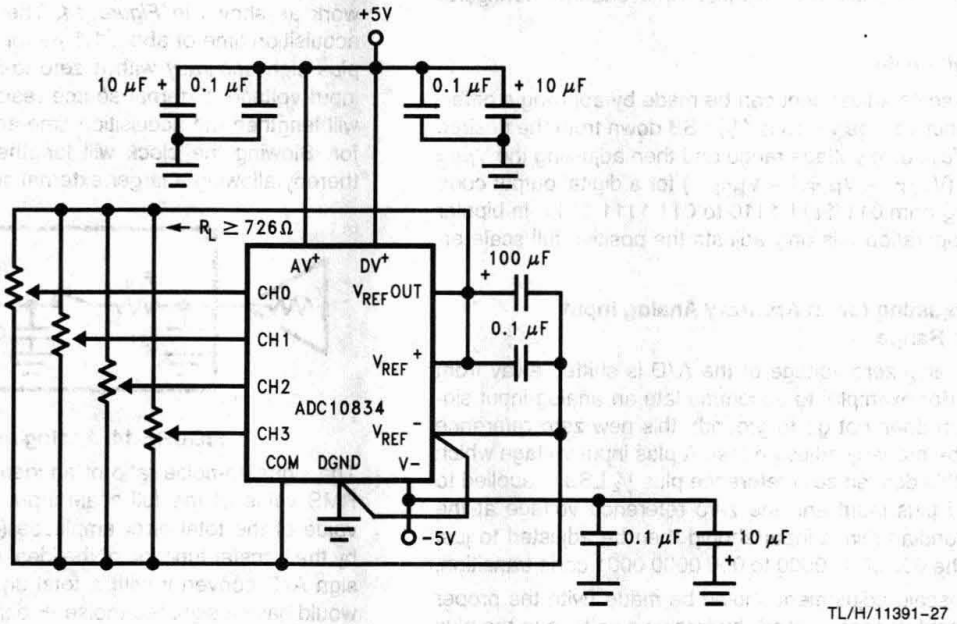


FIGURE 12. Analog Input Multiplexer Options

a. Ratiometric Using the Internal Reference



b. Absolute Using a ±4.096V Span

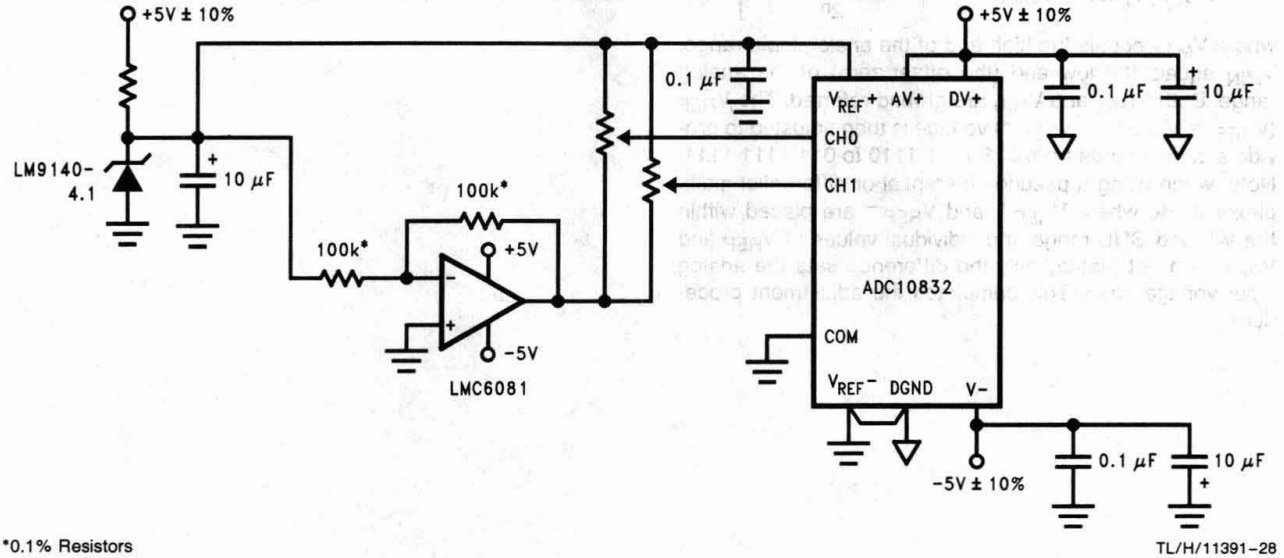


FIGURE 13. Different Reference Configurations

Applications Hints (Continued)

3.4 Optional Adjustments

3.4.1 Zero Error

The zero error of the A/D converter relates to the location of the first riser of the transfer function (see *Figure 1*) and can be measured by grounding the minus input and applying a small magnitude voltage to the plus input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 000 0000 0000 to 000 0000 0001 and the ideal ½ LSB value (½ LSB = 2.0 mV for V_{REF} = + 4.096V).

The zero error of the A/D does not require adjustment. If the minimum analog input voltage value, V_{IN}(Min), is not ground, the effective "zero" voltage can be adjusted to a convenient value. The converter can be made to output an all zeros digital code for this minimum input voltage by biasing any minus input to V_{IN}(Min). This is useful for either the differential or pseudo-differential input channel configurations.

3.4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the V_{REF} voltage ($V_{REF} = V_{REF}^+ - V_{REF}^-$) for a digital output code changing from 011 1111 1110 to 011 1111 1111. In bipolar signed operation this only adjusts the positive full scale error.

3.4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A plus input voltage which equals this desired zero reference plus ½ LSB is applied to selected plus input and the zero reference voltage at the corresponding minus input should then be adjusted to just obtain the 000 0000 0000 to 000 0000 0001 code transition.

The full-scale adjustment should be made [with the proper minus input voltage applied] by forcing a voltage to the plus input which is given by:

$$V_{IN}(+)\, f_s\, adj = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{2^n} \right]$$

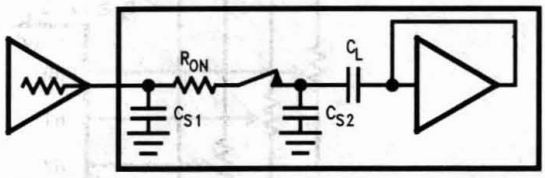
where V_{MAX} equals the high end of the analog input range, V_{MIN} equals the low end (the offset zero) of the analog range. Both V_{MAX} and V_{MIN} are ground referred. The V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) voltage is then adjusted to provide a code change from 011 1111 1110 to 011 1111 1111. Note, when using a pseudo-differential or differential multiplexer mode where V_{REF}^+ and V_{REF}^- are placed within the V^+ and GND range, the individual values of V_{REF} and V_{REF}^- do not matter, only the difference sets the analog input voltage span. This completes the adjustment procedure.

3.5 The Input Sample and Hold

The ADC10831/2/4/8's sample/hold capacitor is implemented in the capacitor array. After the channel address is loaded, the array is switched to sample the selected positive analog input. The sampling period for the assigned positive input is maintained for the duration of the acquisition time (t_A) 4.5 clock cycles.

This acquisition window of 4.5 clock cycles is available to allow the voltage on the capacitor array to settle to the positive analog input voltage. Any change in the analog voltage on a selected positive input before or after the acquisition window will not effect the A/D conversion result.

In the simplest case, the array's acquisition time is determined by the R_{ON} (3 kΩ) of the multiplexer switches, the stray input capacitance C_{S1} (3.5 pF) and the total array (C_L) and stray (C_{S2}) capacitance (48 pF). For a large source resistance the analog input can be modeled as an RC network as shown in *Figure 14*. The values shown yield an acquisition time of about 1.1 μs for 10-bit unipolar or 10-bit plus sign accuracy with a zero-to-full-scale change in the input voltage. External source resistance and capacitance will lengthen the acquisition time and should be accounted for. Slowing the clock will lengthen the acquisition time, thereby allowing a larger external source resistance.



TL/H/11391–29

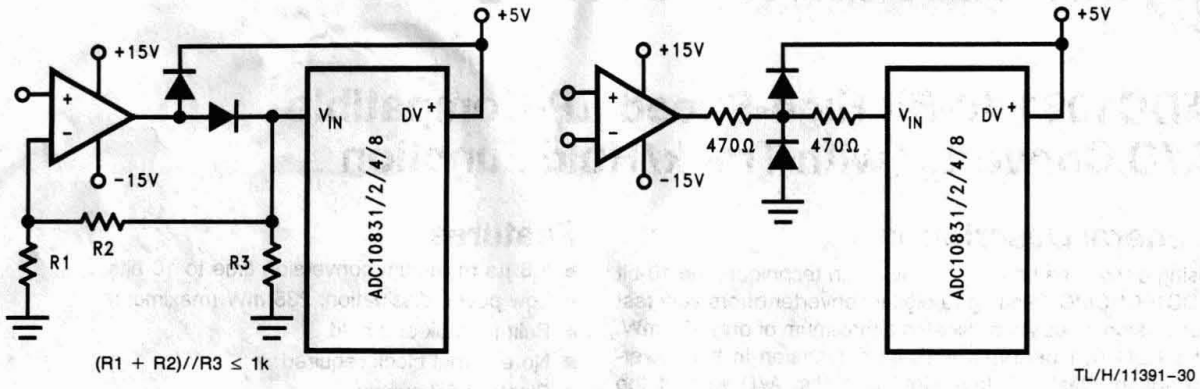
FIGURE 14. Analog Input Model

The signal-to-noise ratio of an ideal A/D is the ratio of the RMS value of the full scale input signal amplitude to the value of the total error amplitude (including noise) caused by the transfer function of the ideal A/D. An ideal 10-bit plus sign A/D converter with a total unadjusted error of 0 LSB would have a signal-to-(noise + distortion) ratio of about 68 dB, which can be derived from the equation:

$$S/(N + D) = 6.02(n) + 1.8$$

where S/(N + D) is in dB and n is the number of bits.

Applications Hints (Continued)



Note 1: Diodes are 1N914.

Note 2: The protection diodes should be able to withstand the output current of the op amp under current limit.

FIGURE 15. Protecting the Analog Inputs

National Semiconductor

ADC1061 10-Bit High-Speed μP-Compatible A/D Converter with Track/Hold Function

General Description

Using a modified half-flash conversion technique, the 10-bit ADC1061 CMOS analog-to-digital converter offers very fast conversion times yet dissipates a maximum of only 235 mW. The ADC1061 performs a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches.

The analog input voltage to the ADC1061 is tracked and held by an internal sampling circuit. Input signals at frequencies from DC to greater than 160 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

For ease of interface to microprocessors, the ADC1061 has been designed to appear as a memory location or I/O port without the need for external interface logic.

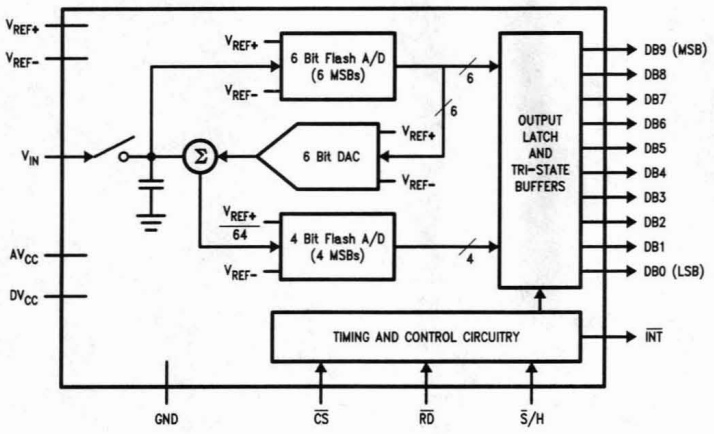
Features

- 1.8 μs maximum conversion time to 10 bits
- Low power dissipation: 235 mW (maximum)
- Built-in track-and-hold
- No external clock required
- Single +5V supply
- No missing codes over temperature

Applications

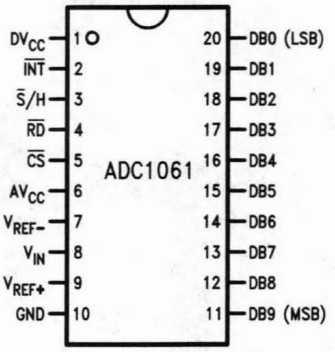
- Waveform digitizers
- Disk drives
- Digital signal processor front ends
- Mobile telecommunications

Simplified Block and Connection Diagrams



TL/H/10559–2

Dual-In-Line Package



TL/H/10559–1

Top View

Order Number ADC1061CIJ, ADC1061CIN, ADC1061CIWM or ADC1061CMJ
See NS Package J20A, M20B or N20A

Ordering Information

Industrial ($-40°C \le T_A \le 85°C$)	Package
ADC1061CIJ	J20A
ADC1061CIN	N20A
ADC1061CIWM	M20B
Military ($-55°C \le T_A \le 125°C$)	**Package**
ADC1061CMJ	J20A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)	−0.3V to +6V
Voltage at any Input or Output	−0.3V to V^+ +0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	875 mW
ESD Susceptibility (Note 5)	1500V
Soldering Information (Note 6)	
N Package (10 seconds)	260°C
J Package (10 seconds)	300°C
SO Package (Note 6):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Junction Temperature, T_J	+150°C
Storage Temperature Range	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1061CIJ, ADC1061CIN, ADC1061CIWM	$-40°C \le T_A \le +85°C$
ADC1061CMJ	$-55°C \le T_A \le +125°C$
Supply Voltage Range	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = 5V$, and $V_{REF(-)} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
	Resolution			**10**	Bits
	Total Unadjusted Error		±1.0	**±2.0**	LSB (Max)
	Integral Linearity Error		±0.3	**±1.5**	LSB (Max)
	Differential Linearity Error			**±1.0**	LSB (Max)
	Offset Error		±0.1	**±1.0**	LSB (Max)
	Fullscale Error		±0.5	**±1.0**	LSB (Max)
R_{REF}	Reference Resistance		0.65	**0.4**	kΩ (Min)
R_{REF}	Reference Resistance		0.65	**0.9**	kΩ (Max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (Max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (Min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (Min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(-)}$**	V (Max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (Max)
V_{IN}	Input Voltage			**GND − 0.05**	V (Min)
	Analog Input Leakage Current	$\overline{CS} = V^+$, $V_{IN} = V^+$ $\overline{CS} = V^+$, $V_{IN} = GND$	0.01 0.01	**3** **−3**	μA (Max) μA (Max)
	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$ $V_{REF} = 4.75V$	±0.125	**±0.5**	LSB

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = 5V$, and $V_{REF(-)} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.25V$		**2.0**	V (Min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.75V$		**0.8**	V (Max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN(1)} = 5V$	0.005	**1.0**	μA (Max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN(0)} = 0V$	−0.005	**−1.0**	μA (Max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.75V$ $I_{OUT} = -360\ \mu A$ $V^+ = 4.75V$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**	V (Min) V (Min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**	V (Max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 5V$ $V_{OUT} = 0V$	0.1 −0.1	**50** **−50**	μA (Max) μA (Max)
DI_{CC}	DV_{CC} Supply Current	$CS = WR = \overline{RD} = 0$	0.1	**2**	mA (Max)
AI_{CC}	AV_{CC} Supply Current	$CS = WR = \overline{RD} = 0$	30	**45**	mA (Max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, and $V_{REF(-)} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{CONV}	Conversion Time from Rising Edge of $\overline{S}/H$ to Falling Edge of $\overline{INT}$	Mode 1	1.2	**1.8**	μs (Max)
t_{CRD}	Conversion Time for MODE 2 (RD Mode)	Mode 2	1.8	**2.4**	μs (Max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; $C_L = 100$ pF	20	**50**	ns (Max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; $C_L = 100$ pF		**t_{CRD} + 50**	ns (Max)
t_{SH}	Minimum Sample Time	*(Figure 1)*; (Note 9)		**250**	ns (Max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	$R_L = 1k$, $C_L = 10$ pF	20	**50**	ns (Max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$		10	**50**	ns (Max)
t_{ID}	Delay from $\overline{INT}$ to Output Valid	$C_L = 100$ pF	20	**50**	ns (Max)
t_P	Delay from End of Conversion to Next Conversion		10	**20**	ns (Max)
SR	Slew Rate for Correct Track-and-Hold Operation		2.5		V/μs

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, and $V_{REF(-)} = GND$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units
C_{VIN}	Analog Input Capacitance		35		pF
C_{OUT}	Logic Output Capacitance		5		pF
C_{IN}	Logic Input Capacitance		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input of 5 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 150°C$, and the typical thermal resistance (θ_{JA}) when board mounted is 47°C/W for the plastic (N) package, 85°C/W for the ceramic (J) package, and 65°C/W for the small outline (WM) package.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

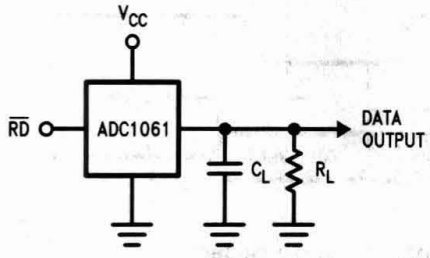
Note 6: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Typicals are at 25°C and represent most likely parametric norm.

Note 8: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Accuracy may degrade if tSH is shorter than the value specified.

TRI-STATE Test Circuits and Waveforms



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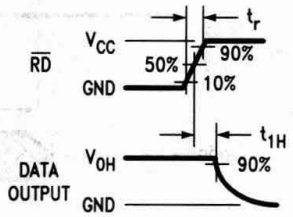
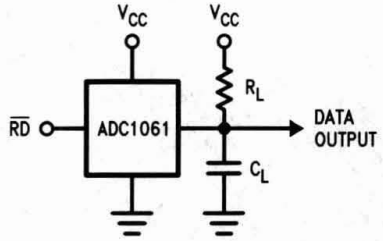
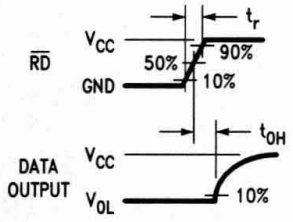


TL/H/10559–4



TL/H/10559–5



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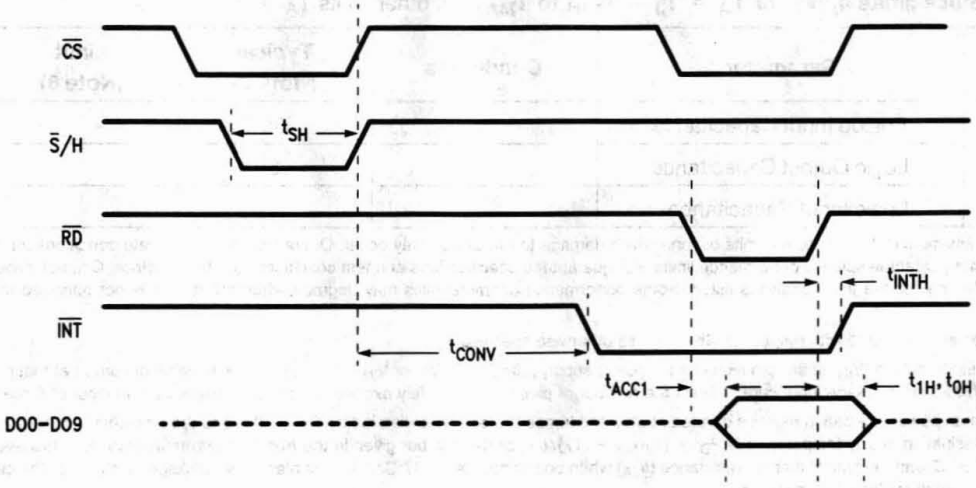
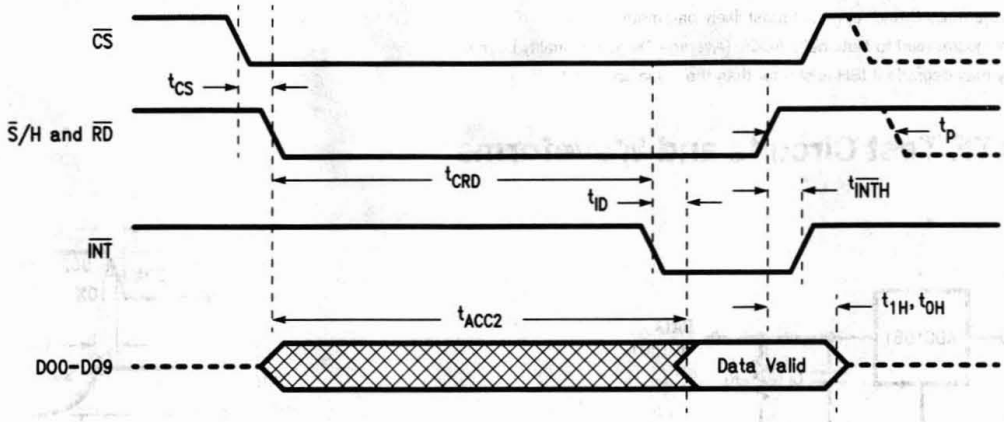
Timing Diagrams



TL/H/10559–7

FIGURE 1. Mode 1. The conversion time (t_{CONV}) is determined by the internal timer.

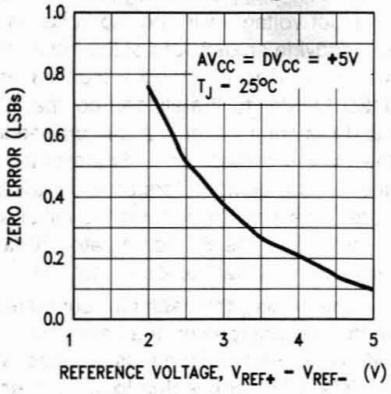


TL/H/10559–8

FIGURE 2. Mode 2 (RD Mode). The conversion time (t_{CRD}) includes the sampling time, and is determined by the internal timer.

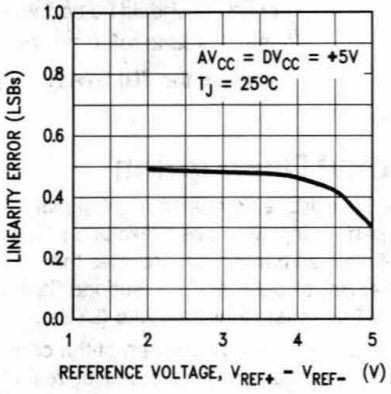
Typical Performance Characteristics

Zero (Offset) Error vs Reference Voltage



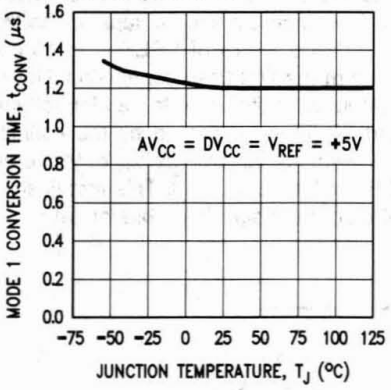
TL/H/10559–9

Linearity Error vs Reference Voltage



TL/H/10559–10

Mode 1 Conversion Time vs Temperature



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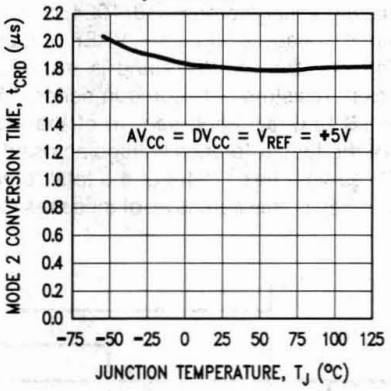
Mode 2 Conversion Time vs Temperature



TL/H/10559–12

Pin Descriptions

Symbol	Function
DV_{CC}, AV_{CC} (1, 6)	These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.
$\overline{INT}$ (2)	This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.
$\overline{S}/H$ (3)	This is the Sample/Hold control input. When this pin is forced low, it causes the analog input signal to be sampled and initiates a new conversion.
$\overline{RD}$ (4)	This is the active low Read control input. When this pin is low, any data present in the ADC1061's output registers will be placed on the data bus. In Mode 2, the Read signal must be low until $\overline{INT}$ goes low. Until $\overline{INT}$ goes low, the data at the output pins will be incorrect.
$\overline{CS}$ (5)	This is the active low Chip Select control input. This pin enables the $\overline{S}/H$ and $\overline{RD}$ inputs.
$V_{REF}-$, $V_{REF}+$ (7, 9)	These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V_{CC} + 50 mV, but $V_{REF}+$ must be greater than $V_{REF}-$. An input voltage equal to $V_{REF}-$ produces an output code of 0, and an input voltage equal to $V_{REF}+$ − 1LSB produces an output code of 1023.
V_{IN} (8)	This is the analog input pin. The impedance of the source should be less than 500Ω for best accuracy and conversion speed. To avoid damage to the ADC1061, V_{IN} should not be allowed to extend beyond the power supply voltages by more than 300 mV unless the drive current is limited. For accurate conversions, V_{IN} should not extend more than 50 mV beyond the supply voltages.

Pin Descriptions (Continued)

Symbol	Function
GND (10)	This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.
DB0–DB9 (11-20)	These are the TRI-STATE output pins.

Functional Description

The ADC1061 digitizes an analog input signal to 10 bits accuracy by performing two lower-resolution "flash" conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits (LSBs).

Figure 3 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024th the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64th of the total reference voltage (V_{REF+} − VREF−) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has 1/8th of the total reference voltage across it, and each of the MSB resistors has 1/64th of the total reference voltage across it. Tap points across all of these resistors can be connected, in groups, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between V_{REF+} − V_{REF-}. Six comparators compare the input voltage with the tap voltages on the resistor string to provide an estimate of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of VREF. The estimator decoder will instruct the comparator mux to connect the 16 comparators to the taps on the MSB Ladder between 10/16 and 14/16 of VREF. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to Ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as $1/16$ of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data.

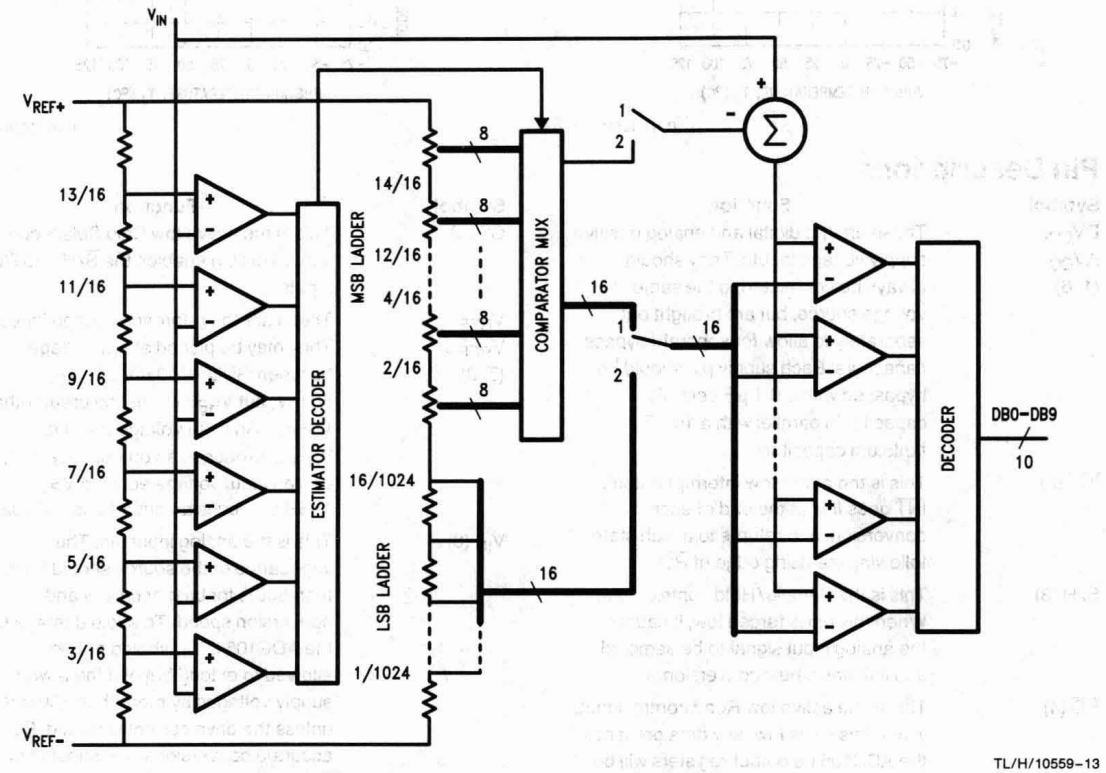


FIGURE 3. Block Diagram of the Modified Half-Flash Converter Architecture

Functional Description (Continued)

The remaining four LSBs may now be determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the half-flash conversion techniques used in the ADC1061 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC1061 to perform high-speed conversions without excessive power drain.

Applications Information

1.0 Modes of Operation

The ADC1061 has two basic digital interface modes. These are illustrated in *Figure 1* and *Figure 2*.

MODE 1

In this mode, the $\overline{S}/H$ pin controls the start of conversion. $\overline{S}/H$ is pulled low for a minimum of 250 ns. This causes the comparators in the "coarse" flash converter to become active. When $\overline{S}/H$ goes high, the result of the coarse conversion is latched and the "fine" conversion begins. After approximately 1.2 μs (1.8 μs maximum), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}/H$ or $\overline{RD}$. $\overline{CS}$ is internally "ANDed" with the sample and read control signals; the input voltage is sampled when $\overline{CS}$ and $\overline{S}/H$ are low, and is read when $\overline{CS}$ and $\overline{RD}$ are low.

MODE 2

In Mode 2, also called "RD mode", the $\overline{S}/H$ and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The ADC1061 samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion.

About 1.8 μs (2.4 μs maximum) after $\overline{S}/H$ and $\overline{RD}$ are pulled low, $\overline{INT}$ goes low, indicating that the conversion is complete. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but will be valid only after $\overline{INT}$ goes low.

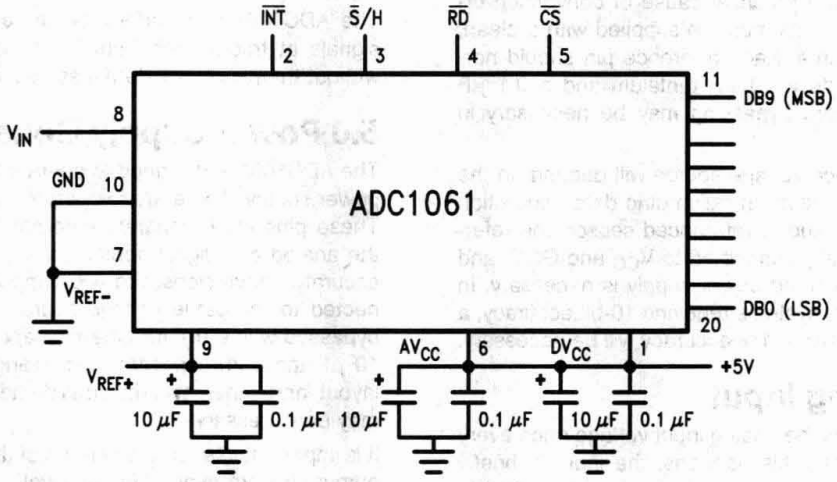


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FIGURE 4. Typical connection. Note the multiple bypass capacitors on the reference and power supply pins. If $V_{REF}-$ is not grounded, it should also be bypassed to ground using multiple capacitors (see 5.0 "Power Supply Considerations").

2.0 Reference Considerations

The ADC1061 has two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range (V_{REF-} = 0V, V_{REF+} = V_{CC}) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required. Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if V_{REF} = 2V, then 1LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See the Typical Performance Curves for more information. Reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC1061. V_{REF-} can be connected to a voltage other than ground as long as the reference for this pin is capable of sinking current. If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should normally be bypassed with a 10 μF tantalum and a 0.1 μF ceramic capacitor. More bypassing may be necessary in some systems.

The choice of reference voltage source will depend on the requirements of the system. In ratiometric data acquisition systems with a power supply-referenced sensor, the reference inputs are normally connected to V_{CC} and GND, and no reference other than the power supply is necessary. In absolute measurement systems requiring 10-bit accuracy, a reference with better than 0.1% accuracy will be necessary.

3.0 The Analog Input

The ADC1061 samples the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can therefore be observed at the analog input during normal operation. These spikes are normal and do not degrade the convertor's performance.

Note that large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time. If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than AV_{CC} and DV_{CC}, or more than 300 mV lower than GND. If the analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the ADC1061.

4.0 Inherent Sample-and-Hold

Because the ADC1061 samples the input signal once during each conversion, it is capable of measuring relatively fast input signals without the help of an external sample-hold. In a conventional successive-approximation A/D converter, regardless of speed, the input signal must be stable to better than ±½ LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion.

The ADC1061 can perform accurate conversions of input signals at frequencies from DC to greater than 160 kHz without the need for external sampling circuitry.

5.0 Power Supply Considerations

The ADC1061 is designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor. Depending on the circuit board layout and other system considerations, more bypassing may be necessary.

It is important to ensure that none of the ADC1061's input or output pins are ever driven to a voltage more than 300 mV above AV_{CC} and DV_{CC}, or more than 300 mV below GND. If these voltage limits are exceeded, the overdrive current into or out of any pin on the ADC1061 must be limited to less than 5 mA, and no more than 20 mA of overdrive current (all overdriven pins combined) should flow. In systems with multiple power supplies, this may require careful attention to power supply sequencing. The ADC1061's power supply pins should be at the proper voltage before signals are applied to any of the other pins.

6.0 Layout and Grounding

In order to ensure fast, accurate conversions from the ADC1061, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome, so digital grounds should always be separate from analog grounds. For best performance, separate ground planes should be provided for the digital and analog parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

National Semiconductor

ADC10061/ADC10062/ADC10064 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep* conversion technique, the 10-bit ADC10061, ADC10062, and ADC10064 CMOS analog-to-digital converters offer sub-microsecond conversion times yet dissipate a maximum of only 235 mW. The ADC10061, ADC10062, and ADC10064 perform a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. The ADC10061 is pin-compatible with the ADC1061 but much faster, thus providing a convenient upgrade path for the ADC1061.

The analog input voltage to the ADC10061, ADC10062, and ADC10064 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 200 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10062 and ADC10064 include a "speed-up" pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 350 ns with only a small increase in linearity error.

For ease of interface to microprocessors, the ADC10061, ADC10062, and ADC10064 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Features

- Built-in sample-and-hold
- Single +5V supply
- 1, 2, or 4-input multiplexer options
- No external clock required
- Speed adjust pin for faster conversions (ADC10062 and ADC10064). See ADC10662/4 for high speed guaranteed performance.

Key Specifications

- Conversion time to 10 bits — 600 ns typical, 900 ns max over temperature
- Sampling Rate — 800 kHz
- Low power dissipation — 235 mW (max)
- Total unadjusted error — ±1.0 LSB (max)
- No missing codes over temperature

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Ordering Information

ADC10061

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10061BIN, ADC10061CIN	N20A Molded DIP
ADC10061BIWM, ADC10061CIWM	M20B Small Outline

Military ($-55°C \le T_A \le +125°C$)	Package
ADC10061CMJ/883	J20A Cerdip

ADC10062

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10062BIN, ADC10062CIN	N24A Molded DIP
ADC10062BIWM, ADC10062CIWM	M24B Small Outline

Military ($-55°C \le T_A \le +125°C$)	Package
ADC10062CMJ/883	J24A Cerdip

ADC10064

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10064BIN, ADC10064CIN	N28B Molded DIP
ADC10064BIWM, ADC10064CIWM	M28B Small Outline

Military ($-55°C \le T_A \le +125°C$)	Package
ADC10064CMJ/883	J28A Cerdip

*U.S. Patent Number 4918449

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)	−0.3V to +6V
Voltage at Any Input or Output	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	875 mW
ESD Susceptability (Note 5)	2000V
Soldering Information (Note 6)	
N Package (10 Sec)	260°C
J Package (10 Sec)	300°C
SO Package:	
Vapor Phase (60 Sec)	215°C
Infrared (15 Sec)	220°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10061BIN, ADC10061BIWM, ADC10061CIN, ADC10061CIWM, ADC10062BIN, ADC10062BIWM, ADC10062CIN, ADC10062CIWM, ADC10064BIN, ADC10064BIWM, ADC10064CIN, ADC10064CIWM	$-40°C \le T_A \le +85°C$
ADC10061CMJ/883, ADC10062CMJ/883, ADC10064CMJ/883	$-55°C \le T_A \le +125°C$
Supply Voltage Range	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = +5V$, $V_{REF(-)} = GND$, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{Min}$ to T_{Max};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Notes 8, 10)	Units (Limit)
	Resolution			**10**	Bits
	Integral Linearity Error	BIN, BIWM Suffixes		±0.6/±**1.1**	LSB (max)
		CIN, CIWM, CMJ Suffixes		±1.0/±**1.5**	LSB (max)
		R_{SA} = 18 kΩ	±0.5		LSB
	Offset Error			±**1**	LSB (max)
	Full-Scale Error			±**1**	LSB (max)
	Total Unadjusted Error	BIN, BIWM Suffixes		±1.0/±**1.5**	LSB (max)
		CIN, CIWM, CMJ Suffixes		±1.5/±**2.0**	LSB (max)
		All Suffixes, R_{SA} = 18 kΩ	±0.5		LSB
	Missing Codes			**0**	(max)
	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.5V$	±1/16		LSB
		$V^+ = 5V \pm 10\%$, $V_{REF} = 4.5V$		±**3/8**	LSB (max)
THD	Total Harmonic Distortion	f_{IN} = 10 kHz, 4.85 V_{P-P}	0.06		%
		f_{IN} = 160 kHz, 4.85 V_{P-P}	0.08		%
SNR	Signal-to-Noise Ratio	f_{IN} = 10 kHz, 4.85 V_{P-P}	61		dB
		f_{IN} = 160 kHz, 4.85 V_{P-P}	60		dB
	Effective Number of Bits	f_{IN} = 10 kHz, 4.85 V_{P-P}	9.6		Bits
		f_{IN} = 160 kHz, 4.85 V_{P-P}	9.4		Bits
R_{REF}	Reference Resistance		650	**400**	Ω (min)
R_{REF}	Reference Resistance		650	**900**	Ω (max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(+)}$**	V (max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (max)
V_{IN}	Input Voltage			**GND − 0.05**	V (min)
	OFF Channel Input Leakage Current	$\overline{CS} = V^+$, $V_{IN} = V^+$	0.01	**3**	μA (max)
	ON Channel Input Leakage Current	$\overline{CS} = V^+$, $V_{IN} = V^+$	±1	**−3**	μA (max)

2

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = 5V$ $V_{REF(-)} = GND$, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Notes 8, 10)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN(1)} = 5V$	0.005	**3.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN(0)}$ 0V	−0.005	**−3.0**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = -360\ \mu A$ $V^+ = 4.5V$, $I_{OUT} = -10\ \mu A$		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 5V$ $V_{OUT} = 0V$	0.1 −0.1	**50** **−50**	μA (max) μA (max)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = \infty$ $\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = 18\ k\Omega$	1.0 1.0	**2**	mA (max) mA (max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = \infty$ $\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = 18\ k\Omega$	30 30	**45**	mA (max) mA (max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Notes 8, 10)	Units (Limits)
t_{CONV}	Mode 1 Conversion Time from Rising Edge of $\overline{S}/H$ to Falling Edge of $\overline{INT}$	BIN, BIWM, CIN, CIWM Suffixes CMJ Suffixes $R_{SA} = 18k$	 600 600 375	 750/**900** **1000**	 ns (max) ns (max) ns
t_{CRD}	Mode 2 Conversion Time	BIN, BIWM, CIN, CIWM Suffixes CMJ Suffixes Mode 2, $R_{SA} = 18k$	 850 850 530	 **1400** **1500**	 ns (max) ns (max) ns
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; $C_L = 100$ pF	30	**60**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; $C_L = 100$ pF	900	t_{CRD} + **50**	ns (max)
t_{SH}	Minimum Sample Time	*(Figure 1)*; (Note 9)		**250**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	$R_L = 1k$, $C_L = 10$ pF	30	**60**	ns (max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 100$ pF	25	**50**	ns (max)
t_P	Delay from End of Conversion to Next Conversion			**50**	ns (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)}$ = GND, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{MS}	Multiplexer Control Setup Time		10	**75**	ns (max)
t_{MH}	Multiplexer Hold Time		10	**40**	ns (max)
C_{VIN}	Analog Input Capacitance		35		pF (max)
C_{OUT}	Logic Output Capacitance		5		pF (max)
C_{IN}	Logic Input Capacitance		5		pF (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditons.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. In most cases, the maximum derated power dissipation will be reached only during fault conditions. For these devices, T_{JMAX} for a board-mounted device can be found from the tables below:

ADC10061

Suffix	θ_{JA} (°C/W)
CMJ	54
BIN, CIN	70
BIWM, CIWM	85

ADC10062

Suffix	θ_{JA} (°C/W)
CMJ	48
BIN, CIN	60
BIWM, CIWM	82

ADC10064

Suffix	θ_{JA} (°C/W)
CMJ	44
BIN, CIN	53
BIWM, CIWM	78

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Typicals are at +25°C and represent must likely parametric norm.

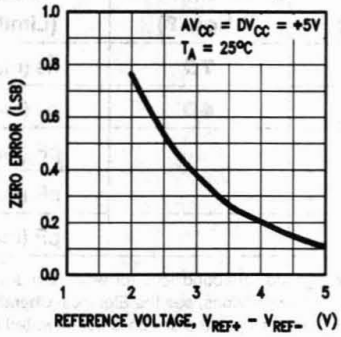
Note 8: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Accuracy may degrade if t_{SH} is shorter than the value specified. See curves of Accuracy vs t_{SH}.

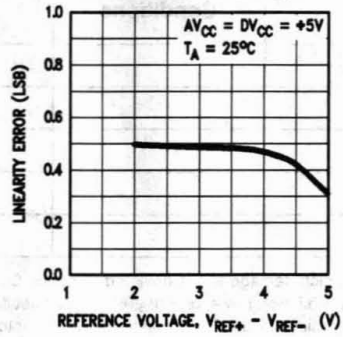
Note 10: A military RETS electrical test specification is available on request. At time of printing, the ADC10061CMJ/883, ADC10062CMJ/883, and ADC10064CMJ/883 RETS specification complies fully with the **boldface** limits in this column.

Typical Performance Characteristics

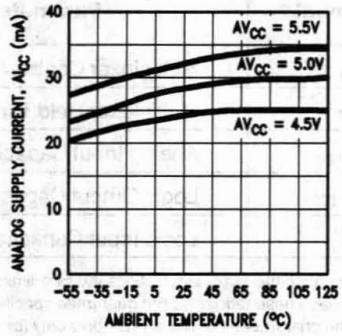
Zero (Offset) Error vs Reference Voltage



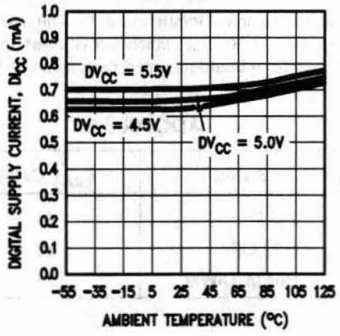
Linearity Error vs Reference Voltage



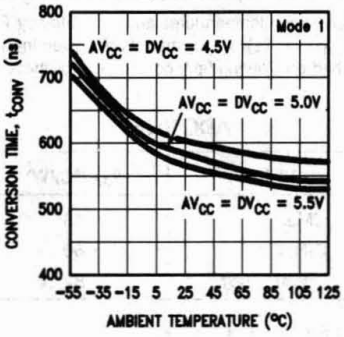
Analog Supply Current vs Temperature



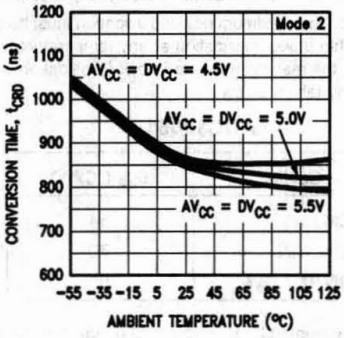
Digital Supply Current vs Temperature



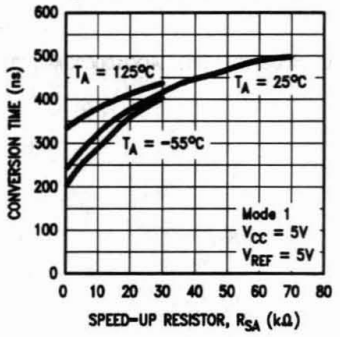
Conversion Time vs Temperature



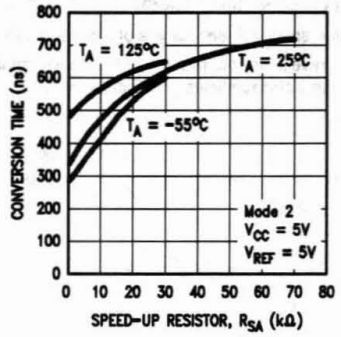
Conversion Time vs Temperature



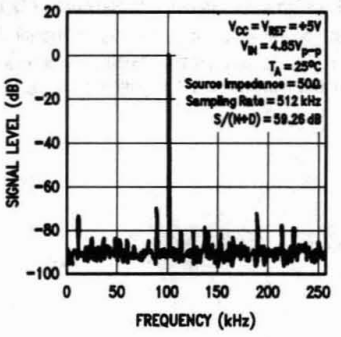
Conversion Time vs Speed-Up Resistor (ADC10062 and ADC10064 Only)



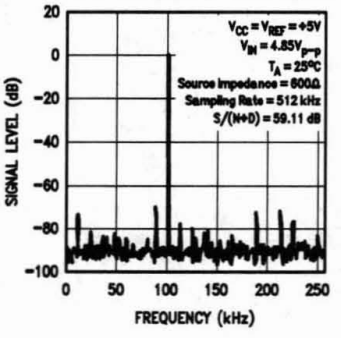
Conversion Time vs Speed-Up Resistor (ADC10062 and ADC10064 Only)



Spectral Response with 100 kHz Sine Wave Input



Spectral Response with 100 kHz Sine Wave Input



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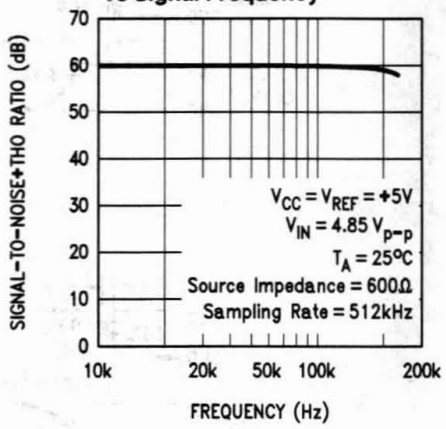
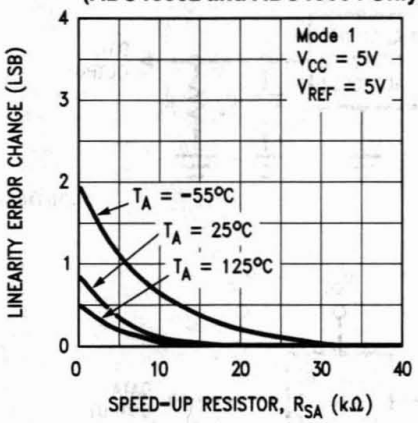
Typical Performance Characteristics (Continued)

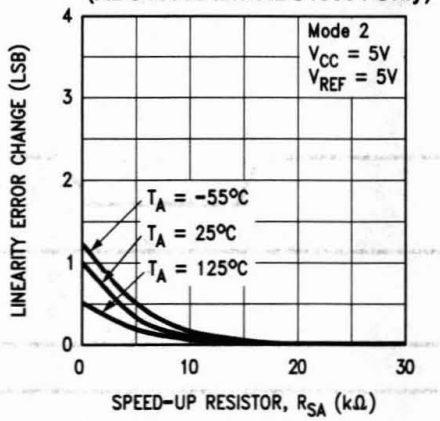
Signal-to-Noise + THD Ratio vs Signal Frequency



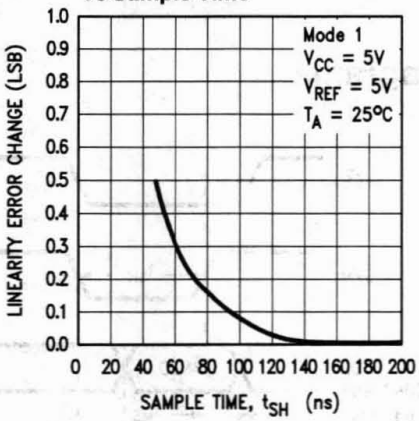
Linearity Change vs Speed-Up Resistor (ADC10062 and ADC10064 Only)



Linearity Change vs Speed-Up Resistor (ADC10062 and ADC10064 Only)



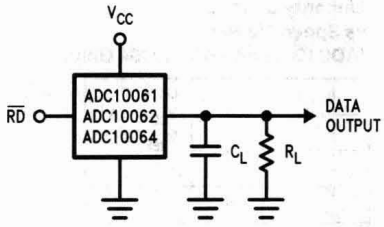
Linearity Error Change vs Sample Time



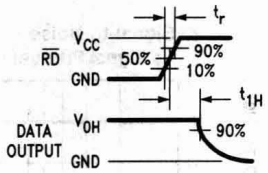
TL/H/11020–4

2

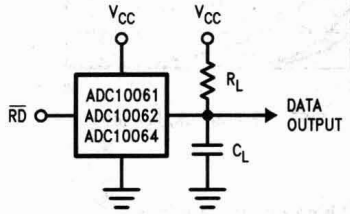
TRI-STATE Test Circuits and Waveforms



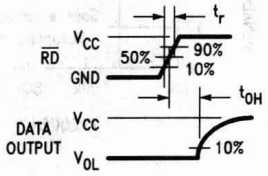
TL/H/11020–5



TL/H/11020–6

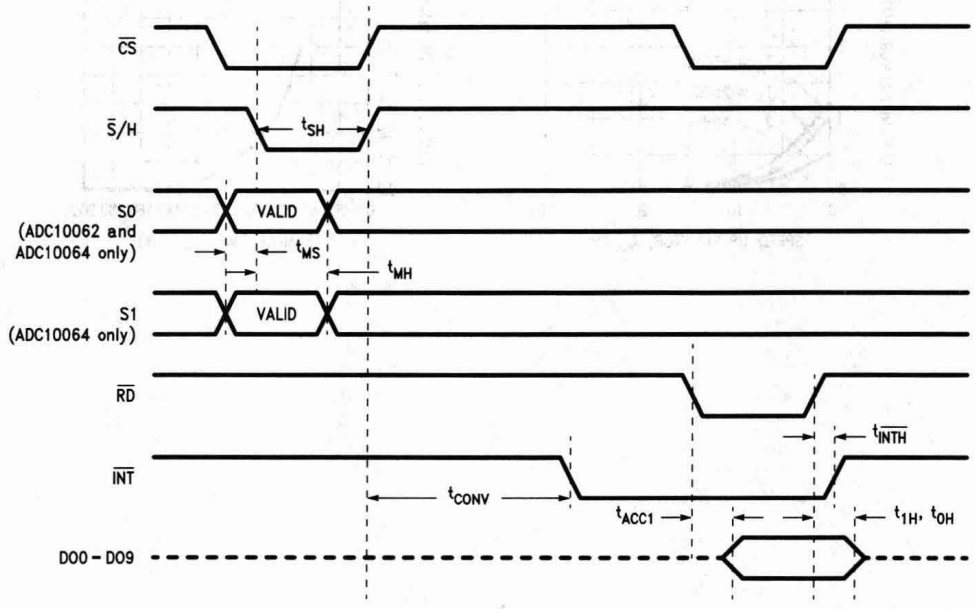


TL/H/11020–7



TL/H/11020–8

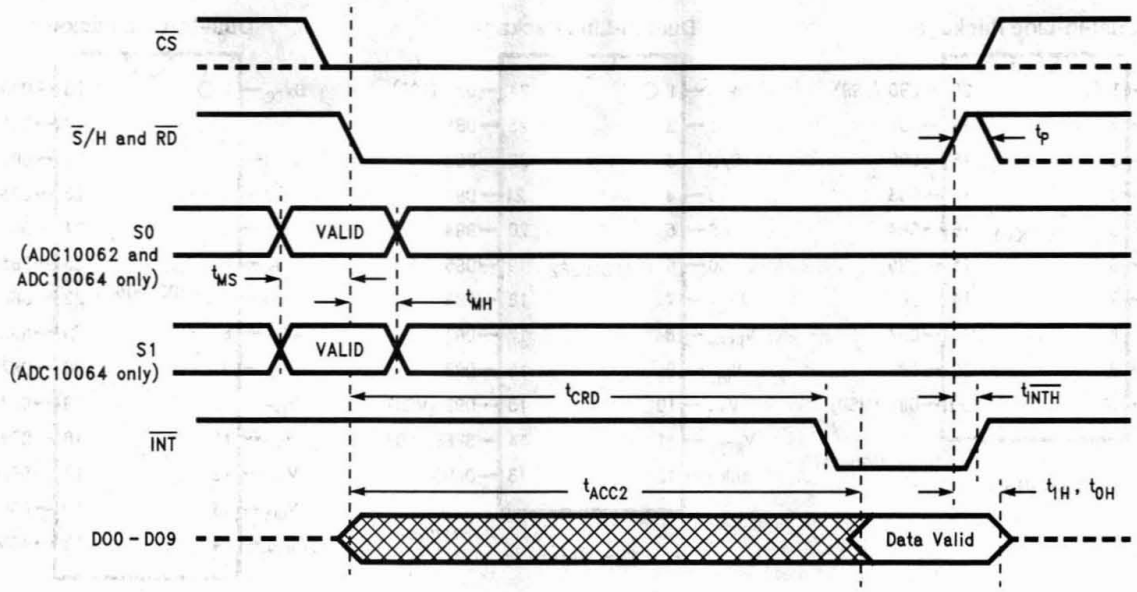
Timing Diagrams



TL/H/11020–9

FIGURE 1. Mode 1. The conversion time (t_{CONV}) is set by the internal timer.

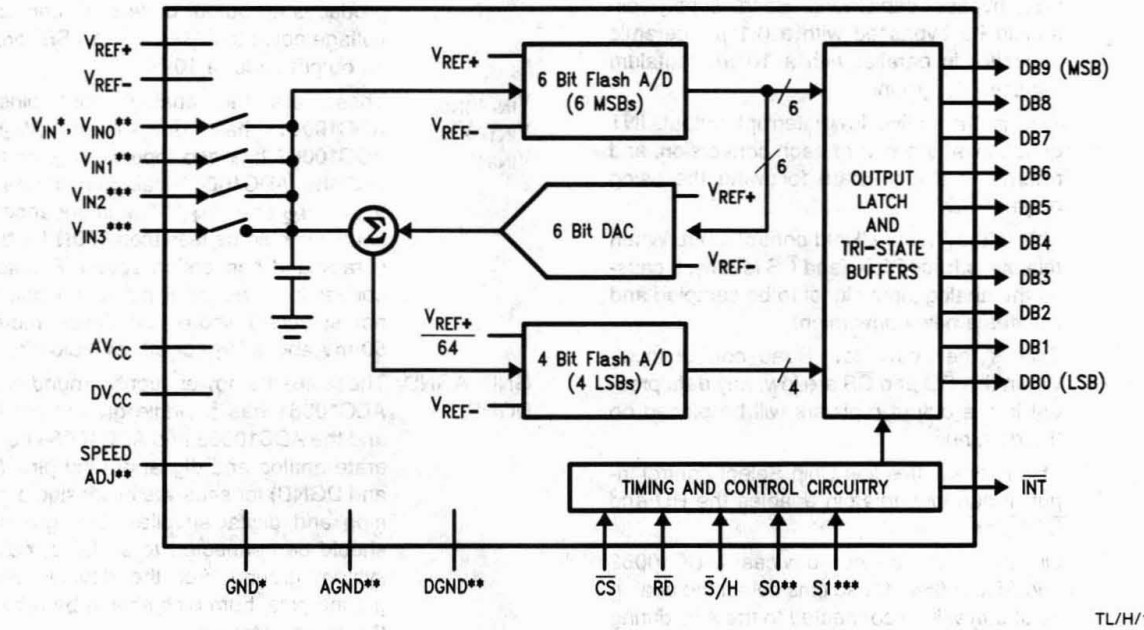
Timing Diagrams (Continued)



TL/H/11020–10

FIGURE 2. Mode 2 ($\overline{RD}$ Mode). The conversion time (t_{CRD}) includes the sampling time and is determined by the internal timer.

Simplified Block Diagram

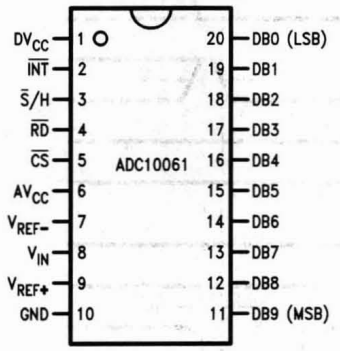


TL/H/11020–1

*ADC10061 Only
**ADC10062 and ADC10064 Only
***ADC10064 Only

Connection Diagrams

Dual-In-Line Package



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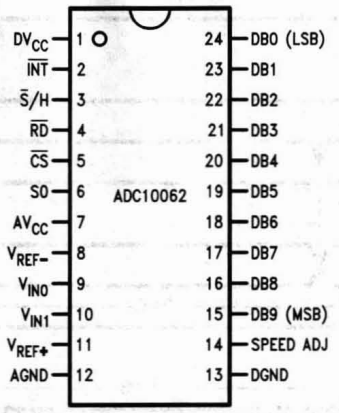
Top View

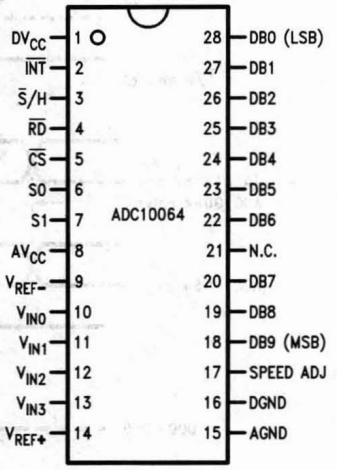
Dual-In-Line Package



TL/H/11020–12

Top View

Dual-In-Line Package



TL/H/11020–13

Top View

Pin Descriptions

DV_{CC}, AV_{CC} These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}/H$ This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}/H$ pins.

S0, S1 On the multiple-input devices (ADC10062 and ADC10064), these pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}/H$ makes its High-to-Low transition (See the Timing Diagrams). The ADC10064 includes both S0 and S1. The ADC10062 includes just S0, and the ADC10061 includes neither.

V_{REF-}, V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to (V_{REF+} − 1 LSB) produces an output code of 1023.

V_{IN}, V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3} These are the analog input pins. The ADC10061 has one input (V_{IN}), the ADC10062 has two inputs (V_{IN0} and V_{IN1}), and the ADC10064 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND These are the power supply ground pins. The ADC10061 has a single ground pin (GND), and the ADC10062 and ADC10064 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. For the devices with two ground pins, both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE output pins.

SPEED ADJ (ADC10062 and ADC10064 only). This pin is normally left unconnected, but by connecting a resistor between this pin and ground, the conversion time can be reduced. See the Typical Performance Curves and the table of Electrical Characteristics.

Functional Description

The ADC10061, ADC10062 and ADC10064 digitize an analog input signal to 10 bits accuracy by performing two lower-resolution "flash" conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits LSBs).

Figure 3 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024 the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has 1/8 of the total reference voltage across it, and each of the LSB resistors has 1/64 of the total reference voltage across it. Tap points across these resistors can be connected, in groups of sixteen, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between V_{REF+} and V_{REF-}. Six comparators compare the input voltage with the tap voltages on this resistor string to provide a low-resolution "estimate" of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator MUX to connect the 16 comparators to the taps on the MSB ladder between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data—four bits in the flash itself, and 2 bits in the estimator.

The remaining four LSBs are now determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second, four-bit flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the multistep conversion technique used in the ADC10061, ADC10062, and ADC10064 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC10061, ADC10062, and ADC10064 to perform high-speed conversions without excessive power drain.

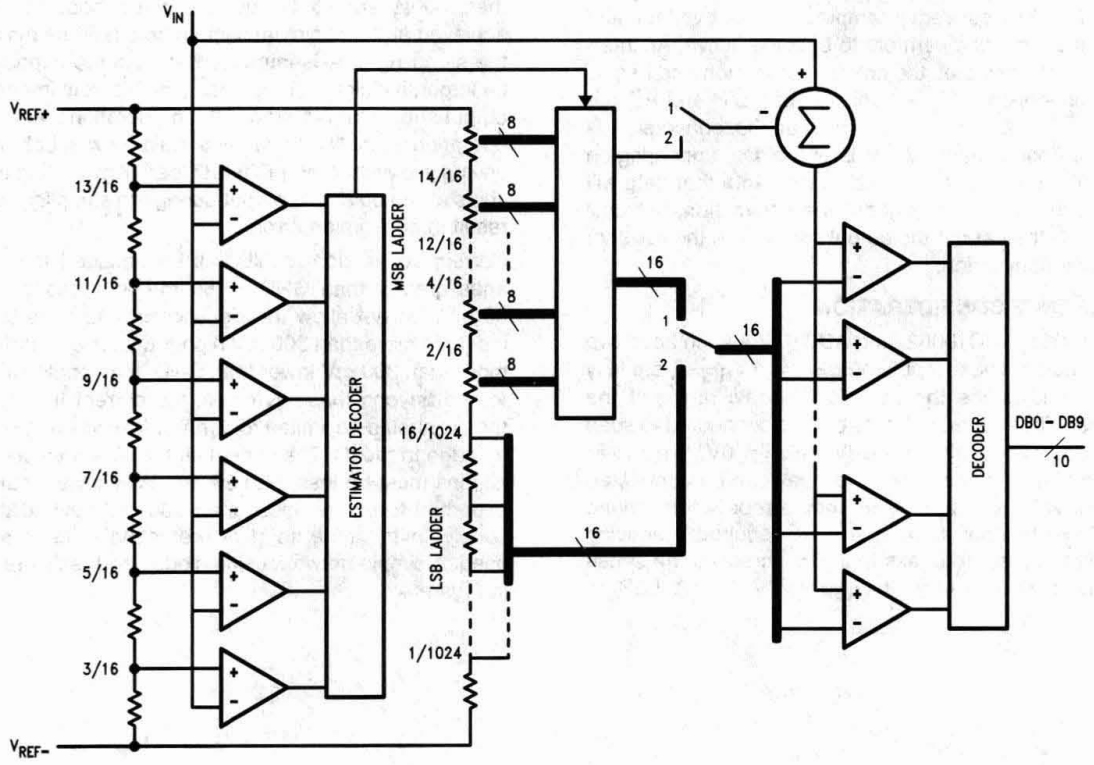


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FIGURE 3. Block Diagram of the Multistep Converter Architecture

Applications Information

1.0 MODES OF OPERATION

The ADC10061, ADC10062, and ADC10064 have two basic digital interface modes. *Figure 1* and *Figure 2* are timing diagrams for the two modes. The ADC10062 and ADC10064 have input multiplexers that are controlled by the logic levels on pins S_0 and S_1 when $\overline{S}/H$ goes low. Table I is a truth table showing how the input channnels are assigned.

Mode 1

In this mode, the $\overline{S}/H$ pin controls the start of conversion. $\overline{S}/H$ is pulled low for a minimum of 250 ns. This causes the comparators in the "coarse" flash converter to become active. When $\overline{S}/H$ goes high, the result of the coarse conversion is latched and the "fine" conversion begins. After 600 ns (typical), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}/H$ or $\overline{RD}$. $\overline{CS}$ is internally "ANDed" with $\overline{S}/H$ and $\overline{RD}$; the input voltage is sampled when $\overline{CS}$ and $\overline{S}/H$ are low, and data is read when $\overline{CS}$ and $\overline{RD}$ are low. $\overline{INT}$ is reset high on the rising edge of $\overline{RD}$.

TABLE I. Input Multiplexer Programming

ADC10064

S_1	S_0	Channel
0	0	V_{IN0}
0	1	V_{IN1}
1	0	V_{IN2}
1	1	V_{IN3}

(a)

ADC10062

S_0	Channel
0	V_{IN0}
1	V_{IN1}

(b)

Mode 2

In Mode 2, also called "$\overline{RD}$ mode", the $\overline{S}/H$ and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The A/D converter samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion. 850 ns (typical) after $\overline{S}/H$ and $\overline{RD}$ are pull low, $\overline{INT}$ goes low, indicating that the conversion is completed. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but until $\overline{INT}$ goes low the data at the output pins will be the result of the previous conversion.

2.0 REFERENCE CONSIDERATIONS

The ADC10061, ADC10062, and ADC10064 each have two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range (V_{REF-} = 0V, V_{REF+} = V_{CC}) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required. Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if V_{REF} = 2V, then 1 LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See the Typical Performance Curves for more information. For this reason, reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC10061, ADC10062, and ADC10064. V_{REF-} can be connected to a voltage other than ground as long as the voltage source connected to this pin is capable of sinking the converter's reference current (12.5 mA Max @ V_{REF} = 5V). If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should be bypassed with a 10 μF tantalum and a 0.1 μF ceramic.

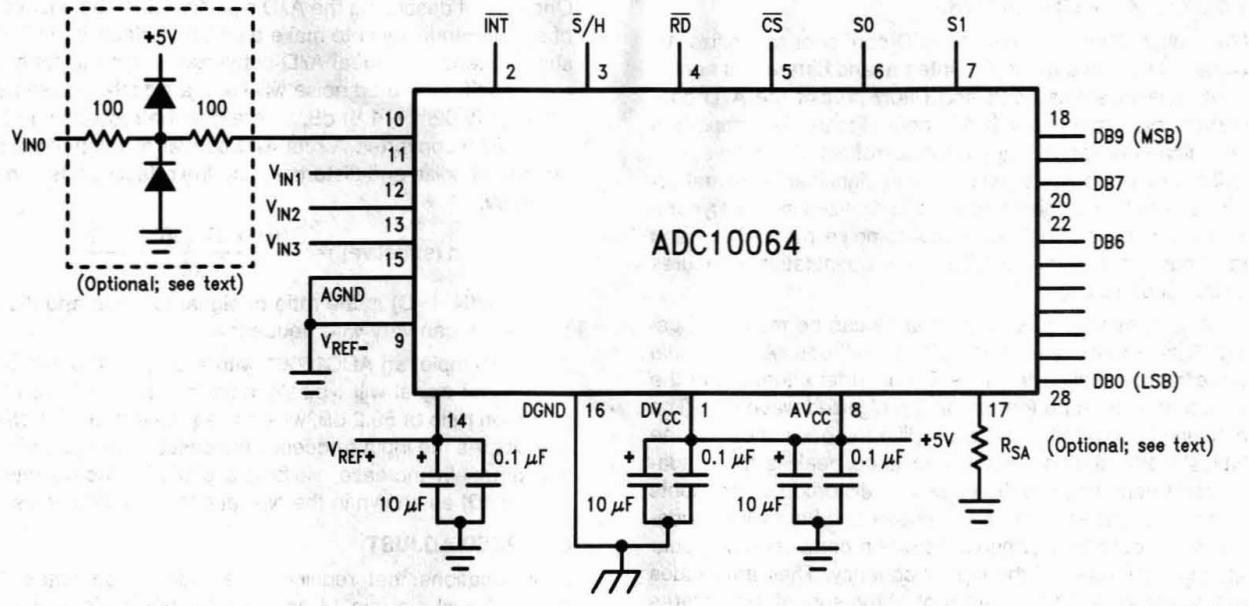
3.0 THE ANALOG INPUT

The ADC10061, ADC10062, and ADC10064 sample the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can therefore be observed at the analog input during normal operation. These spikes are normal and do not degrade the converter's performance.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (250 ns maximum). If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than AV_{CC} and DV_{CC}, or more than 300 mV lower than GND. If an analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 20 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits, some sourt of protection scheme should be used. A simple network using diodes and resistors is shown in *Figure 4*.

Applications Information (Continued)



TL/H/11020–15

FIGURE 4. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. If V_{REF-} is not grounded, it should also be bypassed to analog ground using multiple capacitors (see 5.0 "Power Supply Considerations"). AGND and DGND should be at the same potential. V_{IN0} is shown with an input protection network. Pin 17 is normally left open, but optional "speedup" resistor R_{SA} can be used to reduce the conversion time.

4.0 INHERENT SAMPLE-AND-HOLD

Because the ADC10061, ADC10062, and ADC10064 sample the input signal once during each conversion, they are capable of measuring relatively fast input signals without the help of an external sample-hold. In a non-sampling successive-approximation A/D converter, regardless of speed, the input signal must be stable to better than ±1/2 LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion if a SAR with no internal sample-and-hold is used.

Because they incorporate a direct sample/hold control input, the ADC10061, ADC10062, and ADC10064 are suitable for use in DSP-based systems. The $\overline{S}/H$ input allows synchronization of the A/D converter to the DSP system's sampling rate and to other ADC10061s, ADC10062s, and ADC10064s.

The ADC10061, ADC10062, and ADC10064 can perform accurate conversions of input signals with frequency components from DC to over 160 kHz.

5.0 POWER SUPPLY CONSIDERATIONS

The ADC10061, ADC10062, and ADC10064 are designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor. Depending on the circuit board layout and other system considerations, more bypassing may be necessary.

The ADC10061 has a single ground pin, and the ADC10062 and ADC10064 each have separate analog and digital ground pins for separate bypassing of the analog and digital supplies. The devices with separate analog and digital ground pins should have their ground pins connected to the same potential, and all grounds should be "clean" and free of noise.

In systems with multiple power supplies, careful attention to power supply sequencing may be necessary to avoid overdriving inputs. The A/D converter's power supply pins should be at the proper voltage before digital or analog signals are applied to any of the other pins.

6.0 LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC10061, ADC10062, and ADC10064, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome, so digital grounds should always be separate from analog grounds. For best performance, separate ground planes should be provided for the digital and analog parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

Applications Information (Continued)

7.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but conventional DC integral and differential nonlinearity specifications don't accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), are quantitative measures of this capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. The resulting spectral plot might look like the ones shown in the typical performance curves. The large peak is the fundamental frequency, and the noise and distortion components (if any are present) are visible above and below the fundamental frequency. Harmonic distortion components appear at whole multiples of the input frequency. Their amplitudes are combined as the square root of the sum of the squares and compared to the fundamental amplitude to yield the THD specification. Typical values for THD are given in the table of Electrical Characteristics.

Signal-to-noise ratio is the ratio of the amplitude at the fundamental frequency to the rms value at all other frequencies, excluding any harmonic distortion components. Typical values are given in the Electrical Characteristics table. An alternative definition of signal-to-noise ratio includes the distortion components along with the random noise to yield a signal-to-noise-plus-distortion ration, or S/(N + D).

The THD and noise performance of the A/D converter will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies.

One way of describing the A/D's performance as a function of signal frequency is to make a plot of "effective bits" versus frequency. An ideal A/D converter with no linearity errors or self-generated noise will have a signal-to-noise ratio equal to (6.02n + 1.8) dB, where n is the resolution in bits of the A/D converter. A real A/D converter will have some amount of noise and distortion, and the effective bits can be found by:

$$n\ (\text{effective}) = \frac{S/(N + D)\ (\text{dB}) - 1.8}{6.02}$$

where S/(N + D) is the ratio of signal to noise and distortion, which can vary with frequency.

As an example, an ADC10061 with a 5 V_{P-P}, 100 kHz sine wave input signal will typically have a signal-to-noise-plus-distortion ratio of 59.2 dB, which is equivalent to 9.53 effective bits. As the input frequency increases, noise and distortion gradually increase, yielding a plot of effective bits or S/(N + D) as shown in the typical performance curves.

8.0 SPEED ADJUST

In applications that require faster conversion times, the Speed Adjust pin (pin 14 on the ADC10062, pin 17 on the ADC10064) can significantly reduce the conversion time. The speed adjust pin is connected to an on-chip current source that determines the converter's internal timing. By connecting a resistor between the speed adjust pin and ground as shown in *Figure 4*, the internal programming current is increased, which reduces the conversion time. As an example, an 18k resistor reduces the conversion time of a typical part from 600 ns to 350 ns with no significant effect on linearity. Using smaller resistors to further decrease the conversion time is possible as well, although the linearity will begin to degrade somewhat (see curves). Note that the resistor value needed to obtain a given conversion time will vary from part to part, so this technique will generally require some "tweaking" to obtain satisfactory results.

National Semiconductor

ADC10461/ADC10462/ADC10464 10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep* conversion technique, the 10-bit ADC10461, ADC10462, and ADC10464 CMOS analog-to-digital converters offer sub-microsecond conversion times yet dissipate a maximum of only 235 mW. The ADC10461, ADC10462, and ADC10464 perform a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. Dynamic performance (THD, S/N) is guaranteed. The ADC10461 is pin-compatible with the ADC1061 but much faster, thus providing a convenient upgrade path for the ADC1061.

The analog input voltage to the ADC10461, ADC10462, and ADC10464 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 200 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10462 and ADC10464 include a "speed-up" pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 350 ns with only a small increase in linearity error.

For ease of interface to microprocessors, the ADC10461, ADC10462, and ADC10464 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Features

- Built-in sample-and-hold
- Single +5V supply
- 1, 2, or 4-input multiplexer options
- No external clock required
- Speed adjust pin for faster conversions (ADC10462 and ADC10464)

Key Specifications

- Conversion time to 10 bits — 600 ns typical, 900 ns max over temperature
- Sampling Rate — 800 kHz
- Low power dissipation — 235 mW (max)
- Total harmonic distortion (50 kHz) — −60 dB (max)
- No missing codes over temperature

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Ordering Information

ADC10461

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10461CIN	N20A Molded DIP
ADC10461CIWM	M20B Small Outline

ADC10462

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10462CIN	N24A Molded DIP
ADC10462CIWM	M24B Small Outline

ADC10464

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10464CIN	N28B Molded DIP
ADC10464CIWM	M28B Small Outline

*U.S. Patent Number 4918449

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)	−0.3V to +6V
Voltage at Any Input or Output	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	875 mW
ESD Susceptability (Note 5)	2000V
Soldering Information (Note 6)	
N Package (10 Sec)	260°C
SO Package:	
Vapor Phase (60 Sec)	215°C
Infrared (15 Sec)	220°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10461CIN, ADC10461CIWM, ADC10462CIN, ADC10462CIWM, ADC10464CIN, ADC10464CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage Range	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = +5V$, $V_{REF(-)}$ = GND, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{Min}$ to T_{Max};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
	Resolution			**10**	Bits
	Integral Linearity Error	$R_{SA} \ge 18\ k\Omega$	±0.5		LSB
	Offset Error			**±1**	LSB (max)
	Full-Scale Error			**±1**	LSB (max)
	Total Unadjusted Error	$R_{SA} \ge 18\ k\Omega$	±0.5		LSB
	Missing Codes			**0**	(max)
	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.5V$ $V^+ = 5V \pm 10\%$, $V_{REF} = 4.5V$	±1/16 ±1/8		LSB LSB
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P} f_{IN} = 240 kHz, 4.85 V_{P-P}	**−68** **−66** **−62** **−58**	**−60**	dB dB (max) dB dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P}	**61** **60** **60**	**58**	dB dB (min) dB
ENOB	Effective Number of Bits	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P}	**9.6** **9.5**	**9**	Bits Bits (min)
R_{REF}	Reference Resistance		650	**400**	Ω (min)
R_{REF}	Reference Resistance		650	**900**	Ω (max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(+)}$**	V (max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (max)
V_{IN}	Input Voltage			**GND − 0.05**	V (min)
	OFF Channel Input Leakage Current ON Channel Input Leakage Current	$\overline{CS} = V^+$, $V_{IN} = V^+$ $\overline{CS} = V^+$, $V_{IN} = V^+$	0.01 ±1	**3** **−3**	μA (max) μA (max)

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = 5V$ $V_{REF(-)} = GND$, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN(1)} = 5V$	0.005	**3.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN(0)}$ 0V	−0.005	**−3.0**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = -360\ \mu A$ $V^+ = 4.5V$, $I_{OUT} = -10\ \mu A$		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 5V$ $V_{OUT} = 0V$	0.1 −0.1	**50** **−50**	μA (max) μA (max)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = \infty$ $\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = 18\ k\Omega$	1.0 1.0	**2**	mA (max) mA (max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = \infty$ $\overline{CS} = \overline{S}/H = \overline{RD} = 0$, $R_{SA} = 18\ k\Omega$	30 30	**45**	mA (max) mA (max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{CONV}	Mode 1 Conversion Time from Rising Edge of $\overline{S}/H$ to Falling Edge of $\overline{INT}$	CIN, CIWM Suffixes $R_{SA} = 18k$	 600 375	 750/**900**	 ns (max) ns
t_{CRD}	Mode 2 Conversion Time	CIN, CIWM Suffixes Mode 2, $R_{SA} = 18k$	 850 530	 **1400**	 ns (max) ns
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; $C_L = 100$ pF	30	**60**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; $C_L = 100$ pF	900	t_{CRD} + **50**	ns (max)
t_{SH}	Minimum Sample Time	*(Figure 1)*; (Note 9)		**250**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	$R_L = 1k$, $C_L = 10$ pF	30	**60**	ns (max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 100$ pF	25	**50**	ns (max)
t_P	Delay from End of Conversion to Next Conversion			**50**	ns (max)

2

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, and Speed Adjust pin unconnected unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{MS}	Multiplexer Control Setup Time		10	**75**	ns (max)
t_{MH}	Multiplexer Hold Time		10	**40**	ns (max)
C_{VIN}	Analog Input Capacitance		35		pF (max)
C_{OUT}	Logic Output Capacitance		5		pF (max)
C_{IN}	Logic Input Capacitance		5		pF (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditons.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. In most cases, the maximum derated power dissipation will be reached only during fault conditions. For these devices, T_{JMAX} for a board-mounted device can be found from the tables below:

ADC10461

Suffix	θ_{JA} (°C/W)
CIN	70
CIWM	85

ADC10462

Suffix	θ_{JA} (°C/W)
CIN	60
CIWM	82

ADC10464

Suffix	θ_{JA} (°C/W)
CIN	53
CIWM	78

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

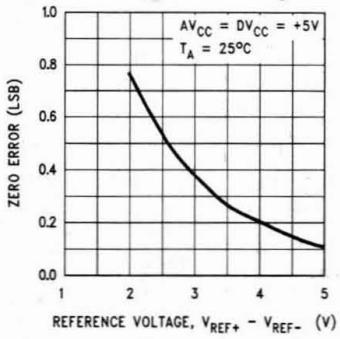
Note 7: Typicals represent most likely parametric norm.

Note 8: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

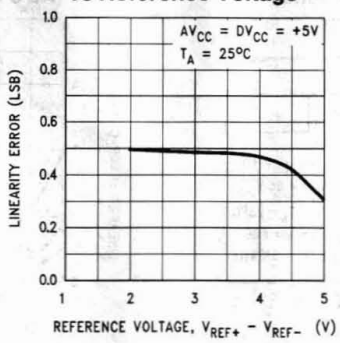
Note 9: Accuracy may degrade if t_{SH} is shorter than the value specified. See curves of Accuracy vs t_{SH}.

Typical Performance Characteristics

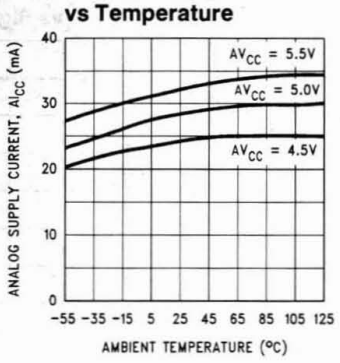
Zero (Offset) Error vs Reference Voltage



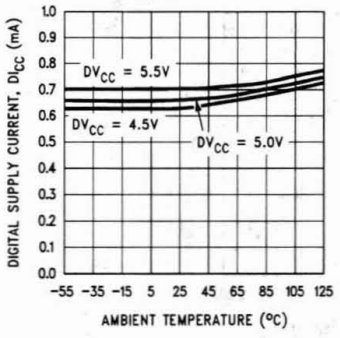
Linearity Error vs Reference Voltage



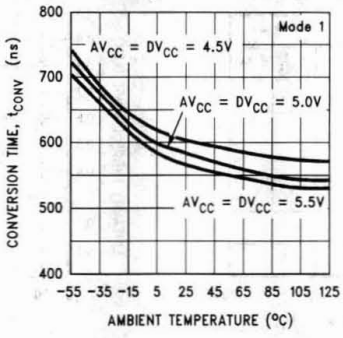
Analog Supply Current vs Temperature



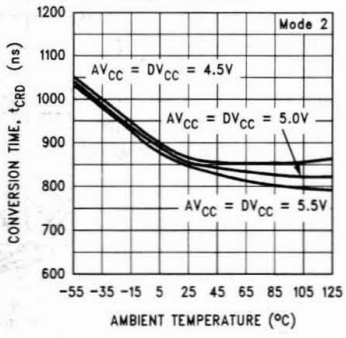
Digital Supply Current vs Temperature



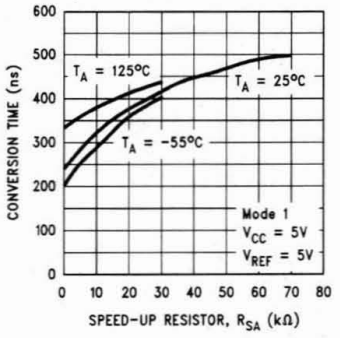
Conversion Time vs Temperature



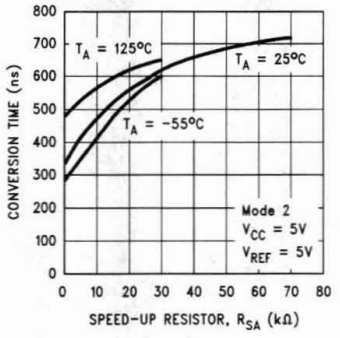
Conversion Time vs Temperature



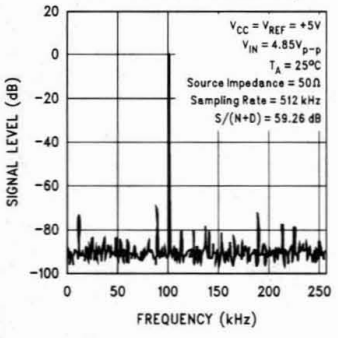
Conversion Time vs Speed-Up Resistor (ADC10462 and ADC10464 Only)



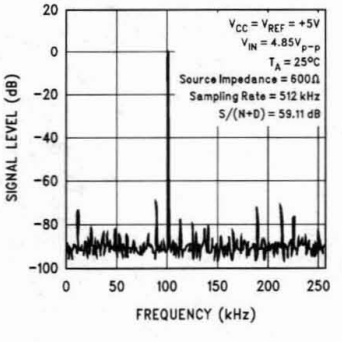
Conversion Time vs Speed-Up Resistor (ADC10462 and ADC10464 Only)



Spectral Response with 100 kHz Sine Wave Input



Spectral Response with 100 kHz Sine Wave Input



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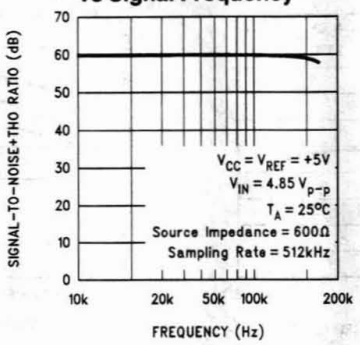
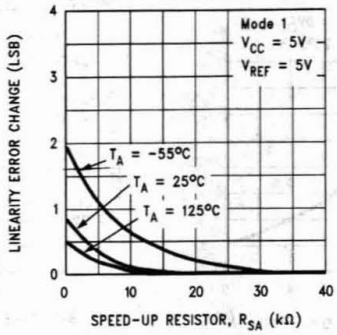
Typical Performance Characteristics (Continued)

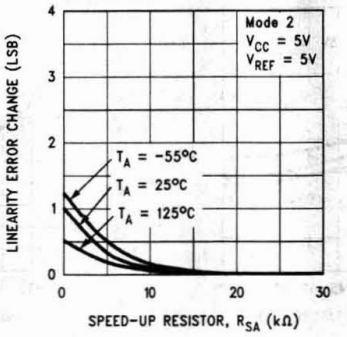
Signal-to-Noise + THD Ratio vs Signal Frequency



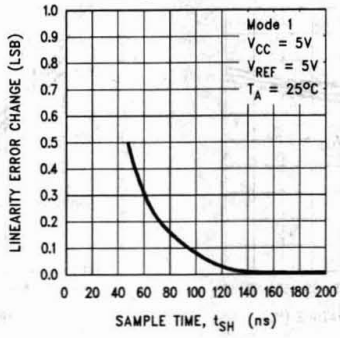
Linearity Change vs Speed-Up Resistor (ADC10462 and ADC10464 Only)



Linearity Change vs Speed-Up Resistor (ADC10462 and ADC10464 Only)

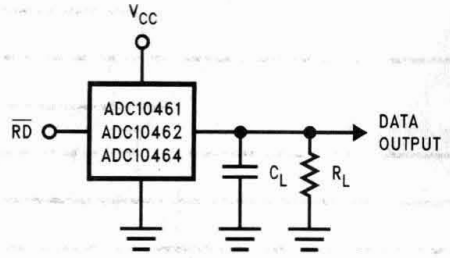


Linearity Error Change vs Sample Time

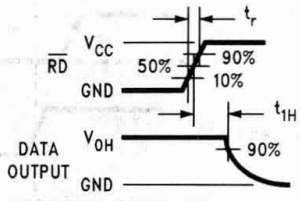


TL/H/11108–2

TRI-STATE Test Circuits and Waveforms



TL/H/11108–3



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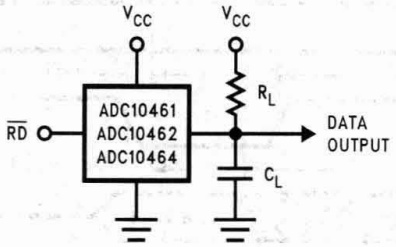

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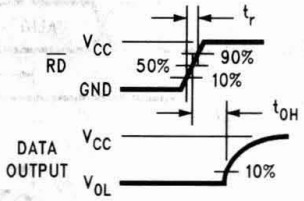
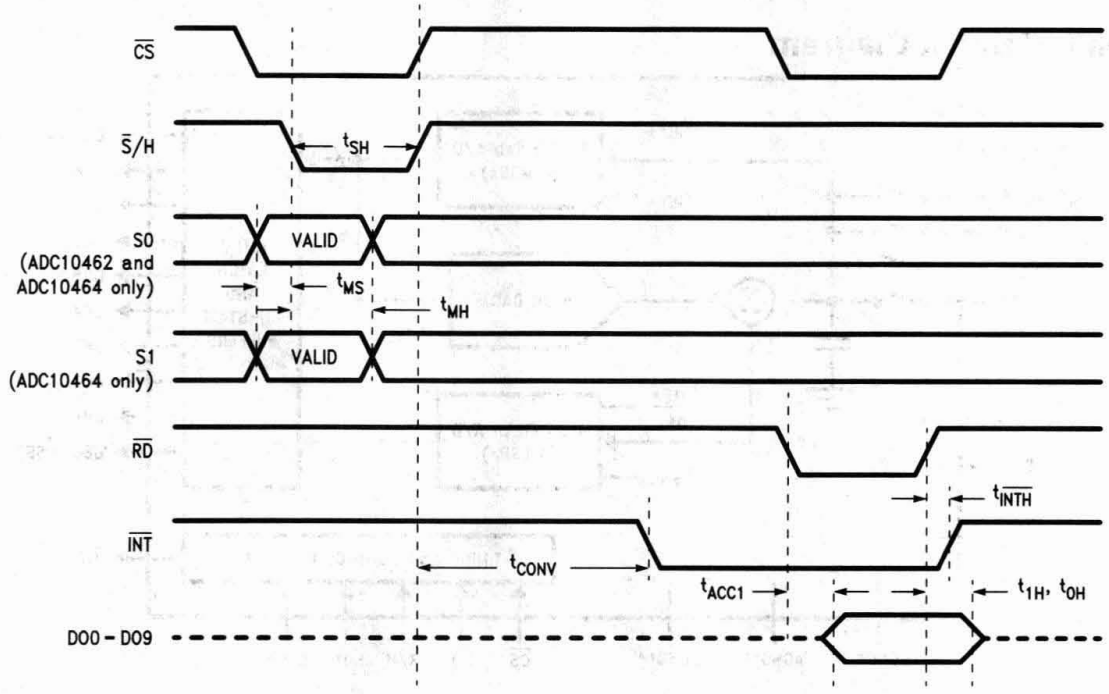


TL/H/11108–6

Timing Diagrams



TL/H/11108–7

FIGURE 1. Mode 1. The conversion time (t_{CONV}) is set by the internal timer.

Timing Diagrams (Continued)

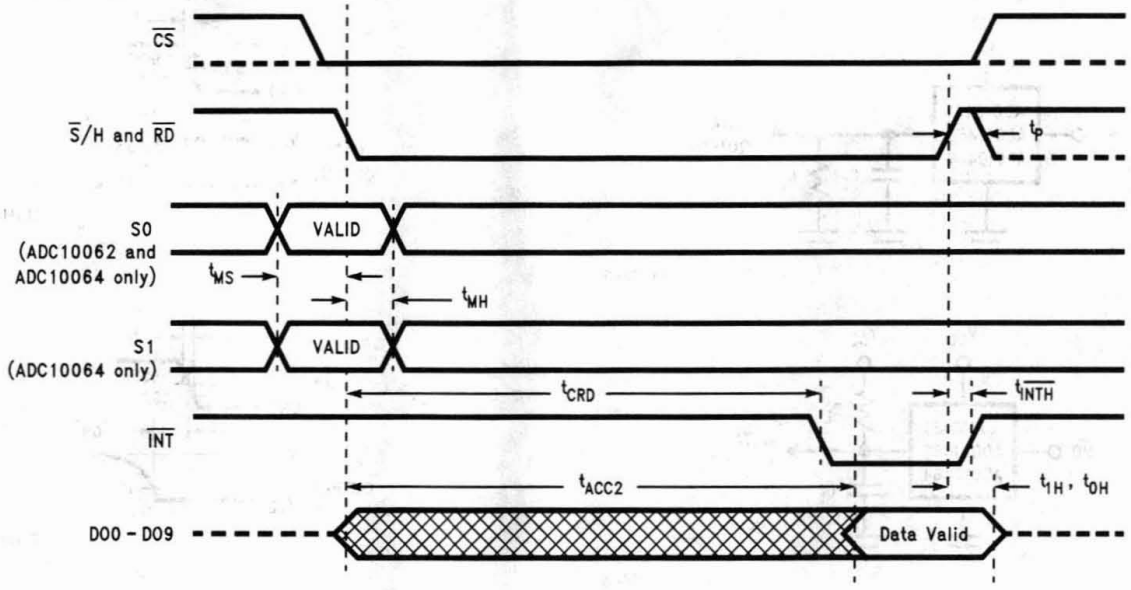


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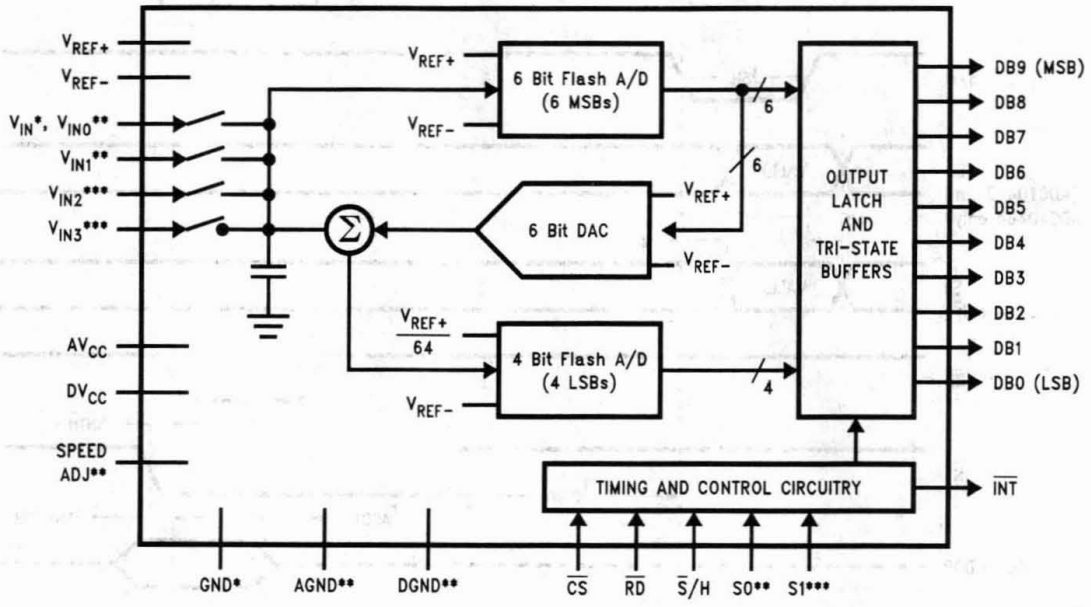
FIGURE 2. Mode 2 ($\overline{RD}$ Mode). The conversion time (t_{CRD}) includes the sampling time and is determined by the internal timer.

Simplified Block Diagram

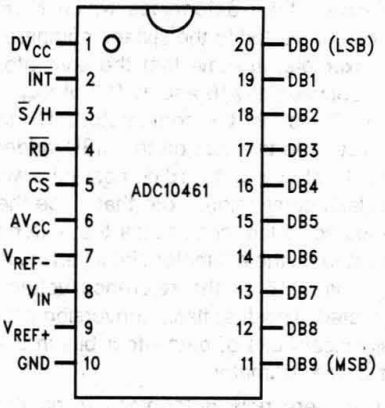


TL/H/11108–9

*ADC10461 Only
**ADC10462 and ADC10464 Only
***ADC10464 Only

Connection Diagrams

Dual-In-Line Package



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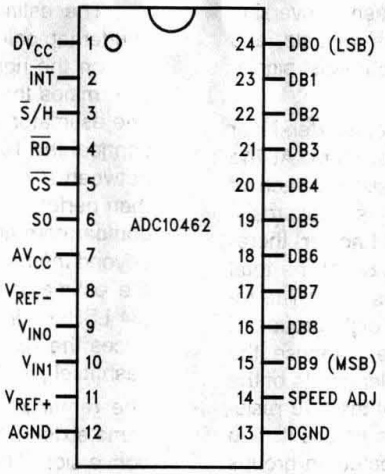
Top View

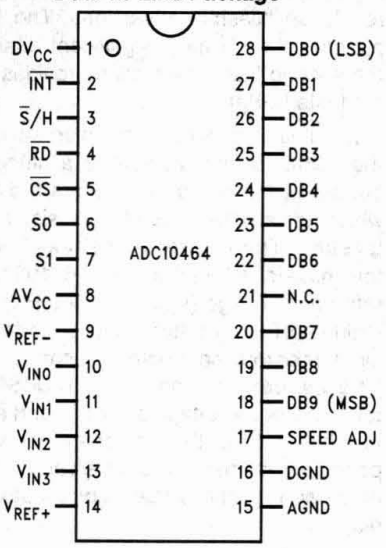
Dual-In-Line Package



TL/H/11108–11

Top View

Dual-In-Line Package



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Top View

Pin Descriptions

DV_{CC}, AV_{CC} These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}$/H This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}$/H pins.

S0, S1 On the multiple-input devices (ADC10462 and ADC10464), these pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}$/H makes its High-to-Low transition (See the Timing Diagrams). The ADC10464 includes both S0 and S1. The ADC10462 includes just S0, and the ADC10461 includes neither.

$V_{REF}-$, $V_{REF}+$ These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but $V_{REF}+$ must be greater than $V_{REF}-$. An input voltage equal to $V_{REF}-$ produces an output code of 0, and an input voltage equal to ($V_{REF}+$ − 1 LSB) produces an output code of 1023.

V_{IN}, V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3} These are the analog input pins. The ADC10461 has one input (V_{IN}), the ADC10462 has two inputs (V_{IN0} and V_{IN1}), and the ADC10464 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND These are the power supply ground pins. The ADC10461 has a single ground pin (GND), and the ADC10462 and ADC10464 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. For the devices with two ground pins, both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE output pins.

SPEED ADJ (ADC10462 and ADC10464 only). This pin is normally left unconnected, but by connecting a resistor between this pin and ground, the conversion time can be reduced. See the Typical Performance Curves and the table of Electrical Characteristics.

2

Functional Description

The ADC10461, ADC10462 and ADC10464 digitize an analog input signal to 10 bits accuracy by performing two lower-resolution "flash" conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits LSBs).

Figure 3 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024 the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has 1/8 of the total reference voltage across it, and each of the LSB resistors has 1/64 of the total reference voltage across it. Tap points across these resistors can be connected, in groups of sixteen, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between V_{REF+} and V_{REF-}. Six comparators compare the input voltage with the tap voltages on this resistor string to provide a low-resolution "estimate" of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator MUX to connect the 16 comparators to the taps on the MSB ladder between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data—four bits in the flash itself, and 2 bits in the estimator.

The remaining four LSBs are now determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second, four-bit flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the multistep conversion technique used in the ADC10461, ADC10462, and ADC10464 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC10461, ADC10462, and ADC10464 to perform high-speed conversions without excessive power drain.

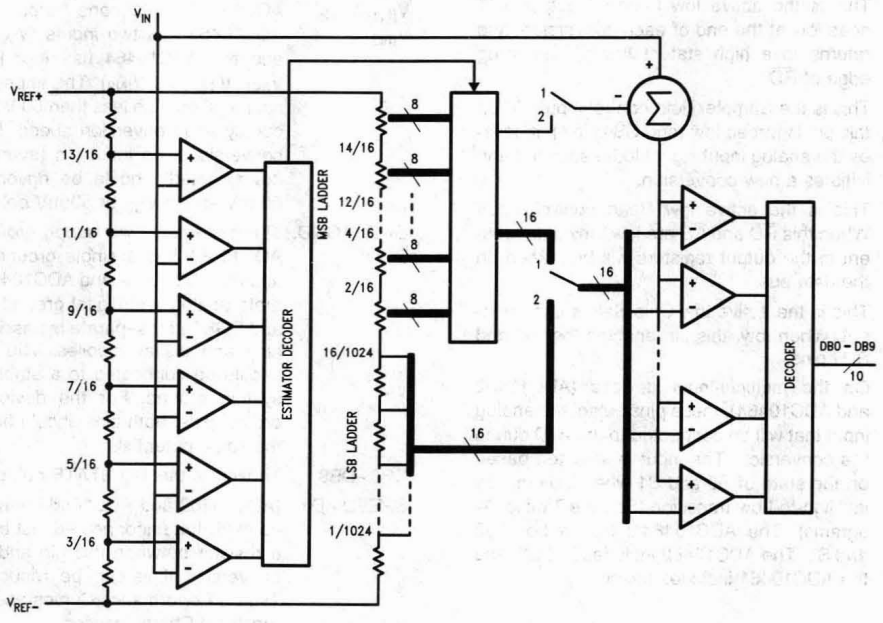

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FIGURE 3. Block Diagram of the Multistep Converter Architecture

Applications Information

1.0 MODES OF OPERATION

The ADC10461, ADC10462, and ADC10464 have two basic digital interface modes. *Figure 1* and *Figure 2* are timing diagrams for the two modes. The ADC10462 and ADC10464 have input multiplexers that are controlled by the logic levels on pins S_0 and S_1 when $\overline{S}/H$ goes low. Table I is a truth table showing how the input channnels are assigned.

Mode 1

In this mode, the $\overline{S}/H$ pin controls the start of conversion. $\overline{S}/H$ is pulled low for a minimum of 250 ns. This causes the comparators in the "coarse" flash converter to become active. When $\overline{S}/H$ goes high, the result of the coarse conversion is latched and the "fine" conversion begins. After 600 ns (typical), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}/H$ or $\overline{RD}$. $\overline{CS}$ is internally "ANDed" with $\overline{S}/H$ and $\overline{RD}$; the input voltage is sampled when $\overline{CS}$ and $\overline{S}/H$ are low, and data is read when $\overline{CS}$ and $\overline{RD}$ are low. $\overline{INT}$ is reset high on the rising edge of $\overline{RD}$.

TABLE I. Input Multiplexer Programming

ADC10464

S_1	S_0	Channel
0	0	V_{IN0}
0	1	V_{IN1}
1	0	V_{IN2}
1	1	V_{IN3}

(a)

ADC10462

S_0	Channel
0	V_{IN0}
1	V_{IN1}

(b)

Mode 2

In Mode 2, also called "$\overline{RD}$ mode", the $\overline{S}/H$ and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The A/D converter samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion. 850 ns (typical) after $\overline{S}/H$ and $\overline{RD}$ are pull low, $\overline{INT}$ goes low, indicating that the conversion is completed. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but until $\overline{INT}$ goes low the data at the output pins will be the result of the previous conversion.

2.0 REFERENCE CONSIDERATIONS

The ADC10461, ADC10462, and ADC10464 each have two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range (V_{REF-} = 0V, V_{REF+} = V_{CC}) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required. Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if V_{REF} = 2V, then 1 LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See the Typical Performance Curves for more information. For this reason, reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC10461, ADC10462, and ADC10464. V_{REF-} can be connected to a voltage other than ground as long as the voltage source connected to this pin is capable of sinking the converter's reference current (12.5 mA Max @ V_{REF} = 5V). If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should be bypassed with a 10 μF tantalum and a 0.1 μF ceramic.

3.0 THE ANALOG INPUT

The ADC10461, ADC10462, and ADC10464 sample the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can therefore be observed at the analog input during normal operation. These spikes are normal and do not degrade the converter's performance.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (250 ns maximum). If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than AV_{CC} and DV_{CC}, or more than 300 mV lower than GND. If an analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 20 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits, some sourt of protection scheme should be used. A simple network using diodes and resistors is shown in *Figure 4*.

Applications Information (Continued)

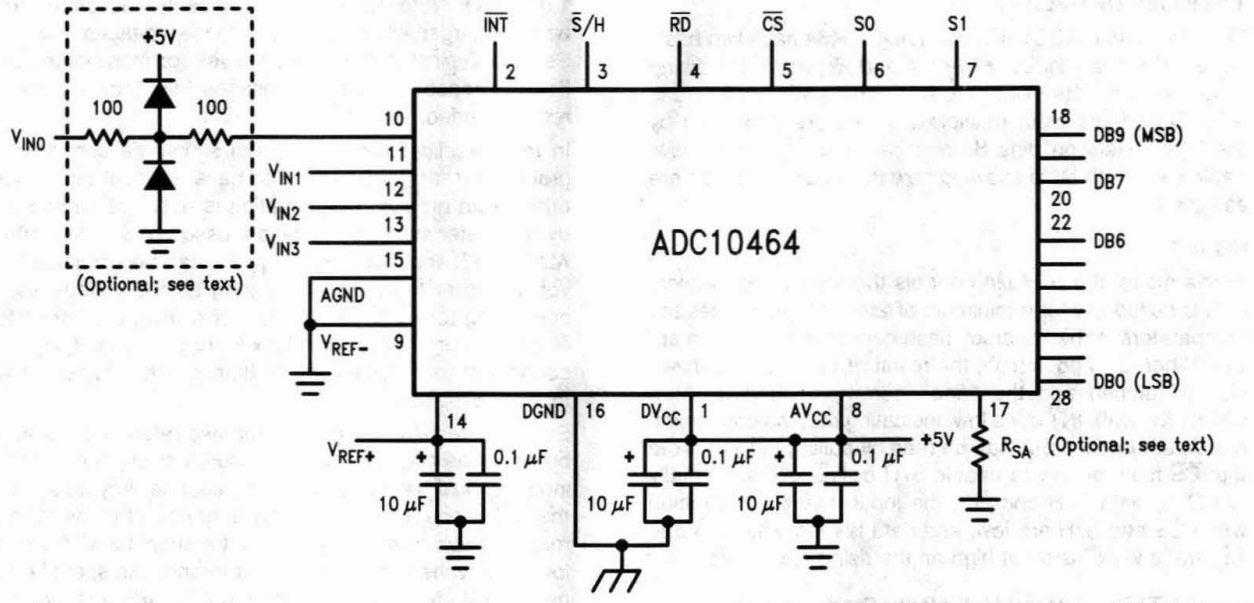

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FIGURE 4. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. If V_{REF-} is not grounded, it should also be bypassed to analog ground using multiple capacitors (see 5.0 "Power Supply Considerations"). AGND and DGND should be at the same potential. V_{IN0} is shown with an input protection network. Pin 17 is normally left open, but optional "speedup" resistor R_{SA} can be used to reduce the conversion time.

4.0 INHERENT SAMPLE-AND-HOLD

Because the ADC10461, ADC10462, and ADC10464 sample the input signal once during each conversion, they are capable of measuring relatively fast input signals without the help of an external sample-hold. In a non-sampling successive-approximation A/D converter, regardless of speed, the input signal must be stable to better than ±1/2 LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion if a SAR with no internal sample-and-hold is used.

Because they incorporate a direct sample/hold control input, the ADC10461, ADC10462, and ADC10464 are suitable for use in DSP-based systems. The $\overline{S}/H$ input allows synchronization of the A/D converter to the DSP system's sampling rate and to other ADC10461s, ADC10462s, and ADC10464s.

The ADC10461, ADC10462, and ADC10464 can perform accurate conversions of input signals with frequency components from DC to over 250 kHz.

5.0 POWER SUPPLY CONSIDERATIONS

The ADC10461, ADC10462, and ADC10464 are designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor. Depending on the circuit board layout and other system considerations, more bypassing may be necessary.

The ADC10461 has a single ground pin, and the ADC10462 and ADC10464 each have separate analog and digital ground pins for separate bypassing of the analog and digital supplies. The devices with separate analog and digital ground pins should have their ground pins connected to the same potential, and all grounds should be "clean" and free of noise.

In systems with multiple power supplies, careful attention to power supply sequencing may be necessary to avoid overdriving inputs. The A/D converter's power supply pins should be at the proper voltage before digital or analog signals are applied to any of the other pins.

6.0 LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC10461, ADC10462, and ADC10464, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome, so digital grounds should always be separate from analog grounds. For best performance, separate ground planes should be provided for the digital and analog parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

7.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but conventional DC integral and differential nonlinearity specifications don't accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynam-

Applications Information (Continued)

ic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), are quantitative measures of this capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. The resulting spectral plot might look like the ones shown in the typical performance curves. The large peak is the fundamental frequency, and the noise and distortion components (if any are present) are visible above and below the fundamental frequency. Harmonic distortion components appear at whole multiples of the input frequency. Their amplitudes are combined as the square root of the sum of the squares and compared to the fundamental amplitude to yield the THD specification. Guaranteed limits for THD are given in the table of Electrical Characteristics.

Signal-to-noise ratio is the ratio of the amplitude at the fundamental frequency to the rms value at all other frequencies, excluding any harmonic distortion components. Guaranteed limits are given in the Electrical Characteristics table. An alternative definition of signal-to-noise ratio includes the distortion components along with the random noise to yield a signal-to-noise-plus-distortion ration, or S/(N + D).

The THD and noise performance of the A/D converter will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. One way of describing the A/D's performance as a function of signal frequency is to make a plot of "effective bits" versus frequency. An ideal A/D converter with no linearity errors or self-generated noise will have a signal-to-noise ratio equal to (6.02n + 1.8) dB, where n is the resolution in bits of the A/D converter. A real A/D converter will have some amount of noise and distortion, and the effective bits can be found by:

$$n\ (\text{effective}) = \frac{S/(N + D)\ (\text{dB}) - 1.8}{6.02}$$

where S/(N + D) is the ratio of signal to noise and distortion, which can vary with frequency.

As an example, an ADC10461 with a 4.85 V_{P-P}, 100 kHz sine wave input signal will typically have a signal-to-noise-plus-distortion ratio of 59.2 dB, which is equivalent to 9.53 effective bits. As the input frequency increases, noise and distortion gradually increase, yielding a plot of effective bits or S/(N + D) as shown in the typical performance curves.

8.0 SPEED ADJUST

In applications that require faster conversion times, the Speed Adjust pin (pin 14 on the ADC10462, pin 17 on the ADC10464) can significantly reduce the conversion time. The speed adjust pin is connected to an on-chip current source that determines the converter's internal timing. By connecting a resistor between the speed adjust pin and ground as shown in *Figure 4*, the internal programming current is increased, which reduces the conversion time. As an example, an 18k resistor reduces the conversion time of a typical part from 600 ns to 350 ns with no significant effect on linearity. Using smaller resistors to further decrease the conversion time is possible as well, although the linearity will begin to degrade somewhat (see curves). Note that the resistor value needed to obtain a given conversion time will vary from part to part, so this technique will generally require some "tweaking" to obtain satisfactory results.

For applications that require guaranteed performance using the speed adjust pin, the ADC10662 and ADC10664 are tested and guaranteed for static and dynamic performance with a fixed value of speed-up resistor.

National Semiconductor

ADC10662/ADC10664 10-Bit 360 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep* conversion technique, the 10-bit ADC10662 and ADC10664 are 2- and 4-input CMOS analog-to-digital converters offering sub-microsecond conversion times yet dissipating a maximum of only 235 mW. The ADC10662 and ADC10664 perform a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. In addition to standard static performance specifications (Linearity, Full-Scale Error, etc.) dynamic performance (THD, S/N) is guaranteed.

The analog input voltage to the ADC10662 and ADC10664 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 250 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10662 and ADC10664 include a "speed-up" pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 360 ns.

For ease of interface to microprocessors, the ADC10662 and ADC10664 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Features

- Built-in sample-and-hold
- Single +5V supply
- 2- or 4-input multiplexer options
- No external clock required

Key Specifications

- Conversion time to 10 bits — 360 ns typical, 466 ns max over temperature
- Sampling Rate — 1.5 MHz (min)
- Low power dissipation — 235 mW (max)
- Total harmonic distortion (50 kHz) — −60 dB (max)
- No missing codes over temperature

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Ordering Information

ADC10662

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10662CIN	N24A Molded DIP
ADC10662CIWM	M24B Small Outline

ADC10664

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC10664CIN	N28B Molded DIP
ADC10664CIWM	M28B Small Outline

*U.S. Patent Number 4918449

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)	−0.3V to +6V
Voltage at Any Input or Output	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	875 mW
ESD Susceptability (Note 5)	2000V
Soldering Information (Note 6)	
N Package (10 Sec)	260°C
SO Package:	
Vapor Phase (60 Sec)	215°C
Infrared (15 Sec)	220°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10662CIN, ADC10662CIWM, ADC10664CIN, ADC10664CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage Range	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = +5V$, $V_{REF(-)} = GND$, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{Min}$ to T_{Max};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
	Resolution			**10**	Bits
	Integral Linearity Error		±0.5	±1.0/±**1.5**	LSB
	Offset Error			±**1**	LSB (max)
	Full-Scale Error			±**1**	LSB (max)
	Total Unadjusted Error		±0.5	±1.5/±**2.0**	LSB
	Missing Codes			**0**	(max)
	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.5V$ $V^+ = 5V \pm 10\%$, $V_{REF} = 4.5V$	±1/16 ±1/8		LSB LSB
THD	Total Harmonic Distortion (Note 10)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P} f_{IN} = 240 kHz, 4.85 V_{P-P}	**−68** **−66** **−62** **−58**	 **−60** 	dB dB (max) dB dB
SNR	Signal-to-Noise Ratio (Note 10)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P}	**61** **60** **60**	 **58** 	dB dB (min) dB
ENOB	Effective Number of Bits (Note 10)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P}	**9.6** **9.5**	 **9**	Bits Bits (min)
R_{REF}	Reference Resistance		650	**400** **900**	Ω (min) Ω (max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(+)}$**	V (max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (max)
V_{IN}	Input Voltage			**GND − 0.05**	V (min)
	OFF Channel Input Leakage Current ON Channel Input Leakage Current	$\overline{CS} = V^+$, $V_{IN} = V^+$ $\overline{CS} = V^+$, $V_{IN} = V^+$	0.01 ±1	**3** **−3**	μA (max) μA (max)

2

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = 5V$ $V_{REF(-)} = GND$, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN(1)} = 5V$	0.005	**3.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN(0)}$ 0V	−0.005	**−3.0**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = -360\ \mu A$ $V^+ = 4.5V$, $I_{OUT} = -10\ \mu A$		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 5V$ $V_{OUT} = 0V$	0.1 −0.1	**50** **−50**	μA (max) μA (max)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$	1.0	**2**	mA (max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$	30	**45**	mA (max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions		Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{CONV}	Mode 1 Conversion Time from Rising Edge of $\overline{S}/H$ to Falling Edge of $\overline{INT}$	CIN, CIWM Suffixes		360	**466**	ns (max)
t_{CRD}	Mode 2 Conversion Time	CIN, CIWM Suffixes		470	**610**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; $C_L = 100$ pF		30	**50**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; $C_L = 100$ pF	CIN, CIWM Suffixes	475	**616**	ns (max)
t_{SH}	Minimum Sample Time	Mode 1 *(Figure 1)*; (Note 9)			**150**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	$R_L = 1k$, $C_L = 10$ pF		30	**60**	ns (max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 100$ pF		25	**50**	ns (max)
t_P	Delay from End of Conversion to Next Conversion				**50**	ns (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{MS}	Multiplexer Control Setup Time		10	**75**	ns (max)
t_{MH}	Multiplexer Hold Time		10	**40**	ns (max)
C_{VIN}	Analog Input Capacitance		35		pF (max)
C_{OUT}	Logic Output Capacitance		5		pF (max)
C_{IN}	Logic Input Capacitance		5		pF (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditons.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. In most cases, the maximum derated power dissipation will be reached only during fault conditions. For these devices, T_{JMAX} for a board-mounted device can be found from the tables below:

ADC10662

Suffix	θ_{JA} (°C/W)
CIN	60
CIWM	82

ADC10664

Suffix	θ_{JA} (°C/W)
CIN	53
CIWM	78

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Typicals represent most likely parametric norm.

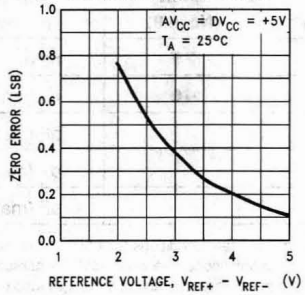
Note 8: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Accuracy may degrade if t_{SH} is shorter than the value specified. See curves of Accuracy vs t_{SH}.

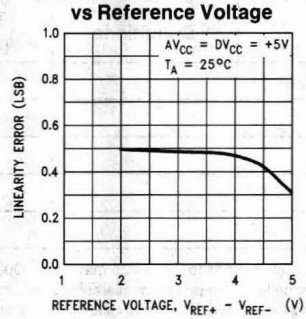
Note 10: THD, SNR, and ENOB are tested in Mode 1. Measuring these quantities in Mode 2 yields similar values.

Typical Performance Characteristics

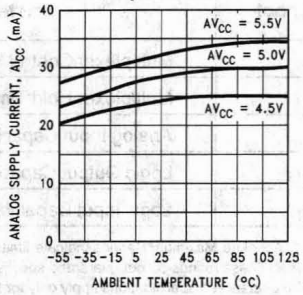
Zero (Offset) Error vs Reference Voltage



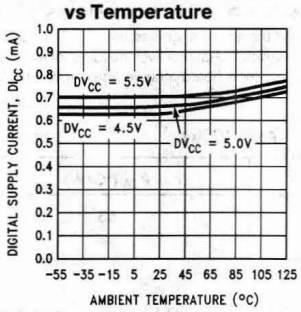
Linearity Error vs Reference Voltage



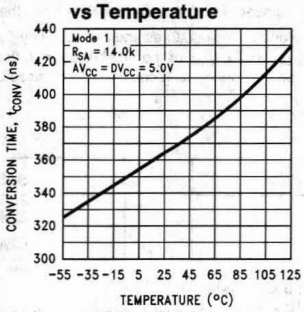
Analog Supply Current vs Temperature



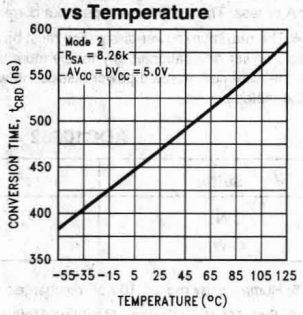
Digital Supply Current vs Temperature



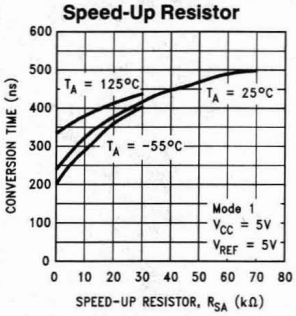
Conversion Time vs Temperature



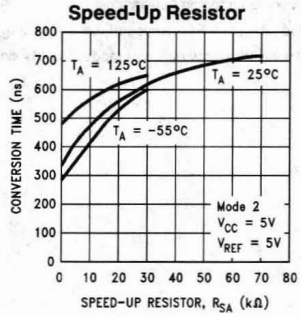
Conversion Time vs Temperature



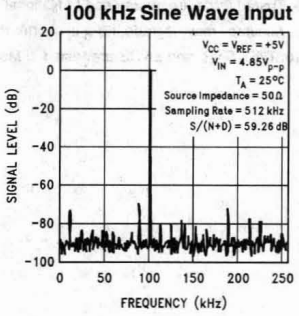
Conversion Time vs Speed-Up Resistor



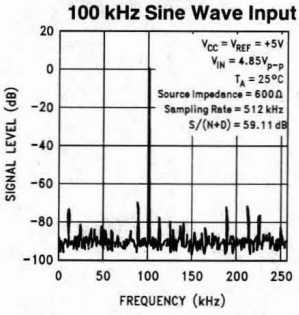
Conversion Time vs Speed-Up Resistor



Spectral Response with 100 kHz Sine Wave Input



Spectral Response with 100 kHz Sine Wave Input



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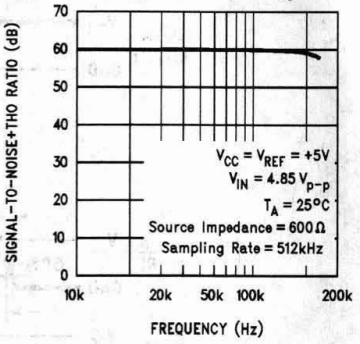
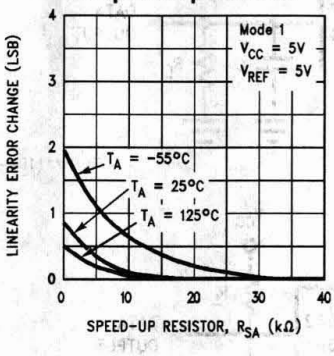
Typical Performance Characteristics (Continued)

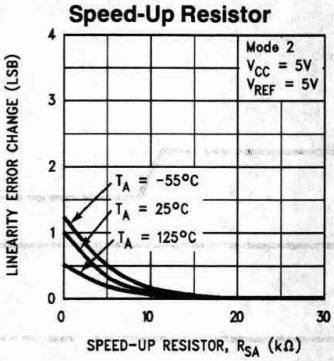
Signal-to-Noise + THD Ratio vs Signal Frequency



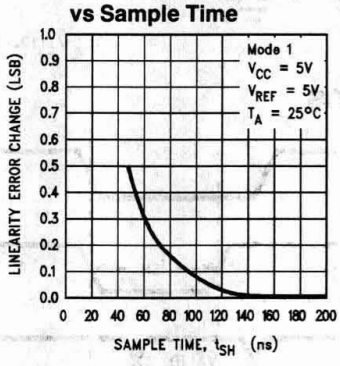
Linearity Change vs Speed-Up Resistor



Linearity Change vs Speed-Up Resistor



Linearity Error Change vs Sample Time



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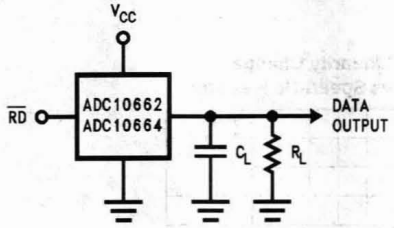
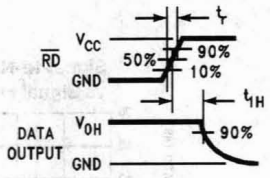
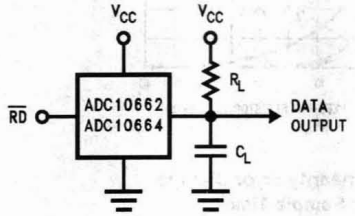
TRI-STATE Test Circuits and Waveforms



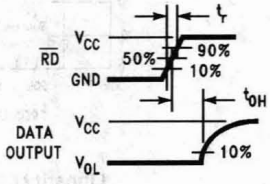
TL/H/11192–3



TL/H/11192–4



TL/H/11192–5



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Timing Diagrams

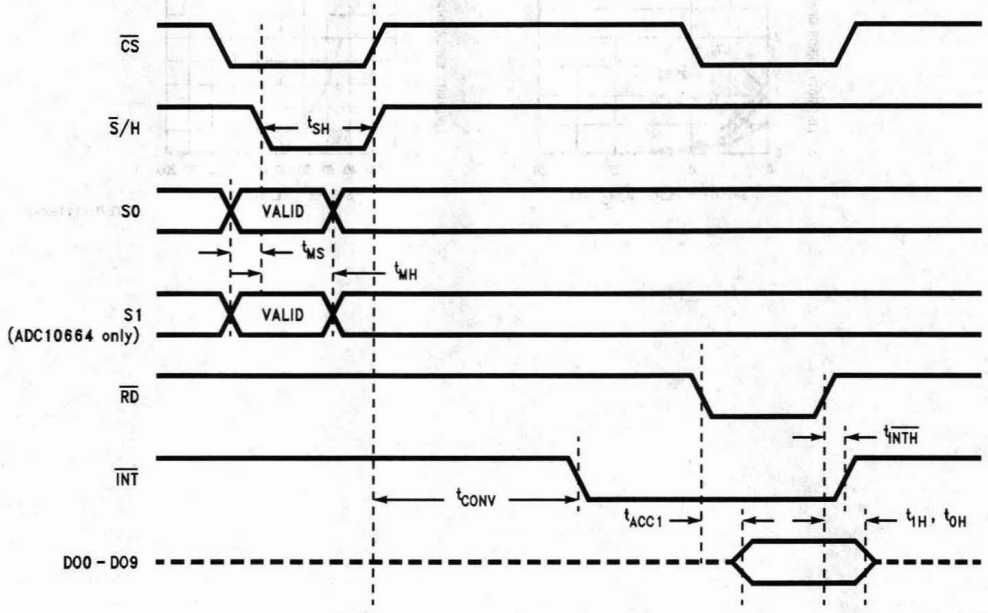

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FIGURE 1. Mode 1. The conversion time (t_{CONV}) is set by the internal timer.

Timing Diagrams (Continued)

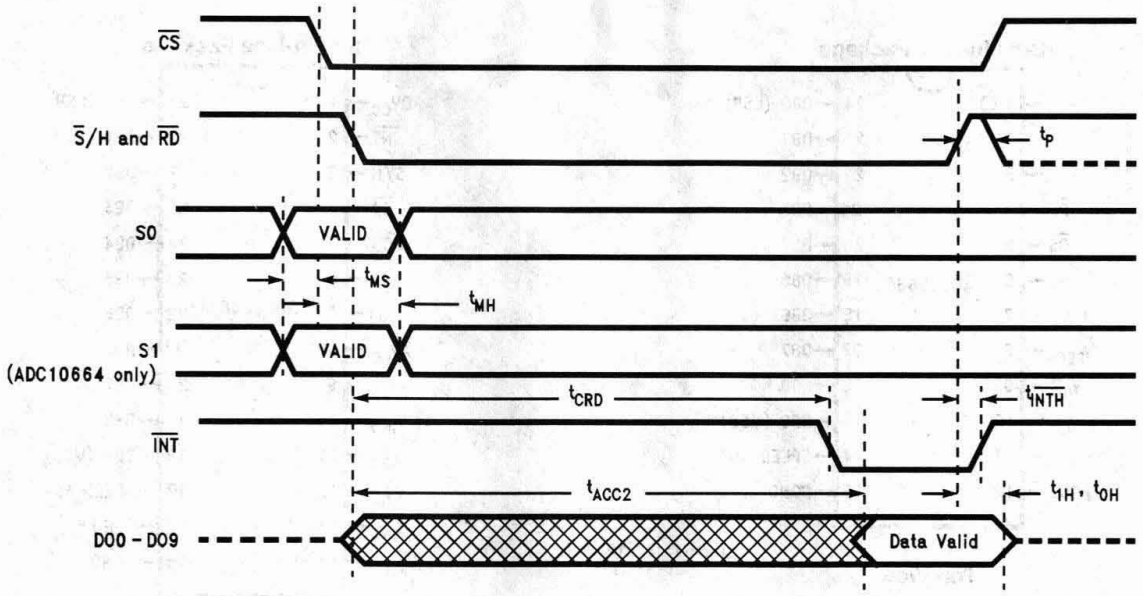

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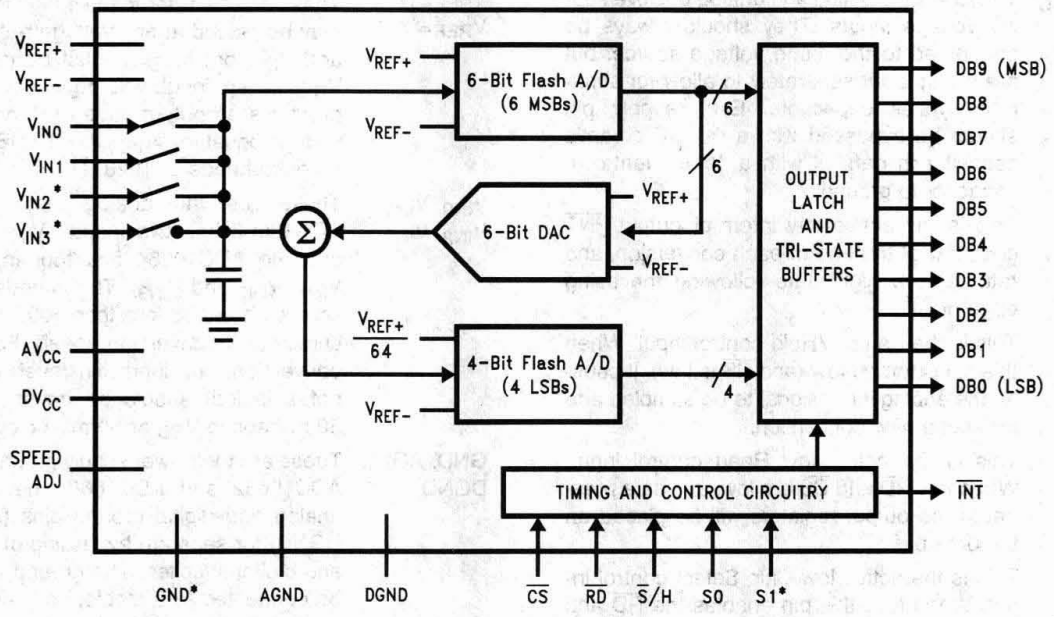
FIGURE 2. Mode 2 ($\overline{RD}$ Mode). The conversion time (t_{CRD}) includes the sampling time and is determined by the internal timer.

Simplified Block Diagram



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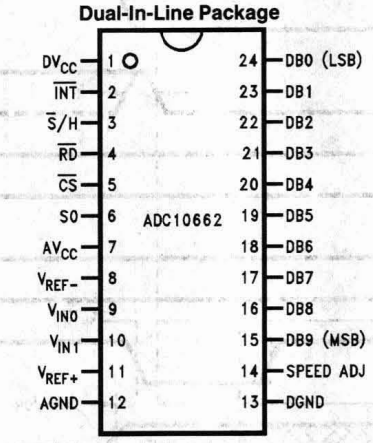
*ADC10664 Only

Connection Diagrams

Dual-In-Line Package



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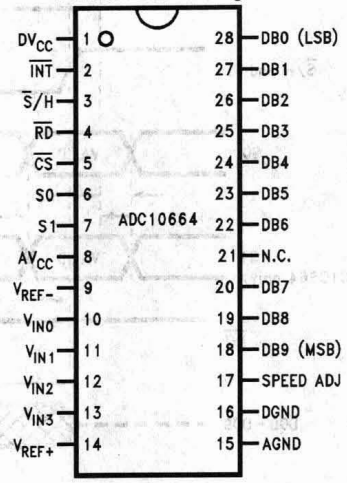
Top View

Dual-In-Line Package



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Top View

Pin Descriptions

DV_{CC}, AV_{CC} These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}/H$ This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}/H$ pins.

S0, S1 These pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}/H$ makes its High-to-Low transition (See the Timing Diagrams). The ADC10664 includes both S0 and S1. The ADC10662 includes just S0.

$V_{REF}-$, $V_{REF}+$ These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but $V_{REF}+$ must be greater than $V_{REF}-$. An input voltage equal to $V_{REF}-$ produces an output code of 0, and an input voltage equal to ($V_{REF}+$ − 1 LSB) produces an output code of 1023.

V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3} These are the analog input pins. The ADC10662 has two inputs (V_{IN0} and V_{IN1}) and the ADC10664 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND These are the power supply ground pins. The ADC10662 and ADC10664 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. Both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE output pins.

SPEED ADJ By connecting a resistor between this pin and ground, the conversion time can be reduced. The specifications listed in the table of Electrical Characteristics apply for a speed adjust resistor (R_{SA}) equal to 14.0 kΩ (Mode 1) or 8.26 kΩ (Mode 2). See the Typical Performance Curves and the table of Electrical Characteristics.

Functional Description

The ADC10662 and ADC10664 digitize an analog input signal to 10 bits accuracy by performing two lower-resolution "flash" conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits LSBs).

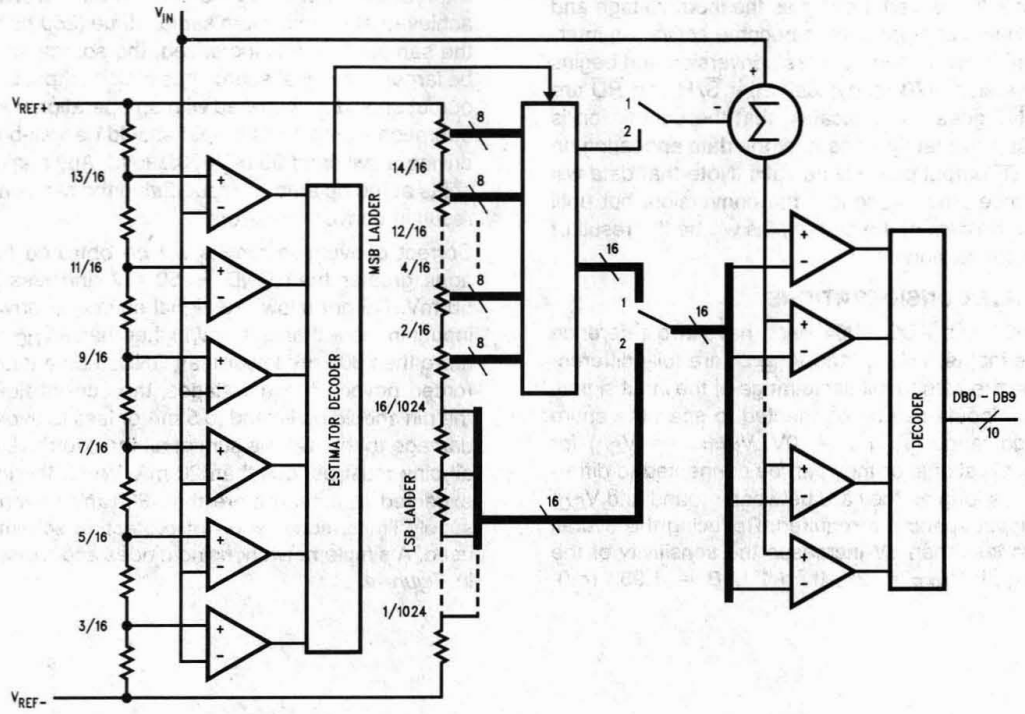
Figure 3 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024 the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has 1/8 of the total reference voltage across it, and each of the LSB resistors has 1/64 of the total reference voltage across it. Tap points across these resistors can be connected, in groups of sixteen, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between V_{REF+} and V_{REF-}. Six comparators compare the input voltage with the tap voltages on this resistor string to provide a low-resolution "estimate" of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator MUX to connect the 16 comparators to the taps on the MSB ladder between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data—four bits in the flash itself, and 2 bits in the estimator.

The remaining four LSBs are now determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second, four-bit flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the multistep conversion technique used in the ADC10662 and ADC10664 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC10662 and ADC10664 to perform high-speed conversions without excessive power drain.



TL/H/11192–12

FIGURE 3. Block Diagram of the Multistep Converter Architecture

Applications Information

1.0 MODES OF OPERATION

The ADC10662 and ADC10664 have two basic digital interface modes. *Figure 1* and *Figure 2* are timing diagrams for the two modes. The ADC10662 and ADC10664 have input multiplexers that are controlled by the logic levels on pins S_0 and S_1 when $\overline{S}/H$ goes low. Table I is a truth table showing how the input channnels are assigned.

Mode 1

In this mode, the $\overline{S}/H$ pin controls the start of conversion. $\overline{S}/H$ is pulled low for a minimum of 150 ns. This causes the comparators in the "coarse" flash converter to become active. When $\overline{S}/H$ goes high, the result of the coarse conversion is latched and the "fine" conversion begins. After 360 ns (typical), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}/H$ or $\overline{RD}$. $\overline{CS}$ is internally "ANDed" with $\overline{S}/H$ and $\overline{RD}$; the input voltage is sampled when $\overline{CS}$ and $\overline{S}/H$ are low, and data is read when $\overline{CS}$ and $\overline{RD}$ are low. $\overline{INT}$ is reset high on the rising edge of $\overline{RD}$.

TABLE I. Input Multiplexer Programming

ADC10664

S_1	S_0	Channel
0	0	V_{IN0}
0	1	V_{IN1}
1	0	V_{IN2}
1	1	V_{IN3}

(a)

ADC10662

S_0	Channel
0	V_{IN0}
1	V_{IN1}

(b)

Mode 2

In Mode 2, also called "$\overline{RD}$ mode", the $\overline{S}/H$ and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The A/D converter samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion. 470 ns (typical) after $\overline{S}/H$ and $\overline{RD}$ are pulled low, $\overline{INT}$ goes low, indicating that the conversion is completed. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but until $\overline{INT}$ goes low the data at the output pins will be the result of the previous conversion.

2.0 REFERENCE CONSIDERATIONS

The ADC10662 and ADC10664 each have two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range (V_{REF-} = 0V, V_{REF+} = V_{CC}) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required. Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if V_{REF} = 2V, then 1 LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See the Typical Performance Curves for more information. For this reason, reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC10662 and ADC10664. V_{REF-} can be connected to a voltage other than ground as long as the voltage source connected to this pin is capable of sinking the converter's reference current (12.5 mA Max @ V_{REF} = 5V). If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should be bypassed with a 10 μF tantalum and a 0.1 μF ceramic.

3.0 THE ANALOG INPUT

The ADC10662 and ADC10664 sample the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can therefore be observed at the analog input during normal operation. These spikes are normal and do not degrade the converter's performance.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (250 ns maximum). If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than AV_{CC} and DV_{CC}, or more than 300 mV lower than GND. If an analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 20 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits, some sourt of protection scheme should be used. A simple network using diodes and resistors is shown in *Figure 4.*

Applications Information (Continued)

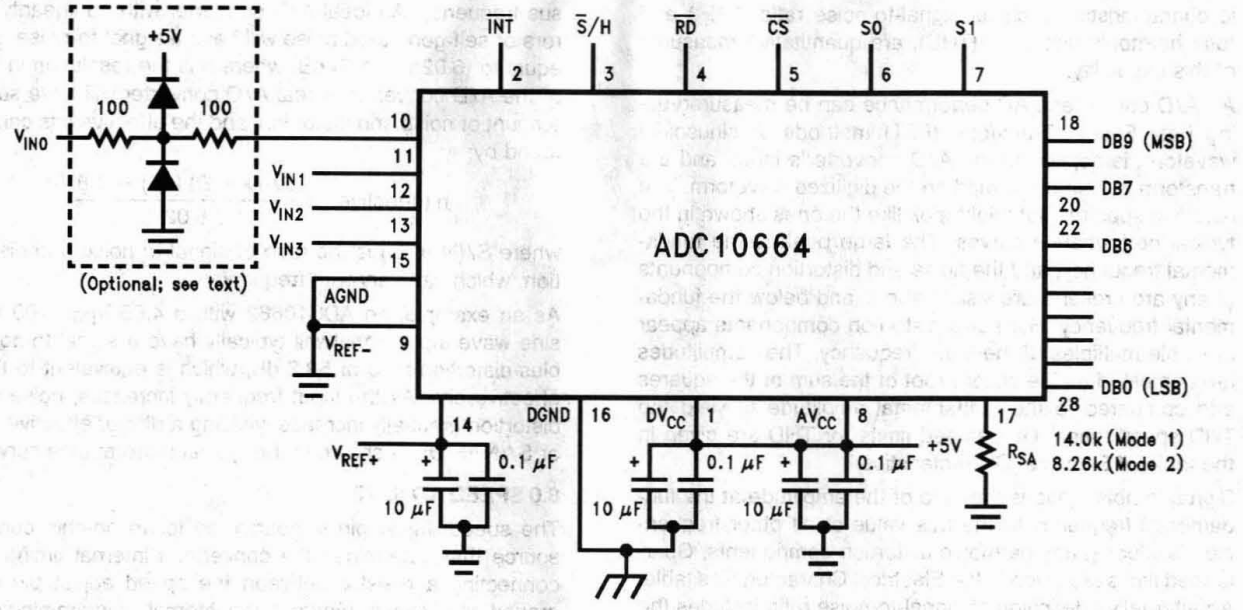


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FIGURE 4. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. If V_{REF-} is not grounded, it should also be bypassed to analog ground using multiple capacitors (see 5.0 "Power Supply Considerations"). AGND and DGND should be at the same potential. V_{IN0} is shown with an input protection network.

4.0 INHERENT SAMPLE-AND-HOLD

Because the ADC10662 and ADC10664 sample the input signal once during each conversion, they are capable of measuring relatively fast input signals without the help of an external sample-hold. In a non-sampling successive-approximation A/D converter, regardless of speed, the input signal must be stable to better than ±1/2 LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion if a SAR with no internal sample-and-hold is used.

Because they incorporate a direct sample/hold control input, the ADC10662 and ADC10664 are suitable for use in DSP-based systems. The $\overline{S}/H$ input allows synchronization of the A/D converter to the DSP system's sampling rate and to other ADC10662s, and ADC10664s.

The ADC10662 and ADC10664 can perform accurate conversions of input signals with frequency components from DC to over 250 kHz.

5.0 POWER SUPPLY CONSIDERATIONS

The ADC10662 and ADC10664 are designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor. Depending on the circuit board layout and other system considerations, more bypassing may be necessary.

The ADC10662 and ADC10664 have separate analog and digital ground pins for separate bypassing of the analog and digital supplies. Their ground pins should be connected to the same potential, and all grounds should be "clean" and free of noise.

In systems with multiple power supplies, careful attention to power supply sequencing may be necessary to avoid overdriving inputs. The A/D converter's power supply pins should be at the proper voltage before digital or analog signals are applied to any of the other pins.

6.0 LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC10662 and ADC10664, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome, so digital grounds should always be separate from analog grounds. For best performance, separate ground planes should be provided for the digital and analog parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

7.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but conventional DC integral and differential nonlinearity specifications don't accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynam-

Applications Information (Continued)

ic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), are quantitative measures of this capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. The resulting spectral plot might look like the ones shown in the typical performance curves. The large peak is the fundamental frequency, and the noise and distortion components (if any are present) are visible above and below the fundamental frequency. Harmonic distortion components appear at whole multiples of the input frequency. Their amplitudes are combined as the square root of the sum of the squares and compared to the fundamental amplitude to yield the THD specification. Guaranteed limits for THD are given in the table of Electrical Characteristics.

Signal-to-noise ratio is the ratio of the amplitude at the fundamental frequency to the rms value at all other frequencies, excluding any harmonic distortion components. Guaranteed limits are given in the Electrical Characteristics table. An alternative definition of signal-to-noise ratio includes the distortion components along with the random noise to yield a signal-to-noise-plus-distortion ration, or S/(N + D).

The THD and noise performance of the A/D converter will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. One way of describing the A/D's performance as a function of signal frequency is to make a plot of "effective bits" versus frequency. An ideal A/D converter with no linearity errors or self-generated noise will have a signal-to-noise ratio equal to (6.02n + 1.8) dB, where n is the resolution in bits of the A/D converter. A real A/D converter will have some amount of noise and distortion, and the effective bits can be found by:

$$n\ (\text{effective}) = \frac{S/(N + D)\ (\text{dB}) - 1.8}{6.02}$$

where S/(N + D) is the ratio of signal to noise and distortion, which can vary with frequency.

As an example, an ADC10662 with a 4.85 V_{P-P}, 100 kHz sine wave input signal will typically have a signal-to-noise-plus-distortion ratio of 59.2 dB, which is equivalent to 9.53 effective bits. As the input frequency increases, noise and distortion gradually increase, yielding a plot of effective bits or S/(N + D) as shown in the typical performance curves.

8.0 SPEED ADJUST

The speed adjust pin is connected to an on-chip current source that determines the converter's internal timing. By connecting a resistor between the speed adjust pin and ground as shown in *Figure 4*, the internal programming current is increased, which reduces the conversion time. The ADC10662 and ADC10664 are specified and guaranteed for operation with R_{SA} = 14.0 kΩ (Mode 1) or R_{SA} = 8.26k (Mode 2). Smaller resistors will result in faster conversion times, but linearity will begin to degrade as R_{SA} becomes smaller (see curves).

National Semiconductor

ADC12H030/ADC12H032/ADC12H034/ADC12H038, ADC12030/ADC12032/ADC12034/ADC12038 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12030, and ADC12H030 families are 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexers. The ADC12032/ADC12H032, ADC12034/ADC12H034 and ADC12038/ADC12H038 have 2, 4 and 8 channel multiplexers, respectively. The differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12030/ADC12H030 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. The ADC12030 family is tested with a 5 MHz clock, while the ADC12H030 family is tested with an 8 MHz clock. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to less than ±1 LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +5V) can be accommodated with a single +5V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE™. For complementary voltage references see the LM4040, LM4041 or LM9140.

Applications

- Medical instruments
- Process control systems
- Test equipment

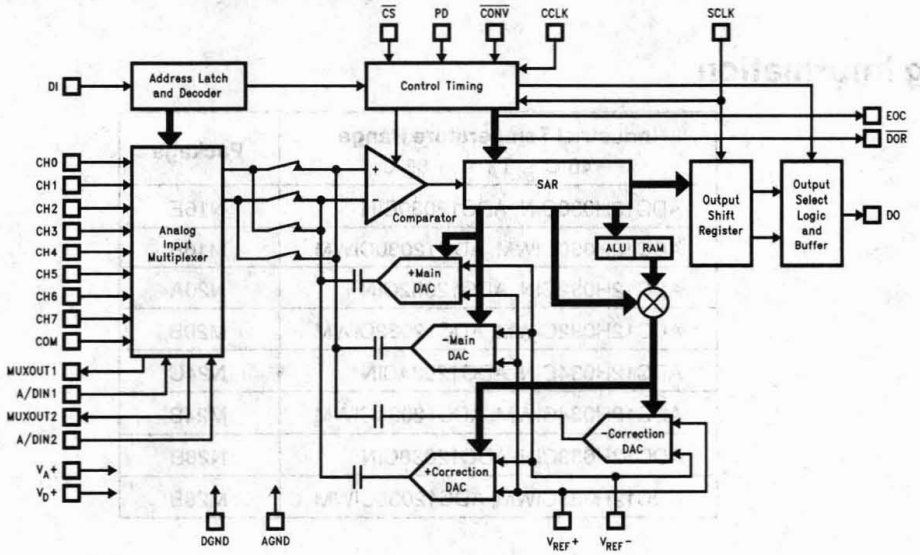
Features

- Serial I/O (MICROWIRE Compatible)
- 2, 4, or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Variable resolution and conversion rate
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- Fully tested and guaranteed with a 4.096V reference
- 0V to 5V analog input range with single 5V power supply
- No Missing Codes over temperature

Key Specifications

■ Resolution	12-bit plus sign
■ 12-bit plus sign conversion time	
— ADC12H030 family	5.5 μs (max)
— ADC12030 family	8.8 μs (max)
■ 12-bit plus sign throughput time	
— ADC12H030 family	8.6 μs (max)
— ADC12030 family	14 μs (max)
■ Integral linearity error	±1 LSB (max)
■ Single supply	5V ±10%
■ Power dissipation	33 mW (max)
— Power down	100 μW (typ)

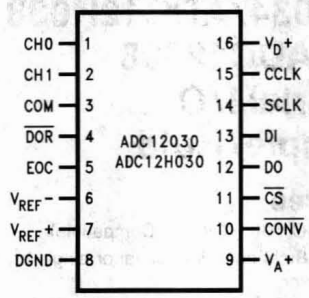
ADC12038 Simplified Block Diagram



TL/H/11354–1

Connection Diagrams

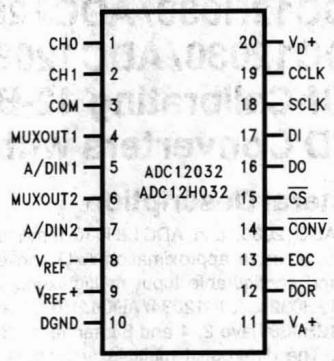
16-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11354–6

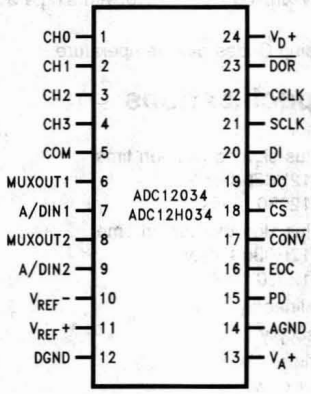
20-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11354–7

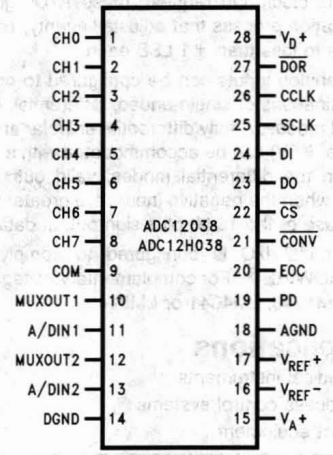
24-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11354–8

28-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11354–9

Ordering Information

Industrial Temperature Range $-40°C \leq T_A \leq +85°C$	Package
ADC12H030CIN, ADC12030CIN	N16E
ADC12H030CIWM, ADC12030CIWM	M16B
ADC12H032CIN, ADC12032CIN	N20A
ADC12H032CIWM, ADC12032CIWM	M20B
ADC12H034CIN, ADC12034CIN	N24C
ADC12H034CIWM, ADC12034CIWM	M24B
ADC12H038CIN, ADC12038CIN	N28B
ADC12H038CIWM, ADC12038CIWM	M28B

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage ($V^+ = V_A^+ = V_D^+$)	6.5V
Voltage at Inputs and Outputs except CH0–CH7 and COM	−0.3V to V^+ +0.3V
Voltage at Analog Inputs CH0–CH7 and COM	GND −5V to V^+ +5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
Input Current at Any Pin (Note 3)	±30 mA
Package Input Current (Note 3)	±120 mA
Package Dissipation at T_A = 25°C (Note 4)	500 mW
ESD Susceptability (Note 5) Human Body Model	1500V
Soldering Information N Packages (10 seconds)	260°C
SO Package (Note 6): Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12030CIN, ADC12030CIWM, ADC12H030CIN, ADC12H030CIWM, ADC12032CIN, ADC12032CIWM, ADC12H032CIN, ADC12H032CIWM, ADC12034CIN, ADC12034CIWM, ADC12H034CIN, ADC12H034CIWM, ADC12038CIN, ADC12038CIWM, ADC12H038CIN, ADC12H038CIWM	−40°C ≤ T_A ≤ +85°C
Supply Voltage ($V^+ = V_A^+ = V_D^+$)	+4.5V to +5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤ 100 mV
V_{REF}^+	0V to V_A^+
V_{REF}^-	0V to V_{REF}^+
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	1V to V_A^+
V_{REF} Common Mode Voltage Range $\frac{(V_{REF}^+ + V_{REF}^-)}{2}$	0.1 V_A^+ to 0.6 V_A^+
A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 Voltage Range	0V to V_A^+
A/D IN Common Mode Voltage Range $\frac{(V_{IN}^+ + V_{IN}^-)}{2}$	0V to V_A^+

Converter Electrical Characteristics

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \le 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and 10(t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25$°C. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12 + sign**	Bits (min)
+ILE	Positive Integral Linearity Error	After Auto-Cal (Notes 12, 18)	±1/2	**±1**	LSB (max)
−ILE	Negative Integral Linearity Error	After Auto-Cal (Notes 12, 18)	±1/2	**±1**	LSB (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 18)	±1/2	**±3.0**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 18)	±1/2	**±3.0**	LSB (max)
	Offset Error	After Auto-Cal (Notes 5, 18) $V_{IN}(+) = V_{IN}(-) = 2.048V$	±1/2	**±2**	LSB (max)
	DC Common Mode Error	After Auto-Cal (Note 15)	±2	**±3.5**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Notes 12, 13 and 14)	±1		LSB
	Resolution with No Missing Codes	8-bit + sign mode		**8 + sign**	Bits (min)
+INL	Positive Integral Linearity Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)
−INL	Negative Integral Linearity Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)
DNL	Differential Non-Linearity	8-bit + sign mode		**±3/4**	LSB (max)
	Positive Full-Scale Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)

Converter Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS (Continued)					
	Negative Full-Scale Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)
	Offset Error	8-bit + sign mode, after Auto-Zero (Note 13) $V_{IN}(+) = V_{IN}(-) = +2.048V$		**±1/2**	LSB (max)
TUE	Total Unadjusted Error	8-bit + sign mode after Auto-Zero (Notes 12, 13 and 14)		**±3/4**	LSB (max)
	Multiplexer Channel to Channel Matching		±0.05		LSB
	Power Supply Sensitivity	$V^+ = +5V \pm 10\%$ $V_{REF} = +4.096V$			
	Offset Error		±0.5	**±1**	LSB (max)
	+ Full-Scale Error		±0.5	**±1.5**	LSB (max)
	− Full-Scale Error		±0.5	**±1.5**	LSB (max)
	+ Integral Linearity Error		±0.5		LSB
	− Integral Linearity Error		±0.5		LSB
	Output Data from "12-Bit Conversion of Offset" (see Table V)	(Note 20)		**+10**	LSB (max)
				−10	LSB (min)
	Output Data from "12-Bit Conversion of Full-Scale" (see Table V)	(Note 20)		**4095**	LSB (max)
				4093	LSB (min)
UNIPOLAR DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	69.4		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	68.3		dB
		$f_{IN} = 40$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	65.7		dB
	−3 dB Full Power Bandwidth	$V_{IN} = 5\ V_{PP}$, where S/(N+D) drops 3 dB	31		kHz
DIFFERENTIAL DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = \pm 5V$, $V_{REF}^+ = 5.0V$	77.0		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 5V$, $V_{REF}^+ = 5.0V$	73.9		dB
		$f_{IN} = 40$ kHz, $V_{IN} = \pm 5V$, $V_{REF}^+ = 5.0V$	67.0		dB
	−3 dB Full Power Bandwidth	$V_{IN} = \pm 5V$, where S/(N+D) drops 3 dB	40		kHz

Electrical Characteristics

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{REF}	Reference Input Capacitance		85		pF
$C_{A/D}$	A/DIN1 and A/DIN2 Analog Input Capacitance		75		pF
	A/DIN1 and A/DIN2 Analog Input Leakage Current	$V_{IN} = +5.0V$ or $V_{IN} = 0V$	±0.1	**±1.0**	μA (max)
	CH0–CH7 and COM Input Voltage			**GND − 0.05** **$V_A^+ + 0.05$**	V (min) V (max)
C_{CH}	CH0–CH7 and COM Input Capacitance		10		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF
	Off Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	−0.01	**−0.3**	μA (min)
		On Channel = 0V and Off Channel = 5V	0.01	**0.3**	μA (max)
	On Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	0.01	**0.3**	μA (max)
		On Channel = 0V and Off Channel = 5V	−0.01	**−0.3**	μA (min)
	MUXOUT1 and MUXOUT2 Leakage Current	$V_{MUXOUT} = 5.0V$ or $V_{MUXOUT} = 0V$	0.01	**0.3**	μA (max)
R_{ON}	MUX On Resistance	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	850	**1150**	Ω (max)
	R_{ON} Matching Channel to Channel	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	5		%
	Channel to Channel Crosstalk	$V_{IN} = 5\ V_{PP}$, $f_{IN} = 40$ kHz	−72		dB
	MUX Bandwidth		90		kHz

DC and Logic Electrical Characteristics

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
CCLK, $\overline{CS}$, $\overline{CONV}$, DI, PD AND SCLK INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5.0V$	0.005	**1.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	μA (min)
DO, EOC AND $\overline{DOR}$ DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = -360\ \mu A$ $V^+ = 4.5V$, $I_{OUT} = -10\ \mu A$		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.1 0.1	**−3.0** **3.0**	μA (max) μA (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	14	**6.5**	mA (min)
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_D^+$	16	**8.0**	mA (min)
POWER SUPPLY CHARACTERISTICS					
I_D^+	Digital Supply Current ADC12030, ADC12032, ADC12034 and ADC12038	Awake $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	1.6 600 20	**2.5**	mA (max) μA μA
	Digital Supply Current ADC12H030, ADC12H032, ADC12H034 and ADC12H038	Awake $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	2.3 0.9 20	**3.2**	mA mA μA
I_A^+	Positive Analog Supply Current	Awake $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	2.7 10 0.1	**4.0**	mA (max) μA μA
I_{REF}	Reference Input Current	Awake $\overline{CS}$ = HIGH, Powered Down	70 0.1		μA μA

AC Electrical Characteristics

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	ADC12H030/2/4/8 Limits (Note 11)	ADC12030/2/4/8 Limits (Note 11)	Units (Limits)
f_{CK}	Conversion Clock (CCLK) Frequency		10 1	**8**	**5**	MHz (max) MHz (min)
f_{SK}	Serial Data Clock SCLK Frequency		10 0	**8**	**5**	MHz (max) Hz (min)
	Conversion Clock Duty Cycle			**40** **60**	**40** **60**	% (min) % (max)
	Serial Data Clock Duty Cycle			**40** **60**	**40** **60**	% (min) % (max)
t_C	Conversion Time	12-Bit + Sign or 12-Bit	$44(t_{CK})$	**$44(t_{CK})$**	**$44(t_{CK})$**	(max)
				5.5	**8.8**	μs (max)
		8-Bit + Sign or 8-Bit	$21(t_{CK})$	**$21(t_{CK})$**	**$21(t_{CK})$**	(max)
				2.625	**4.2**	μs (max)
t_A	Acquisition Time (Note 19)	6 Cycles Programmed	$6(t_{CK})$	**$6(t_{CK})$** **$7(t_{CK})$**	**$6(t_{CK})$** **$7(t_{CK})$**	(min) (max)
				0.75 **0.875**	**1.2** **1.4**	μs (min) μs (max)
		10 Cycles Programmed	$10(t_{CK})$	**$10(t_{CK})$** **$11(t_{CK})$**	**$10(t_{CK})$** **$11(t_{CK})$**	(min) (max)
				1.25 **1.375**	**2.0** **2.2**	μs (min) μs (max)
		18 Cycles Programmed	$18(t_{CK})$	**$18(t_{CK})$** **$19(t_{CK})$**	**$18(t_{CK})$** **$19(t_{CK})$**	(min) (max)
				2.25 **2.375**	**3.6** **3.8**	μs (min) μs (max)
		34 Cycles Programmed	$34(t_{CK})$	**$34(t_{CK})$** **$35(t_{CK})$**	**$34(t_{CK})$** **$35(t_{CK})$**	(min) (max)
				4.25 **4.375**	**6.8** **7.0**	μs (min) μs (max)
t_{CKAL}	Self-Calibration Time		$4944(t_{CK})$	**$4944(t_{CK})$**	**$4944(t_{CK})$**	(max)
				618.0	**988.8**	μs (max)
t_{AZ}	Auto-Zero Time		$76(t_{CK})$	**$76(t_{CK})$**	**$76(t_{CK})$**	(max)
				9.5	**15.2**	μs (max)
t_{SYNC}	Self-Calibration or Auto-Zero Synchronization Time from DOR		$2(t_{CK})$	**$2(t_{CK})$** **$3(t_{CK})$**	**$2(t_{CK})$** **$3(t_{CK})$**	(min) (max)
				0.250 **0.375**	**0.40** **0.60**	μs (min) μs (max)
$t_{\overline{DOR}}$	DOR High Time when $\overline{CS}$ is Low Continuously for Read Data and Software Power Up/Down		$9(t_{SK})$	**$9(t_{SK})$**	**$9(t_{SK})$**	(max)
				1.125	**1.8**	μs (max)
$t_{\overline{CONV}}$	$\overline{CONV}$ Valid Data Time		$8(t_{SK})$	**$8(t_{SK})$**	**$8(t_{SK})$**	(max)
				1.0	**1.6**	μs (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +5.0\ V_{DC}$, $V_{REF}^+ = +4.096\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
t_{HPU}	Hardware Power-Up Time, Time from PD Falling Edge to EOC Rising Edge		140	**250**	μs (max)
t_{SPU}	Software Power-Up Time, Time from Serial Data Clock Falling Edge to EOC Rising Edge		140	**250**	μs (max)
t_{ACC}	Access Time Delay from $\overline{CS}$ Falling Edge to DO Data Valid		20	**50**	ns (max)
t_{SET-UP}	Set-Up Time of $\overline{CS}$ Falling Edge to Serial Data Clock Rising Edge			**30**	ns (min)
t_{DELAY}	Delay from SCLK Falling Edge to $\overline{CS}$ Falling Edge		0	**5**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{CS}$ Rising Edge to DO TRI-STATE®	$R_L = 3k$, $C_L = 100$ pF	40	**100**	ns (max)
t_{HDI}	DI Hold Time from Serial Data Clock Rising Edge		5	**15**	ns (min)
t_{SDI}	DI Set-Up Time from Serial Data Clock Rising Edge		5	**10**	ns (min)
t_{HDO}	DO Hold Time from Serial Data Clock Falling Edge	$R_L = 3k$, $C_L = 100$ pF	25	**50** **5**	ns (max) ns (min)
t_{DDO}	Delay from Serial Data Clock Falling Edge to DO Data Valid		35	**50**	ns (max)
t_{RDO}	DO Rise Time, TRI-STATE to High DO Rise Time, Low to High	$R_L = 3k$, $C_L = 100$ pF	10 10	**30** **30**	ns (max) ns (max)
t_{FDO}	DO Fall Time, TRI-STATE to Low DO Fall Time, High to Low	$R_L = 3k$, $C_L = 100$ pF	12 12	**30** **30**	ns (max) ns (max)
t_{CD}	Delay from $\overline{CS}$ Falling Edge to $\overline{DOR}$ Falling Edge		25	**45**	ns (max)
t_{SD}	Delay from Serial Data Clock Falling Edge to $\overline{DOR}$ Rising Edge		25	**45**	ns (max)
C_{IN}	Capacitance of Logic Inputs		10		pF
C_{OUT}	Capacitance of Logic Outputs		20		pF

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > V_A^+$ or V_D^+), the current at that pin should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.

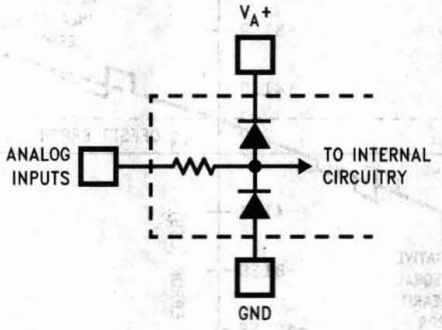
Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J max$, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J max - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_J max = 150°C$. The typical thermal resistance (Θ_{JA}) of these parts when board mounted follow:

Part Number	Thermal Resistance θ_{JA}
ADC12H030CIN, ADC12030CIN	53°C/W
ADC12H030CIWM, ADC12030CIWM	70°C/W
ADC12H032CIN, ADC12032CIN	46°C/W
ADC12H032CIWM, ADC12032CIWM	64°C/W
ADC12H034CIN, ADC12034CIN	42°C/W
ADC12H034CIWM, ADC12034CIWM	57°C/W
ADC12H038CIN, ADC12038CIN	40°C/W
ADC12H038CIWM, ADC12038CIWM	50°C/W

Note 5: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage this device. However, errors in the A/D conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A^+ or below GND by more than 50 mV. As an example, if V_A^+ is 4.5 V_{DC}, full-scale input voltage must be ≤ 4.55 V_{DC} to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that the V_A^+ and V_D^+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.

Note 9: With the test condition for V_{REF} ($V_{REF}^+ - V_{REF}^-$) given as +4.096V, the 12-bit LSB is 1.0 mV and the 8-bit LSB is 16.0 mV.

Note 10: Typicals are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero (see *Figures 1b* and *1c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between 1 to 0 and 0 to +1 (see *Figure 2*).

Note 14: Total unadjusted error includes offset, full-scale, linearity and multiplexer errors.

Note 15: The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.

Note 16: Channel leakage current is measured after the channel selection.

Note 17: Timing specifications are tested at the TTL logic levels, $V_{IL} = 0.4V$ for a falling edge and $V_{IH} = 2.4V$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 18: The ADC12030 family's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a maximum repeatability uncertainty of 0.2 LSB.

Note 19: If SCLK and CCLK are driven from the same clock source, then t_A is 6, 10, 18 or 34 clock periods minimum and maximum.

Note 20: The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

Electrical Characteristics (Continued)

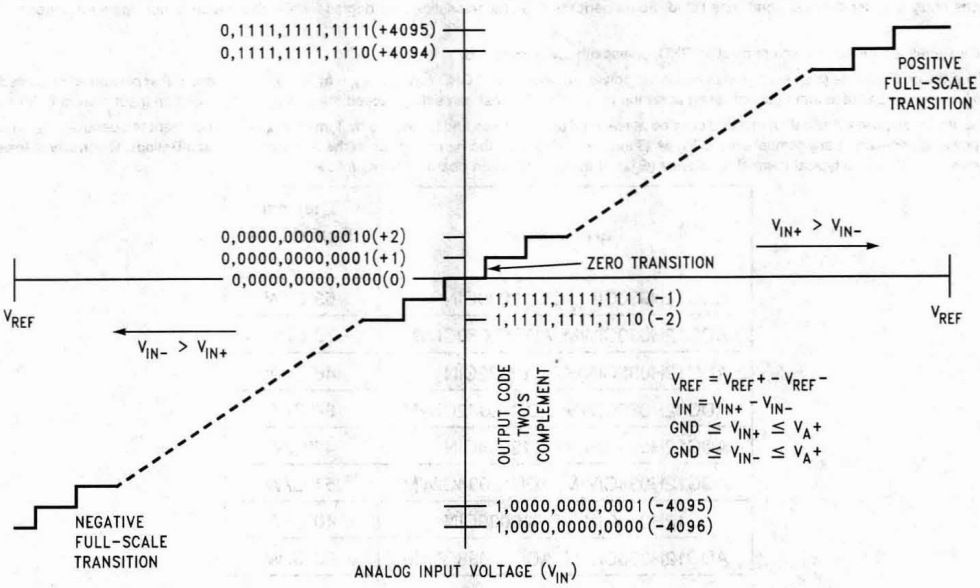

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FIGURE 1a. Transfer Characteristic

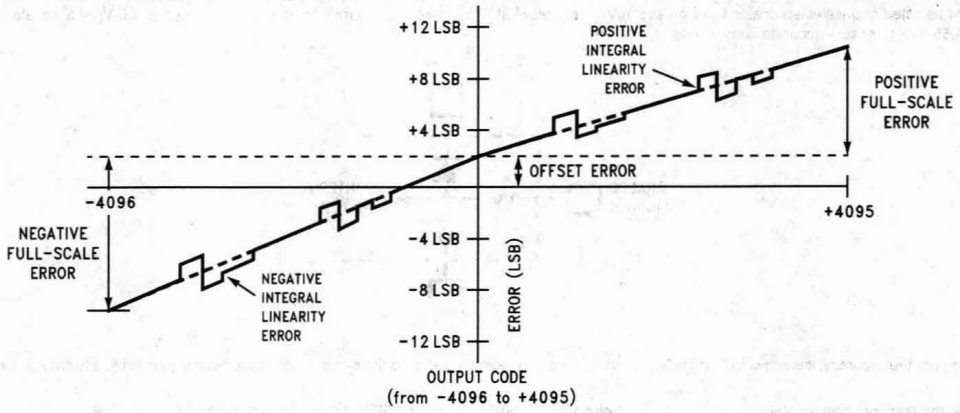

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

Electrical Characteristics (Continued)

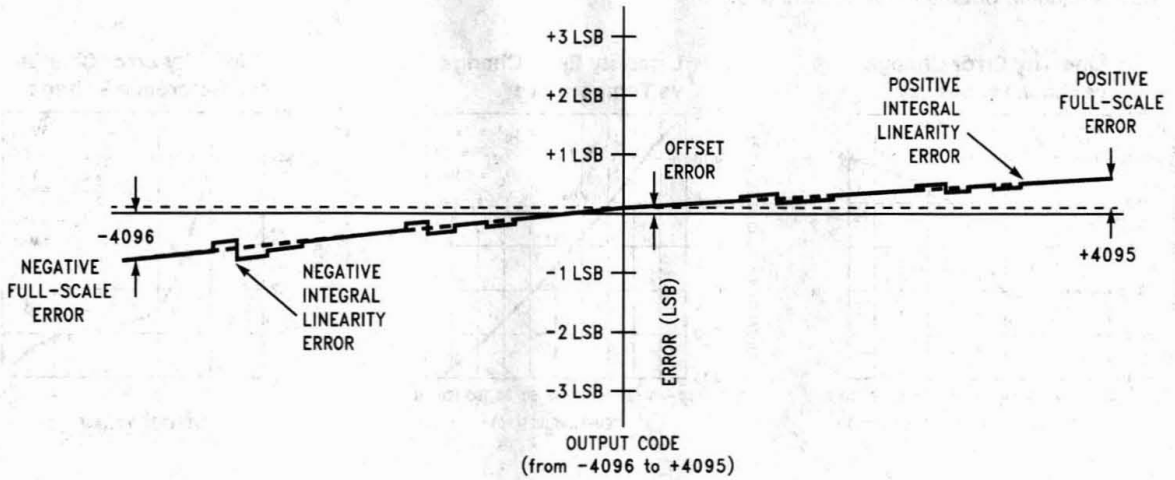

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FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

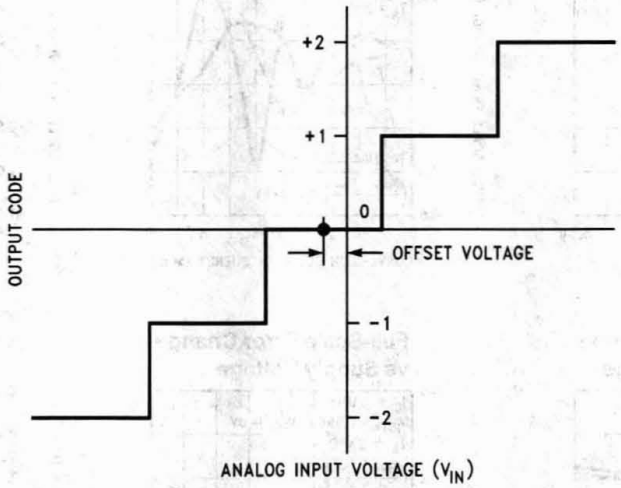

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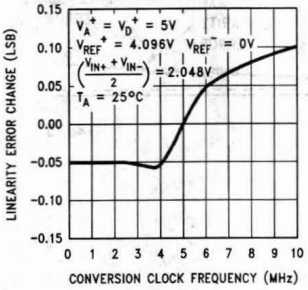
FIGURE 2. Offset or Zero Error Voltage

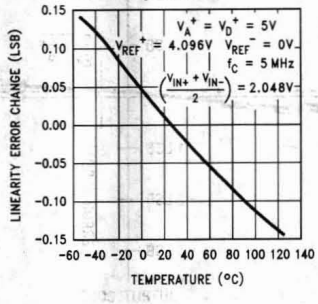
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown. (Note 9)

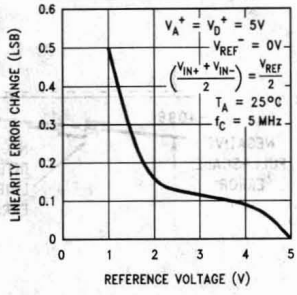
Linearity Error Change vs Clock Frequency


$V_A^+ = V_D^+ = 5V$
$V_{REF}^+ = 4.096V$ $V_{REF}^- = 0V$
$\left(\frac{V_{IN+} + V_{IN-}}{2}\right) = 2.048V$
$T_A = 25°C$
LINEARITY ERROR CHANGE (LSB)
CONVERSION CLOCK FREQUENCY (MHz)

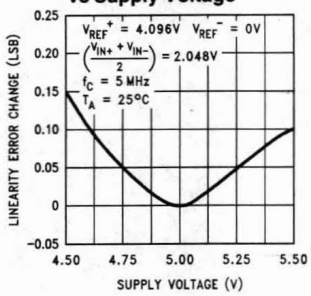
Linearity Error Change vs Temperature



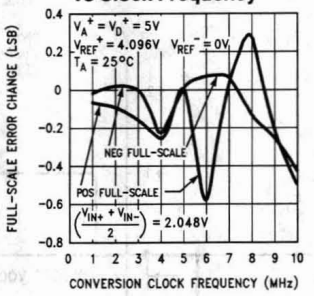
Linearity Error Change vs Reference Voltage



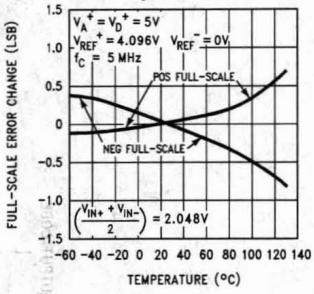
Linearity Error Change vs Supply Voltage



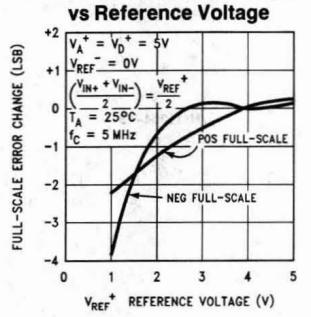
Full-Scale Error Change vs Clock Frequency



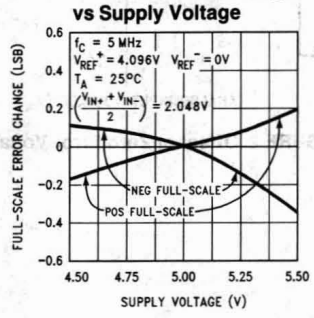
Full-Scale Error Change vs Temperature



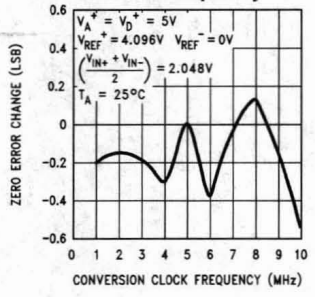
Full-Scale Error Change vs Reference Voltage



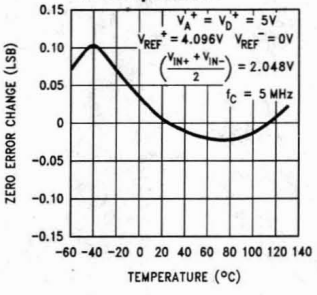
Full-Scale Error Change vs Supply Voltage



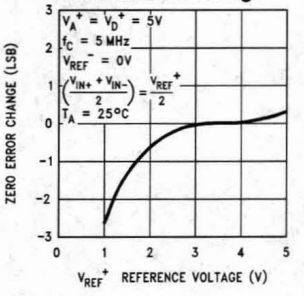
Zero Error Change vs Clock Frequency



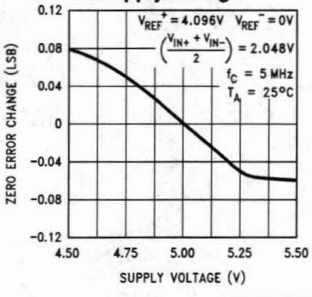
Zero Error Change vs Temperature



Zero Error Change vs Reference Voltage



Zero Error Change vs Supply Voltage

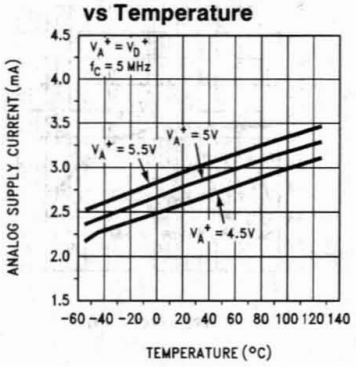


TL/H/11354–14

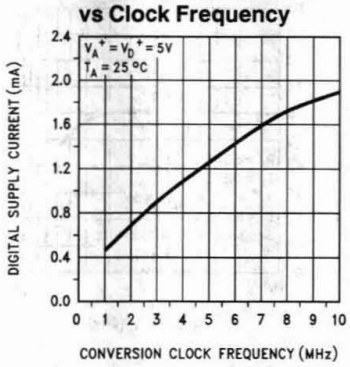
Typical Performance Characteristics (Continued)

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown.

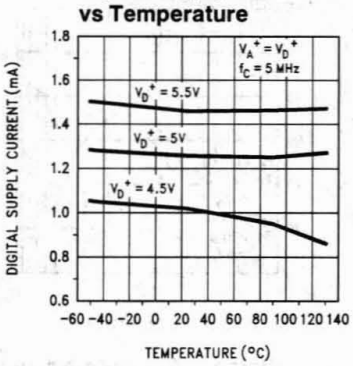
Analog Supply Current vs Temperature



Digital Supply Current vs Clock Frequency



Digital Supply Current vs Temperature



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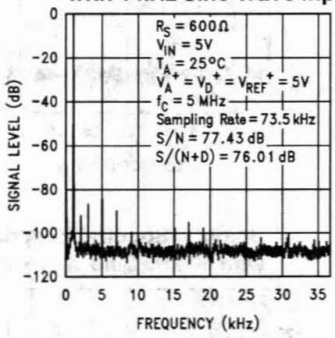
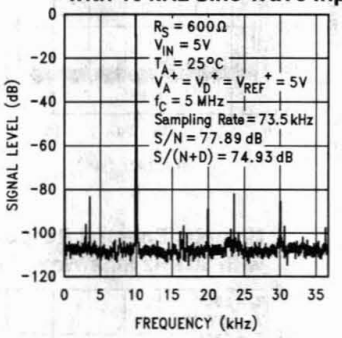
Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

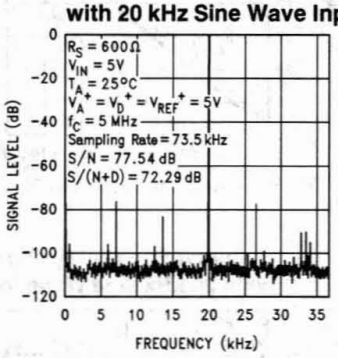
Bipolar Spectral Response with 1 kHz Sine Wave Input



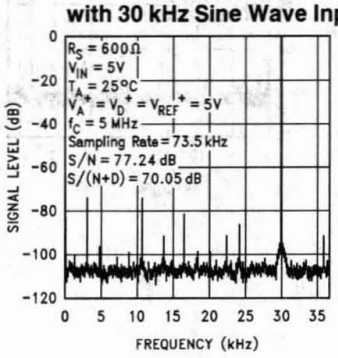
Bipolar Spectral Response with 10 kHz Sine Wave Input



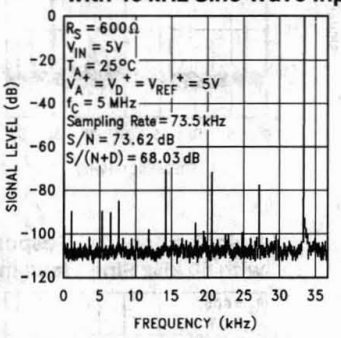
Bipolar Spectral Response with 20 kHz Sine Wave Input



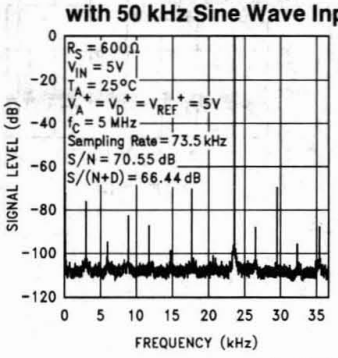
Bipolar Spectral Response with 30 kHz Sine Wave Input



Bipolar Spectral Response with 40 kHz Sine Wave Input



Bipolar Spectral Response with 50 kHz Sine Wave Input



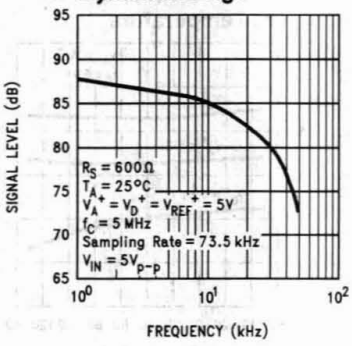
TL/H/11354–16

2

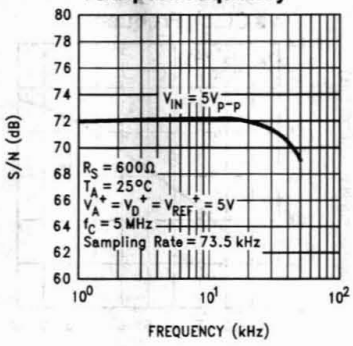
Typical Dynamic Performance Characteristics (Continued)

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

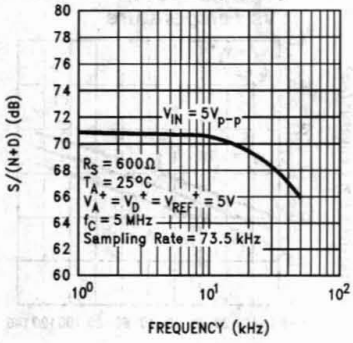
Bipolar Spurious Free Dynamic Range



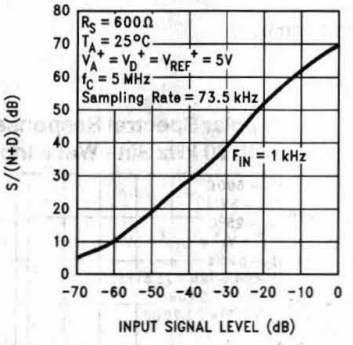
Unipolar Signal-to-Noise Ratio vs Input Frequency



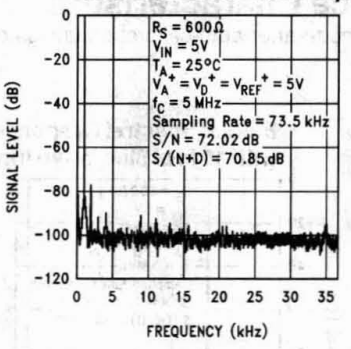
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



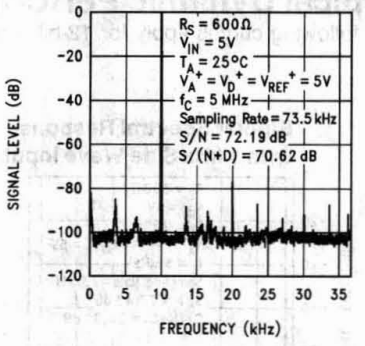
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



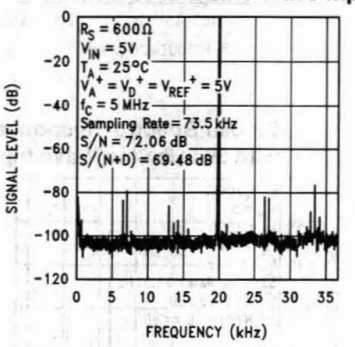
Unipolar Spectral Response with 1 kHz Sine Wave Input



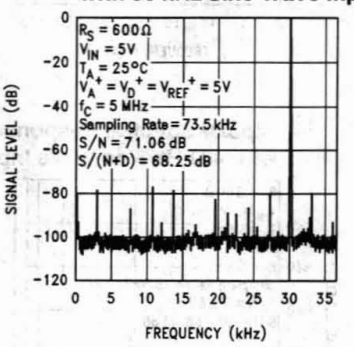
Unipolar Spectral Response with 10 kHz Sine Wave Input



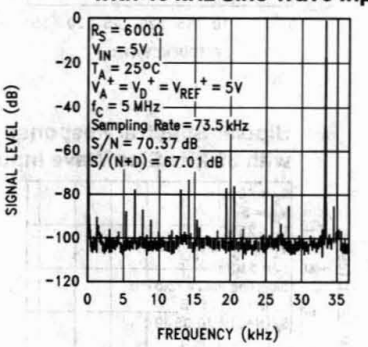
Unipolar Spectral Response with 20 kHz Sine Wave Input



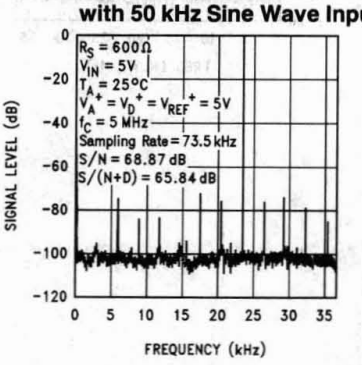
Unipolar Spectral Response with 30 kHz Sine Wave Input



Unipolar Spectral Response with 40 kHz Sine Wave Input



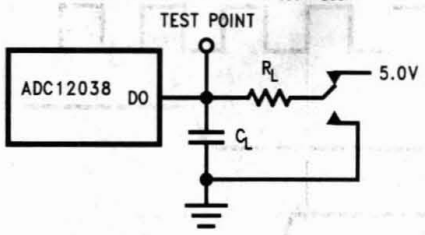
Unipolar Spectral Response with 50 kHz Sine Wave Input



TL/H/11354–17

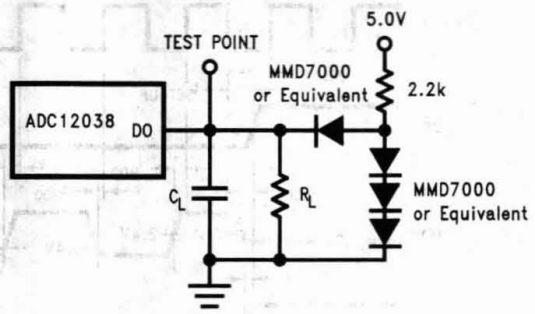
Test Circuits

DO "TRI-STATE" (t_{1H}, t_{0H})



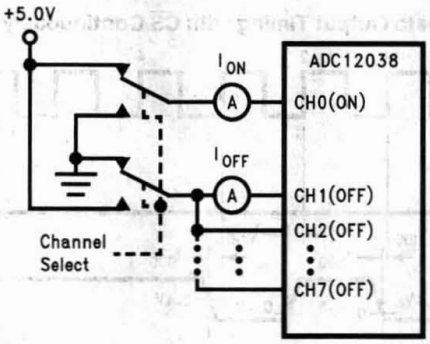
TL/H/11354-3

DO except "TRI-STATE"



TL/H/11354-4

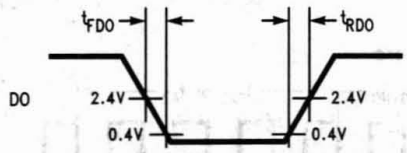
Leakage Current



TL/H/11354-5

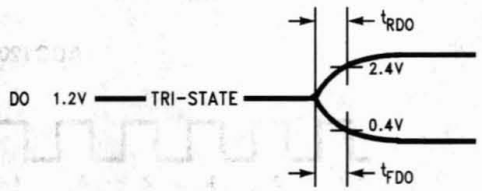
Timing Diagrams

DO Falling and Rising Edge



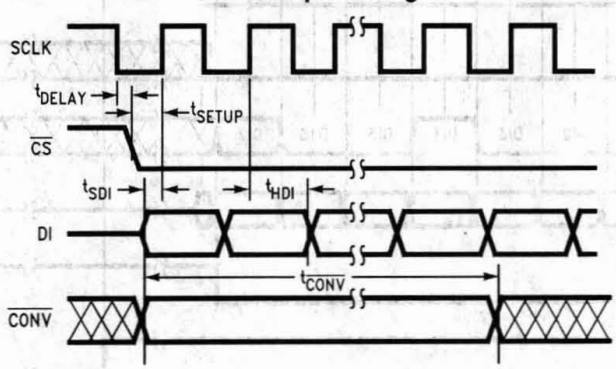
TL/H/11354-18

DO "TRI-STATE" Falling and Rising Edge



TL/H/11354-19

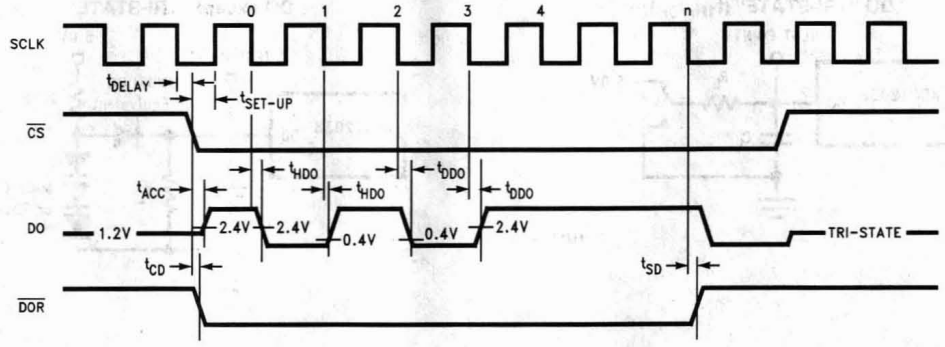
DI Data Input Timing



TL/H/11354-20

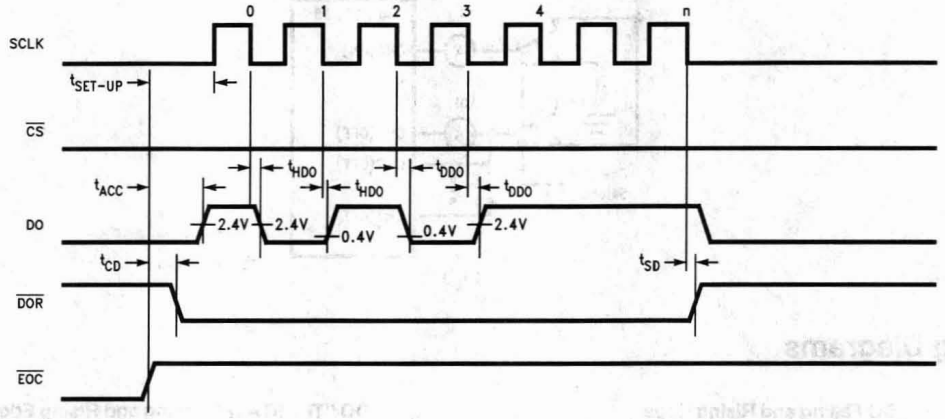
Timing Diagrams (Continued)

DO Data Output Timing Using $\overline{CS}$



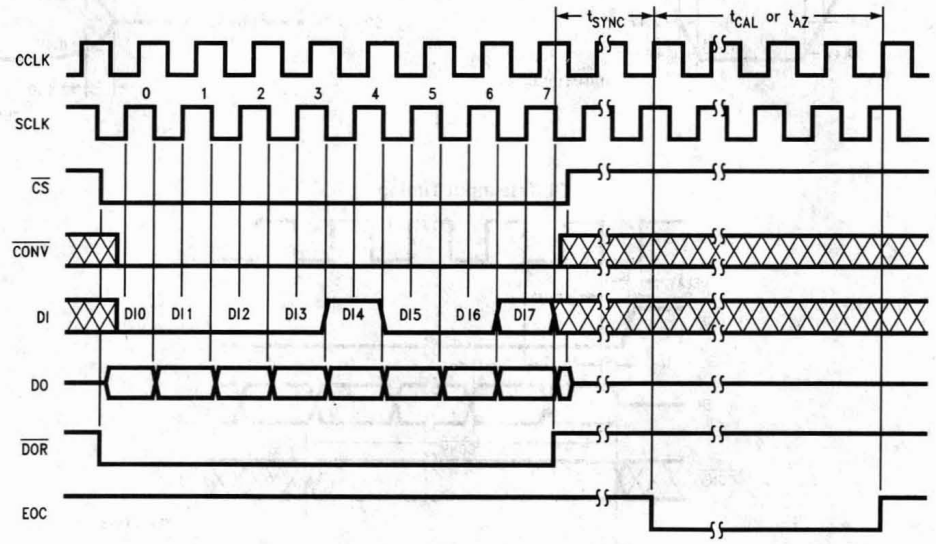
TL/H/11354–21

DO Data Output Timing with $\overline{CS}$ Continuously Low



TL/H/11354–22

ADC12038 Auto Cal or Auto Zero

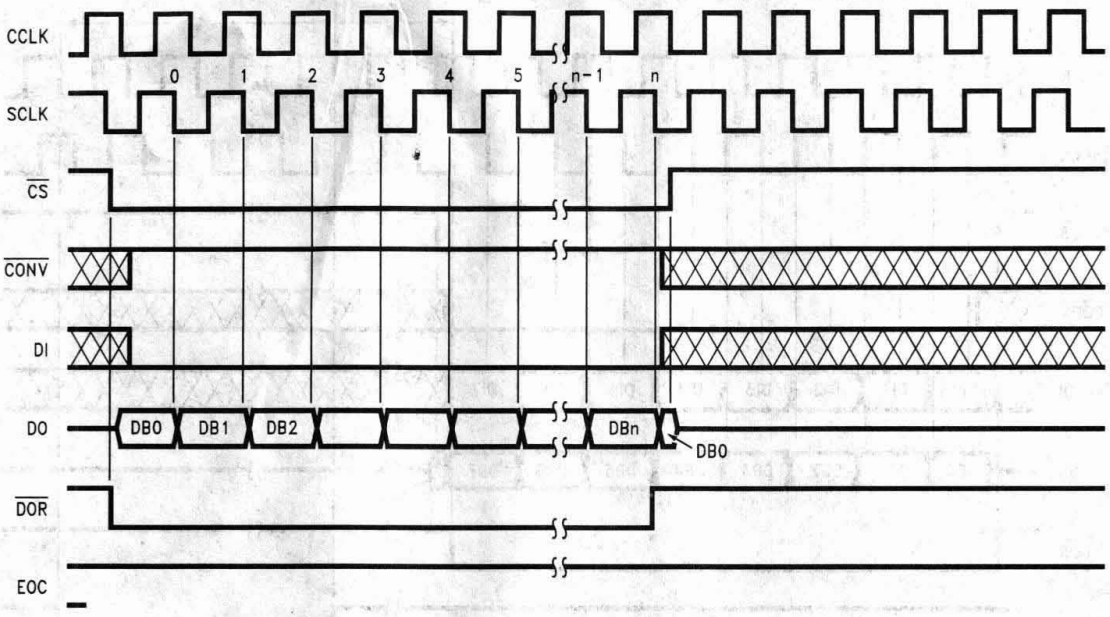


TL/H/11354–23

Note: DO output data is not valid during this cycle.

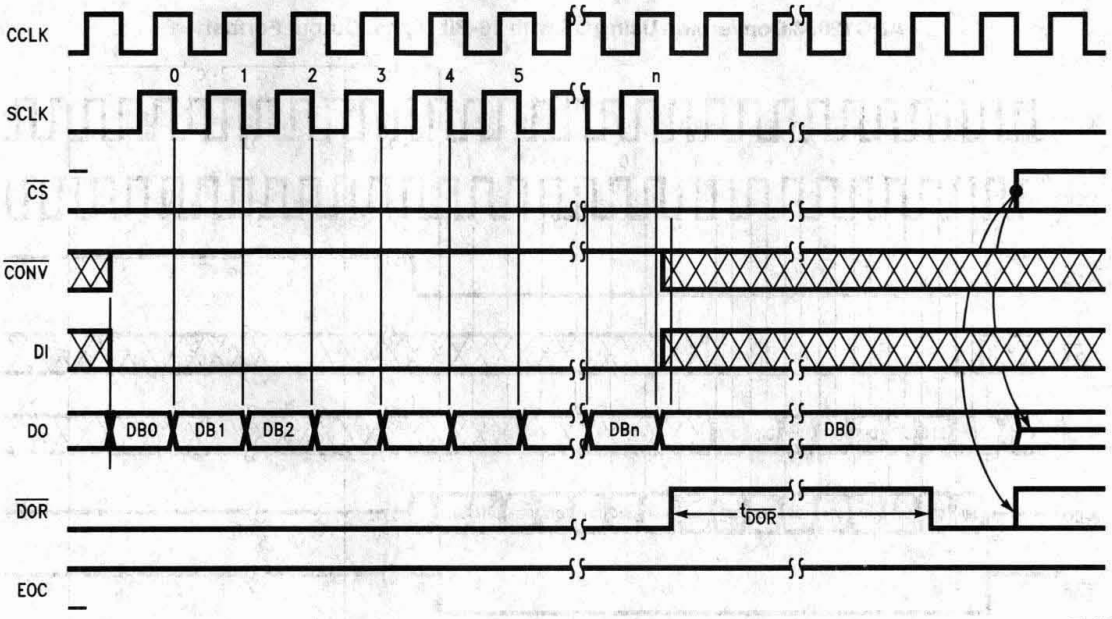
Timing Diagrams (Continued)

ADC12038 Read Data without Starting a Conversion Using $\overline{CS}$



TL/H/11354–24

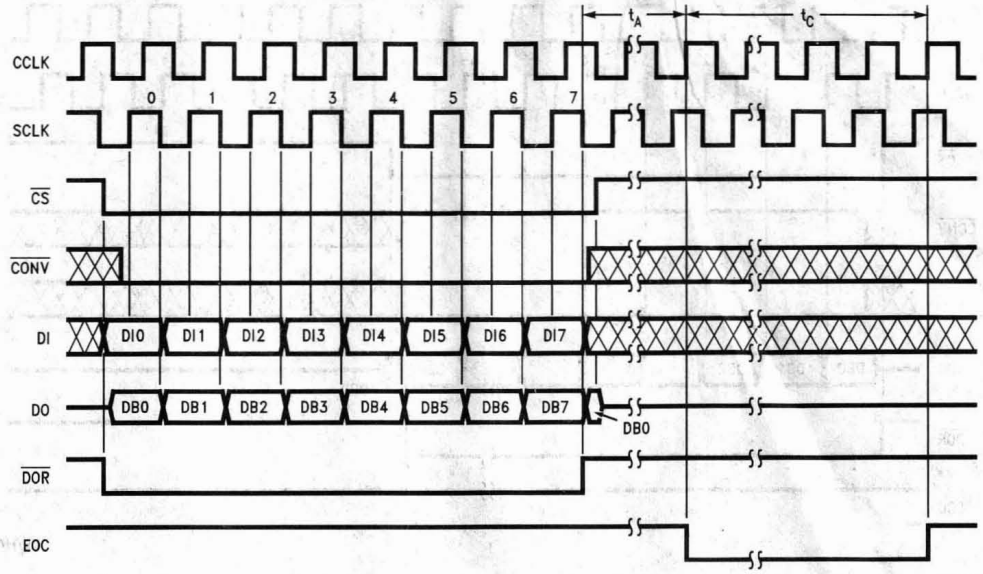
ADC12038 Read Data without Starting a Conversion with $\overline{CS}$ Continuously Low



TL/H/11354–25

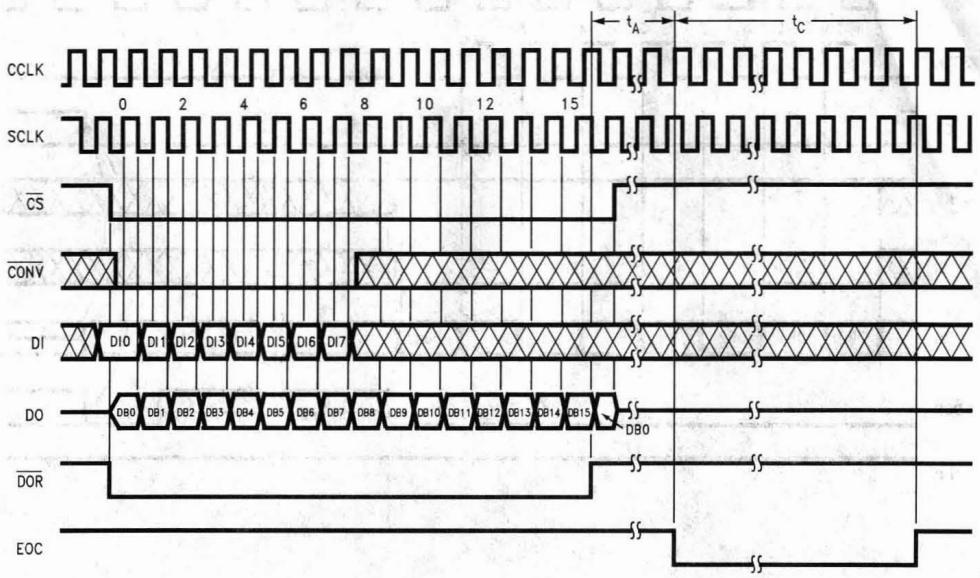
Timing Diagrams (Continued)

ADC12038 Conversion Using $\overline{CS}$ with 8-Bit Digital Output Format



TL/H/11354–26

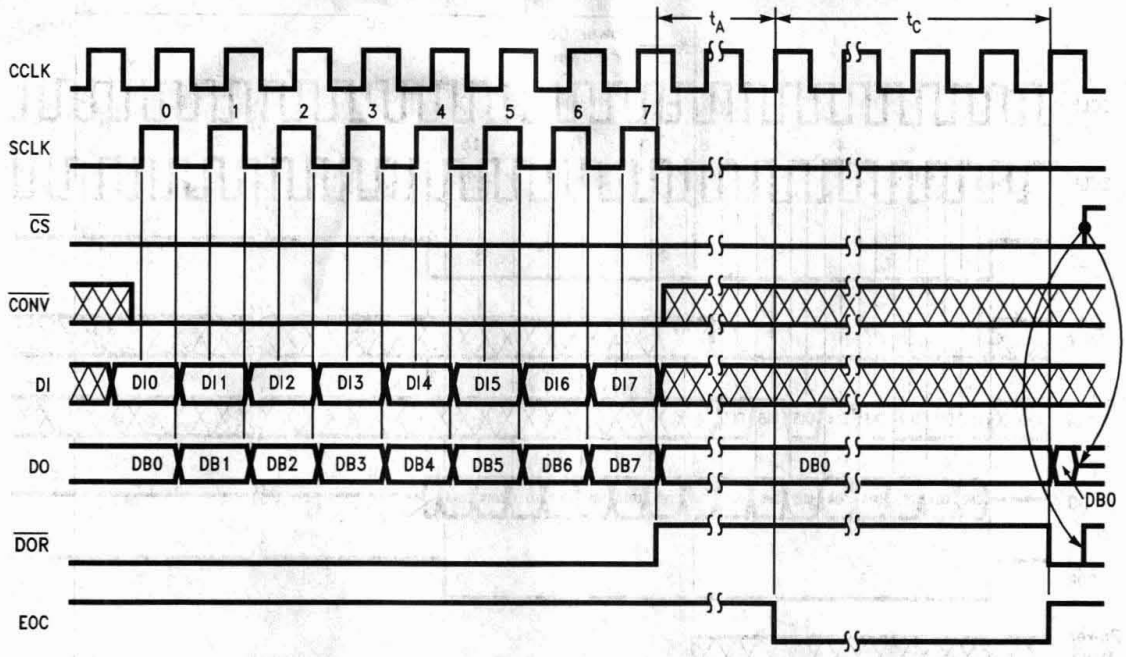
ADC12038 Conversion Using $\overline{CS}$ with 16-Bit Digital Output Format



TL/H/11354–51

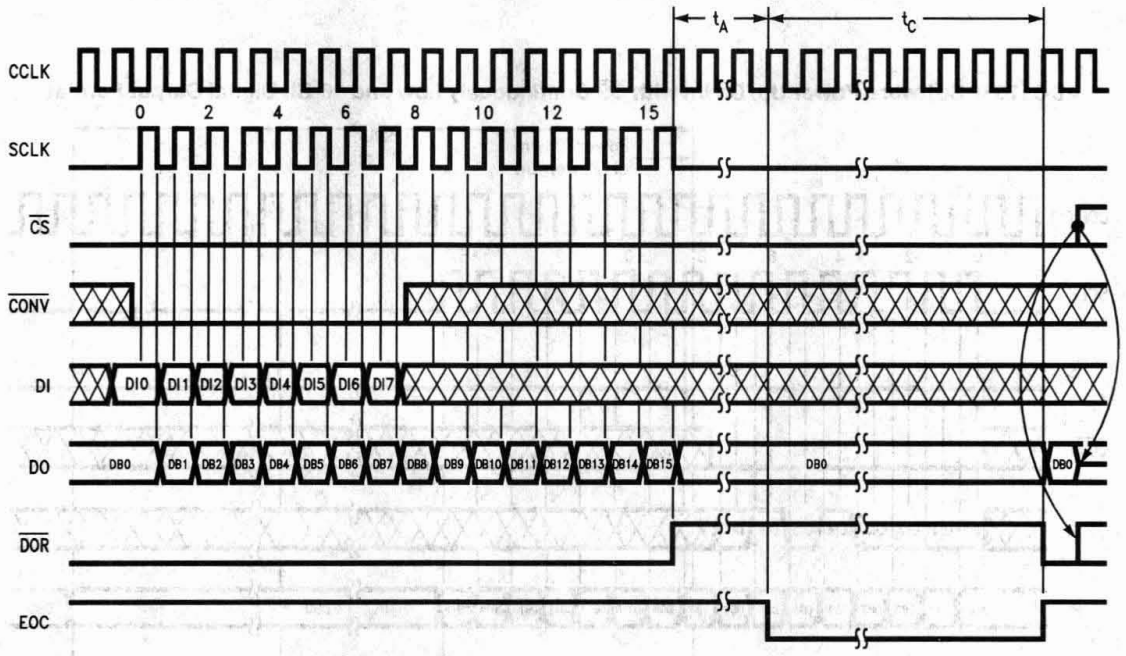
Timing Diagrams (Continued)

ADC12038 Conversion with $\overline{CS}$ Continuously Low and 8-Bit Digital Output Format



TL/H/11354–28

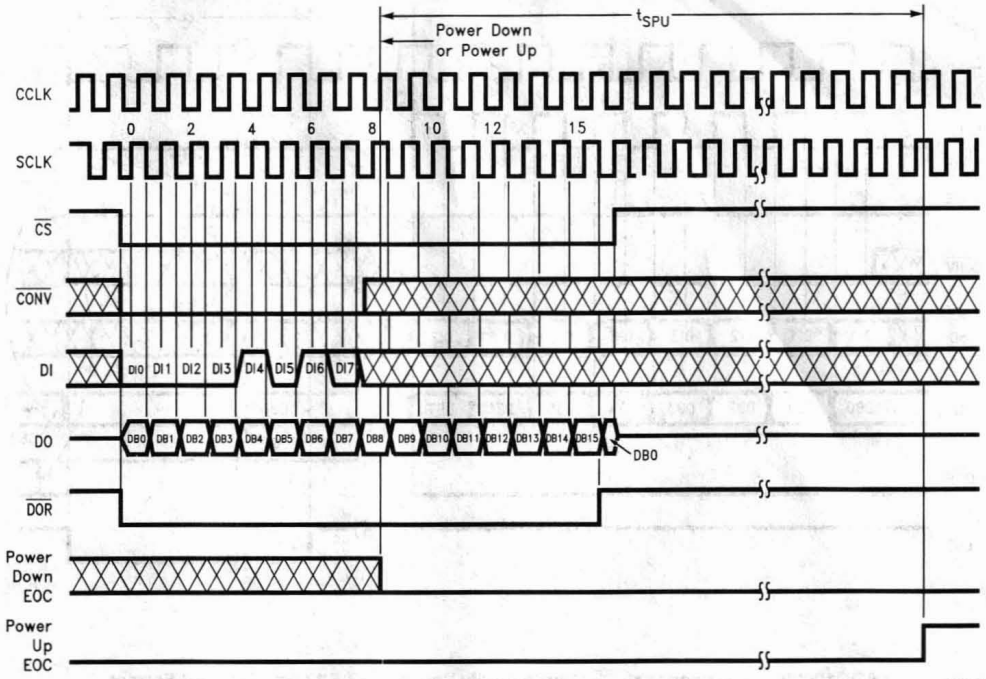
ADC12038 Conversion with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



TL/H/11354–29

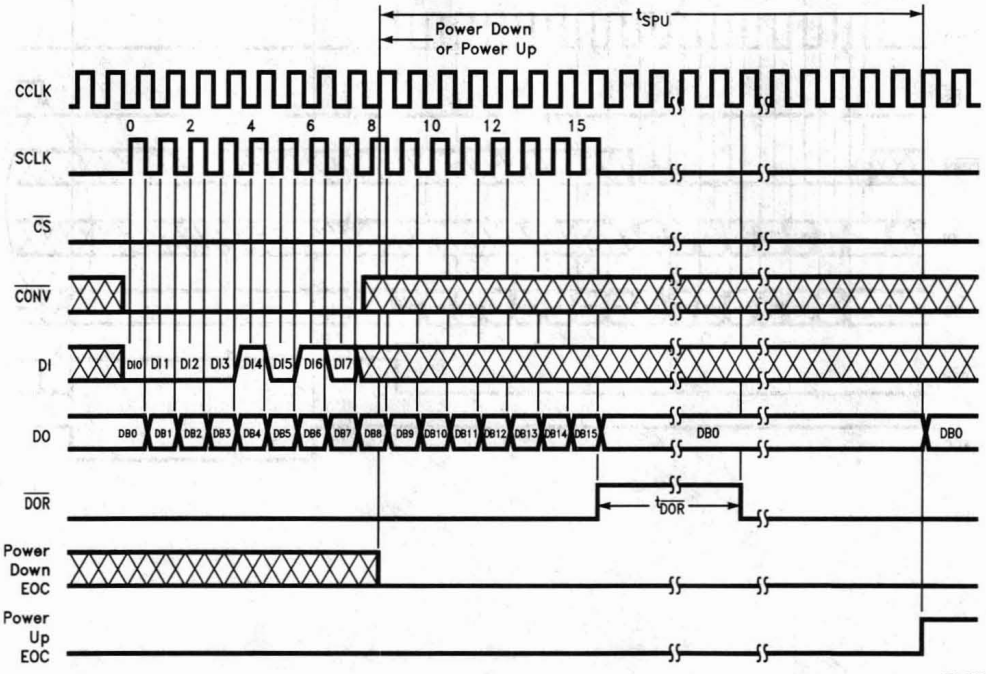
Timing Diagrams (Continued)

ADC12038 Software Power Up/Down Using $\overline{CS}$ with 16-Bit Digital Output Format



TL/H/11354–52

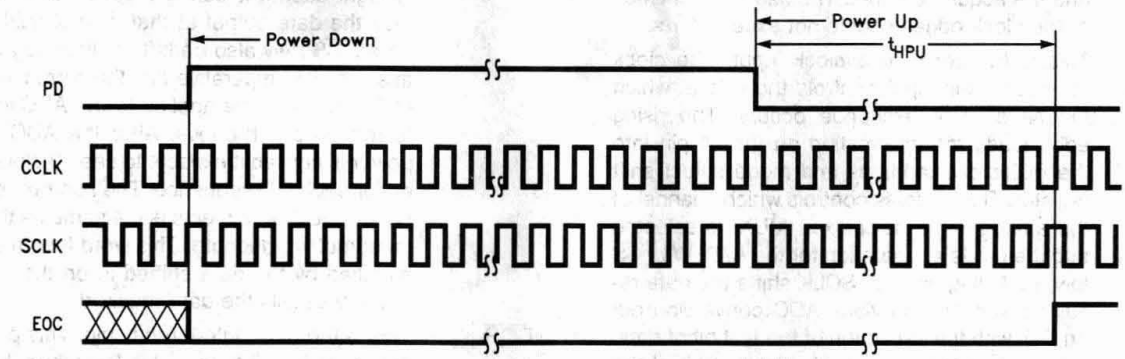
ADC12038 Software Power Up/Down with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



TL/H/11354–31

Timing Diagrams (Continued)

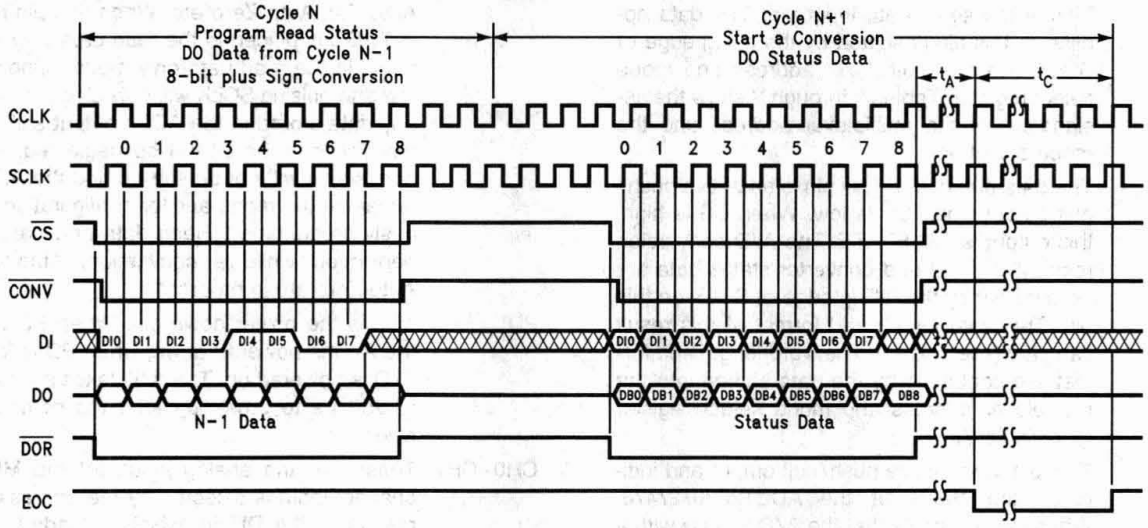
ADC12038 Hardware Power Up/Down



TL/H/11354–32

Note: Hardware power up/down may occur at any time. If PD is high while a conversion is in progress that conversion will be corrupted and erroneous data will be stored in the output shift register.

ADC12038 Configuration Modification—Example of a Status Read



TL/H/11354–33

Note: In order for all 9 bits of Status Information to be accessible, the last conversion programmed before Cycle N needs to have a resolution of 8 bits plus sign, 12 bits, 12 bits plus sign, or greater.

Pin Descriptions

CCLK — The clock applied to this input controls the successive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 μs.

SCLK — This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 μs.

DI — This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. Tables II through V show the assignment of the multiplexer address and the mode select data.

DO — The data output pin. This pin is an active push/pull output when $\overline{CS}$ is low. When $\overline{CS}$ is high, this output is TRI-STATE. The A/D conversion result (D0–D12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see Table I). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see Table V).

EOC — This pin is an active push/pull output and indicates the status of the ADC12030/2/4/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{CS}$ — This is the chip select pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought back low during a conversion, that conversion is prematurely terminated. The data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought back low during a conversion in progress the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. Table V details the data required.

$\overline{DOR}$ — This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{CONV}$ — A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming Table (Table V) such as 12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.

PD — This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 250 μs to power up after the command is given.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (see Tables II through IV).

The voltage applied to these inputs should not exceed V_A^+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2 — These are the multiplexer output pins.

A/DIN1, A/DIN2 — These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_A^+ or go below AGND (see *Figure 3*).

Pin Descriptions (Continued)

$V_{REF}+$ This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range of V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is 1 V_{DC} to 5.0 V_{DC} and the voltage at $V_{REF}+$ cannot exceed V_A+. See *Figure 4* for recommended bypassing.

$V_{REF}-$ The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND or exceed V_A+. (See *Figure 4*).

V_A+, V_D+ These are the analog and digital power supply pins. V_A+ and V_D+ are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see *Figure 4*). The operating voltage range of V_A+ and V_D+ is 4.5 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin (see *Figure 4*).

AGND This is the analog ground pin (see *Figure 4*).

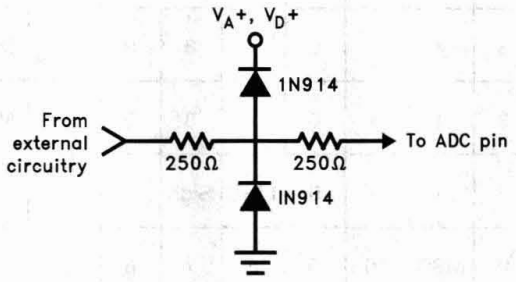


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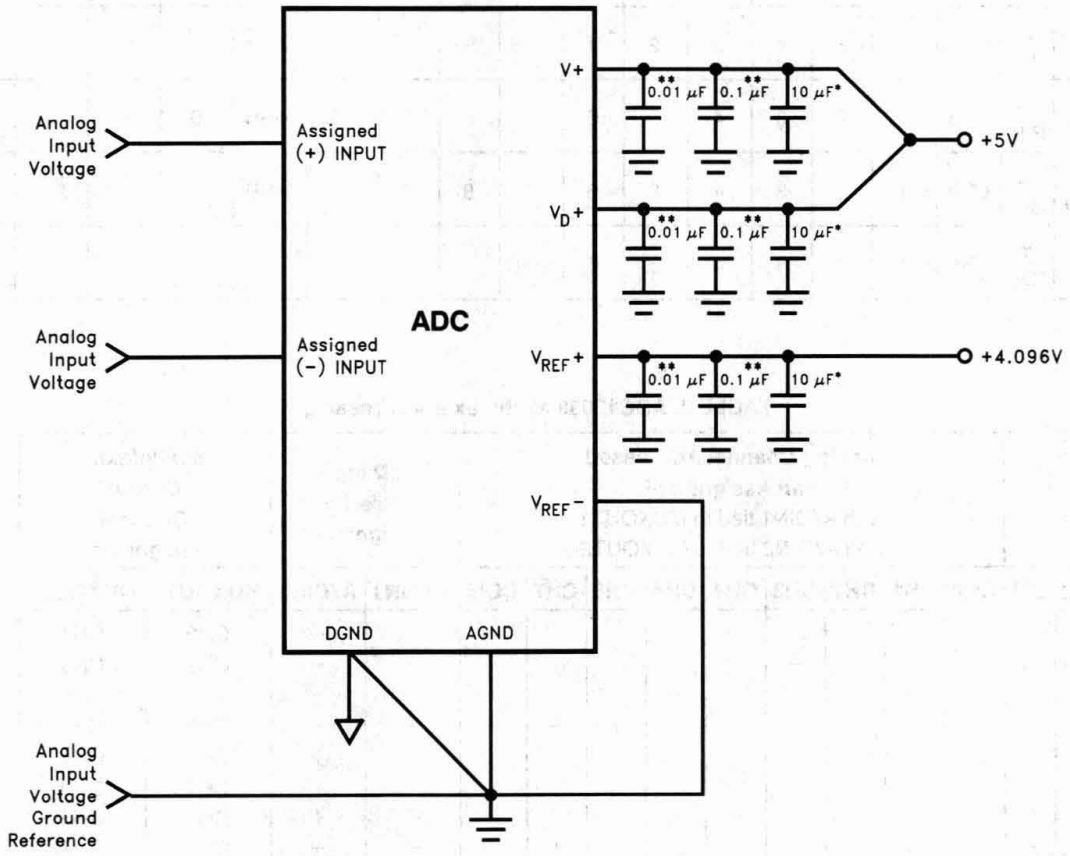
FIGURE 3. Protecting the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 Analog Pins



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*Tantalum

**Monolithic Ceramic or better

FIGURE 4. Recommended Power Supply Bypassing and Grounding

Tables

TABLE I. Data Out Formats

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	MSB First	17 Bits	X	X	X	X	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
		9 Bits	Sign	MSB	6	5	4	3	2	1	LSB								
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	X	X	X	X
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
		9 Bits	LSB	1	2	3	4	5	6	MSB	Sign								
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
		8 Bits	MSB	6	5	4	3	2	1	LSB									
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					
		8 Bits	LSB	1	2	3	4	5	6	MSB									

X = High or Low state.

TABLE II. ADC12038 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	DI3	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	−								+	−	CH0	CH1	Differential
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	Single-Ended
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

Tables (Continued)

TABLE III. ADC12034 Multiplexer Addressing

MUX Address			Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2					A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	CH0	CH1	CH2	CH3	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	+	−				+	−	CH0	CH1	Differential
L	L	H			+	−		+	−	CH2	CH3	
L	H	L	−	+				−	+	CH0	CH1	
L	H	H			−	+		−	+	CH2	CH3	
H	L	L	+				−	+	−	CH0	COM	Single-Ended
H	L	H			+		−	+	−	CH2	COM	
H	H	L		+			−	+	−	CH1	COM	
H	H	H				+	−	+	−	CH3	COM	

TABLE IV. ADC12032 and ADC12030 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-Ended
H	H		+	−	+	−	CH1	COM	

Note: ADC12030 and ADC12H030 do not have A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 pins.

Tables (Continued)

TABLE V. Mode Programming

ADC12038	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Selected (Current)	DO Format (next Conversion Cycle)
ADC12034	DI0	DI1	DI2		DI3	DI4	DI5	DI6		
ADC12030 and ADC12032	DI0	DI1			DI2	DI3	DI4	DI5		
	See Tables II, III or IV				L	L	L	L	12 Bit Conversion	12 or 13 Bit MSB First
	See Tables II, III or IV				L	L	L	H	12 Bit Conversion	16 or 17 Bit MSB First
	See Tables II, III or IV				L	L	H	L	8 Bit Conversion	8 or 9 Bit MSB First
	L	L	L	L	L	L	H	H	12 Bit Conversion of Full-Scale	12 or 13 Bit MSB First
	See Tables II, III or IV				L	H	L	L	12 Bit Conversion	12 or 13 Bit LSB First
	See Tables II, III or IV				L	H	L	H	12 Bit Conversion	16 or 17 Bit LSB First
	See Tables II, III or IV				L	H	H	L	8 Bit Conversion	8 or 9 Bit LSB First
	L	L	L	L	L	H	H	H	12 Bit Conversion of Offset	12 or 13 Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—6 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—10 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—18 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—34 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	X	X	X	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

Note: The A/D powers up with no Auto Cal, no Auto Zero, 10 CCLK acquisition time, 12-bit + sign conversion, power up, 12- or 13-bit MSB first, and user mode.
X = Don't Care

TABLE VI. Conversion/Read Data Only Mode Programming

$\overline{CS}$	$\overline{CONV}$	PD	Mode
L	L	L	See Table V for Mode
L	H	L	Read Only (Previous DO Format). No Conversion.
H	X	L	Idle
X	X	H	Power Down

X = Don't Care

Tables (Continued)

TABLE VII. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	PU	PD	Cal	8 or 9	12 or 13	16 or 17	Sign	Justification	Test Mode
Function	Device Status			DO Output Format Status					
	"High" indicates a Power Up Sequence is in progress	"High" indicates a Power Down Sequence is in progress	"High" indicates an Auto-Cal Sequence is in progress	"High" indicates an 8 or 9 bit format	"High" indicates a 12 or 13 bit format	"High" indicates a 16 or 17 bit format	"High" indicates that the sign bit is included. When "Low" the sign bit is not included.	When "High" the conversion result will be output MSB first. When "Low" the result will be output LSB first.	When "High" the device is in test mode. When "Low" the device is in user mode.

Application Hints

1.0 DIGITAL INTERFACE

1.1 Interface Concepts

The example in *Figure 5* shows a typical sequence of events after the power is applied to the ADC12030/2/4/8:

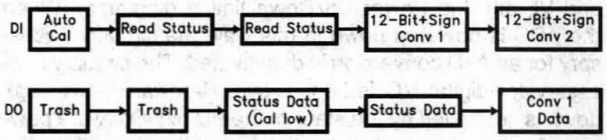

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FIGURE 5. Typical Power Supply Power Up Sequence

The first instruction input to the A/D via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To determine whether the Auto Cal has been completed, a read status instruction is issued to the A/D. Again the data output at that time has no significance since the Auto Cal procedure modifies the data in the output shift register. To retrieve the status information, an additional read status instruction is issued to the A/D. At this time the status data is available on DO. If the Cal signal in the status word, is low Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output at this time is again status information. To keep noise from corrupting the A/D conversion, status can not be read during a conversion. If $\overline{CS}$ is strobed and is brought low during a conversion, that conversion is prematurely ended. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to comnmunicate to the A/D again. Once it has been determined that the A/D has completed a conversion, another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

Note, when $\overline{CS}$ is low continuously it is important to transmit the exact number of SCLK cycles, as shown in the timing diagrams. Not doing so will desynchronize the serial communication to the A/D. (See Section 1.3.)

1.2 Changing Configuration

The configuration of the ADC12030/2/4/8 on power up defaults to 12-bit plus sign resolution, 12- or 13-bit MSB First, 10 CCLK acquisition time, user mode, no Auto Cal, no Auto Zero, and power up mode. Changing the aquisition time and turning the sign bit on and off requires an 8-bit instruction to be issued to the ADC. This instruction will not start a conversion. The instructions that select a multiplexer address and format the output data do start a conversion. *Figure 6* describes an example of changing the configuration of the ADC12030/2/4/8.

During I/O sequence 1, the instruction on DI configures the ADC12030/2/4/8 to do a conversion with 12-bit + sign resolution. Notice that when the 6 CCLK Acquisition and Data Out without Sign instructions are issued to the ADC, I/O sequences 2 and 3, a new conversion is not started. The data output during these instructions is from conversion N which was started during I/O sequence 1. The Configuration Modification timing diagram describes in detail the sequence of events necessary for a Data Out without Sign, Data Out with Sign, or 6/10/18/34 CCLK Acquisition time mode selection. Table V describes the actual data necessary to be input to the ADC to accomplish this configuration modification. The next instruction, shown in *Figure 6*, issued to the A/D starts conversion N+1 with 8 bits of resolution formatted MSB first. Again the data output during this I/O cycle is the data from conversion N.

The number of SCLKs applied to the A/D during any conversion I/O sequence should vary in accord with the data out word format chosen during the previous conversion I/O sequence. The various formats and resolutions available are shown in Table I. In *Figure 6*, since 8-bit without sign MSB first format was chosen during I/O sequence 4, the number of SCLKs required during I/O sequence 5 is 8. In the following I/O sequence the format changes to 12-bit without sign MSB first; therefore the number of SCLKs required during I/O sequence 6 changes accordingly to 12.

1.3 $\overline{CS}$ Low Continuously Considerations

When $\overline{CS}$ is continuously low, it is important to transmit the exact number of SCLK pulses that the ADC expects. Not doing so will desynchronize the serial communications to the ADC. When the supply power is first applied to the ADC,

Application Hints (Continued)

it will expect to see 13 SCLK pulses for each I/O transmission. The number of SCLK pulses that the ADC expects to see is the same as the digital output word length. The digital output word length is controlled by the Data Out (DO) format. The DO format maybe changed any time a conversion is started or when the sign bit is turned on or off. The table below details out the number of clock periods required for different DO formats:

DO Format		Number of SCLKs Expected
8-Bit MSB or LSB First	SIGN OFF	8
	SIGN ON	9
12-Bit MSB or LSB First	SIGN OFF	12
	SIGN ON	13
16-Bit MSB or LSB first	SIGN OFF	16
	SIGN ON	17

If erroneous SCLK pulses desynchronize the communications, the simplest way to recover is by cycling the power supply to the device. Not being able to easily resynchronize the device is a shortcoming of leaving $\overline{CS}$ low continuously.

The number of clock pulses required for an I/O exchange may be different for the case when $\overline{CS}$ is left low continuously vs the case when $\overline{CS}$ is cycled. Take the I/O sequence detailed in *Figure 5* (Typical Power Supply Sequence) as an example. The table below lists the number of SCLK pulses required for each instruction:

Instruction	$\overline{CS}$ Low Continuously	$\overline{CS}$ Strobed
Auto Cal	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 1	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 2	13 SCLKs	13 SCLKs

1.4 Analog Input Channel Selection

The data input on DI also selects the channel configuration for a particular A/D conversion (see Tables II, III, IV and V).

In *Figure 6* the only times when the channel configuration could be modified would be during I/O sequences 1, 4, 5 and 6. Input channels are reselected before the start of each new conversion. Shown below is the data bit stream required on DI, during I/O sequence number 4 in *Figure 6*, to set CH1 as the positive input and CH0 as the negative input for the different versions of ADCs:

Part Number	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
ADC12H030 ADC12030	L	H	L	L	H	L	X	X
ADC12H032 ADC12032	L	H	L	L	H	L	X	X
ADC12H034 ADC12034	L	H	L	L	L	H	L	X
ADC12H038 ADC12038	L	H	L	L	L	L	H	L

Where X can be a logic high (H) or low (L).

1.5 Power Up/Down

The ADC may be powered down at any time by taking the PD pin HIGH or by the instruction input on DI (see Tables V and VI, and the Power Up/Down timing diagrams). When the ADC is powered down in this way, the circuitry necessary for an A/D conversion is deactivated. The circuitry necessary for digital I/O is kept active. Hardware power up/down is controlled by the state of the PD pin. Software power-up/down is controlled by the instruction issued to the ADC. If a software power up instruction is issued to the ADC while a hardware power down is in effect (PD pin high) the device will remain in the power-down state. If a software power down instruction is issued to the ADC while a hardware power up is in effect (PD pin low), the device will power down. When the device is powered down by software, it may be powered up by either issuing a software power up instruction or by taking PD pin high and then low. If the power down command is issued during an A/D conversion, that conversion is disrupted. Therefore, the data output after power up cannot be relied upon.

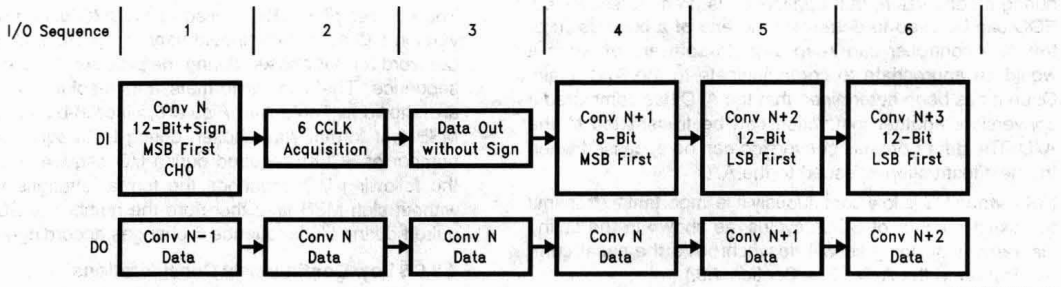

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FIGURE 6. Changing the ADC's Conversion Configuration

Application Hints (Continued)

1.6 User Mode and Test Mode

An instruction may be issued to the ADC to put it into test mode. Test mode is used by the manufacturer to verify complete functionality of the device. During test mode CH0–CH7 become active outputs. If the device is inadvertently put into the test mode with $\overline{CS}$ continuously low, the serial communications may be desynchronized. Synchronization may be regained by cycling the power supply voltage to the device. Cycling the power supply voltage will also set the device into user mode. If $\overline{CS}$ is used in the serial interface, the ADC may be queried to see what mode it is in. This is done by issuing a "read STATUS register" instruction to the ADC. When bit 9 of the status register is high, the ADC is in test mode; when bit 9 is low the ADC, is in user mode. As an alternative to cycling the power supply, an instruction sequence may be used to return the device to user mode. This instruction sequence must be issued to the ADC using $\overline{CS}$. The following table lists the instructions required to return the device to user mode:

Instruction	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
TEST MODE	H	X	X	X	H	H	H	H
Reset Test Mode Instructions	L	L	L	L	H	H	H	L
	L	L	L	L	H	L	H	L
	L	L	L	L	H	L	H	H
USER MODE	L	L	L	L	H	H	H	H
Power Up	L	L	L	L	H	L	H	L
Set DO with or without Sign	H or L	L	L	L	H	H	L	H
Set Acquisition Time	H or L	H or L	L	L	H	H	H	L
Start a Conversion	H or L	H or L	H or L	H or L	L	H or L	H or L	H or L

X = Don't Care

After returning to user mode with the user mode instruction the power up, data with or without sign, and acquisition time instructions need to be resent to ensure that the ADC is in the required state before a conversion is started.

1.7 Reading the Data Without Starting a Conversion

The data from a particular conversion may be accessed without starting a new conversion by ensuring that the $\overline{CONV}$ line is taken high during the I/O sequence. See the Read Data timing diagrams. Table VI describes the operation of the $\overline{CONV}$ pin.

2.0 DESCRIPTION OF THE ANALOG MULTIPLEXER

For the ADC12038, the analog input multiplexer can be configured with 4 differential channels or 8 single ended channels with the COM input as the zero reference or any combination thereof (see *Figure 7*). The difference between the voltages on the V_{REF}^+ and V_{REF}^- pins determines the input voltage span (V_{REF}). The analog input voltage range is 0 to V_A^+. Negative digital output codes result when $V_{IN}^- > V_{IN}^+$. The actual voltage at V_{IN}^- or V_{IN}^+ cannot go below AGND.

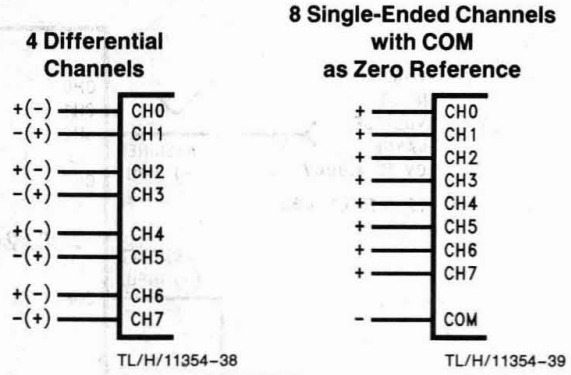

FIGURE 7

CH0, CH2, CH4, and CH6 can be assigned to the MUXOUT1 pin in the differential configuration, while CH1, CH3, CH5, and CH7 can be assigned to the MUXOUT2 pin. In the differential configuration, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The A/DIN1 and A/DIN2 pins can be assigned positive or negative polarity.

Application Hints (Continued)

With the single-ended multiplexer configuration CH0 through CH7 can be assigned to the MUXOUT1 pin. The COM pin is always assigned to the MUXOUT2 pin. A/DIN1 is assigned as the positve input; A/DIN2 is assigned as the negative input. (See *Figure 8*).

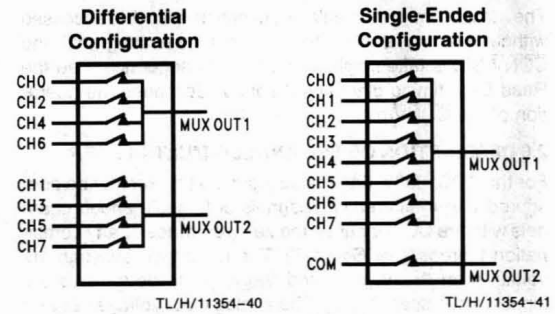

FIGURE 8

The Multiplexer assignment tables for the ADC12030,2,4,8 (Tables II, III, and IV) summarize the aforementioned functions for the different versions of A/Ds.

2.1 Biasing for Various Multiplexer Configurations

Figure 9 is an example of biasing the device for single-ended operation. The sign bit is always low. The digital output range is 0 0000 0000 0000 to 0 1111 1111 1111. One LSB is equal to 1 mV (4.1V/4096 LSBs).

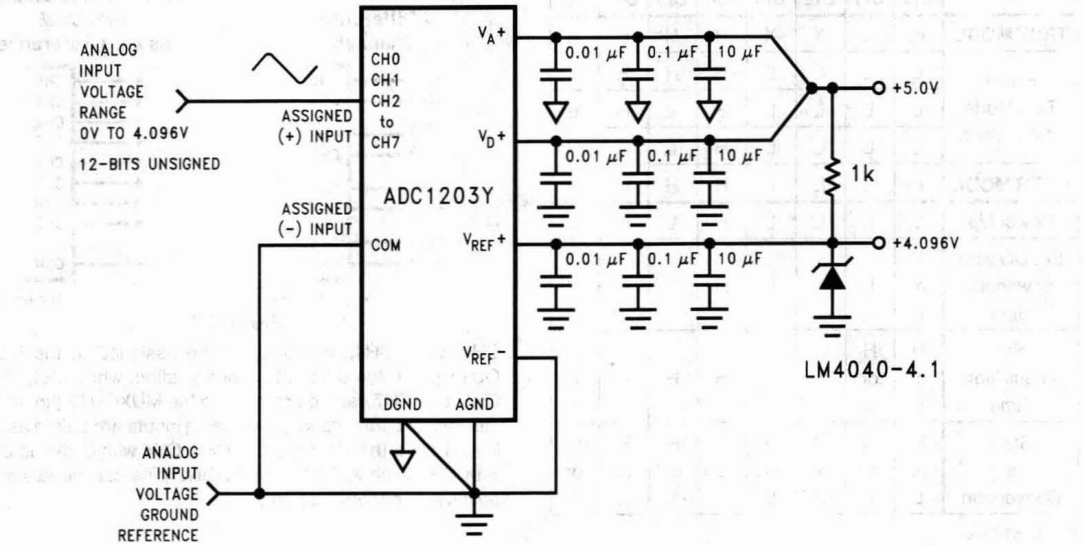

FIGURE 9. Single-Ended Biasing

Application Hints (Continued)

For pseudo-differential signed operation, the biasing circuit shown in *Figure 10* shows a signal AC coupled to the ADC. This gives a digital output range of −4096 to +4095. With a 2.5V reference, as shown, 1 LSB is equal to 610 μV. Although, the ADC is not production tested with a 2.5V reference, linearity error typically will not change more than 0.1 LSB (see the curves in the Typical Electrical Characteristics Section). With the ADC set to an acquisition time of 10 clock periods, the input biasing resistor needs to be 600Ω or less. Notice though that the input coupling capacitor needs to be made fairly large to bring down the high pass corner. Increasing the acquisition time to 34 clock periods (with a 5 MHz CCLK frequency) would allow the 600Ω to increase to 6k, which with a 1 μF coupling capacitor would set the high pass corner at 26 Hz. Increasing R, to 6k would allow R_2 to be 2k.

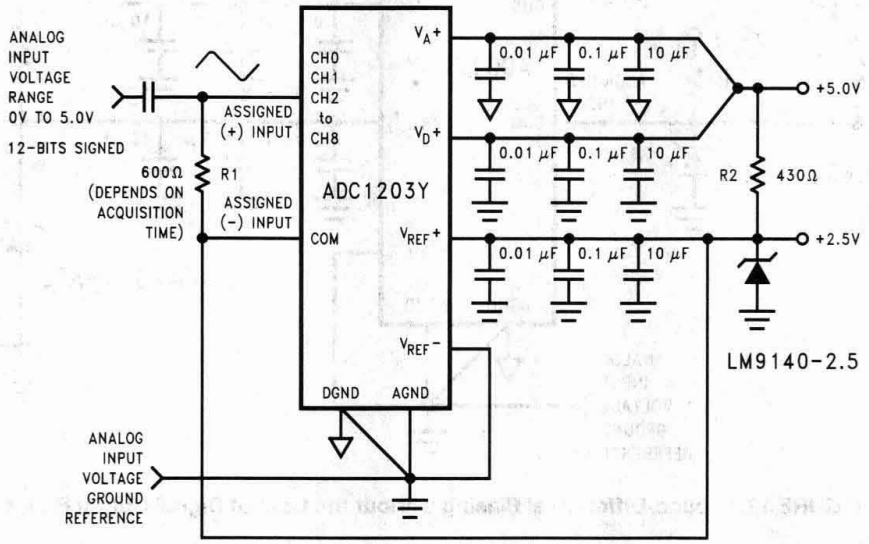

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FIGURE 10. Pseudo-Differential Biasing with the Signal Source AC Coupled Directly into the ADC

An alternative method for biasing pseudo-differential operation is to use the +2.5V from the LM9140 to bias any amplifier circuits driving the ADC as shown in *Figure 11*. The value of the resistor pull-up biasing the LM9140-2.5 will depend upon the current required by the op amp biasing circuitry.

In the circuit of *Figure 11* some voltage range is lost since the amplifier will not be able to swing to +5V and GND with a single +5V supply. Using an adjustable version of the LM4041 to set the full scale voltage at exactly 2.048V and a lower grade LM4040D-2.5 to bias up everything to 2.5V as shown in *Figure 12* will allow the use of all the ADC's digital output range of −4096 to +4095 while leaving plenty of head room for the amplifier.

Fully differential operation is shown in *Figure 13*. One LSB for this case is equal to (4.1V/4096) = 1 mV.

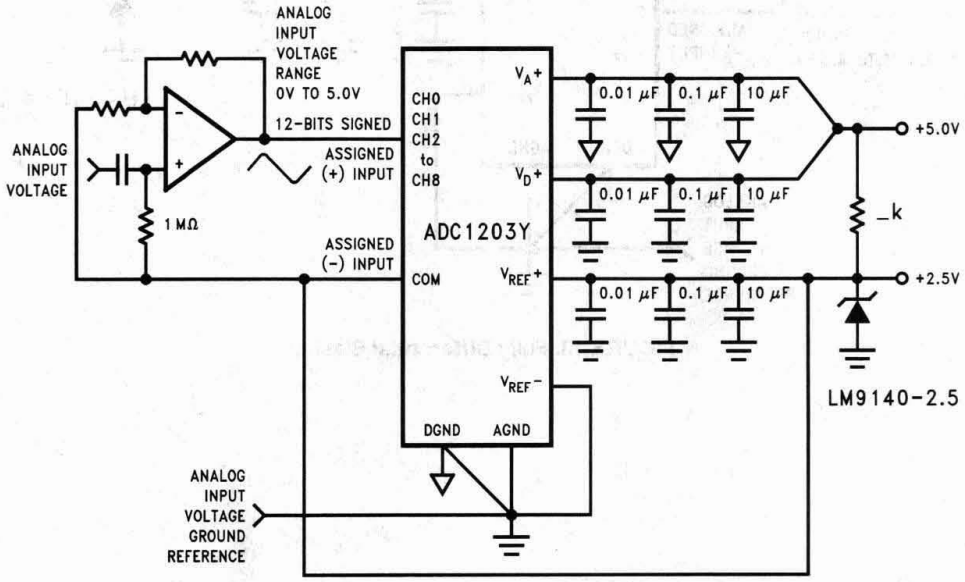

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FIGURE 11. Alternative Pseudo-Differential Biasing

Application Hints (Continued)

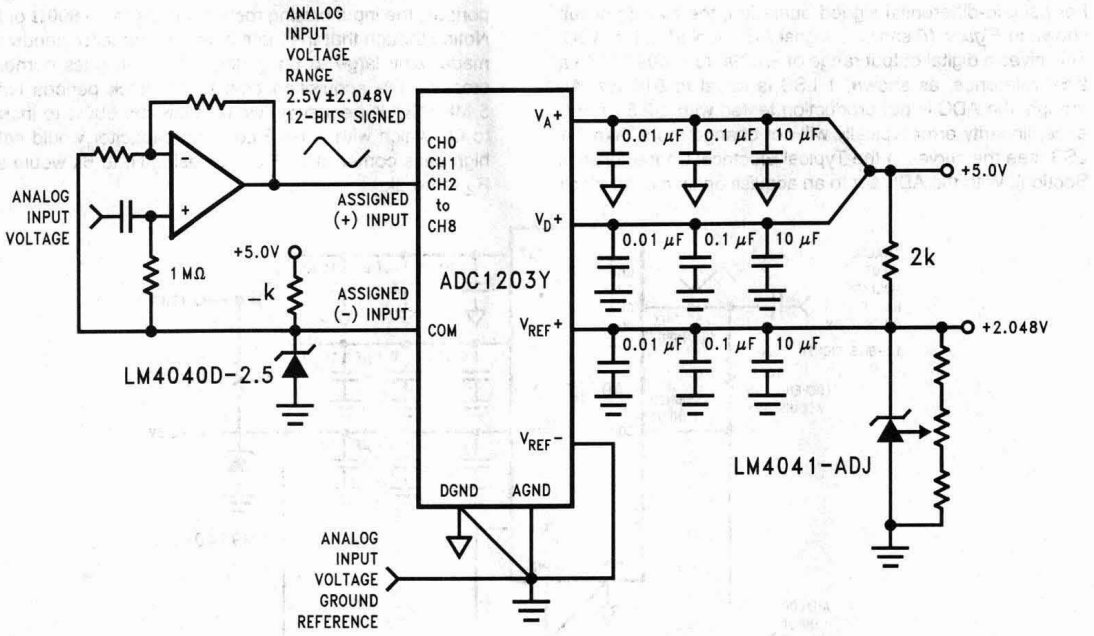

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FIGURE 12. Pseudo-Differential Biasing without the Loss of Digital Output Range

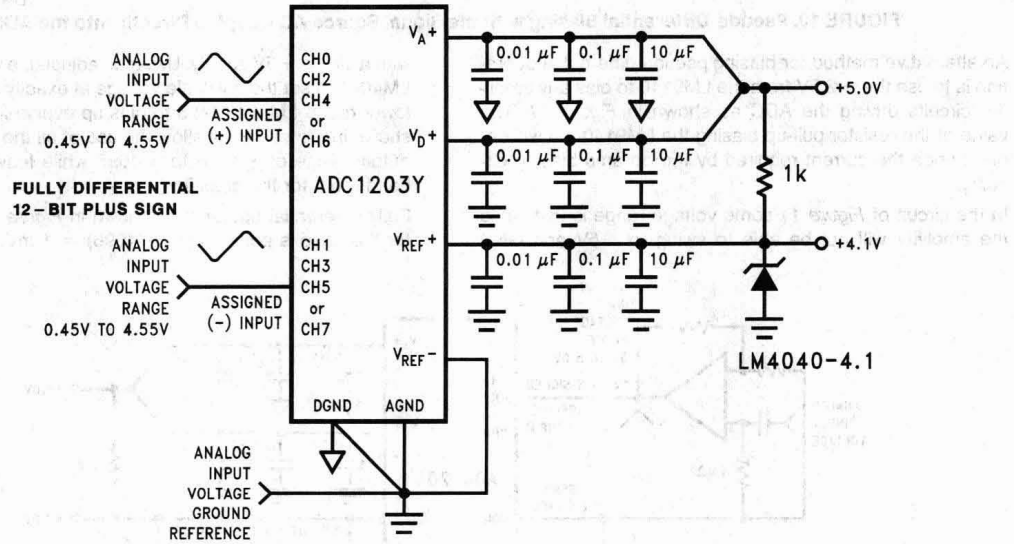

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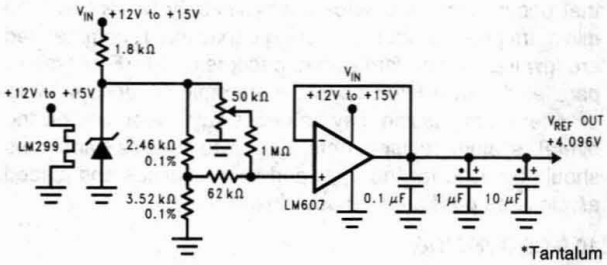
FIGURE 13. Fully Differential Biasing

Application Hints (Continued)

3.0 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF}^+ and V_{REF}^- defines the analog input span (the difference between the voltage applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF}^+ or V_{REF}^- must have very low output impedance and noise. The circuit in *Figure 14* is an example of a very stable reference appropriate for use with the device.



*Tantalum

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FIGURE 14. Low Drift Extremely Stable Reference Circuit

The ADC 12030/2/4/8 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF}^+ pin is connected to V_A^+ and V_{REF}^- is connected to ground. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

Below are recommended references along with some key specifications.

Part Number	Output Voltage Tolerance	Temperature Coefficient
LM4041CI-Adj	±0.5%	±100ppm/°C
LM4040AI-4.1	±0.1%	±100ppm/°C
LM9140BYZ-4.1	±0.5%	±25ppm/°C
LM368Y-5.0	±0.1%	±20ppm/°C
Circuit of *Figure 14*	Adjustable	±2ppm/°C

The reference voltage inputs are not fully differential. The ADC12030/2/4/8 will not generate correct conversions or comparisons if V_{REF}^+ is taken below V_{REF}^-. Correct conversions result when V_{REF}^+ and V_{REF}^- differ by 1V and remain, at all times, between ground and V_A^+. The V_{REF} common mode range, $(V_{REF}^+ + V_{REF}^-)/2$ is restricted to $(0.1 \times V_A^+)$ to $(0.6 \times V_A^+)$. Therefore, with $V_A^+ = 5V$ the center of the reference ladder should not go below 0.5V or above 3.0V. *Figure 15* is a graphic representation of the voltage restrictions on V_{REF}^+ and V_{REF}^-.

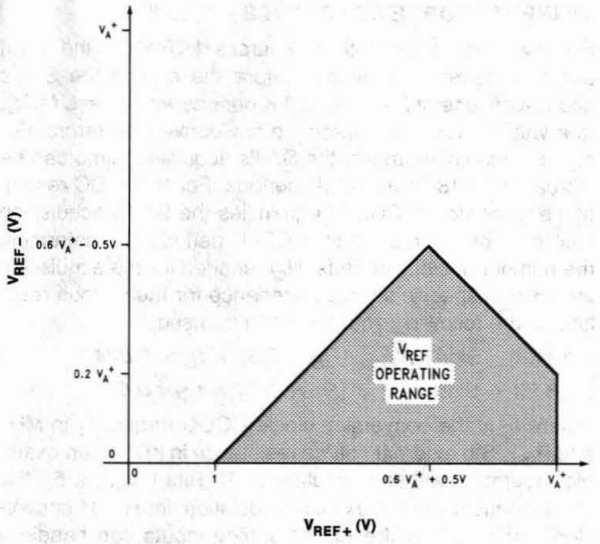

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FIGURE 15. V_{REF} Operating Range

4.0 ANALOG INPUT VOLTAGE RANGE

The ADC12030/2/4/8's fully differential ADC generate a two's complement output that is found by using the equations shown below:

for (12-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-)\,(4096)}{(V_{REF}^+ - V_{REF}^-)}$$

for (8-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-)\,(256)}{(V_{REF}^+ - V_{REF}^-)}$$

Round off to the nearest integer value between −4096 to 4095 for 12-bit resolution and between −256 to 255 for 8-bit resolution if the result of the above equation is not a whole number.

Examples are shown in the table below:

V_{REF}^+	V_{REF}^-	V_{IN}^+	V_{IN}^-	Digital Output Code
+2.5V	+1V	+1.5V	0V	0,1111,1111,1111
+4.096V	0V	+3V	0V	0,1011,1011,1000
+4.096V	0V	+2.499V	+2.500V	1,1111,1111,1111
+4.096V	0V	0V	+4.096V	1,0000,0000,0000

5.0 INPUT CURRENT

At the start of the acquisition window (t_A) a charging current flows into or out of the analog input pins (A/DIN1 and A/DIN2) depending on the input voltage polarity. The analog input pins are CH0–CH7 and COM when A/DIN1 is tied to MUXOUT1 and A/DIN2 is tied to MUXOUT2. The peak value of this input current will depend on the actual input voltage applied, the source impedance and the internal multiplexer switch on resistance. With MUXOUT1 tied to A/DIN1 and MUXOUT2 tied to A/DIN2 the internal multiplexer switch on resistance is typically 1.6 kΩ. The A/DIN1 and A/DIN2 mux on resistance is typically 750Ω.

Application Hints (Continued)

6.0 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<600Ω), the input charging current will decay, before the end of the S/H's acquisition time of 2 μs (10 CCLK periods with f_C = 5 MHz), to a value that will not introduce any conversion errors. For high source impedances, the S/H's acquisition time can be increased to 18 or 34 CCLK periods. For less ADC resolution and/or slower CCLK frequencies the S/H's acquisition time may be decreased to 6 CCLK periods. To determine the number of clock periods (N_c) required for the acquisition time with a specific source impedance for the various resolutions the following equations can be used:

12 Bit + Sign $N_C = [R_S + 2.3] \times f_C \times 0.824$

8 Bit + Sign $N_C = [R_S + 2.3] \times f_C \times 0.57$

Where f_C is the conversion clock (CCLK) frequency in MHz and R_S is the external source resistance in kΩ. As an example, operating with a resolution of 12 Bits+sign, a 5 MHz clock frequency and maximum acquistion time of 34 conversion clock periods the ADC's analog inputs can handle a source impedance as high as 6 kΩ. The acquisition time may also be extended to compensate for the settling or response time of external circuitry connected between the MUXOUT and A/DIN pins.

The acquisition time t_A is started by a falling edge of SCLK and ended by a rising edge of CCLK (see timing diagrams). If SCLK and CCLK are asynchronous one extra CCLK clock period may be inserted into the programmed acquisition time for synchronization. Therefore with asnychronous SCLK and CCLKs the acquisition time will change from conversion to conversion.

7.0 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, CH0–CH7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

8.0 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

9.0 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. The minimum power supply bypassing capacitors recommended are low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF monolithic ceramic capacitors. More or different bypassing may be necessary depending on the overall system requirements. Separate bypass capacitors should be used for the V_A^+ and V_D^+ supplies and placed as close as possible to these pins.

10.0 GROUNDING

The ADC12030/2/4/8's performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all components that handle analog signals. The digital and analog ground planes are connected together at only one point, either the power supply ground or at the pins of the ADC. This greatly reduces the occurence of ground loops and noise.

Shown in *Figure 16* is the ideal ground plane layout for the ADC12038 along with ideal placement of the bypass capacitors. The circuit board layout shown in *Figure 16* uses three bypass capacitors: 0.01 μF (C1) and 0.1 μF (C2) surface mount capacitors and 10 μF (C3) tantalum capacitor.

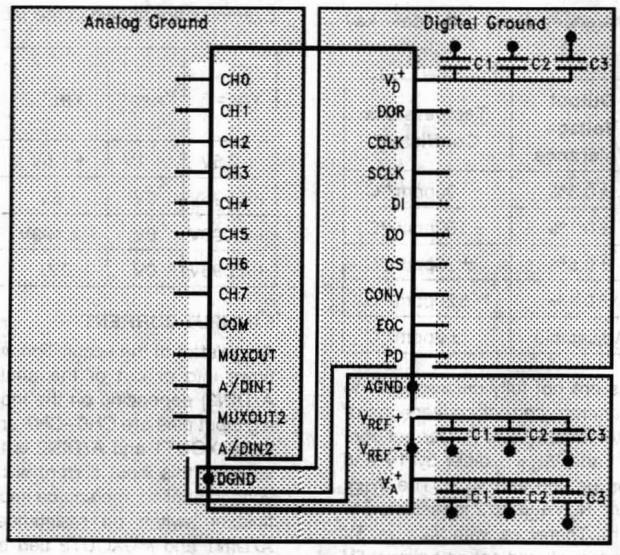

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FIGURE 16. Ideal Ground Plane

Application Hints (Continued)

11.0 CLOCK SIGNAL LINE ISOLATION

The ADC12030/2/4/8's performance is optimized by routing the analog input/output and reference signal conductors as far as possible from the conductors that carry the clock signals to the CCLK and SCLK pins. Ground traces parallel to the clock signal traces can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

12.0 THE CALIBRATION CYCLE

A calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize after initial turn-on. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ± 0.4 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if the Power Supply Voltage and the ambient temperature do not change significantly (see the curves in the Typical Performance Characteristics).

13.0 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature or the power supply voltage change significantly. (See the curves titled "Zero Error Change vs Ambient Temperature" and "Zero Error Change vs Supply Voltage" in the Typical Performance Characteristics.)

14.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in the table of Electrical Characteristics, and spectral plots of S/(N + D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.8)\ dB$$

where n is the A/D's resolution in bits.

The effective bits of a real A/D converter, therefore, can be found by:

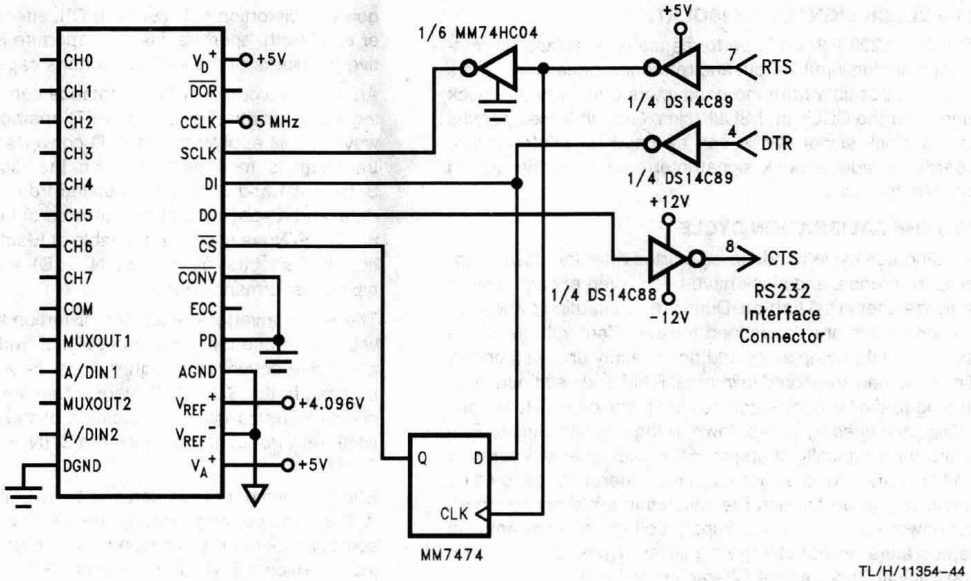
$$n(\text{effective}) = \frac{S/N(dB) - 1.8}{6.02}$$

As an example, this device with a differential signed 5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

15.0 AN RS232 SERIAL INTERFACE

Shown on the following page is a schematic for an RS232 interface to any IBM and compatible PCs. The DTR, RTS, and CTS RS232 signal lines are buffered via level translators and connected to the ADC12038's DI, SCLK, and DO pins, respectively. The D flip flop drives the $\overline{CS}$ control line.

Application Hints (Continued)



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Note: V_A^+, V_D^+, and V_{REF}^+ on the ADC12038 each have 0.01 μF and 0.1 μF chip caps, and 10 μF tantalum caps. All logic devices are bypassed with 0.1 μF caps.

The assignment of the RS232 port is shown below

			B7	B6	B5	B4	B3	B2	B1	B0
COM1	Input Address	3FE	X	X	X	CTS	X	X	X	X
	Output Address	3FC	X	X	X	0	X	X	RTS	DTR

A sample program, written in Microsoft QuickBasic, is shown on the next page. The program prompts for data mode select instruction to be sent to the A/D. This can be found from the Mode Programming table shown earlier. The data should be entered in "1"s and "0"s as shown in the table with DI0 first. Next the program prompts for the number of SCLKs required for the programmed mode select instruction. For instance, to send all "0"s to the A/D, selects CH0 as the + input, CH1 as the − input, 12-bit conversion, and 13-bit MSB first data output format (if the sign bit was not turned off by a previous instruction). This would require 13 SCLK periods since the output data format is 13 bits. The part powers up with No Auto Cal, No Auto Zero, 10 CCLK Acquisition Time, 12-bit conversion, data out with sign, power up, 12- or 13-bit MSB first, and user mode. Auto Cal, Auto Zero, Power Up and Power Down instructions do not change these default settings. The following power up sequence should be followed:

1. Run the program
2. Prior to responding to the prompt apply the power to the ADC12038
3. Respond to the program prompts

It is recommended that the first instruction issued to the ADC12038 be Auto Cal (see Section 1.1).

Application Hints (Continued)

```
'variables DOL=Data Out word length, DI=Data string for A/D DI input,
'          DO=A/D result string
'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC))          'set RTS HIGH
OUT &H3FC, (&HFE AND INP(&H3FC))         'set DTR LOW
OUT &H3FC, (&HFD AND INP(&H3FC))         'set RTS LOW
OUT &H3FC, (&HEF AND INP(&H3FC))         'set B4 low
10
LINE INPUT "DI data for ADC12038 (see Mode Table on data sheet)"; DI$
INPUT "ADC12038 output word length (8,9,12,13,16 or 17)"; DOL
20
'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC))          'set RTS HIGH
OUT &H3FC, (&HFE AND INP(&H3FC))         'set DTR LOW
OUT &H3FC, (&HFD AND INP(&H3FC))         'set RTS LOW
'SET CS# LOW
OUT &H3FC, (&H2 OR INP (&H3FC))          'set RTS HIGH
OUT &H3FC, (&H1 OR INP(&H3FC))           'set DTR HIGH
OUT &H3FC, (&HFD AND INP(&H3FC))         'set RTS LOW
DO$=" "                                  'reset DO variable
  OUT &H3FC, (&H1 OR INP(&H3FC))         'SET DTR HIGH
  OUT &H3FC, (&HFD AND INP(&H3FC))       'SCLK low
FOR N=1 TO 8
  Temp$=MID$(DI$,N,1)
  IF Temp$="0"THEN
    OUT &H3FC,(&H1 OR INP(&H3FC))
  ELSE OUT &H3FC, (&HFE AND INP(&H3FC))
  END IF                                 'out DI
  OUT &H3FC,(&H2 OR INP(&H3FC))          'SCLK high
  IF (INP(&H3FE) AND 16)=16 THEN
    DO$=DO$+"0"
    ELSE
    DO$=DO$+"1"
  END IF                                 'input DO
  OUT &H3FC, (&H1 OR INP(&H3FC))         'SET DTR HIGH
  OUT &H3FC, (&HFD AND INP(&H3FC))       'SCLK low
NEXT N
IF DOL>8 THEN
  FOR N=9 TO DOL
  OUT &H3FC,(&H1 OR INP(&H3FC))          'SET DTR HIGH
  OUT &H3FC,(&HFD AND INP(&H3FC))        'SCLK low
  OUT &H3FC,(&H2 OR INP(&H3FC))          'SCLK high
  IF (INP(&H3FE) AND &H10)=&H10 THEN
    DO$=DO$+"0"
  ELSE
    DO$=DO$+"1"
  END IF
  NEXT N
END IF
OUT &H3FC,(&HFA AND INP(&H3FC))          'SCLK low and DI high
FOR N=1 TO 500
NEXT N
PRINT DO$
INPUT "Enter "C" to convert else "RETURN" to alter DI data"; s$
IF s$="C" OR s$="c" THEN
  GOTO 20
ELSE
  GOTO 10
END IF
END
```

National Semiconductor

ADC12L030/ADC12L032/ADC12L034/ADC12L038 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12L030 family is 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexers. These devices are fully tested with a single 3.3V power supply. The ADC12L032, ADC12L034 and ADC12L038 have 2, 4 and 8 channel multiplexers, respectively. Differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12L030 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to less than $\pm\frac{1}{2}$ LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +3.3V) can be accommodated with a single +3.3V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign two's compliment output data format.

The serial I/O is configured to comply with NSC's MICROWIRE™ and Motorola's SPI standards. For complementary voltage references see the LM4040, LM4041 or LM9140 data sheets.

Features

- 0V to 3.3V analog input range with single 3.3V power supply
- Serial I/O (MICROWIRE and SPI Compatible)
- 2, 4, or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Variable resolution and conversion rate
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- Fully tested and guaranteed with a 2.5V reference
- No Missing Codes over temperature

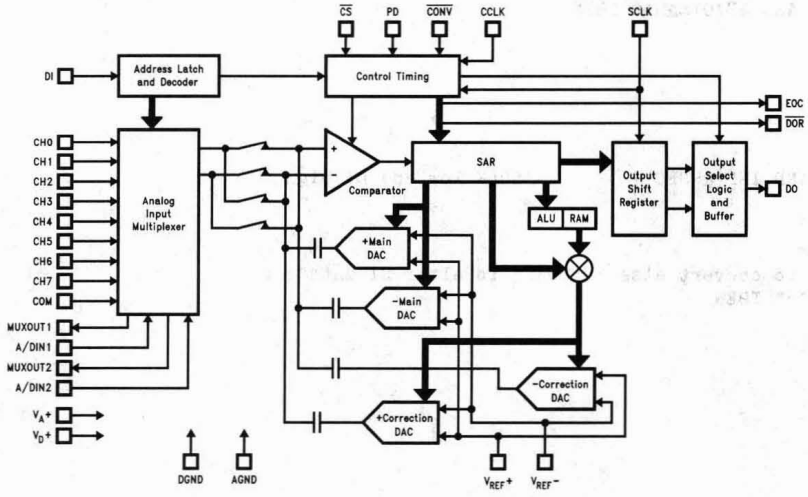
Key Specifications

■ Resolution	12-bit plus sign
■ 12-bit plus sign conversion time	8.8 μs (min)
■ 12-bit plus sign sampling rate	73 kHz (max)
■ Integral linearity error	±1 LSB (max)
■ Single supply	3.3V ±10%
■ Power dissipation	15 mW (max)
— Power down	40 μW (typ)

Applications

- Portable Medical instruments
- Portable computing
- Portable Test equipment

ADC12L038 Simplified Block Diagram



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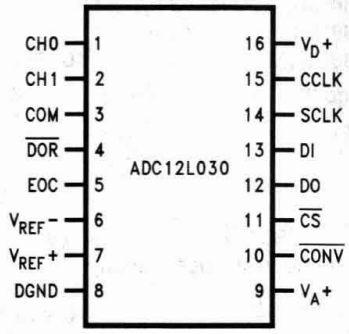
Connection Diagrams

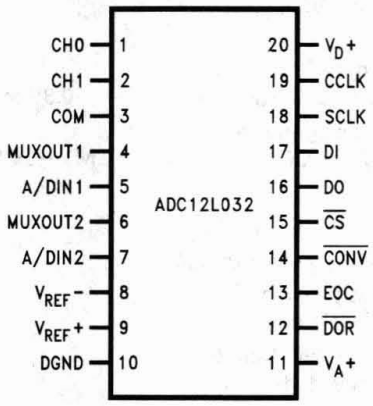
16-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11830–2

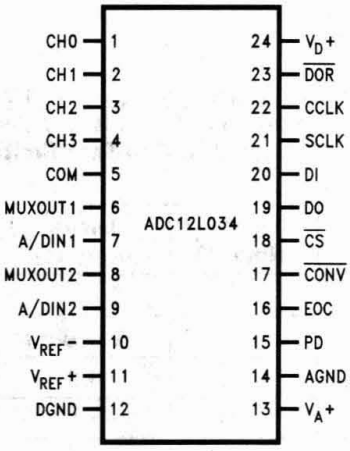
20-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11830–3

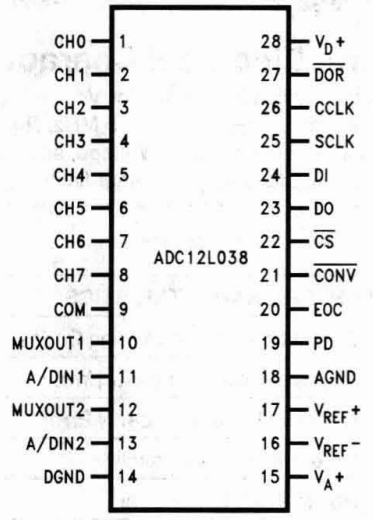
24-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11830–4

28-Pin Dual-In-Line and Wide Body SO Packages



Top View

TL/H/11830–5

Ordering Information

Industrial Temperature Range $-40°C \leq T_A \leq +85°C$	NS Package Number
ADC12L030CIN	N16E
ADC12L030CIWM	M16B
ADC12L032CIN	N20A
ADC12L032CIWM	M20B
ADC12L034CIN	N24C
ADC12L034CIWM	M24B
ADC12L038CIN	N28B
ADC12L038CIWM	M28B

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage ($V^+ = V_A^+ = V_D^+$)	6.5V
Voltage at Inputs and Outputs except CH0–CH7 and COM	−0.3V to V^+ +0.3V
Voltage at Analog Inputs CH0–CH7 and COM	GND −5V to V^+ +5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
Input Current at Any Pin (Note 3)	±30 mA
Package Input Current (Note 3)	±120 mA
Package Dissipation at T_A = 25°C (Note 4)	500 mW
ESD Susceptability (Note 5) Human Body Model	1500V
Soldering Information N Packages (10 seconds)	260°C
SO Package (Note 6): Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12L030CIN, ADC12L030CIWM, ADC12L032CIN, ADC12L032CIWM, ADC12L034CIN, ADC12L034CIWM, ADC12L038CIN, ADC12L038CIWM	−40°C ≤ T_A ≤ +85°C
Supply Voltage ($V^+ = V_A^+ = V_D^+$)	+3.0V to +5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤ 100 mV
V_{REF}^+	0V to V_A^+
V_{REF}^-	0V to V_{REF}^+
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	1V to V_A^+
V_{REF} Common Mode Voltage Range $\frac{(V_{REF}^+ + V_{REF}^-)}{2}$	0.1 V_A^+ to 0.6 V_A^+
A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 Voltage Range	0V to V_A^+
A/D IN Common Mode Voltage Range $\frac{(V_{IN}^+ + V_{IN}^-)}{2}$	0V to V_A^+

Converter Electrical Characteristics

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +3.3\ V_{DC}$, $V_{REF}^+ = +2.500\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \le 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and 10(t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12 + sign**	Bits (min)
+ILE	Positive Integral Linearity Error	After Auto-Cal (Notes 12, 18)	±1/2	**±1**	LSB (max)
−ILE	Negative Integral Linearity Error	After Auto-Cal (Notes 12, 18)	±1/2	**±1**	LSB (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 18)	±1/2	**±2**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 18)	±1/2	**±2**	LSB (max)
	Offset Error	After Auto-Cal (Notes 5, 18) $V_{IN}(+) = V_{IN}(-) = 1.250V$	±1/2	**±2**	LSB (max)
	DC Common Mode Error	After Auto-Cal (Note 15)	±2	**±3.5**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Notes 12, 13 and 14)	±1		LSB
	Resolution with No Missing Codes	8-bit + sign mode		**8 + sign**	Bits (min)
+INL	Positive Integral Linearity Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)
−INL	Negative Integral Linearity Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)
DNL	Differential Non-Linearity	8-bit + sign mode		**±3/4**	LSB (max)
	Positive Full-Scale Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)

Converter Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +3.3\ V_{DC}$, $V_{REF}^+ = +2.500\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and 10(t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS (Continued)					
	Negative Full-Scale Error	8-bit + sign mode (Note 12)		**±1/2**	LSB (max)
	Offset Error	8-bit + sign mode, after Auto-Zero (Note 13) $V_{IN}(+) = V_{IN}(-) = +1.250V$		**±1/2**	LSB (max)
TUE	Total Unadjusted Error	8-bit + sign mode after Auto-Zero (Notes 12, 13 and 14)		**±3/4**	LSB (max)
	Multiplexer Channel to Channel Matching		±0.05		LSB
	Power Supply Sensitivity	$V^+ = +3.3V \pm 10\%$			
	Offset Error		±0.5	**±1**	LSB (max)
	+ Full-Scale Error		±0.5	**±1.5**	LSB (max)
	− Full-Scale Error		±0.5	**±1.5**	LSB (max)
	+ Integral Linearity Error		±0.5		LSB
	− Integral Linearity Error		±0.5		LSB
	Output Data from "12-Bit Conversion of Offset" (see Table V)	(Note 20)		**+10** **−10**	LSB (max) LSB (min)
	Output Data from "12-Bit Conversion of Full-Scale" (see Table V)	(Note 20)		**4095** **4093**	LSB (max) LSB (min)
UNIPOLAR DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = 2.5\ V_{PP}$	69.4		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 2.5\ V_{PP}$	68.3		dB
		$f_{IN} = 40$ kHz, $V_{IN} = 2.5\ V_{PP}$	65.7		dB
	−3 dB Full Power Bandwidth	$V_{IN} = 2.5\ V_{PP}$, where S/(N+D) drops 3 dB	31		kHz
DIFFERENTIAL DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = \pm 2.5V$	77.0		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 2.5V$	73.9		dB
		$f_{IN} = 40$ kHz, $V_{IN} = \pm 2.5V$	67.0		dB
	−3 dB Full Power Bandwidth	$V_{IN} = \pm 2.5V$, where S/(N+D) drops 3 dB	40		kHz

Electrical Characteristics

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +3.3\ V_{DC}$, $V_{REF}^+ = +2.500\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{REF}	Reference Input Capacitance		85		pF
$C_{A/D}$	A/DIN1 and A/DIN2 Analog Input Capacitance		75		pF
	A/DIN1 and A/DIN2 Analog Input Leakage Current	$V_{IN} = +3.3V$ or $V_{IN} = 0V$	±0.1	**±1.0**	µA (max)
	CH0–CH7 and COM Input Voltage			**GND − 0.05** **$V_A^+ + 0.05$**	V (min) V (max)
C_{CH}	CH0–CH7 and COM Input Capacitance		10		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF
	Off Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 3.3V and Off Channel = 0V	−0.01	**−0.3**	µA (min)
		On Channel = 0V and Off Channel = 3.3V	0.01	**0.3**	µA (max)
	On Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 3.3V and Off Channel = 0V	0.01	**0.3**	µA (max)
		On Channel = 0V and Off Channel = 3.3V	−0.01	**−0.3**	µA (min)
	MUXOUT1 and MUXOUT2 Leakage Current	$V_{MUXOUT} = 3.3V$ or $V_{MUXOUT} = 0V$	0.01	**0.3**	µA (max)
R_{ON}	MUX On Resistance	$V_{IN} = 1.65V$ and $V_{MUXOUT} = 1.55V$	1300	**1900**	Ω (max)
	R_{ON} Matching Channel to Channel	$V_{IN} = 1.65V$ and $V_{MUXOUT} = 1.55V$	5		%
	Channel to Channel Crosstalk	$V_{IN} = 3.3\ V_{PP}$, $f_{IN} = 40$ kHz	−72		dB
	MUX Bandwidth		90		kHz

DC and Logic Electrical Characteristics

The following specifications apply for $V^+ = V_A{}^+ = V_D{}^+ = +3.3\ V_{DC}$, $V_{REF}{}^+ = +2.500\ V_{DC}$, $V_{REF}{}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}{}^+$ and $V_{REF}{}^- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
CCLK, $\overline{CS}$, $\overline{CONV}$, DI, PD AND SCLK INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 3.0V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 3.3V$	0.005	**1.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	μA (min)
DO, EOC AND $\overline{DOR}$ DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 3.0V$, $I_{OUT} = -360\ \mu A$ $V^+ = 3.0V$, $I_{OUT} = -10\ \mu A$		**2.4** **2.9**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 3.0V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = 0V$ $V_{OUT} = 3.3V$	−0.1 0.1	**−3.0** **3.0**	μA (max) μA (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	14	**6.5**	mA (min)
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_D{}^+$	16	**8.0**	mA (min)
POWER SUPPLY CHARACTERISTICS					
$I_D{}^+$	Digital Supply Current	Awake $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	1.1 600 12	**1.5**	mA (max) μA μA
$I_A{}^+$	Positive Analog Supply Current	Awake $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	2.2 10 0.1	**3.0**	mA (max) μA μA
I_{REF}	Reference Input Current	Awake $\overline{CS}$ = HIGH, Powered Down	70 0.1		μA μA

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AC Electrical Characteristics

The following specifications apply for $V^+ = V_A{}^+ = V_D{}^+ = +3.3\ V_{DC}$, $V_{REF}{}^+ = +2.500\ V_{DC}$, $V_{REF}{}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}{}^+$ and $V_{REF}{}^- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
f_{CK}	Conversion Clock (CCLK) Frequency		10 1	**5**	MHz (max) MHz (min)
f_{SK}	Serial Data Clock SCLK Frequency		10 0	**5**	MHz (max) Hz (min)
	Conversion Clock Duty Cycle			**40** **60**	% (min) % (max)
	Serial Data Clock Duty Cycle			**40** **60**	% (min) % (max)
t_C	Conversion Time	12-Bit + Sign or 12-Bit	44(t_{CK})	**44(t_{CK})**	(max)
				8.8	μs (max)
		8-Bit + Sign or 8-Bit	21(t_{CK})	**21(t_{CK})**	(max)
				4.2	μs (max)
t_A	Acquisition Time (Note 19)	6 Cycles Programmed	6(t_{CK})	**6(t_{CK})** **7(t_{CK})**	(min) (max)
				1.2 **1.4**	μs (min) μs (max)
		10 Cycles Programmed	10(t_{CK})	**10(t_{CK})** **11(t_{CK})**	(min) (max)
				2.0 **2.2**	μs (min) μs (max)
		18 Cycles Programmed	18(t_{CK})	**18(t_{CK})** **19(t_{CK})**	(min) (max)
				3.6 **3.8**	μs (min) μs (max)
		34 Cycles Programmed	34(t_{CK})	**34(t_{CK})** **35(t_{CK})**	(min) (max)
				6.8 **7.0**	μs (min) μs (max)
t_{CAL}	Self-Calibration Time		4944(t_{CK})	**4944(t_{CK})**	(max)
				988.8	μs (max)
t_{AZ}	Auto-Zero Time		76(t_{CK})	**76(t_{CK})**	(max)
				15.2	μs (max)
t_{SYNC}	Self-Calibration or Auto-Zero Synchronization Time from DOR		2(t_{CK})	**2(t_{CK})** **3(t_{CK})**	(min) (max)
				0.40 **0.60**	μs (min) μs (max)
$t_{\overline{DOR}}$	DOR High Time when $\overline{CS}$ is Low Continuously for Read Data and Software Power Up/Down		9(t_{SK})	**9(t_{SK})**	(max)
				1.8	μs (max)
$t_{\overline{CONV}}$	$\overline{CONV}$ Valid Data Time		8(t_{SK})	**8(t_{SK})**	(max)
				1.6	μs (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_A^+ = V_D^+ = +3.3\ V_{DC}$, $V_{REF}^+ = +2.500\ V_{DC}$, $V_{REF}^- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for V_{REF}^+ and $V_{REF}^- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
t_{HPU}	Hardware Power-Up Time, Time from PD Falling Edge to EOC Rising Edge		250	**700**	μs (max)
t_{SPU}	Software Power-Up Time, Time from Serial Data Clock Falling Edge to EOC Rising Edge		500	**700**	μs (max)
t_{ACC}	Access Time Delay from $\overline{CS}$ Falling Edge to DO Data Valid		25	**60**	ns (max)
t_{SET-UP}	Set-Up Time of $\overline{CS}$ Falling Edge to Serial Data Clock Rising Edge			**50**	ns (min)
t_{DELAY}	Delay from SCLK Falling Edge to $\overline{CS}$ Falling Edge		0	**5**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{CS}$ Rising Edge to DO TRI-STATE®	$R_L = 3k$, $C_L = 100$ pF	70	**100**	ns (max)
t_{HDI}	DI Hold Time from Serial Data Clock Rising Edge		5	**15**	ns (min)
t_{SDI}	DI Set-Up Time from Serial Data Clock Rising Edge		5	**10**	ns (min)
t_{HDO}	DO Hold Time from Serial Data Clock Falling Edge	$R_L = 3k$, $C_L = 100$ pF	35	**65** **5**	ns (max) ns (min)
t_{DDO}	Delay from Serial Data Clock Falling Edge to DO Data Valid		50	**90**	ns (max)
t_{RDO}	DO Rise Time, TRI-STATE to High DO Rise Time, Low to High	$R_L = 3k$, $C_L = 100$ pF	10 10	**40** **40**	ns (max) ns (max)
t_{FDO}	DO Fall Time, TRI-STATE to Low DO Fall Time, High to Low	$R_L = 3k$, $C_L = 100$ pF	15 15	**40** **40**	ns (max) ns (max)
t_{CD}	Delay from $\overline{CS}$ Falling Edge to $\overline{DOR}$ Falling Edge		50	**80**	ns (max)
t_{SD}	Delay from Serial Data Clock Falling Edge to $\overline{DOR}$ Rising Edge		45	**80**	ns (max)
C_{IN}	Capacitance of Logic Inputs		10		pF
C_{OUT}	Capacitance of Logic Outputs		20		pF

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > V_A^+$ or V_D^+), the current at that pin should be limited to 20 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 20 mA to four.

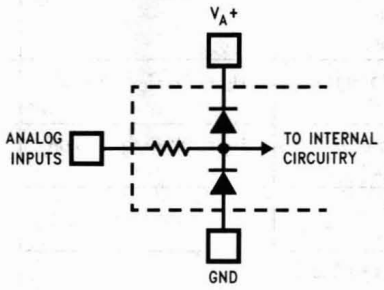
Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J max$, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J max - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_J max = 150°C$. The typical thermal resistance (Θ_{JA}) of these parts when board mounted follow:

Part Number	Thermal Resistance θ_{JA}
ADC12L030CIN	53°C/W
ADC12L030CIWM	70°C/W
ADC12L032CIN	46°C/W
ADC12L032CIWM	64°C/W
ADC12L034CIN	42°C/W
ADC12L034CIWM	57°C/W
ADC12L038CIN	40°C/W
ADC12L038CIWM	50°C/W

Note 5: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage this device. However, errors in the A/D conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A^+ or below GND by more than 50 mV. As an example, if V_A^+ is 3.0 V_{DC}, full-scale input voltage must be ≤ 3.05 V_{DC} to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that the V_A^+ and V_D^+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.

Note 9: With the test condition for V_{REF} ($V_{REF}^+ - V_{REF}^-$) given as +2.500V the 12-bit LSB is 610 μV and the 8-bit LSB is 9.8 mV.

Note 10: Typicals are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero (see *Figures 1b* and *1c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between 1 to 0 and 0 to +1 (see *Figure 2*).

Note 14: Total unadjusted error includes offset, full-scale, linearity and multiplexer errors.

Note 15: The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.

Note 16: Channel leakage current is measured after the channel selection.

Note 17: Timing specifications are tested at the TTL logic levels, $V_{IL} = 0.4V$ for a falling edge and $V_{IH} = 2.4V$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 18: The ADC12L030 family's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a maximum repeatability uncertainty of 0.2 LSB.

Note 19: If SCLK and CCLK are driven from the same clock source, then t_A is 6, 10, 18 or 34 clock periods minimum and maximum.

Note 20: The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

Electrical Characteristics (Continued)

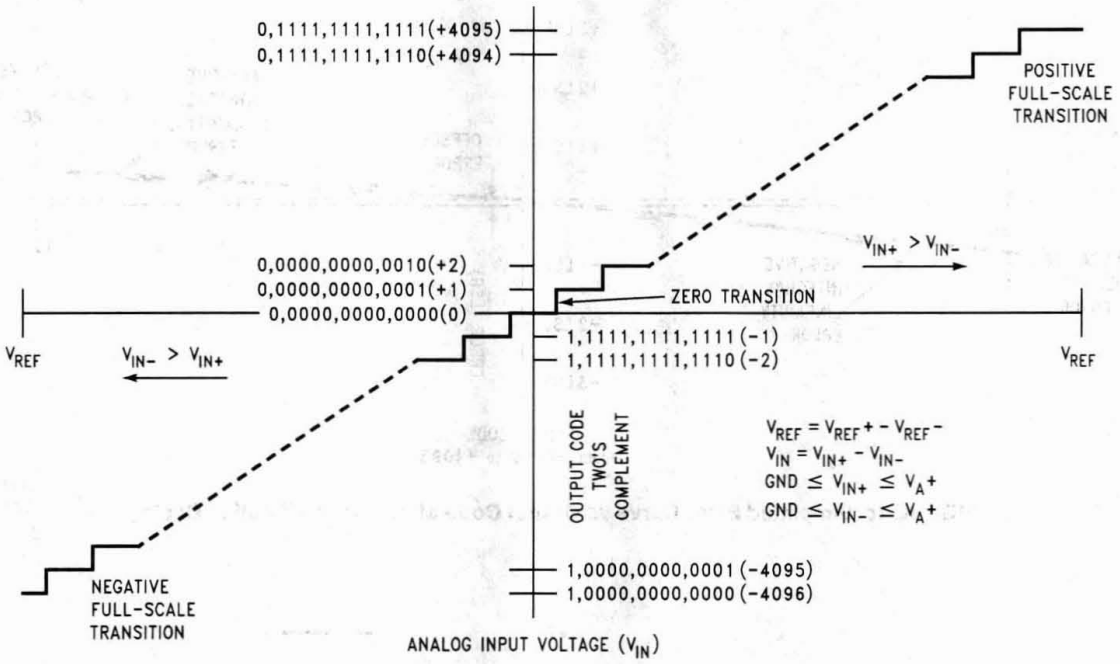

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FIGURE 1a. Transfer Characteristic

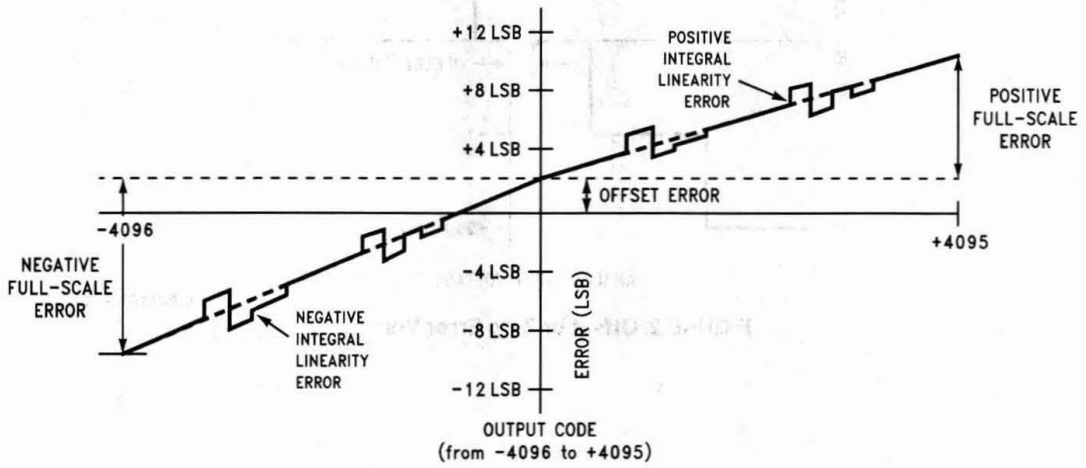

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

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Electrical Characteristics (Continued)

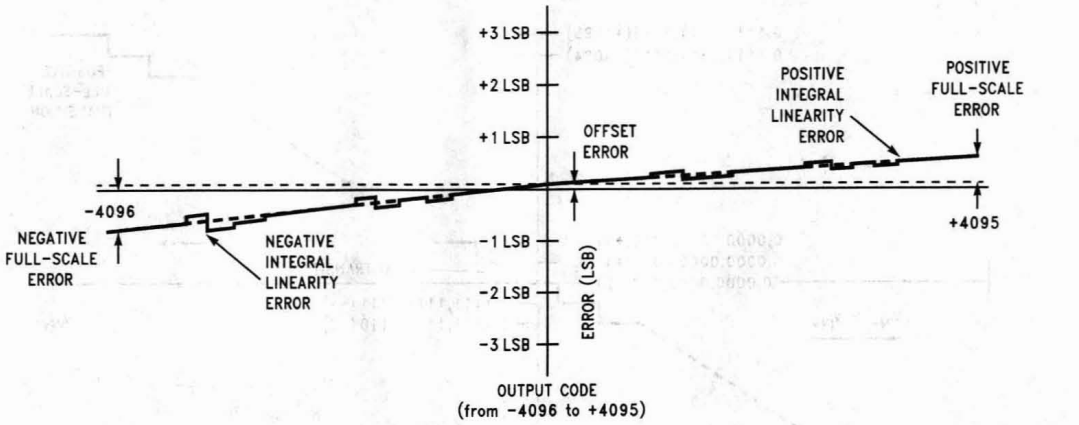

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FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

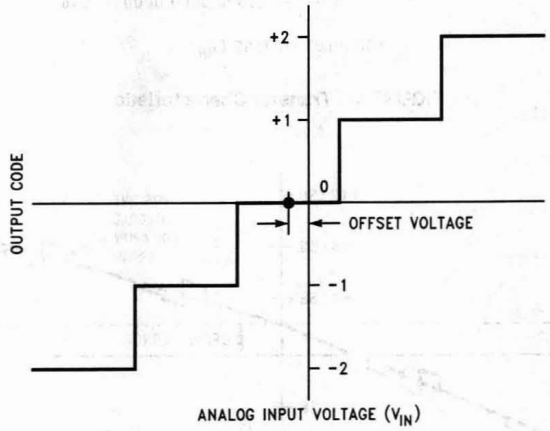

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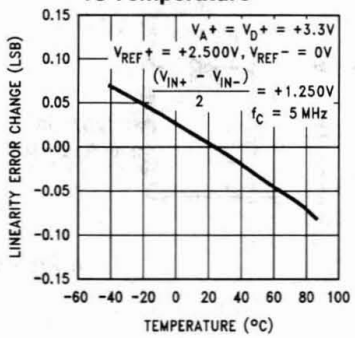
FIGURE 2. Offset or Zero Error Voltage

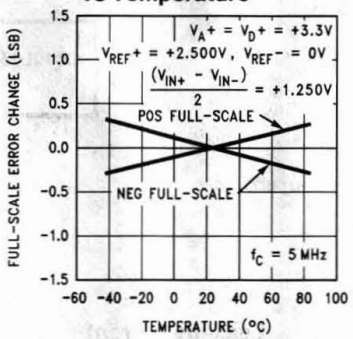
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown. (Note 9)

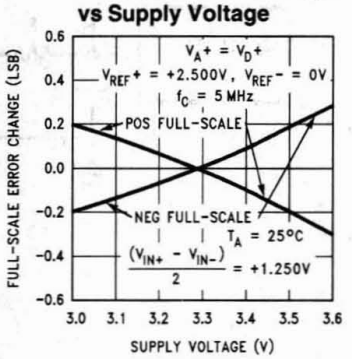
Linearity Error Change vs Temperature



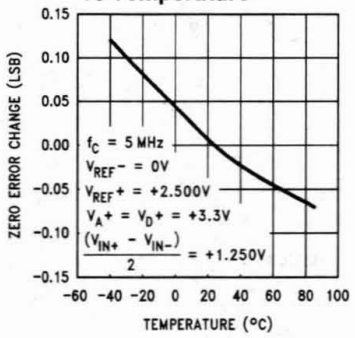
Full-Scale Error Change vs Temperature



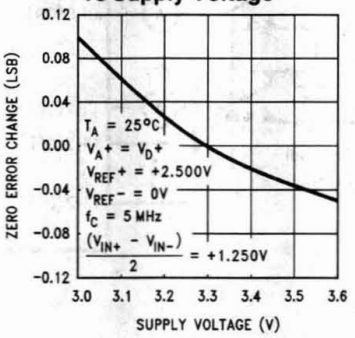
Full-Scale Error Change vs Supply Voltage



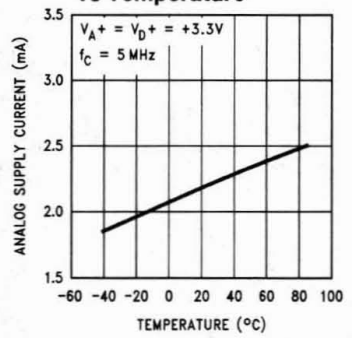
Zero Error Change vs Temperature



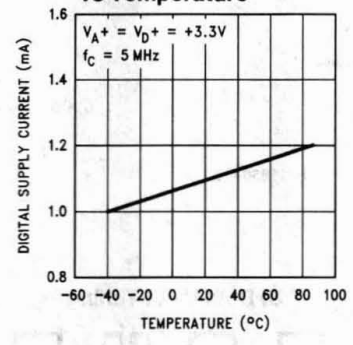
Zero Error Change vs Supply Voltage



Analog Supply Current vs Temperature



Digital Supply Current vs Temperature



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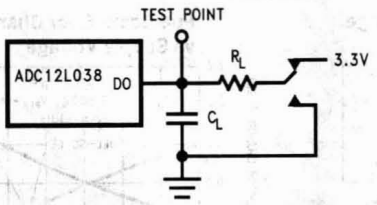
Test Circuits

DO "TRI-STATE" (t_{1H}, t_{0H})



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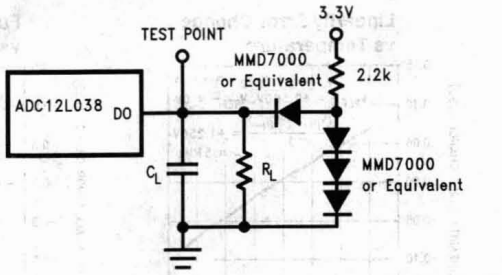
DO except "TRI-STATE"



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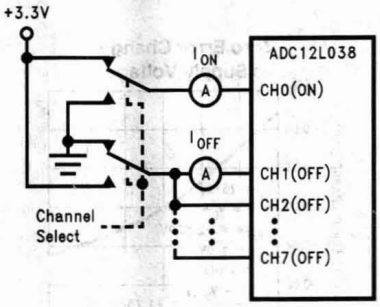
Leakage Current



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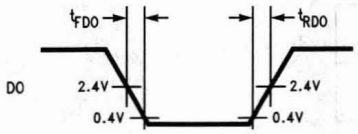
Timing Diagrams

DO Falling and Rising Edge



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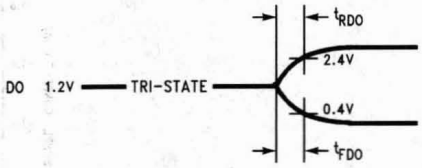
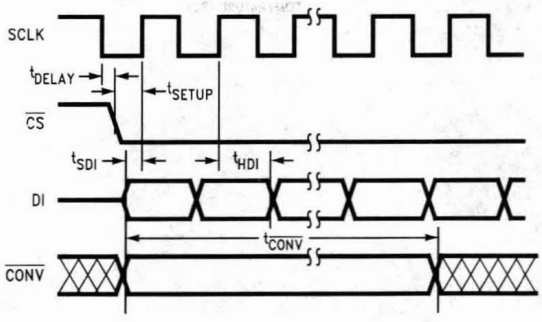
DO "TRI-STATE" Falling and Rising Edge



TL/H/11830–19

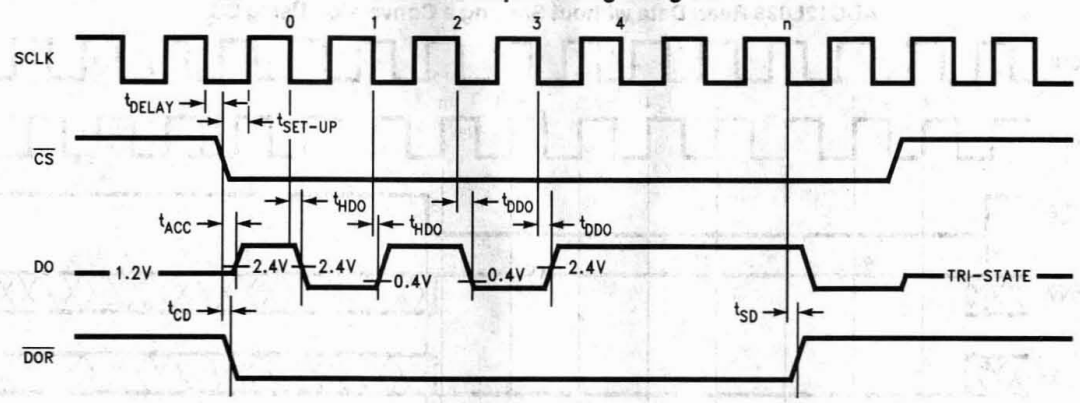
DI Data Input Timing



TL/H/11830–20

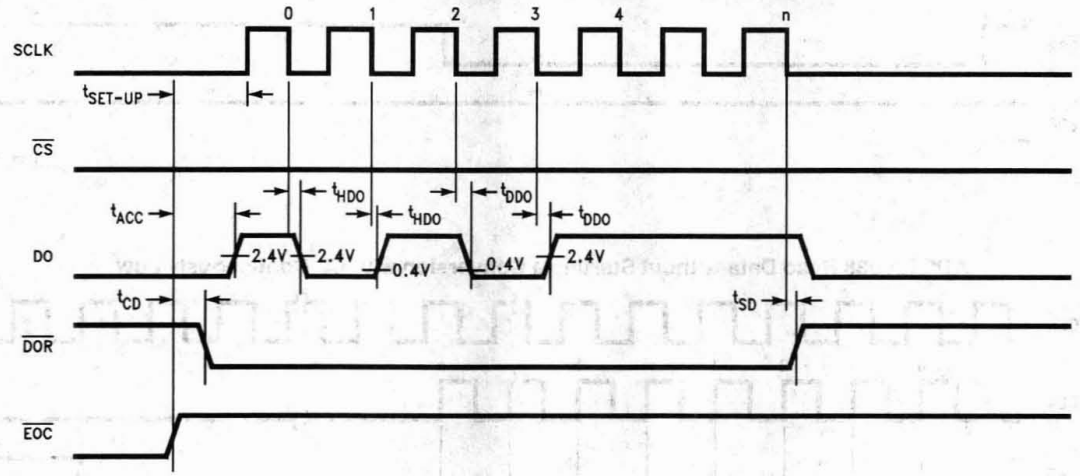
Timing Diagrams (Continued)

DO Data Output Timing Using $\overline{CS}$



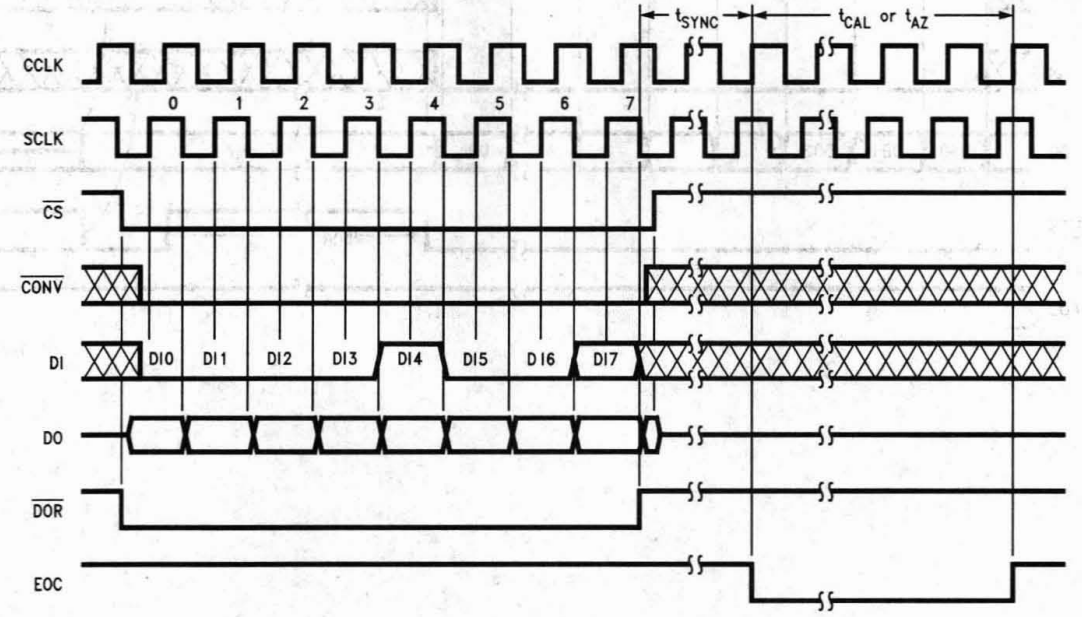
TL/H/11830–21

DO Data Output Timing with $\overline{CS}$ Continuously Low



TL/H/11830–22

ADC12L038 Auto Cal or Auto Zero

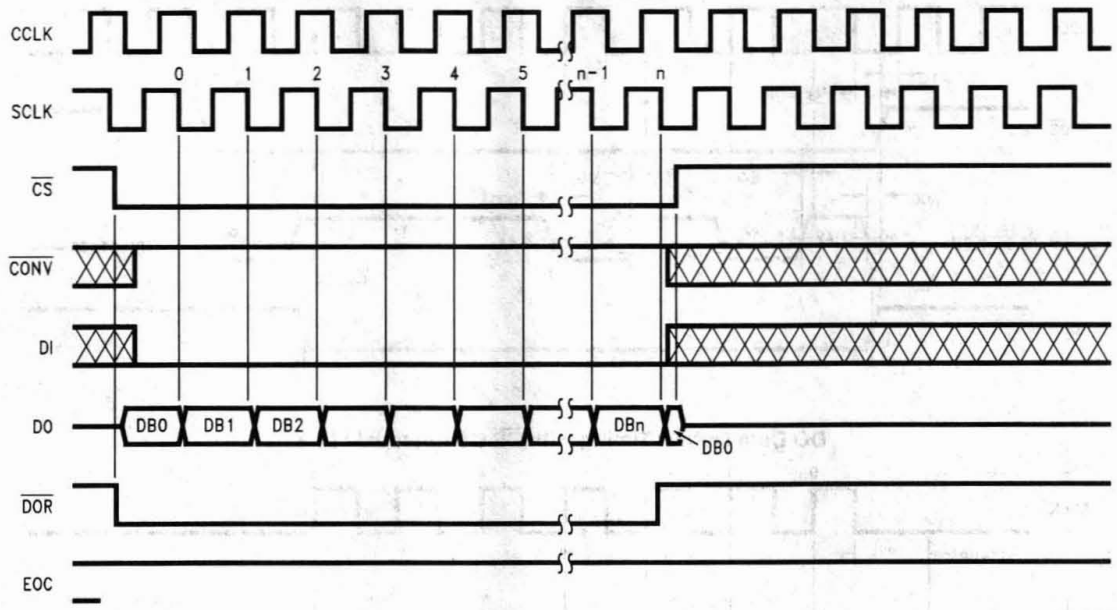


TL/H/11830–23

Note: DO output data is not valid during this cycle.

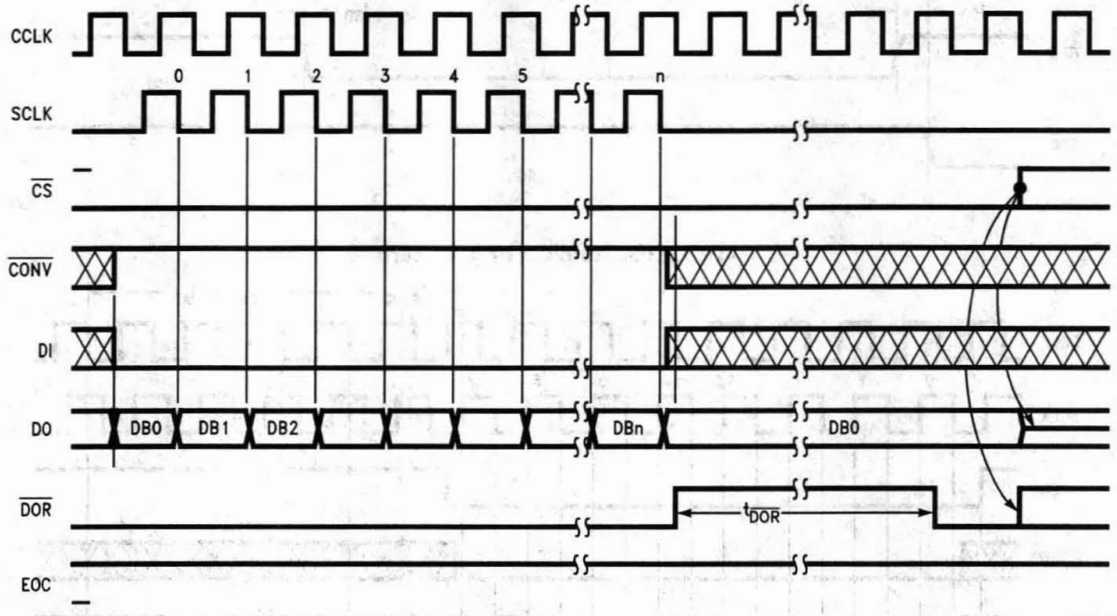
Timing Diagrams (Continued)

ADC12L038 Read Data without Starting a Conversion Using $\overline{CS}$



TL/H/11830–24

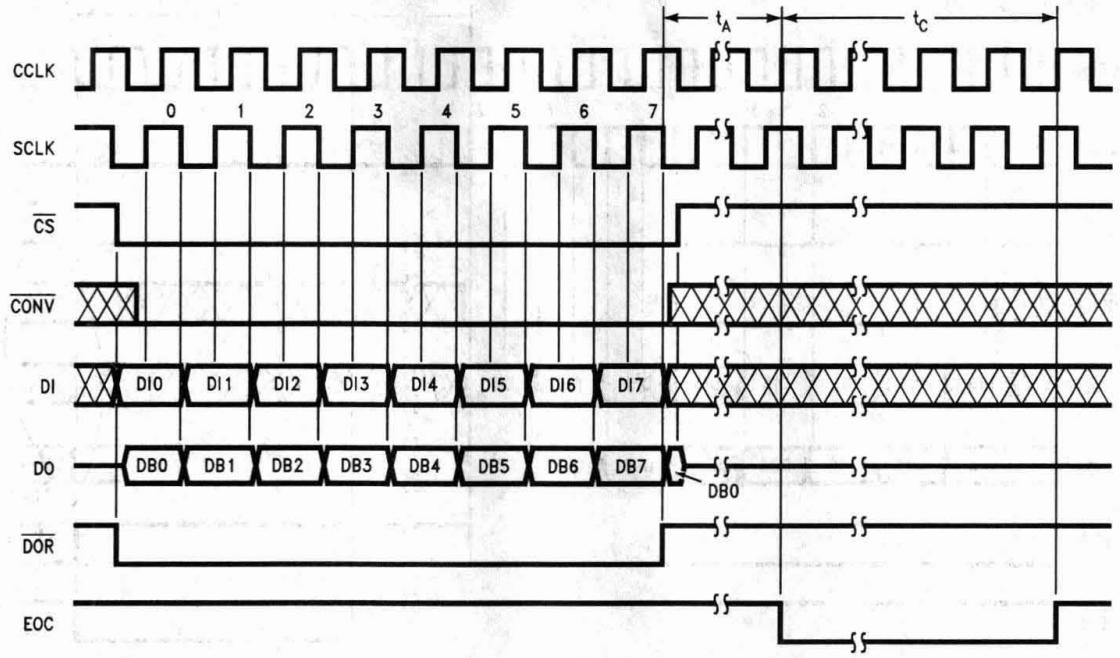
ADC12L038 Read Data without Starting a Conversion with $\overline{CS}$ Continuously Low



TL/H/11830–25

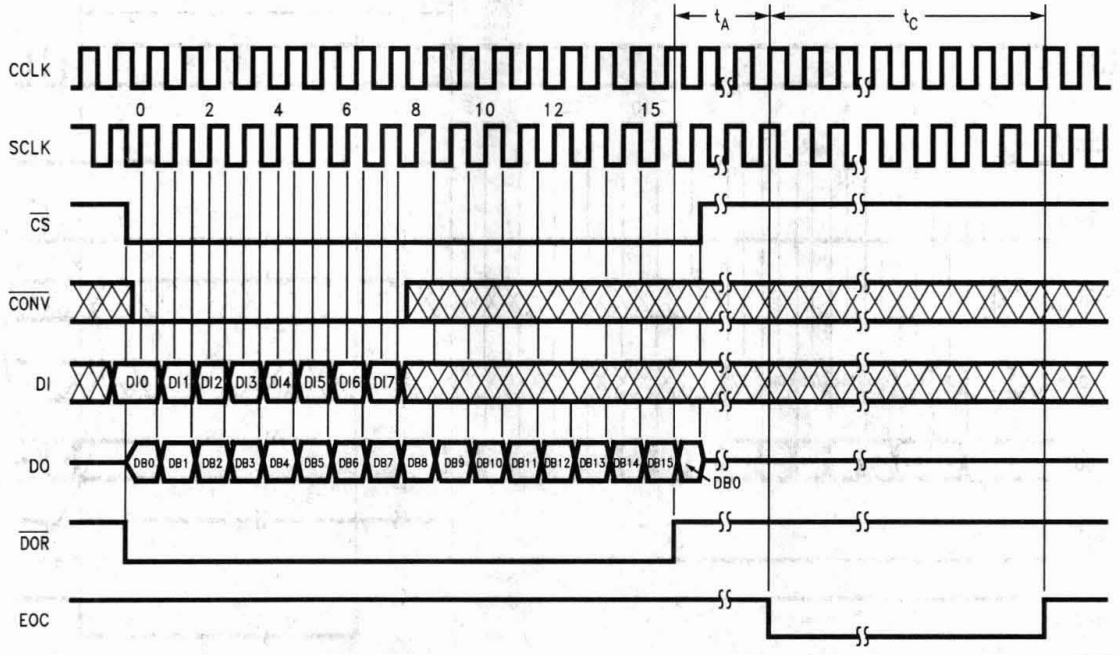
Timing Diagrams (Continued)

ADC12L038 Conversion Using $\overline{CS}$ with 8-Bit Digital Output Format



TL/H/11830–26

ADC12L038 Conversion Using $\overline{CS}$ with 16-Bit Digital Output Format



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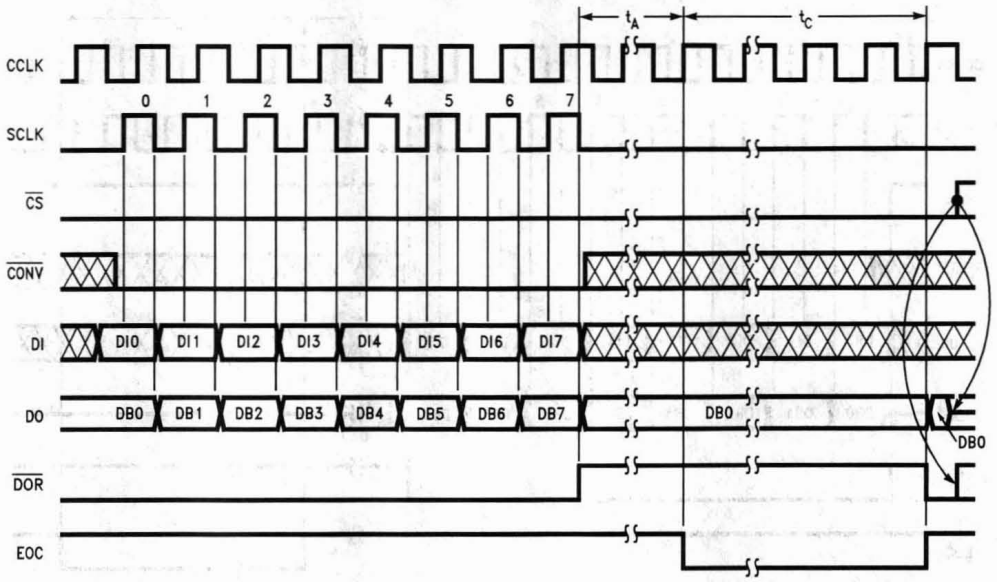
2

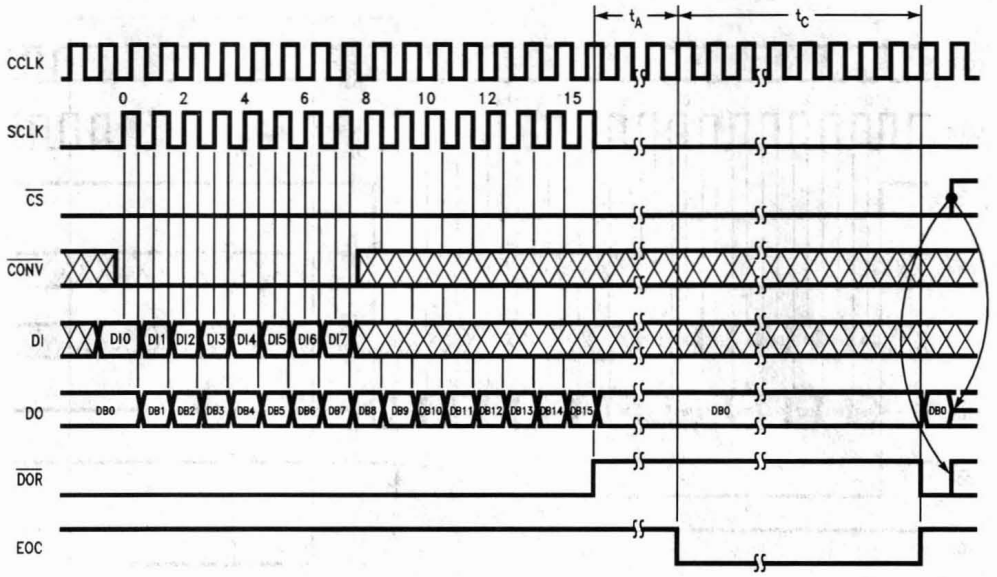
Timing Diagrams (Continued)

ADC12L038 Conversion with $\overline{CS}$ Continuously Low and 8-Bit Digital Output Format



TL/H/11830–28

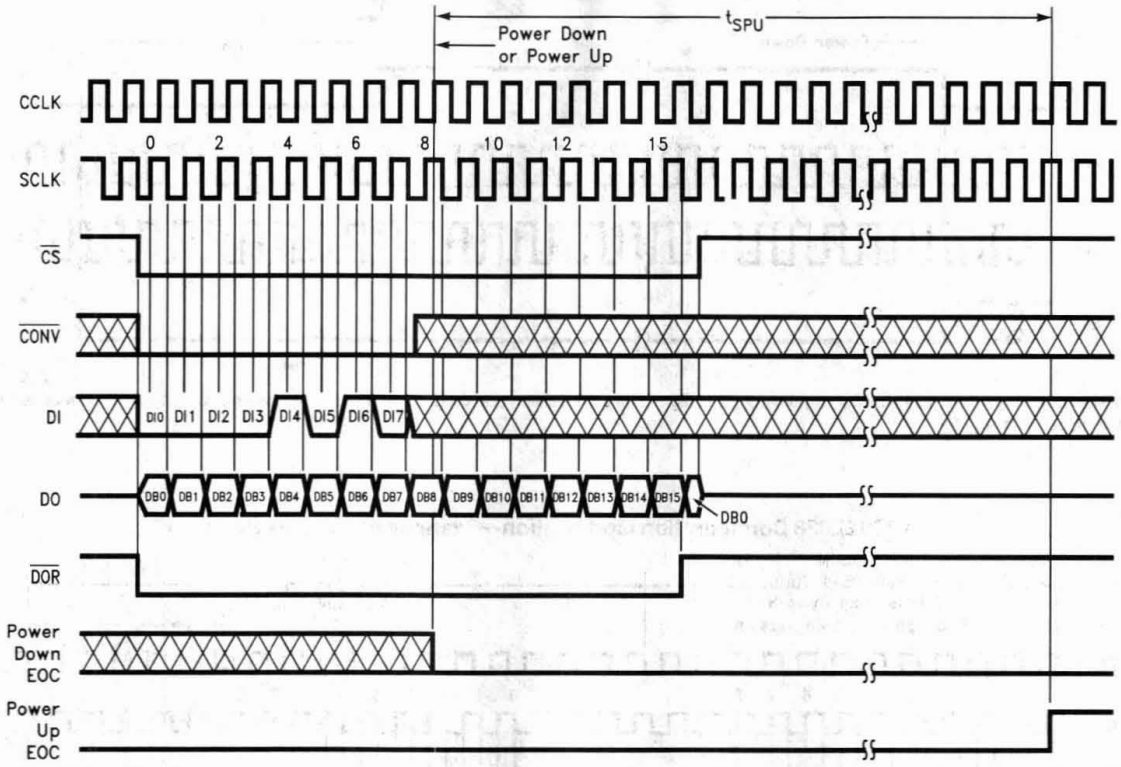
ADC12L038 Conversion with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



TL/H/11830–29

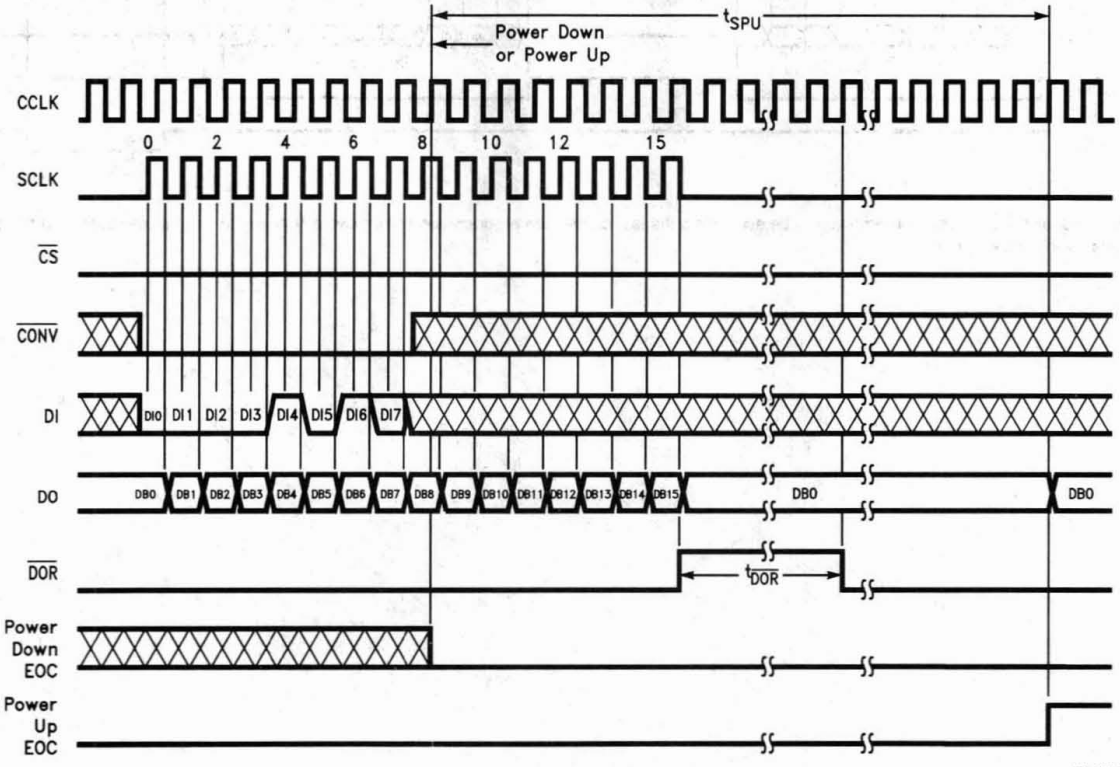
Timing Diagrams (Continued)

ADC12L038 Software Power Up/Down Using $\overline{CS}$ with 16-Bit Digital Output Format



TL/H/11830–30

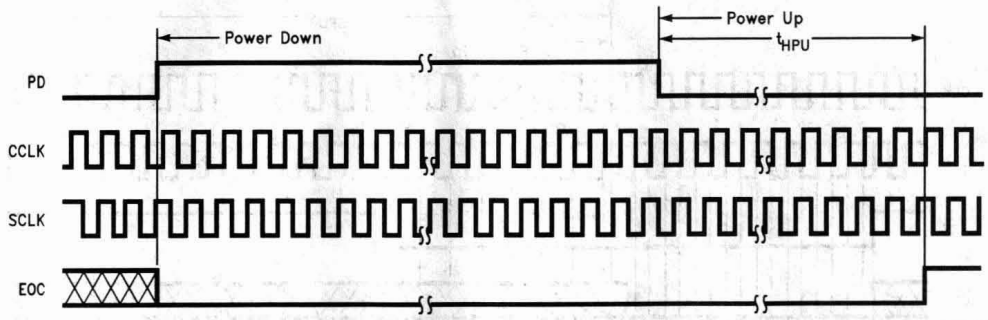
ADC12L038 Software Power Up/Down with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



TL/H/11830–31

Timing Diagrams (Continued)

ADC12L038 Hardware Power Up/Down



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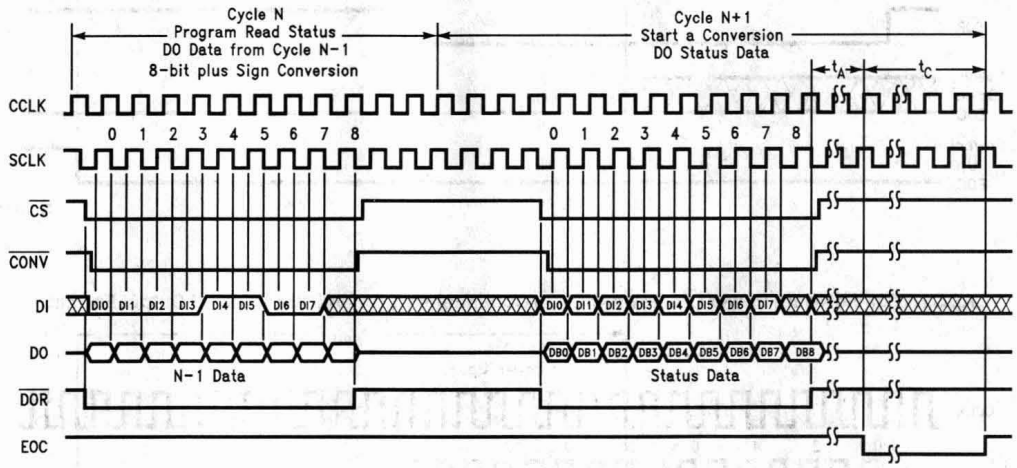
Note: Hardware power up/down may occur at any time. If PD is high while a conversion is in progress that conversion will be corrupted and erroneous data will be stored in the output shift register.

ADC12L038 Configuration Modification—Example of a Status Read



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Note: In order for all 9 bits of status information to be accessible the last conversion programmed before Cycle N needs to have a resolution of 8 bits plus sign, 12 bits, 12 bits plus sign, or greater.

Pin Descriptions

CCLK — The clock applied to this input controls the successive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 μs.

SCLK — This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 μs.

DI — This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. Tables II through V show the assignment of the multiplexer address and the mode select data.

DO — The data output pin. This pin is an active push/pull output when $\overline{CS}$ is Low. When $\overline{CS}$ is High this output is in TRI-STATE. The A/D conversion result (D0–D12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see Table I). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see Table V).

EOC — This pin is an active push/pull output and indicates the status of the ADC12L030/2/4/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{CS}$ — This is the chip select pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought back low during a conversion, that conversion is prematurely ended. The data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought back low during a conversion in progress the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied, it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. Table V details the data required.

$\overline{DOR}$ — This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{CONV}$ — A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming Table (Table V) such as 12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.

PD — This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 700 μs to power up after the command is given.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (see Tables II through IV).

The voltage applied to these inputs should not exceed V_A^+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2 — These are the multiplexer output pins.

A/DIN1, A/DIN2 — These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_A^+ or go below AGND (see *Figure 3*).

2

Pin Descriptions (Continued)

V_{REF}^+ This is the positive analog voltage reference input. In order to maintain accuracy the voltage range of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) is 1 V_{DC} to 3.3 V_{DC} and the voltage at V_{REF}^+ cannot exceed V_A^+. See *Figure 4* for recommended bypassing.

V_{REF}^- The negative voltage reference input. In order to maintain accuracy the voltage at this pin must not go below GND or exceed V_A^+. (See *Figure 4*).

V_A^+, V_D^+ These are the analog and digital power supply pins. V_A^+ and V_D^+ are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see *Figure 4*). The operating voltage range of V_A^+ and V_D^+ is 3.0 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin (see *Figure 4*).

AGND This is the analog ground pin (see *Figure 4*).

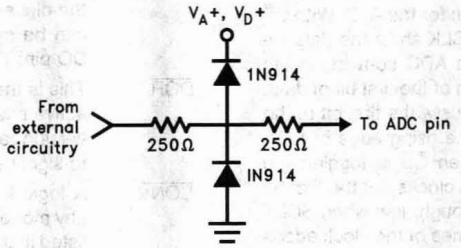

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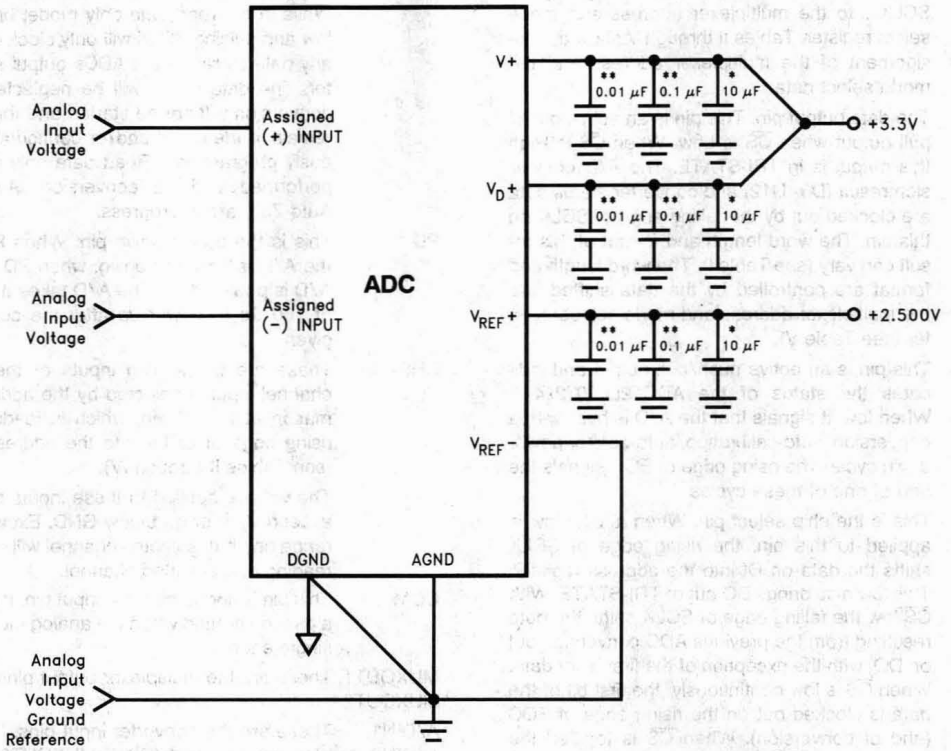
FIGURE 3. Protecting the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 Analog Pins



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*Tantalum

**Monolithic Ceramic or better

FIGURE 4. Recommended Power Supply Bypassing and Grounding

Tables

TABLE I. Data Out Formats

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	MSB First	17 Bits	X	X	X	X	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
		9 Bits	Sign	MSB	6	5	4	3	2	1	LSB								
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	X	X	X	X
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
		9 Bits	LSB	1	2	3	4	5	6	MSB	Sign								
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
		8 Bits	MSB	6	5	4	3	2	1	LSB									
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					
		8 Bits	LSB	1	2	3	4	5	6	MSB									

X = High or Low state.

TABLE II. ADC12L038 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	DI3	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	−								+	−	CH0	CH1	Differential
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	Single-Ended
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

2

Tables (Continued)

TABLE III. ADC12L034 Multiplexer Addressing

MUX Address			Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2					A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	CH0	CH1	CH2	CH3	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	+	−				+	−	CH0	CH1	Differential
L	L	H			+	−		+	−	CH2	CH3	
L	H	L	−	+				−	+	CH0	CH1	
L	H	H			−	+		−	+	CH2	CH3	
H	L	L	+				−	+	−	CH0	COM	Single-Ended
H	L	H			+		−	+	−	CH2	COM	
H	H	L		+			−	+	−	CH1	COM	
H	H	H				+	−	+	−	CH3	COM	

TABLE IV. ADC12L032 and ADC12L030 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-Ended
H	H		+	−	+	−	CH1	COM	

Note: ADC12L030 does not have A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 pins.

Tables (Continued)

TABLE V. Mode Programming

ADC12L038	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Selected (Current)	DO Format (next Conversion Cycle)
ADC12L034	DI0	DI1	DI2		DI3	DI4	DI5	DI6		
ADC12L030 and ADC12L032	DI0	DI1			DI2	DI3	DI4	DI5		
	See Tables II, III or IV				L	L	L	L	12 Bit Conversion	12 or 13 Bit MSB First
	See Tables II, III or IV				L	L	L	H	12 Bit Conversion	16 or 17 Bit MSB First
	See Tables II, III or IV				L	L	H	L	8 Bit Conversion	8 or 9 Bit MSB First
	L	L	L	L	L	L	H	H	12 Bit Conversion of Full-Scale	12 or 13 Bit MSB First
	See Tables II, III or IV				L	H	L	L	12 Bit Conversion	12 or 13 Bit LSB First
	See Tables II, III or IV				L	H	L	H	12 Bit Conversion	16 or 17 Bit LSB First
	See Tables II, III or IV				L	H	H	L	8 Bit Conversion	8 or 9 Bit LSB First
	L	L	L	L	L	H	H	H	12 Bit Conversion of Offset	12 or 13 Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—6 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—10 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—18 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—34 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	X	X	X	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

Note: The A/D powers up with no Auto Cal, no Auto Zero, 10 CCLK acquisition time, 12-bit + sign conversion, power up, 12- or 13-bit MSB first and user mode.

X = Don't Care

TABLE VI. Conversion/Read Data Only Mode Programming

$\overline{CS}$	$\overline{CONV}$	PD	Mode
L	L	L	See Table V for Mode
L	H	L	Read Only (Previous DO Format) No Conversion
H	X	L	Idle
X	X	H	Power Down

X = Don't Care

2

Tables (Continued)

TABLE VII. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	PU	PD	Cal	8 or 9	12 or 13	16 or 17	Sign	Justification	Test Mode
Function	Device Status			DO Output Format Status					
	"High" indicates a Power Up Sequence is in progress	"High" indicates a Power Down Sequence is in progress	"High" indicates an Auto-Cal Sequence is in progress	"High" indicates an 8 or 9 bit format	"High" indicates a 12 or 13 bit format	"High" indicates a 16 or 17 bit format	"High" indicates that the sign bit is included. When "Low" the sign bit is not included.	When "High" the conversion result will be output MSB first. When "Low" the result will be output LSB first.	When "High" the device is in test mode. When "Low" the device is in user mode.

Application Hints

1.0 DIGITAL INTERFACE

1.1 Interface Concepts

The example in *Figure 5* shows a typical sequence of events after the power is applied to the ADC12L030/2/4/8:

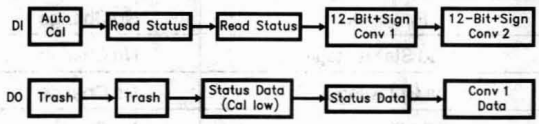

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FIGURE 5. Typical Power Supply Power Up Sequence

The first instruction input to the A/D via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To determine whether the Auto Cal has been completed, a read status instruction is issued to the A/D. Again the data output at that time has no significance since the Auto Cal procedure modifies the data in the output shift register. To retrieve the status information, an additional read status instruction is issued to the A/D. At this time the status data is available on DO. If the Cal signal in the status word is low Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output at this time is again status information. To keep noise from corrupting the A/D conversion, the status can not be read during a conversion. If $\overline{CS}$ is strobed and is brought low during a conversion, that conversion is prematurely ended. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to communicate to the A/D again. Once it has been determined that the A/D has completed a conversion another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

Note, when $\overline{CS}$ is low continuously it is important to transmit the exact number of SCLK cycles, as shown in the timing diagrams. Not doing so will desynchronize the serial communication to the A/D (see Section 1.3).

1.2 Changing Configuration

The configuration of the ADC12L030/2/4/8 on power up defaults to 12-bit plus sign resolution, 12- or 13-bit MSB First, 10 CCLK acquisition time, user mode, no Auto Cal, no Auto Zero, and power up mode. Changing the acquisition time and turning the sign bit on and off requires an 8-bit instruction to be issued to the ADC. This instruction will not start a conversion. The instructions that select a multiplexer address and format the output data do start a conversion. *Figure 6* describes an example of changing the configuration of the ADC12L030/2/4/8.

During I/O sequence 1 the instruction on DI configures the ADC12L030/2/4/8 to do a conversion with 12-bit + sign resolution. Notice that when the 6 CCLK Acquisition and Data Out without Sign instructions are issued to the ADC, I/O sequences 2 and 3, a new conversion is not started. The data output during these instructions is from conversion N which was started during I/O sequence 1. The Configuration Modification timing diagram describes in detail the sequence of events necessary for a Data Out without Sign, Data Out with Sign, or 6/10/18/34 CCLK Acquisition time mode selection. Table V describes the actual data neces-

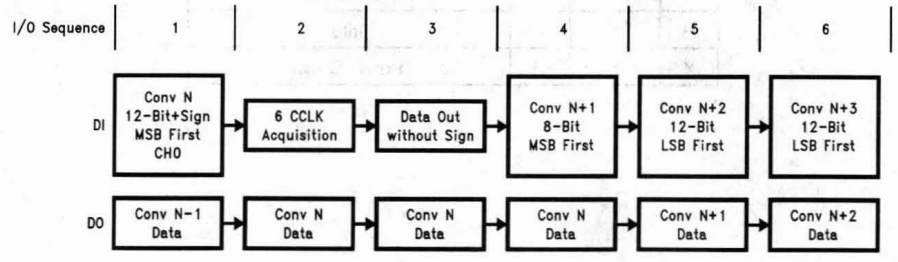

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FIGURE 6. Changing the ADC's Conversion Configuration

Application Hints (Continued)

sary to be input to the ADC to accomplish this configuration modification. The next instruction, shown in *Figure 6*, issued to the A/D starts conversion N+1 with 8 bits of resolution formatted MSB first. Again the data output during this I/O cycle is the data from conversion N.

The number of SCLKs applied to the A/D during any conversion I/O sequence should vary in accord with the data out word format chosen during the previous conversion I/O sequence. The various formats and resolutions available are shown in Table I. In *Figure 6*, since 8-bit without sign MSB first format was chosen during I/O sequence 4, the number of SCLKs required during I/O sequence 5 is 8. In the following I/O sequence the format changes to 12-bit without sine MSB first; therefore the number of SCLKs required during I/O sequence 6 changes accordingly to 12.

1.3 $\overline{CS}$ Low Continuously Considerations

When $\overline{CS}$ is continuously low, it is important to transmit the exact number of SCLK pulses that the ADC expects. Not doing so will desynchronize the serial communications to the ADC. When the supply power is first applied to the ADC, it will expect to see 13 SCLK pulses for each I/O transmission. The number of SCLK pulses that the ADC expects to see is the same as the digital output word length. The digital output word length is controlled by the Data Out (DO) format. The DO format maybe changed any time a conversion is started or when the sign bit is turned on or off. The table below details out the number of clock periods required for different DO formats:

DO Format		Number of SCLKs Expected
8-Bit MSB or LSB First	SIGN OFF	8
	SIGN ON	9
12-Bit MSB or LSB First	SIGN OFF	12
	SIGN ON	13
16-Bit MSB or LSB first	SIGN OFF	16
	SIGN ON	17

If erroneous SCLK pulses desynchronize the communications, the simplest way to recover is by cycling the power supply to the device. Not being able to easily resynchronize the device is a shortcoming of leaving $\overline{CS}$ low continuously.

The number of clock pulses required for an I/O exchange may be different for the case when $\overline{CS}$ is left low continuously vs. the case when $\overline{CS}$ is cycled. Take the I/O sequence detailed in *Figure 5* (Typical Power Supply Sequence) as an example. The table below lists the number of SCLK pulses required for each instruction:

Instruction	$\overline{CS}$ Low Continuously	$\overline{CS}$ Strobed
Auto Cal	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 1	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 2	13 SCLKs	13 SCLKs

1.4 Analog Input Channel Selection

The data input on DI also selects the channel configuration for a particular A/D conversion (see Tables II, III, IV and V).

In *Figure 6* the only times when the channel configuration could be modified would be during I/O sequences 1, 4, 5 and 6. Input channels are reselected before the start of each new conversion. Shown below is the data bit stream required on DI, during I/O sequence number 4 in *Figure 6*, to set CH1 as the positive input and CH0 as the negative input for the different versions of ADCs:

Part Number	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
ADC12L030	L	H	L	L	H	L	X	X
ADC12L032	L	H	L	L	H	L	X	X
ADC12L034	L	H	L	L	L	H	L	X
ADC12L038	L	H	L	L	L	L	H	L

Where X can be a logic high (H) or low (L).

1.5 Power Up/Down

The ADC may be powered down at any time by taking the PD pin HIGH or by the instruction input on DI (see Tables V and VI, and the Power Up/Down timing diagrams). When the ADC is powered down in this way the circuitry necessary for an A/D conversion is deactivated. The circuitry necessary for digital I/O is kept active. Hardware power up/down is controlled by the state of the PD pin. Software power up/down is controlled by the instruction issued to the ADC. If a software power up instruction is issued to the ADC while a hardware power down is in effect (PD pin high) the device will remain in the power-down state. If a software power down instruction is issued to the ADC while a hardware power up is in effect (PD pin low), the device will power down. When the device is powered down by software, it may be powered up by either issuing a software power up instruction or by taking PD pin high and then low. If the power down command is issued during an A/D conversion, that conversion is disrupted. Therefore, the data output after power up cannot be relied on.

1.6 User Mode and Test Mode

An instruction may be issued to the ADC to put it into test mode. Test mode is used by the manufacturer to verify complete functionality of the device. During test mode CH0–CH7 become active outputs. If the device is inadvertently put into the test mode with $\overline{CS}$ low continuously, the serial communications may be desynchronized. Synchronization may be regained by cycling the power supply voltage to the device. Cycling the power supply voltage will also set the device into user mode. If $\overline{CS}$ is used in the serial interface, the ADC may be queried to see what mode it is in. This is done by issuing a "read STATUS register" instruction to the ADC. When bit 9 of the status register is high the ADC is in test mode; when bit 9 is low the ADC is in user mode. As an alternative to cycling the power supply, an instruction sequence may be used to return the device to user mode. This instruction sequence must be issued to the ADC using $\overline{CS}$.

Application Hints (Continued)

The following table lists the instructions required to return the device to user mode:

Instruction	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
TEST MODE	H	X	X	X	H	H	H	H
RESET	L	L	L	L	H	H	H	L
TEST MODE	L	L	L	L	H	L	H	L
INSTRUCTIONS	L	L	L	L	H	L	H	H
USER MODE	L	L	L	L	H	H	H	H
Power Up	L	L	L	L	H	L	H	L
Set DO with or without Sign	H or L	L	L	L	H	H	L	H
Set Acquisition Time	H or L	H or L	L	L	H	H	H	L
Start a Conversion	H or L	H or L	H or L	H or L	L	H or L	H or L	H or L

X = Don't Care

After returning to user mode with the user mode instruction the power up, data with or without sign, and acquisition time instructions need to be resent to ensure that the ADC is in the required state before a conversion is started.

1.7 Reading the Data Without Starting a Conversion

The data from a particular conversion may be accessed without starting a new conversion by ensuring that the $\overline{CONV}$ line is taken high during the I/O sequence. See the Read Data timing diagrams. Table VI describes the operation of the $\overline{CONV}$ pin.

2.0 DESCRIPTION OF THE ANALOG MULTIPLEXER

For the ADC12L038, the analog input multiplexer can be configured with 4 differential channels or 8 single ended channels with the COM input as the zero reference or any combination thereof (see *Figure 7*). The difference between the voltages on the V_{REF}^+ and V_{REF}^- pins determines the input voltage span (V_{REF}). The analog input voltage range is 0 to V_A^+. Negative digital output codes result when $V_{IN}^- > V_{IN}^+$. The actual voltage at V_{IN}^- or V_{IN}^+ cannot go below AGND.

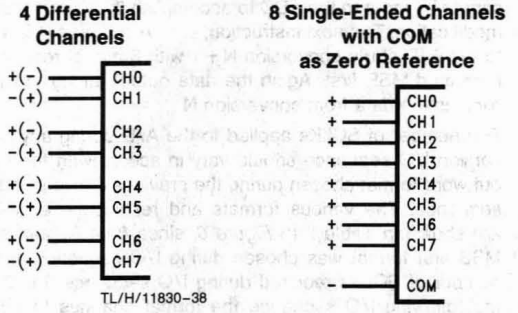

FIGURE 7

CH0, CH2, CH4, and CH6 can be assigned to the MUXOUT1 pin in the differential configuration, while CH1, CH3, CH5, and CH7 can be assigned to the MUXOUT2 pin. In the differential configuration, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The A/DIN1 and A/DIN2 pins can be assigned positive or negative polarity.

With the single-ended multiplexer configuration CH0 through CH7 can be assigned to the MUXOUT1 pin. The COM pin is always assigned to the MUXOUT2 pin. A/DIN1 is assigned as the positive input; A/DIN2 is assigned as the negative input. (See *Figure 8*).

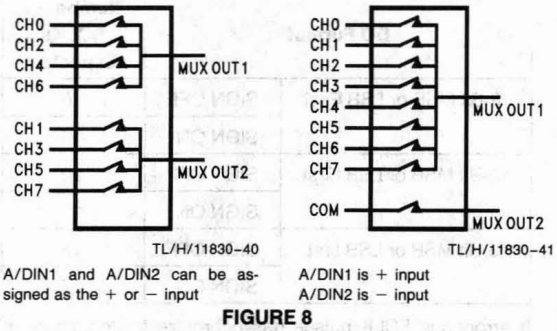

FIGURE 8

The Multiplexer assignment tables for the ADC12L030,2,4,8 (Tables II, III, and IV) summarize the aforementioned functions for the different versions of A/Ds.

2.1 Biasing for Various Multiplexer Configurations

Figure 9 is an example of biasing the device for single-ended operation. The sign bit is always low. The digital output range is 0 0000 0000 0000 to 0 1111 1111 1111. One LSB is equal to 610 μV (2.5V/4096 LSBs).

Application Hints (Continued)

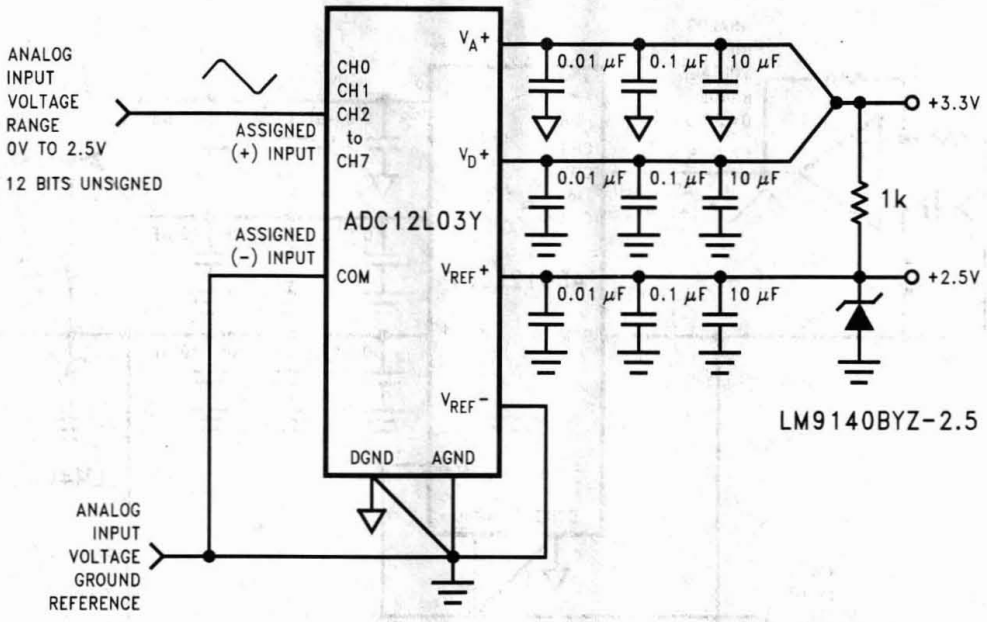

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FIGURE 9. Single-Ended Biasing

For pseudo-differential signed operation the biasing circuit shown in *Figure 10* shows a signal AC coupled to the ADC. This gives a digital output range of −4096 to +4095. With a 1.25V reference, as shown, 1 LSB is equal to 305 μV. Although the ADC is not production tested with a 1.25V reference linearity error typically will not change more than 0.3 LSB. With the ADC set to an acquisition time of 10 clock periods the input biasing resistor needs to be 600Ω or less. Notice though that the input coupling capacitor needs to be made fairly large to bring down the high pass corner. Increasing the acquisition time to 34 clock periods (with a 5 MHz CCLK frequency) would allow the 600Ω to increase to 6k, which with a 1 μF coupling capacitor would set the high pass corner at 26 Hz. The value of R1 will depend on the value of R2.

An alternative method for biasing pseudo-differential operation is to use the +2.5V from the LM9140 to bias any amplifier circuits driving the ADC as shown in *Figure 11.* The value of the resistor pull-up biasing the LM9140-2.5 will depend upon the current required by the op amp biasing circuitry.

Fully differential operation is shown in *Figure 12.* One LSB for this case is equal to (2.5V/4096) = 610 mV.

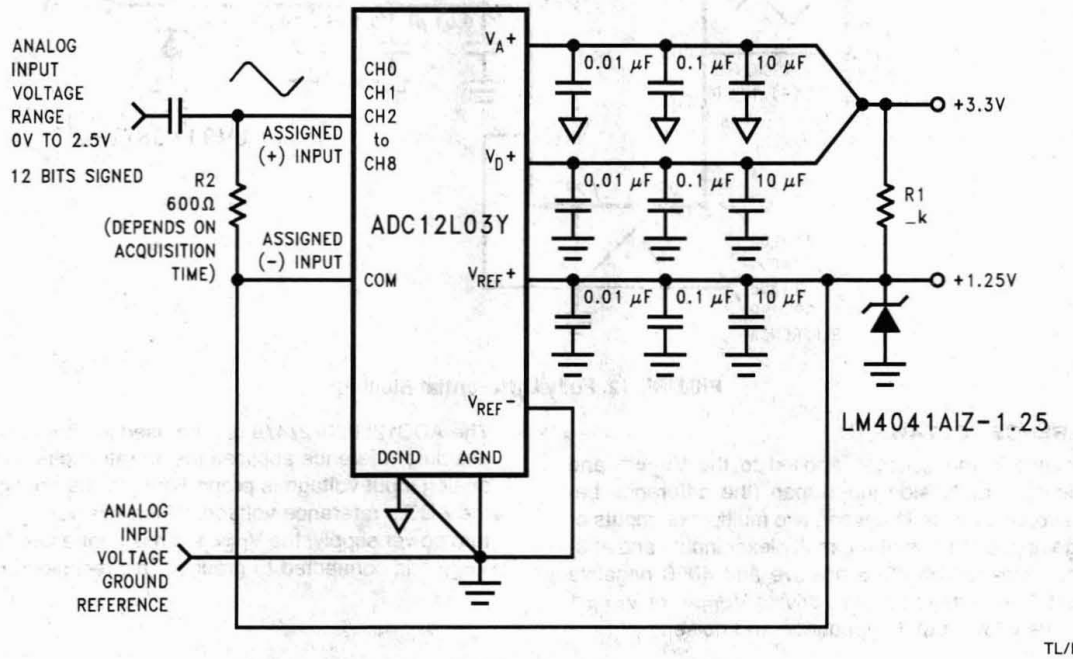

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FIGURE 10. Pseudo-Differential Biasing with the Signal Source AC Coupled Directly into the ADC

Application Hints (Continued)

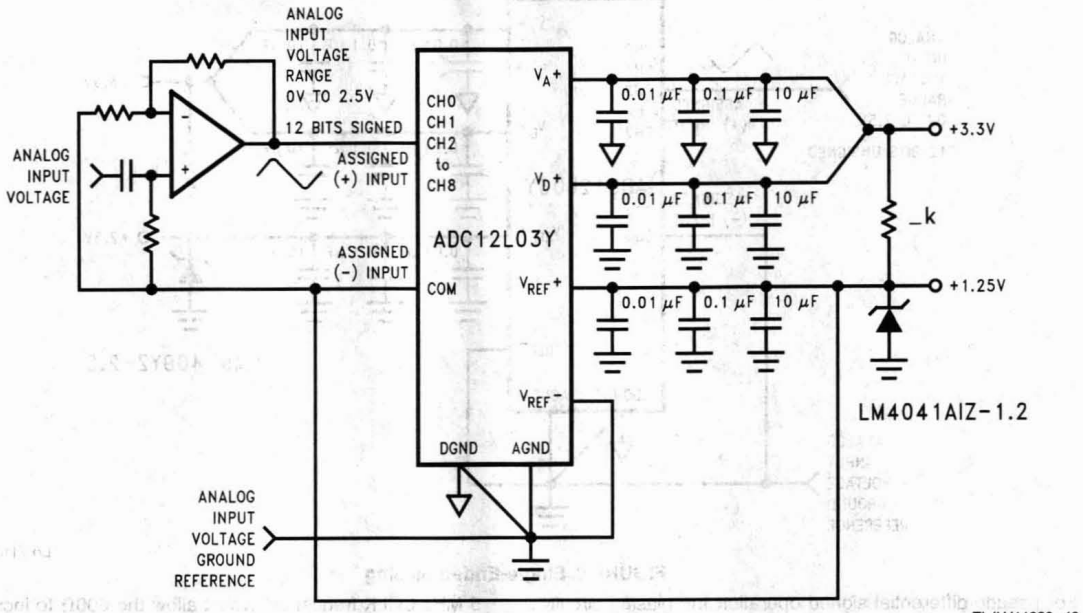

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FIGURE 11. Alternative Pseudo-Differential Biasing

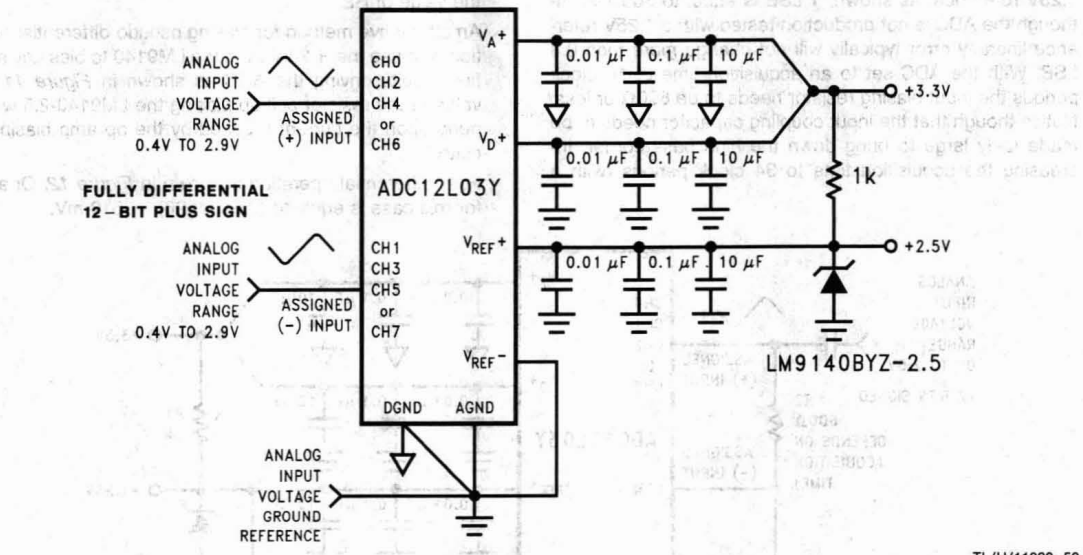

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FIGURE 12. Fully Differential Biasing

3.0 REFERENCE VOLTAGE

The difference in the voltages applied to the $V_{REF}+$ and $V_{REF}-$ defines the analog input span (the difference between the voltage applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving $V_{REF}+$ or $V_{REF}-$ must have very low output impedance and noise.

The ADC12L030/2/4/8 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the $V_{REF}+$ pin is connected to V_A+ and $V_{REF}-$ is connected to ground. This technique relaxes the

Application Hints (Continued)

system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

Below are recommended references along with some key specifications.

Part Number	Output Voltage Tolerance	Temperature Coefficient (max)
LM4041CIM3-Adj	±0.5%	±100ppm/°C
LM4040AIM3-2.5	±0.1%	±100ppm/°C
LM9140BYZ-2.5	±0.5%	±25ppm/°C
LM368Y-2.5	±0.1%	±20ppm/°C

The reference voltage inputs are not fully differential. The ADC12L030/2/4/8 will not generate correct conversions or comparisons if V_{REF}^+ is taken below V_{REF}^-. Correct conversions result when V_{REF}^+ and V_{REF}^- differ by 1V and remain, at all times, between ground and V_A^+. The V_{REF} common mode range, $(V_{REF}^+ + V_{REF}^-)/2$, is restricted to $(0.1 \times V_A^+)$ to $(0.6 \times V_A^+)$. Therefore, with $V_A^+ = 3.3V$ the center of the reference ladder should not go below 0.33V or above 1.98V. *Figure 13* is a graphic representation of the voltage restrictions on V_{REF}^+ and V_{REF}^-.

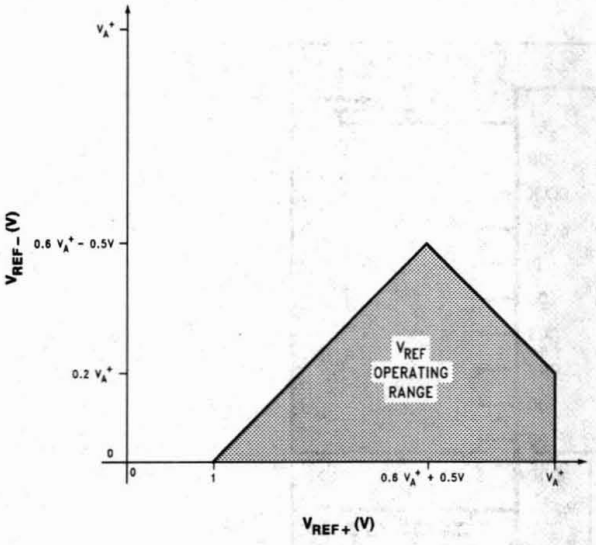

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FIGURE 13. V_{REF} Operating Range

4.0 ANALOG INPUT VOLTAGE RANGE

The ADC12L030/2/4/8's fully differential ADC generate a two's complement output that is found by using the equations shown below:

for (12-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-)\,(4096)}{(V_{REF}^+ - V_{REF}^-)}$$

for (8-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-)\,(256)}{(V_{REF}^+ - V_{REF}^-)}$$

Round off to the nearest integer value between −4096 to 4095 for 12-bit resolution and between −256 to 255 for 8-bit resolution if the result of the above equation is not a whole number.

Examples are shown in the table below:

V_{REF}^+	V_{REF}^-	V_{IN}^+	V_{IN}^-	Digital Output Code
+2.5V	+1V	+1.5V	0V	0,1111,1111,1111
+2.500V	0V	+2V	0V	0,1100,1100,1101
+2.500V	0V	+2.499V	+2.500V	1,1111,1111,1111
+2.500V	0V	0V	+2.500V	1,0000,0000,0000

5.0 INPUT CURRENT

At the start of the acquisition window (t_A) a charging current flows into or out of the analog input pins (A/DIN1 and A/DIN2) depending on the input voltage polarity. The analog input pins are CH0–CH7 and COM when A/DIN1 is tied to MUXOUT1 and A/DIN2 is tied to MUXOUT2. The peak value of this input current will depend on the actual input voltage applied, the source impedance and the internal multiplexer switch on resistance. With MUXOUT1 tied to A/DIN1 and MUXOUT2 tied to A/DIN2 the internal multiplexer switch on resistance is typically 1.6 kΩ. The A/DIN1 and A/DIN2 mux on resistance is typically 750Ω.

6.0 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<600Ω), the input charging current will decay, before the end of the S/H's acquisition time of 2 μs (10 CCLK periods with f_C = 5 MHz), to a value that will not introduce any conversion errors. For high source impedances, the S/H's acquisition time can be increased to 18 or 34 CCLK periods. For less ADC resolution and/or slower CCLK frequencies the S/H's acquisition time may be decreased to 6 CCLK periods. To determine the number of clock periods (N_C) required for the acquisition time with a specific source impedance for the various resolutions the following equations can be used:

12 Bit + Sign $N_C = [R_S + 2.3] \times f_C \times 0.824$

8 Bit + Sign $N_C = [R_S + 2.3] \times f_C \times 0.57$

Where f_C is the conversion clock (CCLK) frequency in MHz and R_S is the external source resistance in kΩ. As an exam-

Application Hints (Continued)

ple, operating with a resolution of 12 Bits+sign, a 5 MHz clock frequency and maximum acquistion time of 34 conversion clock periods the ADC's analog inputs can handle a source impedance as high as 6 kΩ. The acquisition time may also be extended to compensate for the settling or response time of external circuitry connected between the MUXOUT and A/DIN pins.

The acquisition time (t_A) is started by a falling edge of SCLK and ended by a rising edge of CCLK (see Timing Diagrams). If SCLK and CCLK are asynchronous one extra CCLK clock period may be inserted into the programmed acquisition time for synchronization. Therefore with asnychronous SCLK and CCLK the acquisition time will change from conversion to conversion.

7.0 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, CH0–CH7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

8.0 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

9.0 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. The minimum power supply bypassing capacitors recommended are low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF monolithic ceramic capacitors. More or different bypassing may be necessary depending on the overall system requirements. Separate bypass capacitors should be used for the V_A^+ and V_D^+ supplies and placed as close as possible to these pins.

10.0 GROUNDING

The ADC12L030/2/4/8's performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all components that handle analog signals. The digital and analog ground planes are connected together at only one point, either the power supply ground or at the pins of the ADC. This greatly reduces the occurence of ground loops and noise.

Shown in *Figure 14* is the ideal ground plane layout for the ADC12L038 along with ideal placement of the bypass capacitors. The circuit board layout shown in *Figure 14* uses three bypass capacitors: 0.01 μF (C1) and 0.1 μF (C2) surface mount capacitors and 10 μF (C3) tantalum capacitor.

11.0 CLOCK SIGNAL LINE ISOLATION

The ADC12L030/2/4/8's performance is optimized by routing the analog input/output and reference signal conductors as far as possible from the conductors that carry the clock signals to the CCLK and SCLK pins. Ground traces parallel to the clock signal traces can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

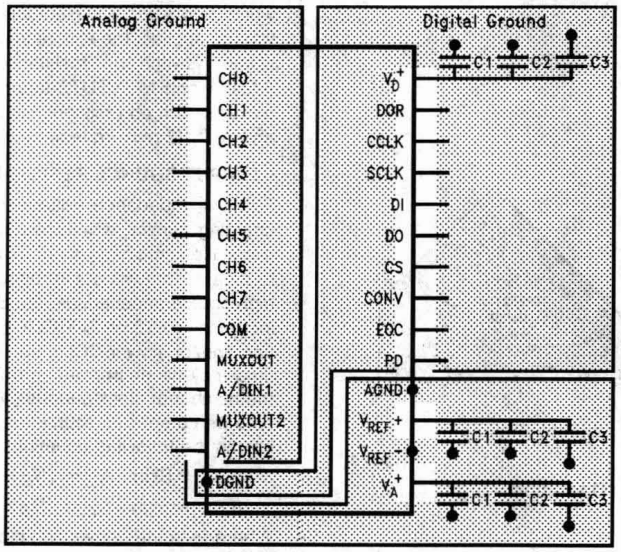


FIGURE 14. Ideal Ground Plane for the ADC12L038

Application Hints (Continued)

12.0 THE CALIBRATION CYCLE

A calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize after initial turn on. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ±0.4 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if the Power Supply Voltage and the ambient temperature do not change significantly (see the curves in the Typical Performance Characteristics).

13.0 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature or the power supply voltage change significantly. (See the curves titled "Zero Error Change vs Ambient Temperature" and "Zero Error Change vs Supply Voltage" in the Typical Performance Characteristics.)

14.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.8)\ dB$$

where n is the A/D's resolution in bits.

The effective bits of a real A/D converter, therefore, can be found by:

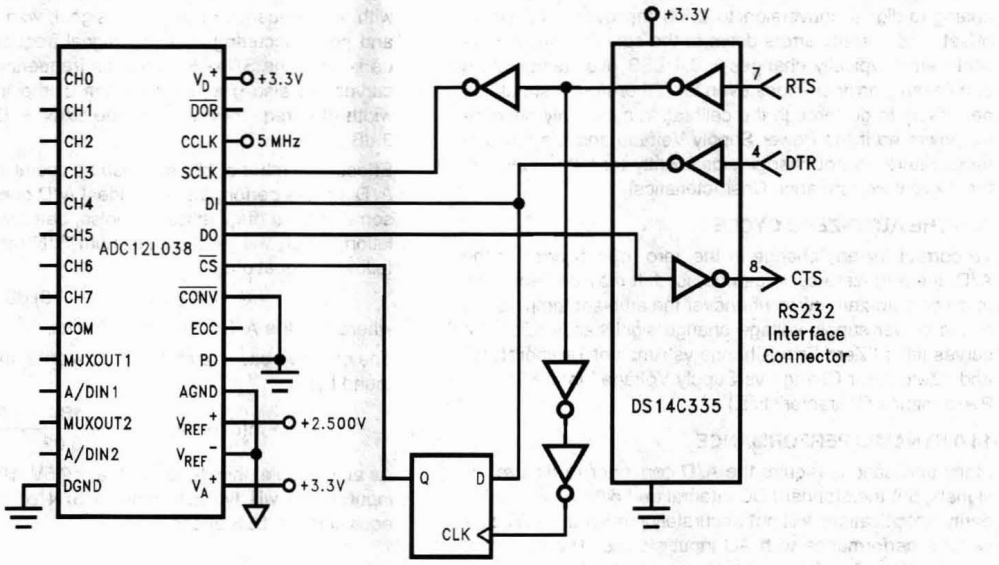
$$n(\text{effective}) = \frac{S/N(dB) - 1.8}{6.02}$$

As an example, this device with a ±2.5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

Application Hints (Continued)

15.0 AN RS232 SERIAL INTERFACE

Shown below is a schematic for an RS232 interface to any IBM and compatible PCs. The DTR, RTS, and CTS RS232 signal lines are buffered via level translators and connected to the ADC12L038's DI, SCLK, and DO pins, respectively. The D flip flop drive the $\overline{CS}$ control line.



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Note: V_A^+, V_D^+, and V_{REF}^+ on the ADC12L038 each have 0.01 μF and 0.1 μF chip caps, and 10 μF tantalum caps. All logic devices are bypassed with 0.1 μF caps. The DS14C335 has an internal DC-DC converter that generates the necessary TIA/EIA-232-E output levels from a 3.3V supply. There are four 0.47 μF capacitors required for the DC-DC converter that are not shown in the above schematic.

The assignment of the RS232 port is shown below

			B7	B6	B5	B4	B3	B2	B1	B0
COM1	Input Address	3FE	X	X	X	CTS	X	X	X	X
	Output Address	3FC	X	X	X	0	X	X	RTS	DTR

A sample program, written in Microsoft™ QuickBasic, is shown on the next page. The program prompts for data mode select instruction to be sent to the A/D. This can be found from the Mode Programming table shown earlier. The data should be entered in "1"s and "0"s as shown in the table with DI0 first. Next the program prompts for the number of SCLKs required for the programmed mode select instruction. For instance, to send all "0"s to the A/D, selects CH0 as the +input, CH1 as the −input, 12-bit conversion, and 13-bit MSB first data output format (if the sign bit was not turned off by a previous instruction). This would require 13 SCLK periods since the output data format is 13 bits. The part powers up with No Auto Cal, No Auto Zero, 10 CCLK Acquisition Time, 12-bit conversion, data out with sign, 12- or 13-bit MSB First, power up, and user mode. Auto Cal, Auto Zero, Power UP and Power Down instructions do not change these default settings. The following power up sequence should be followed:

1. Run the program
2. Prior to responding to the prompt apply the power to the ADC12L038
3. Respond to the program prompts

It is recommended that the first instruction issued to the ADC12L038 be Auto Cal (see Section 1.1).

Application Hints (Continued)

```
'variables DOL=Data Out word length, DI=Data string for A/D DI input,
'          DO=A/D result string
'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC))              'set RTS HIGH
OUT &H3FC, (&HFE AND INP (&H3FC))            'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC))            'SET RTS LOW

OUT &H3FC, (&HEF AND INP (&H3FC))            'set B4 low
10
LINE INPUT "DI data for ADC12038 (see Mode Table on data sheet)"; DI$
INPUT "ADC12038 output word length (8,9,12,13,16 or 17)"; DOL
20

'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC))              'set RTS HIGH
OUT &H3FC, (&HFE AND INP (&H3FC))            'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC))            'SET RTS LOW

'SET CS# LOW
OUT &H3FC, (&H2 OR INP (&H3FC))              'set RTS HIGH
OUT &H3FC, (&H1 OR INP (&H3FC))              'SET DTR HIGH
OUT &H3FC, (&HFD AND INP (&H3FC))            'SET RTS LOW

DO$=""                                       'reset DO variable
  OUT &H3FC, (&H1 OR INP (&H3FC))            'SET DTR HIGH
  OUT &H3FC, (&HFD AND INP (&H3FC))          'SCLK low
FOR N=1 TO 8
  Temp$=MID$(DI$,N,1)
  IF Temp$="0"THEN
    OUT &H3FC,(&H1 OR INP(&H3FC))
  ELSE OUT &H3FC, (&HFE AND INP (&H3FC))
  END IF 'out DI
  OUT &H3FC,(&H2 OR INP (&H3FC))             'SCLK high
  IF (INP (&H3FE) AND 16)=16 THEN
    DO$=DO$+"0"
    ELSE
    DO$=DO$+"1"
  END IF                                     'Input DO
  OUT &H3FC, (&H1 OR INP (&H3FC))            'SET DTR HIGH
  OUT &H3FC, (&HFD AND INP (&H3FC))          'SCLK low
NEXT N
IF DOL>8 THEN
  FOR N=9 TO DOL
  OUT &H3FC,(&H1 OR INP (&H3FC))             'SET DTR HIGH
  OUT &H3FC,(&HFD AND INP (&H3FC))           'SCLK low
  OUT &H3FC,(&H2 OR INP (&H3FC))             'SCLK high

  IF (INP(&H3FE) AND &H16)=&H16 THEN
    DO$=DO$+"0"
  ELSE
    DO$=DO$+"1"
  END IF
  NEXT N
END IF
OUT &H3FC,(&HFA AND INP(&H3FC))              'SCLK low and DI high
FOR N=1 TO 500
NEXT N
PRINT DO$
INPUT "Enter "C" to convert else "RETURN" to alter DI data"; s$
IF s$="C" OR s$="c" THEN
  GOTO 20
ELSE
  GOTO 10
END IF
END
```

National Semiconductor

ADC12130/ADC12132/ADC12138 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12130, ADC12132 and ADC12138 are 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexer. The ADC12132 and ADC12138 have a 2 and an 8 channel multiplexer, respectively. The differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12130 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. The ADC12130 family is tested with a 5 MHz clock. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to typically less than ±1 LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +5V) can be accommodated with a single +5V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE™. For complementary voltage references see the LM4040, LM4041 or LM9140.

Features

- Serial I/O (MICROWIRE, SPI and QSPI Compatible)
- 2 or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- 0V to 5V analog input range with single 5V power supply

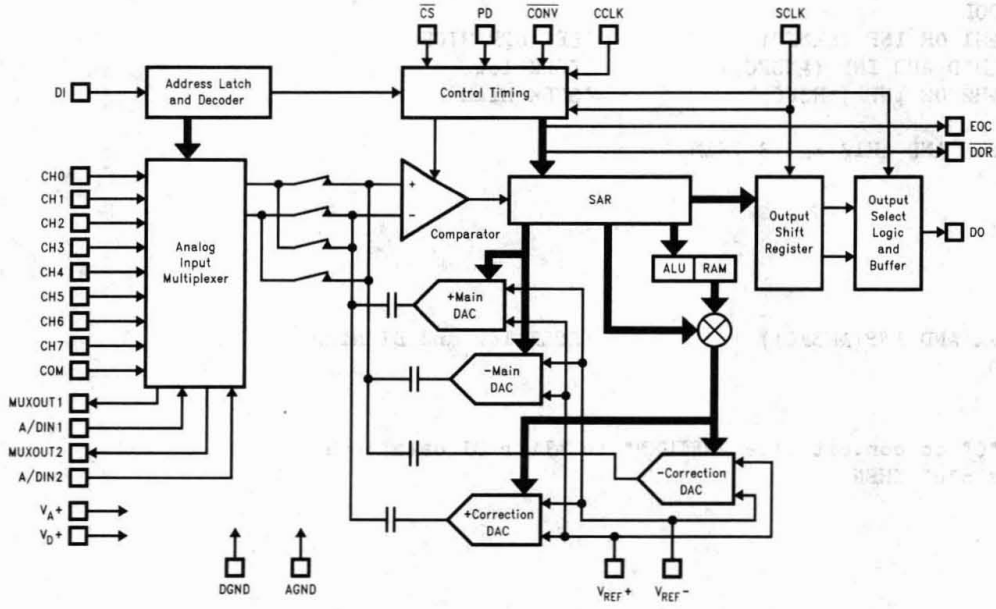
Key Specifications

■ Resolution	12-bit plus sign
■ 12-bit plus sign conversion time	8.8 μs (max)
■ 12-bit plus sign throughput time	14 μs (max)
■ Integral linearity error	±2 LSB (max)
■ Single supply	3.3V or 5V ±10%
■ Power dissipation	
— 3.3V	15 mW (max)
— 3.3V power down	40 μW (typ)
— 5V	33 mW (max)
— 5V power down	100 μW (typ)

Applications

- Pen-based computers
- Digitizers
- Global positioning systems

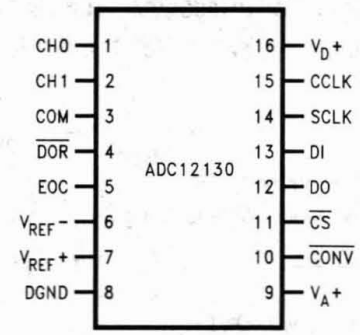
ADC12138 Simplified Block Diagram



TL/H/12079–1

Connection Diagrams

16-Pin Dual-In-Line and Wide Body SO Packages



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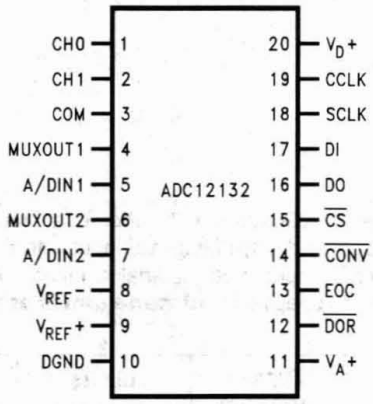
Top View

20-Pin SSOP Package



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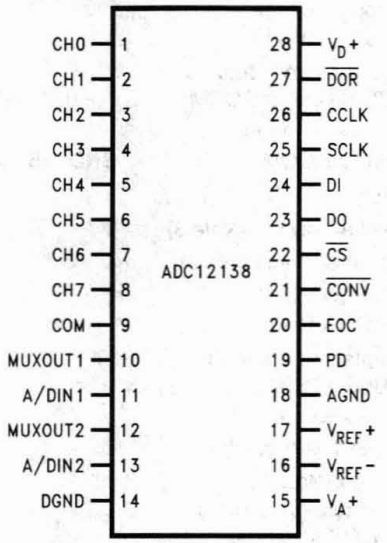
Top View

28-Pin Dual-In-Line, SSOP and Wide Body SO Packages



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Top View

Ordering Information

Industrial Temperature Range $-40°C \leq T_A \leq +85°C$	NS Package Number
ADC12130CIN	N16E, Dual-In-Line
ADC12130CIWM	M16B, Wide Body SO
ADC12132CIMSA	MSA20, SSOP
ADC12138CIN	N28B, Dual-In-Line
ADC12138CIWM	M28B
ADC12138CIMSA	MSA28, SSOP

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage ($V^+ = V_A^+ = V_D^+$)	6.5V
Voltage at Inputs and Outputs except CH0–CH7 and COM	−0.3V to V^+ +0.3V
Voltage at Analog Inputs CH0–CH7 and COM	GND −5V to V^+ +5V
$\lvert V_A^+ - V_D^+ \rvert$	300 mV
Input Current at Any Pin (Note 3)	±30 mA
Package Input Current (Note 3)	±120 mA
Package Dissipation at T_A = 25°C (Note 4)	500 mW
ESD Susceptability (Note 5) Human Body Model	1500V
Soldering Information N Packages (10 seconds)	260°C
SO Package (Note 6): Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12130CIN, ADC12130CIWM, ADC12132CIMSA, ADC12138CIMSA, ADC12138CIN, ADC12138CIWM	−40°C ≤ T_A ≤ +85°C
Supply Voltage ($V^+ = V_A^+ = V_D^+$)	+3.0V to +5.5V
$\lvert V_A^+ - V_D^+ \rvert$	≤ 100 mV
V_{REF}^+	0V to V_A^+
V_{REF}^-	0V to V_{REF}^+
V_{REF} ($V_{REF}^+ - V_{REF}^-$)	1V to V_A^+
V_{REF} Common Mode Voltage Range $\frac{(V_{REF}^+ + V_{REF}^-)}{2}$	0.1 V_A^+ to 0.6 V_A^+
A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 Voltage Range	0V to V_A^+
A/D IN Common Mode Voltage Range $\frac{(V_{IN}^+ + V_{IN}^-)}{2}$	0V to V_A^+

Converter Electrical Characteristics

The following specifications apply for ($V^+ = V_A^+ = V_D^+ = +5V$, $V_{REF}^+ = +4.096V$, and fully differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A^+ = V_D^+ = 3.3V$, $V_{REF}^+ = 2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}^- = 0V$, 12-bit + sign conversion mode, source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \le 25\Omega$, $f_{CK} = f_{SK}$ = 5 MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldfade limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution			**12 + sign**	Bits (min)
+ILE	Positive Integral Linearity Error	After Auto-Cal (Notes 12, 18)	±1/2	**±2**	LSB (max)
−ILE	Negative Integral Linearity Error	After Auto-Cal (Notes 12, 18)	±1/2	**±2**	LSB (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1.5**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (Notes 12, 18)	±1/2	**±3.0**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (Notes 12, 18)	±1/2	**±3.0**	LSB (max)
	Offset Error	After Auto-Cal (Notes 5, 18) $V_{IN}(+) = V_{IN}(-)$ = 2.048V	±1/2	**±2**	LSB (max)
	DC Common Mode Error	After Auto-Cal (Note 15)	±2		LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (Notes 12, 13 and 14)	±1		LSB

Converter Electrical Characteristics

The following specifications apply for ($V^+ = V_A^+ = V_D^+ = +5V$, $V_{REF}^+ = +4.096V$, and fully differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A^+ = V_D^+ = 3.3V$, $V_{REF}^+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}^- = 0V$, 12-bit + sign conversion mode, source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS (Continued)					
	Multiplexer Channel to Channel Matching		±0.05		LSB
	Power Supply Sensitivity	$V^+ = +5V \pm 10\%$ $V_{REF} = +4.096V$			
	Offset Error		±0.5		LSB
	+ Full-Scale Error		±0.5		LSB
	− Full-Scale Error		±0.5		LSB
	+ Integral Linearity Error		±0.5		LSB
	− Integral Linearity Error		±0.5		LSB
UNIPOLAR DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	69.4		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	68.3		dB
		$f_{IN} = 40$ kHz, $V_{IN} = 5\ V_{PP}$, $V_{REF}^+ = 5.0V$	65.7		dB
	−3 dB Full Power Bandwidth	$V_{IN} = 5\ V_{PP}$, where S/(N+D) drops 3 dB	31		kHz
DIFFERENTIAL DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = \pm 5V$, $V_{REF}^+ = 5.0V$	77.0		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 5V$, $V_{REF}^+ = 5.0V$	73.9		dB
		$f_{IN} = 40$ kHz, $V_{IN} = \pm 5V$, $V_{REF}^+ = 5.0V$	67.0		dB
	−3 dB Full Power Bandwidth	$V_{IN} = \pm 5V$, where S/(N+D) drops 3 dB	40		kHz

Electrical Characteristics

The following specifications apply for ($V^+ = V_A^+ = V_D^+ = +5V$, $V_{REF}^+ = +4.096V$, and fully differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A^+ = V_D^+ = +3.3V$, $V_{REF}^+ = 2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}^- = 0V$, 12-bit + sign conversion mode, source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{REF}	Reference Input Capacitance		85		pF
$C_{A/D}$	A/DIN1 and A/DIN2 Analog Input Capacitance		75		pF
	A/DIN1 and A/DIN2 Analog Input Leakage Current	$V_{IN} = +5.0V$ or $V_{IN} = 0V$	±0.1		μA
	CH0–CH7 and COM Input Voltage		**GND − 0.05** **$V_A^+ + 0.05$**		V
C_{CH}	CH0–CH7 and COM Input Capacitance		10		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF
	Off Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	−0.01		μA
		On Channel = 0V and Off Channel = 5V	0.01		μA
	On Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	0.01		μA
		On Channel = 0V and Off Channel = 5V	−0.01		μA
	MUXOUT1 and MUXOUT2 Leakage Current	$V_{MUXOUT} = 5.0V$ or $V_{MUXOUT} = 0V$	0.01		μA
R_{ON}	MUX On Resistance	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	850	**1900**	Ω (max)
	R_{ON} Matching Channel to Channel	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	5		%
	Channel to Channel Crosstalk	$V_{IN} = 5\ V_{PP}$, $f_{IN} = 40$ kHz	−72		dB
	MUX Bandwidth		90		kHz

DC and Logic Electrical Characteristics

The following specifications apply for ($V^+ = V_A^+ = V_D^+ = +5V$, $V_{REF}^+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A^+ = V_D^+ = +3.3V$, $V_{REF}^+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}^- = 0V$, 12-bit + sign conversion mode, source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldfade limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 7, 8 and 9)

Symbol	Parameter	Conditions	Typical (Note 10)	$V^+ = V_A^+ = V_D^+ = 3.3V$ Limits (Note 11)	$V^+ = V_A^+ = V_D^+ = 5V$ Limits (Note 11)	Units (Limits)
CCLK, $\overline{CS}$, $\overline{CONV}$, DI, PD AND SCLK INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_A^+ = V_D^+ = V^+ + 10\%$		**2.0**	**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_A^+ = V_D^+ = V^+ - 10\%$		**0.8**	**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = V^+$	0.005	**1.0**	**1.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	**−1.0**	μA (min)
DO, EOC AND $\overline{DOR}$ DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_A^+ = V_D^+ = V^+ - 10\%$, $I_{OUT} = -360\ \mu A$		**2.4**	**2.4**	V (min)
		$V_A^+ = V_D^+ = V^+ - 10\%$, $I_{OUT} = -10\ \mu A$		**2.9**	**4.25**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_A^+ = V_D^+ = V^+ - 10\%$ $I_{OUT} = 1.6$ mA		**0.4**	**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = 0V$ $V_{OUT} = V^+$	−0.1 −0.1	**−3.0** **3.0**	**−3.0** **3.0**	μA (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	−14			mA
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_D^+$	16			mA
POWER SUPPLY CHARACTERISTICS						
I_D^+	Digital Supply Current	 $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	 600 20	**1.5**	**2.5**	mA (max) μA μA
I_A^+	Positive Analog Supply Current	 $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	 10 0.1	**3.0**	**4.0**	mA (max) μA μA
I_{REF}	Reference Input Current	 $\overline{CS}$ = HIGH, Powered Down, CCLK on $\overline{CS}$ = HIGH, Powered Down, CCLK off	 70 0.1			 μA μA

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AC Electrical Characteristics

The following specifications apply for ($V^+ = V_A^+ = V_D^+ = +5V$, $V_{REF}^+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A^+ = V_D^+ = +3.3V$, $V_{REF}^+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), V_{REF}^- = 0V, 12-bit + sign conversion mode, source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \leq 25\Omega$, $f_{CK} = f_{SK}$ = 5 MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
f_{CK}	Conversion Clock (CCLK) Frequency		10 1	**5**	MHz (max) MHz (min)
f_{SK}	Serial Data Clock SCLK Frequency		10 0	**5**	MHz (max) Hz (min)
	Conversion Clock Duty Cycle			**40** **60**	% (min) % (max)
	Serial Data Clock Duty Cycle			**40** **60**	% (min) % (max)
t_C	Conversion Time	12-Bit + Sign or 12-Bit	44(t_{CK})	**44(t_{CK})**	(max)
				8.8	μs (max)
t_A	Acquisition Time (Note 19)	6 Cycles Programmed	6(t_{CK})	**6(t_{CK})** **7(t_{CK})**	(min) (max)
				1.2 **1.4**	μs (min) μs (max)
		10 Cycles Programmed	10(t_{CK})	**10(t_{CK})** **11(t_{CK})**	(min) (max)
				2.0 **2.2**	μs (min) μs (max)
		18 Cycles Programmed	18(t_{CK})	**18(t_{CK})** **19(t_{CK})**	(min) (max)
				3.6 **3.8**	μs (min) μs (max)
		34 Cycles Programmed	34(t_{CK})	**34(t_{CK})** **35(t_{CK})**	(min) (max)
				6.8 **7.0**	μs (min) μs (max)
t_{CAL}	Self-Calibration Time		4944(t_{CK})	**4944(t_{CK})**	(max)
				988.8	μs (max)
t_{AZ}	Auto-Zero Time		76(t_{CK})	**76(t_{CK})**	(max)
				15.2	μs (max)
t_{SYNC}	Self-Calibration or Auto-Zero Synchronization Time from DOR		2(t_{CK})	**2(t_{CK})** **3(t_{CK})**	(min) (max)
				0.40 **0.60**	μs (min) μs (max)
$t_{\overline{DOR}}$	DOR High Time when $\overline{CS}$ is Low Continuously for Read Data and Software Power Up/Down		9(t_{SK})	**9(t_{SK})**	(max)
				1.8	μs (max)
$t_{\overline{CONV}}$	$\overline{CONV}$ Valid Data Time		8(t_{SK})	**8(t_{SK})**	(max)
				1.6	μs (max)

AC Electrical Characteristics

The following specifications apply for ($V^+ = V_A^+ = V_D^+ = +5V$, $V_{REF}^+ = +4.096V$, and fully-differential input with fixed 2.048V common-mode voltage) or ($V^+ = V_A^+ = V_D^+ = +3.3V$, $V_{REF}^+ = +2.5V$ and fully-differential input with fixed 1.250V common-mode voltage), $V_{REF}^- = 0V$, 12-bit + sign conversion mode, source impedance for analog inputs, V_{REF}^- and $V_{REF}^+ \leq 25\Omega$, $f_{CK} = f_{SK} = 5$ MHz, and 10 (t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Note 17) (Continued)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
t_{HPU}	Hardware Power-Up Time, Time from PD Falling Edge to EOC Rising Edge		500	**700**	μs (max)
t_{SPU}	Software Power-Up Time, Time from Serial Data Clock Falling Edge to EOC Rising Edge		500	**700**	μs (max)
t_{ACC}	Access Time Delay from $\overline{CS}$ Falling Edge to DO Data Valid		25	**60**	ns (max)
t_{SET-UP}	Set-Up Time of $\overline{CS}$ Falling Edge to Serial Data Clock Rising Edge			**50**	ns (min)
t_{DELAY}	Delay from SCLK Falling Edge to $\overline{CS}$ Falling Edge		0	**5**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{CS}$ Rising Edge to DO TRI-STATE®	$R_L = 3k$, $C_L = 100$ pF	70	**100**	ns (max)
t_{HDI}	DI Hold Time from Serial Data Clock Rising Edge		5	**15**	ns (min)
t_{SDI}	DI Set-Up Time from Serial Data Clock Rising Edge		5	**10**	ns (min)
t_{HDO}	DO Hold Time from Serial Data Clock Falling Edge	$R_L = 3k$, $C_L = 100$ pF	35	**65** **5**	ns (max) ns (min)
t_{DDO}	Delay from Serial Data Clock Falling Edge to DO Data Valid		50	**90**	ns (max)
t_{RDO}	DO Rise Time, TRI-STATE to High DO Rise Time, Low to High	$R_L = 3k$, $C_L = 100$ pF	10 10	**40** **40**	ns (max) ns (max)
t_{FDO}	DO Fall Time, TRI-STATE to Low DO Fall Time, High to Low	$R_L = 3k$, $C_L = 100$ pF	15 15	**40** **40**	ns (max) ns (max)
t_{CD}	Delay from $\overline{CS}$ Falling Edge to $\overline{DOR}$ Falling Edge		45	**80**	ns (max)
t_{SD}	Delay from Serial Data Clock Falling Edge to $\overline{DOR}$ Rising Edge		45	**80**	ns (max)
C_{IN}	Capacitance of Logic Inputs		10		pF
C_{OUT}	Capacitance of Logic Outputs		20		pF

AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > V_A^+$ or V_D^+), the current at that pin should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.

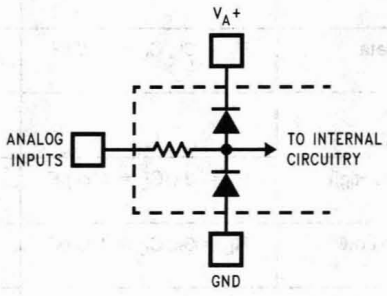
Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J max$, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J max - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_J max = 150°C$. The typical thermal resistance (Θ_{JA}) of these parts when board mounted follow:

Part Number	Thermal Resistance θ_{JA}
ADC12130CIN	53°C/W
ADC12130CIWM	70°C/W
ADC12132CIMSA	134°C/W
ADC12138CIN	40°C/W
ADC12138CIWM	50°C/W
ADC12138CIMSA	125°C/W

Note 5: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A^+ or 5V below GND will not damage this device. However, errors in the A/D conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A^+ or below GND by more than 50 mV. As an example, if V_A^+ is 4.5 V_{DC}, full-scale input voltage must be ≤4.55 V_{DC} to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that the V_A^+ and V_D^+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.

Note 9: With the test condition for V_{REF} ($V_{REF}^+ - V_{REF}^-$) given as +4.096V, the 12-bit LSB is 1.0 mV. For V_{REF} = 2.5V, the 12-bit LSB is 610 μV.

Note 10: Typicals are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero (see *Figures 1b* and *1c*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the average value of the code transitions between −1 to 0 and 0 to +1 (see *Figure 2*).

Note 14: Total unadjusted error includes offset, full-scale, linearity and multiplexer errors.

Note 15: The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.

Note 16: Channel leakage current is measured after the channel selection.

Note 17: Timing specifications are tested at the TTL logic levels, $V_{OL} = 0.4V$ for a falling edge and $V_{OL} = 2.4V$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 18: The ADC12130 family's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a maximum repeatability uncertainty of 0.2 LSB.

Note 19: If SCLK and CCLK are driven from the same clock source, then t_A is 6, 10, 18 or 34 clock periods minimum and maximum.

Note 20: The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

AC Electrical Characteristics (Continued)

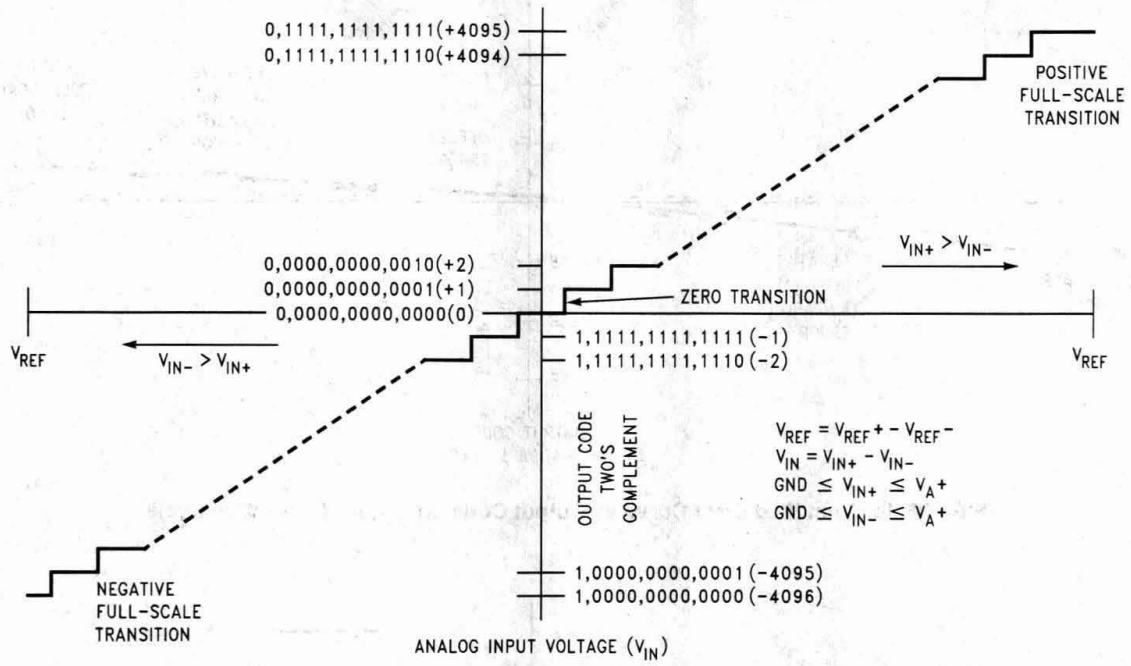

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FIGURE 1a. Transfer Characteristic

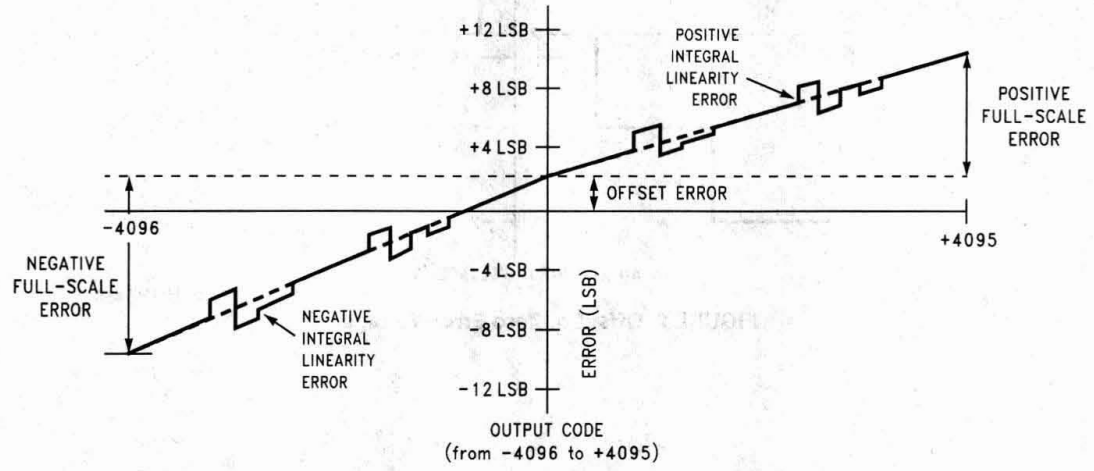

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles

AC Electrical Characteristics (Continued)

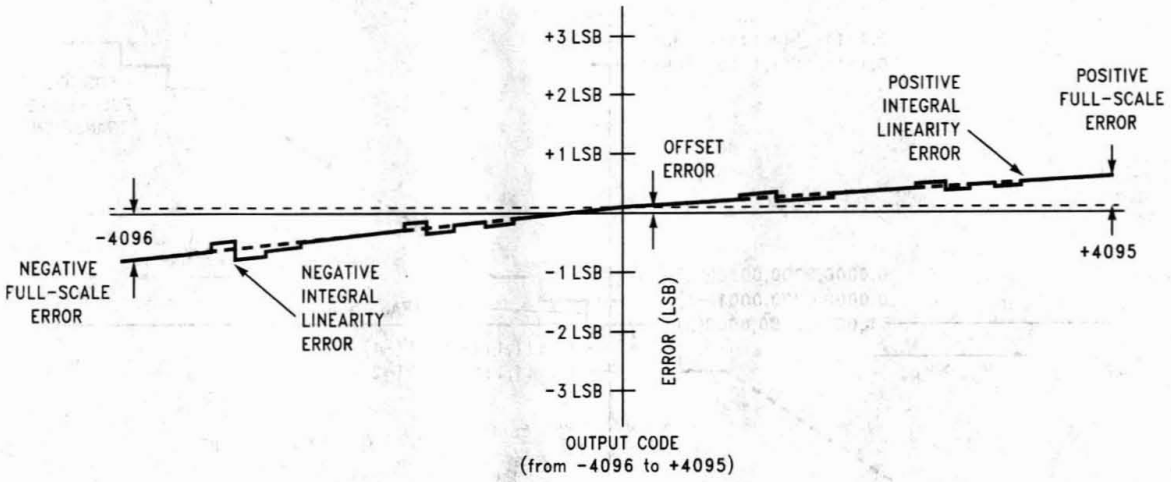

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FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

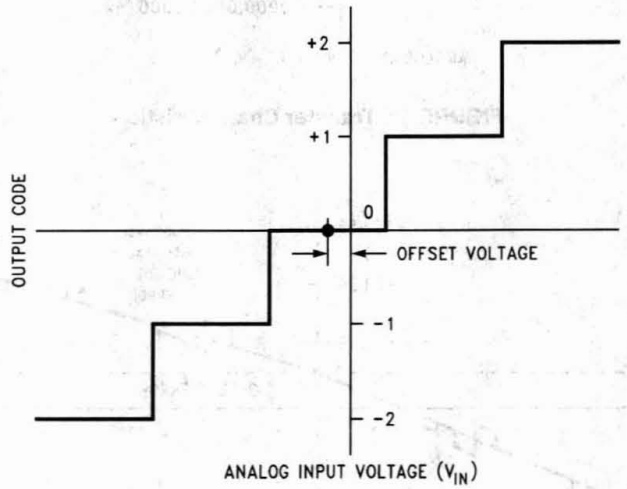

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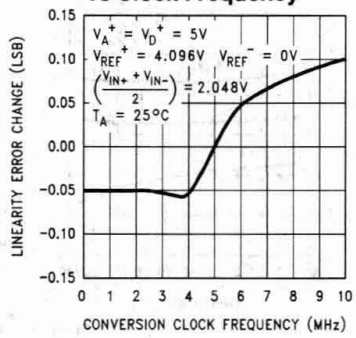
FIGURE 2. Offset or Zero Error Voltage

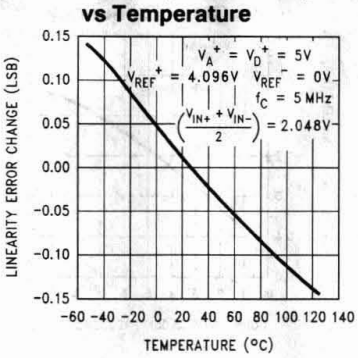
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

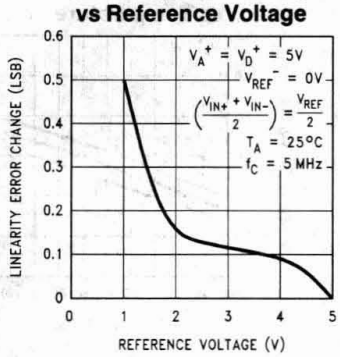
Linearity Error Change vs Clock Frequency


$V_A^+ = V_D^+ = 5V$
$V_{REF}^+ = 4.096V$ $V_{REF}^- = 0V$
$\left(\frac{V_{IN+} + V_{IN-}}{2}\right) = 2.048V$
$T_A = 25°C$
LINEARITY ERROR CHANGE (LSB)
CONVERSION CLOCK FREQUENCY (MHz)

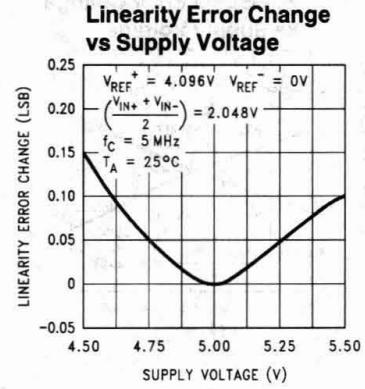
Linearity Error Change vs Temperature



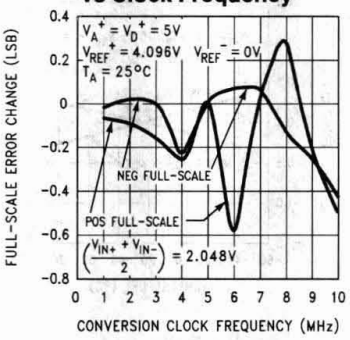
Linearity Error Change vs Reference Voltage



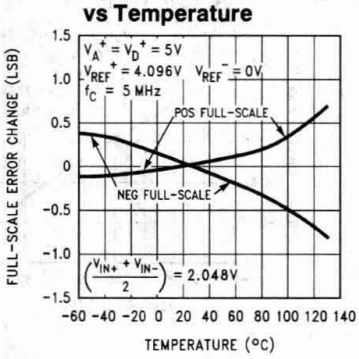
Linearity Error Change vs Supply Voltage



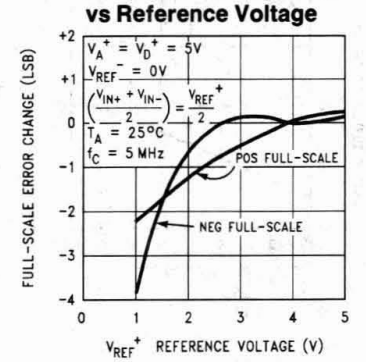
Full-Scale Error Change vs Clock Frequency



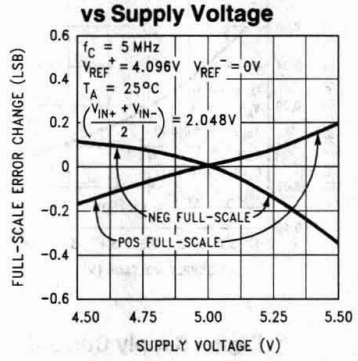
Full-Scale Error Change vs Temperature



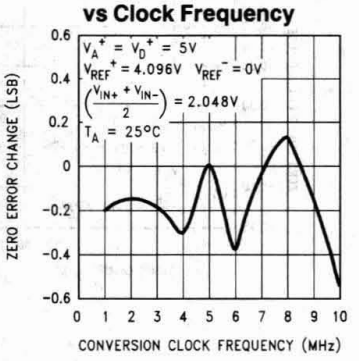
Full-Scale Error Change vs Reference Voltage



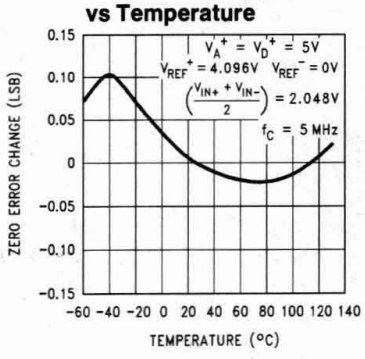
Full-Scale Error Change vs Supply Voltage



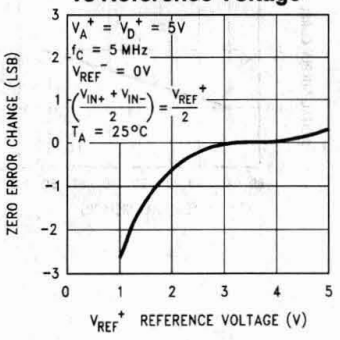
Zero Error Change vs Clock Frequency



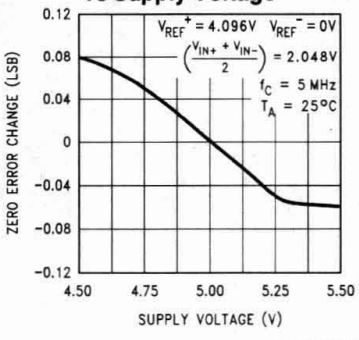
Zero Error Change vs Temperature



Zero Error Change vs Reference Voltage



Zero Error Change vs Supply Voltage



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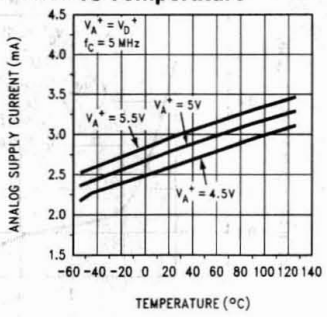
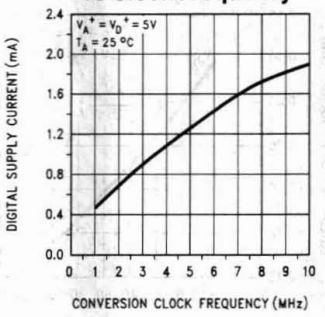
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

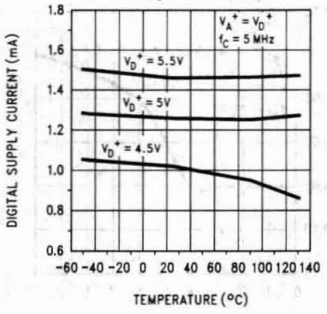
Analog Supply Current vs Temperature



Digital Supply Current vs Clock Frequency



Digital Supply Current vs Temperature



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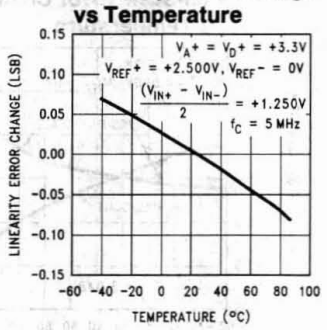
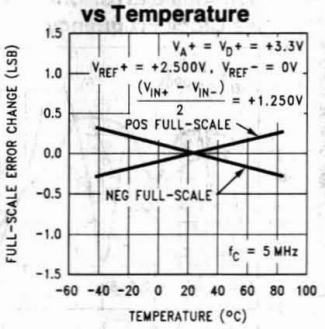
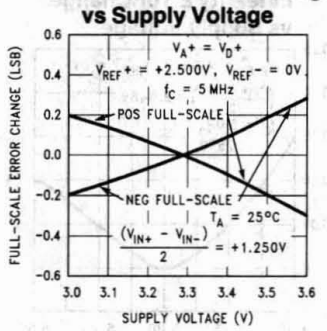
Linearity Error Change vs Temperature



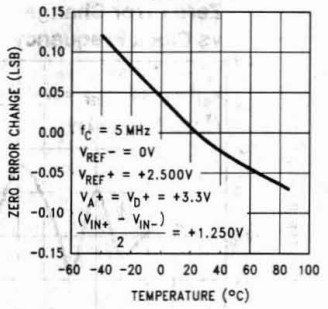
Full-Scale Error Change vs Temperature



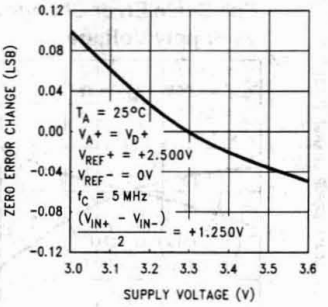
Full-Scale Error Change vs Supply Voltage



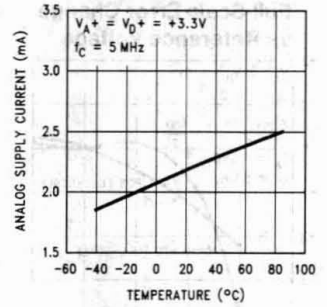
Zero Error Change vs Temperature



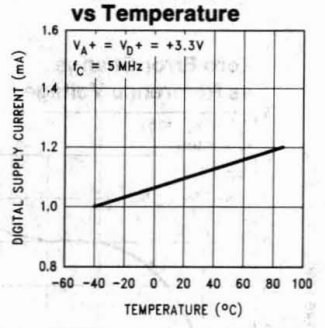
Zero Error Change vs Supply Voltage



Analog Supply Current vs Temperature



Digital Supply Current vs Temperature



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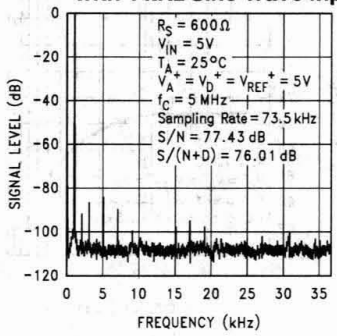
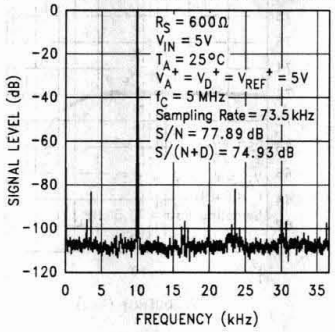
Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

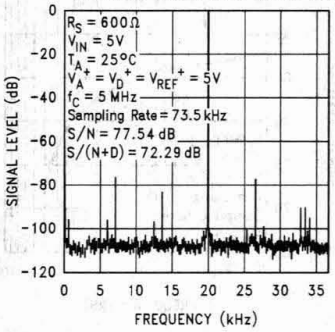
Bipolar Spectral Response with 1 kHz Sine Wave Input



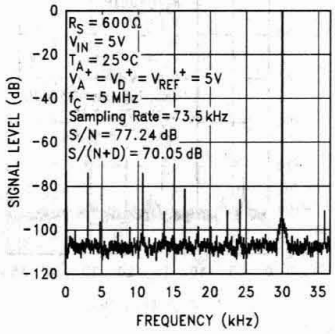
Bipolar Spectral Response with 10 kHz Sine Wave Input



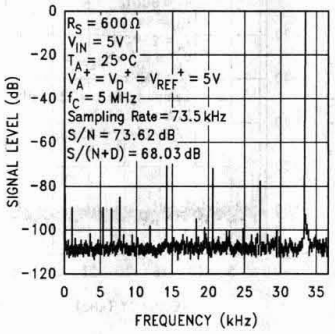
Bipolar Spectral Response with 20 kHz Sine Wave Input



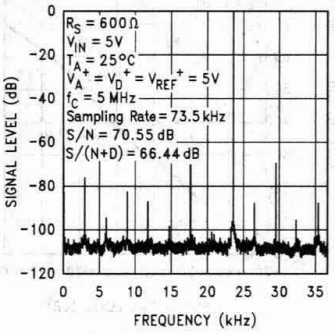
Bipolar Spectral Response with 30 kHz Sine Wave Input



Bipolar Spectral Response with 40 kHz Sine Wave Input



Bipolar Spectral Response with 50 kHz Sine Wave Input



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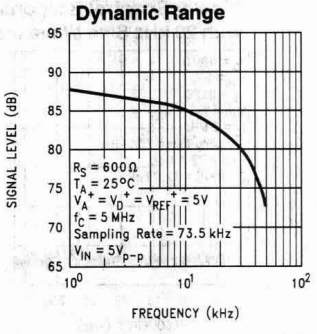
2

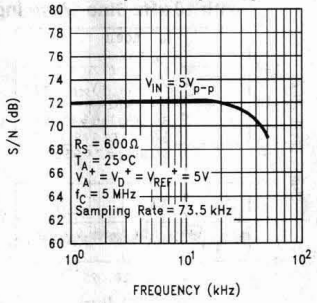
Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

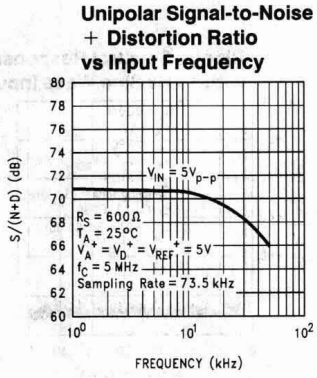
Bipolar Spurious Free Dynamic Range



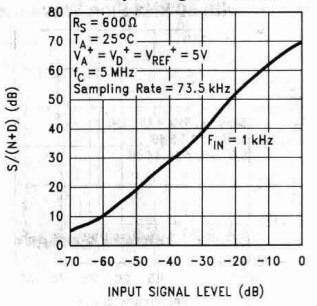
Unipolar Signal-to-Noise Ratio vs Input Frequency



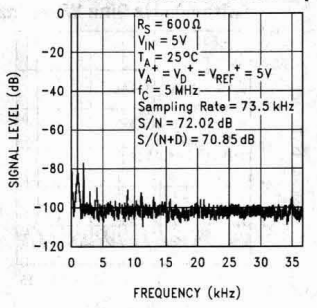
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



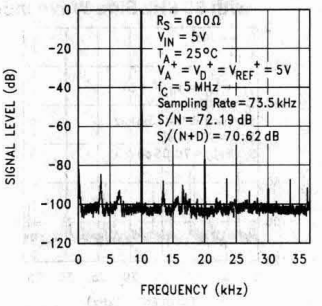
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



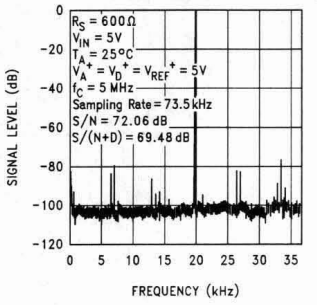
Unipolar Spectral Response with 1 kHz Sine Wave Input



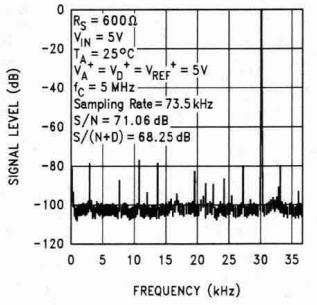
Unipolar Spectral Response with 10 kHz Sine Wave Input



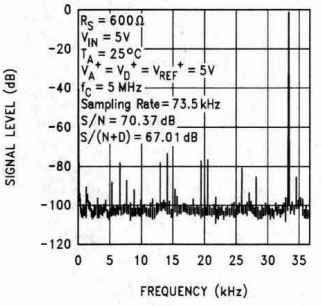
Unipolar Spectral Response with 20 kHz Sine Wave Input



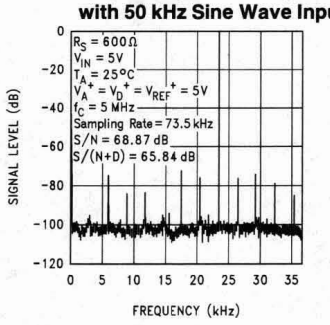
Unipolar Spectral Response with 30 kHz Sine Wave Input



Unipolar Spectral Response with 40 kHz Sine Wave Input



Unipolar Spectral Response with 50 kHz Sine Wave Input



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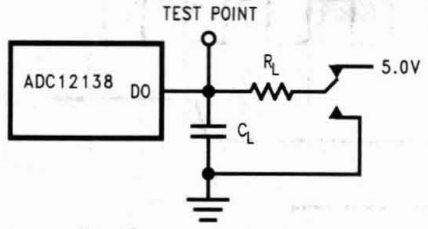
Test Circuits

DO "TRI-STATE" (t_{1H}, t_{0H})



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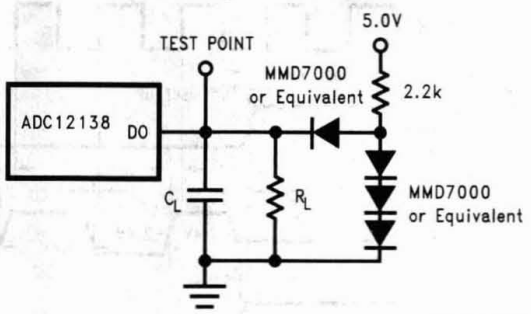
DO except "TRI-STATE"



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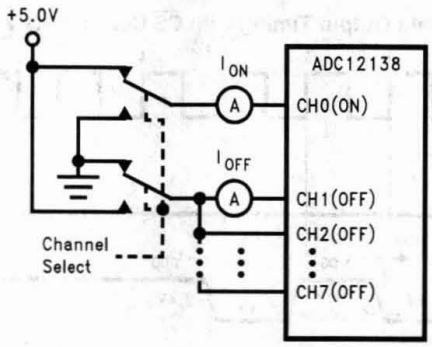
Leakage Current



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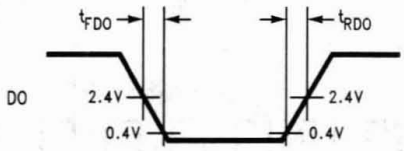
Timing Diagrams

DO Falling and Rising Edge



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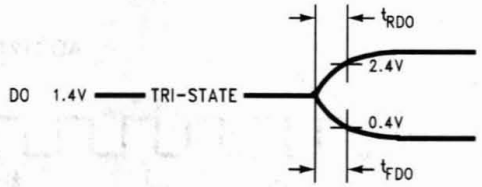
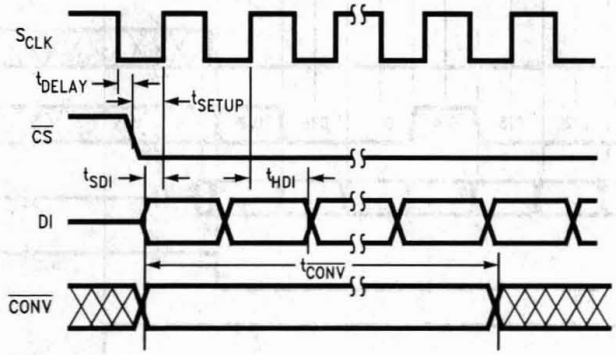
DO "TRI-STATE" Falling and Rising Edge



TL/H/12079–17

DI Data Input Timing



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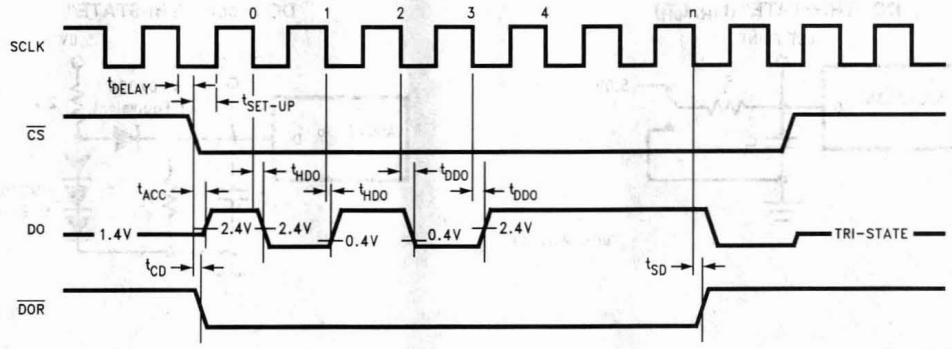
Timing Diagrams (Continued)

DO Data Output Timing Using $\overline{CS}$



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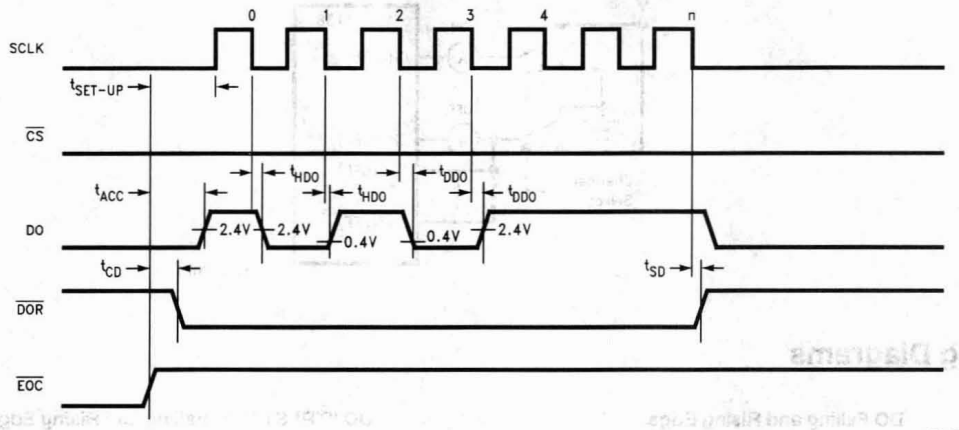
DO Data Output Timing with $\overline{CS}$ Continuously Low



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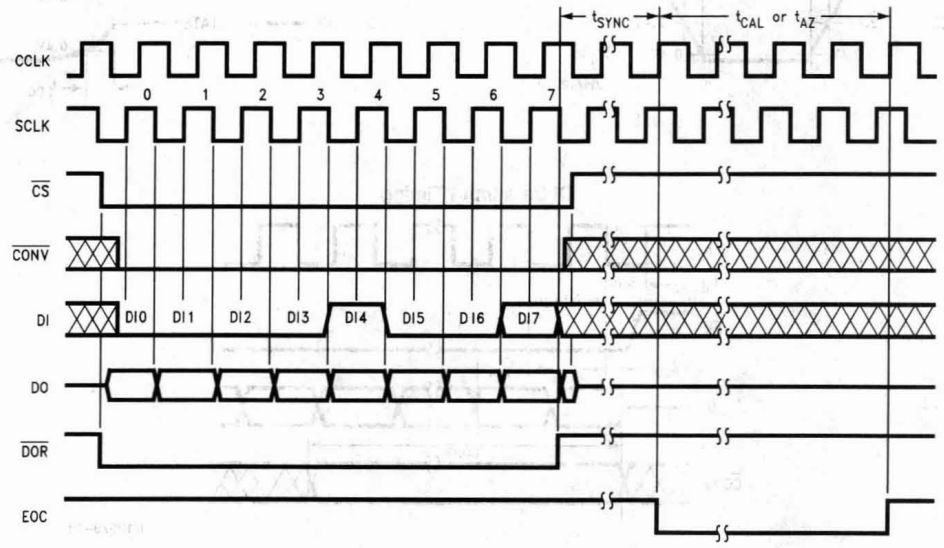
ADC12138 Auto Cal or Auto Zero



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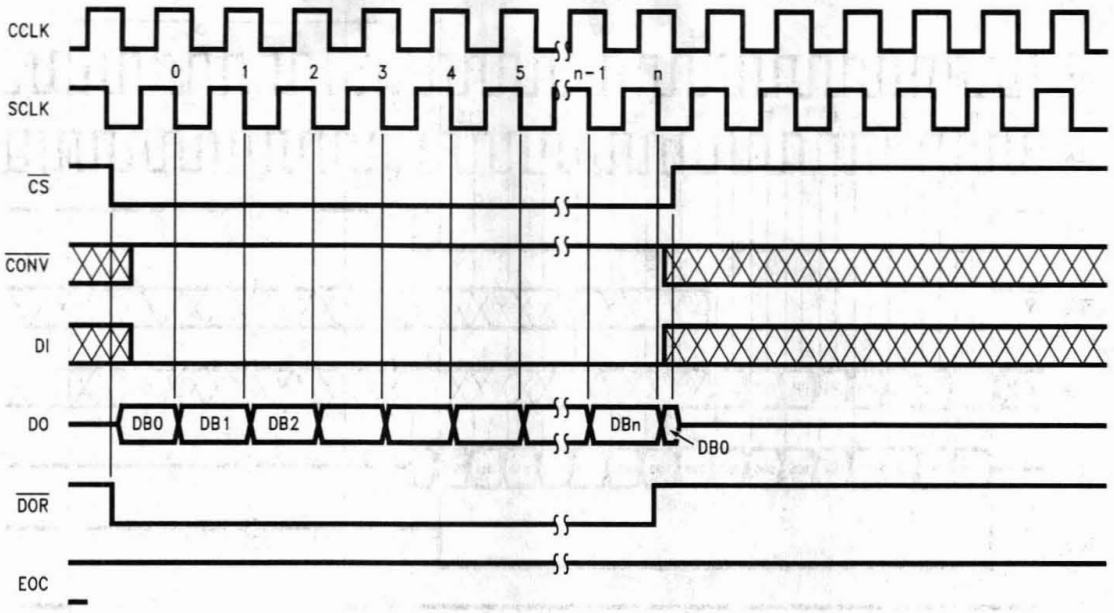
Note: DO output data is not valid during this cycle.

Timing Diagrams (Continued)

ADC12138 Read Data without Starting a Conversion Using $\overline{CS}$



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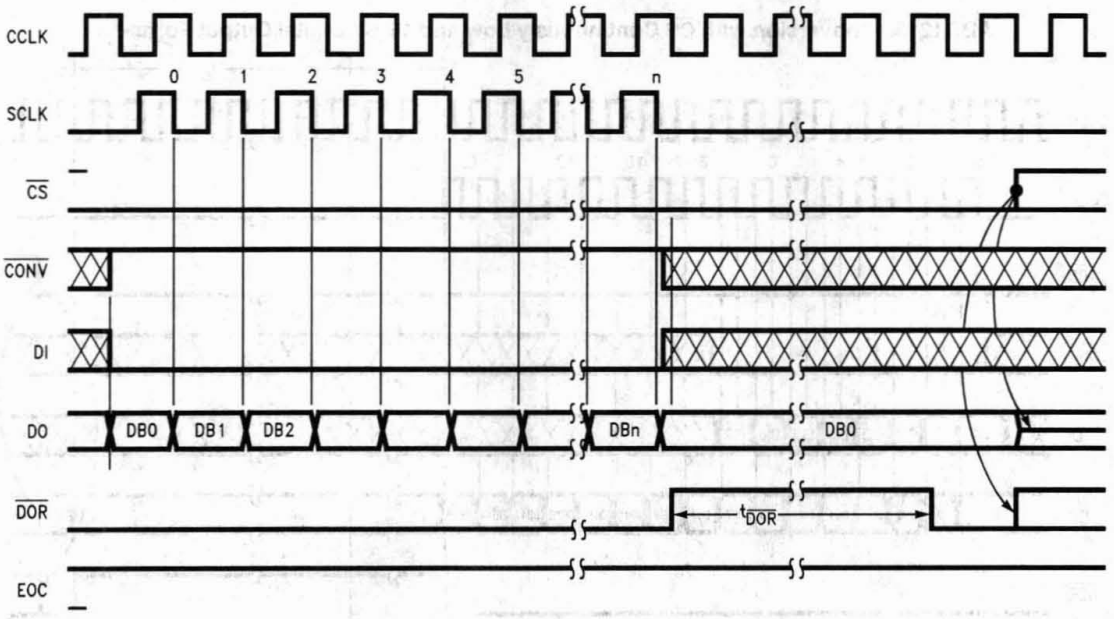
ADC12138 Read Data without Starting a Conversion with $\overline{CS}$ Continuously Low



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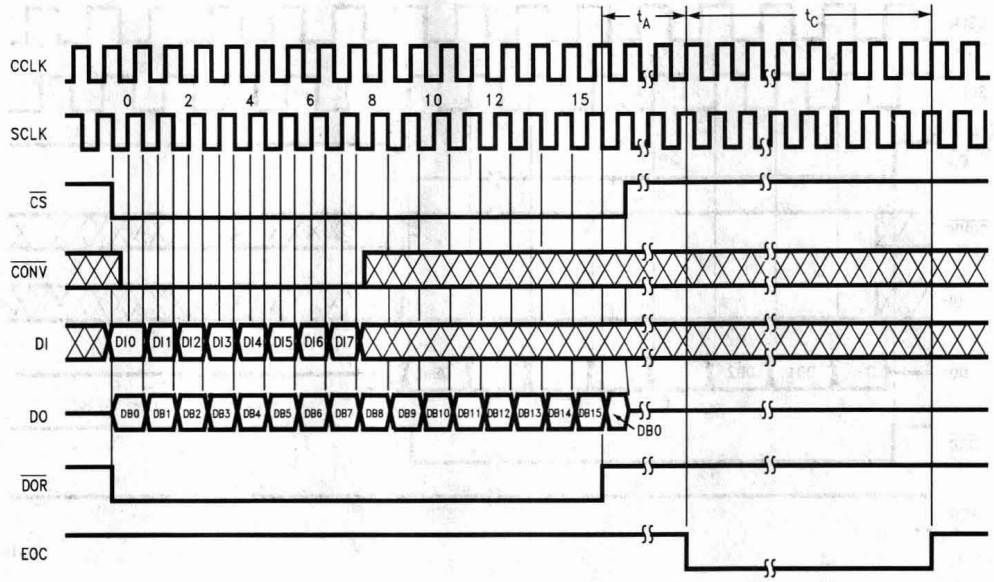
Timing Diagrams (Continued)

ADC12138 Conversion Using $\overline{CS}$ with 16-Bit Digital Output Format



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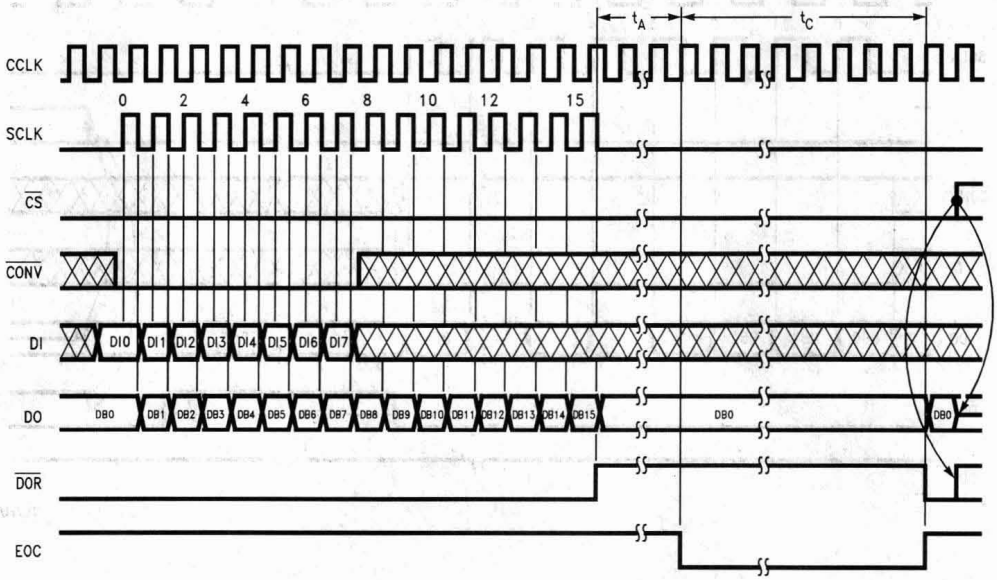
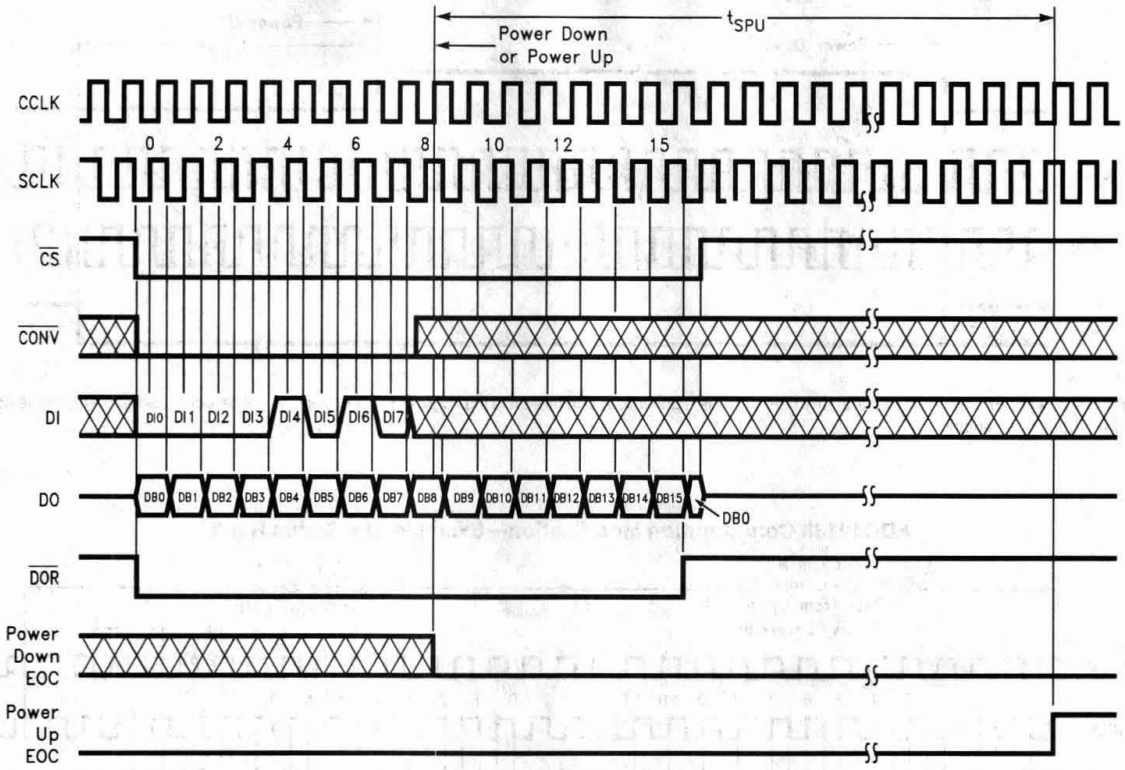
ADC12138 Conversion with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



TL/H/12079–25

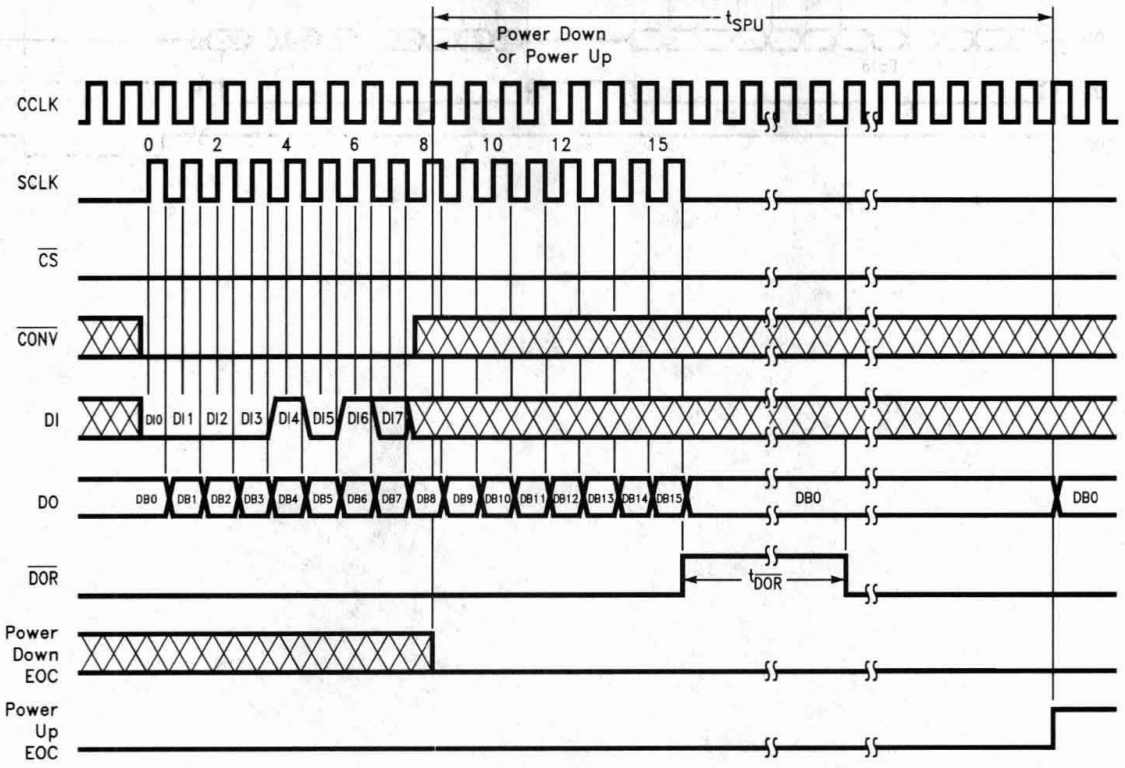
Timing Diagrams (Continued)

ADC12138 Software Power Up/Down Using $\overline{CS}$ with 16-Bit Digital Output Format



TL/H/12079–26

ADC12138 Software Power Up/Down with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format



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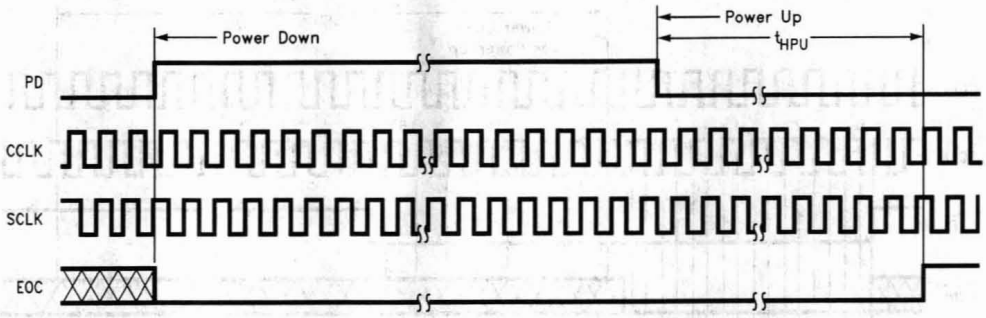
Timing Diagrams (Continued)

ADC12138 Hardware Power Up/Down



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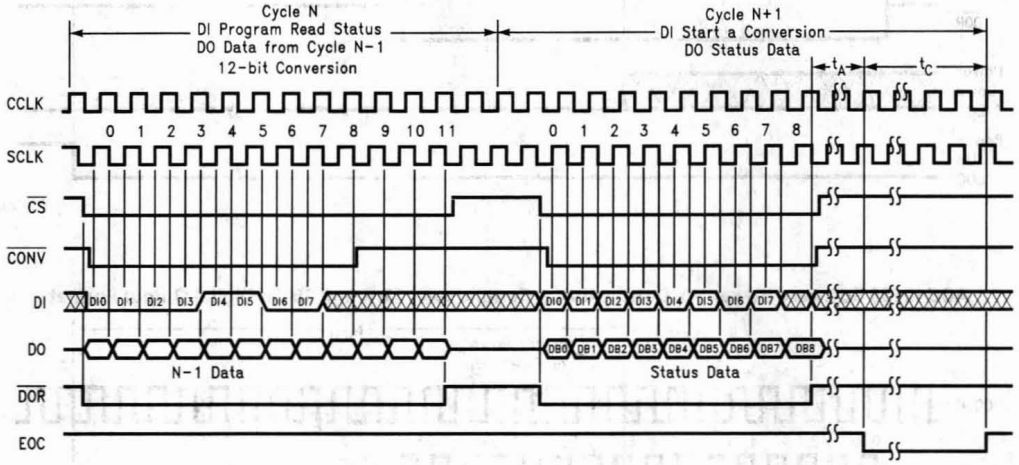
Note: Hardware power up/down may occur at any time. If PD is high while a conversion is in progress that conversion will be corrupted and erroneous data will be stored in the output shift register.

ADC12138 Configuration Modification—Example of a Status Read



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Pin Descriptions

CCLK The clock applied to this input controls the sucessive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 μs.

SCLK This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{CS}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled, the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 μs.

DI This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. Tables II through IV show the assignment of the multiplexer address and the mode select data.

DO The data output pin. This pin is an active push/pull output when $\overline{CS}$ is low. When $\overline{CS}$ is high, this output is TRI-STATE. The A/D conversion result (DB0–DB12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see Table I). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see Table IV).

EOC This pin is an active push/pull output and indicates the status of the ADC12130/2/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{CS}$ This is the chip select pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE. With $\overline{CS}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled, the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought back low during a conversion, that conversion is prematurely terminated. The data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought back low during a conversion in progress the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. Table IV details the data required.

$\overline{DOR}$ This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{CONV}$ A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming Table (Table IV) such as 12-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.

PD This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 700 μs to power up after the command is given.

CH0–CH7 These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (see Tables II and III).

The voltage applied to these inputs should not exceed V_A^+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2 These are the multiplexer output pins.

A/DIN1, A/DIN2 These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_A^+ or go below AGND (see *Figure 3*).

V_{REF}^+ This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range of V_{REF} ($V_{REF} = V_{REF}^+ - V_{REF}^-$) is 1 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF}^+ cannot exceed V_A^+. See *Figure 4* for recommended bypassing.

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Pin Descriptions (Continued)

V_{REF}^- The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND or exceed V_A^+. (See *Figure 4*).

V_A^+, V_D^+ These are the analog and digital power supply pins. V_A^+ and V_D^+ are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see *Figure 4*). The operating voltage range of V_A^+ and V_D^+ is 3.0 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin (see *Figure 4*).

AGND This is the analog ground pin (see *Figure 4*).

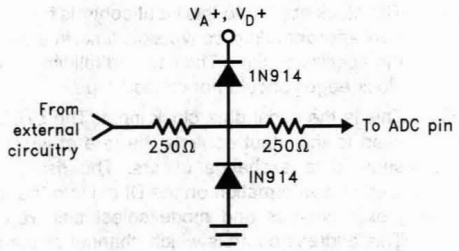

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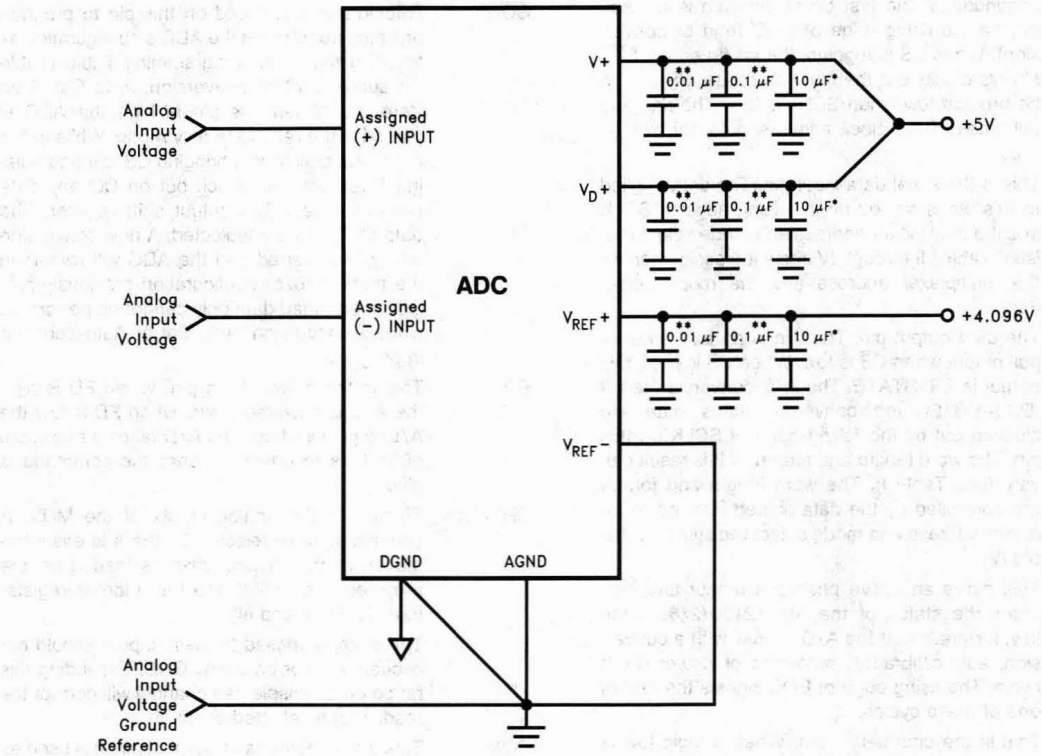
FIGURE 3. Protecting the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 Analog Pins



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*Tantalum

**Monolithic Ceramic or better

FIGURE 4. Recommended Power Supply Bypassing and Grounding

Tables

TABLE I. Data Out Formats

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	MSB First	17 Bits	X	X	X	X	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	X	X	X	X
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					

X = High or Low state.

TABLE II. ADC12138 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	DI3	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	−								+	−	CH0	CH1	Differential
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	Single-Ended
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

2

Tables (Continued)

TABLE III. ADC12130 and ADC12132 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-Ended
H	H		+	−	+	−	CH1	COM	

Note: ADC12130 do not have A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 pins.

TABLE IV. Mode Programming

ADC12138	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Selected (Current)	DO Format (next Conversion Cycle)
ADC12130 and ADC12132	DI0	DI1			DI2	DI3	DI4	DI5		
	See Tables II or III				L	L	L	L	12 Bit Conversion	12 or 13 Bit MSB First
	See Tables II or III				L	L	L	H	12 Bit Conversion	16 or 17 Bit MSB First
	See Tables II or III				L	H	L	L	12 Bit Conversion	12 or 13 Bit LSB First
	See Tables II or III				L	H	L	H	12 Bit Conversion	16 or 17 Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register (LSB First)	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—6 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—10 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—18 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—34 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	X	X	X	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

Note: The A/D powers up with no Auto Cal, no Auto Zero, 10 CCLK acquisition time, 12-bit + sign conversion, power up, 12- or 13-bit MSB First, and user mode.
X = Don't Care

TABLE V. Conversion/Read Data Only Mode Programming

$\overline{CS}$	$\overline{CONV}$	PD	Mode
L	L	L	See Table IV for Mode
L	H	L	Read Only (Previous DO Format). No Conversion.
H	X	L	Idle
X	X	H	Power Down

X = Don't Care

Tables (Continued)

TABLE VI. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	PU	PD	Cal		12 or 13	16 or 17	Sign	Justification	Test Mode
	Device Status			DO Output Format Status					
Function	"High" indicates a Power Up Sequence is in progress	"High" indicates a Power Down Sequence is in progress	"High" indicates an Auto-Cal Sequence is in progress	Not used	"High" indicates a 12 or 13 bit format	"High" indicates a 16 or 17 bit format	"High" indicates that the sign bit is included. When "Low" the sign bit is not included.	When "High" the conversion result will be output MSB first. When "Low" the result will be output LSB first.	When "High" the device is in test mode. When "Low" the device is in user mode.

Application Hints

1.0 DIGITAL INTERFACE

1.1 Interface Concepts

The example in *Figure 5* shows a typical sequence of events after the power is applied to the ADC12130/2/8:

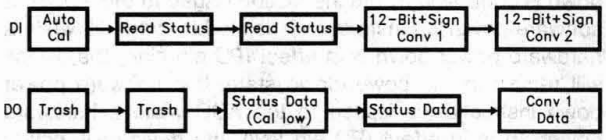

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FIGURE 5. Typical Power Supply Power Up Sequence

The first instruction input to the A/D via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To determine whether the Auto Cal has been completed, a read status instruction is issued to the A/D. Again the data output at that time has no significance since the Auto Cal procedure modifies the data in the output shift register. To retrieve the status information, an additional read status instruction is issued to the A/D. At this time the status data is available on DO. If the Cal signal in the status word, is low Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output at this time is again status information. To keep noise from corrupting the A/D conversion, status can not be read during a conversion. If $\overline{CS}$ is strobed and is brought low during a conversion, that conversion is prematurely ended. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to comnmunicate to the A/D again. Once it has been determined that the A/D has completed a conversion, another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

Note, when $\overline{CS}$ is low continuously it is important to transmit the exact number of SCLK cycles, as shown in the timing diagrams. The Data Out Format sets the number of SCLK cycles required in the next I/O cycle. A 12-bit no sign format will require 12 SCLKs to be transmitted; a 12-bit plus sign format will require 13 SCLKs to be transmitted, etc. Not doing so will desynchronize the serial communication to the A/D. (See Section 1.3.)

1.2 Changing Configuration

The configuration of the ADC12130/2/8 on power up defaults to 12-bit plus sign resolution, 12- or 13-bit MSB First, 10 CCLK acquisition time, user mode, no Auto Cal, no Auto Zero, and power up mode. Changing the acquisition time and turning the sign bit on and off requires an 8-bit instruction to be issued to the ADC. This instruction will not start a conversion. The instructions that select a multiplexer address and format the output data do start a conversion. *Figure 6* describes an example of changing the configuration of the ADC12130/2/8.

During I/O sequence 1, the instruction on DI configures the ADC12130/2/8 to do a conversion with 12-bit + sign resolution. Notice that when the 6 CCLK Acquisition and Data Out without Sign instructions are issued to the ADC, I/O sequences 2 and 3, a new conversion is not started. The data output during these instructions is from conversion N which was started during I/O sequence 1. The Configuration Modification timing diagram describes in detail the sequence of events necessary for a Data Out without Sign, Data Out with Sign, or 6/10/18/34 CCLK Acquisition time mode selection. Table IV describes the actual data necessary to be input to the ADC to accomplish this configuration modification. The next instruction, shown in *Figure 6*, issued to the A/D starts conversion N + 1 with 16-bit format with 12 bits of resolution formatted MSB first. Again the data output during this I/O cycle is the data from conversion N.

The number of SCLKs applied to the A/D during any conversion I/O sequence should vary in accord with the data out word format chosen during the previous conversion I/O sequence. The various formats and resolutions available are shown in Table I. In *Figure 6*, since 16-bit without sign MSB first format was chosen during I/O sequence 4, the number of SCLKs required during I/O sequence 5 is 16. In the following I/O sequence the format changes to 12-bit without sign MSB first; therefore the number of SCLKs required during I/O sequence 6 changes accordingly to 12.

1.3 $\overline{CS}$ Low Continuously Considerations

When $\overline{CS}$ is continuously low, it is important to transmit the exact number of SCLK pulses that the ADC expects. Not doing so will desynchronize the serial communications to the ADC. When the supply power is first applied to the ADC,

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Application Hints (Continued)

it will expect to see 13 SCLK pulses for each I/O transmission. The number of SCLK pulses that the ADC expects to see is the same as the digital output word length. The digital output word length is controlled by the Data Out (DO) format. The DO format maybe changed any time a conversion is started or when the sign bit is turned on or off. The table below details out the number of clock periods required for different DO formats:

DO Format		Number of SCLKs Expected
12-Bit MSB or LSB First	SIGN OFF	12
	SIGN ON	13
16-Bit MSB or LSB first	SIGN OFF	16
	SIGN ON	17

If erroneous SCLK pulses desynchronize the communications, the simplest way to recover is by cycling the power supply to the device. Not being able to easily resynchronize the device is a shortcoming of leaving $\overline{CS}$ low continuously.

The number of clock pulses required for an I/O exchange may be different for the case when $\overline{CS}$ is left low continuously vs the case when $\overline{CS}$ is cycled. Take the I/O sequence detailed in *Figure 5* (Typical Power Supply Sequence) as an example. The table below lists the number of SCLK pulses required for each instruction:

Instruction	$\overline{CS}$ Low Continuously	$\overline{CS}$ Strobed
Auto Cal	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 1	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 2	13 SCLKs	13 SCLKs

1.4 Analog Input Channel Selection

The data input on DI also selects the channel configuration for a particular A/D conversion (see Tables II, III and IV).

In *Figure 6* the only times when the channel configuration could be modified would be during I/O sequences 1, 4, 5 and 6. Input channels are reselected before the start of each new conversion. Shown below is the data bit stream required on DI, during I/O sequence number 4 in *Figure 6*, to set CH1 as the positive input and CH0 as the negative input for the different versions of ADCs:

Part Number	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
ADC12130 and ADC12132	L	H	L	L	H	L	X	X
ADC12138	L	H	L	L	L	L	H	L

Where X can be a logic high (H) or low (L).

1.5 Power Up/Down

The ADC may be powered down at any time by taking the PD pin HIGH or by the instruction input on DI (see Tables IV and V, and the Power Up/Down timing diagrams). When the ADC is powered down in this way, the circuitry necessary for an A/D conversion is deactivated. The circuitry necessary for digital I/O is kept active. Hardware power up/down is controlled by the state of the PD pin. Software power-up/down is controlled by the instruction issued to the ADC. If a software power up instruction is issued to the ADC while a hardware power down is in effect (PD pin high) the device will remain in the power-down state. If a software power down instruction is issued to the ADC while a hardware power up is in effect (PD pin low), the device will power down. When the device is powered down by software, it may be powered up by either issuing a software power up instruction or by taking PD pin high and then low. If the power down command is issued during an A/D conversion, that conversion is disrupted. Therefore, the data output after power up cannot be relied upon.

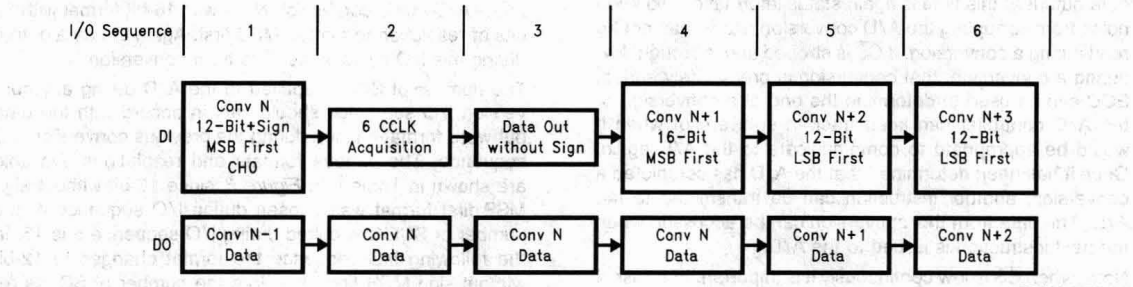

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FIGURE 6. Changing the ADC's Conversion Configuration

Application Hints (Continued)

1.6 User Mode and Test Mode

An instruction may be issued to the ADC to put it into test mode. Test mode is used by the manufacturer to verify complete functionality of the device. During test mode CH0–CH7 become active outputs. If the device is inadvertently put into the test mode with $\overline{CS}$ continuously low, the serial communications may be desynchronized. Synchronization may be regained by cycling the power supply voltage to the device. Cycling the power supply voltage will also set the device into user mode. If $\overline{CS}$ is used in the serial interface, the ADC may be queried to see what mode it is in. This is done by issuing a "read STATUS register" instruction to the ADC. When bit 9 of the status register is high, the ADC is in test mode; when bit 9 is low the ADC, is in user mode. As an alternative to cycling the power supply, an instruction sequence may be used to return the device to user mode. This instruction sequence must be issued to the ADC using $\overline{CS}$. The following table lists the instructions required to return the device to user mode:

Instruction	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
TEST MODE	H	X	X	X	H	H	H	H
Reset Test Mode Instructions	L	L	L	L	H	H	H	L
	L	L	L	L	H	L	H	L
	L	L	L	L	H	L	H	H
USER MODE	L	L	L	L	H	H	H	H
Power Up	L	L	L	L	H	L	H	L
Set DO with or without Sign	H or L	L	L	L	H	H	L	H
Set Acquisition Time	H or L	H or L	L	L	H	H	H	L
Start a Conversion	H or L	H or L	H or L	H or L	L	H or L	H or L	H or L

X = Don't Care

After returning to user mode with the user mode instruction the power up, data with or without sign, and acquisition time instructions need to be resent to ensure that the ADC is in the required state before a conversion is started.

1.7 Reading the Data Without Starting a Conversion

The data from a particular conversion may be accessed without starting a new conversion by ensuring that the $\overline{CONV}$ line is taken high during the I/O sequence. See the Read Data timing diagrams. Table V describes the operation of the $\overline{CONV}$ pin.

2.0 DESCRIPTION OF THE ANALOG MULTIPLEXER

For the ADC12138, the analog input multiplexer can be configured with 4 differential channels or 8 single ended channels with the COM input as the zero reference or any combination thereof (see *Figure 7*). The difference between the voltages on the V_{REF}^+ and V_{REF}^- pins determines the input voltage span (V_{REF}). The analog input voltage range is 0 to V_A^+. Negative digital output codes result when $V_{IN}^- > V_{IN}^+$. The actual voltage at V_{IN}^- or V_{IN}^+ cannot go below AGND.

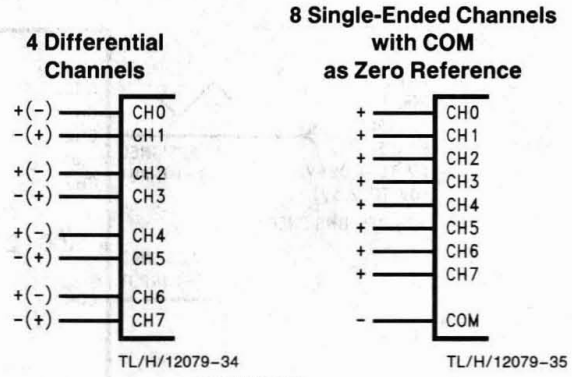

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FIGURE 7

CH0, CH2, CH4, and CH6 can be assigned to the MUXOUT1 pin in the differential configuration, while CH1, CH3, CH5, and CH7 can be assigned to the MUXOUT2 pin. In the differential configuration, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The A/DIN1 and A/DIN2 pins can be assigned positive or negative polarity.

2

Application Hints (Continued)

With the single-ended multiplexer configuration CH0 through CH7 can be assigned to the MUXOUT1 pin. The COM pin is always assigned to the MUXOUT2 pin. A/DIN1 is assigned as the positve input; A/DIN2 is assigned as the negative input. (See *Figure 8*).

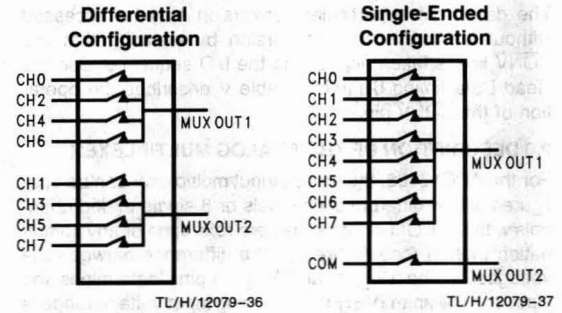

FIGURE 8

The Multiplexer assignment tables for the ADC12130/2/8 (Tables II and III) summarize the aforementioned functions for the different versions of A/Ds.

2.1 Biasing for Various Multiplexer Configurations

Figure 9 is an example of biasing the device for single-ended operation. The sign bit is always low. The digital output range is 0 0000 0000 0000 to 0 1111 1111 1111. One LSB is equal to 1 mV (4.1V/4096 LSBs).

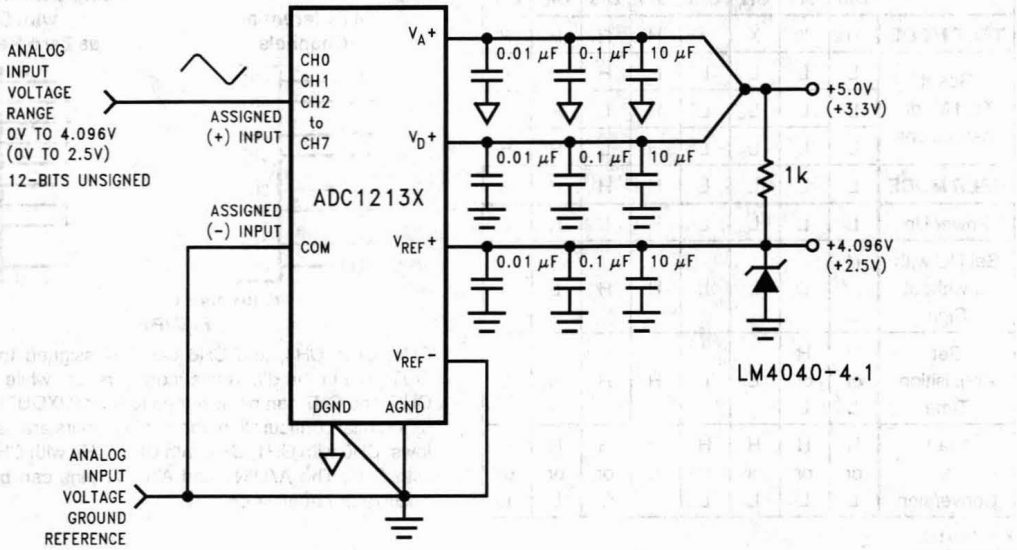

FIGURE 9. Single-Ended Biasing

Application Hints (Continued)

For pseudo-differential signed operation, the biasing circuit shown in *Figure 10* shows a signal AC coupled to the ADC. This gives a digital output range of −4096 to +4095. With a 2.5V reference, as shown, 1 LSB is equal to 610 μV. Although, the ADC is not production tested with a 2.5V reference, when V_A^+ and V_D^+ are +5.0V linearity error typically will not change more than 0.1 LSB (see the curves in the Typical Electrical Characteristics Section). With the ADC set to an acquisition time of 10 clock periods, the input biasing resistor needs to be 600Ω or less. Notice though that the input coupling capacitor needs to be made fairly large to bring down the high pass corner. Increasing the acquisition time to 34 clock periods (with a 5 MHz CCLK frequency) would allow the 600Ω to increase to 6k, which with a 1 μF coupling capacitor would set the high pass corner at 26 Hz. Increasing R, to 6k would allow R_2 to be 2k.

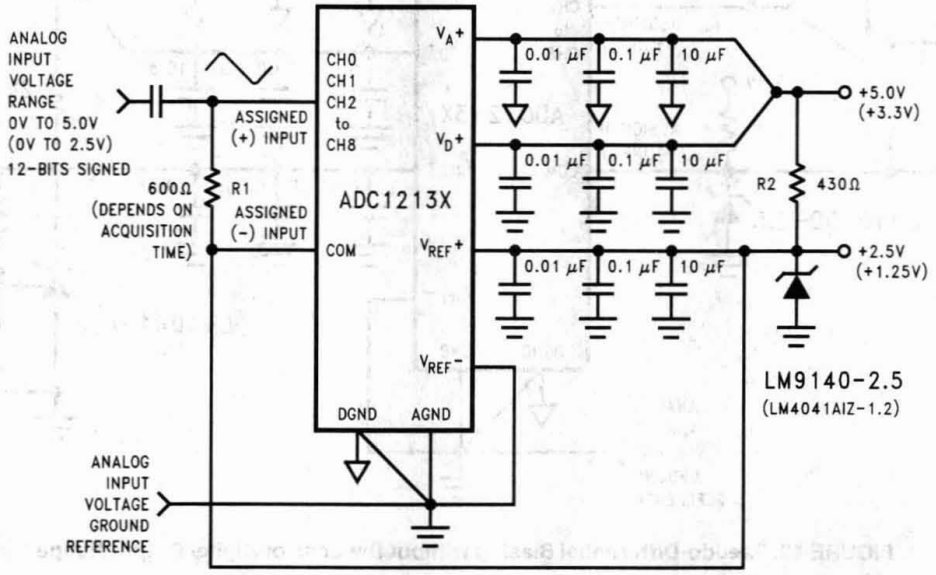

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FIGURE 10. Pseudo-Differential Biasing with the Signal Source AC Coupled Directly into the ADC

An alternative method for biasing pseudo-differential operation is to use the +2.5V from the LM9140 to bias any amplifier circuits driving the ADC as shown in *Figure 11*. The value of the resistor pull-up biasing the LM9140-2.5 will depend upon the current required by the op amp biasing circuitry.

In the circuit of *Figure 11* some voltage range is lost since the amplifier will not be able to swing to +5V and GND with a single +5V supply. Using an adjustable version of the LM4041 to set the full scale voltage at exactly 2.048V and a lower grade LM4040D-2.5 to bias up everything to 2.5V as shown in *Figure 12* will allow the use of all the ADC's digital output range of −4096 to +4095 while leaving plenty of head room for the amplifier.

Fully differential operation is shown in *Figure 13*. One LSB for this case is equal to (4.1V/4096) = 1 mV.

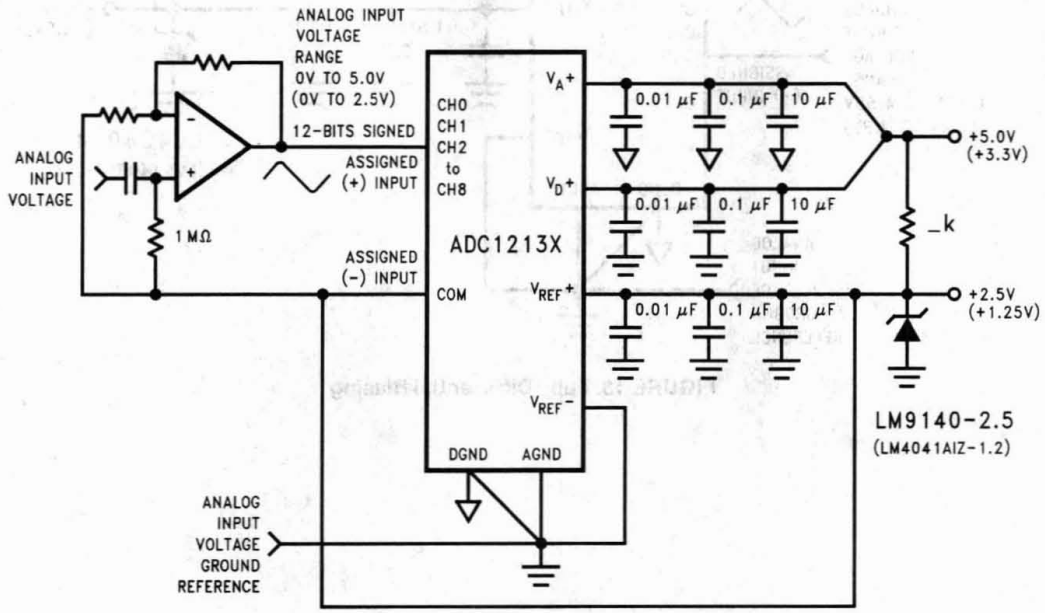

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FIGURE 11. Alternative Pseudo-Differential Biasing

Application Hints (Continued)

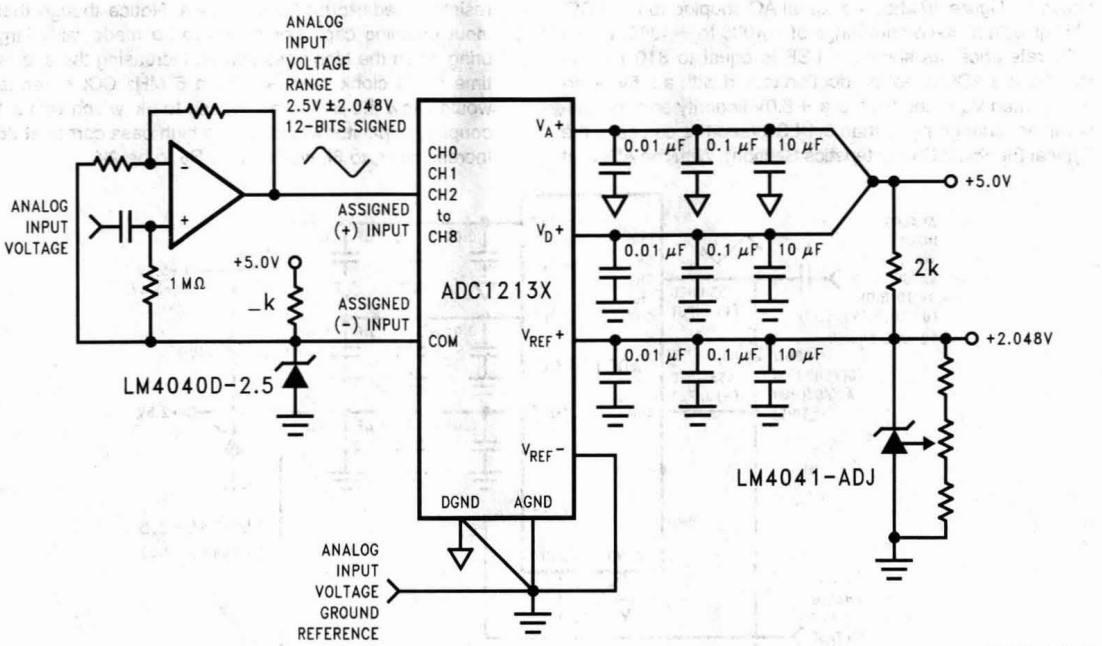

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FIGURE 12. Pseudo-Differential Biasing without the Loss of Digital Output Range

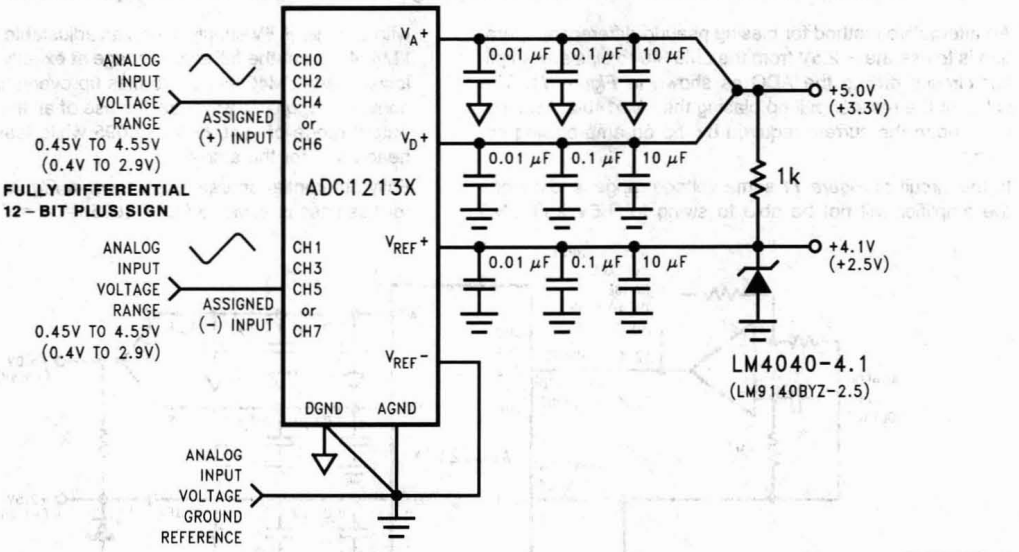

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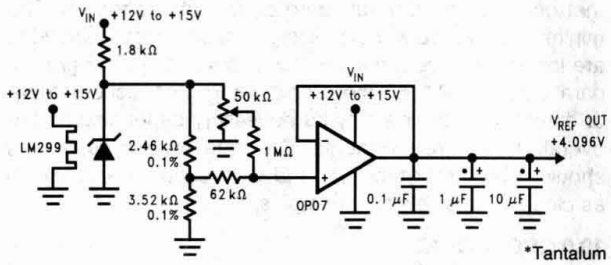
FIGURE 13. Fully Differential Biasing

Application Hints (Continued)

3.0 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF}^+ and V_{REF}^- defines the analog input span (the difference between the voltage applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF}^+ or V_{REF}^- must have very low output impedance and noise. The circuit in *Figure 14* is an example of a very stable reference appropriate for use with the device.



*Tantalum

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FIGURE 14. Low Drift Extremely Stable Reference Circuit

The ADC12130/2/8 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF}^+ pin is connected to V_A^+ and V_{REF}^- is connected to ground. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

Below are recommended references along with some key specifications.

Part Number	Output Voltage Tolerance	Temperature Coefficient
LM4041CI-Adj	±0.5%	±100ppm/°C
LM4040AI-4.1	±0.1%	±100ppm/°C
LM9140BYZ-4.1	±0.5%	±25ppm/°C
LM368Y-5.0	±0.1%	±20ppm/°C
Circuit of *Figure 14*	Adjustable	±2ppm/°C

The reference voltage inputs are not fully differential. The ADC12130/2/8 will not generate correct conversions or comparisons if V_{REF}^+ is taken below V_{REF}^-. Correct conversions result when V_{REF}^+ and V_{REF}^- differ by 1V and remain, at all times, between ground and V_A^+. The V_{REF} common mode range, $(V_{REF}^+ + V_{REF}^-)/2$ is restricted to $(0.1 \times V_A^+)$ to $(0.6 \times V_A^+)$. Therefore, with $V_A^+ = 5V$ the center of the reference ladder should not go below 0.5V or above 3.0V. *Figure 15* is a graphic representation of the voltage restrictions on V_{REF}^+ and V_{REF}^-.

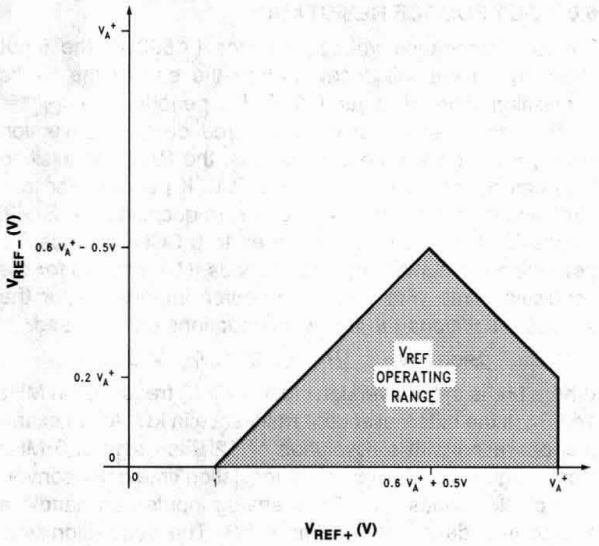

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FIGURE 15. V_{REF} Operating Range

4.0 ANALOG INPUT VOLTAGE RANGE

The ADC12130/2/8's fully differential ADC generate a two's complement output that is found by using the equation shown below:

for (12-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-)\,(4096)}{(V_{REF}^+ - V_{REF}^-)}$$

Round off to the nearest integer value between −4096 to 4095 if the result of the above equation is not a whole number.

Examples are shown in the table below:

V_{REF}^+	V_{REF}^-	V_{IN}^+	V_{IN}^-	Digital Output Code
+2.5V	+1V	+1.5V	0V	0,1111,1111,1111
+4.096V	0V	+3V	0V	0,1011,1011,1000
+4.096V	0V	+2.499V	+2.500V	1,1111,1111,1111
+4.096V	0V	0V	+4.096V	1,0000,0000,0000

5.0 INPUT CURRENT

At the start of the acquisition window (t_A) a charging current flows into or out of the analog input pins (A/DIN1 and A/DIN2) depending on the input voltage polarity. The analog input pins are CH0–CH7 and COM when A/DIN1 is tied to MUXOUT1 and A/DIN2 is tied to MUXOUT2. The peak value of this input current will depend on the actual input voltage applied, the source impedance and the internal multiplexer switch on resistance. With MUXOUT1 tied to A/DIN1 and MUXOUT2 tied to A/DIN2 the internal multiplexer switch on resistance is typically 1.6 kΩ. The A/DIN1 and A/DIN2 mux on resistance is typically 750Ω.

Application Hints (Continued)

6.0 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<600Ω), the input charging current will decay, before the end of the S/H's acquisition time of 2 μs (10 CCLK periods with f_{CK} = 5 MHz), to a value that will not introduce any conversion errors. For high source impedances, the S/H's acquisition time can be increased to 18 or 34 CCLK periods. For less ADC accuracy and/or slower CCLK frequencies the S/H's acquisition time may be decreased to 6 CCLK periods. To determine the number of clock periods (N_C) required for the acquisition time with a specific source impedance for the various resolutions the following equations can be used:

12 Bit + Sign $N_C = [R_S + 2.3] \times f_{CK} \times 0.824$

Where f_{CK} is the conversion clock (CCLK) frequency in MHz and R_S is the external source resistance in kΩ. As an example, operating with a resolution of 12 Bits + sign, a 5 MHz clock frequency and maximum acquistion time of 34 conversion clock periods the ADC's analog inputs can handle a source impedance as high as 6 kΩ. The acquisition time may also be extended to compensate for the settling or response time of external circuitry connected between the MUXOUT and A/DIN pins.

The acquisition time t_A is started by a falling edge of SCLK and ended by a rising edge of CCLK (see timing diagrams). If SCLK and CCLK are asynchronous one extra CCLK clock period may be inserted into the programmed acquisition time for synchronization. Therefore with asnychronous SCLK and CCLKs the acquisition time will change from conversion to conversion.

7.0 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μF–0.1 μF) can be connected between the analog input pins, CH0–CH7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

8.0 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

9.0 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. The minimum power supply bypassing capacitors recommended are low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF monolithic ceramic capacitors. More or different bypassing may be necessary depending on the overall system requirements. Separate bypass capacitors should be used for the V_A^+ and V_D^+ supplies and placed as close as possible to these pins.

10.0 GROUNDING

The ADC12130/2/8's performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all components that handle analog signals. The digital and analog ground planes are connected together at only one point, either the power supply ground or at the pins of the ADC. This greatly reduces the occurence of ground loops and noise.

Shown in *Figure 16* is the ideal ground plane layout for the ADC12138 along with ideal placement of the bypass capacitors. The circuit board layout shown in *Figure 16* uses three bypass capacitors: 0.01 μF (C1) and 0.1 μF (C2) surface mount capacitors and 10 μF (C3) tantalum capacitor.

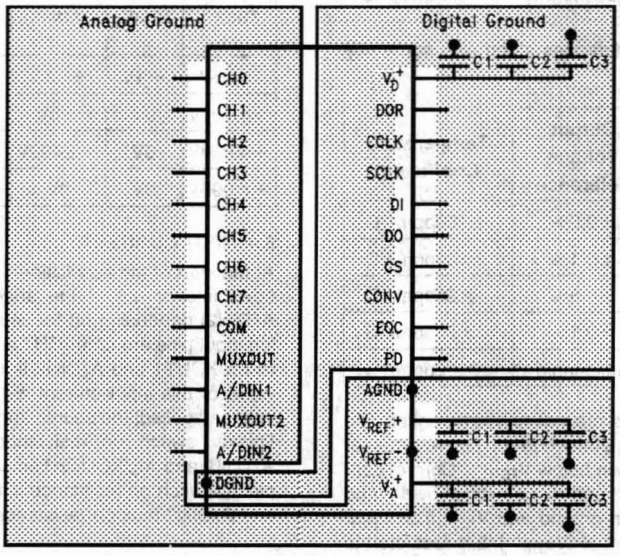

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FIGURE 16. Ideal Ground Plane

Application Hints (Continued)

11.0 CLOCK SIGNAL LINE ISOLATION

The ADC12130/2/8's performance is optimized by routing the analog input/output and reference signal conductors as far as possible from the conductors that carry the clock signals to the CCLK and SCLK pins. Ground traces parallel to the clock signal traces can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

12.0 THE CALIBRATION CYCLE

A calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize after initial turn-on. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ±0.4 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if the Power Supply Voltage and the ambient temperature do not change significantly (see the curves in the Typical Performance Characteristics).

13.0 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature or the power supply voltage change significantly. (See the curves titled "Zero Error Change vs Ambient Temperature" and "Zero Error Change vs Supply Voltage" in the Typical Performance Characteristics.)

14.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in the table of Electrical Characteristics, and spectral plots of S/(N + D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.8)\ dB$$

where n is the A/D's resolution in bits.

The effective bits of a real A/D converter, therefore, can be found by:

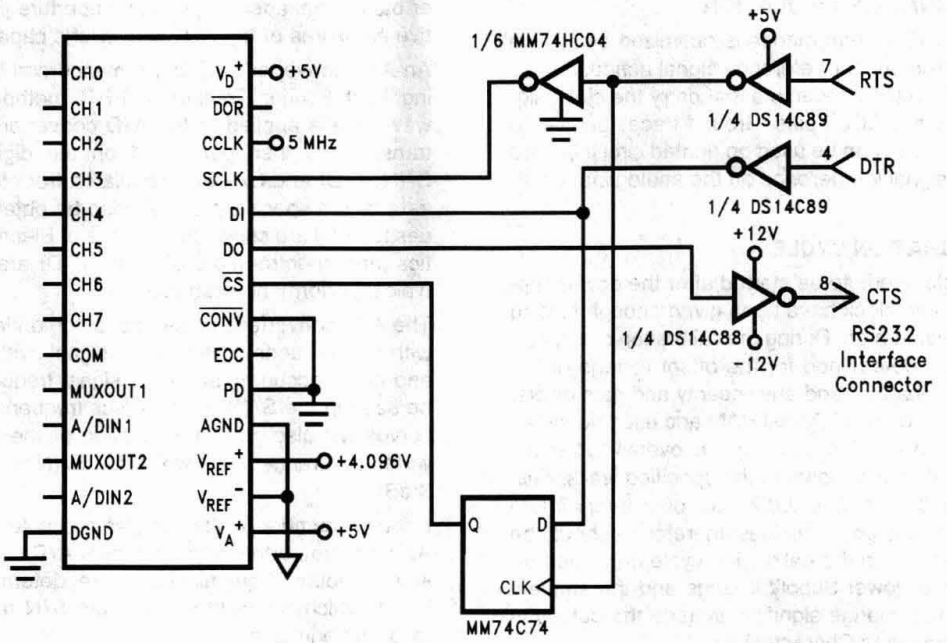
$$n(\text{effective}) = \frac{S/N(dB) - 1.8}{6.02}$$

As an example, this device with a differential signed 5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

15.0 AN RS232 SERIAL INTERFACE

Shown on the following page is a schematic for an RS232 interface to any IBM and compatible PCs. The DTR, RTS, and CTS RS232 signal lines are buffered via level translators and connected to the ADC12138's DI, SCLK, and $\overline{DO}$ pins, respectively. The D flip/flop is used to generate the $\overline{CS}$ signal.

Application Hints (Continued)



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Note: V_A^+, V_D^+, and V_{REF}^+ on the ADC12138 each have 0.01 μF and 0.1 μF chip caps, and 10 μF tantalum caps. All logic devices are bypassed with 0.1 μF caps.

The assignment of the RS232 port is shown below

			B7	B6	B5	B4	B3	B2	B1	B0
COM1	Input Address	3FE	X	X	X	CTS	X	X	X	X
	Output Address	3FC	X	X	X	0	X	X	RTS	DTR

A sample program, written in Microsoft QuickBasic, is shown on the next page. The program prompts for data mode select instruction to be sent to the A/D. This can be found from the Mode Programming table shown earlier. The data should be entered in "1"s and "0"s as shown in the table with DI0 first. Next the program prompts for the number of SCLKs required for the programmed mode select instruction. For instance, to send all "0"s to the A/D, selects CH0 as the + input, CH1 as the − input, 12-bit conversion, and 13-bit MSB first data output format (if the sign bit was not turned off by a previous instruction). This would require 13 SCLK periods since the output data format is 13 bits. The part powers up with No Auto Cal, No Auto Zero, 10 CCLK Acquisition Time, 12-bit conversion, data out with sign, power up, 12- or 13-bit MSB First, and user mode. Auto Cal, Auto Zero, Power Up and Power Down instructions do not change these default settings. Since there is no $\overline{CS}$ signal to synchronize the serial interface the following power up sequence should be followed:

1. Run the program
2. Prior to responding to the prompt apply the power to the ADC12138
3. Respond to the program prompts

It is recommended that the first instruction issued to the ADC12138 be Auto Cal (see Section 1.1).

Application Hints (Continued)

```
'variables DOL=Data Out word length, DI=Data string for A/D DI input,
'            DO=A/D result string

'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC)                                    'set RTS HIGH
OUT &H3FC, (&HFE AND INP(&H3FC)                                   'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC)                                  'SET RTS LOW

OUT &H3FC, (&HEF AND INP(&H3FC))                                  'set B4 low
10
LINE INPUT "DI data for ADC12138 (see Mode Table on data sheet)"; DI$
INPUT "ADC12138 output word length (12,13,16 or 17)"; DOL
20

'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC)                                    'set RTS HIGH
OUT &H3FC, (&HFE AND INP(&H3FC)                                   'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC)                                  'SET RTS LOW

'SET CS# LOW
OUT &H3FC, (&H2 OR INP (&H3FC)                                    'set RTS HIGH
OUT &H3FC, (&H1 OR INP(&H3FC)                                     'SET DTR HIGH
OUT &H3FC, (&HFD AND INP (&H3FC)                                  'SET RTS LOW

DO$=""                                                            'reset DO variable
    OUT &H3FC, (&H1 OR INP(&H3FC)                                 'SET DTR HIGH
    OUT &H3FC, (&HFD AND INP(&H3FC))                              'SCLK low
FOR N = 1 TO 8
    Temp$ = MID$(DI$, N, 1)
    IF Temp$="0" THEN
        OUT &H3FC, (&H1 OR INP(&H3FC))
    ELSE OUT &H3FC, (&HFE AND INP(&H3FC))
    END IF                                                        'out DI
    OUT &H3FC, (&H2 OR INP(&H3FC))                                'SCLK high
    IF (INP(&H3FE) AND 16) = 16 THEN
        DO$ = DO$ + "0"
        ELSE
        DO$ = DO$ + "1"
    END IF                                                        'Input DO
    OUT &H3FC, (&H1 OR INP(&H3FC)                                 'SET DTR HIGH
    OUT &H3FC, (&HFD AND INP(&H3FC))                              'SCLK low
NEXT N
IF DOL > 8 THEN
    FOR N=9 TO DOL
    OUT &H3FC, (&H1 OR INP(&H3FC)                                 'SET DTR HIGH
    OUT &H3FC, (&HFD AND INP(&H3FC))                              'SCLK low
    OUT &H3FC, (&H2 OR INP(&H3FC))                                'SCLK high

    IF (INP(&H3FE) AND &H10) = &H10 THEN
        DO$ = DO$ + "0"
    ELSE
        DO$ = DO$+"1"
    END IF
    NEXT N
END IF
OUT &H3FC, (&HFA AND INP(&H3FC))                                  'SCLK low and DI high
FOR N = 1 TO 500
NEXT N
PRINT DO$
INPUT "Enter "C" to convert else "RETURN" to alter DI data"; s$
IF s$ = "C" OR s$ = "c" THEN
GOTO 20
ELSE
GOTO 10
END IF
END
```

National Semiconductor

ADC1205/ADC1225 12-Bit Plus Sign μP Compatible A/D Converters

General Description

The ADC1205 and ADC1225 are CMOS, 12-bit plus sign successive approximation A/D converters. The 24-pin ADC1205 outputs the 13-bit data result in two 8-bit bytes, formatted high-byte first with sign extended. The 28-pin ADC1225 outputs a 13-bit word in parallel for direct interface to a 16-bit data bus.

Negative numbers are represented in 2's complement data format. All digital signals are fully TTL and MOS compatible.

A unipolar input (0V to 5V) can be accommodated with a single 5V supply, while a bipolar input (−5V to +5V) requires the addition of a 5V negative supply.

The ADC1205C and ADC1225C have a maximum non-linearity of 0.0224% of Full Scale.

Key Specifications

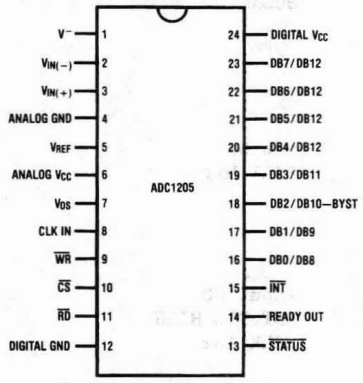
- Resolution—12 bits plus sign
- Linearity Error—±1 LSB
- Conversion Time—100 μs

Features

- Compatible with all μPs
- True differential analog voltage inputs
- 0V to 5V analog voltage range with single 5V supply
- TTL/MOS input/output compatible
- Low power—25 mW max
- Standard 24-pin or 28-pin DIP

Connection and Functional Diagrams

Dual-In-Line Package



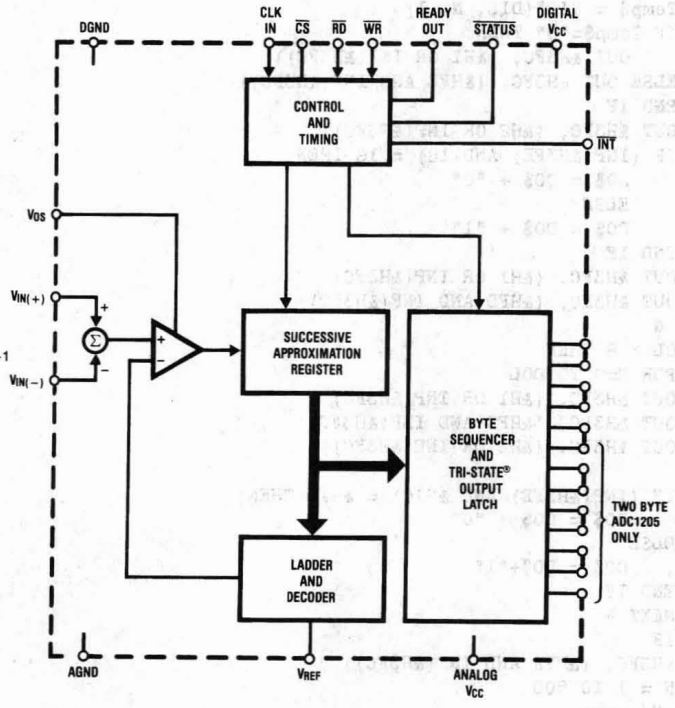
Top View

TL/H/5676-1

Dual-In-Line Package

Top View

TL/H/5676-2



TL/H/5676-3

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (DV_{CC} and AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−15V to GND
Logic Control Inputs	−0.3V to +15V
Voltage at Analog Inputs $[V_{IN(+)}, V_{IN(-)}]$	$(V^-)-0.3V$ to $V_{CC}+0.3V$
Voltage at All Outputs, V_{REF}, V_{OS}	−0.3V to $(V_{CC}+0.3)V$
Input Current per Pin	±5mA
Input Current per Package	±20mA
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A=25°C$	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 12)	800V

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN}\le T_A\le T_{MAX}$
ADC1205CCJ, ADC1225CCD	$-40°C\le T_A\le +85°C$
ADC1205CCJ-1, ADC1225CCD-1	$0°C\le T_A\le 70°C$
Supply Voltage (DV_{CC} and AV_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Negative Supply Voltage (V^-)	−15V to GND

Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- =$ GND for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205CCJ, ADC1225CCD			ADC1205CCJ-1, ADC1225CCD-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CONVERTER CHARACTERISTICS								
Linearity Error ADC1205CCJ, ADC1225CCD ADC1205CCJ-1, ADC1225CCD-1	Unipolar Input Range (Note 11)		**±1**			±1	**±1**	LSB LSB
Unadjusted Zero Error	Unipolar Input Range		**±2**			±2	**±2**	LSB
Unadjusted Positive and Negative Full-Scale Error	Unipolar Input Range		**±30**			±30	**±30**	LSB
Negative Full-Scale Error	Unipolar Input Range, Full Scale Adj. to Zero			**±½**			**±½**	LSB
Linearity Error ADC1205CCJ, ADC1225CCD ADC1205CCJ-1, ADC1225CCD-1	Bipolar Input Range (Note 11)		**±2**			±2	**±2**	LSB LSB
Unadjusted Zero Error	Bipolar Input Range		**±2**			±2	**±2**	LSB
Unadjusted Positive and Negative Full-Scale Error	Bipolar Input Range		**±30**			±30	**±30**	LSB
Negative Full-Scale Error	Bipolar Input Range, Full Scale Adj. to Zero		**±2**			±2	**±2**	LSB
Maximum Gain Temperature Coefficient		6		**15**	6		**15**	ppm/°C
Maximum Offset Temperature Coefficient		0.5		**1.5**	0.5		**1.5**	ppm/°C
Minimum V_{REF} Input Resistance		4.0	**2**		4.0	2	**2**	kΩ
Maximum V_{REF} Input Resistance		4.0	**8**		4.0	8	**8**	kΩ

Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- =$ GND for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205CCJ, ADC1225CCD			ADC1205CCJ-1, ADC1225CCD-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CONVERTER CHARACTERISTICS (Continued)								
Minimum Analog Input Voltage	Unipolar Input Range		**GND-0.05**			GND-0.05	**GND-0.05**	V
	Bipolar Input Range		**$-V_{CC}-0.05$**			$-V_C-0.05$	**$-V_{CC}-0.05$**	V
Maximum Analog Input Voltage	Unipolar Input Range		**$V_{CC}+0.05$**			$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
	Bipolar Input Range	**$V_{CC}+0.05$**				$V_{CC}+0.05$	**$V_{CC}+0.05$**	V
DC Common-Mode Error		$\pm 1/8$	$\pm 1/2$		$\pm 1/8$	$\pm 1/2$	$\pm 1/2$	LSB
Power Supply Sensitivity	$AV_{CC} = DV_{CC} = 5V \pm 5\%$, $V^- = -5V \pm 5\%$							
Zero Error			$\pm 3/4$			$\pm 3/4$	$\pm 3/4$	LSB
Positive and Negative Full-Scale Error			$\pm 3/4$			$\pm 3/4$	$\pm 3/4$	LSB
Linearity Error			$\pm 1/4$			$\pm 1/4$	$\pm 1/4$	LSB
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC} = 5.25V$, All Inputs except CLK IN		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC} = 4.75V$, All Inputs except CLK IN		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN} = 5V$	0.005	**1**		0.005		**1**	**μA**
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN} = 0V$	−0.005	**−1**		−0.005		**−1**	**μA**
V_T^+ (Min), Minimum Positive-Going Threshold Voltage	CLK IN	3.1	**2.7**		3.1	2.7	**2.7**	V
V_T^+ (Max), Maximum Positive-Going Threshold Voltage	CLK IN	3.1	**3.5**		3.1	3.5	**3.5**	V
V_T^- (Min), Minimum Negative-Going Threshold Voltage	CLK IN	1.8	**1.4**		1.8	1.4	**1.4**	V
V_T^- (Max), Maximum Negative-Going Threshold Voltage	CLK IN	1.8	**2.1**		1.8	2.1	**2.1**	V
V_H(Min), Minimum Hysteresis $[V_T^+(Min) - V_T^-(Max)]$	CLK IN	1.3	**0.6**		1.3	0.6	**0.6**	V
V_H(Max), Maximum Hysteresis $[V_T^+(Max) - V_T^-(Min)]$	CLK IN	1.3	**2.1**		1.3	2.1	**2.1**	V

Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = 5V$, $V_{REF} = 5V$, $f_{CLK} = 1.0$ MHz, $V^- = -5V$ for bipolar input range, or $V^- = GND$ for unipolar input range unless otherwise specified. Bipolar input range is defined as $-5.05V \le V_{IN(+)} \le 5.05V$; $-5.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. Unipolar input range is defined as $-0.05V \le V_{IN(+)} \le 5.05V$; $-0.05V \le V_{IN(-)} \le 5.05V$ and $|V_{IN(+)} - V_{IN(-)}| \le 5.05V$. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$ (Notes 3, 4, 5, 6, 7).

Parameter	Conditions	ADC1205CCJ, ADC1225CCD			ADC1205CCJ-1, ADC1225CCD-1			Limit Units
		Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
DIGITAL AND DC CHARACTERISTICS (Continued)								
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**			2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Leakage Current (Max)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−0.3 0.3	**−3** **3**	μA μA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT} = 0V$	−12	**−6.0**		−12	−7.0	**−6.0**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT} = 5V$	16	**8.0**		16	9.0	**8.0**	mA
DI_{CC}, DV_{CC} Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	1	**3**		1	2.5	**3**	mA
AI_{CC}, AV_{CC} Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	1	**3**		1	2.5	**3**	mA
I^-, V^- Supply Current (Max)	$f_{CLK} = 1$ MHz, $\overline{CS} = 1$	10	**100**		10	100	**100**	μA

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = 5.0V$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Limit Units
f_{CLK}, Clock Frequency	MIN MAX		1.0 1.0	0.3 1.5		MHz MHz
Clock Duty Cycle	MIN MAX				40 60	% %
T_C, Conversion Time	MIN MAX MIN MAX	 $f_{CLK} = 1.0$ MHz $f_{CLK} = 1.0$ MHz			108 109 108 109	$1/f_{CLK}$ $1/f_{CLK}$ μs μs
$t_{W(\overline{WR})L}$, $\overline{WR}$ Pulse Width	MAX		220		350	ns
t_{ACC}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid) (Max)		$C_L = 100$ pF	210		340	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State) (Max)		$R_L = 2k$, $C_L = 100$ pF	170		290	ns
$t_{PD(READYOUT)}$, $\overline{RD}$ or $\overline{WR}$ to READYOUT Delay (Max)			250		400	ns
$t_{PD(INT)}$, $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$ (Max)			250		400	ns

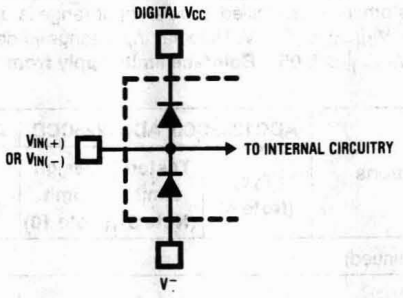
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: A parasitic zener diode exists internally from AV_{CC} and DV_{CC} to ground. This parasitic zener has a typical breakdown voltage of 7 V_{DC}.

AC Electrical Characteristics (Continued)

Note 4: Two on-chip diodes are tied to each analog input as shown below.



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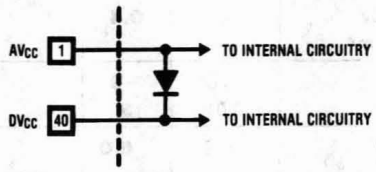
Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV. This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is minimum ($-4.75V_{DC}$), full-scale must be $\leq 4.8V_{DC}$.

Note 5: A diode exists between analog V_{CC} and digital V_C.



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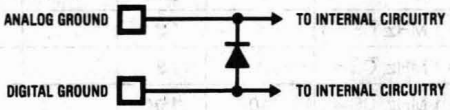
To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 6: A diode exists between analog ground and digital ground.



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To guarantee accuracy, it is required that the analog ground and digital ground be connected together externally.

Note 7: Accuracy is guaranteed at $f_{CLK} = 1.0$ MHz. At higher clock frequencies accuracy may degrade.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 11: Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through positive full scale and zero, after adjusting zero error. (See *Figures 1b* and *1c*).

Note 12: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

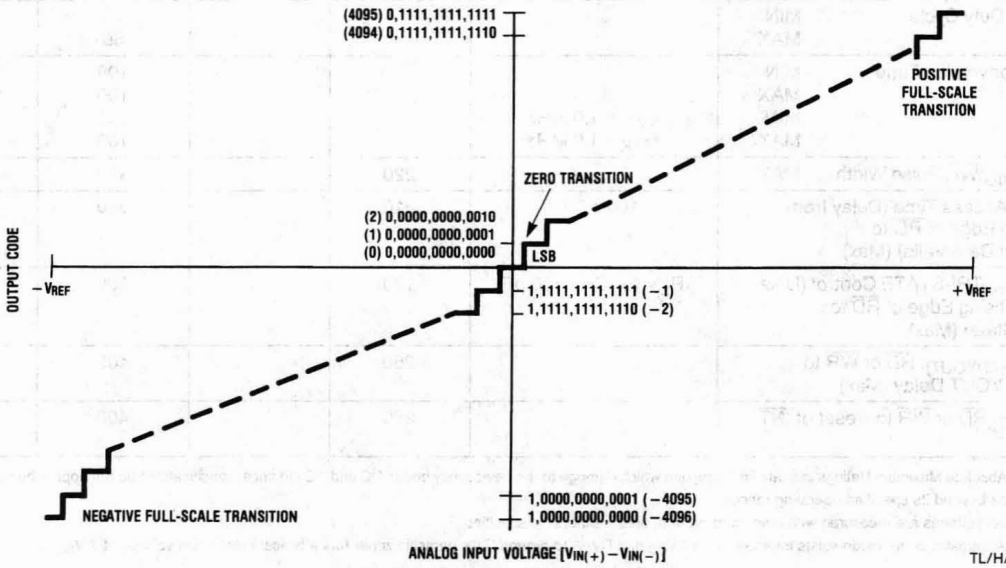

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FIGURE 1a. Transfer Characteristic

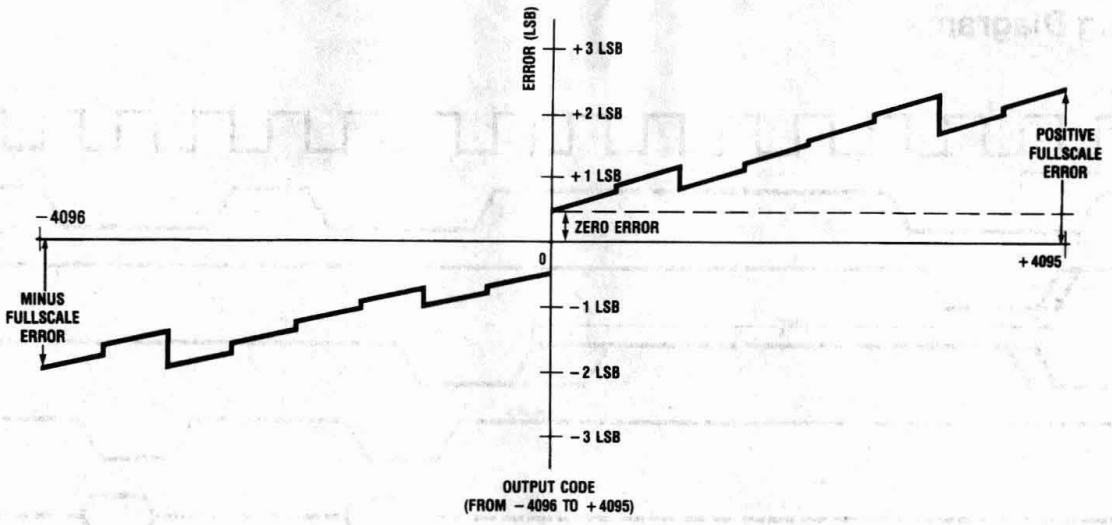

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FIGURE 1b. Simplified Error Curve vs. Output Code Without Zero and Fullscale Adjustment

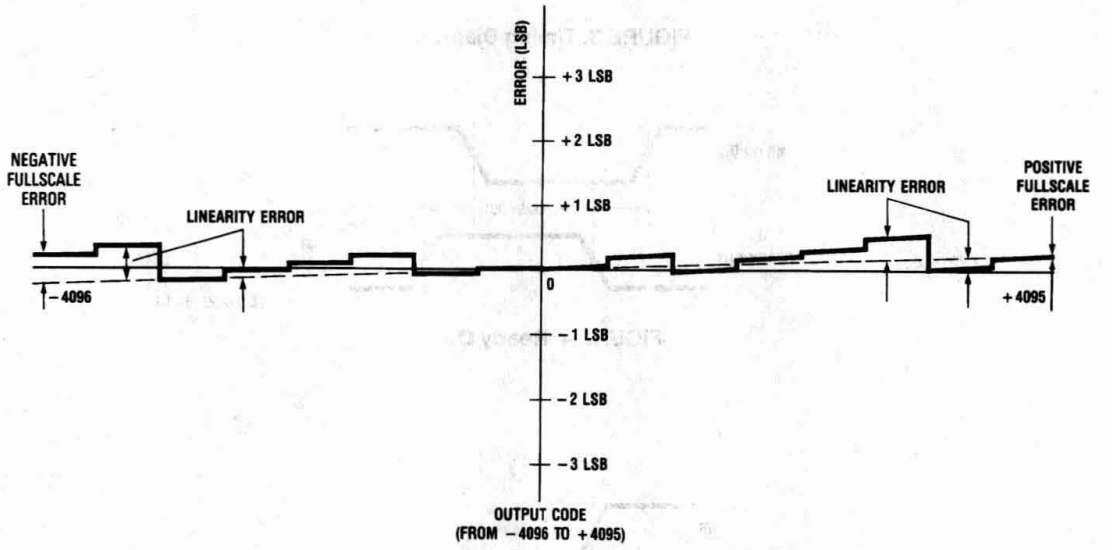

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FIGURE 1c. Simplified Error Curve vs. Output Code after Zero/Fullscale Adjustment

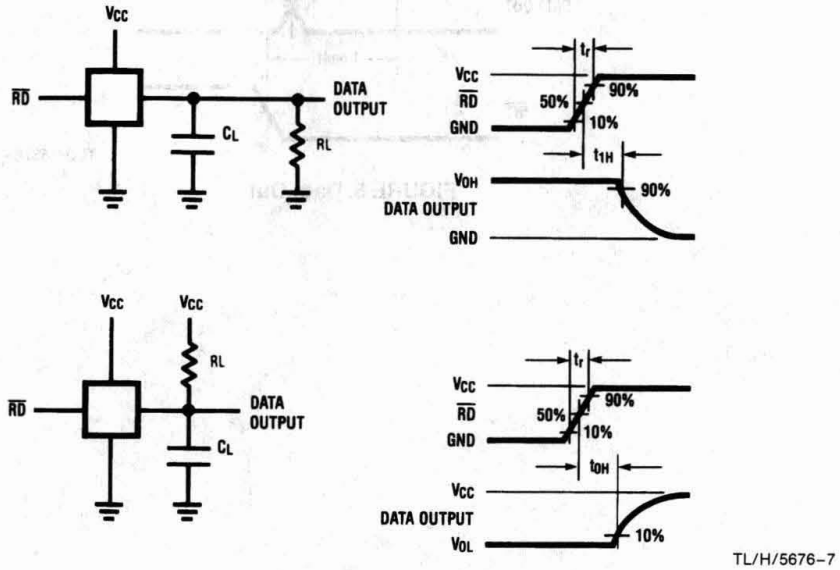

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FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

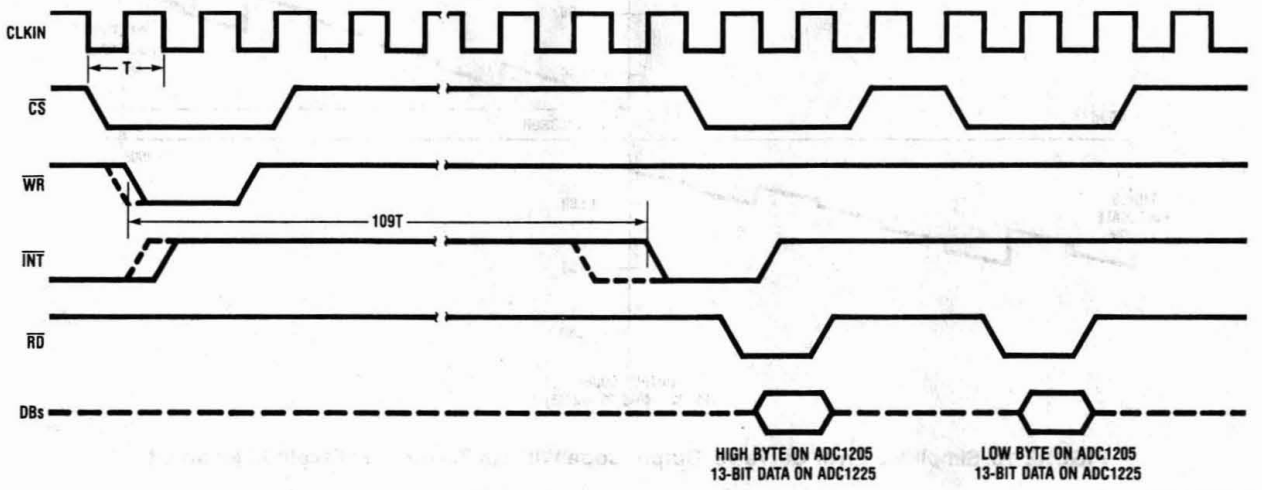

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FIGURE 3. Timing Diagram

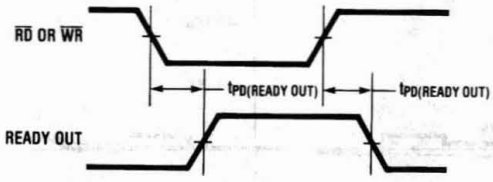

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FIGURE 4. Ready Out

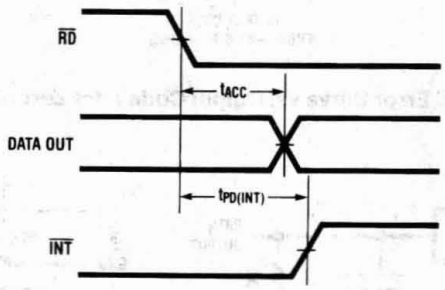

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FIGURE 5. Data Out

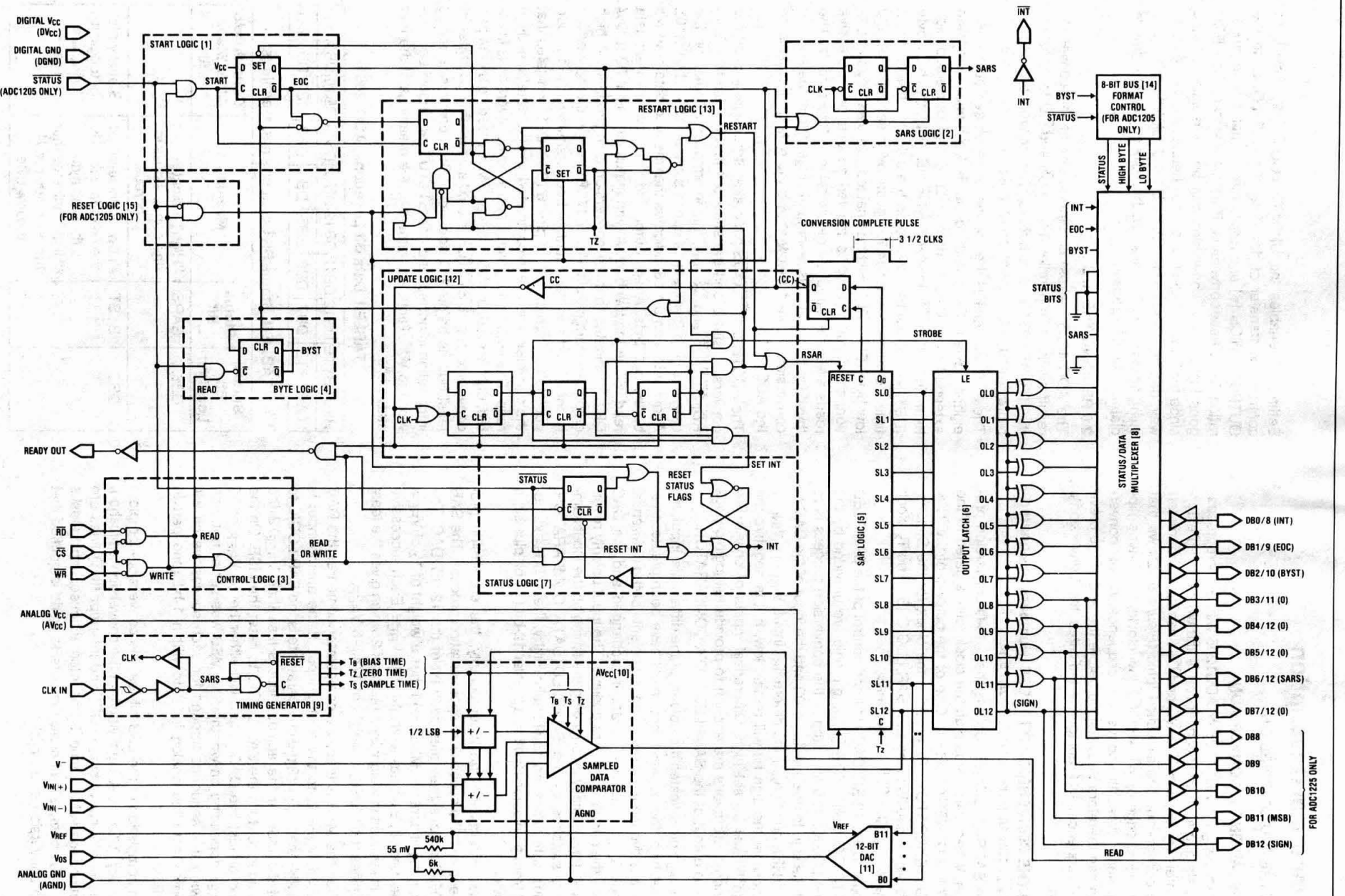


FIGURE 6. Functional Block Diagram

Functional Description

1.0 THE A/D CONVERSION

1.1 STARTING A CONVERSION

When using the ADC1225 or ADC1205 with a microprocessor, starting an A-to-D conversion is like writing to an external memory location. The $\overline{WR}$ and $\overline{CS}$ lines are used to start the conversion. The simplified logic (*Figure 6*) shows that the falling edge of $\overline{WR}$ with $\overline{CS}$ low clocks the D-type flip-flop and initiates the conversion sequence. A new conversion can therefore be restarted before the end of the previous sequence. $\overline{INT}$ going low indicates the conversion's end.

1.2 THE CONVERSION PROCESS (Numbers designated by [ ] refer to portions of *Figure 6.*)

The SARS LOGIC [2] controls the A-to-D conversion process. When 'sars' goes high the clock (clk) is gated to the TIMING GENERATOR [9]. One of the outputs of the TIMING GENERATOR, T_Z, provides the clock for the Successive Approximation Register, SAR LOGIC [5]. The T_Z clock rate is 1/8 of the CLK IN frequency.

Inputs to the 12-BIT DAC [11] and control of the SAMPLED DATA COMPARATOR [10] sign logic are provided by the SAR LOGIC. The first step in the conversion process is to set the sign to positive (logic '0') and the input of the DAC to 000 (HEX notation). If the differential input, $V_{IN(+)} - V_{IN(-)}$, is positive the sign bit will remain low. If it is negative the sign bit will be set high. Differential inputs of only a few hundred microvolts are enough to provide full logic swings at the output of the SAMPLED DATA COMPARATOR.

The sign bit indicates the polarity of the differential input. If it is set high, the negative input must have been greater than the positive input. By reversing the polarity of the differential input, $V_{IN(+)}$ and $V_{IN(-)}$ are interchanged and the DAC sees the negative input as positive. The input polarity reversal is done digitally by changing the timing on the input sampling switches of the SAMPLED DATA COMPARATOR. Thus, with almost no additional circuitry, the A/D is extended from a unipolar 12-bit to a bipolar 12-bit (12-bit plus sign) device.

After determining the input polarity, the conversion proceeds with the successive approximation process. The SAR LOGIC successively tries each bit of the 12-BIT DAC. The most significant bit (MSB), B11, has a weight of 1/2 of V_{REF}. The next bit, B10, has a weight of 1/4 V_{REF}. Each successive bit is reduced in weight by a factor of 2 which gives the least significant bit (LSB) a weight of 1/4096 V_{REF}.

When the MSB is tried, the comparator compares the DAC output, $V_{REF}/2$, to the analog input. If the analog input is greater than $V_{REF}/2$ the comparator tells the SAR LOGIC to set the MSB. If the analog input is less than $V_{REF}/2$ the comparator tells the SAR LOGIC to reset the MSB. On the next bit-test the DAC output will either be 3/4 V_{REF} or 1/4 V_{REF} depending on whether the MSB was set or not. Following this sequence through for each successive bit will approximate the analog input to within 1-bit (one part in 4096).

On completion of the LSB bit-test the conversion-complete flip-flop (CC) is set, signifying that the conversion is finished. The end-of-conversion (EOC) and interrupt ($\overline{INT}$) lines are not changed at this time. Some internal housekeeping tasks must be completed before the outside world is notified that the conversion is finished.

Setting CC enables the UPDATE LOGIC [12]. This logic controls the transfer of data from the SAR LOGIC to the OUTPUT LATCH [6] and resets the internal logic in preparation for a new conversion. This means that when EOC goes high, a new conversion can be immediately started since the internal logic has already been reset. In the same way, data is transferred to the OUTPUT LATCH prior to issuing an interrupt. This assures that data can be read immediately after $\overline{INT}$ goes low.

2.0 READING THE A/D

The ADC 1225 makes all thirteen bits of the conversion result available in parallel. Taking $\overline{CS}$ and $\overline{RD}$ low enables the TRI-STATE® output buffers. The conversion result is represented in 2's complement format.

The ADC1205 makes the conversion result available in two eight-bit bytes. The output format is 2's complement with extended sign. Data is right justified and presented high byte first. With $\overline{CS}$ low and $\overline{STATUS}$ high, the high byte (DB12–DB8) will be enabled on the output buffers the first time $\overline{RD}$ goes low. When $\overline{RD}$ goes low a second time, the low byte (DB7–DB0) will be enabled. On each read operation, the 'byst' flip-flop is toggled so that on successive reads alternate bytes will be available on the outputs. The 'byst' flip-flop is always reset to the high byte at the end of a conversion. Table 1 below shows the data bit locations on the ADC1205.

The ADC1205's $\overline{STATUS}$ pin makes it possible to read the conversion status and the state of the 'byst' flip-flop. With $\overline{RD}$, $\overline{STATUS}$ and $\overline{CS}$ low, this information appears on the data bus. The 'byst' status appears on pin 18 (DB2/DB10). A low output on pin 18 indicates that the next data read will be the high byte. A high output indicates that the next data read will be the low byte. A high status bit on pin 22 (DB6/DB12) indicates that the conversion is in progress. A high output appears on pin 17 (DB1/DB9) when the conversion is completed and the data has been transferred to the output latch. A high output on pin 16 (DB0/DB8) indicates that the conversion has been completed and the data is ready to read. This status bit is reset when a new conversion is initiated, data is read, or status is read. When reading status or a conversion result, $\overline{STATUS}$ should always change states at least 600 ns before $\overline{RD}$ goes low. If the conversion status information is not needed, the $\overline{STATUS}$ pin should be hardwired to V^+. Table 2 summarizes the meanings of the four status bits.

TABLE I. Data Bit Locations, ADC1205

HIGH BYTE	DB12	DB12	DB12	DB12	DB11	DB10	DB9	DB8
LOW BYTE	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

TABLE II. Status Bit Locations and Meanings

Status Bit Location	Status Bit	Meaning	Condition to Clear Status Bit
DB6	SARS	"High" indicates that the conversion is in progress	
DB2	BYST	"Low" indicates that the next data read is the high byte. "High" indicates that the next data read is the low byte	Status write or toggle it with data read

Functional Description (Continued)

TABLE II. Status Bit Locations and Meanings
(Continued)

Status Bit Location	Status Bit	Meaning	Condition to Clear Status Bit
DB1	EOC	"High" indicates that the conversion is completed and data is transferred to the output latch.	
DB0	INT	"High" indicates that it is the end of the conversion and the data is ready to read	Data read or status read or status write

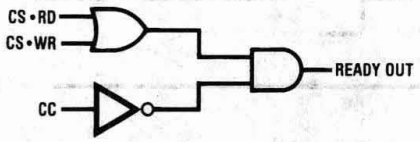
3.0 INTERFACE

3.1 RESET OF INTERRUPT

$\overline{INT}$ goes low at the end of the conversion and indicates that data is transferred to the output latch. By reading data, $\overline{INT}$ will be reset to high on the leading edge of the first read ($\overline{RD}$ going low). $\overline{INT}$ is also reset on the leading (falling) edge of $\overline{WR}$ when starting a conversion.

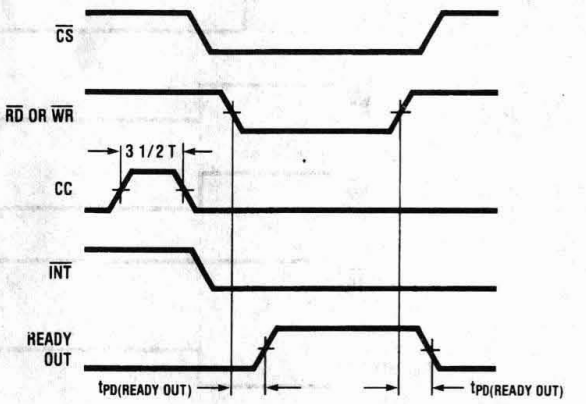
3.2 READY OUT

To simplify the hardware connection to high speed microprocessors, a READY OUT line is provided. This allows the A-to-D to insert a wait state in the μP's read cycle. The equivalent circuit and the timing diagram for READY OUT is shown in *Figures 7* and *8*.



TL/H/5676–9

FIGURE 7. READY OUT Equivalent Circuit



TL/H/5676–10

FIGURE 8. READY OUT Timing Diagram

3.3 RESETTING THE A/D

All the internal logic can be reset, which will abort any conversion in process and reset the status bits. The reset function is achieved by performing a status write ($\overline{CS}$, $\overline{WR}$ and $\overline{STATUS}$ are low).

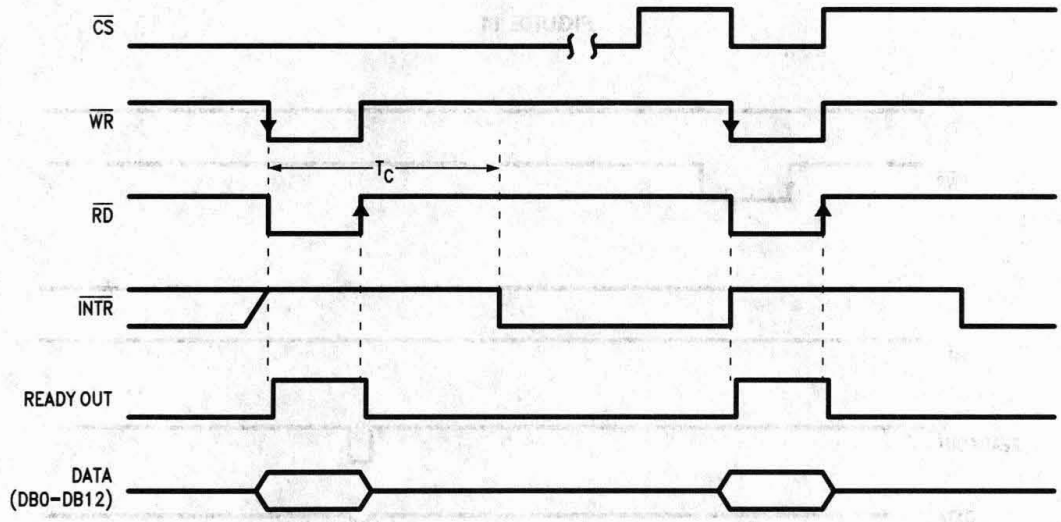
3.4 ADDITIONAL TIMING AND INTERFACE OPTIONS

ADC1225

1. $\overline{WR}$ and $\overline{RD}$ can be tied together with $\overline{CS}$ low continuously or strobed. The previous conversion's data will be available when the $\overline{WR}$ and $\overline{RD}$ are low as shown below.

One drawback is that, since the conversion is started on the falling edge and the data read on the rising edge of $\overline{WR}/\overline{RD}$, the first data access will have erroneous information depending on the power-up state of the internal output latches.

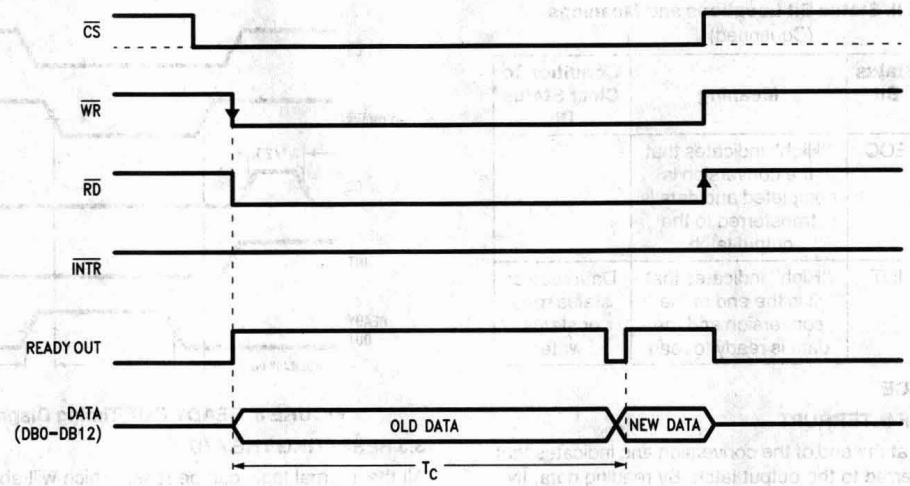
If the $\overline{WR}/\overline{RD}$ strobe is longer than the conversion time, $\overline{INTR}$ will never go low to signal the end of a conversion. The conversion will be completed and the output latches will be updated. In this case the READY OUT signal can be used to sense the end of the conversion since it will go low when the output latches are being updated.



TL/H/5676–24

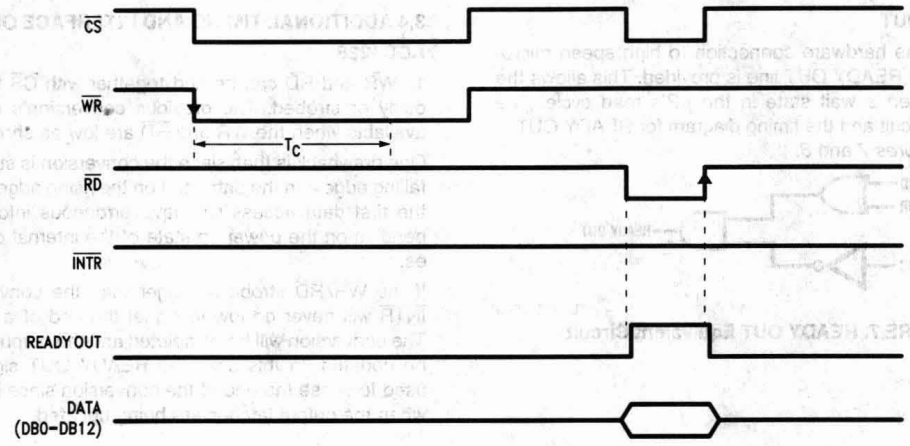
FIGURE 9

Functional Description (Continued)



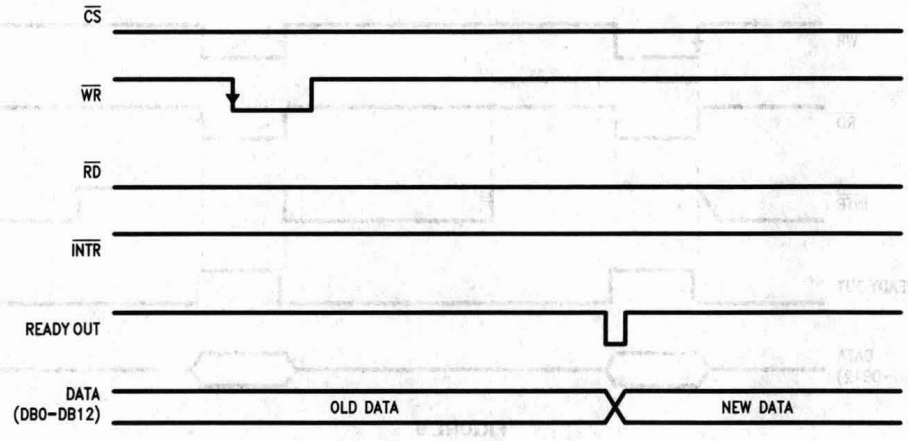
TL/H/5676–25

FIGURE 10



TL/H/5676–26

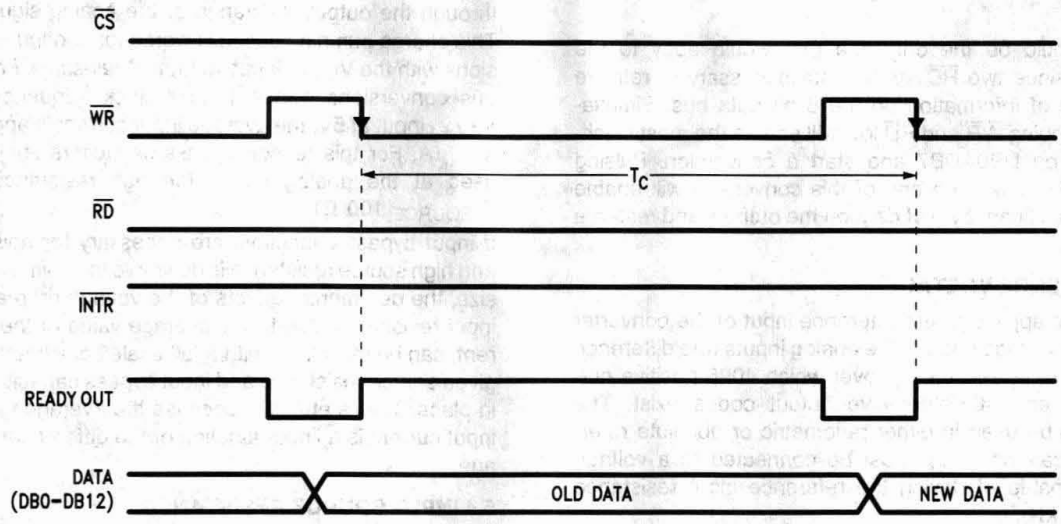
FIGURE 11



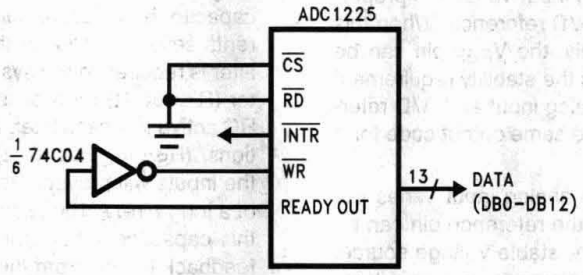
TL/H/5676–27

FIGURE 12

Functional Description (Continued)



TL/H/5676–28



TL/H/5676–29

FIGURE 13

When using this method of conversion only one strobe is necessary and the rising edge of $\overline{WR}/\overline{RD}$ can be used to read the current conversion results. These methods reduce the throughput time of the conversion since the $\overline{RD}$ and $\overline{WR}$ cycles are combined.

2. With the standard timing $\overline{WR}$ pulse width longer than the conversion time a conversion is completed but the $\overline{INTR}$ will never go low to signal the end of a conversion. The output latches will be updated and valid information will be available when the $\overline{RD}$ cycle is accomplished.

3. Tying $\overline{CS}$ and $\overline{RD}$ low continuously and strobing $\overline{WR}$ to initiate a conversion will also yield valid data. The $\overline{INTR}$ will never go low to signal the end of a conversion and the digital outputs will always be enabled, so using $\overline{INTR}$ to strobe the $\overline{WR}$ line for a continuous conversion cannot be done with this part.

A simple stand-alone circuit can be accomplished by driving $\overline{WR}$ with the inverse of the READY OUT signal using a simple inverter as shown below.

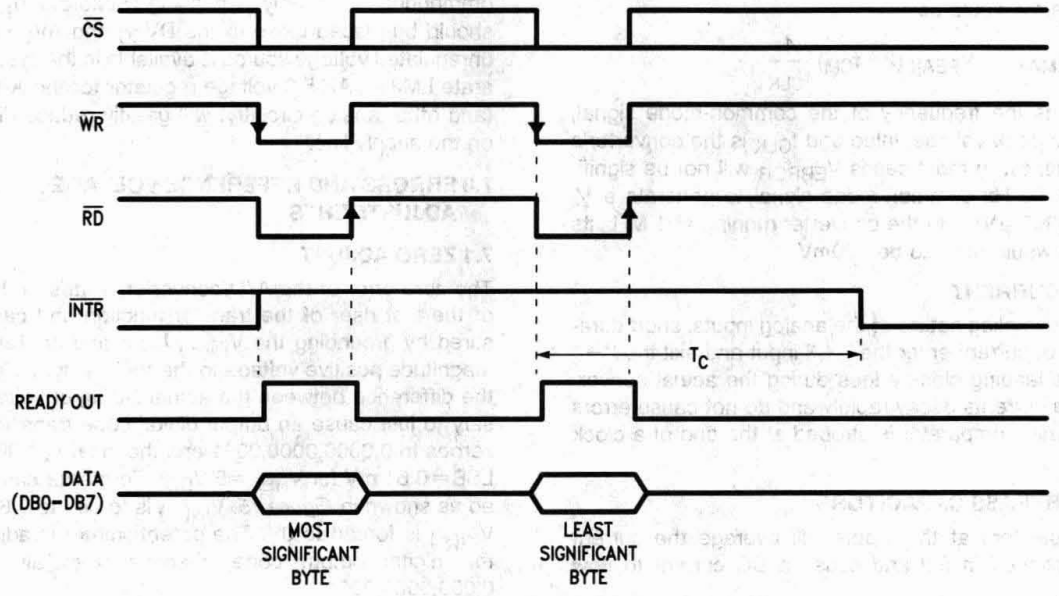


FIGURE 14

TL/H/5676–30

Functional Description (Continued)

ADC1205

Case 1 would be the only one that would appy to the ADC1205 since two $\overline{RD}$ strobes are necessary to retrieve the 13 bits of information on the 8 bit data bus. Simultaneously strobing $\overline{WR}$ and $\overline{RD}$ low will enable the most significant byte on DB0–DB7 and start a conversion. Pulsing $\overline{WR}/\overline{RD}$ low before the end of this conversion will enable the least significant byte of data on the outputs and restart a conversion.

4.0 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog inputs (the difference between $V_{IN(+)}$ and $V_{IN(-)}$, over which 4096 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. V_{REF} must be connected to a voltage source capable of driving the reference input resistance (typically 4 kΩ).

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

5.0 THE ANALOG INPUTS

5.1 DIFFERENTIAL VOLTAGE INPUTS AND COMMON MODE REJECTION

The differential inputs of the ADC1225 and ADC1205 actually reduce the effects of common-mode input noise, i.e., signals common to both $V_{IN(+)}$ and $V_{IN(-)}$ inputs (60 Hz is most typical). The time interval between sampling the "+" and "−" input is 4 clock periods. Therefore, a change in the common-mode voltage during this short time interval may cause conversion errors. For a sinusoidal common-mode signal the error would be:

$$V_{ERROR(MAX)} = V_{PEAK}\,(2\pi\, f_{CM})\,\frac{4}{f_{CLK}}$$

where f_{CM} is the frequency of the common-mode signal, V_{PEAK} is its peak voltage value and f_{CLK} is the converter's clock frequency. In most cases V_{ERROR} will not be significant. For a 60 Hz common-mode signal to generate a ¼ LSB error (300 μV) with the converter running at 1 MHz its peak value would have to be 200mV.

5.2 INPUT CURRENT

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the leading clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

5.3 INPUT BYPASS CAPACITORS

Bypass capacitors at the inputs will average the current spikes mentioned in 5.2 and cause a DC current to flow through the output resistance of the analog signal source. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For continuous conversions with a 1 MHz clock frequency and the $V_{IN(+)}$ input at 5V, the average input current is approximately 5 μA. For this reason bypass capacitors should not be used at the analog inputs for high resistance sources (R_{SOURCE} 100 Ω).

If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, due to the average value of the input current, can be minimized with a full-scale adjustment while the given source resistance and input bypass capacitor are both in place. This is effective because the average value of the input current is a linear function of the differential input voltage.

5.4 INPUT SOURCE RESISTANCE

Large values of source resistance where an input bypass capacitor is not used, will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($R \leq 100\ \Omega$) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($R_{SOURCE} \leq 100\ \Omega$) a 0.001 μF bypass capacitor at the inputs will prevent pickup due to series lead inductance of a long wire. A 100 Ω series resistor can be used to isolate this capacitor – both the R and C are placed outside the feedback loop – from the output of an op amp, if used.

5.5 NOISE

The leads to the analog inputs should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause errors. Input filtering can be used to reduce the effects of these sources, but careful note should be taken of sections 5.3 and 5.4 if this route is taken.

6.0 POWER SUPPLIES

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. Low inductance tantalum capacitors of 1 μF or greater are recommended for supply bypassing. Separate bypass caps should be placed close to the DV_{CC} and AV_{CC} pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

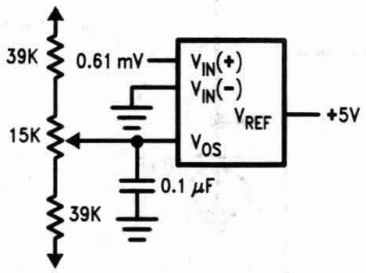
7.0 ERRORS AND REFERENCE VOLTAGE ADJUSTMENTS

7.1 ZERO ADJUST

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage necessary to just cause an output digital code transition from all zeroes to 0,0000,0000,0001 and the ideal ½ LSB value (½ LSB = 0.61 mV for $V_{REF} = 5\ V_{DC}$). Zero error can be adjusted as shown in *Figure 15*. $V_{IN(+)}$ is forced to 0.61 mV, and $V_{IN(-)}$ is forced to 0V. The potentiometer is adjusted until the digital output code changes from all zeroes to 0,000,0000,0001.

Functional Description (Continued)

A simpler, although slightly less accurate, approach is to ground $V_{IN(+)}$ and $V_{IN(-)}$, and adjust for all zeros at the output. Error will be well under ½ LSB if the adjustment is done so that the potentiometer is "centered" within the 0,000,000 range. A positive voltage at the V_{OS} input will reduce the output code. The adjustment range is +4 to −30 LSB.



TL/H/5676–11

FIGURE 15. Zero Adjust Circuit

7.2 POSITIVE AND NEGATIVE FULL-SCALE ADJUSTMENT

Unipolar Inputs

Apply a differential input voltage which is 1.5 LSB below the desired analog full-scale voltage (V_F) and adjust the magnitude of the V_{REF} input so that the output code is just changing from 0,1111,1111,1110 to 0,1111,1111,1111.

Bipolar Inputs

Do the same procedure outlined above for the unipolar case and then change the differential input voltage so that the digital output code is just changing from 1,0000,0000,0001 to 1,0000,0000,0000. Record the differential input voltage, V_X. the ideal differential input voltage for that transition should be;

$$\left(-V_F + \frac{V_F}{8192}\right)$$

Calculate the difference between Vx and the ideal voltage;

$$\Delta = V_X - \left(-V_F + \frac{V_F}{8192}\right)$$

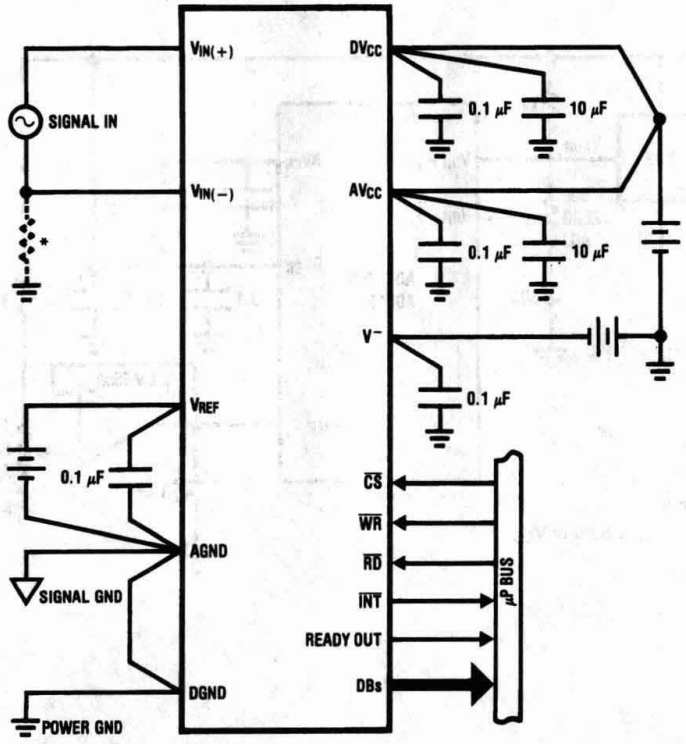
Then apply a differential input voltage of;

$$\left(V_X - \frac{\Delta}{2}\right)$$

and adjust the magnitude of V_{REF} so the digital output code is just changing from 1,0000,0000,0001 to 1,0000,0000,0000. That will obtain the positive and negative full-scale transition with symmetrical minimum error.

Typical Applications

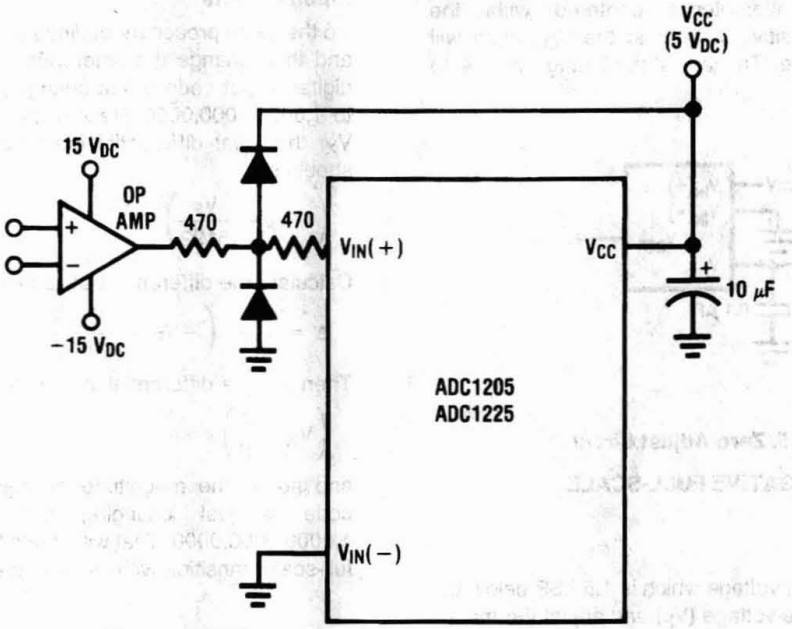
*Input must have some current return path to signal ground



TL/H/5676–12

Typical Applications (Continued)

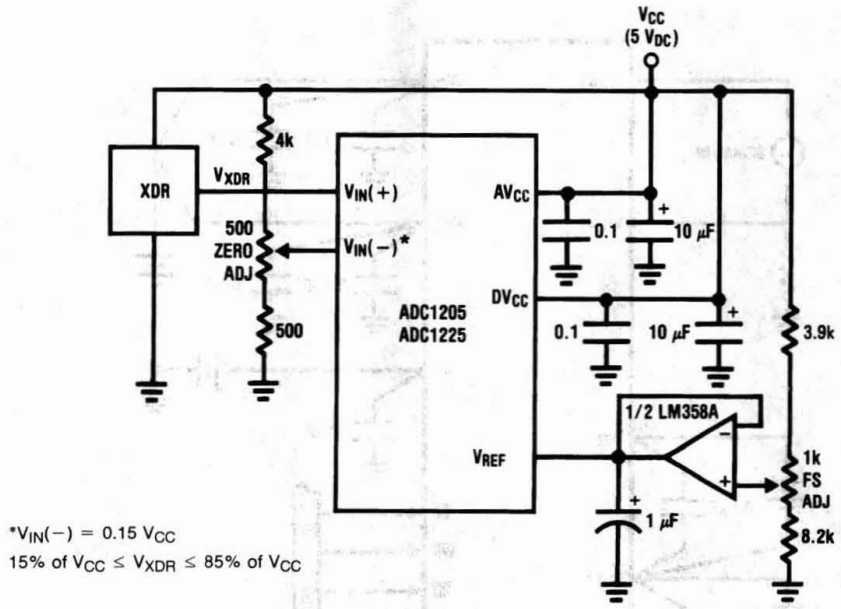
Protecting the Input



Diodes are 1N914

TL/H/5676–16

Operating with Ratiometric Transducers



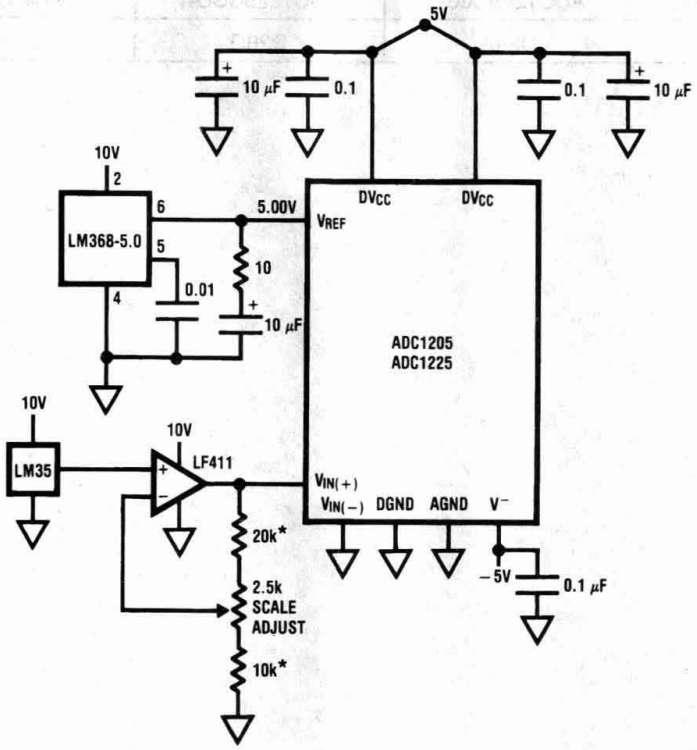
*$V_{IN}(-)$ = 0.15 V_{CC}

15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}

TL/H/5676–17

Typical Applications (Continued)

Bipolar Input Temperature Converter

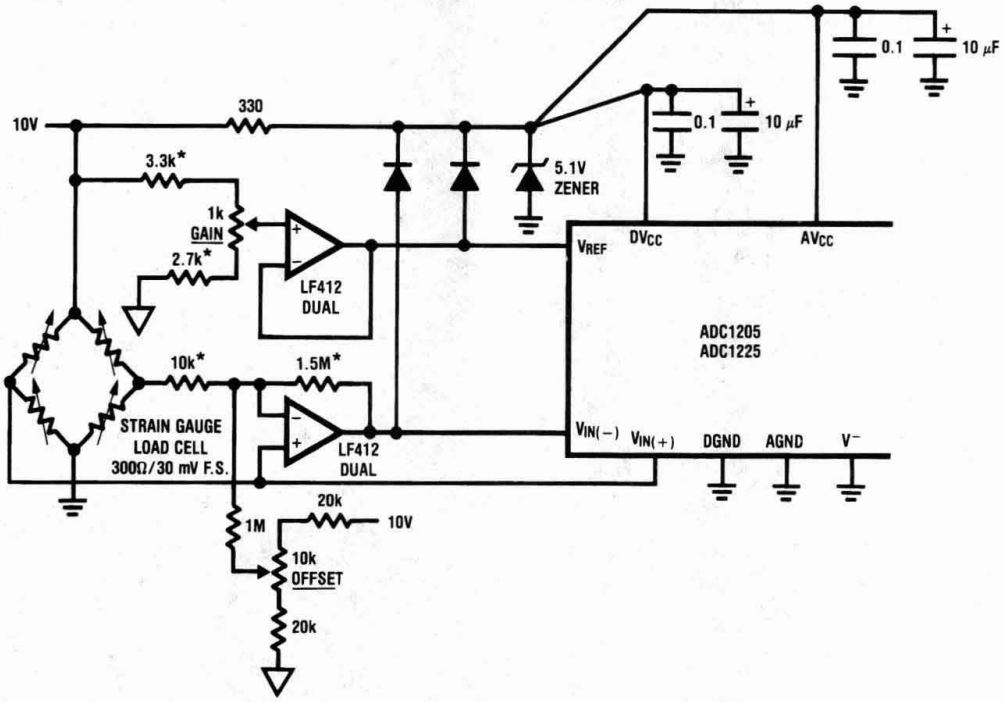


TL/H/5676–18

+150 to −55°C with 0.04°C resolution

Note: * resistors are 1% metal film types

Strain Gauge Converter with .025% Resolution and Single Power Supply



TL/H/5676–19

Note: 1)* resistors are 1% metal film types

2) LF412 power +10V and ground

Ordering Information

Temperature Range		0°C to 70°C		−40°C to +85°C	
Non-Linearity	0.024%	ADC1205CCJ-1	ADC1225CCD-1	ADC1205CCJ	ADC1225CCD
Package Outline		J24A	D28D	J24A	D28D

National Semiconductor

ADC12062
12-Bit, 1 MHz, 75 mW A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative multistep conversion technique, the 12-bit ADC12062 CMOS analog-to-digital converter digitizes signals at a 1 MHz sampling rate while consuming a maximum of only 75 mW on a single +5V supply. The ADC12062 performs a 12-bit conversion in three lower-resolution "flash" conversions, yielding a fast A/D without the cost and power dissipation associated with true flash approaches.

The analog input voltage to the ADC12062 is tracked and held by an internal sampling circuit, allowing high frequency input signals to be accurately digitized without the need for an external sample-and-hold circuit. The multiplexer output is available to the user in order to perform additional external signal processing before the signal is digitized.

When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 100 μW.

Features

- Built-in sample-and-hold
- Single +5V supply
- Single channel or 2 channel multiplexer operation
- Low Power Standby mode

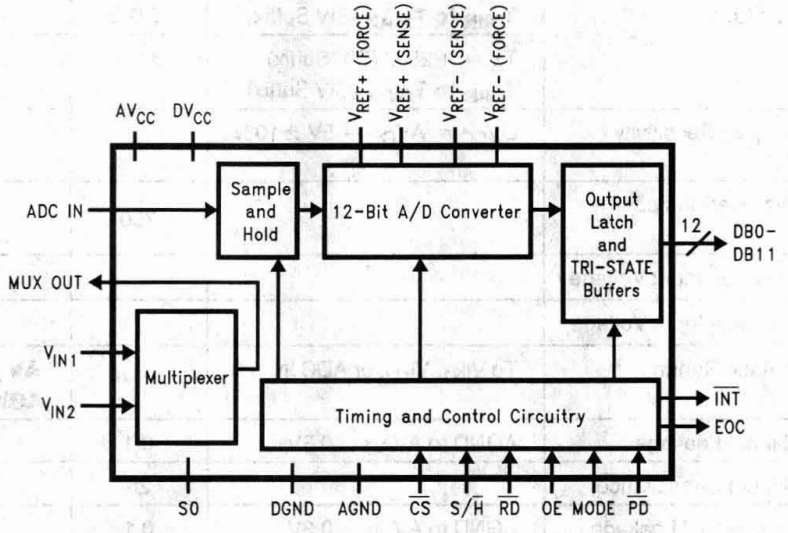
Key Specifications

■ Sampling rate	1 MHz (min)
■ Conversion time	740 ns (typ)
■ Signal-to-Noise Ratio, f_{IN} = 100 kHz	69.5 dB (min)
■ Power dissipation (f_S = 1 MHz)	75 mW (max)
■ No missing codes over temperature	Guaranteed

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications
- Waveform digitizers

Block Diagram



TL/H/11490–1

Ordering Information

Industrial ($-40°C \le T_A \le +85°$)	Package
ADC12062BIV	V44 Plastic Leaded Chip Carrier
ADC12062BIVF	VGZ44A Plastic Quad Flat Package
ADC12062CIV	V44 Plastic Leaded Chip Carrier
ADC12062CIVF	VGZ44A Plastic Quad Flat Package
ADC12062EVAL	Evaluation Board

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	−0.3V to +6V
Voltage at Any Input or Output	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 3)	25 mA
Package Input Current (Note 3)	50 mA
Power Dissipation (Note 4)	875 mW
ESD Susceptibility (Note 5)	2000V
Soldering Information (Note 6)	
V Package, Infrared, 15 seconds	+300°C
VF Package	
Vapor Phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_{JMAX})	150°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12062BIV, ADC12062CIV, ADC12062BIVF, ADC12062CIVF	$-40°C \le T_A \le +85°C$
Supply Voltage Range (DV_{CC} = AV_{CC})	4.5V to 5.5V

Converter Characteristics

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_S = 1 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limit)
	Resolution			**12**	Bits
	Differential Linearity Error	T_A = 25°C	±0.4	±0.8	LSB (max)
		T_{MIN} to T_{MAX}		**±0.95**	LSB (max)
	Integral Linearity Error (Note 9)	**T_{MIN} to T_{MAX}** (BIV Suffix)	±0.4	**±1.0**	LSB (max)
		T_A = +25°C (CIV Suffix)	±0.4	±1.0	LSB (max)
		T_{MIN} to T_{MAX} (CIV Suffix)		**±1.5**	LSB (max)
	Offset Error	**T_{MIN} to T_{MAX}** (BIV Suffix)	±0.3	**±1.25**	LSB (max)
		T_A = +25°C (CIV Suffix)	±0.3	±1.25	LSB (max)
		T_{MIN} to T_{MAX} (CIV Suffix)		**±2.0**	LSB (max)
	Full Scale Error	**T_{MIN} to T_{MAX}** (BIV Suffix)	±0.2	**±1.0**	LSB (max)
		T_A = +25°C (CIV Suffix)	±0.2	±1.0	LSB (max)
		T_{MIN} to T_{MAX} (CIV Suffix)		**±1.5**	LSB (max)
	Power Supply Sensitivity (Note 15)	DV_{CC} = AV_{CC} = 5V ±10%		**±1.0**	LSB (max)
R_{REF}	Reference Resistance		750	**500**	Ω (min)
				1000	Ω (max)
$V_{REF(+)}$	$V_{REF+(SENSE)}$ Input Voltage			**AV_{CC}**	V (max)
$V_{REF(-)}$	$V_{REF-(SENSE)}$ Input Voltage			**AGND**	V (min)
V_{IN}	Input Voltage Range	To V_{IN1}, V_{IN2}, or ADC IN		**AV_{CC} + 0.05V**	V (max)
				AGND − 0.05V	V (min)
	ADC IN Input Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	μA (max)
C_{ADC}	ADC IN Input Capacitance		25		pF
	MUX On-Channel Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	μA (max)
	MUX Off-Channel Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	μA (max)
C_{MUX}	Multiplexer Input Cap		7		pF
	MUX Off Isolation	f_{IN} = 100 kHz	92		dB

Dynamic Characteristics

(Note 10) The following specifications apply for $DV_{CC} = AV_{CC} = +5V$, $V_{REF+(SENSE)} = +4.096V$, $V_{REF-(SENSE)} = AGND$, $R_S = 25\Omega$, $f_{IN} = 100$ kHz, 0 dB from fullscale, and $f_s = 1$ MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limit)
SINAD	Signal-to-Noise Plus Distortion Ratio	**T_{MIN} to T_{MAX}**	71	**68.0**	dB (min)
SNR	Signal-to-Noise Ratio (Note 11)	**T_{MIN} to T_{MAX}**	72	**69.5**	dB (min)
THD	Total Harmonic Distortion (Note 12)	$T_A = +25°C$ **T_{MIN} to T_{MAX}**	−82	−74 **−70**	dBc (max) dBc (max)
ENOB	Effective Number of Bits (Note 13)	**T_{MIN} to T_{MAX}**	11.5	**11.0**	Bits (min)
IMD	Intermodulation Distortion	$f_{IN} = 102.3$ kHz, 102.7 kHz	−80		dBc

DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5V$, $V_{REF+(SENSE)} = +4.096V$, $V_{REF-(SENSE)} = AGND$, and $f_s = 1$ MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage	$DV_{CC} = AV_{CC} = +5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$DV_{CC} = AV_{CC} = +4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current		0.1	**1.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current		0.1	**1.0**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$DV_{CC} = AV_{CC} = +4.5V$, $I_{OUT} = -360\ \mu A$ $I_{OUT} = -100\ \mu A$		 **2.4** **4.25**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$DV_{CC} = AV_{CC} = +4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Leakage Current	Pins DB0–DB11	0.1	**3**	μA (max)
C_{OUT}	TRI-STATE Output Capacitance	Pins DB0–DB11	5		pF
C_{IN}	Digital Input Capacitance		4		pF
DI_{CC}	DV_{CC} Supply Current		2	**3**	mA (max)
AI_{CC}	AV_{CC} Supply Current		10	**12**	mA (max)
$I_{STANDBY}$	Standby Current ($DI_{CC} + AI_{CC}$)	$\overline{PD} = 0V$	20		μA

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5V$, $V_{REF+(SENSE)} = +4.096V$, $V_{REF-(SENSE)} = AGND$, and $f_S = 1$ MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limits)
f_S	Maximum Sampling Rate ($1/t_{THROUGHPUT}$)			**1**	MHz (min)
t_{CONV}	Conversion Time (S/$\overline{H}$ Low to EOC High)		740	**600** **980**	ns (min) ns (max)
t_{AD}	Aperture Delay (S/$\overline{H}$ Low to Input Voltage Held)		20		ns
$t_{S/\overline{H}}$	S/$\overline{H}$ Pulse Width			**5** **550**	ns (min) ns (max)
t_{EOC}	S/$\overline{H}$ Low to EOC Low		95	**60** **125**	ns (min) ns (max)
t_{ACC}	Access Time ($\overline{RD}$ Low or OE High to Data Valid)	$C_L = 100$ pF	10	**20**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control ($\overline{RD}$ High or OE Low to Databus TRI-STATE)	$R_L = 1k$, $C_L = 10$ pF	25	**40**	ns (max)
$t_{\overline{INT}H}$	Delay from $\overline{RD}$ Low to $\overline{INT}$ High	$C_L = 100$ pF	35	**60**	ns (max)
$t_{\overline{INT}L}$	Delay from EOC High to $\overline{INT}$ Low	$C_L = 100$ pF	−25	**−35** **−10**	ns (min) ns (max)
t_{UPDATE}	EOC High to New Data Valid		5	**15**	ns (max)
t_{MS}	Multiplexer Address Setup Time (MUX Address Valid to EOC Low)			**50**	ns (min)
t_{MH}	Multiplexer Address Hold Time (EOC Low to MUX Address Invalid)			**50**	ns (min)
$t_{\overline{CS}S}$	$\overline{CS}$ Setup Time ($\overline{CS}$ Low to $\overline{RD}$ Low, S/$\overline{H}$ Low, or OE High)			**20**	ns (min)
$t_{\overline{CS}H}$	$\overline{CS}$ Hold Time ($\overline{CS}$ High after $\overline{RD}$ High, S/$\overline{H}$ High, or OE Low)			**20**	ns (min)
t_{WU}	Wake-Up Time ($\overline{PD}$ High to First S/$\overline{H}$ Low)		1		μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND (GND = AGND = DGND), unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V_{CC}$) the absolute value of current at that pin should be limited to 25 mA or less. The 50 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. θ_{JA} for the V (PLCC) package is 55°C/W. θ_{JA} for the VF (PQFP) package is 62°C/W. In most cases the maximum derated power dissipation will be reached only during fault conditions.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model ESD rating is 200V.

Note 6: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Typicals are at +25°C and represent most likely parametric norm.

Note 8: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Integral Linearity Error is the maximum deviation from a straight line between the *measured* offset and full scale endpoints.

Note 10: Dynamic testing of the ADC12062 is done using the ADC IN input. The input multiplexer adds harmonic distortion at high frequencies. See the graph in the Typical Performance Characteristics section for a typical graph of THD performance vs input frequency with and without the input multiplexer.

Note 11: The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.

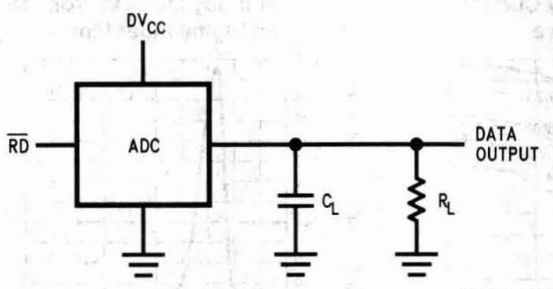
Note 12: The contributions from the first nine harmonics are used in the calculation of the THD.

Note 13: Effective Number of Bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation ENOB = (SINAD − 1.76)/6.02.

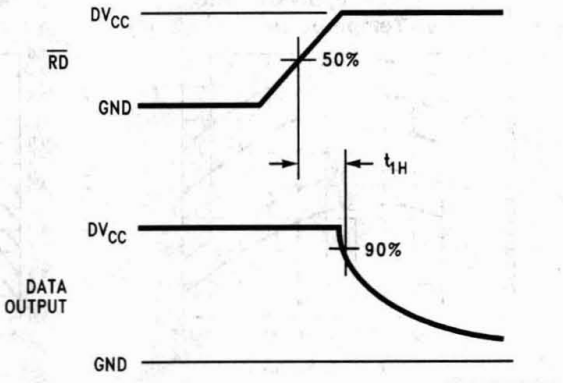
Note 14: The digital power supply current takes up to 10 seconds to decay to its final value after PD is pulled low. This prohibits production testing of the standby current. Some parts may exhibit significantly higher standby currents than the 20 μA typical.

Note 15: Power Supply Sensitivity is defined as the change in the Offset Error or the Full Scale Error due to a change in the supply voltage.

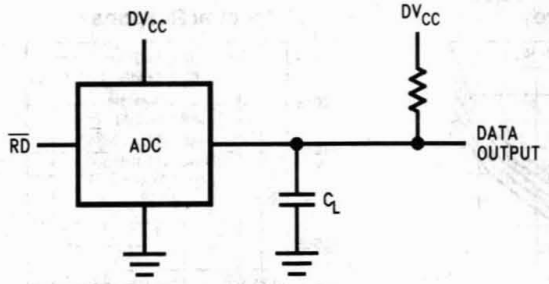
TRI-STATE Test Circuit and Waveforms



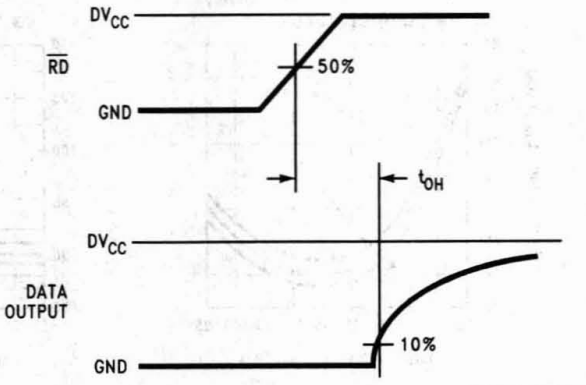
TL/H/11490–2



TL/H/11490–3



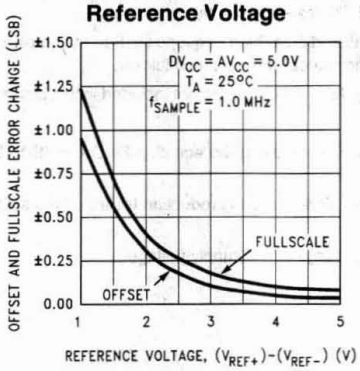
TL/H/11490–4



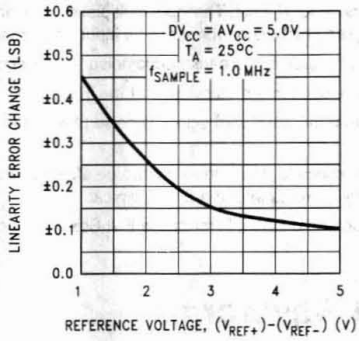
TL/H/11490–5

Typical Performance Characteristics

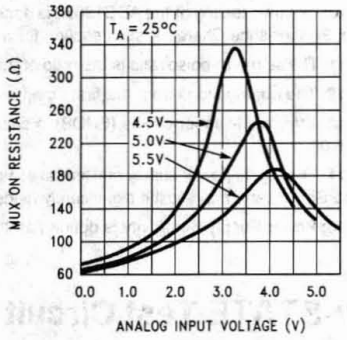
Offset and Fullscale Error Change vs Reference Voltage



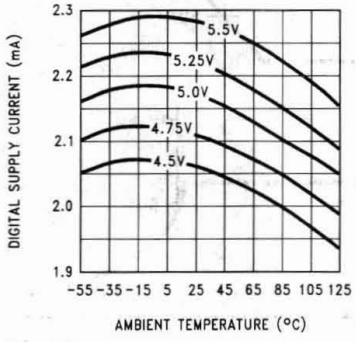
Linearity Error Change vs Reference Voltage



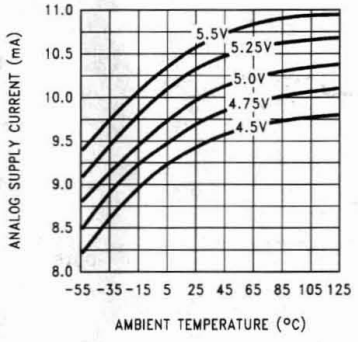
Mux ON Resistance vs Input Voltage



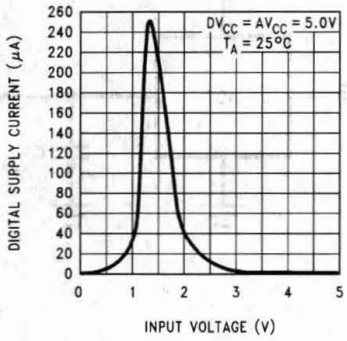
Digital Supply Current vs Temperature



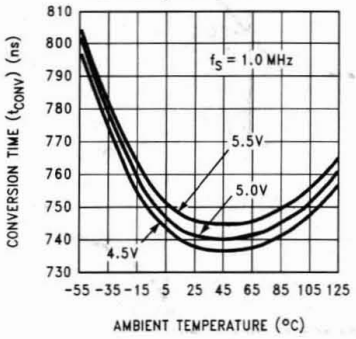
Analog Supply Current vs Temperature



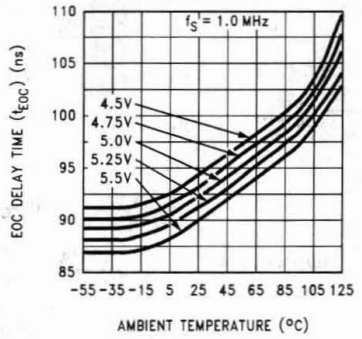
Current Consumption in Standby Mode vs Voltage on Digital Input Pins



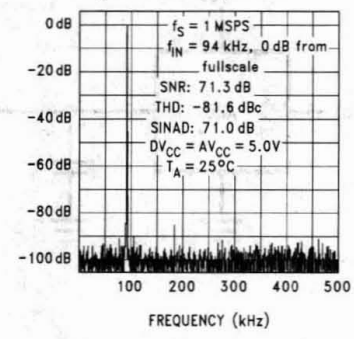
Conversion Time (t_{CONV}) vs Temperature



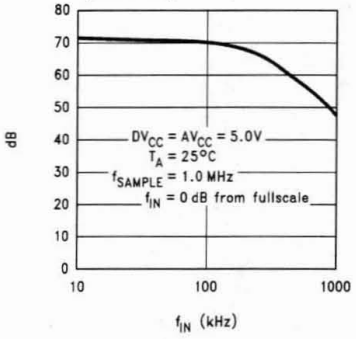
EOC Delay Time (t_{EOC}) vs Temperature



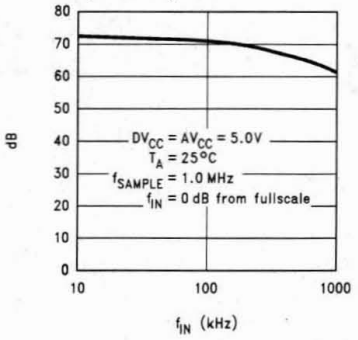
Spectral Response



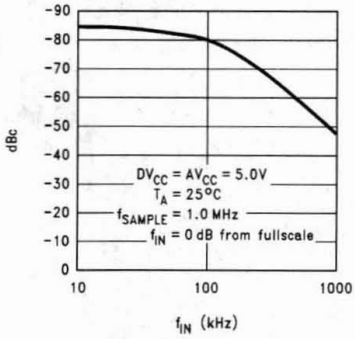
SINAD vs Input Frequency (ADC IN)



SNR vs Input Frequency (ADC IN)



THD vs Input Frequency (ADC IN)



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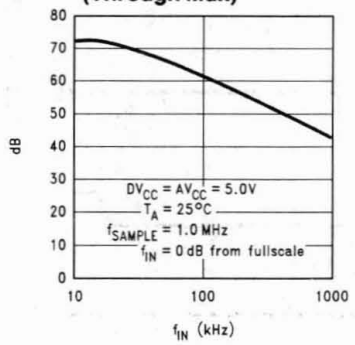
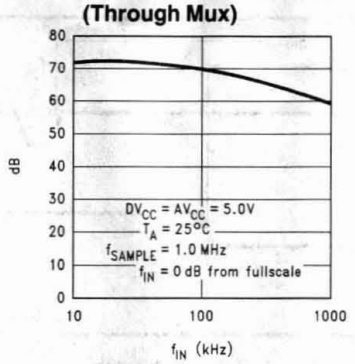
Typical Performance Characteristics (Continued)

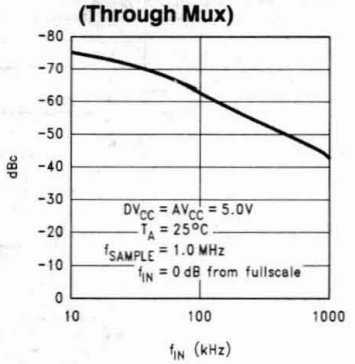
SINAD vs Input Frequency (Through Mux)



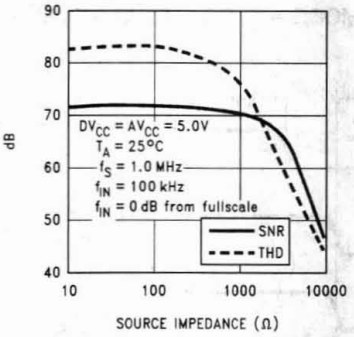
SNR vs Input Frequency (Through Mux)



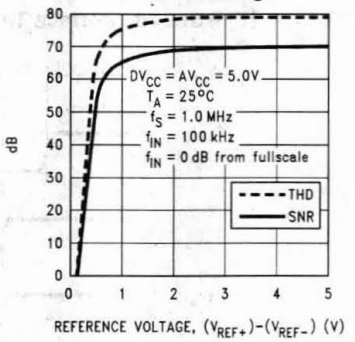
THD vs Input Frequency (Through Mux)



SNR and THD vs Source Impedance



SNR and THD vs Reference Voltage



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Timing Diagrams

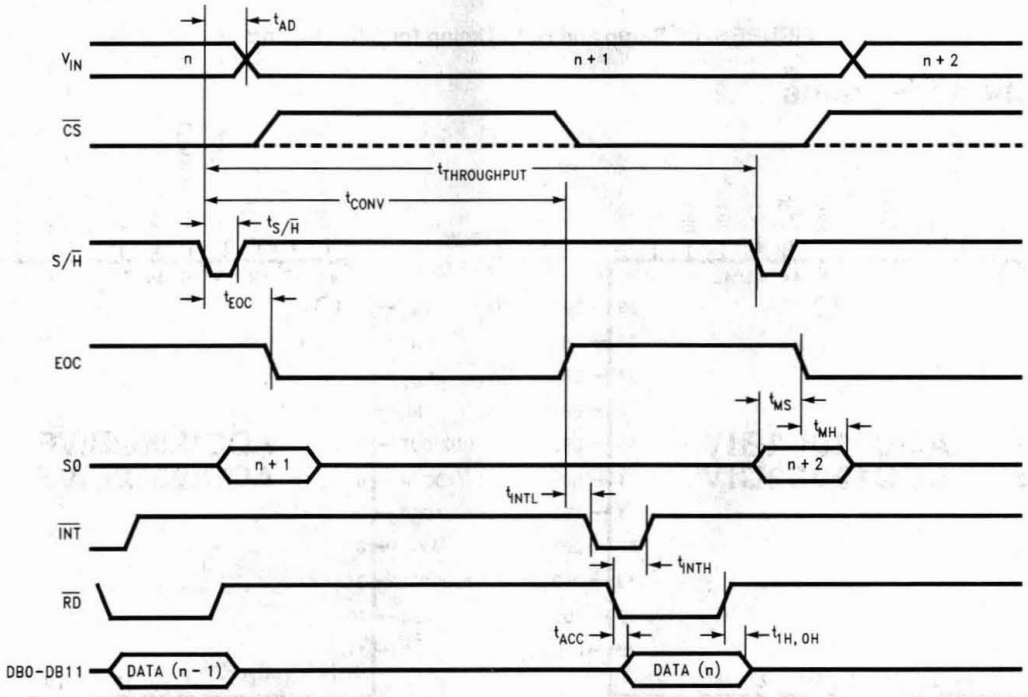

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FIGURE 1. Interrupt Interface Timing (MODE = 1, OE = 1)

Timing Diagrams (Continued)

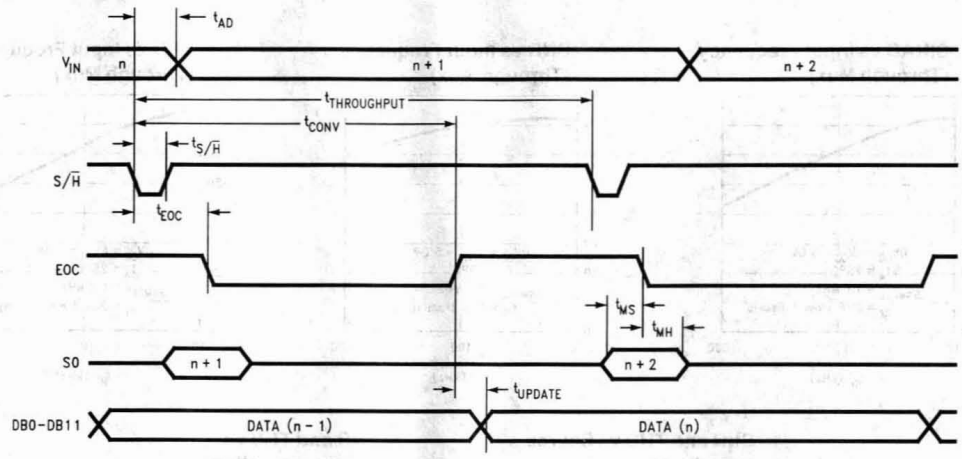

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FIGURE 2. High Speed Interface Timing (MODE = 1, OE = 1, $\overline{CS}$ = 0, $\overline{RD}$ = 0)

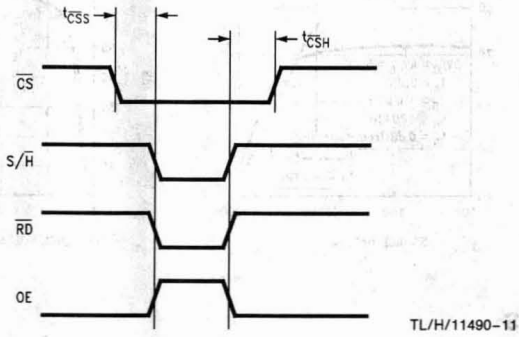

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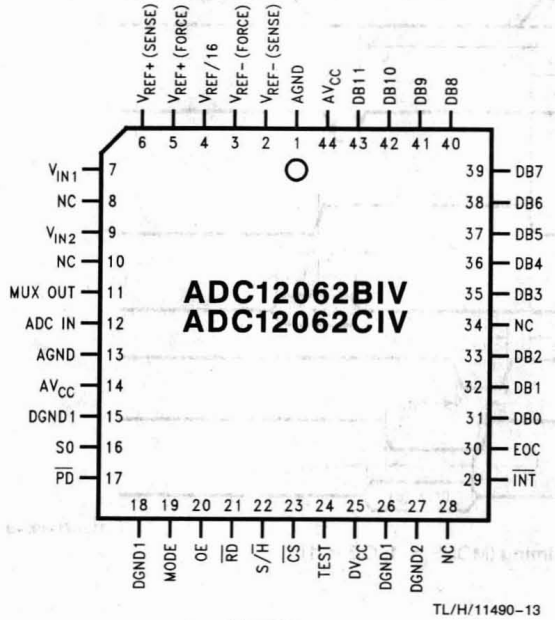
FIGURE 3. $\overline{CS}$ Setup and Hold Timing for $S/\overline{H}$, $\overline{RD}$, and OE

Connection Diagrams



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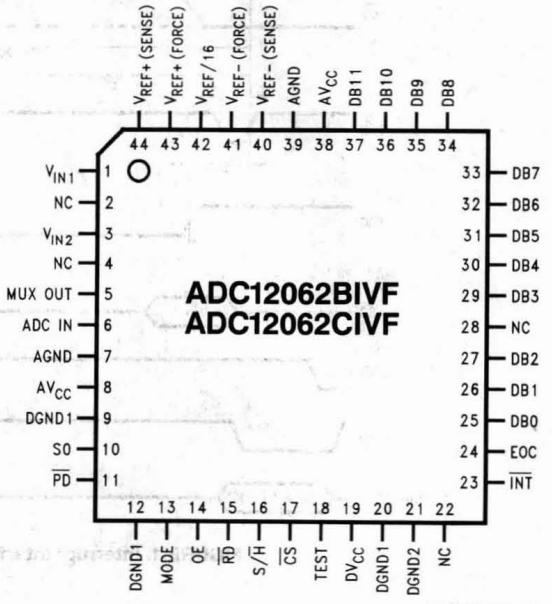
Top View



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Top View

Pin Descriptions

AV_{CC}	These are the two positive analog supply inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed to AGND with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.
DV_{CC}	This is the positive digital supply input. It should always be connected to the same voltage as the analog supply, AV_{CC}. It should be bypassed to DGND2 with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.
AGND, DGND1, DGND2	These are the power supply ground pins. There are separate analog and digital ground pins for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. All of the ground pins should be returned to the same potential. AGND is the analog ground for the converter. DGND1 is the ground pin for the digital control lines. DGND2 is the ground return for the output databus. See Section 6.0 LAYOUT AND GROUNDING for more information.
DB0–DB11	These are the TRI-STATE output pins, enabled by $\overline{RD}$, $\overline{CS}$, and OE.
V_{IN1}, V_{IN2}	These are the analog input pins to the multiplexer. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV below ground or 50 mV above V_{CC}.
MUX OUT	This is the output of the on-board analog input multiplexer.
ADC IN	This is the direct input to the 12-bit sampling A/D converter. For accurate conversions, this pin should not be driven more than 50 mV below AGND or 50 mV above AV_{CC}.
S0	This pin selects the analog input that will be connected to the ADC12062 during the conversion. The input is selected based on the state of S0 when EOC makes its high-to-low transition. Low selects V_{IN1}, high selects V_{IN2}.
MODE	This pin should be tied to DV_{CC}.
$\overline{CS}$	This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$, S/$\overline{H}$, and OE inputs. This pin can be tied low.
$\overline{INT}$	This is the active low Interrupt output. When using the Interrupt Interface Mode *(Figure 1)*, this output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. This output is always high when $\overline{RD}$ is held low *(Figure 2)*.
$\overline{EOC}$	This is the End-of-Conversion control output. This output is low during a conversion.
$\overline{RD}$	This is the active low Read control input. When $\overline{RD}$ is low (and $\overline{CS}$ is low), the $\overline{INT}$ output is reset and (if OE is high) data appears on the data bus. This pin can be tied low.
OE	This is the active high Output Enable control input. This pin can be thought of as an inverted version of the $\overline{RD}$ input (see *Figure 6*). Data output pins DB0–DB11 are TRI-STATE when OE is low. Data appears on DB0–DB11 only when OE is high and $\overline{CS}$ and $\overline{RD}$ are both low. This pin can be tied high.
S/$\overline{H}$	This is the Sample/$\overline{Hold}$ control input. The analog input signal is held and a new conversion is initiated by the falling edge of this control input (when $\overline{CS}$ is low).
$\overline{PD}$	This is the Power Down control input. This pin should be held high for normal operation. When this pin is pulled low, the device goes into a low power standby mode.
$V_{REF+(FORCE)}$, $V_{REF-(FORCE)}$	These are the positive and negative voltage reference force inputs, respectively. See Section 4, REFERENCE INPUTS, for more information.
$V_{REF+(SENSE)}$, $V_{REF-(SENSE)}$	These are the positive and negative voltage reference sense pins, respectively. See Section 4, REFERENCE INPUTS, for more information.
$V_{REF}/16$	This pin should be bypassed to AGND with a 0.1 μF ceramic capacitor.
TEST	This pin should be tied to DV_{CC}.

Functional Description

The ADC12062 performs a 12-bit analog-to-digital conversion using a 3 step flash technique. The first flash determines the six most significant bits, the second flash generates four more bits, and the final flash resolves the two least significant bits. *Figure 4* shows the major functional blocks of the converter. It consists of a 2½-bit Voltage Estimator, a resistor ladder with two different resolution voltage spans, a sample/hold capacitor, a 4-bit flash converter with front end multiplexer, a digitally corrected DAC, and a capacitive voltage divider.

The resistor string near the center of the block diagram in *Figure 4* generates the 6-bit and 10-bit reference voltages for the first two conversions. Each of the 16 resistors at the bottom of the string is equal to $1/1024$ of the total string resistance. These resistors form the **LSB Ladder*** and have a voltage drop of $1/1024$ of the total reference voltage ($V_{REF+} - V_{REF-}$) across each of them. The remaining resistors form the **MSB Ladder**. It is comprised of eight groups of eight resistors each connected in series (the lowest MSB ladder resistor is actually the entire LSB ladder). Each MSB Ladder section has $1/8$ of the total reference voltage across it. Within a given MSB ladder section, each of the eight MSB resistors has $1/64$ of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB ladders. The Comparator Multiplexer can connect any of these tap points, in two adjacent groups of eight, to the sixteen comparators shown at the right of *Figure 4*. This function provides the necessary reference voltages to the comparators during the first two flash conversions.

The six comparators, seven-resistor string (Estimator DAC ladder), and Estimator Decoder at the left of *Figure 4* form the Voltage Estimator. The Estimator DAC, connected between V_{REF+} and V_{REF-}, generates the reference voltages for the six Voltage Estimator comparators. The comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is used to control the placement of the Comparator Multiplexer, connecting the appropriate MSB ladder section to the sixteen flash comparators. A total of only 22 comparators (6 in the Voltage Estimator and 16 in the flash converter) is required to quantize the input to 6 bits, instead of the 64 that would be required using a traditional 6-bit flash.

Prior to a conversion, the Sample/Hold switch is closed, allowing the voltage on the S/H capacitor to track the input voltage. Switch 1 is in position 1. A conversion begins by opening the Sample/Hold switch and latching the output of the Voltage Estimator. The estimator decoder then selects two adjacent banks of tap points along the MSB ladder. These sixteen tap points are then connected to the sixteen flash converters. For example, if the input voltage is between $5/16$ and $7/16$ of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the sixteen tap points between $2/8$ and $4/8$ ($4/16$ and $8/16$) of V_{REF} and connects them to the sixteen comparators. The first flash conversion is now performed, producing the first 6 MSBs of data.

At this point, Voltage Estimator errors as large as $1/16$ of V_{REF} will be corrected since the comparators are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if $(7/16)V_{REF} < V_{IN} < (9/16)V_{REF}$, the Voltage Estimator's comparators tied to the tap points below $(9/16)V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The 16 comparators will be placed on the MSB ladder

*Note: The weight of each resistor on the LSB ladder is actually equivalent to four 12-bit LSBs. It is called the LSB ladder because it has the highest resolution of all the ladders in the converter.

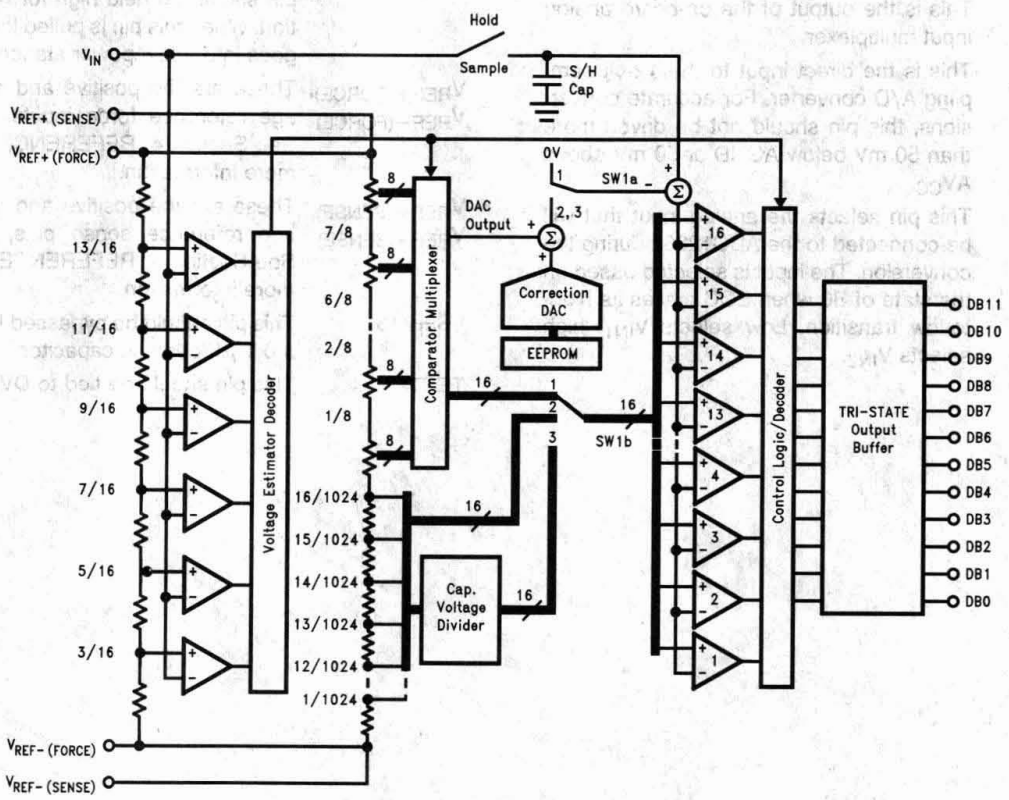

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FIGURE 4. Functional Block Diagram

Functional Description (Continued)

tap points between $(3/8)V_{REF}$ and $(5/8)V_{REF}$. This overlap of $(1/16)V_{REF}$ will automatically cancel a Voltage Estimator error of up to 256 LSBs. If the first flash conversion determines that the input voltage is between $(3/8)V_{REF}$ and $((4/8)V_{REF} - LSB/2)$, the Voltage Estimator's output code will be corrected by subtracting "1", resulting in a corrected value of "01" for the first two MSBs. If the first flash conversion determines that the input voltage is between $(4/8)V_{REF} - LSB/2)$ and $(5/8)V_{REF}$, the voltage estimator's output code is unchanged.

The results of the first flash and the Voltage Estimator's output are given to the factory-programmed on-chip EEPROM which returns a correction code corresponding to the error of the MSB ladder at that tap. This code is converted to a voltage by the Correction DAC. To generate the next four bits, SW1 is moved to position 2, so the ladder voltage and the correction voltage are subtracted from the input voltage. The remainder is applied to the sixteen flash converters and compared with the 16 tap points from the LSB ladder.

The result of this second conversion is accurate to 10 bits and describes the input remainder as a voltage between two tap points (V_H and V_L) on the LSB ladder. To resolve the last two bits, the voltage across the ladder resistor (between V_H and V_L) is divided up into 4 equal parts by the capacitive voltage divider, shown in *Figure 5*. The divider also creates 6 LSBs below V_L and 6 LSBs above V_H to provide overlap used by the digital error correction. SW1 is moved to position 3, and the remainder is compared with these 16 new voltages. The output is combined with the results of the Voltage Estimator, first flash, and second flash to yield the final 12-bit result.

By using the same sixteen comparators for all three flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard multi-step techniques.

Applications Information

1.0 MODES OF OPERATION

The ADC12062 has two interface modes: An interrupt/read mode and a high speed mode. *Figures 1* and *2* show the timing diagrams for these interfaces.

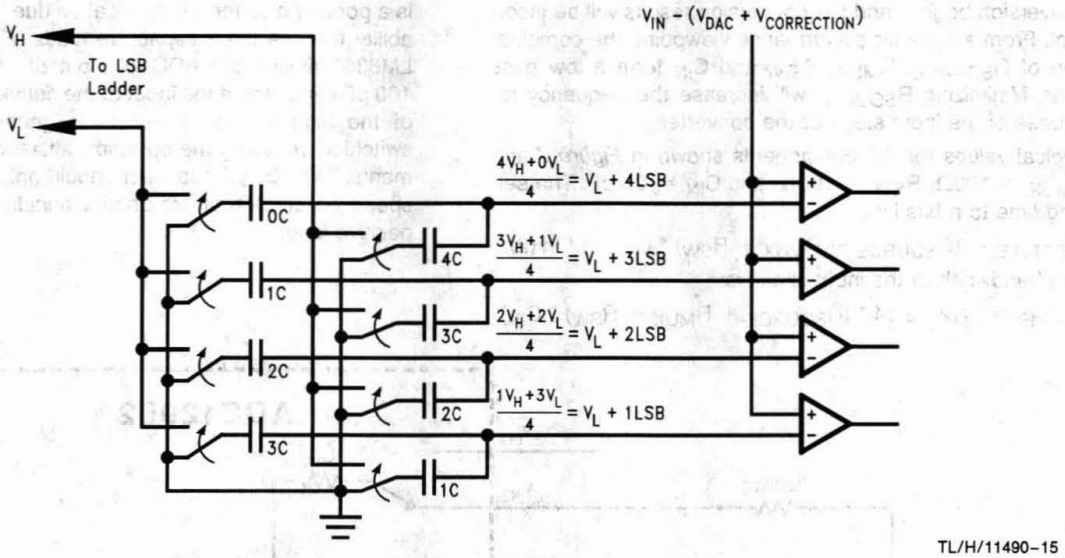
In order to clearly show the relationship between S/$\overline{H}$, $\overline{CS}$, $\overline{RD}$, and OE, the control logic decoding section of the ADC12062 is shown in *Figure 6*.

Interrupt Interface

As shown in *Figure 1*, the falling edge of S/$\overline{H}$ holds the input voltage and initiates a conversion. At the end of the conversion, the EOC output goes high and the $\overline{INT}$ output goes low, indicating that the conversion results are latched and may be read by pulling $\overline{RD}$ low. The falling edge of $\overline{RD}$ resets the $\overline{INT}$ line. Note that $\overline{CS}$ must be low to enable S/$\overline{H}$ or $\overline{RD}$.

High Speed Interface

This is the fastest interface, shown in *Figure 2*. Here the output data is always present on the databus, and the $\overline{INT}$ to $\overline{RD}$ delay is eliminated.



TL/H/11490–15

FIGURE 5. The Capacitive Voltage Divider

Applications Information (Continued)

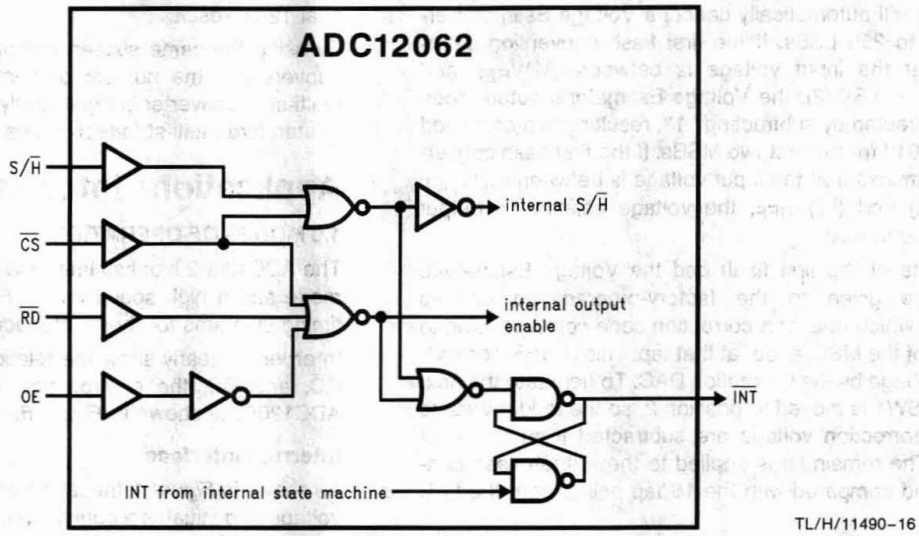


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FIGURE 6. ADC Control Logic

2.0 THE ANALOG INPUT

The analog input of the ADC12062 can be modeled as two small resistances in series with the capacitance of the input hold capacitor (C_{IN}), as shown in *Figure 7*. The S/H switch is closed during the Sample period, and open during Hold. The source has to charge C_{IN} to the input voltage within the sample period. Note that the source impedance of the input voltage (R_{SOURCE}) has a direct effect on the time it takes to charge C_{IN}. If R_{SOURCE} is too large, the voltage across C_{IN} will not settle to within 0.5 LSBs of V_{SOURCE} before the conversion begins, and the conversion results will be incorrect. From a dynamic performance viewpoint, the combination of R_{SOURCE}, R_{MUX}, R_{SW}, and C_{IN} form a low pass filter. Minimizing R_{SOURCE} will increase the frequency response of the input stage of the converter.

Typical values for the components shown in *Figure 7* are: $R_{MUX} = 100\Omega$, $R_{SW} = 100\Omega$, and $C_{IN} = 25$ pF. The settling time to n bits is:

$$t_{SETTLE} = (R_{SOURCE} + R_{MUX} + R_{SW}) * C_{IN} * n * \ln(2).$$

The bandwidth of the input circuit is:

$$f_{-3dB} = 1/(2 * 3.14 * (R_{SOURCE} + R_{MUX} + R_{SW}) * C_{IN})$$

For maximum performance, the impedance of the source driving the ADC12062 should be made as small as possible. A source impedance of 100Ω or less is recommended. A plot of dynamic performance vs. source impedance is given in the Typical Performance Characteristics section.

If the signal source has a high output impedance, its output should be buffered with an operational amplifier capable of driving a switched 25 pF/100Ω load. Any ringing or instabilities at the op amp's output during the sampling period can result in conversion errors. The LM6361 high speed op amp is a good choice for this application due to its speed and its ability to drive large capacitive loads. *Figure 8* shows the LM6361 driving the ADC IN input of an ADC12062. The 100 pF capacitor at the input of the converter absorbs some of the high frequency transients generated by the S/H switching, reducing the op amp transient response requirements. The 100 pF capacitor should only be used with high speed op amps that are unconditionally stable driving capacitive loads.

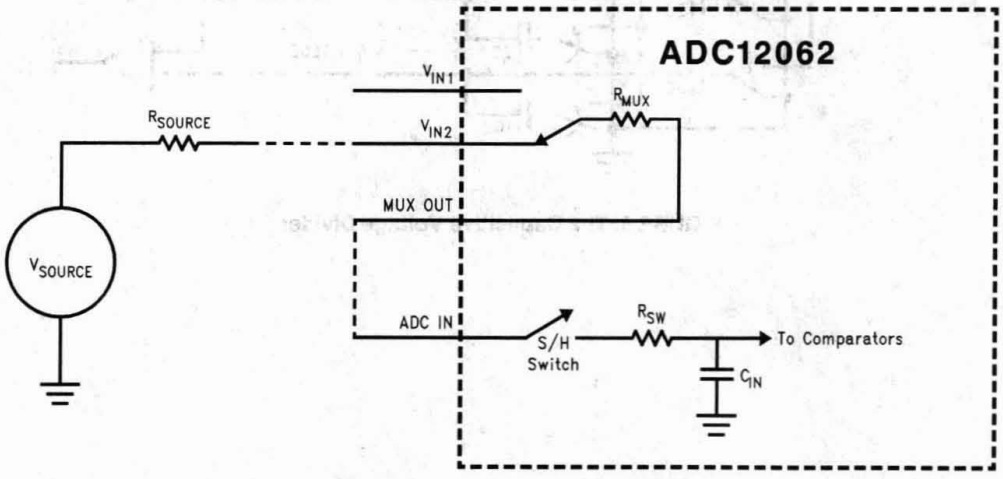

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FIGURE 7. Simplified ADC12062 Input Stage

Applications Information (Continued)

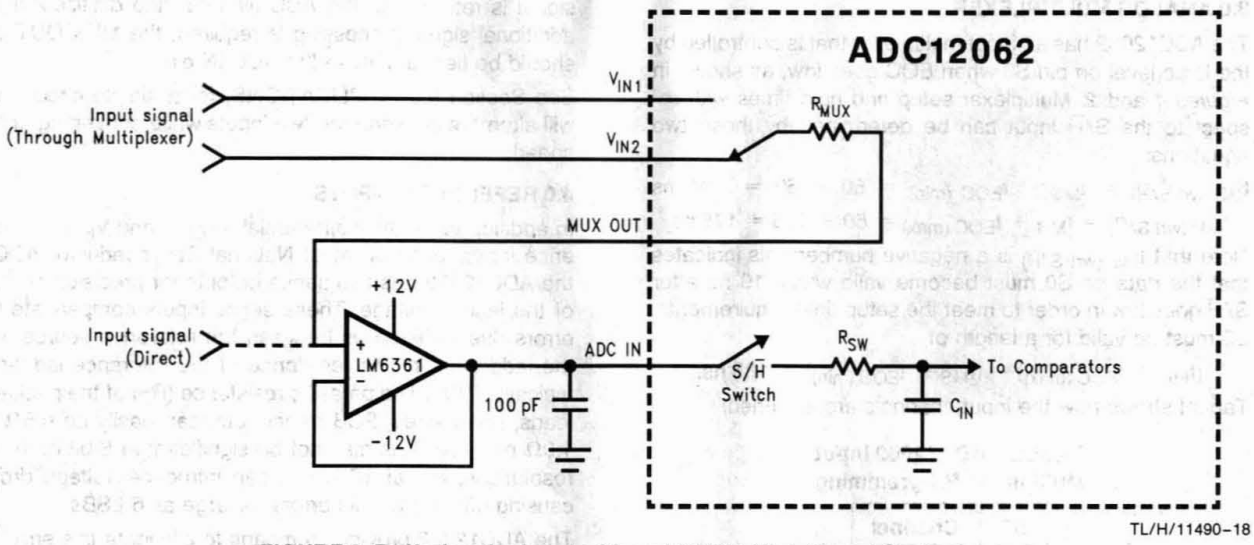

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FIGURE 8. Buffering the Input with an LM6361 High Speed Op Amp

Another benefit of using a high speed buffer is improved THD performance when using the multiplexer of the ADC12062. The MUX on-resistance is somewhat non-linear over input voltage, causing the RC time constant formed by C_{IN}, R_{MUX}, and R_{SW} to vary depending on the input voltage. This results in increasing THD with increasing frequency. Inserting the buffer between the MUX OUT and the ADC IN terminals as shown in *Figure 8* will eliminate the loading on R_{MUX}, significantly reducing the THD of the multiplexed system.

Correct converter operation will be obtained for input voltages greater than AGND − 50 mV and less than AV_{CC} + 50 mV. Avoid driving the signal source more than 300 mV higher than AV_{CC}, or more than 300 mV below AGND. If an analog input pin is forced beyond these voltages, the current flowing through that pin should be limited to 25 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 50 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits for any reason (unknown/uncontrollable input voltage range, power-on transients, fault conditions, etc.) some form of input protection, such as that shown in *Figure 9,* should be used.

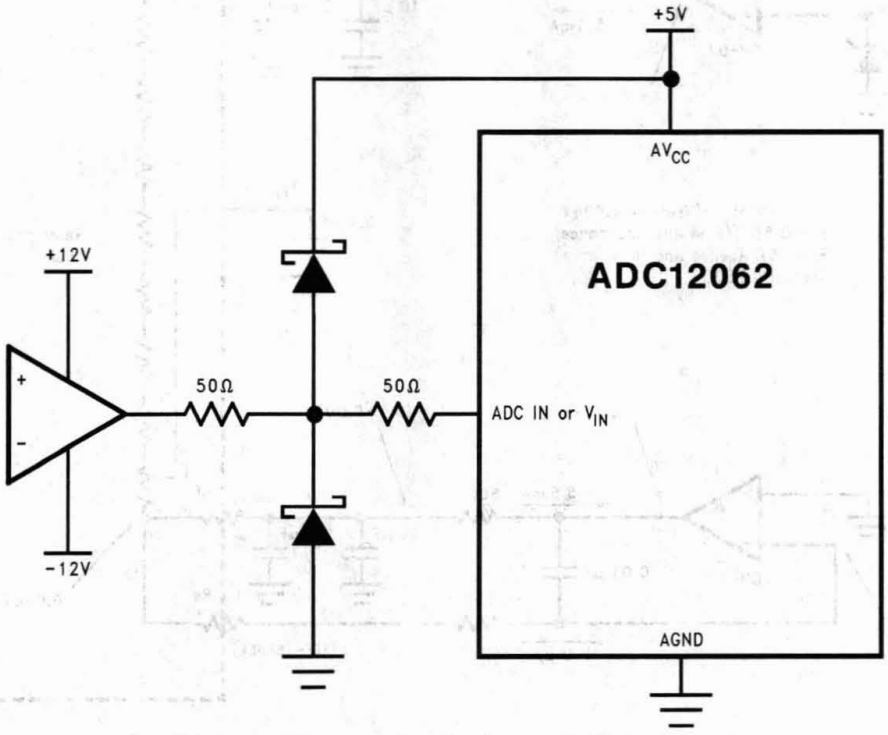

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FIGURE 9. Input Protection

Applications Information (Continued)

3.0 ANALOG MULTIPLEXER

The ADC12062 has an input multiplexer that is controlled by the logic level on pin S0 when EOC goes low, as shown in *Figures 1* and *2*. Multiplexer setup and hold times with respect to the S/$\overline{H}$ input can be determined by these two equations:

$t_{MS\ (wrt\ S/\overline{H})} = t_{MS} - t_{EOC\ (min)} = 50 - 60 = -10$ ns

$t_{MH\ (wrt\ S/\overline{H})} = t_{MH} + t_{EOC\ (max)} = 50 + 125 = 175$ ns

Note that $t_{MS\ (wrt\ S/\overline{H})}$ is a negative number; this indicates that the data on S0 must become valid within 10 ns after S/$\overline{H}$ goes low in order to meet the setup time requirements. S0 must be valid for a length of

$$(t_{MH} + t_{EOC\ (max)}) - (t_{MS} - t_{EOC\ (min)}) = 185\ \text{ns}.$$

Table I shows how the input channels are assigned:

TABLE I. ADC12062 Input Multiplexer Programming

S0	Channel
0	V_{IN1}
1	V_{IN2}

The output of the multiplexer is available to the user via the MUX OUT pin. This output allows the user to perform additional signal processing, such as filtering or gain, before the signal is returned to the ADC IN input and digitized. If no additional signal processing is required, the MUX OUT pin should be tied directly to the ADC IN pin.

See Section 9.0 (APPLICATIONS) for a simple circuit that will alternate between the two inputs while converting at full speed.

4.0 REFERENCE INPUTS

In addition to the fully differential V_{REF+} and V_{REF-} reference inputs used on most National Semiconductor ADCs, the ADC12062 has two sense outputs for precision control of the ladder voltage. These sense inputs compensate for errors due to IR drops between the reference source and the ladder itself. The resistance of the reference ladder is typically 750Ω. The parasitic resistance (R_P) of the package leads, bond wires, PCB traces, etc. can easily be 0.5Ω to 1.0Ω or more. This may not be significant at 8-bit or 10-bit resolutions, but at 12 bits it can introduce voltage drops causing offset and gain errors as large as 6 LSBs.

The ADC12062 provides a means to eliminate this error by bringing out two additional pins that sense the exact voltage at the top and bottom of the ladder. With the addition of two op amps, the voltages on these internal nodes can be forced to the exact value desired, as shown in *Figure 10*.

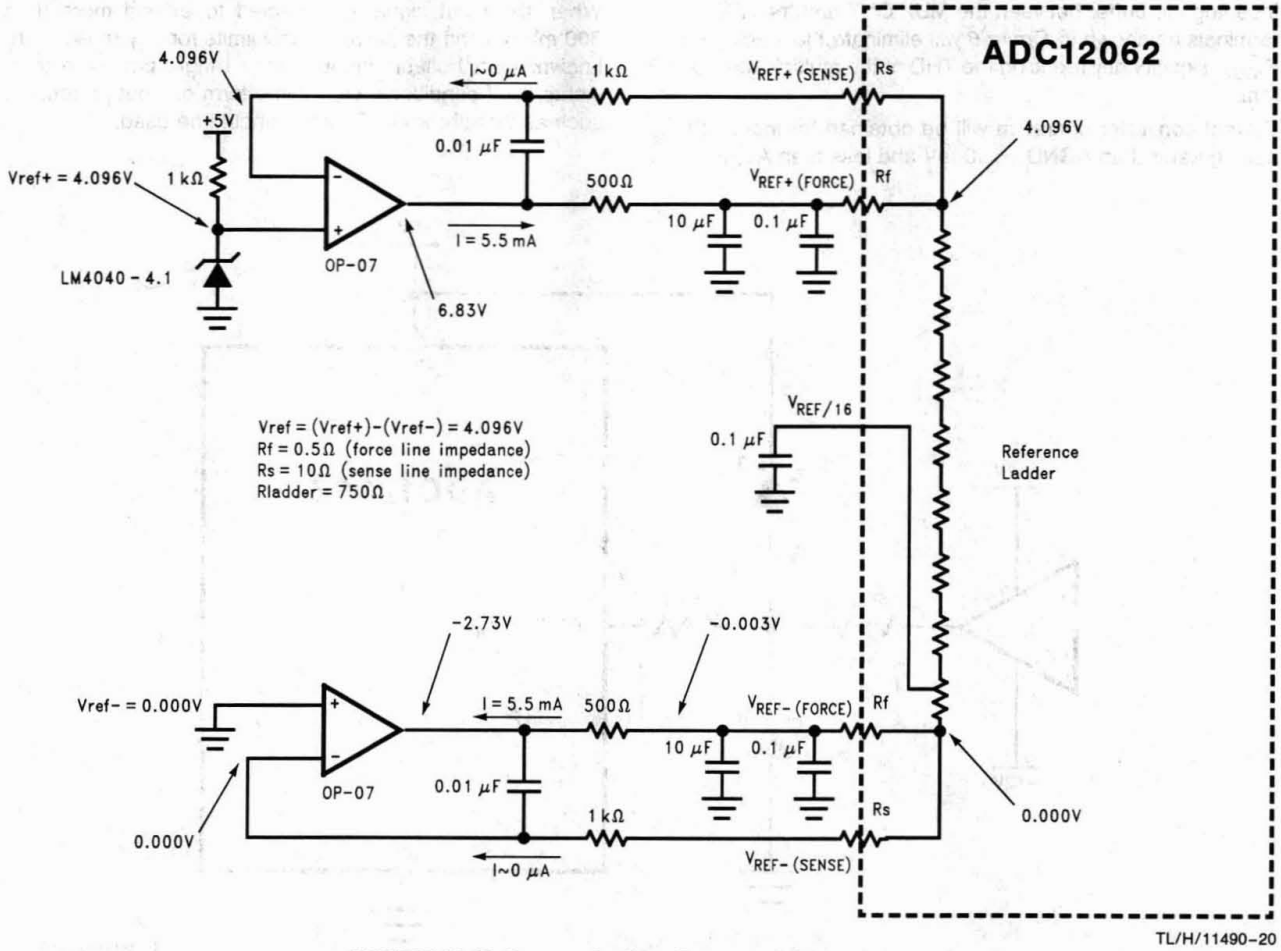

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FIGURE 10. Reference Ladder Force and Sense Inputs

Applications Information (Continued)

Since the current flowing through the SENSE lines is essentially zero, there is negligible voltage drop across R_S and the 1 kΩ resistor, so the voltage at the inverting input of the op amp accurately represents the voltage at the top (or bottom) of the ladder. The op amp drives the FORCE input and forces the voltage at the ends of the ladder to equal the voltage at the op amps's non-inverting input, plus or minus its input offset voltage. For this reason op amps with low V_{OS}, such as the LM627 or LM607, should be used for this application. When used in this configuration, the ADC12062 typically has less than 0.5 LSB of offset and gain error without any user adjustments.

The 0.1 μF and 10 μF capacitors on the force inputs provide high frequency decoupling of the reference ladder. The 500Ω force resistors isolate the op amps from this large capacitive load. The 0.01 μF/1 kΩ network provides zero phase shift at high frequencies to ensure stability. Note that the op amp supplies in this example must be ±10V to ±15V to meet the input/output voltage range requirements of the LM627 and supply the sub-zero voltage to the V_{REF-} (FORCE) pin. The $V_{REF/16}$ output should be bypassed to analog ground with a 0.1 μF ceramic capacitor.

The reference inputs are fully differential and define the zero to full-scale range of the input signal. They can be configured to span up to 5V (V_{REF-} = 0V, V_{REF+} = 5V), or they can be connected to different voltages (within the 0V to 5V limits) when other input spans are required. The ADC12062 is tested at V_{REF-} (SENSE) = 0V, V_{REF+} (SENSE) = 4.096V. Reducing the reference voltage span to less than 4V increases the sensitivity (reduces the LSB size) of the converter; however noise performance degrades when lower reference voltages are used. A plot of dynamic performance vs reference voltage is given in the Typical Performance Characteristics section.

If the converter will be used in an application where DC accuracy is secondary to dynamic performance, then a simpler reference circuit may suffice. The circuit shown in *Figure 11* will introduce several LSBs of offset and gain error, but INL, DNL, and all dynamic specifications will be unaffected.

All bypass capacitors should be located as close to the ADC12062 as possible to minimize noise on the reference ladder. The $V_{REF/16}$ output should be bypassed to analog ground with a 0.1 μF ceramic capacitor.

The LM4040 shunt voltage reference is available with a 4.096V output voltage. With initial accuracies as low as ±0.1%, it makes an excellent reference for the ADC12062.

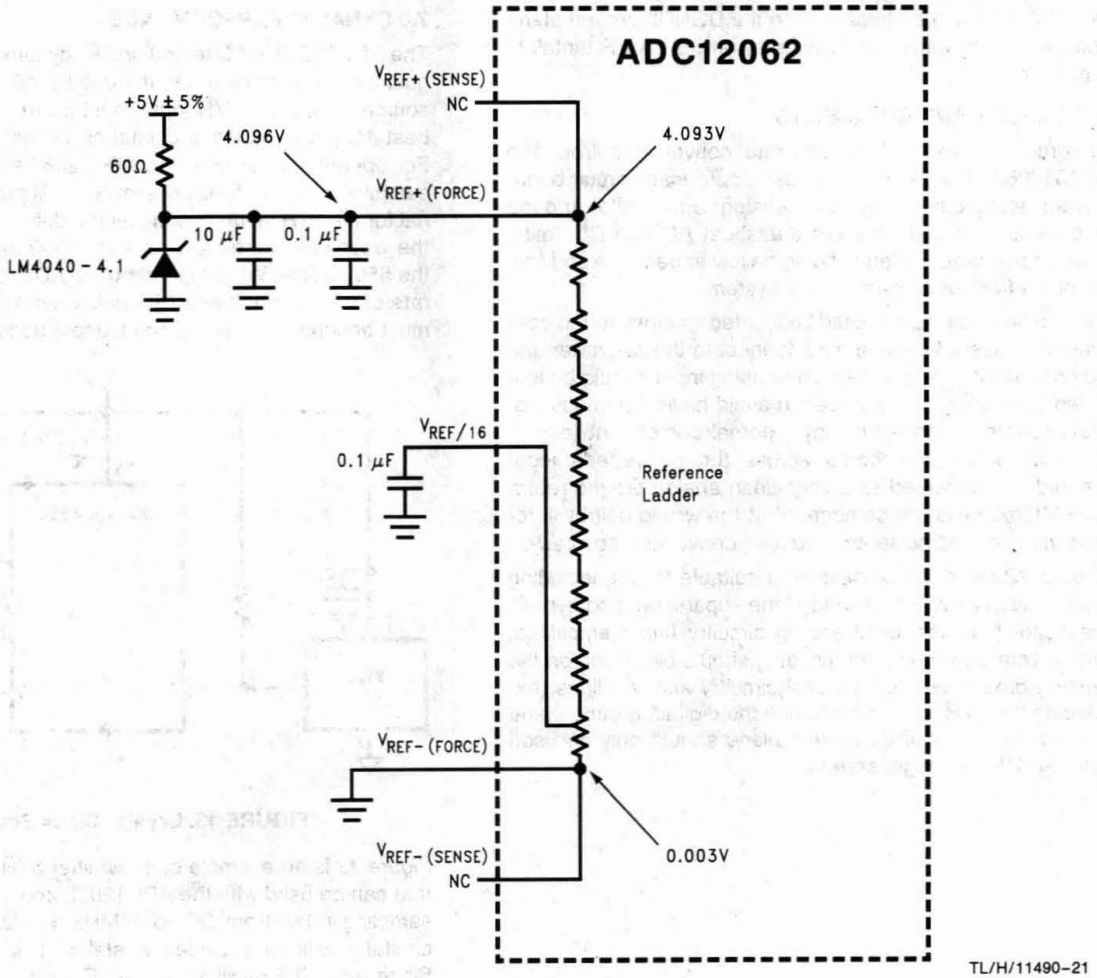

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FIGURE 11. Using the V_{REF} Force Pins Only

Applications Information (Continued)

5.0 POWER SUPPLY CONSIDERATIONS

The ADC12062 is designed to operate from a single +5V power supply. There are two analog supply pins (AV_{CC}) and one digital supply pin (DV_{CC}). These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee proper operation of the converter, all three supply pins should be connected to the same voltage source. In systems with separate analog and digital supplies, the converter should be powered from the analog supply.

The ground pins are AGND (analog ground), DGND1 (digital input ground), and DGND2 (digital output ground). These pins allow for three separate ground planes for these sections of the chip. Isolating the analog section from the two digital sections reduces digital interference in the analog circuitry, improving the dynamic performance of the converter. Separating the digital outputs from the digital inputs (particularly the S/$\overline{H}$ input) reduces the possibility of ground bounce from the 12 data lines causing jitter on the S/$\overline{H}$ input. The analog ground plane should be connected to the Digital2 ground plane at the ground return for the power supply. The Digital1 ground plane should be tied to the Digital2 ground plane at the DGND1 and DGND2 pins.

Both AV_{CC} pins should be bypassed to the AGND ground plane with 0.1 μF ceramic capacitors. One of the two AV_{CC} pins should also be bypassed with a 10 μF tantalum capacitor. DV_{CC} should be bypassed to the DGND2 ground plane with a 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor.

6.0 LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC12062, it is necessary to use appropriate circuit board layout techniques. Separate analog and digital ground planes are required to meet datasheet AC and DC limits. The analog ground plane should be low-impedance and free of noise from other parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean analog ground return point. Grounding the component at the wrong point will result in increased noise and reduced conversion accuracy.

Figure 12 gives an example of a suitable layout, including power supply routing, ground plane separation, and bypass capacitor placement. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on the analog ground plane. All digital circuitry and I/O lines (excluding the S/$\overline{H}$ input) should use the digital2 ground plane as ground. The digital1 ground plane should only be used for the S/$\overline{H}$ signal generation.

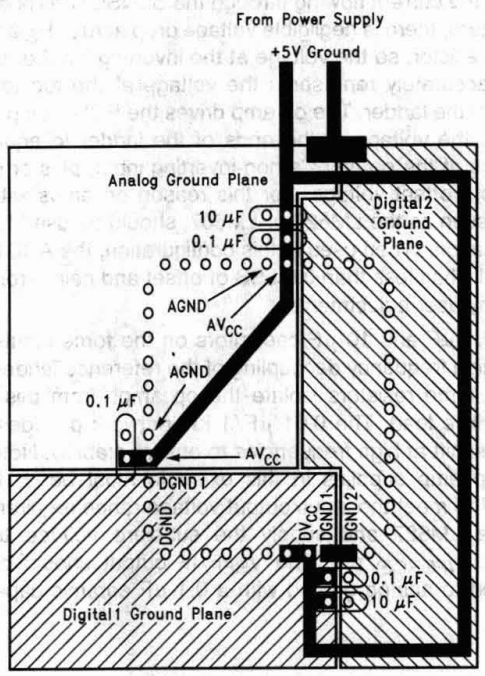

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FIGURE 12. PC Board Layout

7.0 DYNAMIC PERFORMANCE

The ADC12062 is AC tested and its dynamic performance is guaranteed. In order to meet these specifications, the clock source driving the S/$\overline{H}$ input must be free of jitter. For the best AC performance, a crystal oscillator is recommended. For operation at or near the ADC12062's 1 MHz maximum sampling rate, a 1 MHz squarewave will provide a good signal for the S/$\overline{H}$ input. As long as the duty cycle is near 50%, the waveform will be low for about 500 ns, which is within the 550 ns limit. When operating the ADC12062 at a sample rate of 910 kHz or below, the pulse width of the S/$\overline{H}$ signal must be smaller than half the sample period.

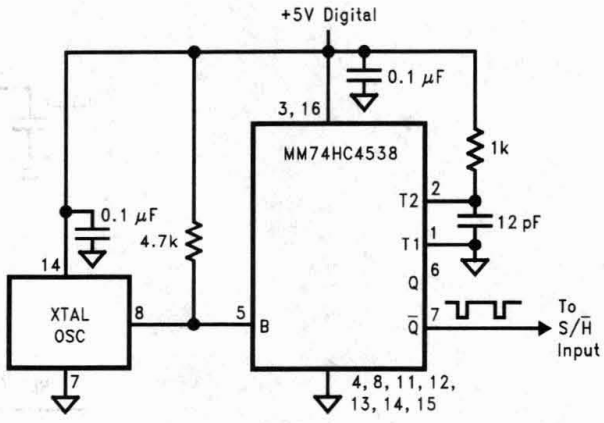

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FIGURE 13. Crystal Clock Source

Figure 13 is an example of a low jitter S/$\overline{H}$ pulse generator that can be used with the ADC12062 and allow operation at sampling rates from DC to 1 MHz. A standard 4-pin DIP crystal oscillator provides a stable 1 MHz squarewave. Since most DIP oscillators have TTL outputs, a 4.7k pullup resistor is used to raise the output high voltage to CMOS input levels. The output is fed to the trigger input (falling

Applications Information (Continued)

edge) of an MM74HC4538 one-shot. The 1k resistor and 12 pF capacitor set the pulse length to approximately 100 ns. The S/$\overline{H}$ pulse stream for the converter appears on the Q output of the HC4538. This is the S/$\overline{H}$ clock generator used on the ADC12062EVAL evaluation board. For lower power, a CMOS inverter-based crystal oscillator can be used in place of the DIP crystal oscillator. See Application Note AN-340 in the National Semiconductor CMOS Logic Databook for more information on CMOS crystal oscillators.

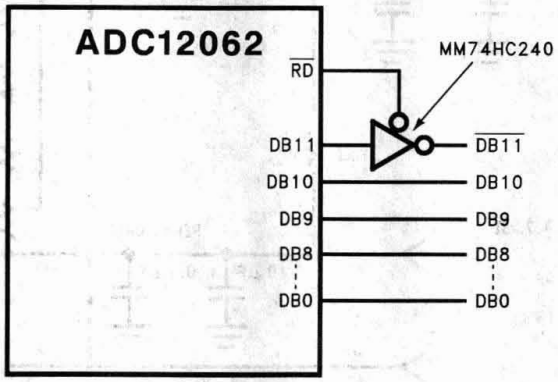
8.0 COMMON APPLICATION PITFALLS

Driving inputs (analog or digital) outside power supply rails. The Absolute Maximum Ratings state that all inputs must be between GND − 300 mV and V_{CC} + 300 mV. This rule is most often broken when the power supply to the converter is turned off, but other devices connected to it (op amps, microprocessors) still have power. Note that if there is no power to the converter, DGND = AGND = DV_{CC} = AV_{CC} = 0V, so all inputs should be within ±300 mV of AGND and DGND.

Driving a high capacitance digital data bus. The more capacitance the data bus has to charge for each conversion, the more instantaneous digital current required from DV_{CC} and DGND. These large current spikes can couple back to the analog section, decreasing the SNR of the converter. While adequate supply bypassing and separate analog and digital ground planes will reduce this problem, buffering the digital data outputs (with a pair of MM74HC541s, for example) may be necessary if the converter must drive a heavily loaded databus.

9.0 APPLICATIONS

2's Complement Output



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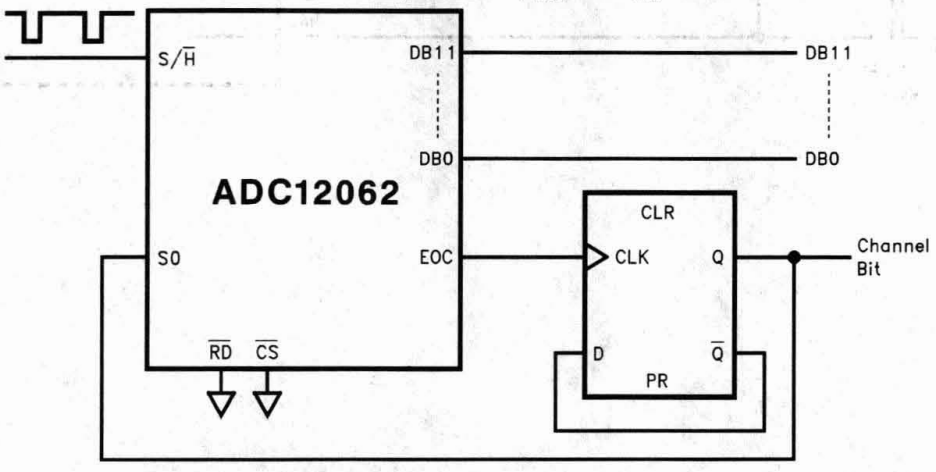
Ping-Ponging between V_{IN1} and V_{IN2}



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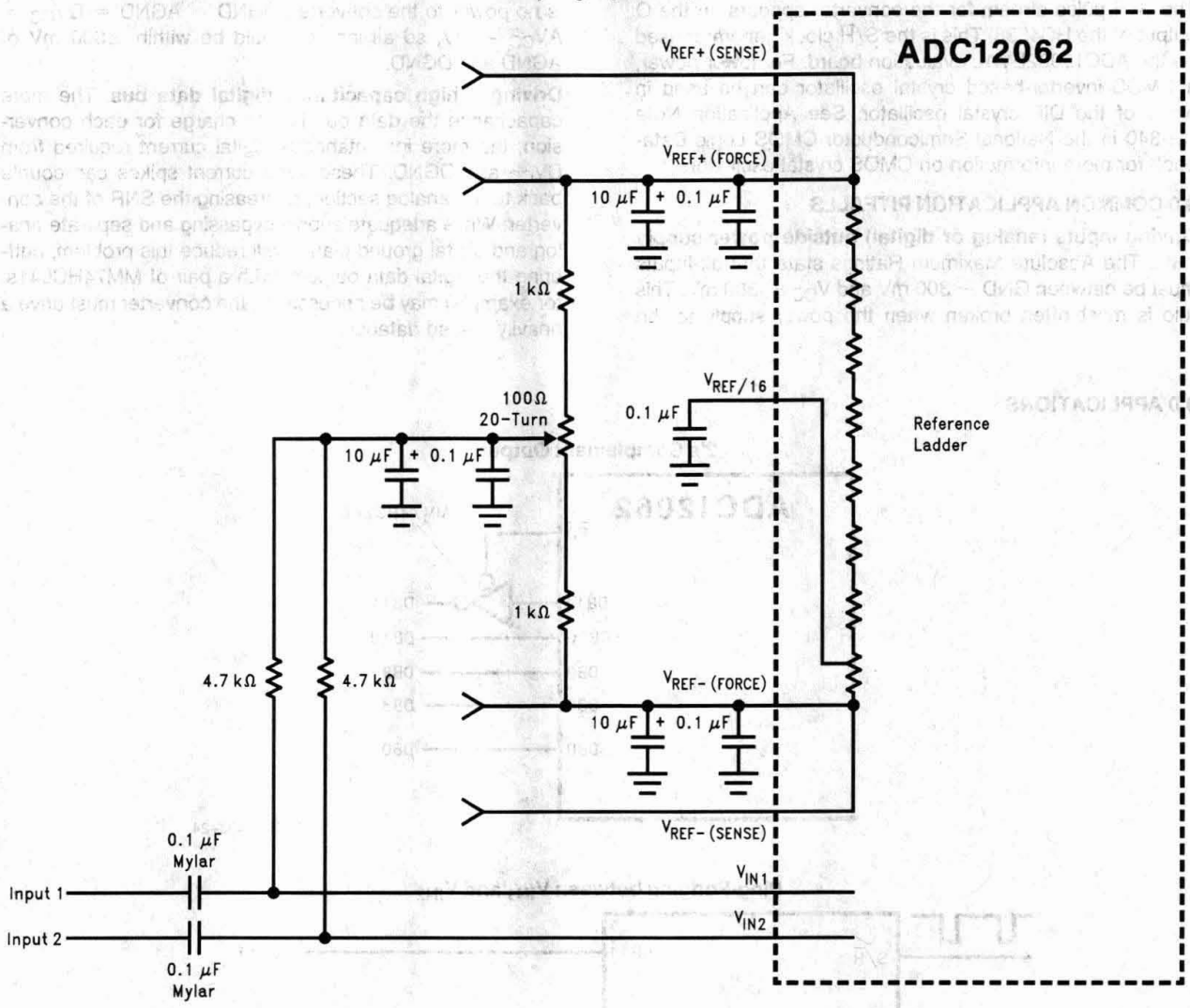
Applications Information (Continued)

AC Coupling Bipolar Inputs



TL/H/11490–26

National Semiconductor

ADC12662
12-Bit, 1.5 MHz, 200 mW A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative multistep conversion technique, the 12-bit ADC12662 CMOS analog-to-digital converter digitizes signals at a 1.5 MHz sampling rate while consuming a maximum of only 200 mW on a single +5V supply. The ADC12662 performs a 12-bit conversion in three lower-resolution "flash" conversions, yielding a fast A/D without the cost and power dissipation associated with true flash approaches.

The analog input voltage to the ADC12662 is tracked and held by an internal sampling circuit, allowing high frequency input signals to be accurately digitized without the need for an external sample-and-hold circuit. The ADC12662 feature two sample-and-hold/flash comparator sections which allow the converter to acquire one sample while converting the previous. This pipelining technique increases conversion speed without sacrificing performance. The multiplexer output is available to the user in order to perform additional external signal processing before the signal is digitized.

When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 250 μW.

Features

- Built-in sample-and-hold
- Single +5V supply
- Single channel or 2 channel multiplexer operation
- Low Power Standby mode

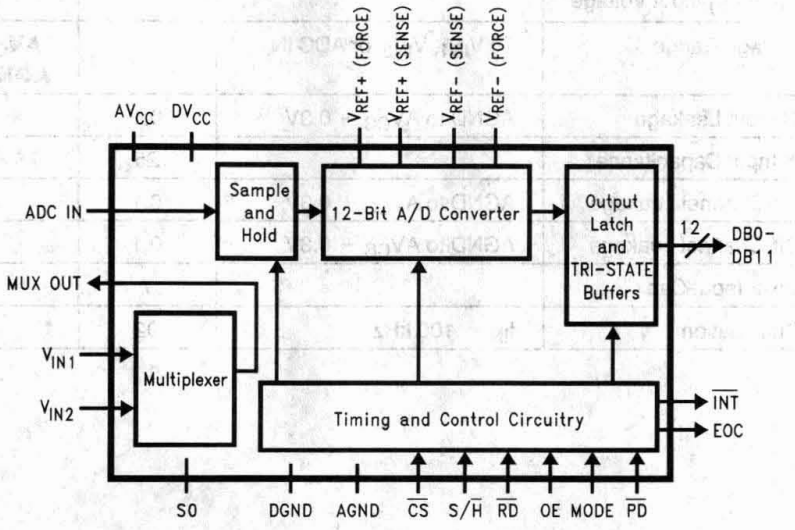
Key Specifications

■ Sampling rate	1.5 MHz (min)
■ Conversion time	580 ns (typ)
■ Signal-to-Noise Ratio, f_{IN} = 100 kHz	67.5 dB (min)
■ Power dissipation (f_s = 1.5 MHz)	200 mW (max)
■ No missing codes over temperature	Guaranteed

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications
- Waveform digitizers

ADC12662 Block Diagram



TL/H/11876–1

Ordering Information

Industrial ($-40°C \le T_A \le +85°$)	Package
ADC12662CIV	V44 Plastic Leaded Chip Carrier
ADC12662CIVF	VGZ44A Plastic Quad Flat Package
ADC12062EVAL	Evaluation Board

2

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	−0.3V to +6V
Voltage at Any Input or Output	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 3)	25 mA
Package Input Current (Note 3)	50 mA
Power Dissipation (Note 4)	
ADC12662CIV	875 mW
ESD Susceptibility (Note 5)	2000V
Soldering Information (Note 6)	
V Package, Infrared, 15 seconds	+300°C
VF Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_{JMAX})	150°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12662CIV, ADC12662CIVF	$-40°C \le T_A \le +85°C$
Supply Voltage Range (DV_{CC} = AV_{CC})	4.75V to 5.25V

Converter Characteristics

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limit)
	Resolution			**12**	Bits
	Differential Linearity Error	**T_{MIN} to T_{MAX}**	±0.4	**±0.95**	LSB (max)
	Integral Linearity Error (Note 9)	**T_{MIN} to T_{MAX}**	±0.4	**±1.5**	LSB (max)
	Offset Error	**T_{MIN} to T_{MAX}**	±0.3	**±2.0**	LSB (max)
	Full-Scale Error	**T_{MIN} to T_{MAX}**	±0.3	**±1.5**	LSB (max)
	Power Supply Sensitivity (Note 15)	DV_{CC} = AV_{CC} = 5V ±5%		**±0.75**	LSB (max)
R_{REF}	Reference Resistance		750	**500** **1000**	Ω (min) Ω (max)
$V_{REF(+)}$	$V_{REF+(SENSE)}$ Input Voltage			**AV_{CC}**	V (max)
$V_{REF(-)}$	$V_{REF-(SENSE)}$ Input Voltage			**AGND**	V (min)
V_{IN}	Input Voltage Range	To V_{IN1}, V_{IN2}, or ADC IN		**AV_{CC} + 0.05V** **AGND − 0.05V**	V (max) V (min)
	ADC IN Input Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	µA (max)
C_{ADC}	ADC IN Input Capacitance		25		pF
	MUX On-Channel Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	µA (max)
	MUX Off-Channel Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	µA (max)
C_{MUX}	Multiplexer Input Cap		7		pF
	MUX Off Isolation	f_{IN} = 100 kHz	92		dB

Dynamic Characteristics

(Note 10) The following specifications apply for $DV_{CC} = AV_{CC} = +5V$, $V_{REF+(SENSE)} = +4.096V$, $V_{REF-(SENSE)} = AGND$, $R_S = 25\Omega$, $f_{IN} = 100$ kHz, 0 dB from fullscale, and $f_s = 1.5$ MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limit)
SINAD	Signal-to-Noise Plus Distortion Ratio	**T_{MIN} to T_{MAX}**	70	**67.0**	dB (min)
SNR	Signal-to-Noise Ratio (Note 11)	**T_{MIN} to T_{MAX}**	70	**67.5**	dB (min)
THD	Total Harmonic Distortion (Note 12)	**T_{MIN} to T_{MAX}**	−80	**−70**	dBc (max)
ENOB	Effective Number of Bits (Note 13)	**T_{MIN} to t_{MAX}**	11.3	**10.8**	Bits (min)
IMD	Intermodulation Distortion	$f_{IN} = 88.7$ kHz, 89.5 kHz	−80		dBc

DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5V$, $V_{REF+(SENSE)} = +4.096V$, $V_{REF-(SENSE)} = AGND$, and $f_s = 1.5$ MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage	$DV_{CC} = AV_{CC} = +5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$DV_{CC} = AV_{CC} = +4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current		0.1	**1.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current		0.1	**1.0**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$DV_{CC} = AV_{CC} = +4.5V$, $I_{OUT} = -360$ μA $I_{OUT} = -100$ μA		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$DV_{CC} = AV_{CC} = +4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Leakage Current	Pins DB0–DB11	0.1	**3**	μA (max)
C_{OUT}	TRI-STATE Output Capacitance	Pins DB0–DB11	5		pF
C_{IN}	Digital Input Capacitance		4		pF
DI_{CC}	DV_{CC} Supply Current		2	**3**	mA (max)
AI_{CC}	AV_{CC} Supply Current		32	**37**	mA (max)
$I_{STANDBY}$	Standby Current ($DI_{CC} + AI_{CC}$)	$\overline{PD} = 0V$	50		μA

2

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5V$, $V_{REF+(SENSE)} = +4.096V$, $V_{REF-(SENSE)} = AGND$, and $f_S = 1.5$ MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typ (Note 7)	Limit (Note 8)	Units (Limits)
f_S	Maximum Sampling Rate ($1/t_{THROUGHPUT}$)			**1.5**	MHz (min)
t_{CONV}	Conversion Time (S/$\overline{H}$ Low to EOC High)		580	**510** **660**	ns (min) ns (max)
t_{AD}	Aperture Delay (S/$\overline{H}$ Low to Input Voltage Held)		20		ns
$t_{S/\overline{H}}$	S/$\overline{H}$ Pulse Width		10	**5** **400**	ns (min) ns (max)
t_{EOC}	S/$\overline{H}$ Low to EOC Low		90	**60** **126**	ns (min) ns (max)
t_{ACC}	Access Time ($\overline{RD}$ Low or OE High to Data Valid)	$C_L = 100$ pF	10	**20**	ns (max)
t_{1H}, t_{0H}	TRI-STATE® Control ($\overline{RD}$ High or OE Low to Databus TRI-STATE)	$R_L = 1k$, $C_L = 10$ pF	25	**40**	ns (max)
$t_{\overline{INT}H}$	Delay from $\overline{RD}$ Low to $\overline{INT}$ High	$C_L = 100$ pF	35	**60**	ns (max)
$t_{\overline{INT}L}$	Delay from EOC High to $\overline{INT}$ Low	$C_L = 100$ pF	−25	**−35** **−10**	ns (min) ns (max)
t_{UPDATE}	EOC High to New Data Valid		5	**15**	ns (max)
t_{MS}	Multiplexer Address Setup Time (MUX Address Valid to EOC Low)			**50**	ns (min)
t_{MH}	Multiplexer Address Hold Time (EOC Low to MUX Address Invalid)			**50**	ns (min)
$t_{\overline{CS}S}$	$\overline{CS}$ Setup Time ($\overline{CS}$ Low to $\overline{RD}$ Low, S/$\overline{H}$ Low, or OE High)			**20**	ns (min)
$t_{\overline{CS}H}$	$\overline{CS}$ Hold Time ($\overline{CS}$ High after $\overline{RD}$ High, S/$\overline{H}$ High, or OE Low)			**20**	ns (min)
t_{WU}	Wake-Up Time ($\overline{PD}$ High to First S/$\overline{H}$ Low)		1		μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND (GND = AGND = DGND), unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25 mA or less. The 50 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. θ_{JA} for the V (PLCC) package is 55°C/W. θ_{JA} for the VF (PQFP) package is 62°C/W. In most cases the maximum derated power dissipation will be reached only during fault conditions.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model ESD rating is 200V.

Note 6: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Typicals are at +25°C and represent most likely parametric norm.

Note 8: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Integral Linearity Error is the maximum deviation from a straight line between the *measured* offset and full scale endpoints.

Note 10: Dynamic testing of the ADC12662 is done using the ADC IN input. The input multiplexer adds harmonic distortion at high frequencies. See the graph in the Typical Performance Characteristics section for a typical graph of THD performance vs input frequency with and without the input multiplexer.

Note 11: The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.

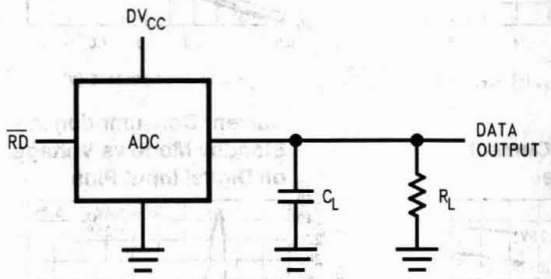
Note 12: The contributions from the first nine harmonics are used in the calculation of the THD.

Note 13: Effective Number of Bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation ENOB = (SINAD − 1.76)/6.02.

Note 14: The digital power supply current takes up to 10 seconds to decay to its final value after PD is pulled low. This prohibits production testing of the standby current. Some parts may exhibit significantly higher standby currents than the 50 μA typical.

Note 15: Power Supply Sensitivity is defined as the change in the Offset Error or the Full Scale Error due to a change in the supply voltage.

TRI-STATE Test Circuit and Waveforms



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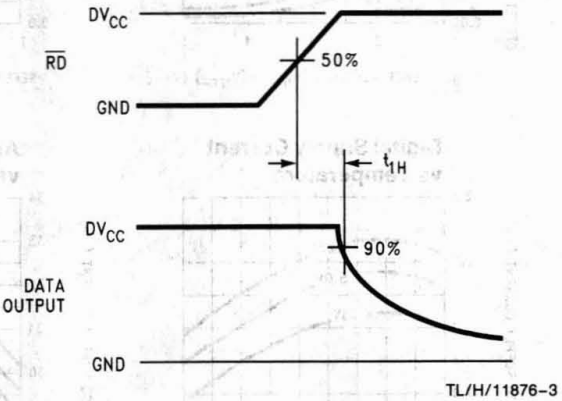
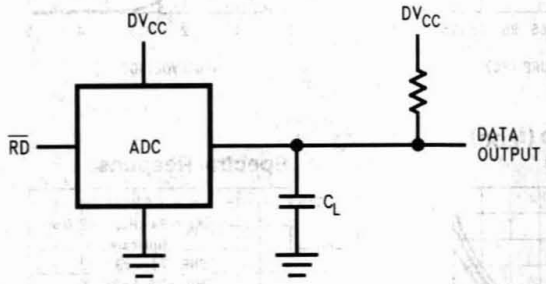


TL/H/11876–3



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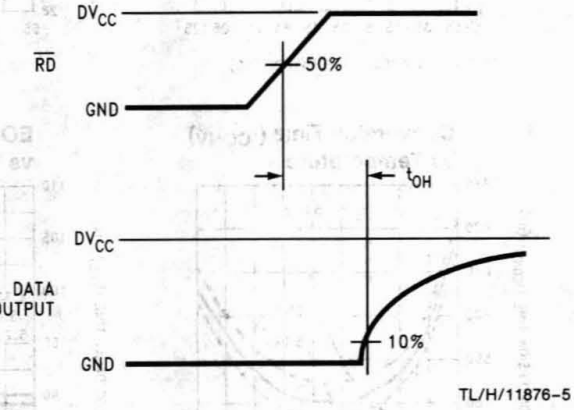

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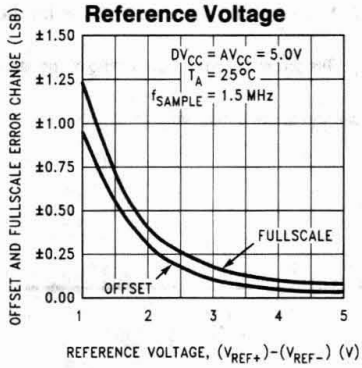
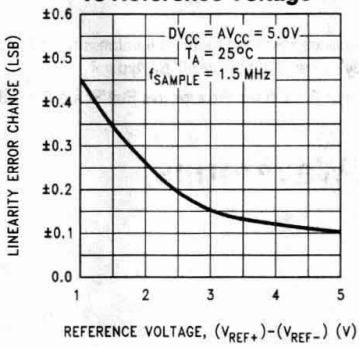
Typical Performance Characteristics

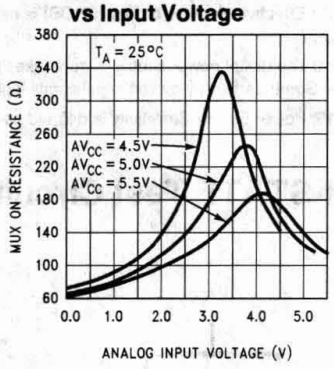
Offset and Fullscale Error Change vs Reference Voltage



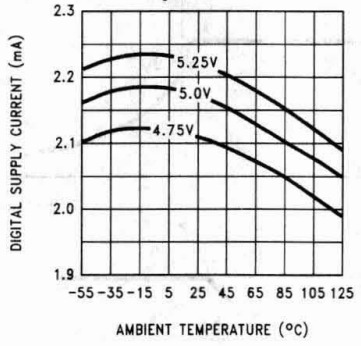
Linearity Error Change vs Reference Voltage



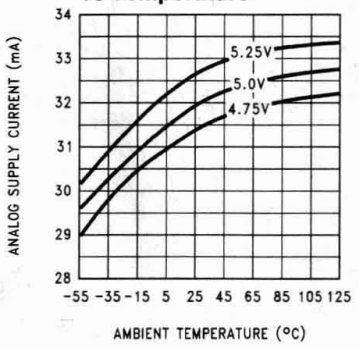
Mux ON Resistance vs Input Voltage



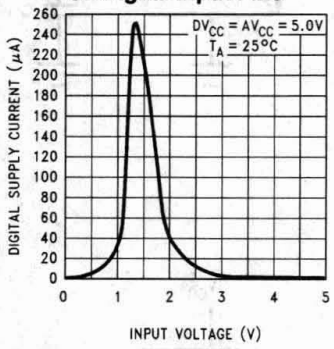
Digital Supply Current vs Temperature



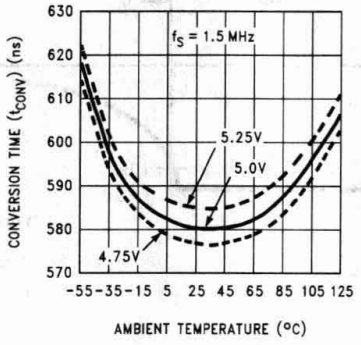
Analog Supply Current vs Temperature



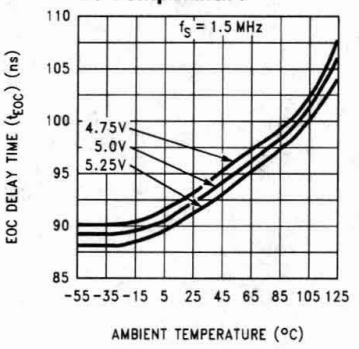
Current Consumption in Standby Mode vs Voltage on Digital Input Pins



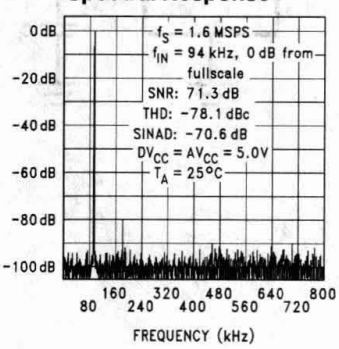
Conversion Time (t_{CONV}) vs Temperature



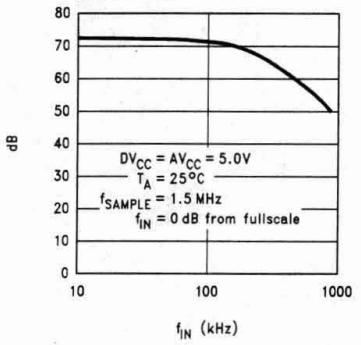
EOC Delay Time (t_{EOC}) vs Temperature



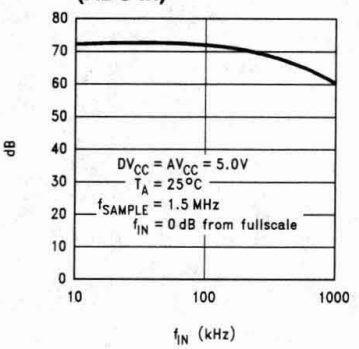
Spectral Response



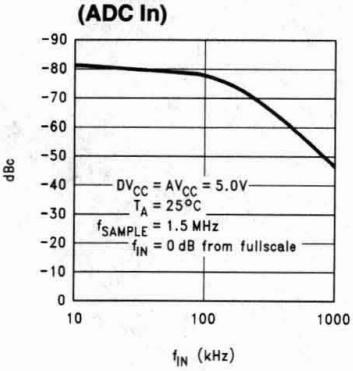
SINAD vs Input Frequency (ADC In)



SNR vs Input Frequency (ADC In)



THD vs Input Frequency (ADC In)



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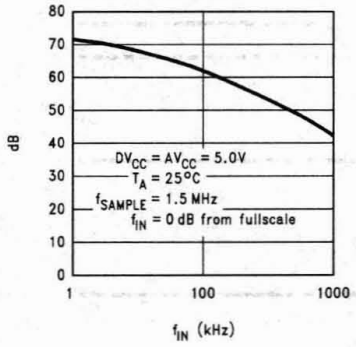
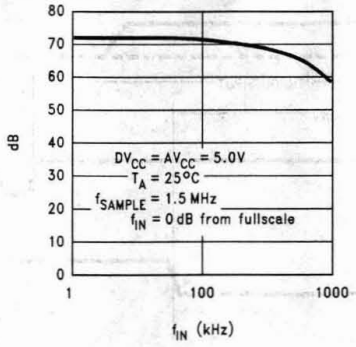
Typical Performance Characteristics (Continued)

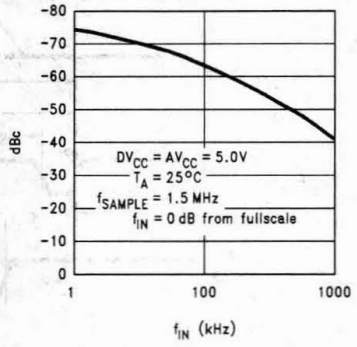
SINAD vs Input Frequency (Through Mux)



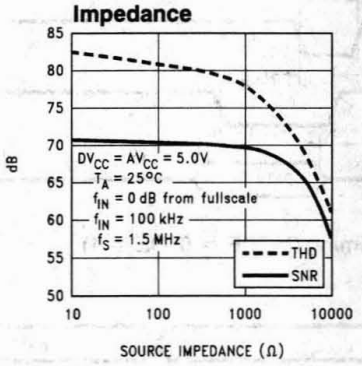
SNR vs Input Frequency (Through Mux)



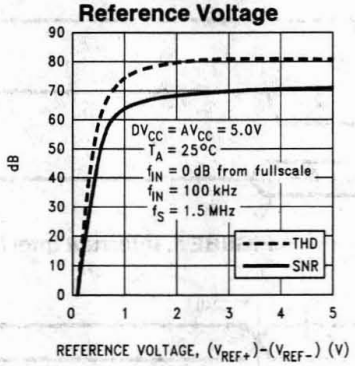
THD vs Input Frequency (Through Mux)



SNR and THD vs Source Impedance



SNR and THD vs Reference Voltage



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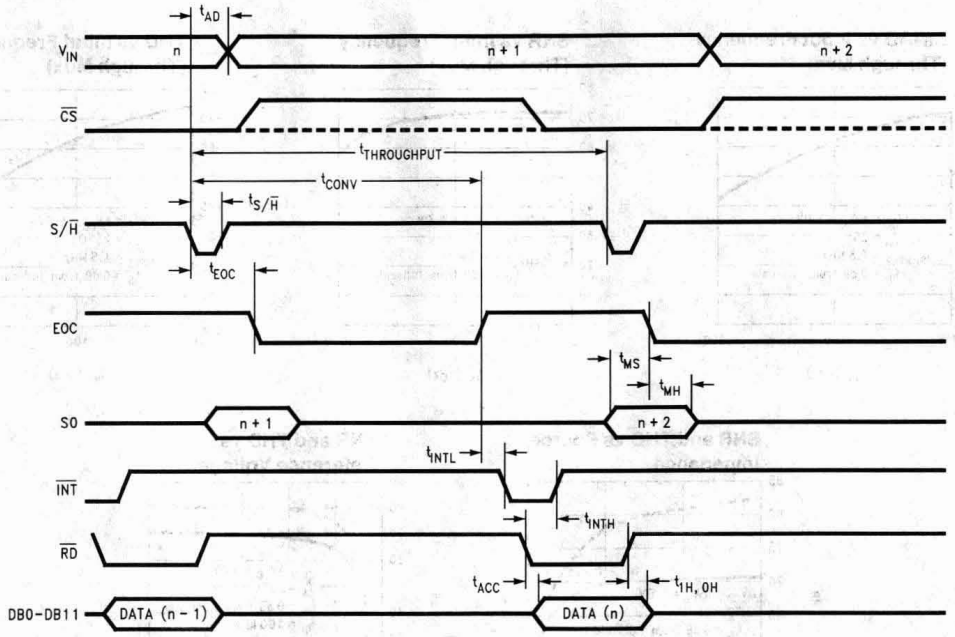
Timing Diagrams



TL/H/11876-9

FIGURE 1. Interrupt Interface Timing (MODE = 0, OE = 1)

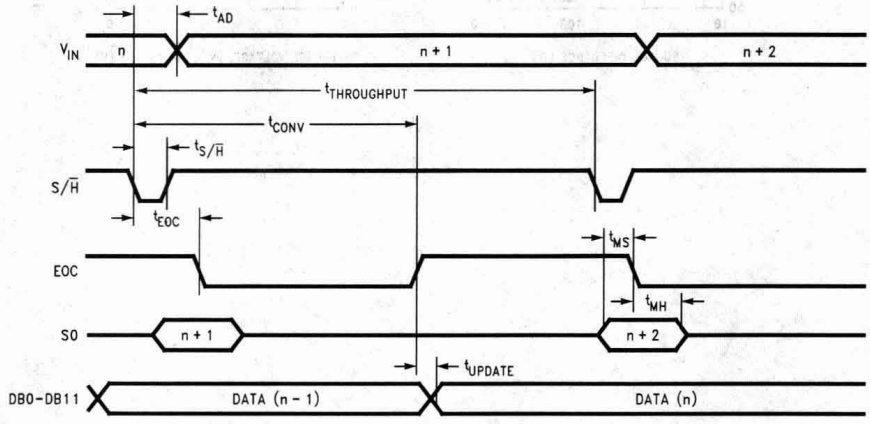


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FIGURE 2. High Speed Interface Timing (MODE = 0, OE = 1, $\overline{CS}$ = 0, $\overline{RD}$ = 0)

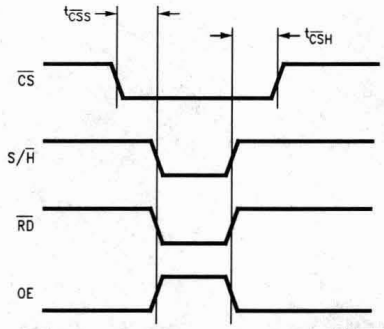

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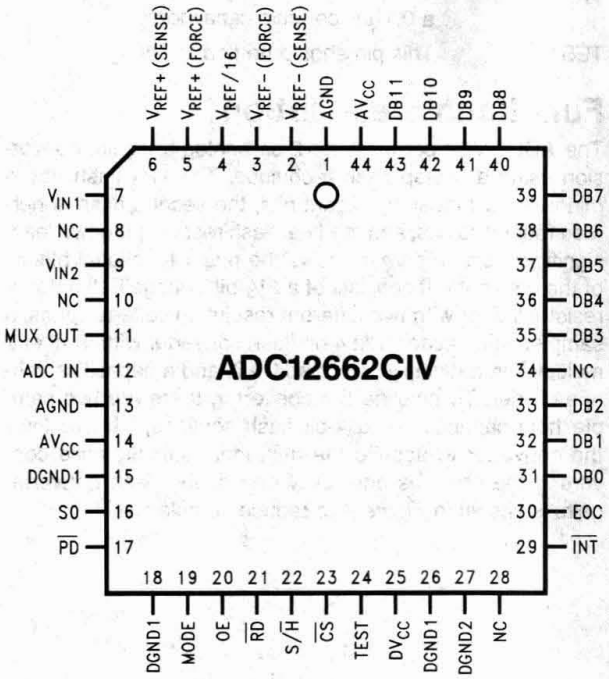
FIGURE 3. $\overline{CS}$ Setup and Hold Timing for S/$\overline{H}$, $\overline{RD}$, and OE

Connection Diagrams



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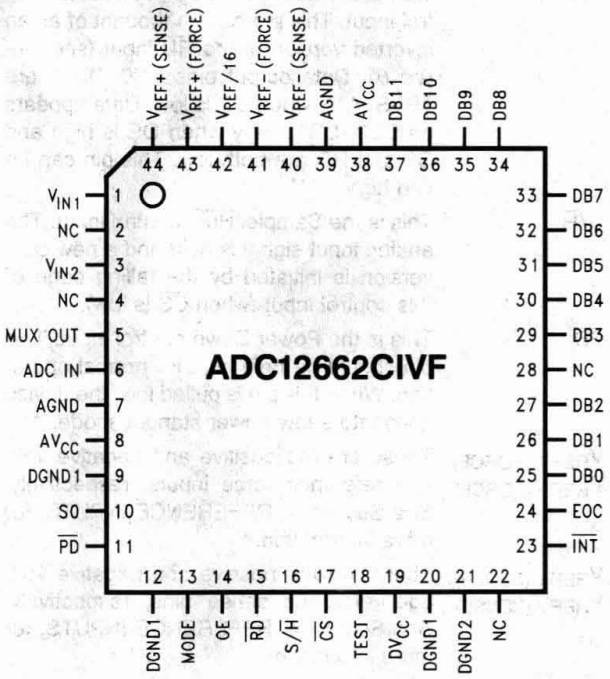
Top View



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Top View

Pin Descriptions

AV_{CC} These are the two positive analog supply inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed to AGND with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

DV_{CC} This is the positive digital supply input. It should always be connected to the same voltage as the analog supply, AV_{CC}. It should be bypassed to DGND2 with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

AGND, DGND1, DGND2 These are the power supply ground pins. There are separate analog and digital ground pins for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. All of the ground pins should be returned to the same potential. AGND is the analog ground for the converter. DGND1 is the ground pin for the digital control lines. DGND2 is the ground return for the output databus. See Section 6.0 LAYOUT AND GROUNDING for more information.

DB0–DB11 These are the TRI-STATE output pins, enabled by $\overline{RD}$, $\overline{CS}$, and OE.

V_{IN1}, V_{IN2} These are the analog input pins to the multiplexer. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV below ground or 50 mV above V_{CC}.

MUX OUT This is the output of the on-board analog input multiplexer.

ADC IN This is the direct input to the 12-bit sampling A/D converter. For accurate conversions, this pin should not be driven more than 50 mV below ground or 50 mV above V_{CC}.

S0 This pin selects the analog input that will be connected to the ADC12662 during the conversion. The input is selected based on the state of S0 when EOC makes its high-to-low transition. Low selects V_{IN1}, high selects V_{IN2}.

MODE This pin should be tied to DGND1.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$, S/$\overline{H}$, and OE inputs. This pin can be tied low.

$\overline{INT}$ This is the active low Interrupt output. When using the Interrupt Interface Mode *(Figure 1)*, this output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. This output is always high when $\overline{RD}$ is held low *(Figure 2)*.

$\overline{EOC}$ This is the End-of-Conversion control output. This output is low during a conversion.

$\overline{RD}$ This is the active low Read control input. When $\overline{RD}$ is low (and $\overline{CS}$ is low), the $\overline{INT}$ output is reset and (if OE is high) data appears on the data bus. This pin can be tied low.

2

Pin Descriptions (Continued)

OE — This is the active high Output Enable control input. This pin can be thought of as an inverted version of the $\overline{RD}$ input (see *Figure 6*). Data output pins DB0–DB11 are TRI-STATE when OE is low. Data appears on DB0–DB11 only when OE is high and $\overline{CS}$ and $\overline{RD}$ are both low. This pin can be tied high.

S/$\overline{H}$ — This is the Sample/$\overline{Hold}$ control input. The analog input signal is held and a new conversion is initiated by the falling edge of this control input (when $\overline{CS}$ is low).

$\overline{PD}$ — This is the Power Down control input. This pin should be held high for normal operation. When this pin is pulled low, the device goes into a low power standby mode.

$V_{REF}+(FORCE)$, $V_{REF}-(FORCE)$ — These are the positive and negative voltage reference force inputs, respectively. See Section 4, REFERENCE INPUTS, for more information.

$V_{REF}+(SENSE)$, $V_{REF}-(SENSE)$ — These are the positive and negative voltage reference sense pins, respectively. See Section 4, REFERENCE INPUTS, for more information.

$V_{REF}/16$ — This pin should be bypassed to AGND with a 0.1 μF ceramic capacitor.

TEST — This pin should be tied to DV_{CC}.

Functional Description

The ADC12662 performs a 12-bit analog-to-digital conversion using a 3 step flash technique. The first flash determines the six most significant bits, the second flash generates four more bits, and the final flash resolves the two least significant bits. *Figure 4* shows the major functional blocks of the converter. It consists of a 2½-bit Voltage Estimator, a resistor ladder with two different resolution voltage spans, a sample/hold capacitor, a 4-bit flash converter with front end multiplexer, a digitally corrected DAC, and a capacitive voltage divider. To pipeline the converter, there are two sample/hold capacitors and 4-bit flash sections, which allows the converter to acquire the next input sample while converting the previous one. Only one of the flash converter pairs is shown in *Figure 4* to reduce complexity.

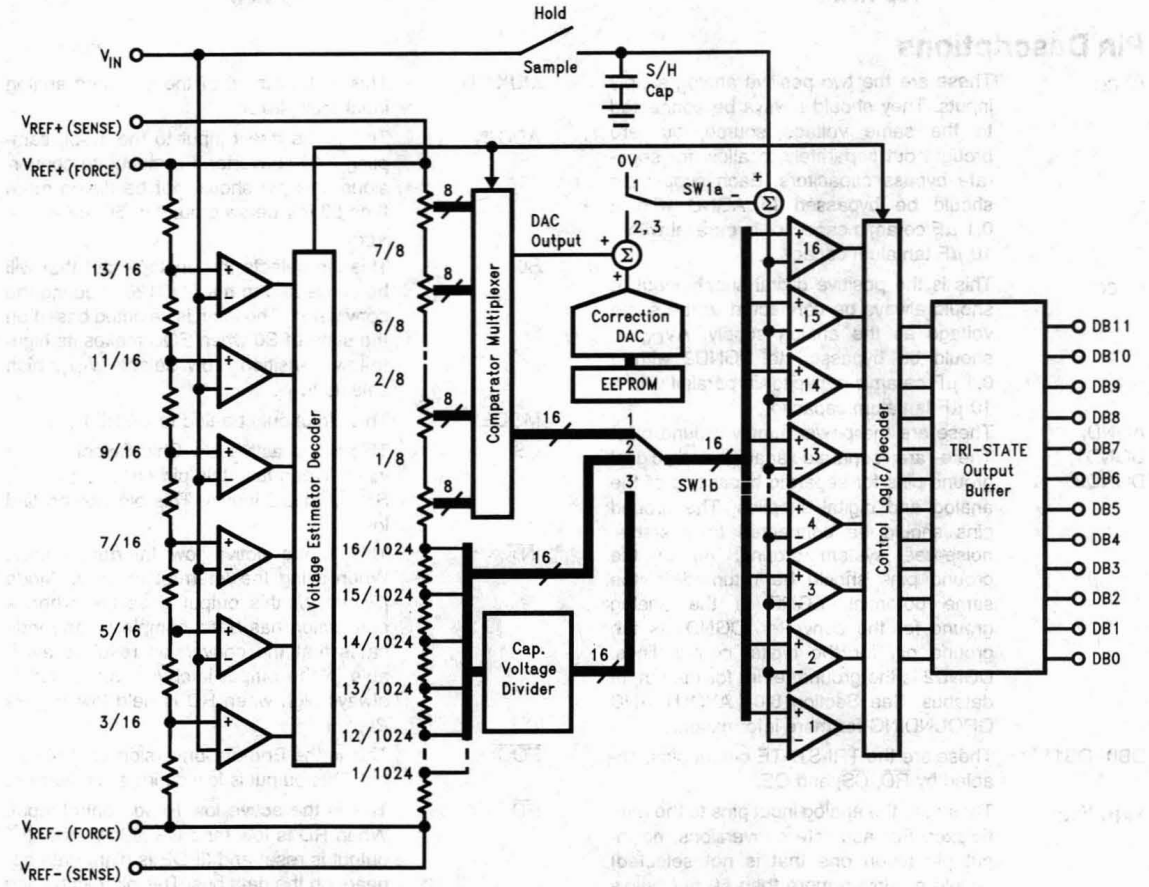

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FIGURE 4. Functional Block Diagram

Functional Description (Continued)

The resistor string near the center of the block diagram in *Figure 4* generates the 6-bit and 10-bit reference voltages for the first two conversions. Each of the 16 resistors at the bottom of the string is equal to $1/1024$ of the total string resistance. These resistors form the **LSB Ladder*** and have a voltage drop of $1/1024$ of the total reference voltage ($V_{REF+} - V_{REF-}$) across each of them. The remaining resistors form the **MSB Ladder**. It is comprised of eight groups of eight resistors each connected in series (the lowest MSB ladder resistor is actually the entire LSB ladder). Each MSB Ladder section has $1/8$ of the total reference voltage across it. Within a given MSB ladder section, each of the eight MSB resistors has $1/64$ of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB ladders. The Comparator Multiplexer can connect any of these tap points, in two adjacent groups of eight, to the sixteen comparators shown at the right of *Figure 4.* This function provides the necessary reference voltages to the comparators during the first two flash conversions.

*Note: The weight of each resistor on the LSB ladder is actually equivalent to four 12-bit LSBs. It is called the LSB ladder because it has the highest resolution of all the ladders in the converter.

The six comparators, seven-resistor string (Estimator DAC ladder), and Estimator Decoder at the left of *Figure 4* form the Voltage Estimator. The Estimator DAC, connected between V_{REF+} and V_{REF-}, generates the reference voltages for the six Voltage Estimator comparators. The comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is used to control the placement of the Comparator Multiplexer, connecting the appropriate MSB ladder section to the sixteen flash comparators. A total of only 22 comparators (6 in the Voltage Estimator and 16 in the flash converter) is required to quantize the input to 6 bits, instead of the 64 that would be required using a traditional 6-bit flash.

Prior to a conversion, the Sample/Hold switch is closed, allowing the voltage on the S/H capacitor to track the input voltage. Switch 1 is in position 1. A conversion begins by opening the Sample/Hold switch and latching the output of the Voltage Estimator. The estimator decoder then selects two adjacent banks of tap points along the MSB ladder. These sixteen tap points are then connected to the sixteen flash converters. For example, if the input voltage is between $5/16$ and $7/16$ of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the sixteen tap points between $2/8$ and $4/8$ ($4/16$ and $8/16$) of V_{REF} and connects them to the sixteen flash converters. The first flash conversion is now performed, producing the first 6 MSBs of data.

At this point, Voltage Estimator errors as large as $1/16$ of V_{REF} will be corrected since the flash converters are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if $(7/16)V_{REF} < V_{IN} < (9/16)V_{REF}$, the Voltage Estimator's comparators tied to the tap points below $(9/16)V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The 16 comparators will be placed on the MSB ladder tap points between $(3/8)V_{REF}$ and $(5/8)V_{REF}$. This overlap of $(1/16)V_{REF}$ will automatically cancel a Voltage Estimator error of up to 256 LSBs. If the first flash conversion determines that the input voltage is between $(3/8)V_{REF}$ and $((4/8)V_{REF} - LSB/2)$, the Voltage Estimator's output code will be corrected by subtracting "1", resulting in a corrected value of "01" for the first two MSBs. If the first flash conversion determines that the input voltage is between $(4/8)V_{REF} - LSB/2)$ and $(5/8)V_{REF}$, the voltage estimator's output code is unchanged.

The results of the first flash and the Voltage Estimator's output are given to the factory-programmed on-chip EEPROM which returns a correction code corresponding to the error of the MSB ladder at that tap. This code is converted to a voltage by the Correction DAC. To generate the next four bits, SW1 is moved to position 2, so the ladder voltage and the correction voltage are subtracted from the input voltage. The remainder is applied to the sixteen flash converters and compared with the 16 tap points from the LSB ladder.

Functional Description (Continued)

The result of this second conversion is accurate to 10 bits and describes the input remainder as a voltage between two tap points (V_H and V_L) on the LSB ladder. To resolve the last two bits, the voltage across the ladder resistor (between V_H and V_L) is divided up into 4 equal parts by the capacitive voltage divider, shown in *Figure 5*. The divider also creates 6 LSBs below V_L and 6 LSBs above V_H to provide overlap used by the digital error correction. SW1 is moved to position 3, and the remainder is compared with these 16 new voltages. The output is combined with the results of the Voltage Estimator, first flash, and second flash to yield the final 12-bit result.

By using the same sixteen comparators for all three flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard multi-step techniques.

Applications Information

1.0 MODES OF OPERATION

The ADC12662 has two interface modes: An interrupt/read mode and a high speed mode. *Figures 1* and *2* show the timing diagrams for these interfaces.

In order to clearly show the relationship between S/$\overline{H}$, $\overline{CS}$, $\overline{RD}$, and OE, the control logic decoding section of the ADC12662 is shown in *Figure 6*.

Interrupt Interface

As shown in *Figure 1*, the falling edge of S/$\overline{H}$ holds the input voltage and initiates a conversion. At the end of the conversion, the EOC output goes high and the $\overline{INT}$ output goes low, indicating that the conversion results are latched and may be read by pulling $\overline{RD}$ low. The falling edge of $\overline{RD}$ resets the $\overline{INT}$ line. Note that $\overline{CS}$ must be low to enable S/$\overline{H}$ or $\overline{RD}$.

High Speed Interface

The Interrupt interface works well at lower speeds, but few microprocessors could keep up with the 1 μs interrupts that would be generated if the ADC12662 was running at full speed. The most efficient interface is shown in *Figure 2*. Here the output data is always present on the databus, and the $\overline{INT}$ to $\overline{RD}$ delay is eliminated.

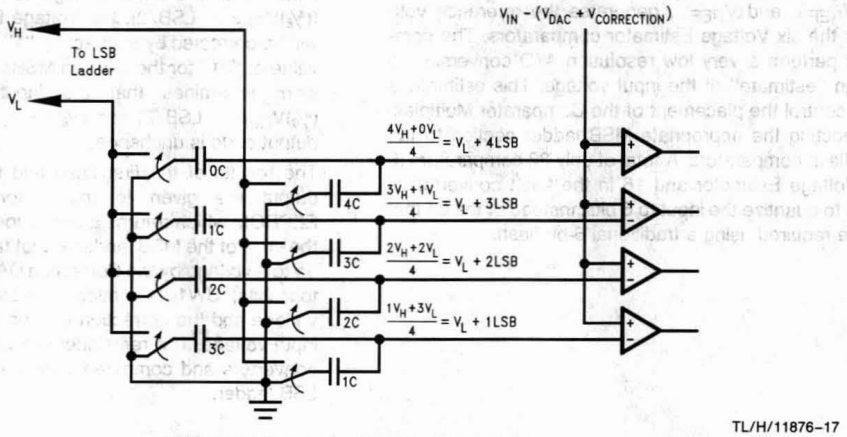

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FIGURE 5. The Capacitive Voltage Divider

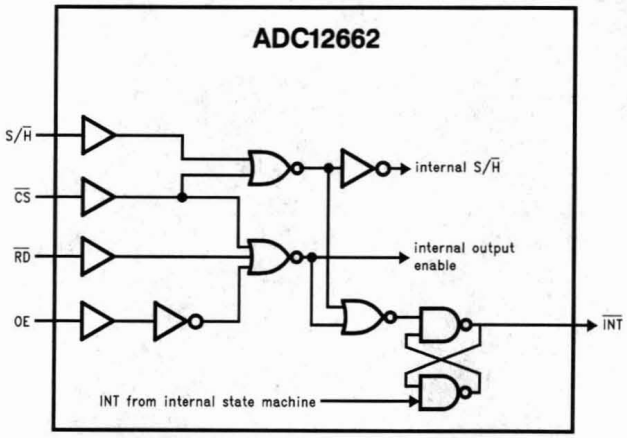

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FIGURE 6. ADC Control Logic

Applications Information (Continued)

2.0 THE ANALOG INPUT

The analog input of the ADC12662 can be modeled as two small resistances in series with the capacitance of the input hold capacitor (C_{IN}), as shown in *Figure 7*. The S/$\overline{H}$ switch is closed during the Sample period, and open during Hold. The source has to charge C_{IN} to the input voltage within the sample period. Note that the source impedance of the input voltage (R_{SOURCE}) has a direct effect on the time it takes to charge C_{IN}. If R_{SOURCE} is too large, the voltage across C_{IN} will not settle to within 0.5 LSBs of V_{SOURCE} before the conversion begins, and the conversion results will be incorrect. From a dynamic performance viewpoint, the combination of R_{SOURCE}, R_{MUX}, R_{SW}, and C_{IN} form a low pass filter. Minimizing R_{SOURCE} will increase the frequency response of the input stage of the converter.

Typical values for the components shown in *Figure 7* are: R_{MUX} = 100Ω, R_{SW} = 100Ω, and C_{IN} = 25 pF. The settling time to n bits is:

$$t_{SETTLE} = (R_{SOURCE} + R_{MUX} + R_{SW}) * C_{IN} * n * \ln(2).$$

The bandwidth of the input circuit is:

$$f_{-3dB} = 1/(2 * 3.14 * (R_{SOURCE} + R_{MUX} + R_{SW}) * C_{IN})$$

The ADC12662 is operated in a pipelined sequence, with one hold capacitor acquiring the next sample while a conversion is being performed on the voltage stored on the other hold capacitor. This gives the source over t_{CONV} seconds to charge the hold capacitor to its final value. At 1.5 MHz, the settling time must be less than 667 ns. Using the settling time equation and component values given, the maximum source impedance that will allow the input to settle to ½ LSB (n = 13) at full speed is ~2.8 kΩ. To ensure ½ LSB settling over temperature and device-to-device variation, R_{SOURCE} should be a maximum of 500Ω when the converter is operated at full speed.

If the signal source has a high output impedance, its output should be buffered with an operational amplifier capable of driving a switched 25 pF/100Ω load. Any ringing or instabilities at the op amp's output during the sampling period can result in conversion errors. The LM6361 high speed op amp is a good choice for this application due to its speed and its ability to drive large capacitive loads. *Figure 8* shows the LM6361 driving the ADC IN input of an ADC12662. The 100 pF capacitor at the input of the converter absorbs some of the high frequency transients generated by the S/$\overline{H}$ switching, reducing the op amp transient response requirements. The 100 pF capacitor should only be used with high speed op amps that are unconditionally stable driving capacitive loads.

Another benefit of using a high speed buffer is improved THD performance when using the multiplexer of the ADC12662. The MUX on-resistance is somewhat non-linear over input voltage, causing the RC time constant formed by C_{IN}, R_{MUX}, and R_{SW} to vary depending on the input voltage. This results in increasing THD with increasing frequency. Inserting the buffer between the MUX OUT and the ADC IN terminals as shown in *Figure 8* will eliminate the loading on R_{MUX}, significantly reducing the THD of the multiplexed system.

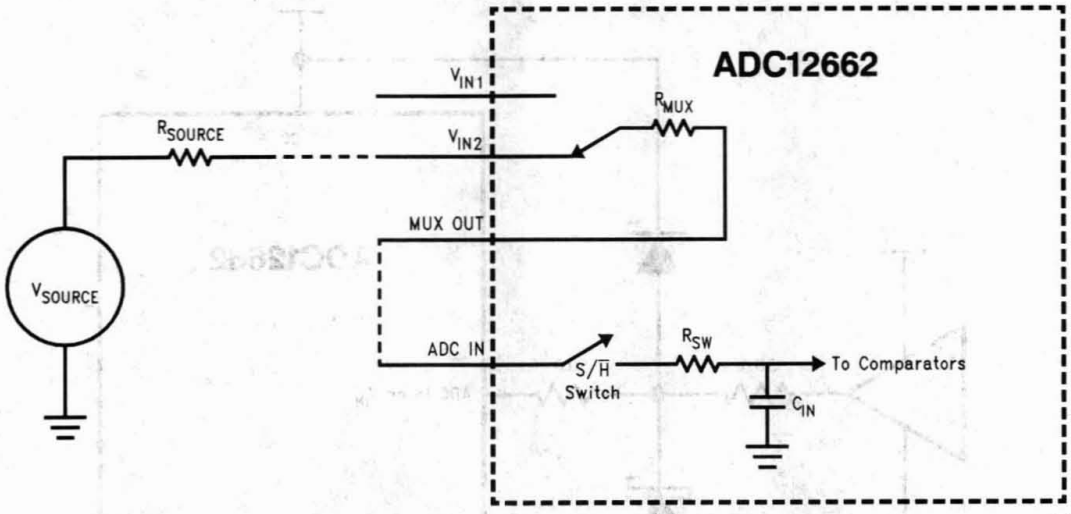

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FIGURE 7. Simplified ADC12662 Input Stage

Applications Information (Continued)

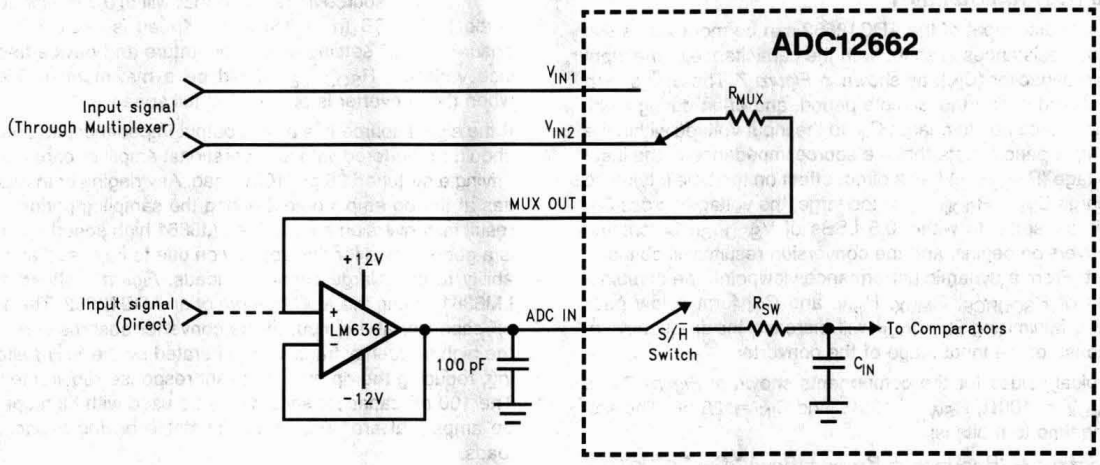

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FIGURE 8. Buffering the Input with an LM6361 High Speed Op Amp

Correct converter operation will be obtained for input voltages greater than AGND − 50 mV and less than AV_{CC} + 50 mV. Avoid driving the signal source more than 300 mV higher than AV_{CC}, or more than 300 mV below AGND. If an analog input pin is forced beyond these voltages, the current flowing through that pin should be limited to 25 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 50 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits for any reason (unknown/uncontrollable input voltage range, power-on transients, fault conditions, etc.) some form of input protection, such as that shown in *Figure 9,* should be used.

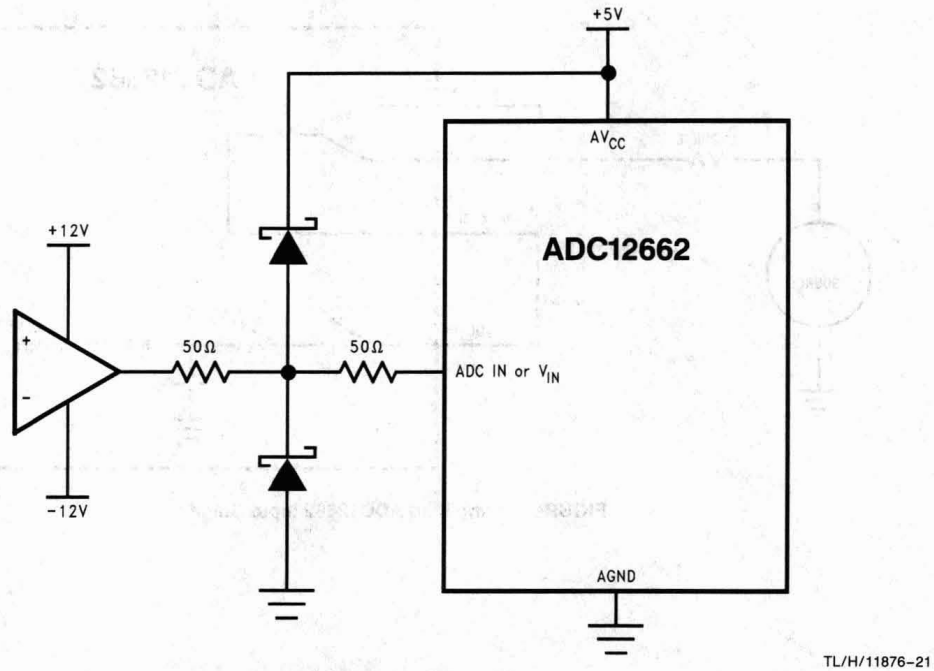

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FIGURE 9. Input Protection

Applications Information (Continued)

3.0 ANALOG MULTIPLEXER

The ADC12662 has an input multiplexer that is controlled by the logic level on pin S0 when EOC goes low, as shown in *Figures 1* and *2.* Multiplexer setup and hold times with respect to the S/$\overline{H}$ input can be determined by these two equations:

$t_{MS\ (wrt\ S/\overline{H})} = t_{MS} - t_{EOC\ (min)} = 50 - 60 = -10$ ns

$t_{MH\ (wrt\ S/\overline{H})} = t_{MH} + t_{EOC\ (max)} = 50 + 125 = 175$ ns

Note that $t_{MS\ (wrt\ S/\overline{H})}$ is a negative number; this indicates that the data on S0 must become valid within 10 ns after S/$\overline{H}$ goes low in order to meet the setup time requirements. S0 must be valid for a length of

$(t_{MH} + t_{EOC\ (max)}) - (t_{MS} - t_{EOC\ (min)}) = 185$ ns.

Table I shows how the input channels are assigned:

TABLE I. ADC12662 Input Multiplexer Programming

S0	Channel
0	V_{IN1}
1	V_{IN2}

The output of the multiplexer is available to the user via the MUX OUT pin. This output allows the user to perform additional signal processing, such as filtering or gain, before the signal is returned to the ADC IN input and digitized. If no additional signal processing is required, the MUX OUT pin should be tied directly to the ADC IN pin.

See Section 9.0 (APPLICATIONS) for a simple circuit that will alternate between the two inputs while converting at full speed.

4.0 REFERENCE INPUTS

In addition to the fully differential V_{REF+} and V_{REF-} reference inputs used on most National Semiconductor ADCs, the ADC12662 has two sense outputs for precision control of the ladder voltage. These sense inputs compensate for errors due to IR drops between the reference source and the ladder itself. The resistance of the reference ladder is typically 750Ω. The parasitic resistance (R_P) of the package leads, bond wires, PCB traces, etc. can easily be 0.5Ω to 1.0Ω or more. This may not be significant at 8-bit or 10-bit resolutions, but at 12 bits it can introduce voltage drops causing offset and gain errors as large as 6 LSBs.

The ADC12662 provides a means to eliminate this error by bringing out two additional pins that sense the exact voltage at the top and bottom of the ladder. With the addition of two op amps, the voltages on these internal nodes can be forced to the exact value desired, as shown in *Figure 10.*

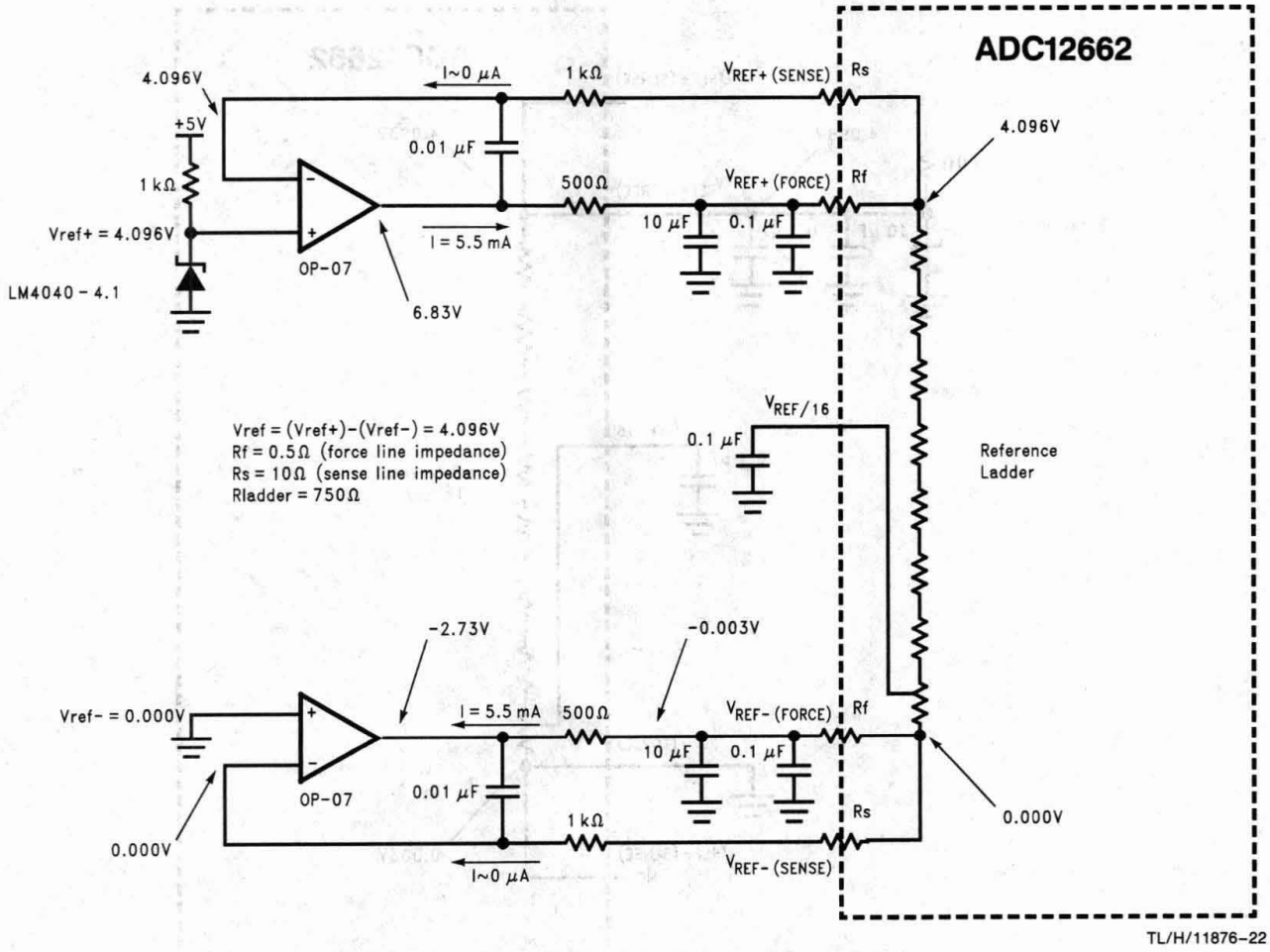

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FIGURE 10. Reference Ladder Force and Sense Inputs

Applications Information (Continued)

Since the current flowing through the SENSE lines is essentially zero, there is negligible voltage drop across R_S and the 1 kΩ resistor, so the voltage at the inverting input of the op amp accurately represents the voltage at the top (or bottom) of the ladder. The op amp drives the FORCE input and forces the voltage at the ends of the ladder to equal the voltage at the op amps's non-inverting input, plus or minus its input offset voltage. For this reason op amps with low V_{OS}, such as the LM627 or LM607, should be used for this application. When used in this configuration, the ADC12662 has less than 2 LSBs of offset and 1.5 LSB of gain error without any user adjustments.

The 0.1 μF and 10 μF capacitors on the force inputs provide high frequency decoupling of the reference ladder. The 500Ω force resistors isolate the op amps from this large capacitive load. The 0.01 μF/1 kΩ network provides zero phase shift at high frequencies to ensure stability. Note that the op amp supplies in this example must be ±10V to ±15V to meet the input/output voltage range requirements of the LM627 and supply the sub-zero voltage to the V_{REF-} (FORCE) pin. The $V_{REF/16}$ output should be bypassed to analog ground with a 0.1 μF ceramic capacitor.

The reference inputs are fully differential and define the zero to full-scale range of the input signal. They can be configured to span up to 5V (V_{REF-} = 0V, V_{REF+} = 5V), or they can be connected to different voltages (within the 0V to 5V limits) when other input spans are required. The ADC12662 is tested at V_{REF-} (SENSE) = 0V, V_{REF+} (SENSE) = 4.096V. Reducing the reference voltage span to less than 4V increases the sensitivity (reduces the LSB size) of the converter; however noise performance degrades when lower reference voltages are used. A plot of dynamic performance vs reference voltage is given in the Typical Performance Characteristics section.

If the converter will be used in an application where DC accuracy is secondary to dynamic performance, then a simpler reference circuit may suffice. The circuit shown in *Figure 11* will introduce several LSBs of offset and gain error, but INL, DNL, and all dynamic specifications will be unaffected.

All bypass capacitors should be located as close to the ADC12662 as possible to minimize noise on the reference ladder. The $V_{REF/16}$ output should be bypassed to analog ground with a 0.1 μF ceramic capacitor.

The LM4040 shunt voltage reference is available with a 4.096V output voltage. With initial accuracies as low as ± 0.1%, it makes an excellent reference for the ADC12662.

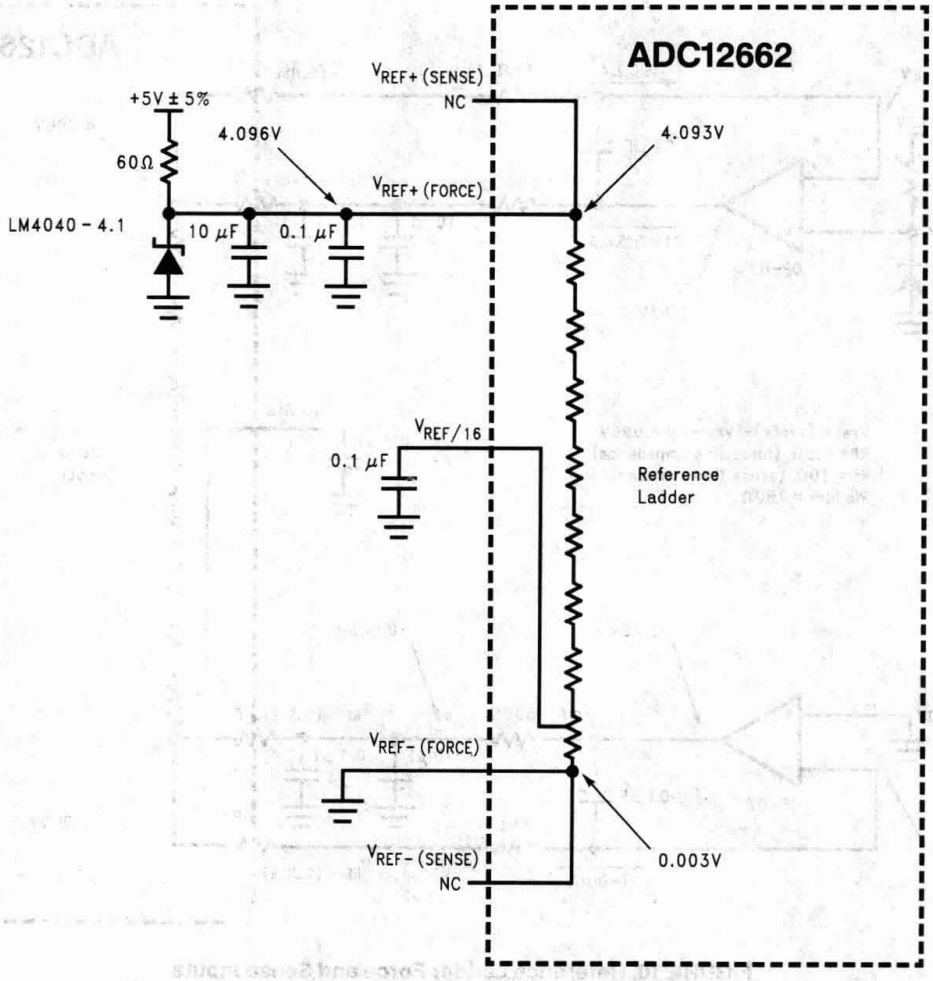

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FIGURE 11. Using the V_{REF} Force Pins Only

Applications Information (Continued)

5.0 POWER SUPPLY CONSIDERATIONS

The ADC12662 is designed to operate from a single +5V power supply. There are two analog supply pins (AV_{CC}) and one digital supply pin (DV_{CC}). These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee proper operation of the converter, all three supply pins should be connected to the same voltage source. In systems with separate analog and digital supplies, the converter should be powered from the analog supply.

The ground pins are AGND (analog ground), DGND1 (digital input ground), and DGND2 (digital output ground). These pins allow for three separate ground planes for these sections of the chip. Isolating the analog section from the two digital sections reduces digital interference in the analog circuitry, improving the dynamic performance of the converter. Separating the digital outputs from the digital inputs (particularly the S/$\overline{H}$ input) reduces the possibility of ground bounce from the 12 data lines causing jitter on the S/$\overline{H}$ input. The analog ground plane should be connected to the Digital2 ground plane at the ground return for the power supply. The Digital1 ground plane should be tied to the Digital2 ground plane at the DGND1 and DGND2 pins.

Both AV_{CC} pins should be bypassed to the AGND ground plane with 0.1 μF ceramic capacitors. One of the two AV_{CC} pins should also be bypassed with a 10 μF tantalum capacitor. DV_{CC} should be bypassed to the DGND2 ground plane with a 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor.

6.0 LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC12662, it is necessary to use appropriate circuit board layout techniques. Separate analog and digital ground planes are required to meet datasheet AC and DC limits. The analog ground plane should be low-impedance and free of noise from other parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean analog ground return point. Grounding the component at the wrong point will result in increased noise and reduced conversion accuracy.

Figure 12 gives an example of a suitable layout, including power supply routing, ground plane separation, and bypass capacitor placement. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on the analog ground plane. All digital circuitry and I/O lines (excluding the S/$\overline{H}$ input) should use the digital2 ground plane as ground. The digital1 ground plane should only be used for the S/$\overline{H}$ signal generation.

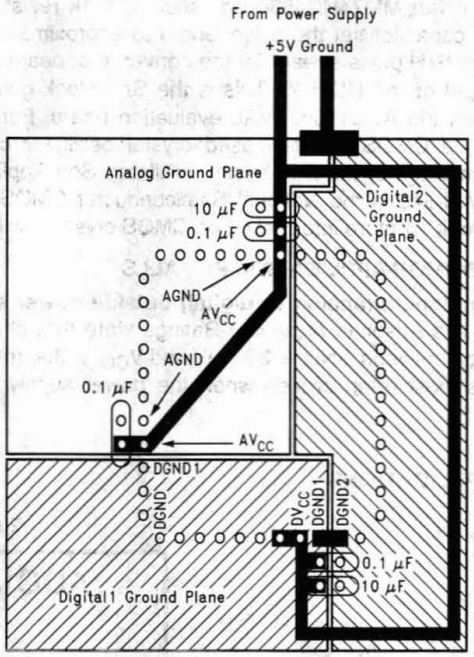

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FIGURE 12. PC Board Layout

7.0 DYNAMIC PERFORMANCE

The ADC12662 is AC tested and its dynamic performance is guaranteed. In order to meet these specifications, the clock source driving the S/$\overline{H}$ input must be free of jitter. For the best AC performance, a crystal oscillator is recommended. For operation at or near the ADC12662's 1.5 MHz maximum sampling rate, a 1.5 MHz squarewave will provide a good signal for the S/$\overline{H}$ input. As long as the duty cycle is near 50%, the waveform will be low for about 333 ns, which is within the 400 ns limit. When operating the ADC12662 at a sample rate of 1.25 MHz or below, the pulse width of the S/$\overline{H}$ signal must be smaller than half the sample period.

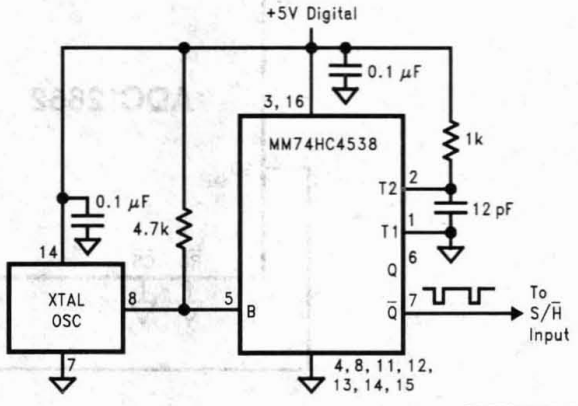

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FIGURE 13. Crystal Clock Source

Figure 13 is an example of a low jitter S/$\overline{H}$ pulse generator that can be used with the ADC12662 and allow operation at sampling rates from DC to 1.5 MHz. A standard 4-pin DIP crystal oscillator provides a stable 1.5 MHz squarewave. Since most DIP oscillators have TTL outputs, a 4.7k pullup resistor is used to raise the output high voltage to CMOS input levels. The output is fed to the trigger input (falling

Applications Information (Continued)

edge) of an MM74HC4538 one-shot. The 1k resistor and 12 pF capacitor set the pulse length to approximately 100 ns. The S/$\overline{H}$ pulse stream for the converter appears on the Q output of the HC4538. This is the S/$\overline{H}$ clock generator used on the ADC12062EVAL evaluation board. For lower power, a CMOS inverter-based crystal oscillator can be used in place of the DIP crystal oscillator. See Application Note AN-340 in the National Semiconductor CMOS Logic Databook for more information on CMOS crystal oscillators.

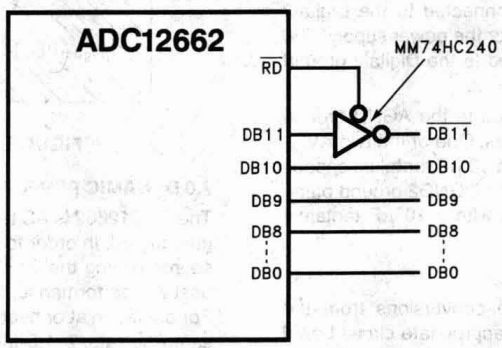
8.0 COMMON APPLICATION PITFALLS

Driving inputs (analog or digital) outside power supply rails. The Absolute Maximum Ratings state that all inputs must be between GND − 300 mV and V_{CC} + 300 mV. This rule is most often broken when the power supply to the converter is turned off, but other devices connected to it (op amps, microprocessors) still have power. Note that if there is no power to the converter, DGND = AGND = DV_{CC} = AV_{CC} = 0V, so all inputs should be within ±300 mV of AGND and DGND.

Driving a high capacitance digital data bus. The more capacitance the data bus has to charge for each conversion, the more instantaneous digital current required from DV_{CC} and DGND. These large current spikes can couple back to the analog section, decreasing the SNR of the converter. While adequate supply bypassing and separate analog and digital ground planes will reduce this problem, buffering the digital data outputs (with a pair of MM74HC541s, for example) may be necessary if the converter must drive a heavily loaded databus.

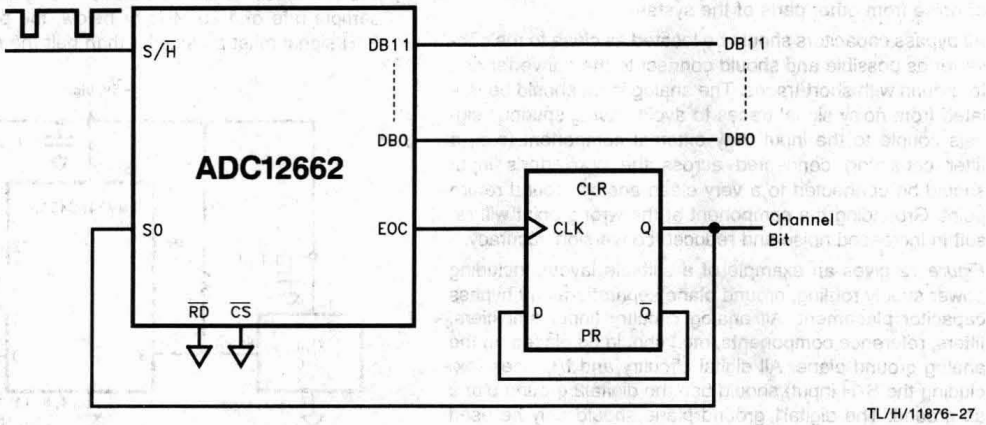
9.0 APPLICATIONS

2's Complement Output



TL/H/11876–26

Ping-Ponging between V_{IN1} and V_{IN2}



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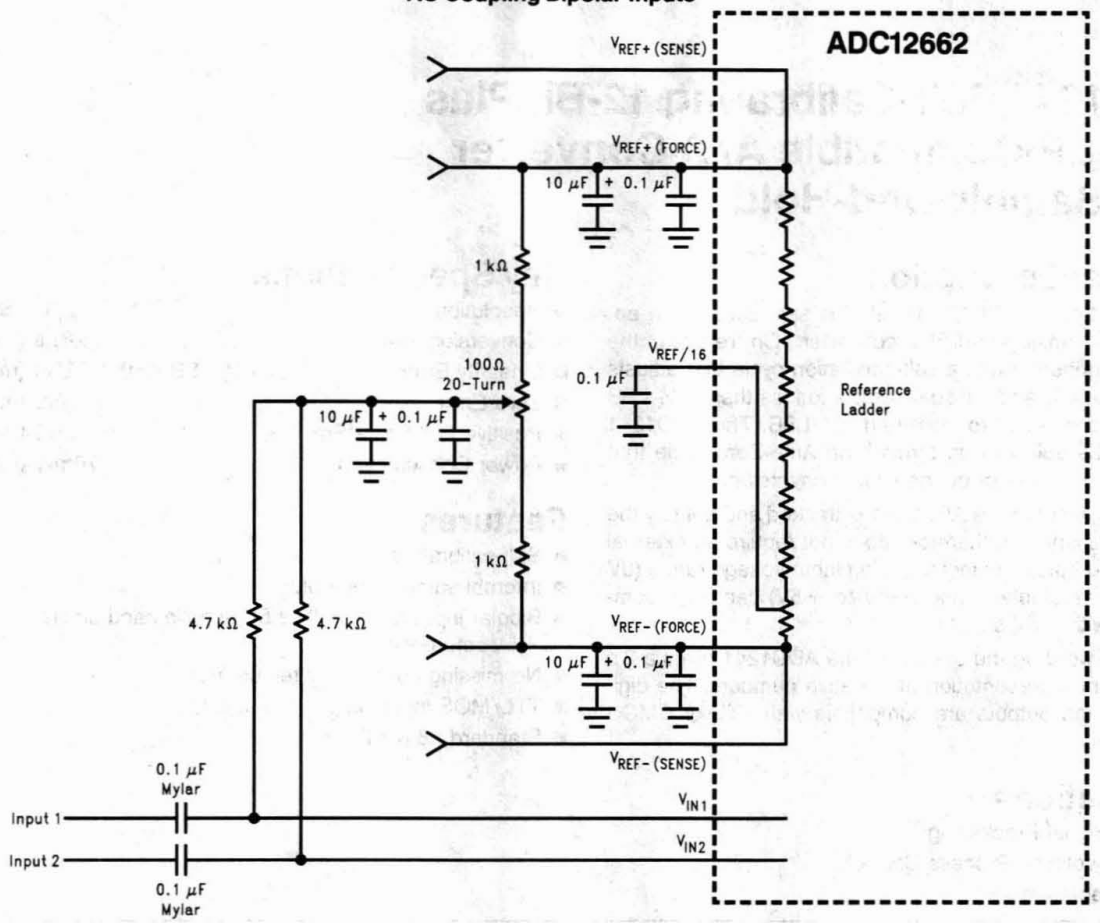
Applications Information (Continued)

AC Coupling Bipolar Inputs



TL/H/11876–28

National Semiconductor

ADC1241 Self-Calibrating 12-Bit Plus Sign μP-Compatible A/D Converter with Sample-and-Hold

General Description

The ADC1241 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter. On request, the ADC1241 goes through a self-calibration cycle that adjusts positive linearity and full-scale errors to less than ±½ LSB each and zero error to less than ±1 LSB. The ADC1241 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC1241 is tracked and held by the internal circuitry, and therefore does not require an external sample-and-hold. A unipolar analog input voltage range (0V to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit word on the outputs of the ADC1241 gives a 2's complement representation of negative numbers. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Key Specifications

■ Resolution	12 Bits plus Sign
■ Conversion Time	13.8μs (max)
■ Linearity Error	±½ LSB (±0.0122%) (max)
■ Zero Error	±1LSB (max)
■ Positive Full Scale Error	±1LSB (max)
■ Power Consumption	70mW (max)

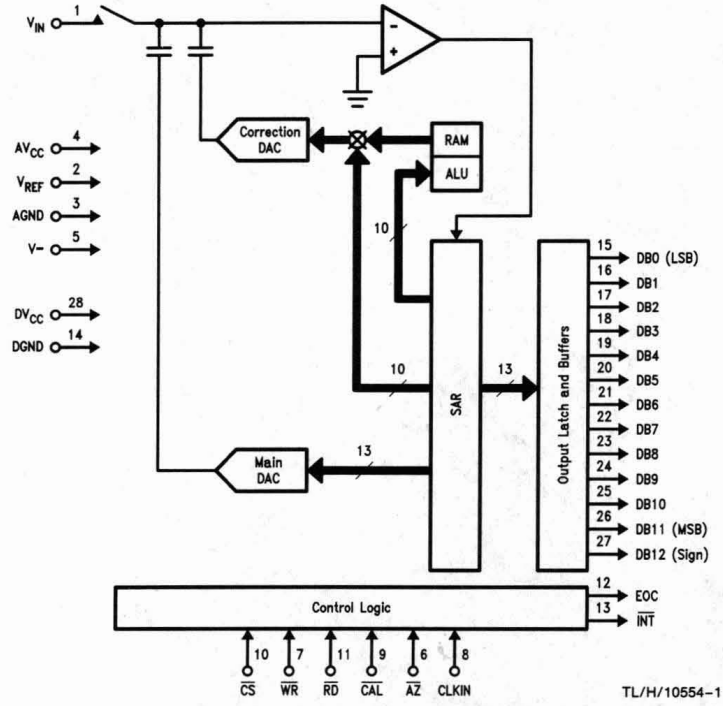
Features

- Self-calibrating
- Internal sample-and-hold
- Bipolar input range with ±5V supplies and single +5V reference
- No missing codes over temperature
- TTL/MOS input/output compatible
- Standard 28-pin DIP

Applications

- Digital Signal Processing
- High Resolution Process Control
- Instrumentation

Simplified Schematic



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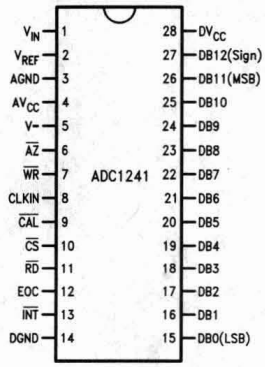
Connection Diagram

Dual-In-Line Package



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Top View

Order Number ADC1241CMJ, ADC1241CMJ/883, ADC1241BIJ or ADC1241CIJ
See NS Package Number J28A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Input (V_{IN})	(V^- −0.3V) to (V_{CC} + 0.3V)
AV_{CC}-DV_{CC} (Note 7)	0.3V
Input Current at any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information	
J Package (10 sec)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1241BIJ, ADC1241CIJ	$-40°C \le T_A \le +85°C$
ADC1241CMJ, ADC1241CMJ/883	$-55°C \le T_A \le +125°C$
DV_{CC} and AV_{CC} Voltage (Notes 6 & 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 & 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +5.0V, and f_{CLK} = 2.0 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Notes 10, 18)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error	ADC1241BIJ	After Auto-Cal (Notes 11 & 12)		**±½**	LSB(max)
		ADC1241CMJ, CIJ			**±1**	LSB max
	Negative Integral Linearity Error	ADC1241BIJ	After Auto-Cal (Notes 11 & 12)		**±1**	LSB(max)
		ADC1241CMJ, CIJ			**±1**	LSB(max)
	Differential Linearity		After Auto-Cal (Notes 11 & 12)		**12**	Bits(min)
	Zero Error		After Auto-Zero or Auto-Cal (Notes 12 & 13)		**±1**	LSB(max)
	Positive Full-Scale Error		After Auto-Cal (Note 12)	±½	**±1**	LSB(max)
	Negative Full-Scale Error		After Auto-Cal (Note 12)		±1 / **±2**	LSB(max)
C_{REF}	V_{REF} Input Capacitance			80		pF
C_{IN}	Analog Input Capacitance			65		pF
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB
DYNAMIC CHARACTERISTICS						
S/(N+D)	Unipolar Signal-to-Noise+Distortion Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	72		dB
			f_{IN} = 10 kHz, V_{IN} = 4.85 V_{p-p}	72		dB
S/(N+D)	Bipolar Signal-to-Noise+Distortion Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85 V_{p-p}	76		dB
			f_{IN} = 10 kHz, V_{IN} = ±4.85 V_{p-p}	76		dB
	Unipolar Full Power Bandwidth (Note 17)		V_{IN} = 0V to 4.85V	32		kHz
	Bipolar Full Power Bandwidth (Note 17)		V_{IN} = ±4.85 V_{p-p}	25		kHz
t_{Ap}	Aperture Time			100		ns
	Aperture Jitter			100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 2.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Condition	Typical (Note 9)	Limit (Notes 10, 18)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	$V_{CC} = 5.25V$		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	$V_{CC} = 4.75V$		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1**	μA(max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**	μA(max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V(min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V(max)
V_H	CLK IN Hysteresis $[V_T^+(min) - V_T^-(max)]$		0.7	**0.4**	V(min)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**	V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**	V(max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA(max)
		$V_{OUT} = 5V$	0.01	**3**	μA(max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA(min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA(min)
DI_{CC}	DV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	1	**2**	mA(max)
AI_{CC}	AV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA(max)
I^-	V^- Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA(max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 18)	Units (Limits)
f_{CLK}	Clock Frequency			**2.0**	MHz
			0.5		MHz(min)
			4.0		MHZ(max)
	Clock Duty Cycle		50		%
				40	%(min)
				60	%(max)
t_C	Conversion Time		$27(1/f_{CLK})$	**$27(1/f_{CLK}) + 300$ ns**	(max)
		$f_{CLK} = 2.0$ MHz	13.5		μs
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$	$7(1/f_{CLK})$	**$7(1/f_{CLK}) + 300$ ns**	(max)
		$f_{CLK} = 2.0$ MHz	3.5		μs
t_Z	Auto Zero Time		26	**26**	$1/f_{CLK}$(max)
		$f_{CLK} = 2.0$ MHz	13		μs
$t_{\overline{CAL}}$	Calibration Time		1396		$1/f_{CLK}$
		$f_{CLK} = 2.0$ MHz	698	**706**	μs (max)
$t_{W(\overline{CAL})L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns(min)
$t_{W(\overline{WR})L}$	Minimum $\overline{WR}$ Pulse Width		60	**200**	ns(min)
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	85	ns(max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	90	ns(max)
$t_{PD(\overline{INT})}$	Maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns(max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

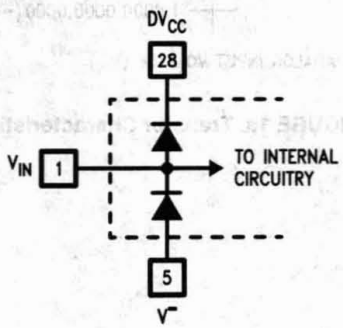
Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} >$ (AV_{CC} or DV_{CC}), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 125°C$, and the typical thermal resistance (θ_{JA}) of the ADC1241 with CMJ, BIJ, and CIJ suffixes when board mounted is 47°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV.



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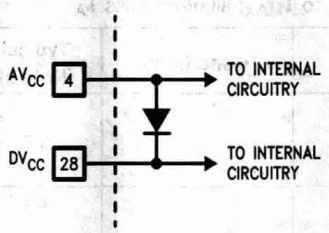
This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (−4.75 V_{DC}), full-scale must be ≤ 4.8 V_{DC}.

AC Electrical Characteristics (Continued)

Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at f_{CLK} = 2.0 MHz. At higher and lower clock frequencies accuracy may degrade. See curves in the Typical Performance Characteristics Section.

Note 9: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*).

Note 12: The ADC1241's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started, see the typical performance characteristic curves.

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

Note 15: If the clock is asynchronous to the falling edge of $\overline{WR}$ an uncertainty of one clock period will exist in the interval of t_A, therefore making the minimum t_A = 6 clock periods and the maximum t_A = 7 clock periods. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods.

Note 16: The $\overline{CAL}$ line must be high before any other conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: A military RETS electrical test specification is available on request. At time of printing, the ADC1241CMJ/883 RETS specification complies fully with the **boldface** limits in this column.

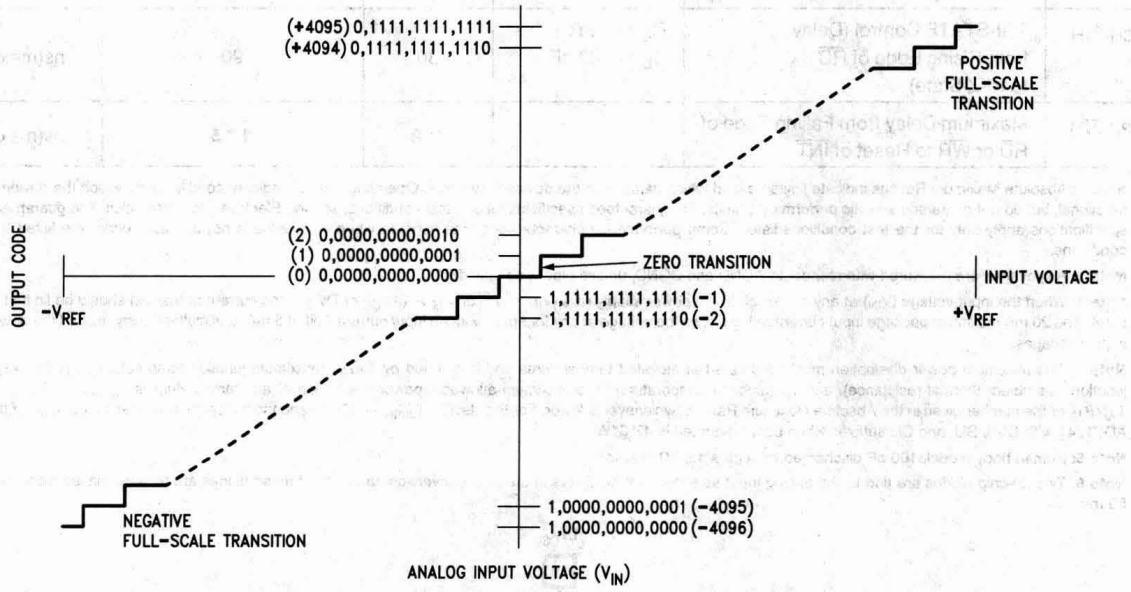

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FIGURE 1a. Transfer Characteristic

AC Electrical Characteristics (Continued)

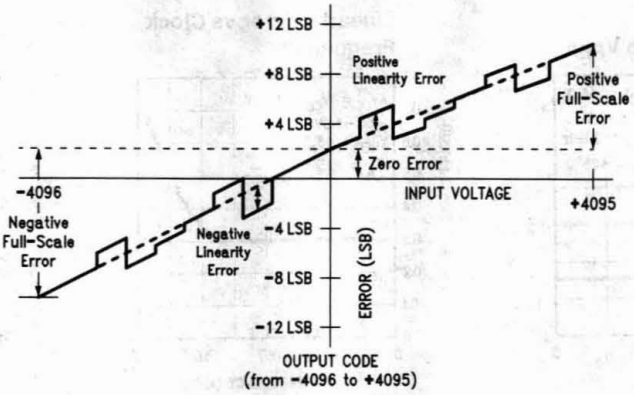

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FIGURE 1b. Simplified Error Curve vs Output Code Without Auto-Cal or Auto-Zero Cycles

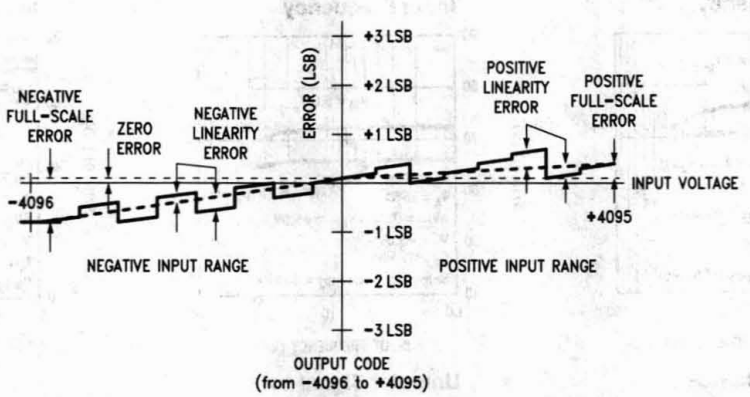

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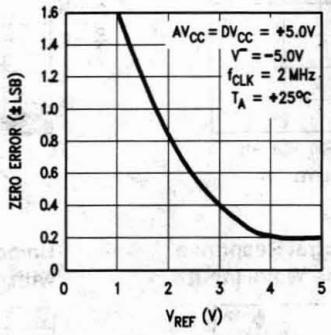
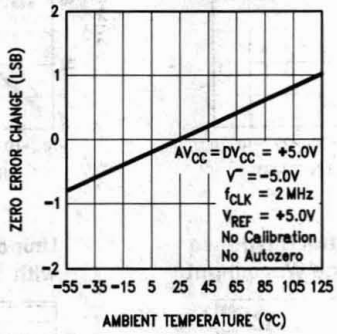
FIGURE 1c. Simplified Error Curve vs Output Code After Auto-Cal Cycle

Typical Performance Characteristics

Zero Error vs V_{REF}



Zero Error Change vs Ambient Temperature



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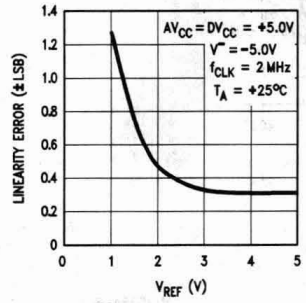
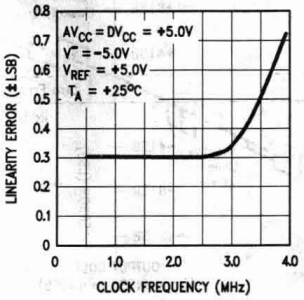
Typical Performance Characteristics (Continued)

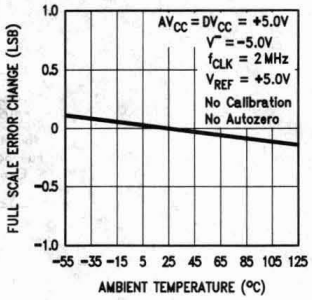
Linearity Error vs V_{REF}



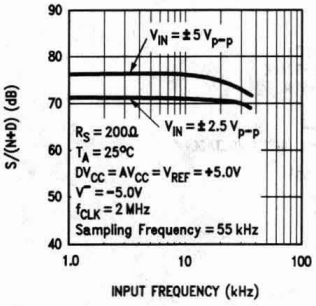
Linearity Error vs Clock Frequency



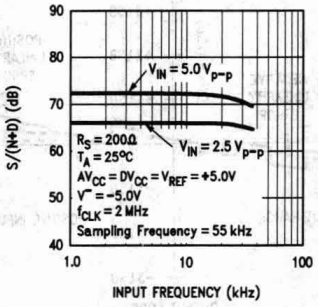
Full Scale Error Change vs Ambient Temperature



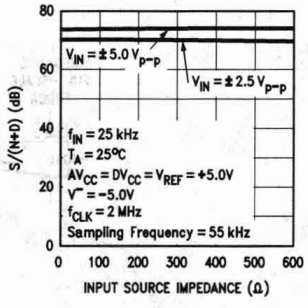
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



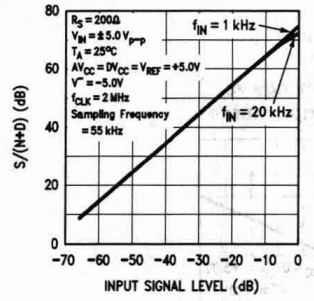
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



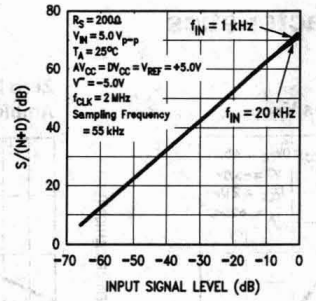
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance


VIN = ±5.0 Vp-p
VIN = ±2.5 Vp-p
fIN = 25 kHz
TA = 25°C
AVCC = DVCC = VREF = +5.0V
V⁻ = −5.0V
fCLK = 2 MHz
Sampling Frequency = 55 kHz
S/(N+D) (dB)
INPUT SOURCE IMPEDANCE (Ω)

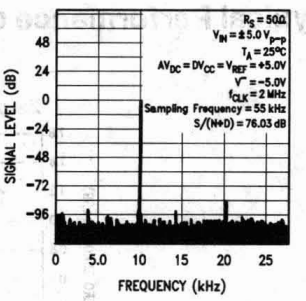
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



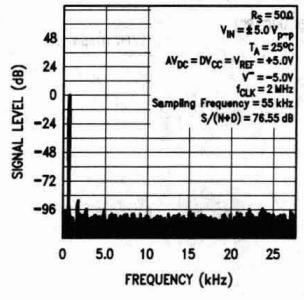
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



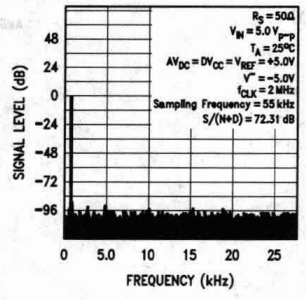
Bipolar Spectral Response with 10 kHz Sine Wave Input



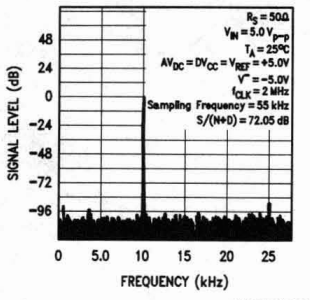
Bipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 10 kHz Sine Wave Input



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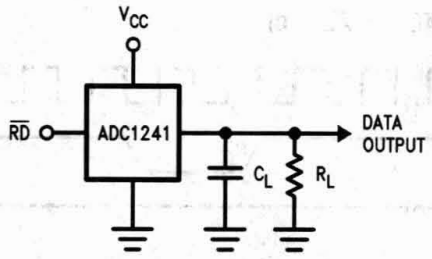
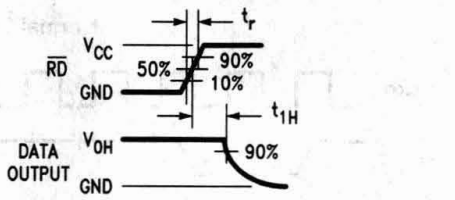
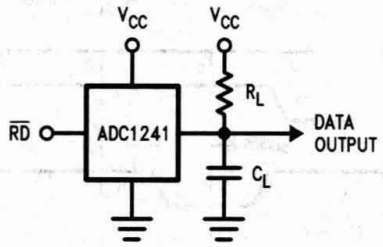
Test Circuits



TL/H/10554–9



TL/H/10554–10



TL/H/10554–11

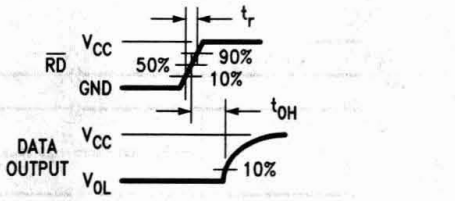


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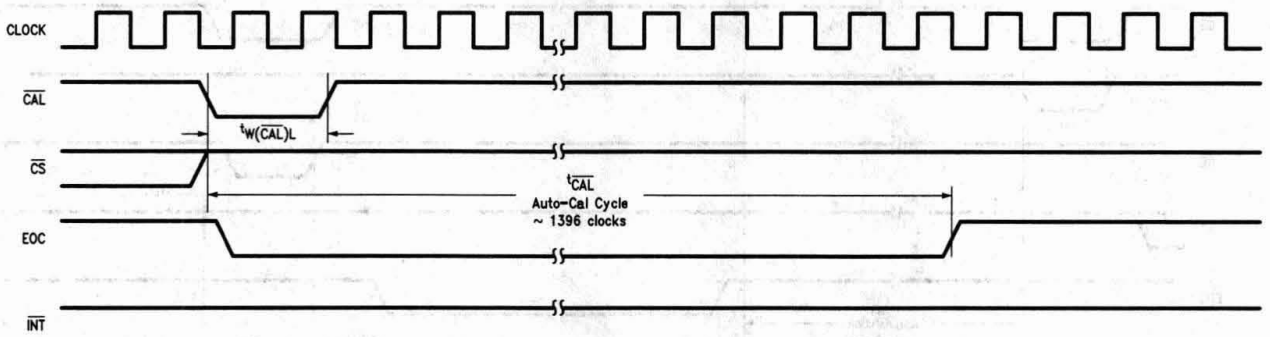
FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Auto-Cal Cycle ($\overline{CS}$ = 1, $\overline{WR}$ = X, $\overline{RD}$ = X, $\overline{AZ}$ = X, X = Don't Care)



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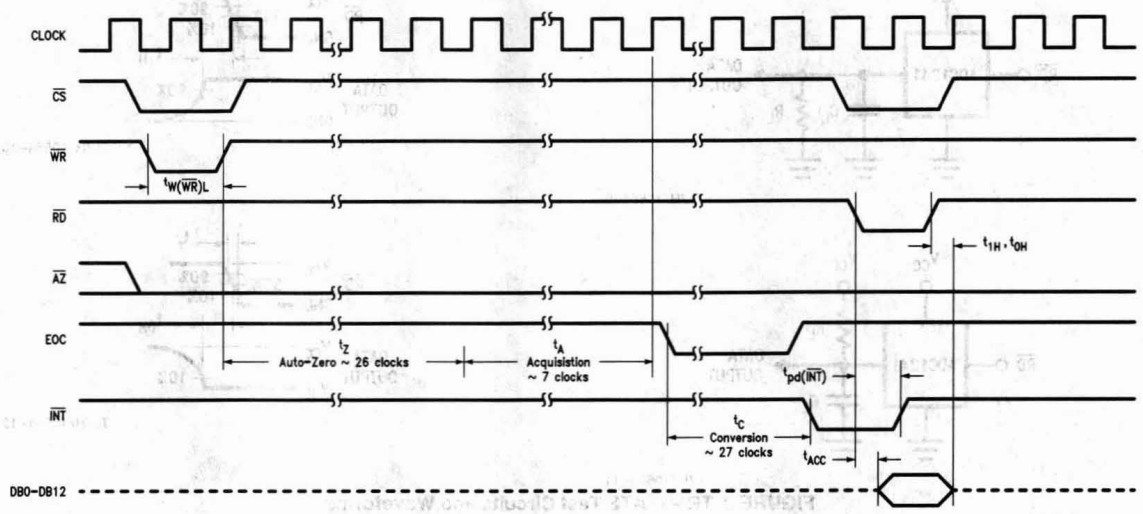
Timing Diagrams (Continued)

Normal Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



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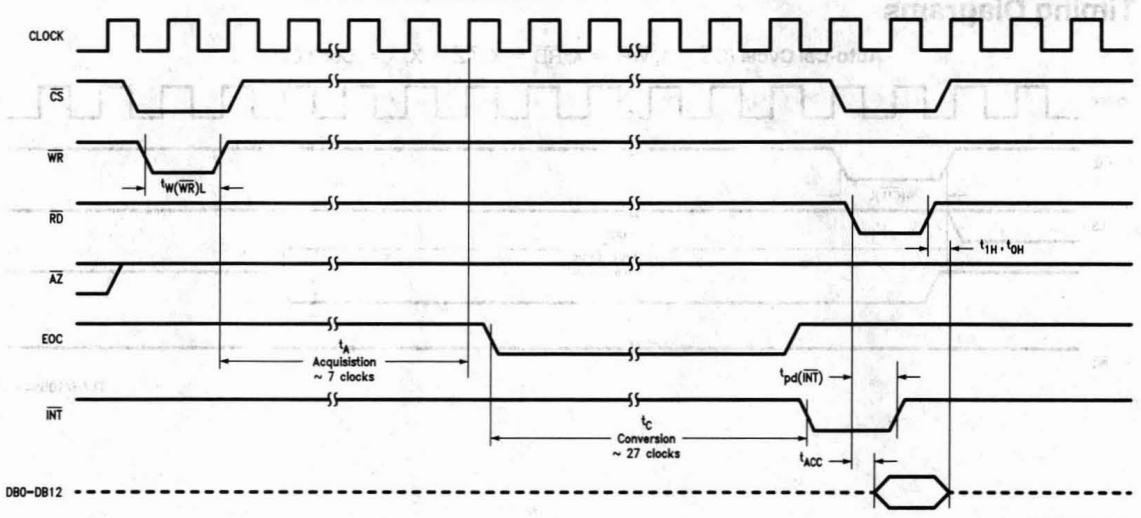
Normal Conversion without Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 1)



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1.0 Pin Descriptions

DV_{CC} (28), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC1241 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass filters (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs a bypass filter of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (14), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below 3.5 VDC.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$ and $\overline{RD}$ functions.

$\overline{RD}$ (11) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The converison is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low.

CLK (8) — The external clock input pin. The clock frequency range is 500 kHz to 4 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC1241 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC1241 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (12) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (13) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0–DB12 (15–27) — The TRI-STATE output pins. The output is in two's complement format with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC1241 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Cal routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC1241 without the need of trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC1241 at any time, which ensures its long term stability.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1396 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch error is found. Correction factors for these errors are then stored in internal RAM.

A conversion is initiated by taking $\overline{CS}$ and $\overline{WR}$ low. The $\overline{AZ}$ (Auto Zero) signal line should be tied high or low during the conversion process. If $\overline{AZ}$ is low an auto zero cycle, which takes approximately 26 clock periods, occurs before the actual conversion is started. The auto zero cycle determines the correction factors for the comparator's offset voltage. If $\overline{AZ}$ is high, the auto zero cycle is skipped. Next the analog input is sampled for 7 clock periods, and held in the capacitive DAC's ladder structure. The EOC then goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC1241. Next EOC goes high, and $\overline{INT}$ goes low to signal the end of the conversion. The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0–DB12 output buffers.

2.0 Functional Description (Continued)

Digital Control Inputs					A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊓	⊓	1	1	1	Start Conversion without Auto-Zero
⊓	1	⊓	1	1	Read Conversion Result without Auto-Zero
⊓	⊓	1	1	0	Start Conversion with Auto-Zero
⊓	1	⊓	1	0	Read Conversion Result with Auto-Zero
1	X	X	⊓	X	Start Calibration Cycle
0	X	1	0	X	Test Mode (DB2, DB3, DB5 and DB6 become active)

FIGURE 1. Function of the A/D Control Inputs

The table in *Figure 1* summarizes the effect of the digital control inputs on the function of the ADC1241. The Test Mode, where $\overline{RD}$ is high and $\overline{CS}$ and $\overline{CAL}$ are low, is used by the factory to thoroughly check out the operation of the ADC1241. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

All internal logic can be reset, which will abort any conversion in process. The A/D is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore making it necessary to do an Auto-Cal cycle before the next conversion. This is true with or without Auto-Zero. The Calibration Cycle cannot be reset once started. On power-up the ADC1241 automatically goes through a Calibration Cycle that takes typically 1396 clock cycles.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 2* is an example of a very stable reference that is appropriate for use with the ADC1241.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for given input condition.

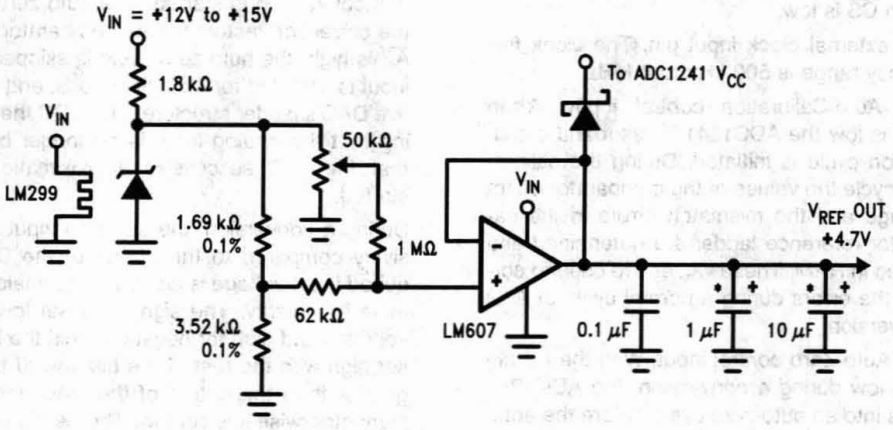

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FIGURE 2. Low Drift Extremely Stable Reference Circuit

3.0 Analog Considerations (Continued)

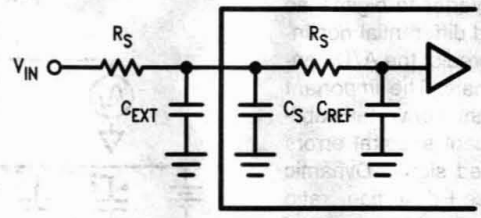

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FIGURE 3. Analog Input Equivalent Circuit

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 INPUT CURRENT

A charging current will flow into or out of (depending on the input voltage polarity) of the analog input pin (V_{IN}) on the start of the analog input sampling period (t_A). The peak value of this current will depend on the actual input voltage applied.

3.3 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.4 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 3*. External R_S will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With f_{CLK} = 2 MHz t_A = 7 clock periods = 3.5 μs, $R_S \leq 1\ k\Omega$ will allow a 5V analog input voltage to settle properly.

3.5 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.6 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the auto-zero or auto-cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors whould be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.7 THE CALIBRATION CYCLE

On power up the ADC1241 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall gain, offset, and linearity errors down to the specified limits. It should be necessary to go through the calibration cycle only once after power up.

3.8 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature changes significantly. (See the curved titled "Zero Error Change vs Ambient Temperature" in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than ±1 LSB. An auto-zero cycle will maintain the zero error to ±1 LSB or less.

4.0 Dynamic Performance

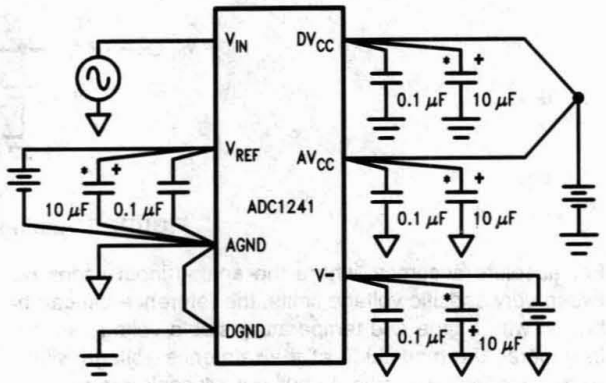
Many applications require the A/D converter to digitize ac signals, but the standard dc integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with ac input signals. The important specifications for ac applications reflect the converter's ability to digitize ac signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise+distortion ratio (S/(N+D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's ac performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N+D) is calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/(N+D) are shown in the table of Electrical Characteristics, and spectral plots are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N+D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N+D) drops 3 dB).

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC1241 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC1241, the hold command is internally generated. When the Auto-Zero function is not being used, the hold command occurs at the end of the acquisition window, or seven clock periods after the rising edge of the $\overline{WR}$. The delay between the internally generated hold command and the time that the ADC1241 actually holds the input signal is the aperture time. For the ADC1241, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC1241 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

Power Supply Bypassing



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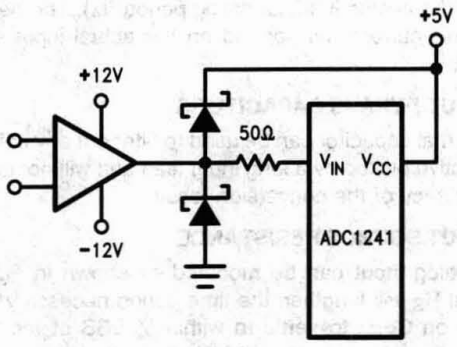
Protecting the Analog Inputs



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National Semiconductor

ADC1242
12-Bit Plus Sign Sampling A/D Converter

General Description

The ADC1242 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter. On request, the ADC1242 goes through a self-calibration cycle that adjusts positive linearity error to less than ±1 LSB full-scale error to less than ±3 LSB, and zero error to less than ±2 LSB. The ADC1242 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC1242 is tracked and held by the internal circuitry, and therefore does not require an external sample-and-hold. A unipolar analog input voltage range (0V to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit word on the outputs of the ADC1242 gives a 2's complement representation of negative numbers. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Key Specifications

■ Resolution	12 Bits plus Sign
■ Conversion Time	13.8 μs (max)
■ Linearity Error	±1 LSB (± 0.0244%) (max)
■ Zero Error	±2 LSB (max)
■ Positive Full Scale Error	±3 LSB (max)
■ Power Consumption	70 mW (max)

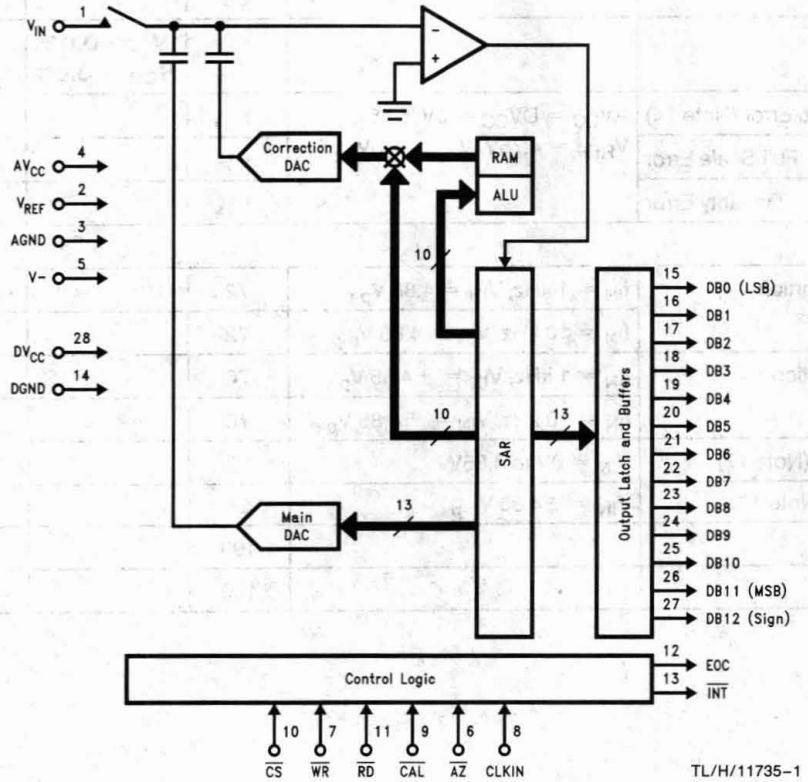
Features

- Self-calibrating
- Internal sample-and-hold
- Bipolar input range with ±5V supplies and single +5V reference
- No missing codes over temperature
- TTL/MOS input/output compatible
- Standard 28-pin ceramic DIP

Applications

- Digital Signal Processing
- High Resolution Process Control
- Instrumentation

Simplified Schematic



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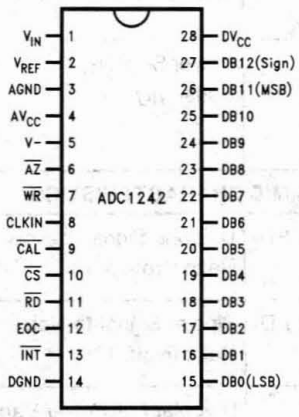
Connection Diagram

Dual-In-Line Package



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Top View

Order Number ADC1242CIJ
See NS Package Number J28A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Input (V_{IN})	(V^- −0.3V) to (V_{CC} + 0.3V)
AV_{CC}-DV_{CC} (Note 7)	0.3V
Input Current at any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information J Package (10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1242CIJ	−40°C ≤ T_A ≤ +85°C
DV_{CC} and AV_{CC} Voltage (Notes 6 and 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 and 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +4.096V, and f_{CLK} = 2.0 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Notes 10, 18)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error		After Auto-Cal (Notes 11 and 12)		**±1**	LSB(max)
	Differential Linearity		After Auto-Cal (Notes 11 and 12)		**12**	Bits(min)
	Zero Error		After Auto-Zero or Auto-Cal (Notes 12 and 13)		**±2**	LSB(max)
	Positive and Negative Full-Scale Error		After Auto-Cal (Note 12)		**±3**	LSB(max)
C_{REF}	V_{REF} Input Capacitance			80		pF
C_{IN}	Analog Input Capacitance			65		pF
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB
DYNAMIC CHARACTERISTICS						
S/(N+D)	Unipolar Signal-to-Noise+Distortion Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	72		dB
			f_{IN} = 10 kHz, V_{IN} = 4.85 V_{p-p}	72		dB
S/(N+D)	Bipolar Signal-to-Noise+Distortion Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85 V_{p-p}	76		dB
			f_{IN} = 10 kHz, V_{IN} = ±4.85 V_{p-p}	76		dB
	Unipolar Full Power Bandwidth (Note 17)		V_{IN} = 0V to 4.85V	32		kHz
	Bipolar Full Power Bandwidth (Note 17)		V_{IN} = ±4.85 V_{p-p}	25		kHz
t_{Ap}	Aperture Time			100		ns
	Aperture Jitter			100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +4.096V$, and $f_{CLK} = 2.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Condition	Typical (Note 9)	Limit (Notes 10, 18)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	$V_{CC} = 5.25V$		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	$V_{CC} = 4.75V$		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1**	μA(max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**	μA(max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V(min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V(max)
V_H	CLK IN Hysteresis $[V_T^+(min) - V_T^-(max)]$		0.7	**0.4**	V(min)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**	V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = 1.6$ mA		**0.4**	V(max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA(max)
		$V_{OUT} = 5V$	0.01	**3**	μA(max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA(min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA(min)
DI_{CC}	DV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	1	**2**	mA(max)
AI_{CC}	AV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA(max)
I^-	V^- Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA(max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 18)	Units (Limits)
f_{CLK}	Clock Frequency			**2.0**	MHz
			0.5		MHz(min)
			4.0		MHz(max)
	Clock Duty Cycle		50		%
				40	%(min)
				60	%(max)
t_C	Conversion Time		$27(1/f_{CLK})$	**$27(1/f_{CLK}) + 300$ ns**	(max)
		$f_{CLK} = 2.0$ MHz	13.5		μs
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$	$7(1/f_{CLK})$	**$7(1/f_{CLK}) + 300$ ns**	(max)
		$f_{CLK} = 2.0$ MHz	3.5		μs
t_Z	Auto Zero Time		26	**26**	$1/f_{CLK}$(max)
		$f_{CLK} = 2.0$ MHz	13		μs
$t_{\overline{CAL}}$	Calibration Time		1396		$1/f_{CLK}$
		$f_{CLK} = 2.0$ MHz	698	**706**	μs(max)
$t_{W(\overline{CAL})L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns(min)
$t_{W(\overline{WR})L}$	Minimum $\overline{WR}$ Pulse Width		60	**200**	ns(min)
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	85	ns(max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	90	ns(max)
$t_{PD(\overline{INT})}$	Maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns(max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

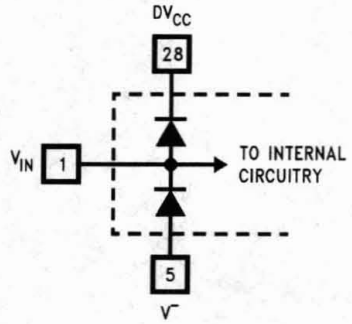
Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > (AV_{CC}$ or $DV_{CC})$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 125°C$, and the typical thermal resistance (θ_{JA}) of the ADC1242 CIJ when board mounted is 47°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV.



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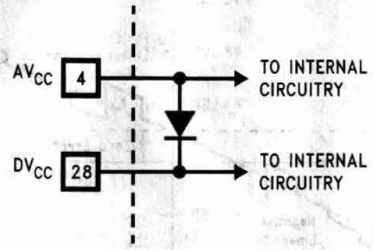
This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (−4.75 V_{DC}), full-scale must be ≤ 4.8 V_{DC}.

AC Electrical Characteristics (Continued)

Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at f_{CLK} = 2.0 MHz. At higher and lower clock frequencies accuracy may degrade. See curves in the Typical Performance Characteristics Section.

Note 9: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*).

Note 12: The ADC1242's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started, see the typical performance characteristic curves.

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

Note 15: If the clock is asynchronous to the falling edge of $\overline{WR}$ an uncertainty of one clock period will exist in the interval of t_A, therefore making the minimum t_A = 6 clock periods and the maximum t_A = 7 clock periods. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods.

Note 16: The $\overline{CAL}$ line must be high before any other conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: A military RETS electrical test specification is available upon request. At time of printing, the ADC1241CMJ/883 RETS specification complies fully with the **boldface** limits in this column.

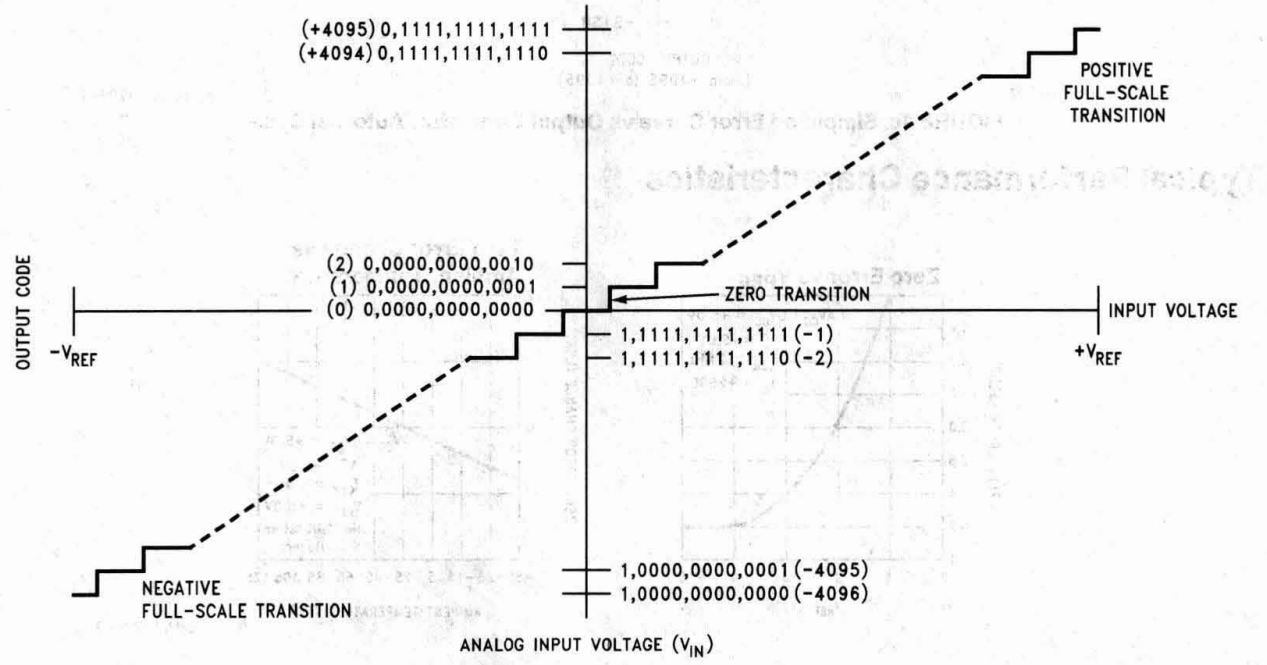

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FIGURE 1a. Transfer Characteristic

AC Electrical Characteristics (Continued)

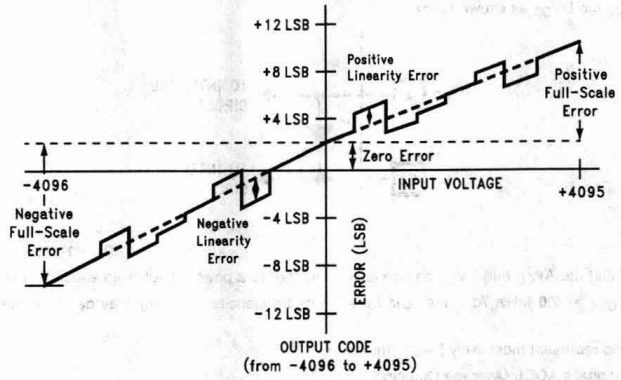

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Cal or Auto-Zero Cycles

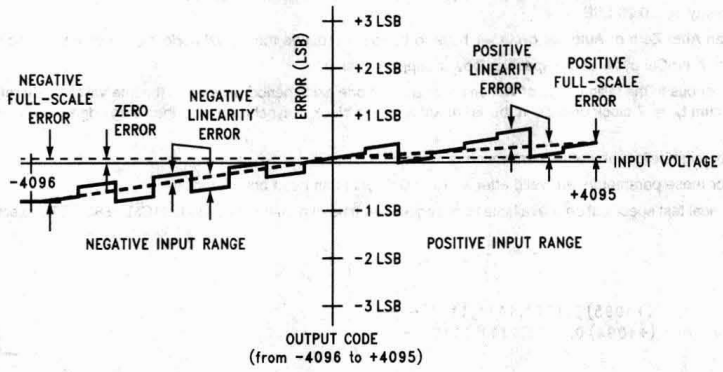

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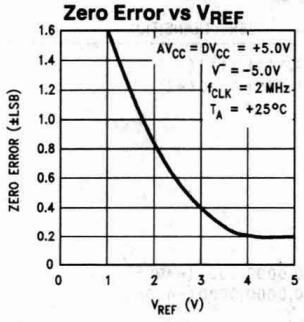
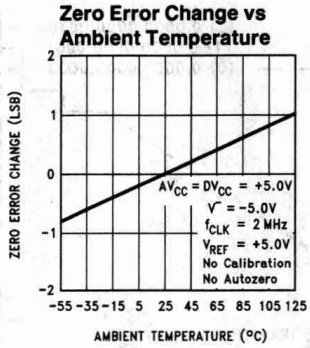
FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Cal Cycle

Typical Performance Characteristics





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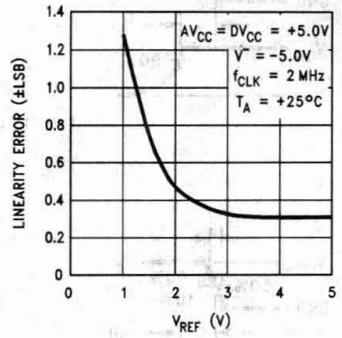
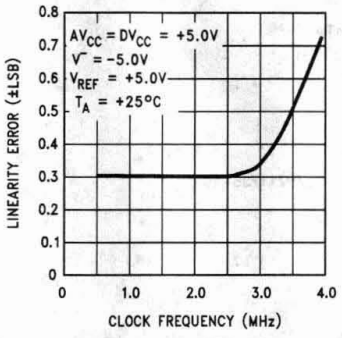
Typical Performance Characteristics (Continued)

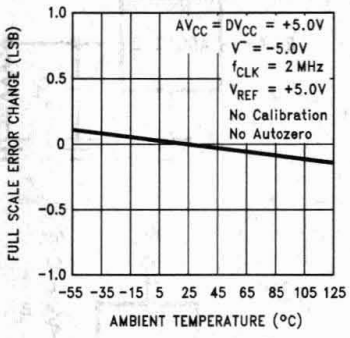
Linearity Error vs V_{REF}



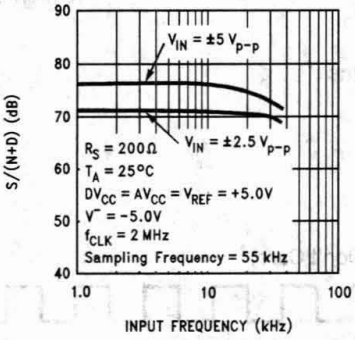
Linearity Error vs Clock Frequency



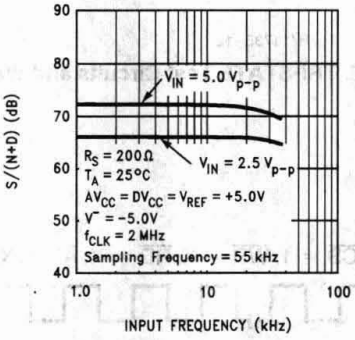
Full Scale Error Change vs Ambient Temperature



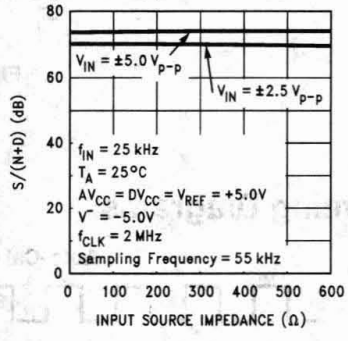
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



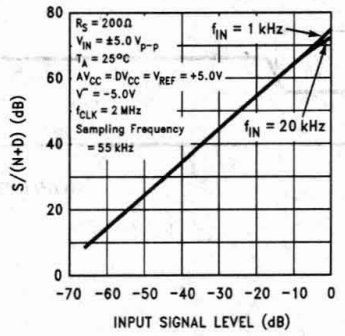
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



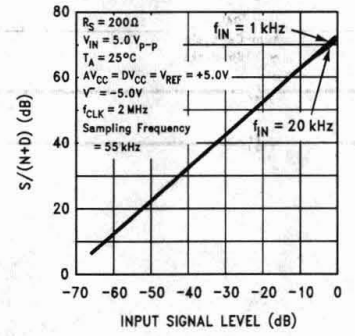
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance


VIN = ±5.0 Vp-p
VIN = ±2.5 Vp-p
fIN = 25 kHz
TA = 25°C
AVCC = DVCC = VREF = +5.0V
V⁻ = −5.0V
fCLK = 2 MHz
Sampling Frequency = 55 kHz
S/(N+D) (dB)
INPUT SOURCE IMPEDANCE (Ω)

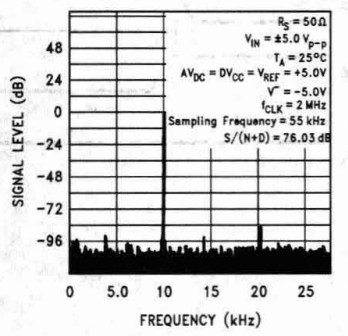
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



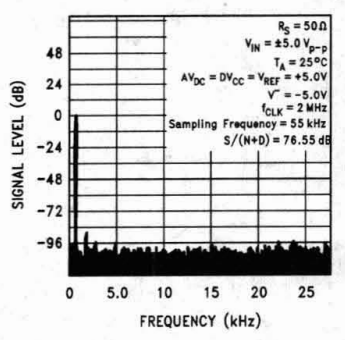
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



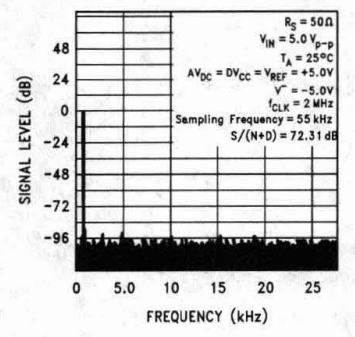
Bipolar Spectral Response with 10 kHz Sine Wave Input



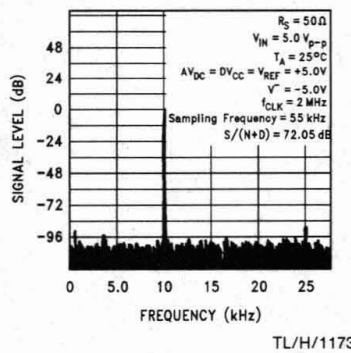
Bipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 10 kHz Sine Wave Input



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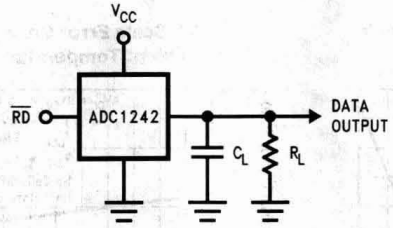
2

Test Circuits



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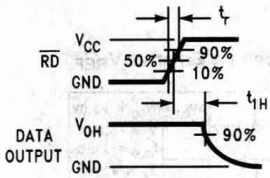

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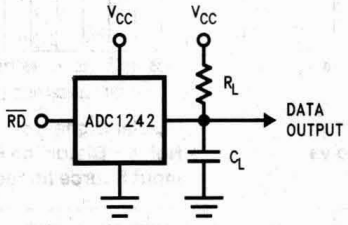

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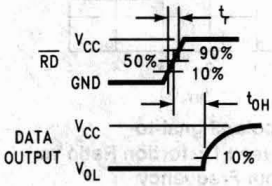

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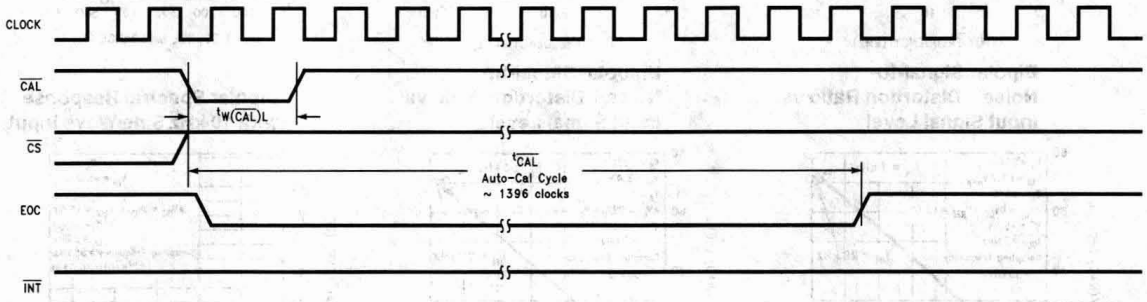
FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Auto-Cal Cycle ($\overline{CS}$ = 1, $\overline{WR}$ = X, $\overline{RD}$ = X, $\overline{AZ}$ = X, X = Don't Care)



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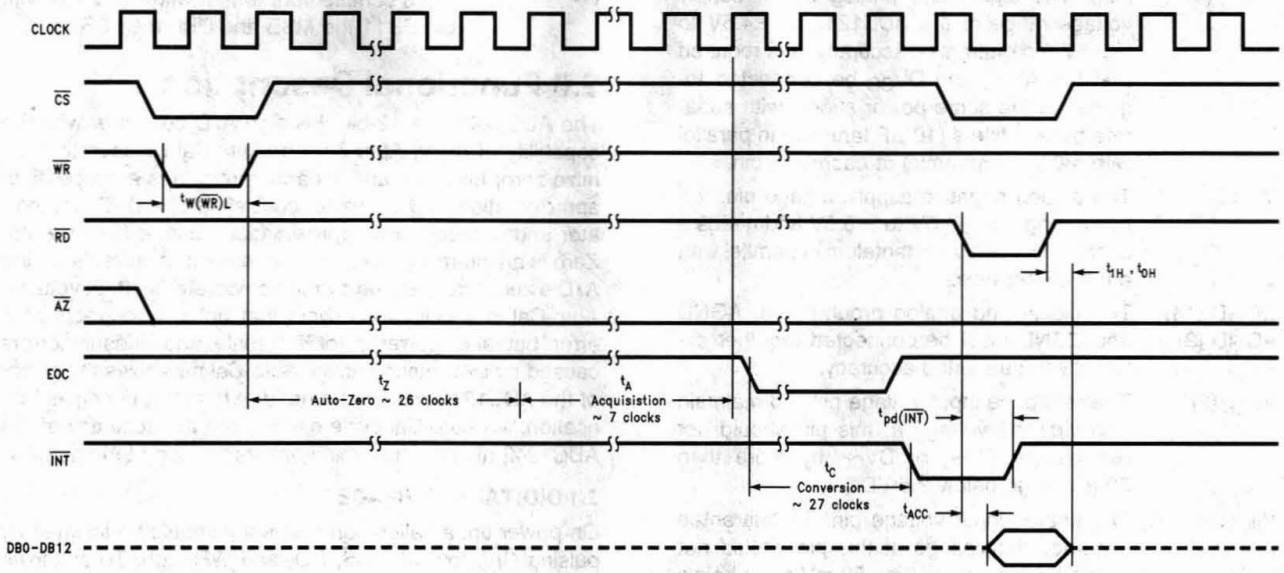
Timing Diagrams (Continued)

Normal Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



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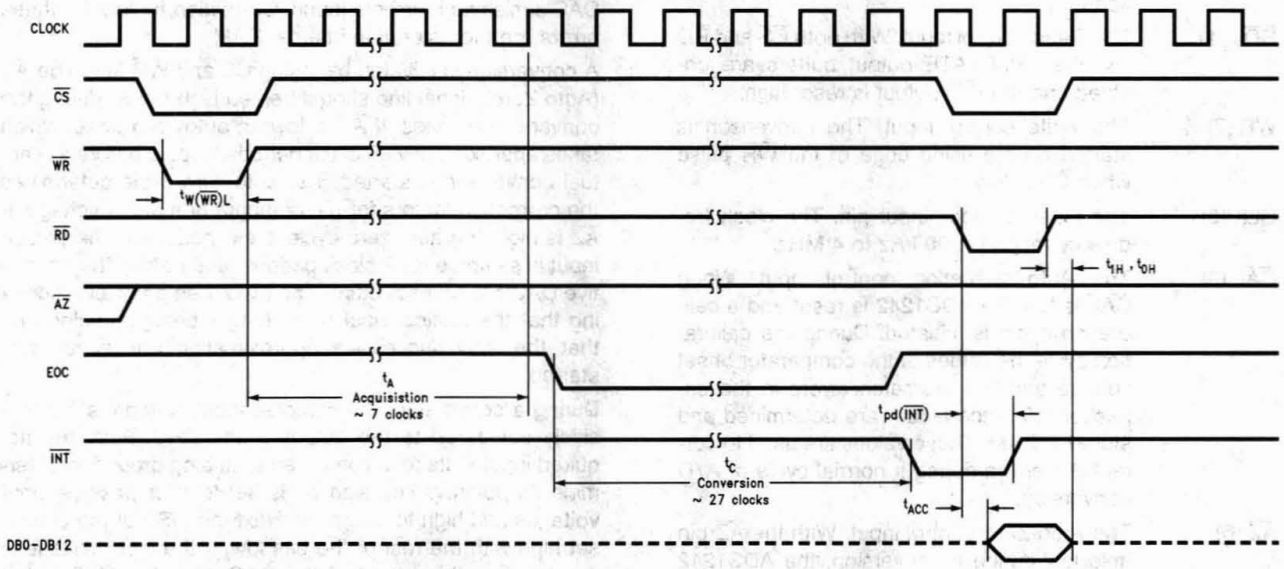
Normal Conversion without Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 1)



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2

1.0 Pin Descriptions

DV_{CC} (28), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC1242 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass filters (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs a bypass filter of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (14), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below 3.5 VDC.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$ and $\overline{RD}$ functions.

$\overline{RD}$ (11) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The converison is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low.

CLK (8) — The external clock input pin. The clock frequency range is 500 kHz to 4 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC1242 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC1242 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (12) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (13) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0–DB12 (15–27) — The TRI-STATE output pins. The output is in two's complement format with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC1242 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Cal routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC1242 without the need of trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC1242 at any time, which ensures its long term stability.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1396 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch error is found. Correction factors for these errors are then stored in internal RAM.

A conversion is initiated by taking $\overline{CS}$ and $\overline{WR}$ low. The $\overline{AZ}$ (Auto Zero) signal line should be tied high or low during the conversion process. If $\overline{AZ}$ is low an auto zero cycle, which takes approximately 26 clock periods, occurs before the actual conversion is started. The auto zero cycle determines the correction factors for the comparator's offset voltage. If $\overline{AZ}$ is high, the auto zero cycle is skipped. Next the analog input is sampled for 7 clock periods, and held in the capacitive DAC's ladder structure. The EOC then goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC1242. Next EOC goes high, and $\overline{INT}$ goes low to signal the end of the conversion. The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0–DB12 output buffers.

2.0 Functional Description (Continued)

Digital Control Inputs					A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⌐	⌐	1	1	1	Start Conversion without Auto-Zero
⌐	1	⌐	1	1	Read Conversion Result without Auto-Zero
⌐	⌐	1	1	0	Start Conversion with Auto-Zero
⌐	1	⌐	1	0	Read Conversion Result with Auto-Zero
1	X	X	⌐	X	Start Calibration Cycle
0	X	1	0	X	Test Mode (DB2, DB3, DB5 and DB6 become active)

FIGURE 3. Function of the A/D Control Inputs

The table in *Figure 3* summarizes the effect of the digital control inputs on the function of the ADC1242. The Test Mode, where $\overline{RD}$ is high and $\overline{CS}$ and $\overline{CAL}$ are low, is used by the factory to thoroughly check out the operation of the ADC1242. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

All internal logic can be reset, which will abort any conversion in process. The A/D is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore making it necessary to do an Auto-Cal cycle before the next conversion. This is true with or without Auto-Zero. The Calibration Cycle cannot be reset once started. On power-up the ADC1242 automatically goes through a Calibration Cycle that takes typically 1396 clock cycles.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 4* is an example of a very stable reference that is appropriate for use with the ADC1242.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for given input condition.

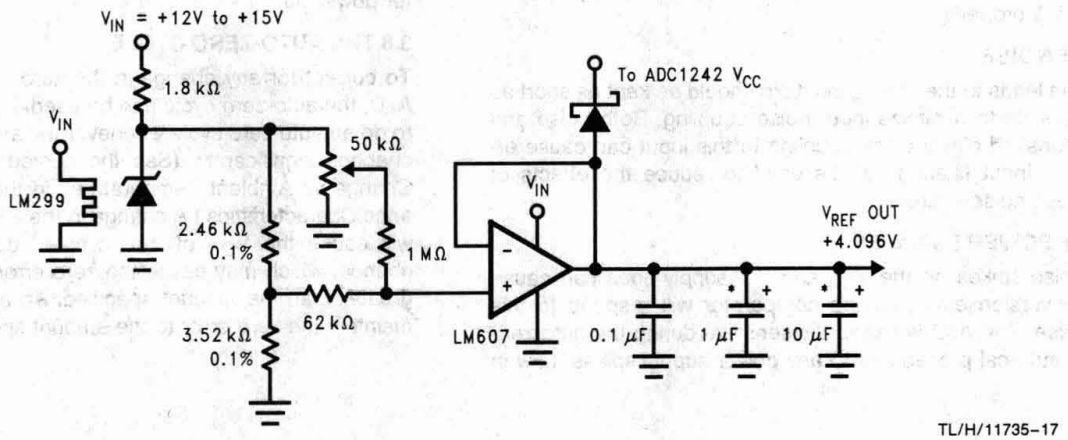

FIGURE 4. Low Drift Extremely Stable Reference Circuit

3.0 Analog Considerations (Continued)

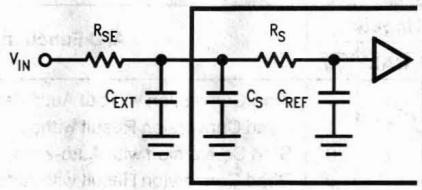

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FIGURE 5. Analog Input Equivalent Circuit

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 INPUT CURRENT

A charging current will flow into or out of (depending on the input voltage polarity) of the analog input pin (V_{IN}) on the start of the analog input sampling period (t_A). The peak value of this current will depend on the actual input voltage applied.

3.3 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.4 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 5.* External R_{SE} will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With f_{CLK} = 2 MHz t_A = 7 clock periods = 3.5 μs, $R_{SE} \leq 1\ k\Omega$ will allow a 5V analog input voltage to settle properly.

3.5 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.6 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the auto-zero or auto-cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors whould be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.7 THE CALIBRATION CYCLE

On power up the ADC1242 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall gain, offset, and linearity errors down to the specified limits. It should be necessary to go through the calibration cycle only once after power up.

3.8 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature changes significantly. (See the curved titled "Zero Error Change vs Ambient Temperature" in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than the amount specified. An auto-zero cycle will maintain the zero error to the amount specified or less.

4.0 Dynamic Performance

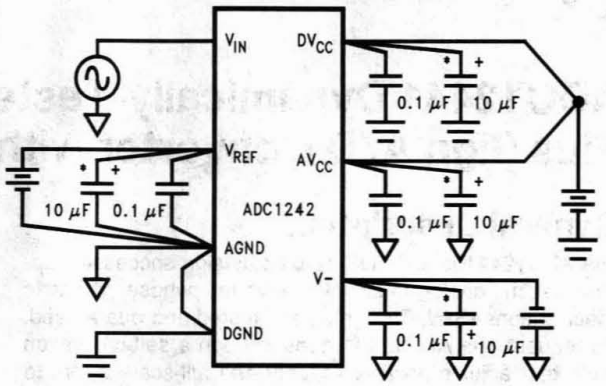
Many applications require the A/D converter to digitize ac signals, but the standard dc integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with ac input signals. The important specifications for ac applications reflect the converter's ability to digitize ac signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise+distortion ratio (S/(N+D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's ac performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N+D) is calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/(N+D) are shown in the table of Electrical Characteristics, and spectral plots are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N+D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N+D) drops 3 dB).

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC1242 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC1242, the hold command is internally generated. When the Auto-Zero function is not being used, the hold command occurs at the end of the acquisition window, or seven clock periods after the rising edge of the $\overline{WR}$. The delay between the internally generated hold command and the time that the ADC1242 actually holds the input signal is the aperture time. For the ADC1242, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC1242 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

Power Supply Bypassing



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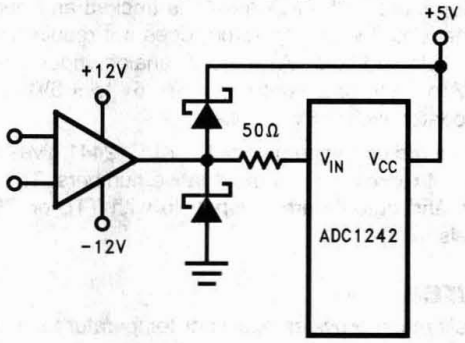
*Tantalum

Protecting the Analog Inputs



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National Semiconductor

ADC12441 Dynamically-Tested Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample-and-Hold

General Description

The ADC12441 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter whose dynamic specifications (S/N, THD, etc.) are tested and guaranteed. On request, the ADC12441 goes through a self-calibration cycle that adjusts positive linearity and full-scale errors to less than ±½ LSB each and zero error to less than ±1 LSB. The ADC12441 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC12441 is tracked and held by the internal circuitry, and therefore does not require an external sample-and-hold. A unipolar analog input voltage range (0V to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit word on the outputs of the ADC12441 gives a 2's complement representation of negative numbers. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Applications

- Digital signal processing
- Telecommunications
- Audio
- High resolution process control
- Instrumentation

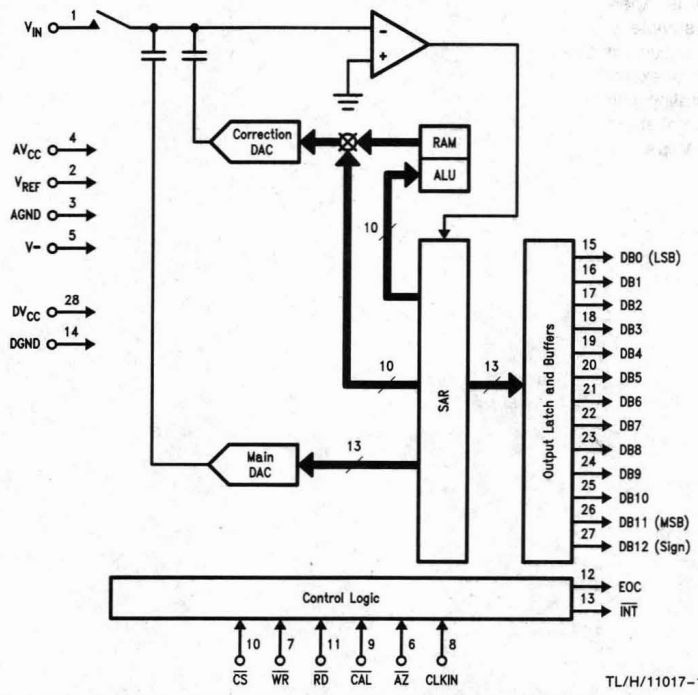
Key Specifications

■ Resolution	12 bits plus sign
■ Conversion Time	13.8 μs (max)
■ Bipolar Signal/Noise	76.5 dB (min)
■ Total Harmonic Distortion	−75 dB (max)
■ Aperture Time	100 ns
■ Aperture Jitter	100 ps_{rms}
■ Zero Error	±1 LSB (max)
■ Positive Full Scale Error	±1 LSB (max)
■ Power Consumption @ ±5V	70 mW (max)
■ Sampling rate	55 kHz (max)

Features

- Self-calibration provides excellent temperature stability
- Internal sample-and-hold
- Bipolar input range with single +5V reference

Simplified Block Diagram



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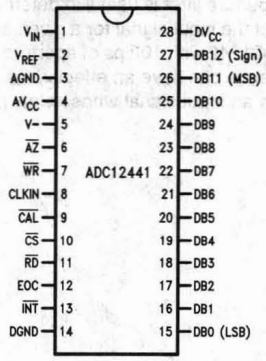
Connection Diagram

Dual-In-Line Package



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Top View

Order Number
ADC12441CMJ, ADC12441CMJ/883
or ADC12441CIJ
See NS Package Number J28A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Inputs (V_{IN} and V_{REF})	(V^- − 0.3V) to (V_{CC} + 0.3V)
AV_{CC}–DV_{CC} (Note 7)	0.3V
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information J Package (10 sec.)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12441CIJ	$-40°C \le T_A \le +85°C$
ADC12441CMJ, ADC12441CMJ/883	$-55°C \le T_A \le +125°C$
DV_{CC} and AV_{CC} Voltage (Notes 6 & 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 & 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +5.0V, Analog Input Source Impedance = 600Ω, and f_{CLK} = 2.0 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Note 10)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error		After Auto-Cal (Notes 11 & 12)	±½		LSB
	Negative Integral Linearity Error		After Auto-Cal (Notes 11 & 12)	±¾		LSB
	Positive or Negative Differential Linearity		After Auto-Cal (Notes 11 & 12)	12		Bits
	Zero Error		After Auto-Zero or Auto-Cal (Notes 12 & 13)		**±1**	LSB (max)
	Positive Full-Scale Error		After Auto-Cal (Note 12)	±½	**±1**	LSB (max)
	Negative Full-Scale Error		After Auto-Cal (Note 12)		**±1 / ±2**	LSB (max)
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB
C_{REF}	V_{REF} Input Capacitance (Note 18)			80		pF
C_{IN}	Analog Input Capacitance			65		pF
DYNAMIC CHARACTERISTICS						
	Bipolar Effective Bits (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85V	12.6		Bits
			f_{IN} = 20 kHz, V_{IN} = ±4.85V	12.6	**12.4**	Bits (min)
	Unipolar Effective Bits (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	11.8		Bits
			f_{IN} = 20 kHz, V_{IN} = 4.85 V_{p-p}	11.8	**11.6**	Bits (min)
S/N	Bipolar Signal-to-Noise Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85V	78		dB
			f_{IN} = 10 kHz, V_{IN} = ±4.85V	78		dB
			f_{IN} = 20 kHz, V_{IN} = ±4.85V	78	**76.5**	dB (min)
S/N	Unipolar Signal-to-Noise Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	73		dB
			f_{IN} = 10 kHz, V_{IN} = 4.85 V_{p-p}	73		dB
			f_{IN} = 20 kHz, V_{IN} = 4.85 V_{p-p}	73	**71.5**	dB (min)

Converter Electrical Characteristics

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, Analog Input Source Impedance = 600Ω, and f_{CLK} = 2.0 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8) (Continued)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
DYNAMIC CHARACTERISTICS (Continued)					
THD	Bipolar Total Harmonic Distortion (Note 17)	f_{IN} = 1 kHz, $V_{IN} = \pm 4.85V$	−82		dB
		f_{IN} = 19.688 kHz, $V_{IN} = \pm 4.85V$	−80	**−75**	dB (max)
THD	Unipolar Total Harmonic Distortion (Note 17)	f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	−82		dB
		f_{IN} = 19.688 kHz, V_{IN} = 4.85 V_{p-p}	−80	**−75**	dB (max)
	Bipolar Peak Harmonic or Spurious Noise (Note 17)	f_{IN} = 1 kHz, $V_{IN} = \pm 4.85V$	−88		dB
		f_{IN} = 10 kHz, $V_{IN} = \pm 4.85V$	−84		dB
		f_{IN} = 20 kHz, $V_{IN} = \pm 4.85V$	−80		dB
	Unipolar Peak Harmonic or Spurious Noise (Note 17)	f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	−90		dB
		f_{IN} = 10 kHz, V_{IN} = 4.85 V_{p-p}	−86		dB
		f_{IN} = 20 kHz, V_{IN} = 4.85 V_{p-p}	−82		dB
	Bipolar Two Tone Intermodulation Distortion (Note 17)	$V_{IN} = \pm 4.85V$, f_{IN1} = 19.375 kHz, f_{IN2} = 20.625 kHz	−78	**−74**	dB (max)
	Unipolar Two Tone Intermodulation Distortion (Note 17)	V_{IN} = 4.85 V_{p-p}, f_{IN1} = 19.375 kHz, f_{IN2} = 20.625 kHz	−78	**−73**	dB (max)
	−3 dB Bipolar Full Power Bandwidth	$V_{IN} = \pm 4.85V$ (Note 17)	25	**20**	kHz (Min)
	−3 dB Unipolar Full Power Bandwidth	V_{IN} = 4.85 V_{p-p} (Note 17)	30	**20**	kHz (Min)
	Aperture Time		100		ns
	Aperture Jitter		100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and f_{CLK} = 2.0 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	V_{CC} = 5.25V		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	V_{CC} = 4.75V		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5V	0.005	**1**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−0.005	**−1**	μA (max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V (min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V (max)
V_H	CLK IN Hysteresis [V_T^+ (min) − V_T^- (max)]		0.7	**0.4**	V (min)
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_{OUT} = 1.6 mA		**0.4**	V (max)

Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 2.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7) (Continued)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limits)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA (max)
		$V_{OUT} = 5V$	0.01	**3**	μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA (min)
DI_{CC}	DV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	1	**2**	mA (max)
AI_{CC}	AV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA (max)
I^-	V^- Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA (max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limits)
f_{CLK}	Clock Frequency		0.5 4.0	 **2.0**	MHz (min) MHz (max)
	Clock Duty Cycle		50	 **40** **60**	% % (min) % (max)
t_C	Conversion Time		$27(1/f_{CLK})$	**$27(1/f_{CLK}) + 300$ ns**	(max)
		$f_{CLK} = 2.0$ MHz	13.5		μs
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$, $f_{CLK} = 2.0$ MHz	$7(1/f_{CLK})$	**$7(1/f_{CLK}) + 300$ ns**	(max)
			3.5		μs
t_Z	Auto Zero Time		$26(1/f_{CLK})$	**$26(1/f_{CLK})$**	(max)
		$f_{CLK} = 2.0$ MHz	13		μs
t_{CAL}	Calibration Time		$1396(1/f_{CLK})$		max
		$f_{CLK} = 2.0$ MHz	698	**706**	μs (max)
$t_{W(CAL)L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns (min)
$t_{W(WR)L}$	Minimum $\overline{WR}$ Pulse Width		60	**200**	ns (min)
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	85	ns (max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	90	ns (max)
$t_{PD(INT)}$	Maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

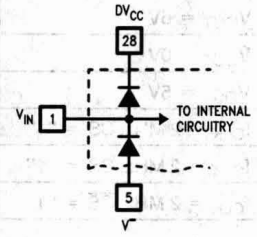
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > (AV_{CC}$ or $DV_{CC})$, the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

AC Electrical Characteristics (Continued)

Note 4: The power dissipation of this device under normal operation should never exceed 169 mW (Quiescent Power Dissipation + TTL Loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (ex. when any inputs or outputs exceed the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 125°C$, and the typical thermal resistance (θ_{JA}) of the ADC12441 with CMJ and CIJ suffixes when board mounted is 47°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV.



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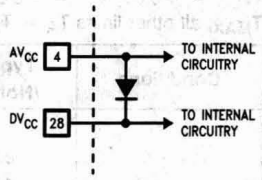
This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (−4.75 V_{DC}), full-scale must be ≤ 4.8 V_{DC}.

Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at $f_{CLK} = 2.0$ MHz. At higher and lower clock frequencies accuracy may degrade. See curves in the Typical Performance Characteristics section.

Note 9: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*.)

Note 12: The ADC12441's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started (see the Typical Performance Characteristic curves).

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

Note 15: If the clock is asynchronous to the falling edge of $\overline{WR}$ an uncertainty of one clock period will exist in the interval of t_A, therefore making the minimum t_A = 6 clock periods and the maximum t_A = 7 clock periods. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods.

Note 16: The $\overline{CAL}$ line must be high before a conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: The ADC12441 reference ladder is composed solely of capacitors.

Note 19: A Military RETS Electrical Test Specification is available on request. At time of printing the ADC12441CMJ/883 RETS complies fully with the **boldface** limits in this column.

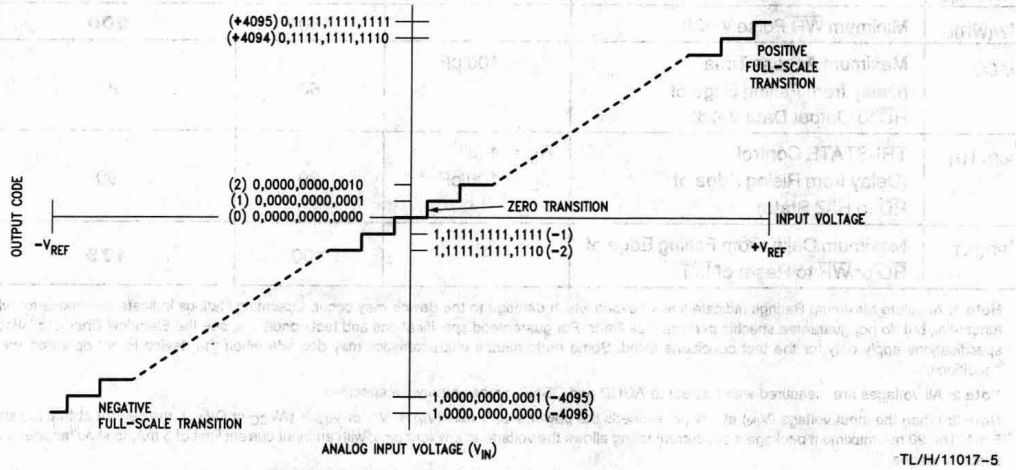

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FIGURE 1a. Transfer Characteristic

Electrical Characteristics (Continued)

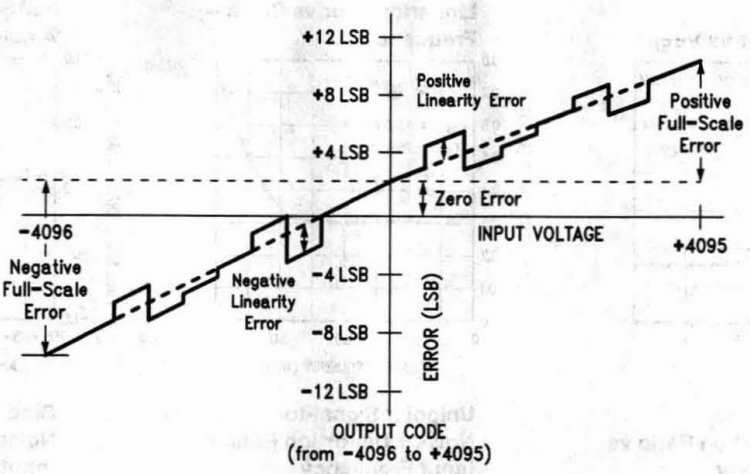

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Cal or Auto-Zero Cycles

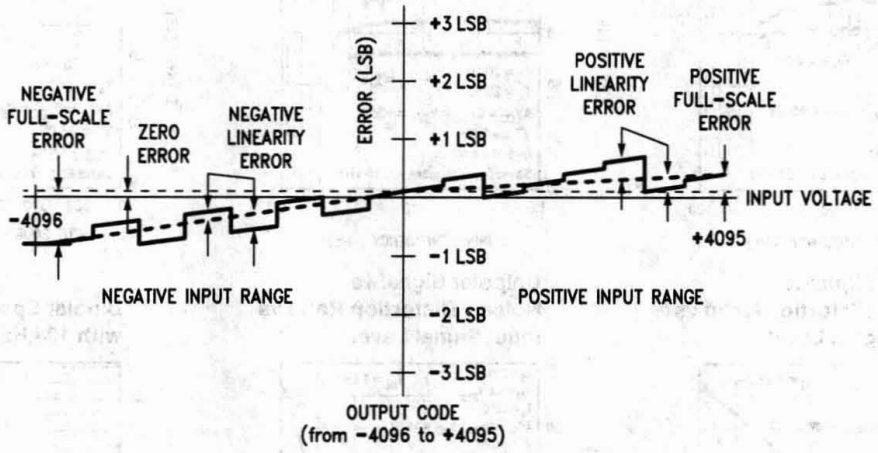

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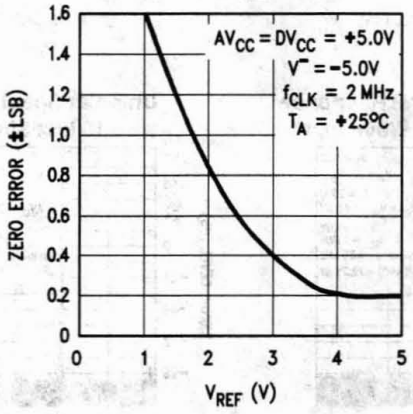
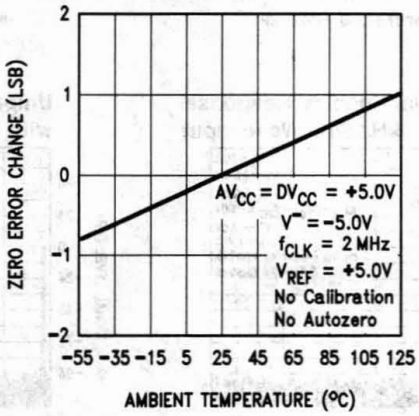
FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Cal Cycle

Typical Performance Characteristics

Zero Error vs V_{REF}



Zero Error Change vs Ambient Temperature



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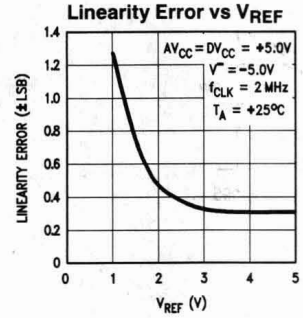
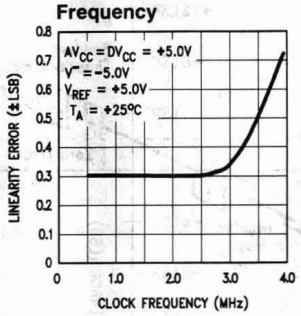
Typical Performance Characteristics (Continued)

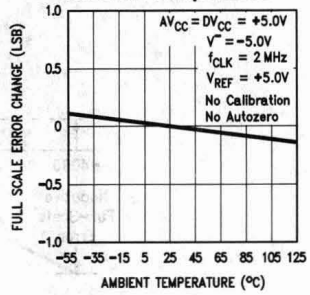
Linearity Error vs V_{REF}



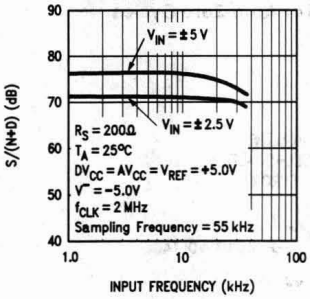
Linearity Error vs Clock Frequency



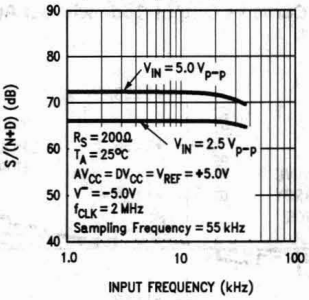
Full Scale Error Change vs Ambient Temperature



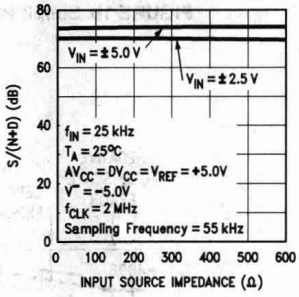
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



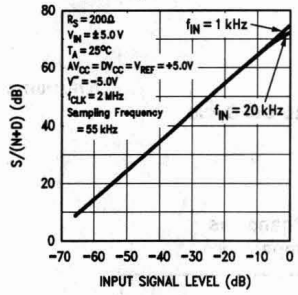
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



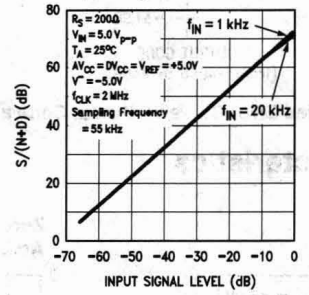
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance


VIN = ±5.0 V
VIN = ±2.5 V
fIN = 25 kHz
TA = 25°C
AVCC = DVCC = VREF = +5.0V
V⁻ = −5.0V
fCLK = 2 MHz
Sampling Frequency = 55 kHz
S/(N+D) (dB)
INPUT SOURCE IMPEDANCE (Ω)

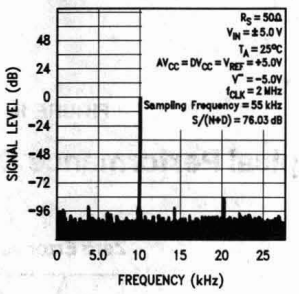
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



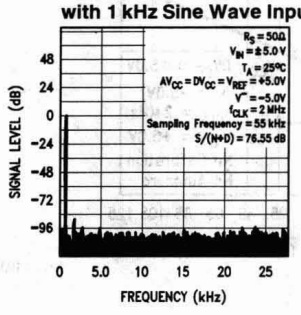
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



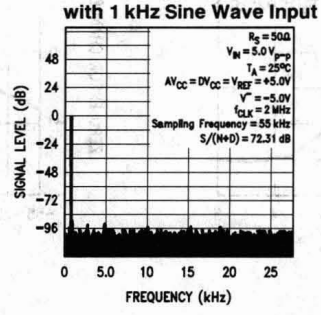
Bipolar Spectral Response with 10 kHz Sine Wave Input



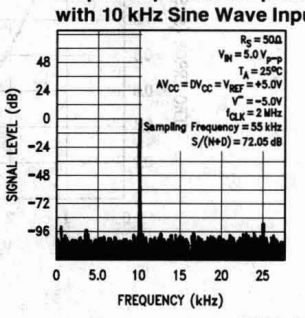
Bipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 1 kHz Sine Wave Input



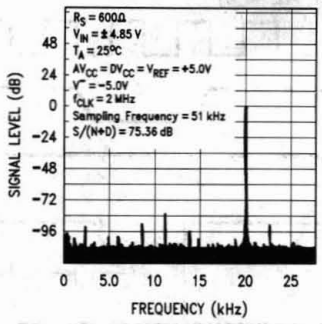
Unipolar Spectral Response with 10 kHz Sine Wave Input



TL/H/11017–9

Typical Performance Characteristics (Continued)

Bipolar Spectral Response with 20 kHz Sine Wave Input



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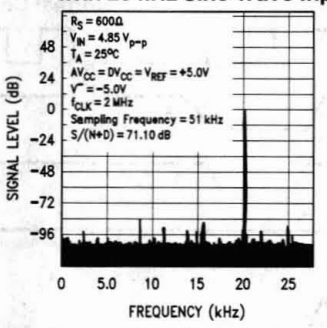
Unipolar Spectral Response with 20 kHz Sine Wave Input



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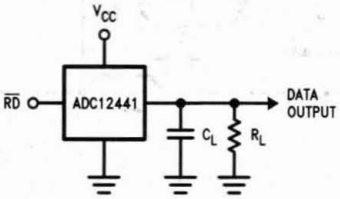
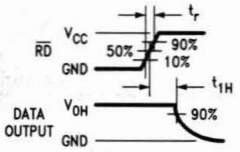
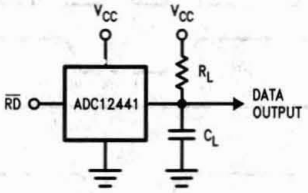
Test Circuits



TL/H/11017–12



TL/H/11017–13



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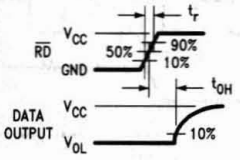
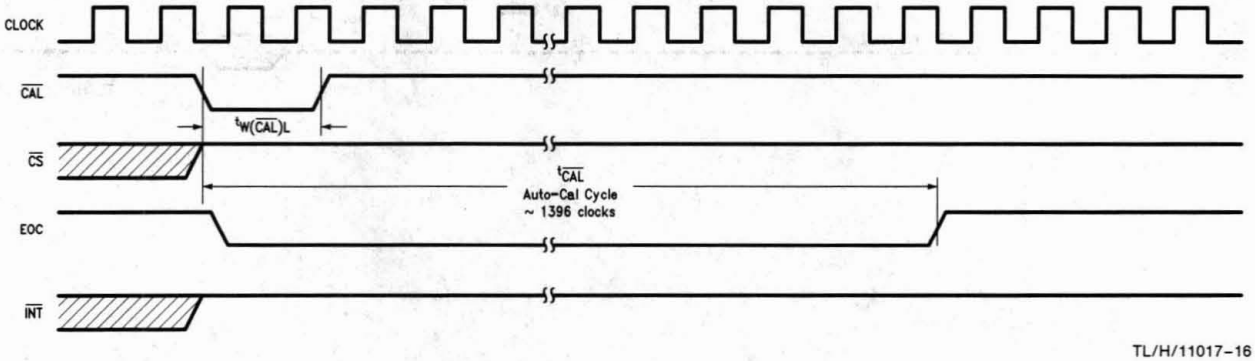


TL/H/11017–15

FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Auto-Cal Cycle ($\overline{CS}$ = 1, $\overline{WR}$ = X, $\overline{RD}$ = X, $\overline{AZ}$ = X, X = Don't Care)



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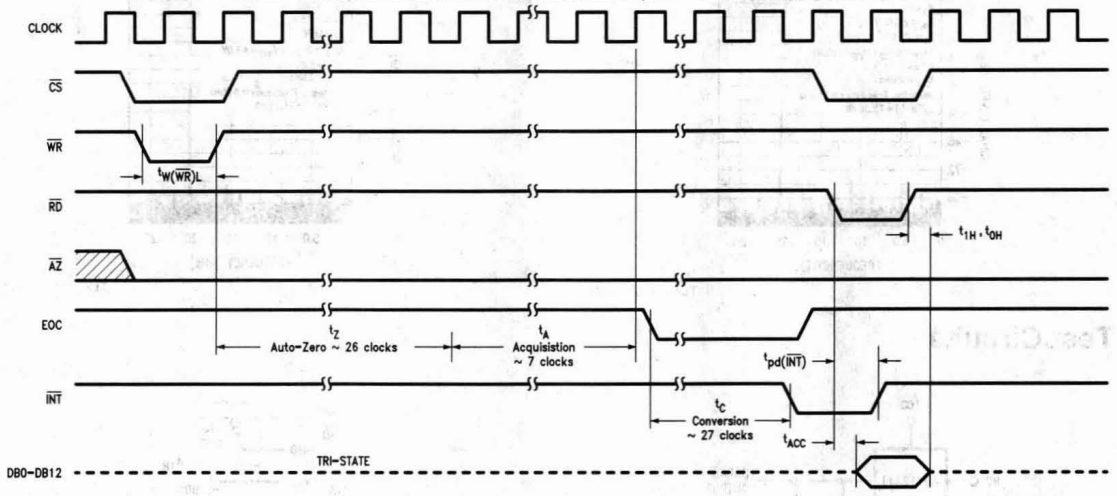
Timing Diagrams (Continued)

Normal Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



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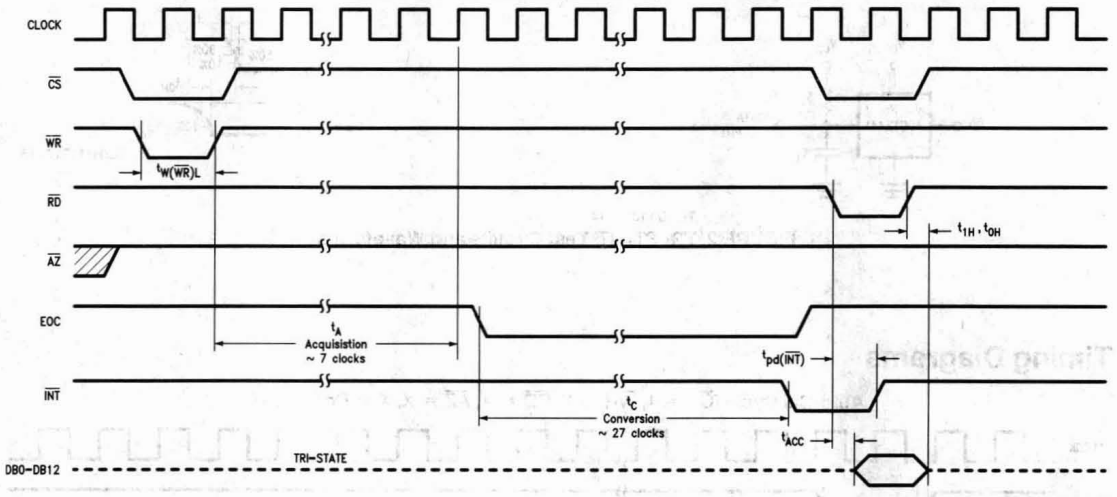
Normal Conversion without Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 1)



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1.0 Pin Descriptions

DV_{CC} (28), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC12441 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass filters (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs a bypass filter of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (14), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below 3.5 VDC.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$ and $\overline{RD}$ functions.

$\overline{RD}$ (11) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The converison is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low.

CLK (8) — The external clock input pin. The clock frequency range is 500 kHz to 4 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC12441 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC12441 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (12) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (13) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0–DB12 (15–27) — The TRI-STATE output pins. The output is in two's complement format with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC12441 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Cal routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC12441 without the need of trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC12441 at any time, which ensures its long term stability.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1396 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch error is found. Correction factors for these errors are then stored in internal RAM.

A conversion is initiated by taking $\overline{CS}$ and $\overline{WR}$ low. The $\overline{AZ}$ (Auto Zero) signal line should be tied high or low during the conversion process. If $\overline{AZ}$ is low an auto zero cycle, which takes approximately 26 clock periods, occurs before the actual conversion is started. The auto zero cycle determines the correction factors for the comparator's offset voltage. If $\overline{AZ}$ is high, the auto zero cycle is skipped. Next the analog input is sampled for 7 clock periods, and held in the capacitive DAC's ladder structure. The EOC then goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC12441. Next EOC goes high, and $\overline{INT}$ goes low to signal the end of the conversion. The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0–DB12 output buffers.

2.0 Functional Description (Continued)

Digital Control Inputs					A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊓	⊓	1	1	1	Start Conversion without Auto-Zero
⊓	1	⊓	1	1	Read Conversion Result without Auto-Zero
⊓	⊓	1	1	0	Start Conversion with Auto-Zero
⊓	1	⊓	1	0	Read Conversion Result with Auto-Zero
1	X	X	⊓	X	Start Calibration Cycle
0	X	1	0	X	Test Mode (DB2, DB3, DB5 and DB6 become active)

FIGURE 1. Function of the A/D Control Inputs

The table in *Figure 1* summarizes the effect of the digital control inputs on the function of the ADC12441. The Test Mode, where $\overline{RD}$ is high and $\overline{CS}$ and $\overline{CAL}$ are low, is used during manufacture to thoroughly check out the operation of the ADC12441. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

All internal logic can be reset, which will abort any conversion in process. The A/D is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore requiring an Auto-Cal cycle before the next conversion. This is true with or without Auto-Zero. The Calibration Cycle cannot be reset once started. On power-up the ADC12441 automatically goes through a Calibration Cycle that takes typically 1396 clock cycles. For reasons that will be discussed in Section 3.7, a new calibration cycle needs to be started after the completion of the automatic one.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 2a* is an example of a very stable reference that is appropriate for use with the ADC12441. The simple reference circuit of *Figure 2b* may be used when the application does not require low full scale errors.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for given input condition.

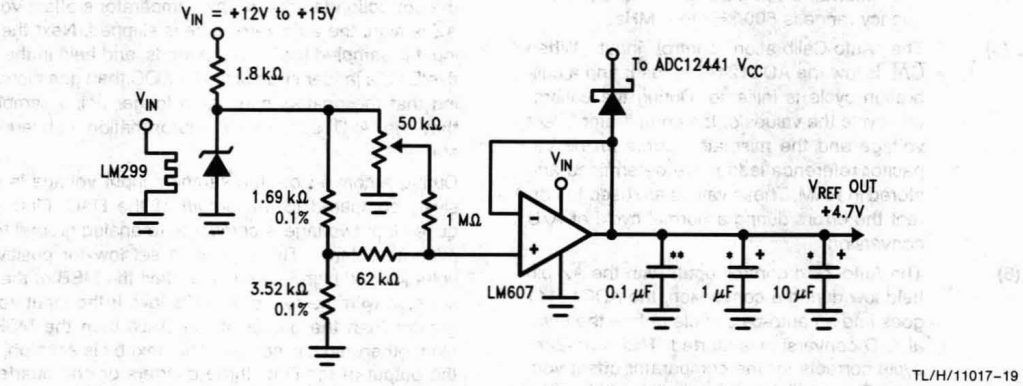

FIGURE 2a. Low Drift Extremely Stable Reference Circuit

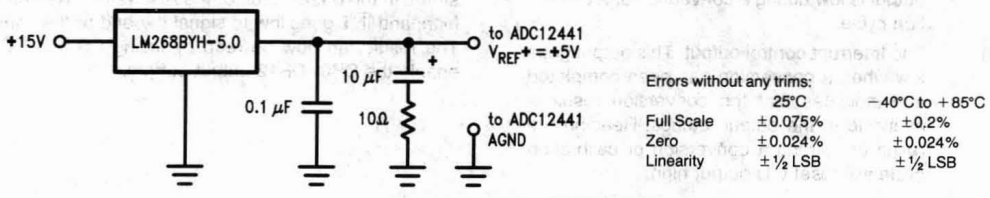

FIGURE 2b. Simple Reference Circuit

3.0 Analog Considerations (Continued)

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 INPUT CURRENT

Because the input network of the ADC12441 is made up of a switch and a network of capacitors, a charging current will flow into or out of (depending on the input voltage polarity) of the analog input pin (V_{IN}) on the start of the analog input sampling period (t_A). The peak value of this current will depend on the actual input voltage applied.

3.3 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.4 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.5 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 3*. External R_S will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With f_{CLK} = 2 MHz t_A = 7 clock periods = 3.5 μs, $R_S \leq 1$ kΩ will allow a 5V analog input voltage to settle properly.

3.6 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the auto-zero or auto-cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors whould be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.7 THE CALIBRATION CYCLE

On power up the ADC12441 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full scale, offset, and linearity errors down to the specified limits. Full scale error typically changes ±0.1 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up, if auto-zero is used to correct the zero error change.

3.8 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature changes significantly. (See the curved titled "Zero Error Change vs Ambient Temperature" in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than ±1 LSB. An auto-zero cycle will maintain the zero error to ±1 LSB or less.

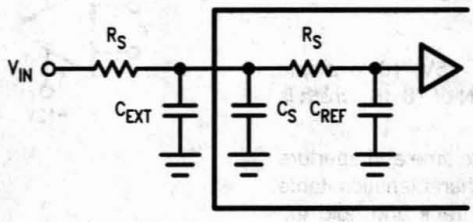

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FIGURE 3. Analog Input Equivalent Circuit

4.0 Dynamic Performance

Many applications require the A/D converter to digitize ac signals, but the standard dc integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with ac input signals. The important specifications for ac applications reflect the converter's ability to digitize ac signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise ratio (S/N), signal-to-noise + distortion ratio (S/(N+D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's ac performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N+D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in the table of Electrical Characteristics, and spectral plots of S/(N+D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N+D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N+D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.8)dB$$

where n is the A/D's resolution in bits.

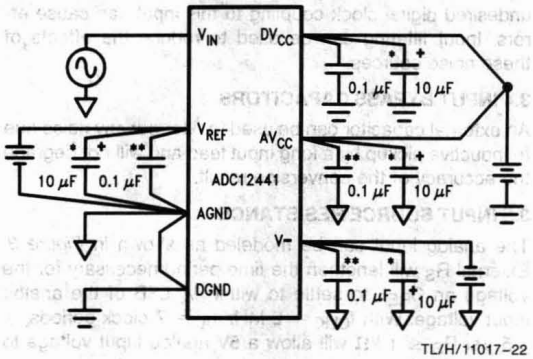
The effective bits of a real A/D converter, therefore, can be found by:

$$n(\text{effective}) = \frac{S/N(dB) - 1.8}{6.02}$$

As an example, an ADC12441 with a ±5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC12441 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC12441, the hold command is internally generated. When the Auto-Zero function is not being used, the hold command occurs at the end of the acquisition window, or seven clock periods after the rising edge of the $\overline{WR}$. The delay between the internally generated hold command and the time that the ADC12441 actually holds the input signal is the aperture time. For the ADC12441, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC12441 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

Power Supply Bypassing



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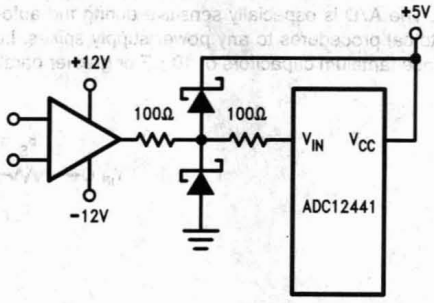
*Tantalum
**Ceramic

Protecting the Analog Inputs



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Note: External protection diodes should be able to withstand the op amp current limit.

National Semiconductor

ADC1251 Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample-and-Hold

General Description

The ADC1251 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter. On request, the ADC1251 goes through a self-calibration cycle that adjusts for any zero, full scale, or linearity errors. The ADC1251 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC1251 is tracked and held by the internal circuitry, so an external sample-and-hold is not required. The ADC1251 has an $\overline{S}/H$ control input which directly controls the track-and-hold state of the A/D. A unipolar analog input voltage range (0 to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit data result is available on the eight outputs of the ADC1251 in two bytes, high-byte first and sign extended. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Features

- Self-calibration provides excellent temperature stability
- Internal sample-and-hold
- 8-bit μP/DSP interface
- Bipolar input range with a single +5V reference
- No missing codes over temperature
- TTL/MOS input/output compatible

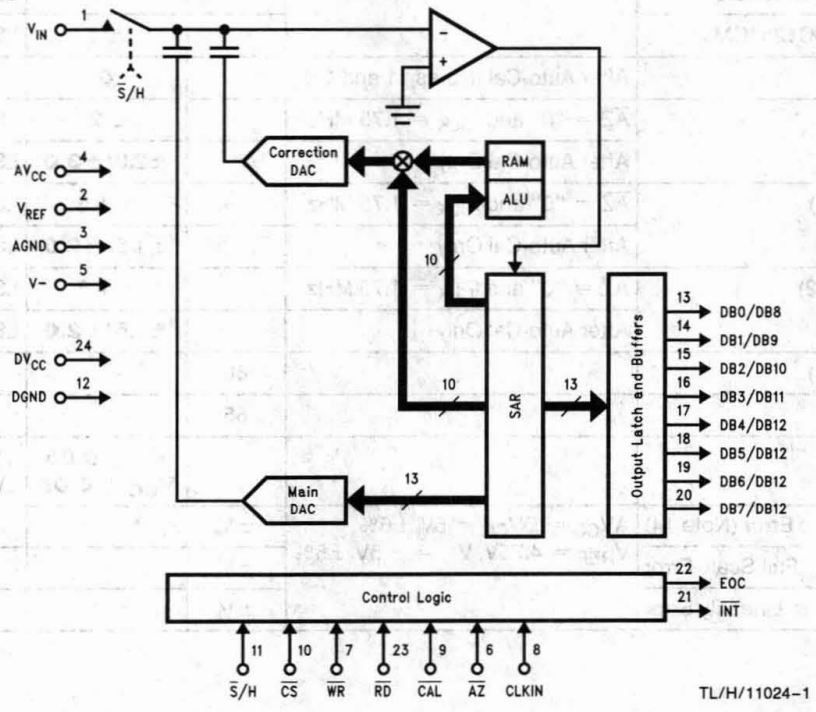
Key Specifications

■ Resolution	12 bits plus sign
■ Conversion Time	8 μs (max)
■ Sampling Rate	83 kHz (max)
■ Linearity Error	±0.6 LSB (±0.0146%) (max)
■ Zero Error	±1 LSB (max)
■ Full Scale Error	±1.5 LSB (max)
■ Power Consumption @ ±5V	113 mW (max)

Applications

- Digital signal processing
- High resolution process control
- Instrumentation

Simplified Block Diagram



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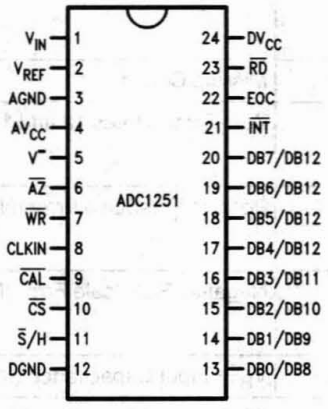
Connection Diagram

Dual-In-Line Package



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Top View

Ordering Information

Industrial ($-40°C \le T_A \le +85°C$)	Package
ADC1251BIJ, ADC1251CIJ	J24A
Military ($-55°C \le T_A \le +125°C$)	**Package**
ADC1251CMJ, ADC1251CMJ/883	J24A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Inputs (V_{REF}, V_{IN})	(V^- − 0.3V) to (V_{CC} + 0.3V)
AV_{CC}-DV_{CC} (Note 7)	0.3V
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information J Package (10 sec.)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC1251BIJ, ADC1251CIJ	−40°C ≤ T_A ≤ +85°C
ADC1251CMJ	−55°C ≤ T_A ≤ +125°C
ADC1251CMJ/883	−55°C ≤ T_A ≤ +125°C
DV_{CC} and AV_{CC} Voltage (Notes 6 & 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 & 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +5.0V, $\overline{AZ}$ = "1", f_{CLK} = 3.5 MHz and tested using $\overline{WR}$ control unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error	ADC1251BIJ	After Auto-Cal (Notes 11 & 12)		**±0.6**	LSB(max)
		ADC1251CIJ			**±1**	LSB(max)
		ADC1251CMJ			**±1**	LSB(max)
	Negative Integral Linearity Error	ADC1251BIJ	After Auto-Cal (Notes 11 and 12)		**±0.6**	LSB(max)
		ADC1251CIJ			**±1**	LSB(max)
		ADC1251CMJ			**±1**	LSB(max)
	Missing Codes		After Auto-Cal (Notes 11 and 12)		**0**	
	Zero Error (Notes 12 and 13)		$\overline{AZ}$ = "0" and f_{CLK} = 1.75 MHz		**±2**	LSB(max)
			After Auto-Cal Only		±2.0/**±3.0**	LSB(max)
	Positive Full-Scale Error (Note 12)		$\overline{AZ}$ = "0" and f_{CLK} = 1.75 MHz		**±1.5**	LSB(max)
			After Auto-Cal Only		±1.5/**±2.0**	LSB(max)
	Negative Full-Scale Error (Note 12)		$\overline{AZ}$ = "0" and f_{CLK} = 1.75 MHz		**±1.5**	LSB(max)
			After Auto-Cal Only		±1.5/**±2.0**	LSB(max)
C_{REF}	V_{REF} Input Capacitance (Note 18)			80		pF
C_{IN}	Analog Input Capacitance			65		pF
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB

Converter Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, $\overline{AZ}$ = "1" and $f_{CLK} = 3.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
DYNAMIC CHARACTERISTICS					
S/(N+D)	Unipolar Signal-to-Noise+Distortion Ratio (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	72		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 4.85\ V_{p-p}$	72		dB
S/(N+D)	Bipolar Signal-to-Noise+Distortion Ratio (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = \pm 4.85V$	76		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 4.85V$	76		dB
	−3 dB Unipolar Full Power Bandwidth	$V_{IN} = 4.85V$, (Note 17)	32		kHz
	−3 dB Bipolar Full Power Bandwidth	$V_{IN} = \pm 4.85V$, (Note 17)	25		kHz
t_{Ap}	Aperture Time		100		ns
	Aperture Jitter		100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 3.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	$V_{CC} = 5.25V$		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	$V_{CC} = 4.75V$		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1**	μA(max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**	μA(max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V(min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V(max)
V_H	CLK IN Hysteresis $[V_T^+(min) - V_T^-(max)]$		0.7	**0.4**	V(min)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		**2.4** **4.5**	V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 1.6$ mA		**0.4**	V(max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA(max)
		$V_{OUT} = 5V$	0.01	**3**	μA(max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA(min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA(min)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS}$ = "1"	1	**2.5**	mA(max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS}$ = "1"	4	**10**	mA(max)
I^-	V^- Supply Current	$\overline{CS}$ = "1"	2.8	**10**	mA(max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
f_{CLK}	Clock Frequency				MHz
			0.5		MHz(min)
			6.0	**3.5**	MHz(max)
	Clock Duty Cycle		50		%
				40	%(min)
				60	%(max)
t_C	Conversion Time Using $\overline{WR}$ to Start a Conversion		$27(1/f_{CLK})$	**$27(1/f_{CLK}) + 250$ ns**	(max)
		$f_{CLK} = 3.5$ MHz, $\overline{AZ}$ = "1"	7.7	**7.95**	μs(max)
		$f_{CLK} = 1.75$ MHz, $\overline{AZ}$ = "0"	15.4	**15.65**	μs(max)
t_C	Conversion Time Using $\overline{S}/H$ to Start a Conversion	$\overline{AZ}$ = "1"	$34(1/f_{CLK})$	**$34(1/f_{CLK}) + 250$ ns**	(max)
		$f_{CLK} = 3.5$ MHz, $\overline{AZ}$ = "1"	9.7	**9.95**	μs(max)
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$	3.5	**3.5**	μs(min)
t_{IA}	Internal Acquisition Time (When Using $\overline{WR}$ Control Only)		$7(1/f_{CLK})$	**$7(1/f_{CLK})$**	(max)
t_{ZA}	Auto Zero Time + Acquisition Time		$33(1/f_{CLK})$	**$33(1/f_{CLK}) + 250$ ns**	(max)
		$f_{CLK} = 1.75$ MHz	18.8	**19.05**	μs(max)
$t_{D(EOC)L}$	Delay from Hold Command to Falling Edge of EOC	Using $\overline{WR}$ Control	200	**350**	ns(max)
		Using $\overline{S}/H$ Control	100	**150**	ns(max)
$t_{\overline{CAL}}$	Calibration Time		$1399(1/f_{CLK})$	**$1399(1/f_{CLK})$**	(max)
		$f_{CLK} = 3.5$ MHz	399	**400**	μs(max)
$t_{W(\overline{CAL})L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns(min)
$t_{W(\overline{WR})L}$	Minimum $\overline{WR}$ Pulse Width		60	**200**	ns(min)
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	**95**	ns(max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	**70**	ns(max)
$t_{PD(\overline{INT})}$	Maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns(max)
t_{RR}	Delay between Successive $\overline{RD}$ Pulses		30	**60**	ns(min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

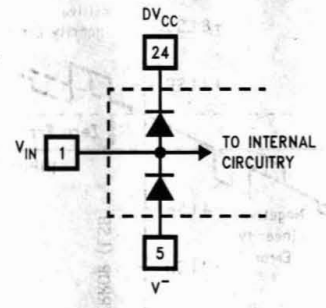
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > (AV_{CC}$ or $DV_{CC})$, the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The power dissipation of this device under normal operation should never exceed 191 mW (Quiescent Power Dissipation + 1 TTL Load on each digital output). Caution should be taken not to exceed absolute maximum power rating when the device is operating in severe fault condition (ex. when any inputs or outputs exceed the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150°C$, and the typical thermal resistance (θ_{JA}) of the ADC1251 with CMJ, BIJ, and CIJ suffixes when board mounted is 51°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Electrical Characteristics (Continued)

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV. This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (−4.75 V_{DC}), the analog input full-scale voltage must be ≤ ±4.8 V_{DC}.



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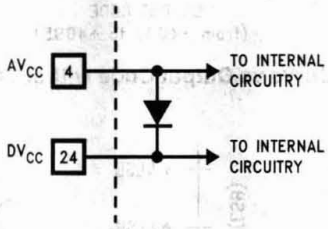
Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at f_{CLK} = 3.5 MHz. At higher or lower clock frequencies accuracy may degrade. See the Typical Performance Characteristics curves.

Note 9: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*).

Note 12: The ADC1251's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started. See the typical performance characteristic curves.

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

Note 15: When using the $\overline{WR}$ control to start a conversion if the clock is asynchronous to the rising edge of $\overline{WR}$ an uncertainty of one clock period will exist in the end of the interval t_A, therefore making t_A end a minimum 6 clock periods or a maximum 7 clock periods after the rising edge of $\overline{WR}$. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will end exactly 6.5 clock periods after the rising edge of $\overline{WR}$. This does not occur when $\overline{S}/H$ control is used.

Note 16: The $\overline{CAL}$ line must be high before a conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: The ADC1251 reference ladder is composed solely of capacitors.

Note 19: A Military RETS Electrical Test Specification is available on request. At time of printing the ADC1251CMJ/883 RETS specification complies fully with the **boldface** limits in this column.

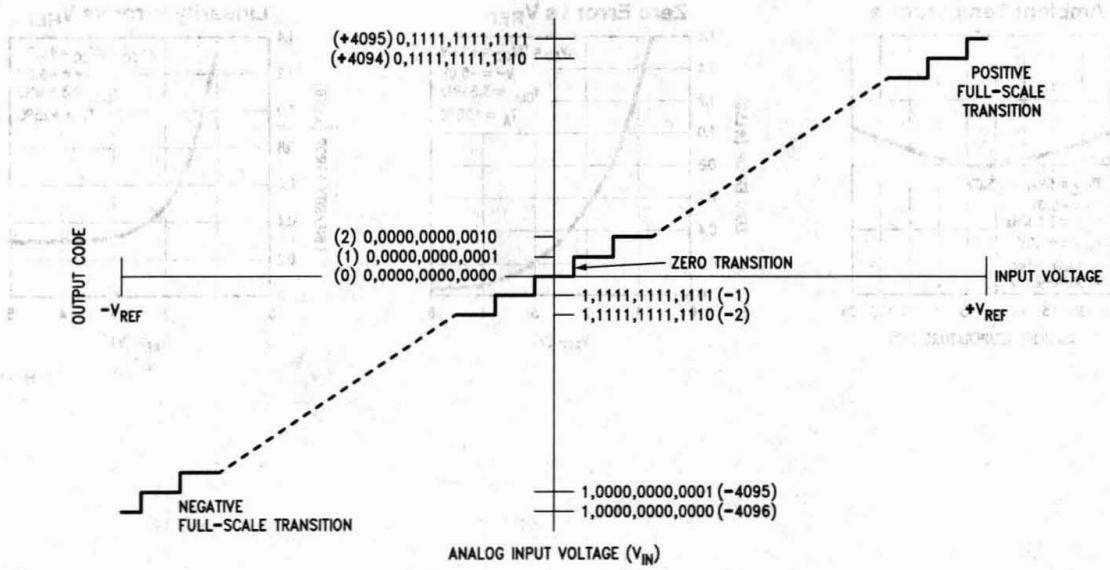

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FIGURE 1a. Transfer Characteristic

Electrical Characteristics (Continued)

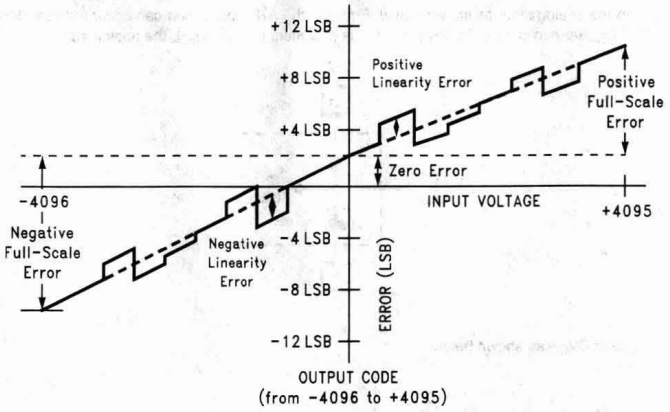

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Cal or Auto-Zero Cycles

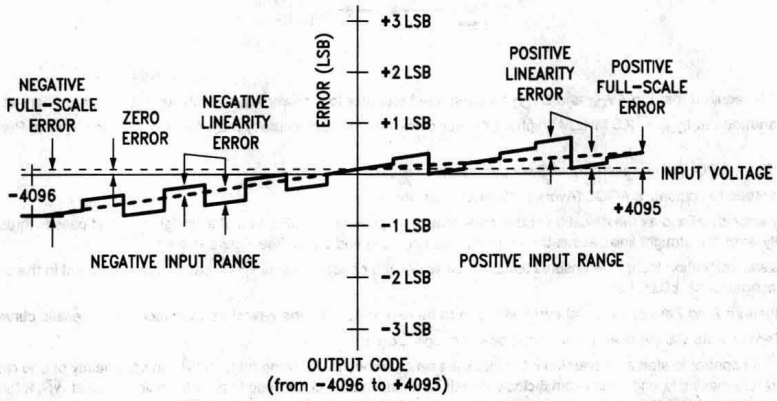

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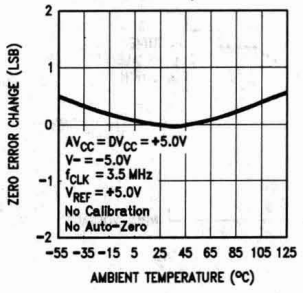
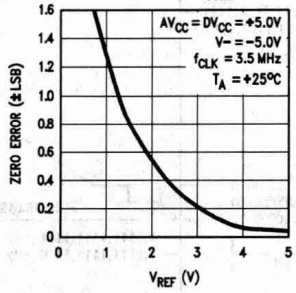
FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Cal Cycle

Typical Performance Characteristics

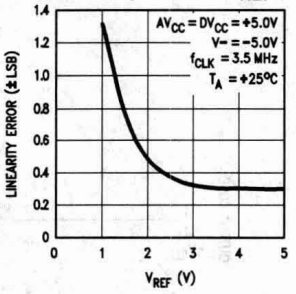
Zero Error Change vs Ambient Temperature



Zero Error vs V_{REF}



Linearity Error vs V_{REF}



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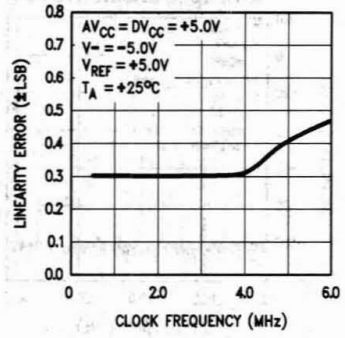
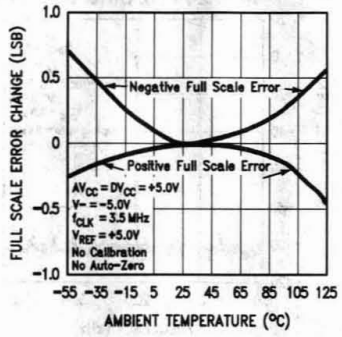
Typical Performance Characteristics (Continued)

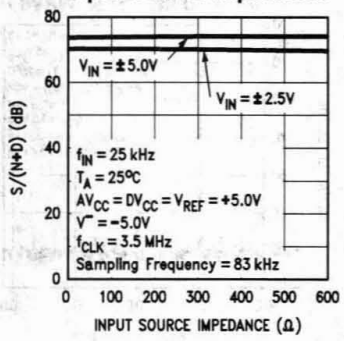
Linearity Error vs Clock Frequency



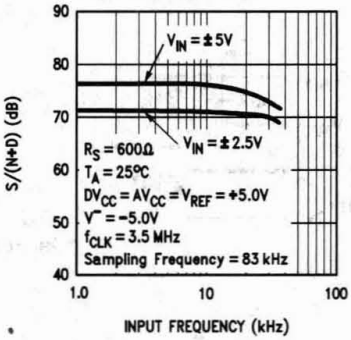
Full Scale Error Change vs Ambient Temperature



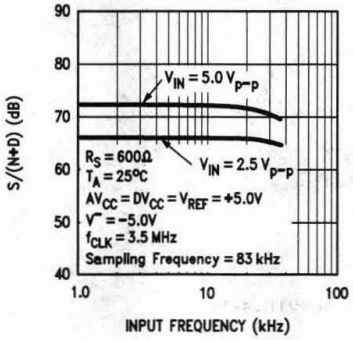
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance


$V_{IN} = \pm 5.0V$
$V_{IN} = \pm 2.5V$
$f_{IN} = 25$ kHz
$T_A = 25°C$
$AV_{CC} = DV_{CC} = V_{REF} = +5.0V$
$V^- = -5.0V$
$f_{CLK} = 3.5$ MHz
Sampling Frequency = 83 kHz
S/(N+D) (dB)
INPUT SOURCE IMPEDANCE (Ω)

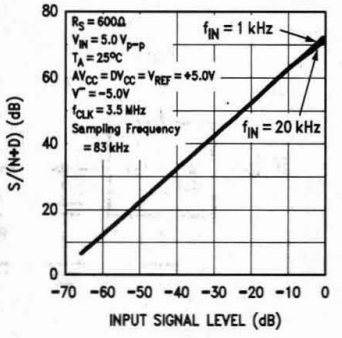
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



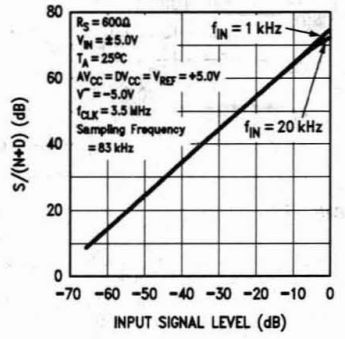
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



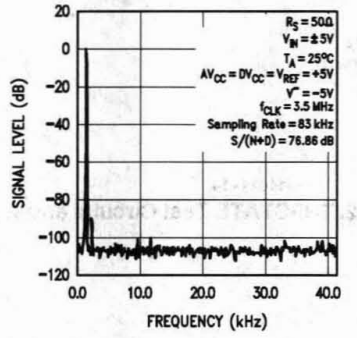
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



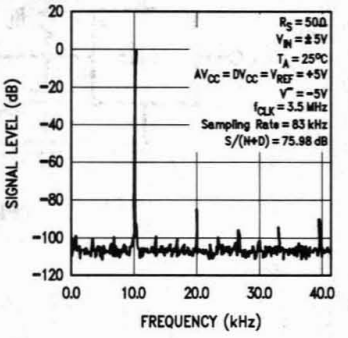
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



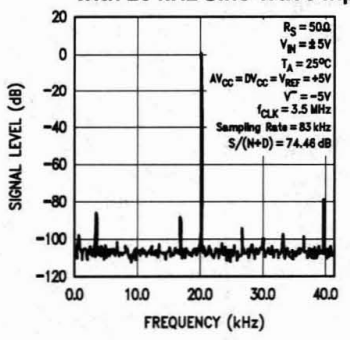
Bipolar Spectral Response with 1 kHz Sine Wave Input



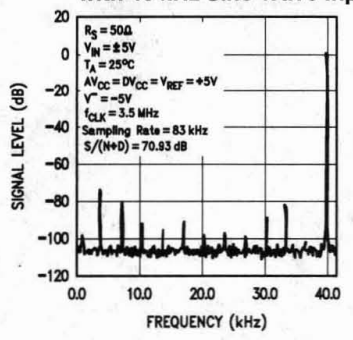
Bipolar Spectral Response with 10 kHz Sine Wave Input



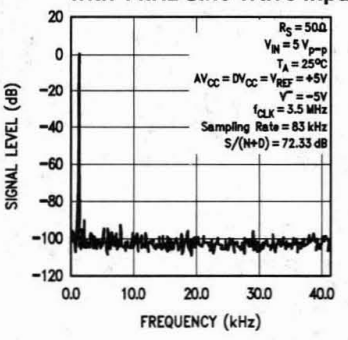
Bipolar Spectral Response with 20 kHz Sine Wave Input



Bipolar Spectral Response with 40 kHz Sine Wave Input



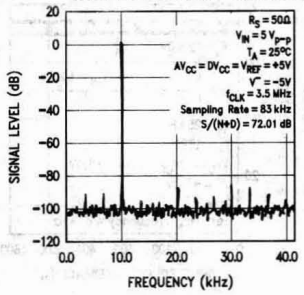
Unipolar Spectral Response with 1 kHz Sine Wave Input



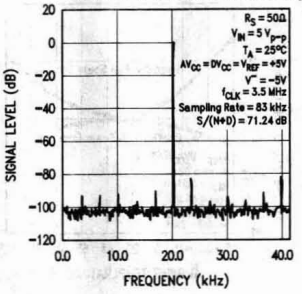
TL/H/11024–10

Typical Performance Characteristics (Continued)

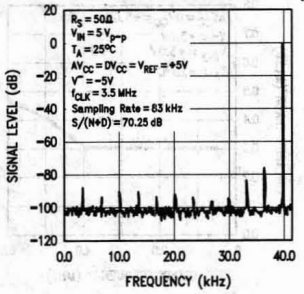
Unipolar Spectral Response with 10 kHz Sine Wave Input



Unipolar Spectral Response with 20 kHz Sine Wave Input

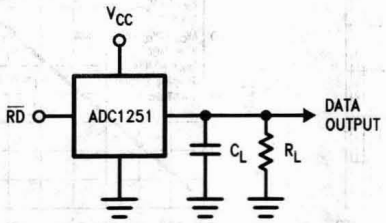


Unipolar Spectral Response with 40 kHz Sine Wave Input

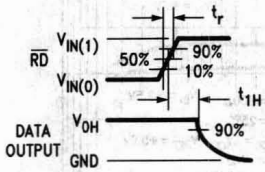


TL/H/11024–11

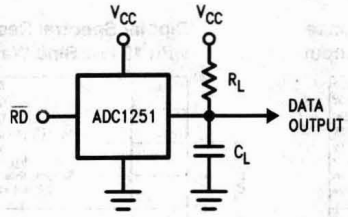
Test Circuits



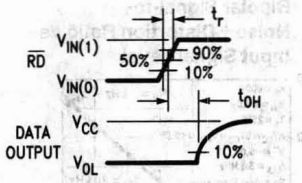
TL/H/11024–12



TL/H/11024–13



TL/H/11024–14

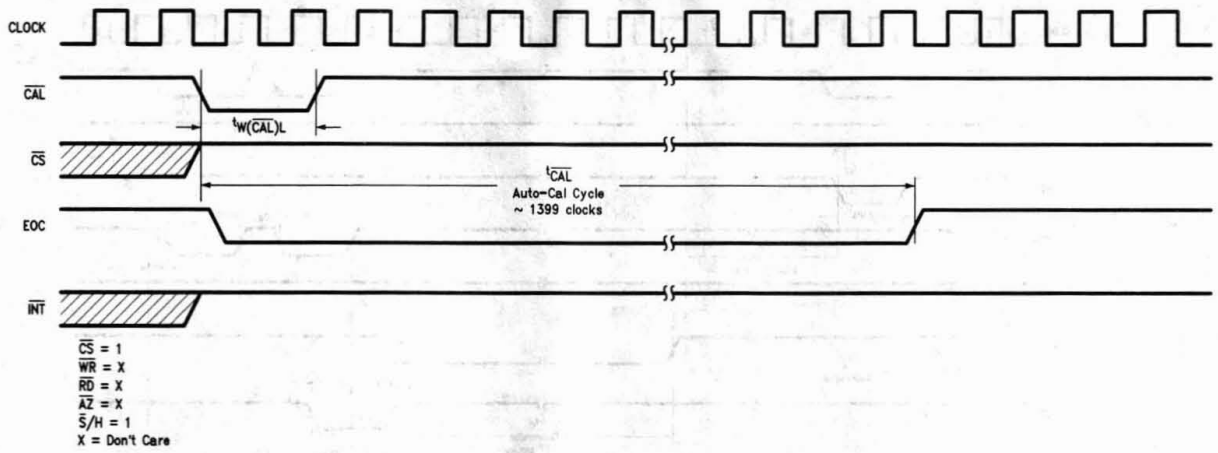


TL/H/11024–15

FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Auto-Cal Cycle



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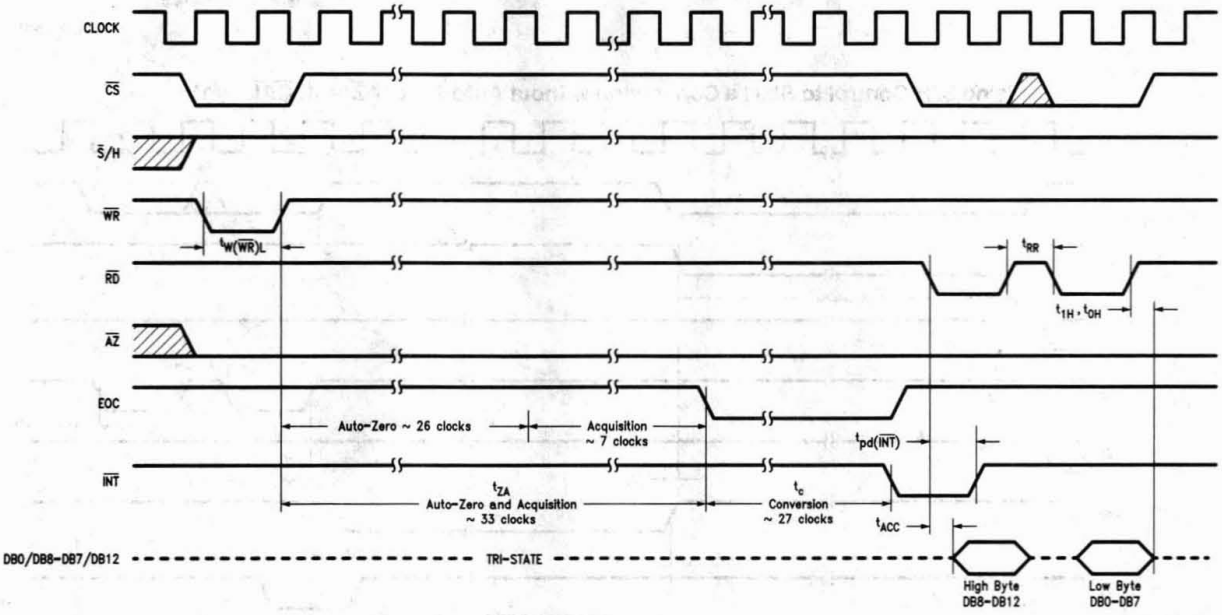
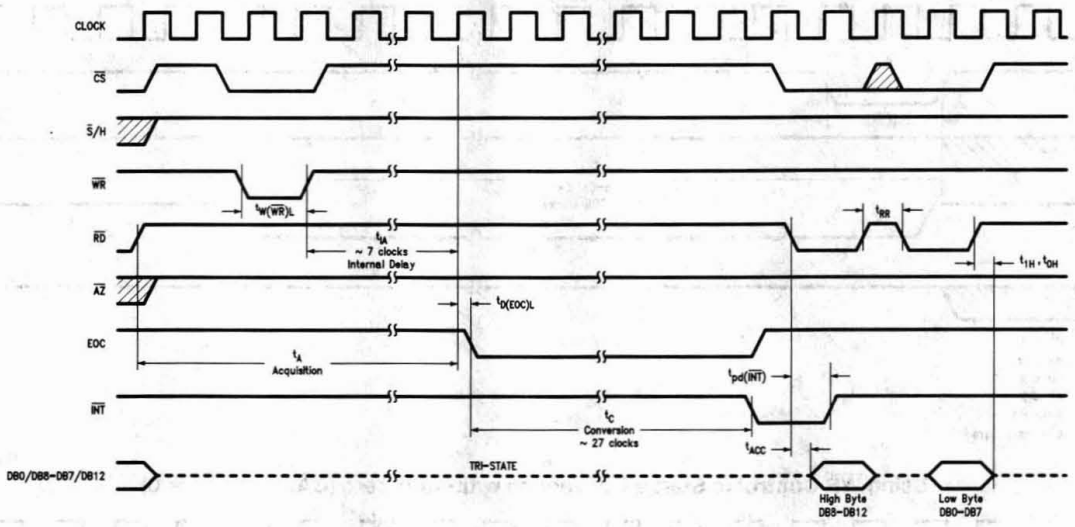
Using WR Control to Start a Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



TL/H/11024–17

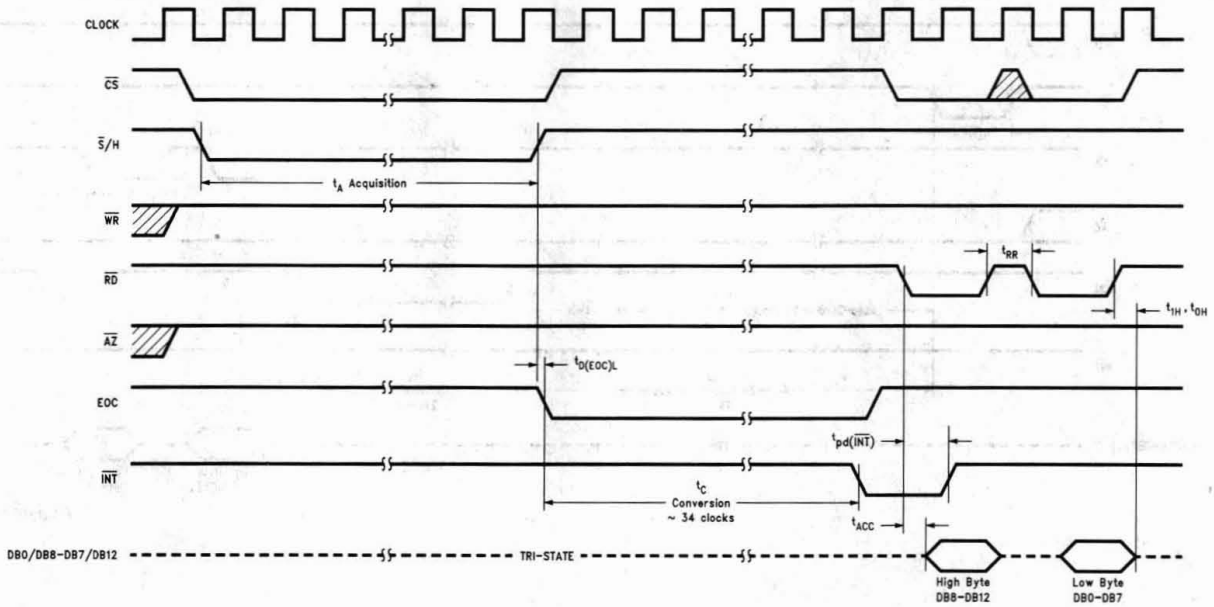
Timing Diagrams (Continued)

Using $\overline{WR}$ Control to Start a Conversion without Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 1)



TL/H/11024–18

Using $\overline{S}$/H Control to Start a Conversion without Auto-Zero ($\overline{AZ}$ = 1, $\overline{CAL}$ = 1)



TL/H/11024–19

1.0 Pin Descriptions

DV_{CC} (24), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC1251 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass capacitors (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs bypass capacitors of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (12), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below +3.5 V_{DC}.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$, $\overline{RD}$ and $\overline{S}/H$ functions.

$\overline{RD}$ (23) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The conversion is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low. When this control line is used the end of the analog input voltage acquisition window is internally controlled by the ADC1251.

$\overline{S}/H$ (11) — The sample and hold control input. This control input can also be used to start a conversion. With $\overline{CS}$ low the falling edge of $\overline{S}/H$ starts the analog input acquisition window. The rising edge of $\overline{S}/H$ ends the acquisition window and starts a conversion.

CLKIN (8) — The external clock input pin. The typical clock frequency range is 500 kHz to 6.0 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC1251 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC1251 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (22) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (21) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0/DB8–DB7/DB12 (13–20) — The TRI-STATE output pins. Twelve bit plus sign output data access is accomplished using two successive $\overline{RD}$s of one byte each, high byte first (DB8–DB12). The data format used is two's complement sign bit extended with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC1251 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Cal routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC1251 without the need for trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC1251 at any time, which ensures accuracy over temperature and time.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$ and $\overline{S}/H$ high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1399 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch errors are found. Correction factors for these errors are then stored in internal RAM.

A conversion can be initiated by taking $\overline{CS}$ and $\overline{WR}$ low. If $\overline{AZ}$ is low an Auto-Zero cycle, which takes approximately 26 clock periods, is inserted before the analog input is sampled and the actual conversion is started. $\overline{AZ}$ must remain low during the complete conversion sequence. After Auto-Zero the acquisition opens and the analog input is sampled for approximately 7 clock periods. If $\overline{AZ}$ is high, the Auto-Zero cycle is not inserted after the rising edge of $\overline{WR}$. In this case the acquisition window opens when the ADC1251 completes a conversion, signaled by the rising edge of EOC. At the end of the acquisition window EOC goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

2.0 Functional Description (Continued)

A conversion sequence can also be controlled by the $\overline{S}$/H and $\overline{CS}$ inputs. Taking $\overline{CS}$ and $\overline{S}$/H low starts the acquisition window for the analog input voltage. The rising edge of $\overline{S}$/H immediately puts the A/D in the hold mode and starts the conversion. Using $\overline{S}$/H will simplify synchronizing the end of the acquisition window to other signals, which may be necessary in a DSP environment.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC1251. Next $\overline{INT}$ goes low and EOC goes high to signal the end of the conversion.

The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0/DB8–DB7/DB12 output buffers. The high byte of data is relayed first on the data bus outputs as shown below:

DB0/ DB8	DB1/ DB9	DB2/ DB10	DB3/ DB11	DB4/ DB12	DB5/ DB12	DB6/ DB12	DB7/ DB12
Bit 8	Bit 9	Bit 10	MSB	Sign Bit	Sign Bit	Sign Bit	Sign Bit

Taking $\overline{CS}$ and $\overline{RD}$ low a second time will relay the low byte of data on the data bus outputs as shown below:

DB0/ DB8	DB1/ DB9	DB2/ DB10	DB3/ DB11	DB4/ DB12	DB5/ DB12	DB6/ DB12	DB7/ DB12
LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7

The table in *Figure 3* summarizes the effect of the digital control inputs on the function of the ADC1251. The Test Mode, where $\overline{RD}$ and $\overline{S}$/H are high and $\overline{CS}$ and $\overline{CAL}$ are low, is used during manufacture to thoroughly check out the operation of the ADC1251. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

The ADC1251 is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ or $\overline{S}$/H low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore requiring an Auto-Cal cycle before the next conversion. When using $\overline{WR}$ or $\overline{S}$/H without Auto-Zero ($\overline{AZ}$ = 1) to start a conversion, a new conversion can be restarted only after EOC has gone high, signaling the end of the current conversion. When using $\overline{WR}$ with Auto-Zero ($\overline{AZ}$ = 0) a new conversion can be restarted during the first 26 clock periods after the rising edge of $\overline{WR}$ (t_Z) or after EOC has returned high without corrupting the Auto-Cal correction factors.

The Calibration Cycle cannot be reset once started. On power-up the ADC1251 automatically goes through a Calibration Cycle that takes typically 1399 clock cycles. For reasons that will be discussed in Section 3.8, a new calibration cycle needs to be started after the completion of the automatic one.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 4* is an example of a very stable reference that is appropriate for use with the ADC1251.

Digital Control Inputs						A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{S}$/H	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊓	⊓	1	1	1	1	Start Conversion without Auto-Zero
⊓	1	⊓	1	1	1	Start Conversion synchronous with rising edge of $\overline{S}$/H without Auto-Zero
⊓	1	1	⊓	1	1	Read Conversion Result without Auto-Zero
⊓	⊓	1	1	1	0	Start Conversion with Auto-Zero
⊓	1	1	⊓	1	0	Read Conversion Result with Auto-Zero
1	X	1	X	⊓	X	Start Calibration Cycle
0	X	X	1	0	X	Test Mode (DB2, DB3, DB5, and DB6 become active)

FIGURE 3. Function of the A/D Control Inputs

3.0 Analog Considerations (Continued)

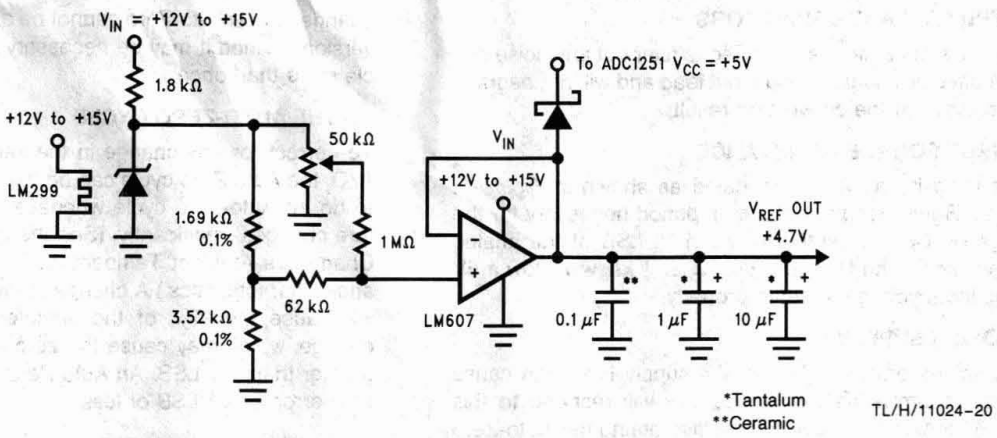


FIGURE 4. Low Drift Extremely Stable Reference Circuit

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 ACQUISITION WINDOW

As shown in the timing diagrams there are three different methods of starting a conversion, each of which affects the acquisition window and timing.

With Auto-Zero high a conversion can be started with the $\overline{WR}$ or $\overline{S}$/H controls. In either method of starting a conversion the rising edge of EOC signals the actual beginning of the acquisition window. At this time a voltage spike may be noticed on the analog input of the ADC1251 whose amplitude is dependent on the input voltage and the source resistance. The timing diagrams for these two methods of starting a conversion do not show the acquisition window starting at this time because the acquisition time (t_A) must start after the conversion result high and low bytes have been read. This is necessary since activating and deactivating the digital outputs (DB0/DB7–DB8/DB12) causes current fluctuations in the ADC1251's internal DV_{CC} lines. This generates digital noise which couples into the capacitive ladder that stores the analog input voltage. Therefore, the time interval between the rising edge of EOC and the second read is inappropriate for analog input voltage acquisition.

When $\overline{WR}$ is used to start a conversion with $\overline{AZ}$ low the Auto-Zero cycle is inserted before the acquisition window. In this method the acquisition window is internally controlled by the ADC1251 and lasts for approximately 7 clock periods. Since the acquisition window needs to be at least 3.5 μs at all times, when using Auto-Zero the maximum clock frequency is limited to 2 MHz. The zero error with the Auto-Zero cycle is production tested at a clock frequency of 1.75 MHz. This accommodates easy switching between a conversion with the Auto-Zero cycle (f_{CLK} = 1.75 MHz) and without (f_{CLK} = 3.5 MHz) as shown in *Figure 5*.

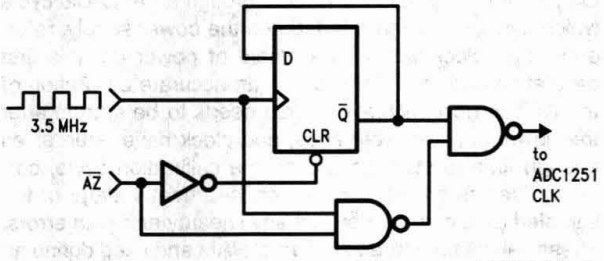


FIGURE 5. Switching between a Conversion with and without Auto-Zero when Using $\overline{WR}$ Control

3.3 INPUT CURRENT

Because the input network of the ADC1251 is made up of a switch and a network of capacitors a charging current will flow into or out of (depending on the input voltage polarity) the analog input pin (V_{IN}) on the start of the analog input sampling period. The peak value of this current will depend on the actual input voltage applied and the source resistance.

3.4 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.0 Analog Considerations (Continued)

3.5 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.6 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 6*. External R_S will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With $t_A = 3.5\ \mu s$, $R_S \leq 1\ k\Omega$ will allow a 5V analog input voltage to settle properly.

3.7 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the Auto-Zero or -Cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors should be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.8 THE CALIBRATION CYCLE

On power up the ADC1251 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full scale, offset, and linearity errors down to the specified limits. Full scale error typically changes ±0.2 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if Auto-Zero is used to correct the zero error change. Since Auto-Zero cannot be activated with $\overline{S}/H$ conversion method it may be necessary to do a calibration cycle more than once.

3.9 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the Auto-Zero cycle can be used. It may be necessary to do an Auto-Zero cycle whenever the ambient temperature changes significantly. (See the curve titled "Zero Error Change vs Ambient Temperature" in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than ±1 LSB. An Auto-Zero cycle will maintain the zero error to ±1 LSB or less.

4.0 Dynamic Performance

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise+distortion ratio (S/(N+D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N+D) is calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/(N+D) are shown in the table of Electrical Characteristics, and spectral plots are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N+D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N+D) drops 3 dB).

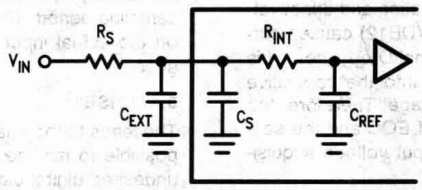


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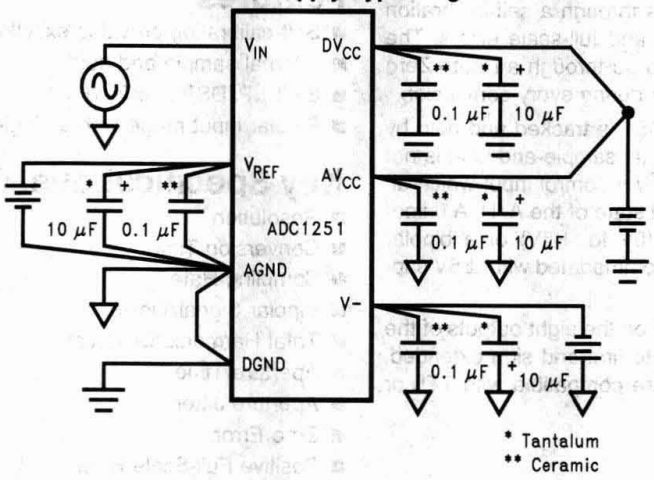
FIGURE 6. Analog Input Equivalent Circuit

4.0 Dynamic Performance (Continued)

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC1251 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC1251 when using the $\overline{S}$/H control to start a conversion, the hold command is generated by the rising edge of $\overline{S}$/H. The delay between the rising edge of $\overline{S}$/H and the time that the ADC1251 actually holds the input signal is the aperture time. For the ADC1251, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC1251 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

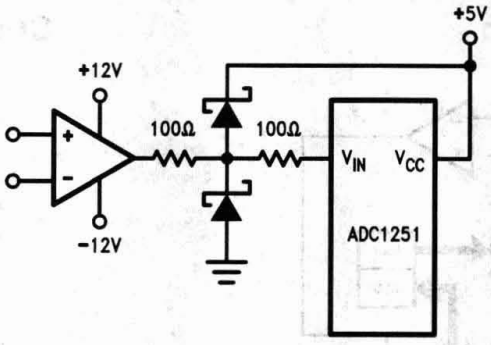
5.0 Typical Applications

Power Supply Bypassing



TL/H/11024–23

Protecting the Analog Inputs



TL/H/11024–24

Note: External protection diodes should be able to withstand the op amp current limit.

National Semiconductor

ADC12451 Dynamically-Tested Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample-and-Hold

General Description

The ADC12451 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter whose dynamic specifications (S/N, THD, etc.) are tested and guaranteed. On request, the ADC12451 goes through a self-calibration cycle that adjusts linearity, zero and full-scale errors. The ADC12451 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC12451 is tracked and held by the internal circuitry, so an external sample-and-hold is not required. The ADC12451 has a $\overline{S}$/H control input which directly controls the track-and-hold state of the A/D. A unipolar analog input voltage range (0V to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit data result is available on the eight outputs of the ADC12451 in two bytes, high-byte first and sign extended. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Applications

- Digital Signal Processing
- Audio
- Telecommunications
- High Resolution Process Control
- Instrumentation

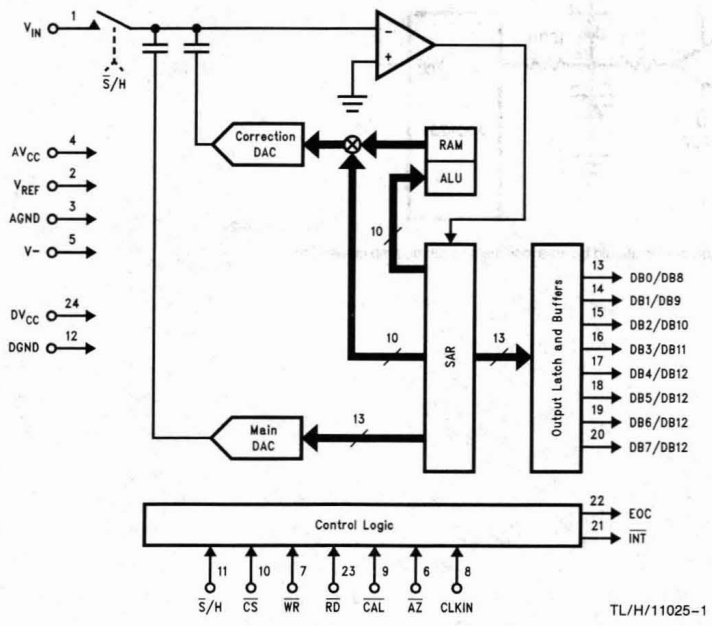
Features

- Self-calibration provides excellent temperature stability
- Internal sample-and-hold
- 8-bit μP/DSP interface
- Bipolar input range with a single +5V reference

Key Specifications

■ Resolution	12 bits plus sign
■ Conversion Time	7.7 μs (max)
■ Sampling Rate	83 kHz (max)
■ Bipolar Signal/Noise	73.5 dB (min)
■ Total Harmonic Distortion	−78.0 dB (max)
■ Aperture Time	100 ns
■ Aperture Jitter	100 ps_{rms}
■ Zero Error	±2 LSB (max)
■ Positive Full-Scale Error	±1.5 LSB (max)
■ Power Consumption @ ±5V	113 mW (max)

Simplified Block Diagram



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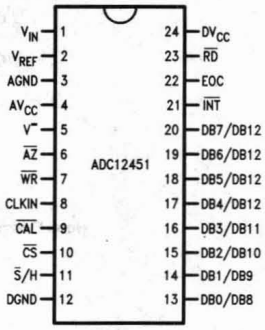
Connection Diagram

Dual-In-Line Package



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Top View

Ordering Information

Industrial ($-40°C \le T_A \le 85°C$)	Package
ADC12451CIJ	J24A
Military ($-55°C \le T_A \le 125°C$)	**Package**
ADC12451CMJ, ADC12451CMJ/883	J24A

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Inputs (V_{IN}, V_{REF})	(V^- −0.3V) to (V_{CC} + 0.3V)
AV_{CC}-DV_{CC} (Note 7)	0.3V
Input Current at any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information J Package (10 Seconds)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12451CIJ	−40°C ≤ T_A ≤ +85°C
ADC12451CMJ, ADC12451CMJ/883	−55°C ≤ T_A ≤ +125°C
DV_{CC} and AV_{CC} Voltage (Notes 6 & 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 & 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +5.0V, using $\overline{S}$/H input for conversion control, and f_{CLK} = 3.5 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Note 10, 19)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error		After Auto-Cal, (Notes 11 & 12)	±½		LSB
	Negative Integral Linearity Error		After Auto-Cal, (Notes 11 & 12)	±½		LSB
	Positive or Negative Differential Linearity		After Auto-Cal (Notes 11 & 12)	12		Bits
	Zero Error (Notes 12 & 13)		$\overline{AZ}$ = "0", f_{CLK} = 1.75 MHz	±1		LSB
			After Auto-Cal Only		±2/ **±3.0**	LSB(max)
	Positive Full-Scale Error (Note 12)		$\overline{AZ}$ = "0", f_{CLK} = 1.75 MHz	±1		LSB
			Auto-Cal Only		±1.5/ **±2.5**	LSB(max)
	Negative Full-Scale Error (Note 12)		$\overline{AZ}$ = "0", f_{CLK} = 1.75 MHz	±1		LSB
			Auto-Cal Only		±1.5/ **±3.0**	LSB(max)
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB
C_{REF}	V_{REF} Input Capacitance			80		pF
C_{IN}	Analog Input Capacitance			65		pF
DYNAMIC CHARACTERISTICS						
	Bipolar Effective Bits (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85V	12.6		Bits
			f_{IN} = 20.67 kHz, V_{IN} = ±4.85V	12.6	**11.9**	Bits(min)
	Unipolar Effective Bits (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	11.8		Bits
			f_{IN} = 20.67 kHz, V_{IN} = 4.85 V_{p-p}	11.8	**11.1**	Bits(min)
S/N	Bipolar Signal to Noise Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85V	78		dB
			f_{IN} = 10 kHz, V_{IN} = ±4.85V	78		dB
			f_{IN} = 20.67 kHz, V_{IN} = ±4.85V	78	**73.5**	dB(min)

Converter Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, using $\overline{S}/H$ input for conversion control, and $f_{CLK} = 3.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Note 10, 19)	Units (Limit)
DYNAMIC CHARACTERISTICS (Continued)					
S/N	Unipolar Signal to Noise Ratio (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	73		dB
		$f_{IN} = 10$ kHz, $V_{IN} = 4.85\ V_{p-p}$	73		dB
		$f_{IN} = 20.67$ kHz, $V_{IN} = 4.85\ V_{p-p}$	73	**68.7**	dB(min)
THD	Bipolar Total Harmonic Distortion (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = \pm 4.85V$	−82		dB
		$f_{IN} = 20.67$ kHz, $V_{IN} = \pm 4.85V$	−80	**−78.0**	dB(max)
THD	Unipolar Total Harmonic Distortion (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−82		dB
		$f_{IN} = 20.67$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−80	**−73.1**	dB(max)
	Bipolar Peak Harmonic or Spurious Noise (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = \pm 4.85V$	−88		dB
		$f_{IN} = 10$ kHz, $V_{IN} = \pm 4.85V$	−84		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 4.85V$	−80		dB
	Unipolar Peak Harmonic or Spurious Noise (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−90		dB
		$f_{IN} = 10$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−86		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−82		dB
	Bipolar Two Tone Intermodulation Distortion (Note 17)	$V_{IN} = \pm 4.85V$, $f_{IN1} = 19.375$ kHz, $f_{IN2} = 20$ kHz	−78		dB(max)
	Unipolar Two Tone Intermodulation Distortion (Note 17)	$V_{IN} = 4.85\ V_{p-p}$, $f_{IN1} = 19.375$ kHz, $f_{IN2} = 20$ kHz	−78		dB(max)
	−3 dB Bipolar Full Power Bandwidth	$V_{IN} = \pm 4.85V$, (Note 17)	25	**20.67**	kHz(min)
	−3 dB Unipolar Full Power Bandwidth	$V_{IN} = 4.85\ V_{p-p}$, (Note 17)	32	**20.67**	kHz(min)
	Aperture Time		100		ns
	Aperture Jitter		100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 3.5$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Condition	Typical (Note 9)	Limit (Note 10, 19)	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	$V_{CC} = 5.25V$		**2.0**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	$V_{CC} = 4.75V$		**0.8**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1**	μA(max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**	μA(max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V(min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V(max)
V_H	CLK IN Hysteresis $[V_T^+(min) - V_T^-(max)]$		0.7	**0.4**	V(min)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**	 V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 1.6$ mA		**0.4**	V(max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA(max)
		$V_{OUT} = 5V$	0.01	**3**	μA(max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA(min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA(min)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS}$ = "1"	1	**2.5**	mA(max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS}$ = "1"	2.8	**10**	mA(max)
I^-	V^- Supply Current	$\overline{CS}$ = "1"	2.8	**10**	mA(max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Note 10, 19)	Units (Limit)
f_{CLK}	Clock Frequency		 0.5 6.0	 **3.5**	MHz MHz(min) MHz(max)
	Clock Duty Cycle		50	 **40** **60**	% %(min) %(max)
t_C	Conversion Time using $\overline{WR}$ to start a Conversion		$27(1/f_{CLK})$	$\mathbf{27(1/f_{CLK}) + 250\ ns}$	(max)
		$f_{CLK} = 3.5$ MHz, $\overline{AZ}$ = "1"	7.7	**7.95**	μs(max)
		$f_{CLK} = 1.75$ MHz, $\overline{AZ}$ = "0"	15.4	**15.65**	μs(max)
t_C	Conversion Time using $\overline{S}/H$ to start a Conversion	$\overline{AZ}$ = "1"	$34(1/f_{CLK})$	$\mathbf{34(1/f_{CLK}) + 250\ ns}$	(max)
		$f_{CLK} = 3.5$ MHz, $\overline{AZ}$ = "1"	9.7	**9.95**	μs(max)

AC Electrical Characteristics (Continued)

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Note 10, 19)	Units (Limit)
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$	3.5	**3.5**	μs(min)
t_{IA}	Internal Acquisition Time (when using $\overline{WR}$ Control Only)		$7(1/f_{CLK})$	**$7(1/f_{CLK})$**	(max)
t_{ZA}	Auto Zero Time + Acquisition Time		$33(1/f_{CLK})$	**$33(1/f_{CLK}) + 250$ ns**	(max)
		$f_{CLK} = 1.75$ MHz	18.8	**19.05**	μs(max)
$t_{D(EOC)L}$	Delay from Hold Command to Falling Edge of EOC	Using $\overline{WR}$ Control	200	**350**	ns(max)
		Using $\overline{S}/\overline{H}$ Control	100	**150**	ns(max)
$t_{\overline{CAL}}$	Calibration Time		1399 $(1/f_{CLK})$	**1399 $(1/f_{CLK})$**	(max)
		$f_{CLK} = 3.5$ MHz	399	**400**	μs(max)
$t_{W(\overline{CAL})L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns(min)
$t_{W(\overline{WR})L}$	minimum $\overline{WR}$ Pulse Width		60	**200**	ns(min)
t_{ACC}	maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	**95**	ns(max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	**70**	ns(max)
$t_{PD(\overline{INT})}$	maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns(max)
t_{RR}	Delay between Successive $\overline{RD}$ Pulses		30	**60**	ns(min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

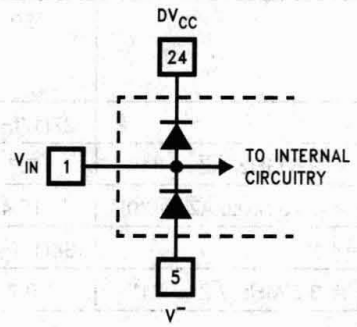
Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > (AV_{CC}$ or $DV_{CC})$, the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The power dissipation of this device under normal operation should never exceed 191 mW (Quiescent Power Dissipation + 1 TTL Load on each digital output). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (ex. when any inputs or outputs exceed the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{DMax} = (T_{JMax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMax} = 150°C$, and the typical thermal resistance (θ_{JA}) of the ADC12451 with CMJ, and CIJ suffixes when board mounted is 51°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV. This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (−4.75 V_{DC}), the analog input full-scale voltage must be ≤ ±4.8 V_{DC}.



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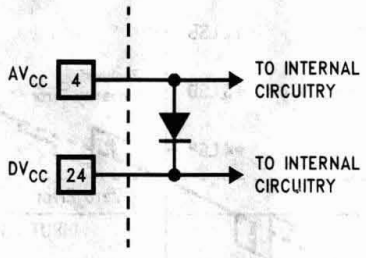
Electrical Characteristics (Continued)

Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at $f_{CLK} = 3.5$ MHz. At higher or lower clock frequencies accuracy may degrade, see the typical performance characteristic curves.

Note 9: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*).

Note 12: The ADC12451's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started, see the typical performance characteristic curves.

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

Note 15: When using the $\overline{WR}$ control to start a conversion if the clock is asynchronous to the rising edge of $\overline{WR}$ an uncertainty of one clock period will exist in the end of the interval of t_A, therefore making t_A end a minimum 6 clock periods or a maximum 7 clock periods after the rising edge of $\overline{WR}$. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will end exactly 6.5 clock periods after the rising edge of $\overline{WR}$. This does not occur when $\overline{S}/H$ control is used.

Note 16: The $\overline{CAL}$ line must be high before a conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: The ADC12451 reference ladder is composed solely of capacitors.

Note 19: A military RETS electrical test specification is available on request. At time of printing, the ADC12451CMJ/883 RETS specification complies fully with the **boldface** limits in this column.

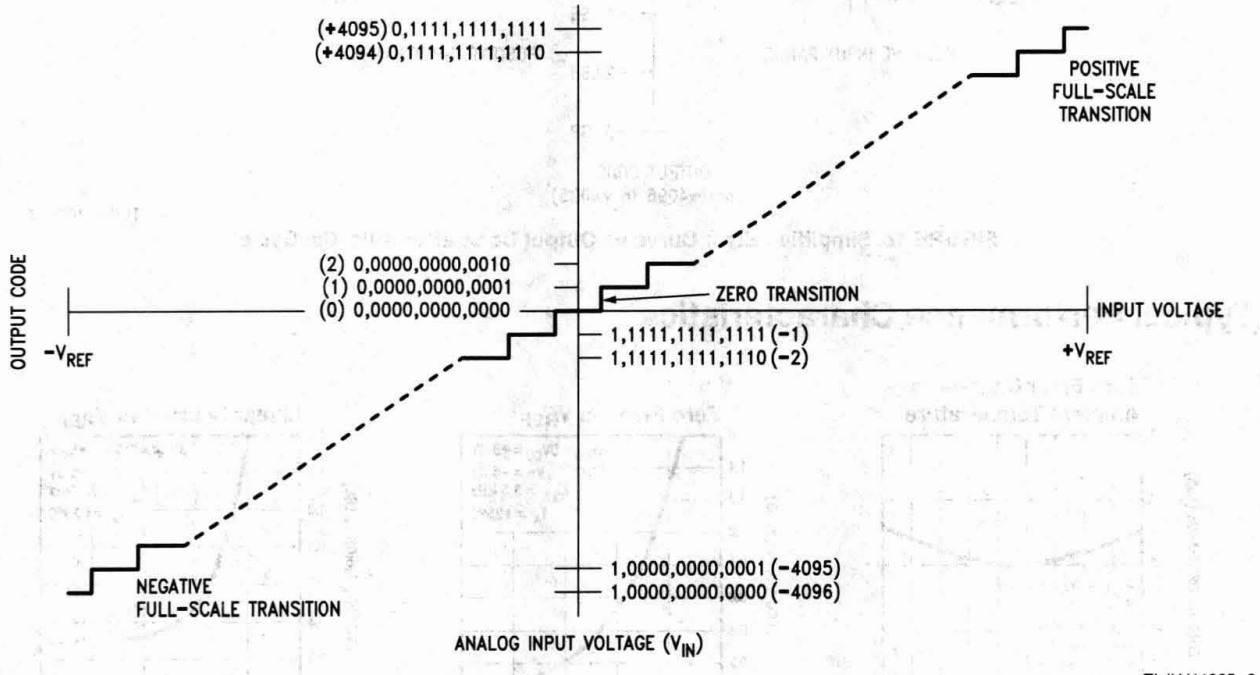

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FIGURE 1a. Transfer Characteristic

Electrical Characteristics (Continued)

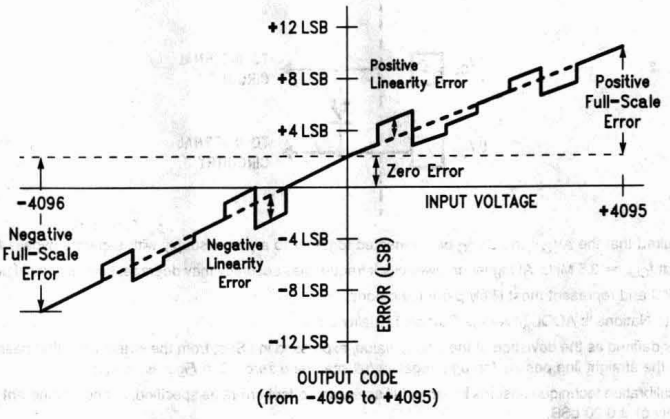

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Cal or Auto-Zero Cycles

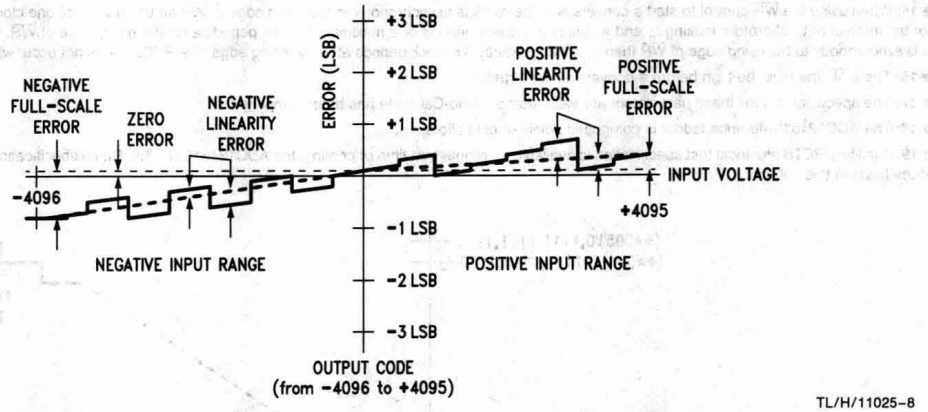

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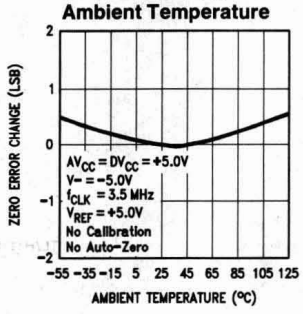
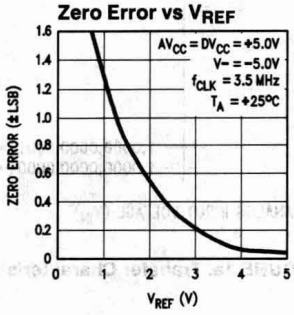
FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Cal Cycle

Typical Performance Characteristics

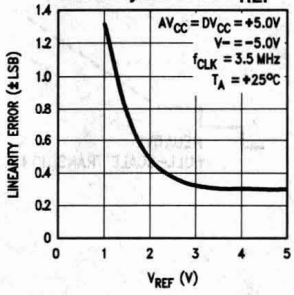
Zero Error Change vs Ambient Temperature



Zero Error vs V_{REF}



Linearity Error vs V_{REF}



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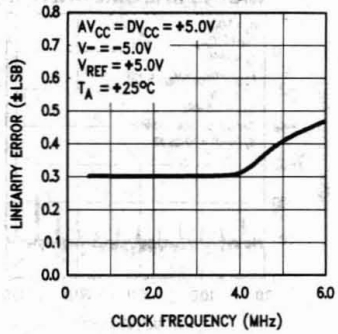
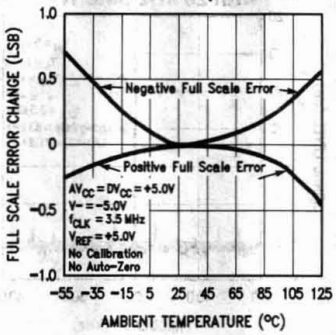
Typical Performance Characteristics (Continued)

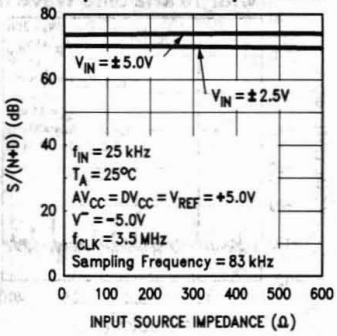
Linearity Error vs Clock Frequency



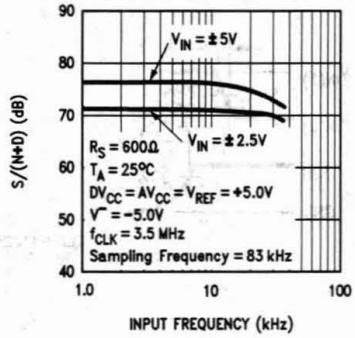
Full Scale Error Change vs Ambient Temperature



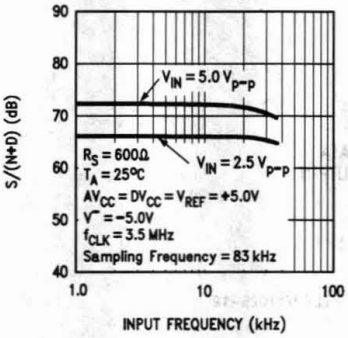
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance



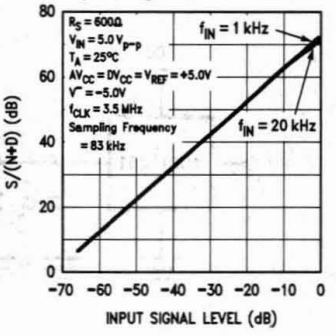
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



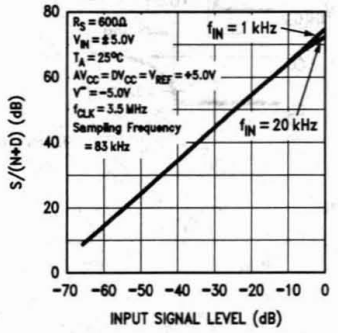
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



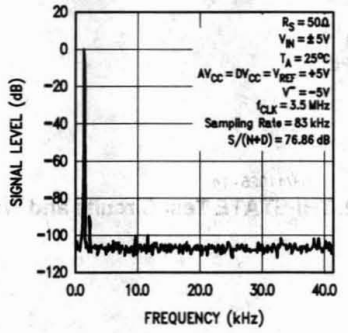
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



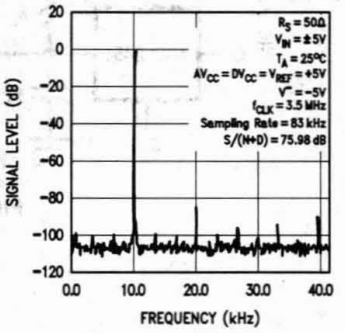
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



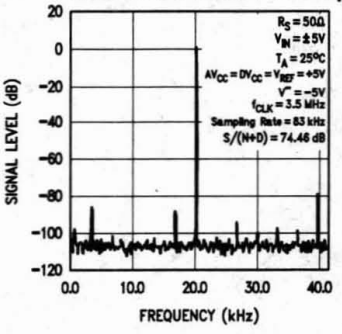
Bipolar Spectral Response with 1 kHz Sine Wave Input



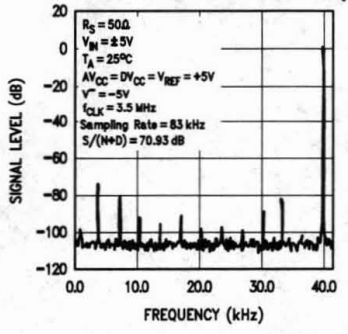
Bipolar Spectral Response with 10 kHz Sine Wave Input



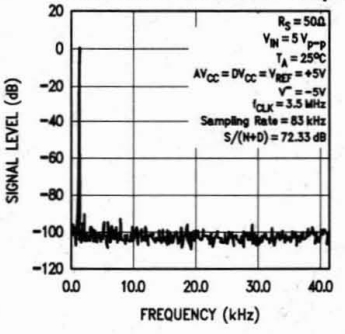
Bipolar Spectral Response with 20 kHz Sine Wave Input



Bipolar Spectral Response with 40 kHz Sine Wave Input



Unipolar Spectral Response with 1 kHz Sine Wave Input



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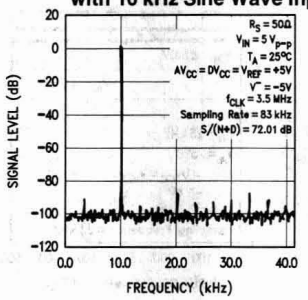
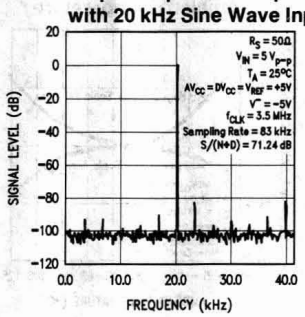
2

Typical Performance Characteristics (Continued)

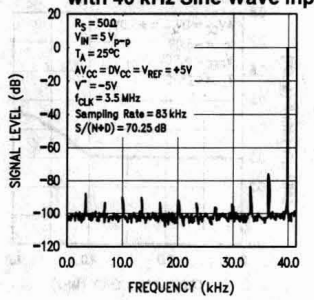
Unipolar Spectral Response with 10 kHz Sine Wave Input



Unipolar Spectral Response with 20 kHz Sine Wave Input



Unipolar Spectral Response with 40 kHz Sine Wave Input



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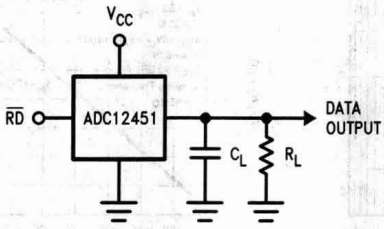
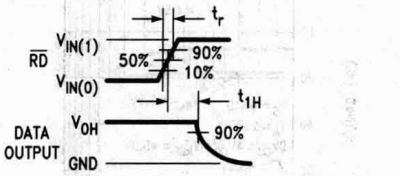
Test Circuits



TL/H/11025–12



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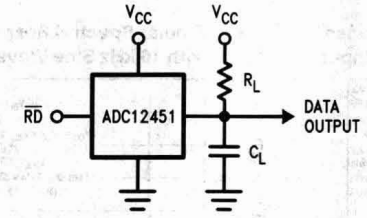

TL/H/11025–14

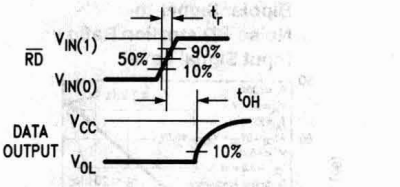

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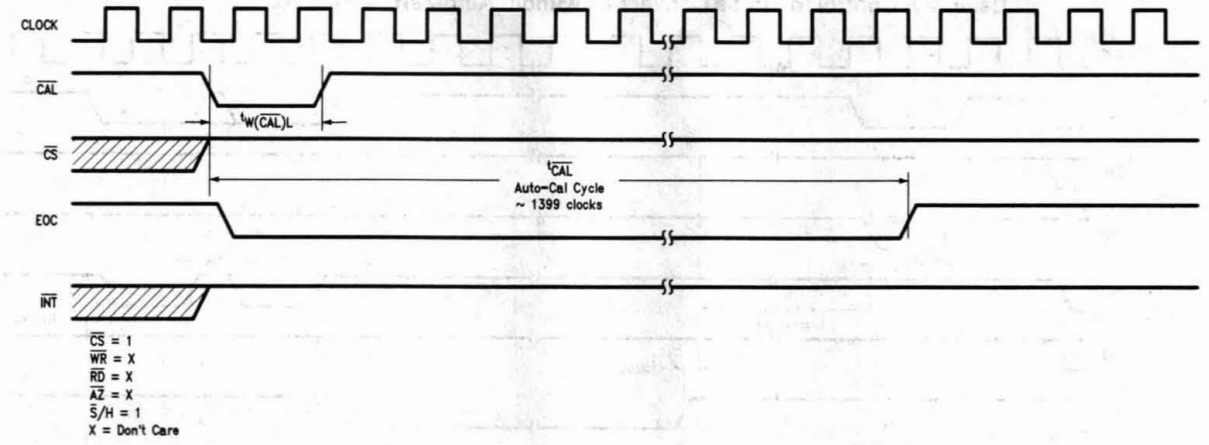
FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Auto-Cal Cycle



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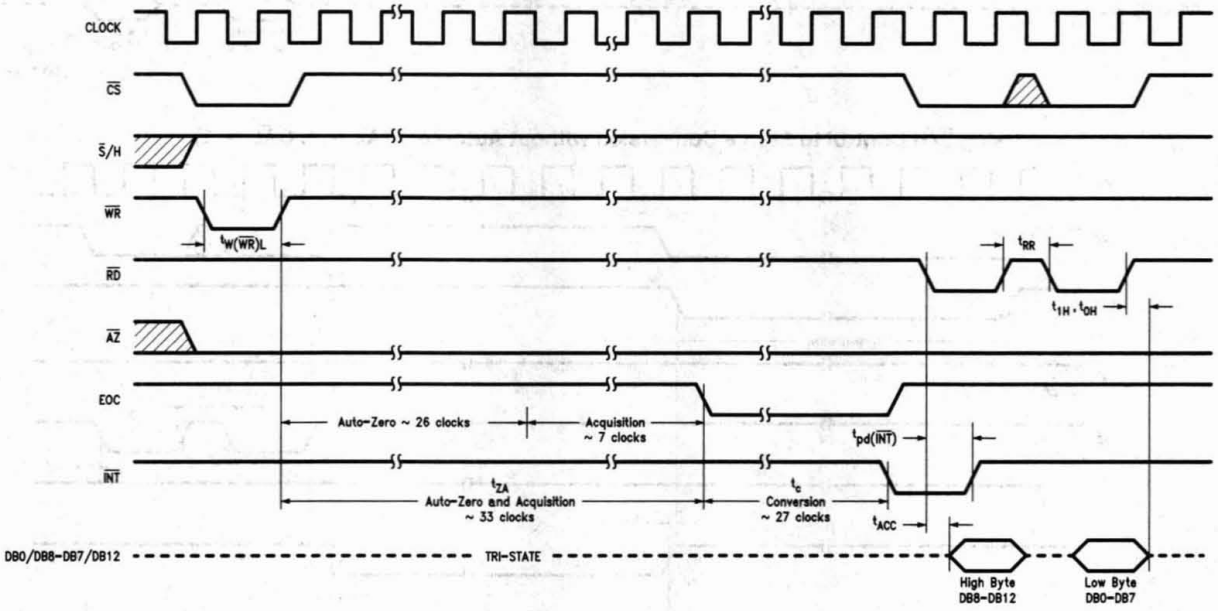
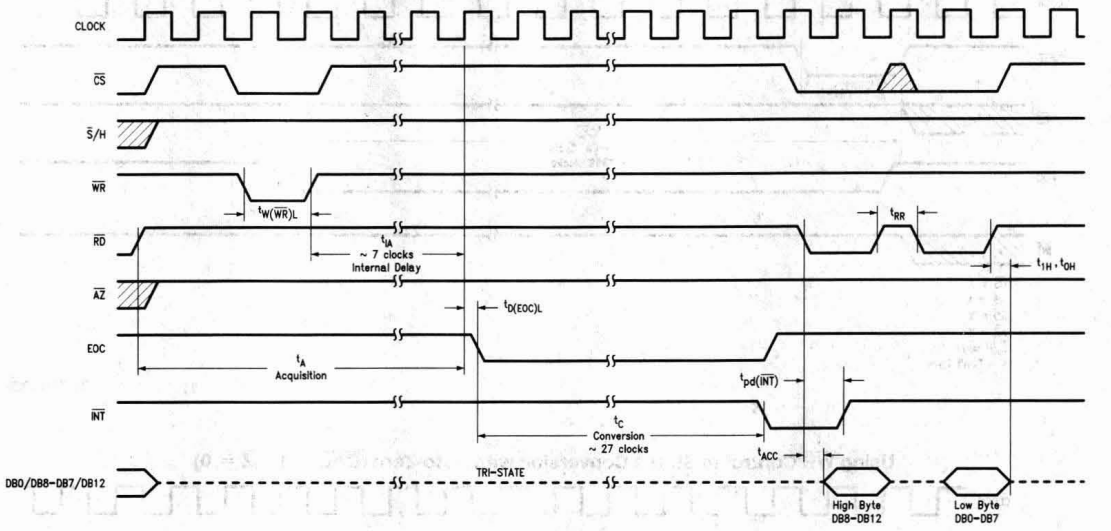
Using WR Control to Start a Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



TL/H/11025–17

Timing Diagrams (Continued)

Using $\overline{WR}$ Control to Start a Conversion without Auto-Zero ($\overline{CAL}$ 1, $\overline{AZ}$ = 1)



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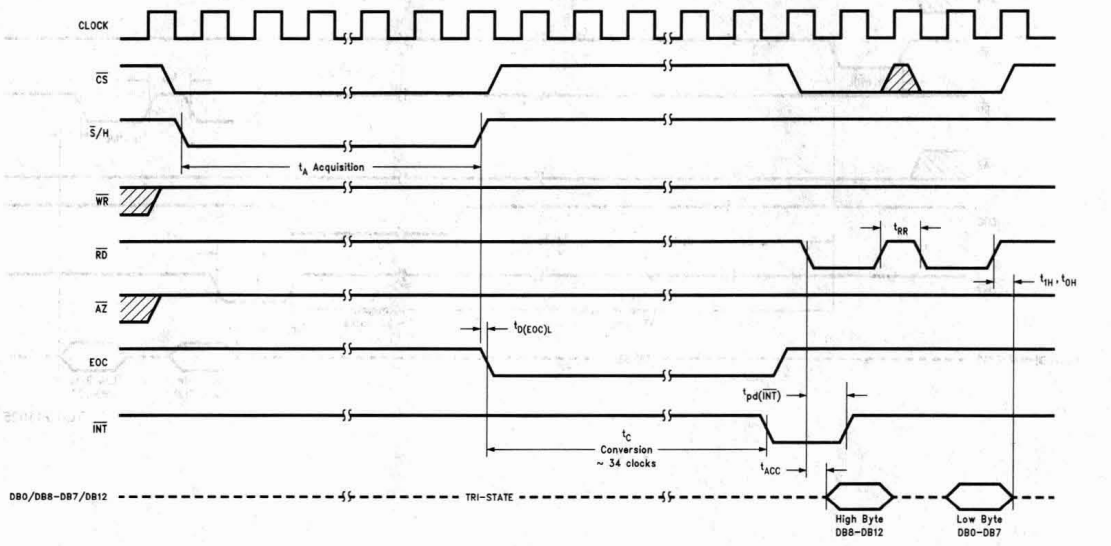
Using $\overline{S}$/H Control to Start a Conversion without Auto-Zero ($\overline{AZ}$ = 1, $\overline{CAL}$ = 1)



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1.0 Pin Descriptions

DV_{CC} (24), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC12451 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass capacitors (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs bypass capacitors of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (12), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below +3.5 V_{DC}.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$, $\overline{RD}$ and $\overline{S}$/H functions.

$\overline{RD}$ (23) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The conversion is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low. When this control line is used the end of the analog input voltage acquisition window is internally controlled by the ADC12451.

$\overline{S}$/H (11) — The sample and hold control input. This control input can also be used to start a conversion. With $\overline{CS}$ low the falling edge of $\overline{S}$/H starts the analog input acquisition window. The rising edge of $\overline{S}$/H ends the acquisition window and starts a conversion.

CLKIN (8) — The external clock input pin. The typical clock frequency range is 500 kHz to 6.0 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC12451 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC12451 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (22) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (21) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0/DB8 - DB7/DB12 (13–20) — The TRI-STATE output pins. Twelve bit plus sign output data access is accomplished using two successive $\overline{RD}$s of one byte each, high byte first (DB8–DB12). The data format used is two's complement sign bit extended with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC12451 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Calibration routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC12451 without the need of trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC12451 at any time, which ensures accuracy over temperature and time.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$ and $\overline{S}$/H high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1399 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch error is found. Correction factors for these errors are then stored in internal RAM.

A conversion is initiated by taking $\overline{CS}$ and $\overline{WR}$ low. If $\overline{AZ}$ is low an Auto-Zero cycle, which takes approximately 26 clock periods, is inserted before the analog input is sampled and the actual conversion is started. $\overline{AZ}$ must remain low during the complete conversion sequence. After Auto-Zero the acquisition opens and the analog input is sampled for appproximately 7 clock periods. If $\overline{AZ}$ is high, the Auto-Zero cycle is not inserted after the rising edge of $\overline{WR}$. In this case the acquisition window opens when the ADC12451 completes a conversion, signaled by the rising edge of EOC. At the end of the acquisition window EOC goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

2.0 Functional Description (Continued)

A conversion sequence can also be controlled by the $\overline{S}$/H and $\overline{CS}$ inputs. Taking $\overline{CS}$ and $\overline{S}$/H low starts the acquisition window for the analog input voltage. The rising edge of $\overline{S}$/H immediately puts the A/D in the hold mode and starts the conversion. Using $\overline{S}$/H will simplify synchronizing the end of the acquisition window to other signals, which may be necessary in a DSP environment.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC12451. Next $\overline{INT}$ goes low, and EOC goes high to signal the end of the conversion.

The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0/DB8–DB7/DB12 output buffers. The high byte of data is relayed first on the data bus outputs as shown below:

DB0/ DB8	DB1/ DB9	DB2/ DB10	DB3/ DB11	DB4/ DB12	DB5/ DB12	DB6/ DB12	DB7/ DB12
Bit 8	Bit 9	Bit 10	MSB	Sign Bit	Sign Bit	Sign Bit	Sign Bit

Taking $\overline{CS}$ and $\overline{RD}$ low a second time will relay the low byte of data on the data bus outputs as shown below:

DB0/ DB8	DB1/ DB9	DB2/ DB10	DB3/ DB11	DB4/ DB12	DB5/ DB12	DB6/ DB12	DB7/ DB12
LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7

The table in *Figure 3* summarizes the effect of the digital control inputs on the function of the ADC12451. The Test Mode, where $\overline{RD}$ and $\overline{S}$/H are high and $\overline{CS}$ and $\overline{CAL}$ are low, is used during manufacture to thoroughly check out the operation of the ADC12451. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

The ADC12451 is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ or $\overline{S}$/H low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore requiring an Auto-Cal cycle before the next conversion. When using $\overline{WR}$ or $\overline{S}$/H without Auto-Zero ($\overline{AZ}$ = 1) to start a conversion, a new conversion can be restarted only after EOC has gone high signaling the end of the current conversion. When using $\overline{WR}$ with Auto-Zero ($\overline{AZ}$ = 0) a new conversion can be restarted during the first 26 clock periods after the rising edge of $\overline{WR}$ (t_Z) or after EOC has returned high without corrupting the Auto-Cal correction factors.

The Calibration Cycle cannot be reset once started. On power-up the ADC12451 automatically goes through a Calibration Cycle that takes typically 1399 clock cycles. For reasons that will be discussed in Section 3.8, a new calibration cycle needs to be started after the completion of the automatic one.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 4a* is an example of a very stable reference that is appropriate for use with the ADC12451. The simple reference circuit of *Figure 4b* may be used when the application does not require a low full-scale error.

Digital Control Inputs						A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{S}$/H	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊓	⊓	1	1	1	1	Start Conversion without Auto-Zero
⊓	1	⊓	1	1	1	Start Conversion synchronous with rising edge of $\overline{S}$/H without Auto-Zero
⊓	1	1	⊓	1	1	Read Conversion Result without Auto-Zero
⊓	⊓	1	1	1	0	Start Conversion with Auto-Zero
⊓	1	1	⊓	1	0	Read Conversion Result with Auto-Zero
1	X	1	X	⊓	X	Start Calibration Cycle
0	X	X	1	0	X	Test Mode (DB2, DB3, DB5, and DB6 become active)

FIGURE 3. Function of the A/D Control Inputs

3.0 Analog Considerations (Continued)

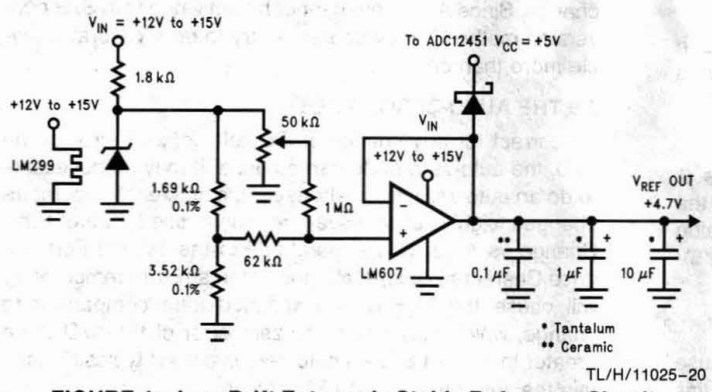
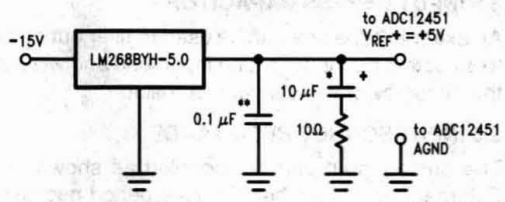


FIGURE 4a. Low Drift Extremely Stable Reference Circuit



Errors without any trims:

	25°C	−40°C to +85°C
Full Scale	±0.075%	±0.2%
Zero	±0.024%	±0.024%
Linearity	±½ LSB	±½ LSB

FIGURE 4b. Simple Reference Circuit

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 ACQUISITION WINDOW

As shown in the timing diagrams there are three different methods of starting a conversion, each of which affects the acquisition window and timing.

With Auto-Zero high a conversion can be started with the $\overline{WR}$ or $\overline{S}$/H controls. In either method of starting a conversion the rising edge of EOC signals the actual beginning of the acquisition window. At this time a voltage spike may be noticed on the analog input of the ADC12451 whose amplitude is dependent on the input voltage and the source resistance. The timing diagrams for these two methods of starting a conversion do not show the acquisition window starting at this time because the acquisition time (t_A) must start after the conversion result high and low bytes have been read. This is necessary since activating and deactivating the digital outputs (DB0/DB7–DB8/DB12) causes current fluctuations in the ADC12451's internal DV_{CC} lines. This generates digital noise which couples into the capacitive ladder that stores the analog input voltage. Therefore, the time interval between the rising edge of EOC and the second read is inappropriate for analog input voltage acquisition.

When $\overline{WR}$ is used to start a conversion with $\overline{AZ}$ low the Auto-Zero cycle is inserted before the acquisition window. In this method the acquisition window is internally controlled by the ADC12451 and lasts for approximately 7 clock periods. Since the acquisition window needs to be at least 3.5 μs at all times, when using Auto-Zero the maximum clock frequency is limited to 2 MHz. The zero error with the Auto-Zero cycle is production tested at a clock frequency of 1.75 MHz. This accommodates easy switching between a conversion with the Auto-Zero cycle (f_{CLK} = 1.75 MHz) and without (f_{CLK} = 3.5 MHz) as shown in *Figure 5*.

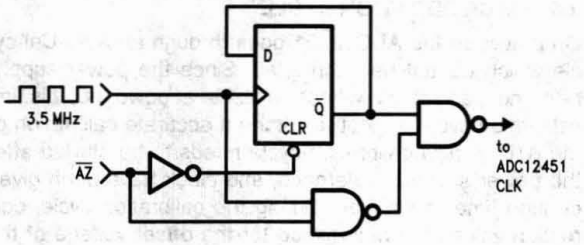


FIGURE 5. Switching between a Conversion with and without Auto-Zero when Using $\overline{WR}$ Control

3.3 INPUT CURRENT

Because the input network of the ADC12451 is made up of a switch and a network of capacitors a charging current will flow into or out of (depending on the input voltage polarity) of the analog input pin (V_{IN}) on the start of the analog input sampling period. The peak value of this current will depend on the actual input voltage applied and the source resistance.

3.4 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.0 Analog Considerations (Continued)

3.5 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.6 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 6*. External R_S will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With $t_A = 3.5\ \mu s$, $R_S \leq 1\ k\Omega$ will allow a 5V analog input voltage to settle properly.

3.7 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the Auto-Zero or -Cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors should be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.8 THE CALIBRATION CYCLE

On power up the ADC12451 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ±0.2 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if Auto-Zero is used to correct the zero error change. Since Auto-Zero cannot be activated with $\overline{S}$/H conversion method it may be necessary to do a calibration cycle more than once.

3.9 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature changes significantly. (See the curve titled "Zero Error Change vs Ambient Temperature" in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than ±1 LSB. An auto-zero cycle will typically maintain the zero error to ±1 LSB or less.

4.0 Dynamic Performance

Many applications require the A/D converter to digitize ac signals, but the standard dc integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with ac input signals. The important specifications for ac applications reflect the converter's ability to digitize ac signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio (S/(N+D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's ac performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N+D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in the table of Electrical Characteristics, and spectral plots of S/(N+D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N+D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N+D) or S/N drops 3 dB).

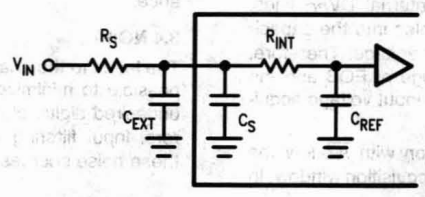


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FIGURE 6. Analog Input Equivalent Circuit

4.0 Dynamic Performance (Continued)

Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.8)\ dB$$

where n is the A/D's resolution in bits.

The effective bits of a real A/D converter, therefore, can be found by:

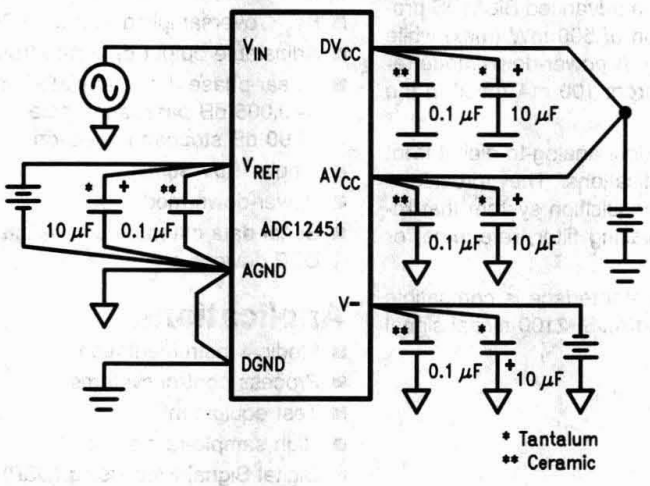
$$n(\text{effective}) = \frac{S/N(dB) - 1.8}{6.02}$$

As an example, an ADC12451 with a ±5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC12451 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC12451, the hold command is internally generated. When the Auto-Zero function is not being used, the hold command occurs at the end of the acquisition window, or seven clock periods after the rising edge of the $\overline{WR}$. The delay between the internally generated hold command and the time that the ADC12451 actually holds the input signal is the aperture time. For the ADC12451, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC12451 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

5.0 Typical Applications

Power Supply Bypassing



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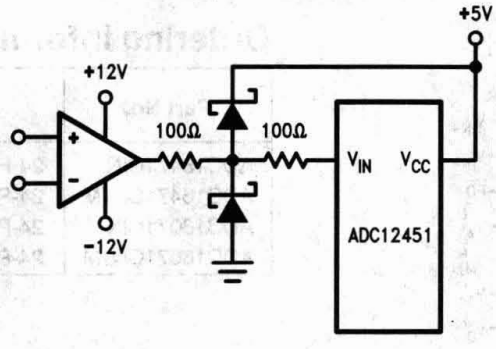
Protecting the Analog Inputs



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Note: External protection diodes should be able to withstand the op amp current limit.

National Semiconductor

ADC16071/ADC16471
16-Bit Delta-Sigma 192 ks/s Analog-to-Digital Converters

General Description

The ADC16071/ADC16471 are 16-bit delta-sigma analog-to-digital converters using 64 × oversampling at 12.288 MHz. A 5th-order comb filter and a 246 tap FIR decimation filter are used to achieve an output data rate of up to 192 kHz. The combination of oversampling and internal digital filtering greatly reduces the external anti-alias filter requirements to a simple RC low pass filter. The FIR filters offer linear phase response, 0.005 dB passband ripple, and ≥90 dB stopband rejection. The ADC16071/ADC16471's analog fourth-order modulator uses switched capacitor technology. A built-in fully-differential bandgap voltage reference is also included in the ADC16471. The ADC16071 has no internal reference and requires externally applied reference voltages.

The ADC16071/ADC16471 use an advanced BiCMOS process for a low power consumption of 500 mW (max) while operating from a single 5V supply. A power-down mode reduces the power supply current from 100 mA (max) in the active mode to 1.3 mA (max).

The ADC16071/ADC16471 are ideal analog-to-digital front ends for signal processing applications. They provide a complete high resolution signal acquisition system that requires a minimal external anti-aliasing filter, reference, or interface logic.

The ADC16071/ADC16471's serial interface is compatible with the DSP56001, TMS320, and ADSP2100 digital signal processors.

Key Specifications

- Resolution — 16 bits
- Total harmonic distortion
  - 48 kHz output data rate — −94 dB (typ)
  - 192 kHz output data rate — −80 dB (typ)
- Maximum output data rate — 192 kHz (min)
- Power dissipation
  - — Active
    - 192 kHz output data rate — 500 mW (max)
    - 48 kHz output data rate — 275 mW (max)
  - — Power-down — 6.5 mW (max)

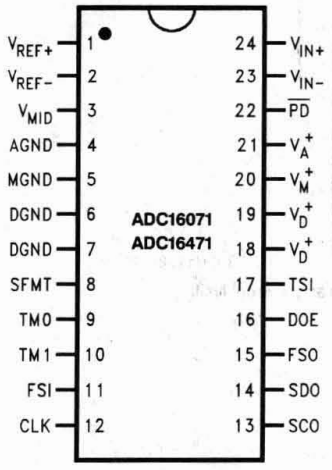
Key Features

- Voltage reference (ADC16471 only)
- Fourth-order modulator
- 64 × oversampling with a 12.288 MHz sample rate
- Adjustable output data rate from 7 kHz to 192 kHz
- Linear-phase digital anti-aliasing filter:
  - — 0.005 dB passband ripple
  - — 90 dB stopband rejection
- Single +5V supply
- Power-down mode
- Serial data interface compatible with popular DSP devices

Applications

- Medical instrumentation
- Process control systems
- Test equipment
- High sample-rate audio
- Digital Signal Processing (DSP) analog front-end
- Vibration and noise analysis

Connection Diagram



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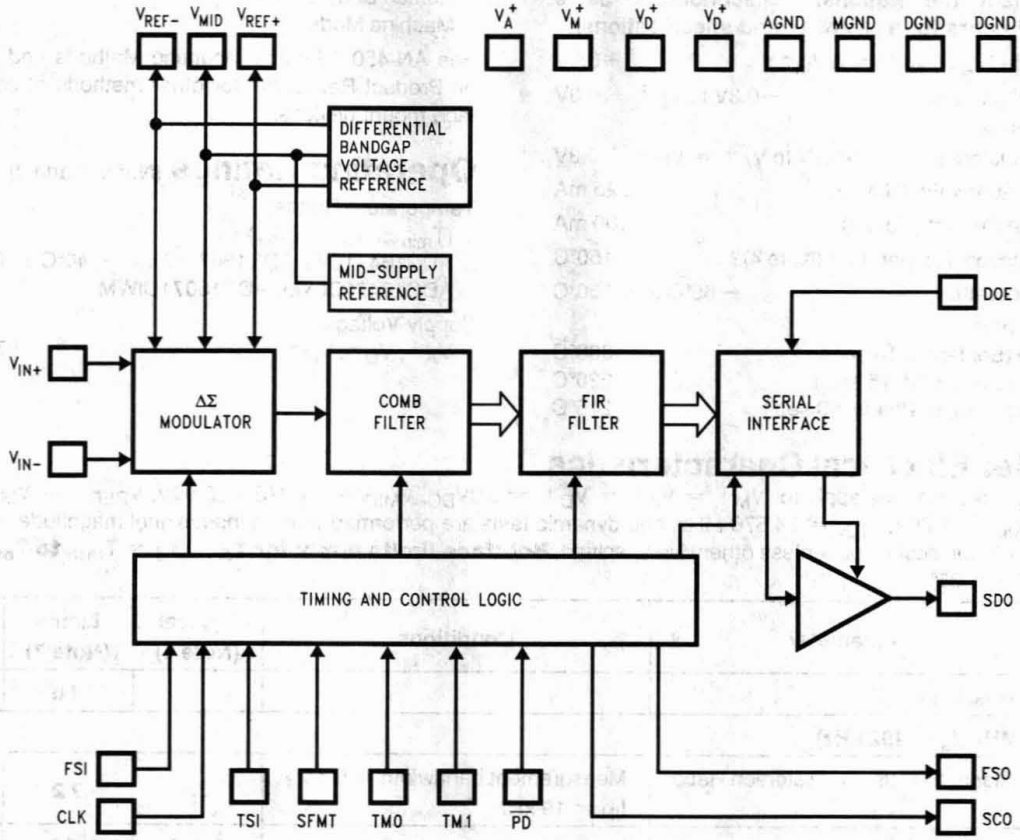
Ordering Information

Part No.	Package	NS Package No.
ADC16471CIN	24-Pin Molded DIP	N24C
ADC16471CIWM	24-Pin SOIC	M24B
ADC16071CIN	24-Pin Molded DIP	N24C
ADC16071CIWM	24-Pin SOIC	M24B

Block Diagram

ADC16471



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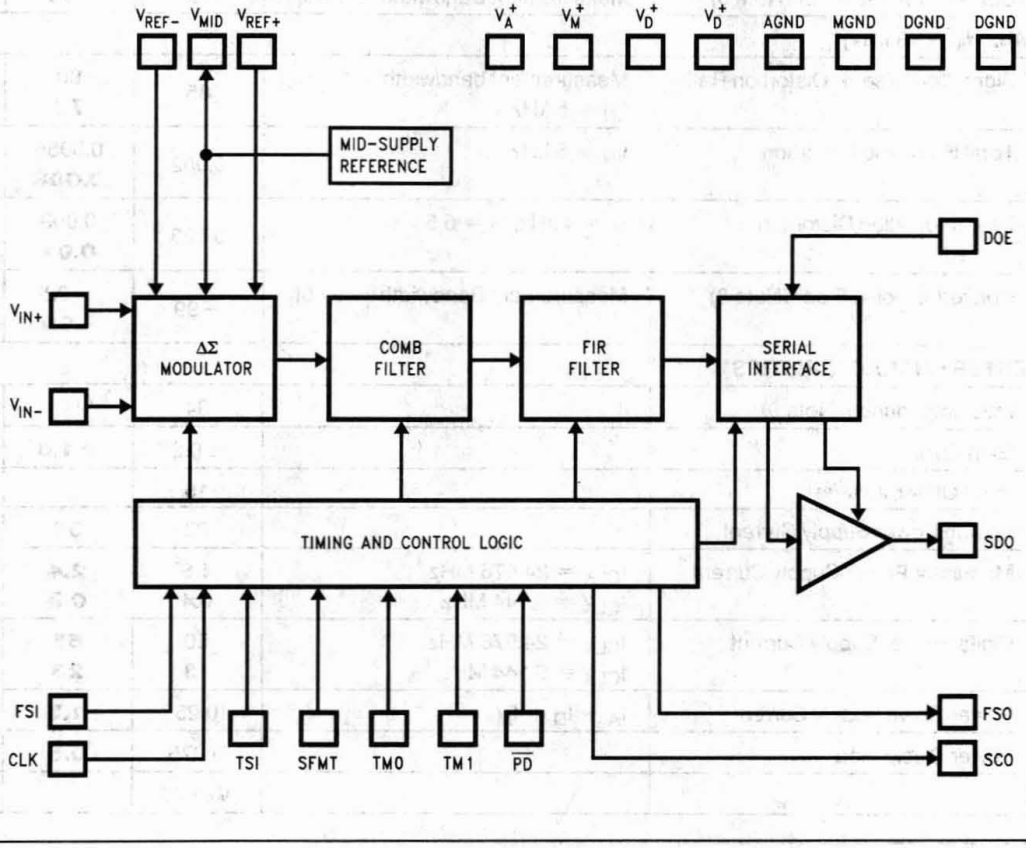
ADC16071



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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_A^+, V_D^+, and V_M^+)	+6.5V
Logic Control Inputs	−0.3V to V_D^+ + 0.3V
Voltage at Other Inputs and Outputs	−0.3V to $V_A^+ = V_M^+$ + 0.3V
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±100 mA
Maximum Junction Temperature (Note 4)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package (Soldering, 10 sec.)	300°C
WM Package (Infrared, 15 sec.)	220°C
WM Package (Vapor Phase, 60 sec.)	215°C
ESD Susceptibility (Note 5)	
Human Body Model	4000V
Machine Model	250V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 and 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	
ADC16471CIN, ADC16071CIN, ADC16471CIWM, ADC16071CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage	
V_A^+, V_D^+, V_M^+	4.75V to 5.25V

Converter Electrical Characteristics

The following specifications apply for $V_M^+ = V_A^+ = V_D^+ = 5.0V_{DC}$, $V_{MID} = V_A^+/2 = 2.50V$, $V_{REF+} = V_{MID} + 1.25V$, $V_{REF-} = V_{MID} - 1.25V$, $f_{CLK} = 24.576$ MHz, and dynamic tests are performed with an input signal magnitude set at −6 dB with respect to a full-scale input unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{min}$ to T_{max}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
	Resolution			**16**	Bits
f_{CLK} = 24.576 MHz (f_s = 192 kHz)					
S/(N+D)	Signal-to-Noise + Distortion Ratio	Measurement bandwidth = $0.45f_s$ f_{IN} = 19 kHz	76	**72**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 19 kHz	0.010	**0.022**	% (max)
IMD	Intermodulation Distortion	f_1 = 18.5 kHz, f_2 = 19.5 kHz	0.010	**0.017**	% (max)
	Converter Noise Floor (Note 8)	Measurement Bandwidth = $0.45f_s$	−88	**−77**	dBFS (min)
f_{CLK} = 6.144 MHz (f_s = 48 kHz)					
S/(N+D)	Signal-to-Noise + Distortion Ratio	Measurement bandwidth = $0.45f_s$ f_{IN} = 5 kHz	85	80 **73**	dB (min) dB (min)
THD	Total Harmonic Distortion	f_{IN} = 5 kHz	0.002	0.0055 **0.008**	% (max) % (max)
IMD	Intermodulation Distortion	f_1 = 4 kHz, f_2 = 5.5 kHz	0.003	0.009 **0.01**	% (max) % (max)
	Converter Noise Floor (Note 8)	Measurement Bandwidth = $0.45f_s$	−99	−92 **−89**	dBFS (min) dBFS (min)
OTHER CONVERTER CHARACTERISTICS					
Z_{IN}	Input Impedance (Note 9)		34		kΩ
ΔA_V	Gain Error		±0.2	**±1.0**	%FS (max)
V_{OS}	Input Offset Voltage		15		mV
I_A	Analog Power Supply Current		23	**31**	mA (max)
I_M	Modulator Power Supply Current	f_{CLK} = 24.576 MHz f_{CLK} = 6.144 MHz	1.6 0.4	**2.4** **0.8**	mA (max)
I_D	Digital Power Supply Current	f_{CLK} = 24.576 MHz f_{CLK} = 6.144 MHz	50 13	**65** **23**	mA (max)
I_{SPD}	Power-Down Supply Current	$I_A + I_D + I_M$	0.25	**1.3**	mA
P_D	Power Dissipation		0.375	**0.5**	W
V_{MID}			$V_A^+/2$		V

Digital Filter Characteristics

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{min}$ to T_{max}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
	Stopband Rejection		−90.0		dB
	Passband Ripple		±0.005		dB
	3 dB Cutoff Frequency		0.45		fs
	Data Latency		3,968		Clock Cycles

Reference Characteristics (ADC16471 Only)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{min}$ to T_{max}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
V_{REF}^+	Positive Internal Reference Output Voltage		$V_{MID} + 1.25$	**$V_{MID} + 1.175$** **$V_{MID} + 1.325$**	V (min) V (max)
V_{REF}^-	Negative Internal Reference Output Voltage		$V_{MID} - 1.25$	**$V_{MID} - 1.325$** **$V_{MID} - 1.175$**	V (min) V (max)
$\Delta(V_{REF+} - V_{REF-})/\Delta T$	Internal Reference Temperature Coefficient		30		ppm/°C
$\Delta V_{REF+}/\Delta I$	Positive Internal Reference Load Regulation	Sourcing (0 mA ≤ I ≤ +10 mA) Sinking (−1 mA ≤ I ≤ 0 mA)	3.4	**6.0**	mV (max)
$\Delta V_{REF-}/\Delta I$	Negative Internal Reference Load Regulation	Sinking (−1 mA ≤ I ≤ 0 mA) Sourcing (0 mA ≤ I ≤ 10 mA)	3.2	**6.0**	

Input Reference Characteristics (ADC16071 Only)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units
V_{REF+}	Positive Reference Voltage		1 V_A+		V V
V_{REF-}	Negative Reference Voltage		0 $V_A+ - 1$		V V
$V_{REF+} - V_{REF-}$	Total Reference Voltage		1 V_A+		V V

DC Electrical Characteristics

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
V_{IH}	Logic High Input Voltage	$V_D^+ = 5.25V$		**V_D^+** **2.3**	V (max) V (min)
V_{IL}	Logic Low Input Voltage	$V_D^+ = 4.75V$		**0.8** **−0.3**	V (max) V (min)
V_{OH}	Logic High Output Voltage	Logic High Output Current = −400 μA, $V_D^+ = 4.75V$		**2.4**	V (min)
V_{OL}	Logic Low Output Voltage	Logic Low Output Current = 2 mA, $V_D^+ = 5.25V$		**0.5**	V (max)
$I_{IN(1)}$	Logical "1" Input Current		1.0	**5.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current		−1.0	**−5.0**	μA (max)
I_{TSI}	SDO TRI-STATE® Leakage Current	$V_{IN} = 0.4V$ to 2.4V	1.0	**5.0**	μA (max)
C_{IN}	Logic Input Capacitance	$V_{IN} = 0$ to V_D^+	5		pF

AC Electrical Characteristics for Clock In (CLK), Serial Clock Out (SCO), and Frame Sync In (FSI)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
f_{CLK}	CLK Frequency Range ($f_{CLK} = 1/t_{CLK}$)			**25** **1**	MHz (max) MHz (min)
t_{CLK}	CLK Period ($t_{CLK} = 1/f_{CLK}$)			**1000** **40**	ns (max) ns (min)
t_{CLKL}	CLK Low Pulse Width			**16**	ns (min)
t_{CLKH}	CLK High Pulse Width			**14**	ns (min)
t_R	CLK Rise Time			**10** **3**	ns (max) ns (min)
t_F	CLK Fall Time			**10** **3**	ns (max) ns (min)
t_{FSILOW}	Minimum Frame Sync Input Low Time before Frame Sync Input Asserted High		2		t_{CLK} (min)
t_{FSISU}	Frame Sync Input Setup Time			**10**	ns (min)
t_{FSIH}	Frame Sync Input Hold Time			**10**	ns (min)
t_{SCOD}	Serial Clock Output Delay Time from Rising Edge of CLK		12	**20** **5**	ns (max) ns (min)
t_{SCO}	Serial Clock Output Period			**4**	t_{CLK}

AC Electrical Characteristics for Frame Sync Out (FSO), Serial Clock Out (SCO), and Serial Data Out (SDO)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
$t_{SCOFSOH}$	Delay from Serial Clock Out to Frame Sync Output High		2	**5**	ns (max)
$t_{SCOFSOL}$	Delay from Serial Clock Out to Frame Sync Output Low		2	**5**	ns (max)
t_{SDOV}	Delay from Serial Clock Out to Serial Data Output Valid		3	**8**	ns (max)
$t_{FSIFSOL}$	Delay from Frame Sync Input to Frame Sync Output Low			**8**	t_{CLK} (max)

AC Electrical Characteristics for Data Output Enable (DOE)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
t_{DOEE}	Data Output Enable Delay Time		20	**25**	ns (max)
t_{DOED}	Data Output Disable Delay Time		16	**20**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > (V_A^+, V_M^+,$ or $V_D^+)$), the current at that pin should be limited to 25 mA. The 100 mA maximum package input current rating allows the voltage at any four pins, with an input current of 25 mA each, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation is a function of the maximum junction temperature ($T_{J(MAX)}$), total thermal resistance (θ_{JA}), and ambient temperature (T_A). The maximum allowable power dissipation at any ambient temperature is $P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$. When board mounted, the ADC16071/ADC16471's typical thermal resistance is:

Order Number	θ_{JA}
ADC16071CIN, ADC16471CIN	47°C/W
ADC16071CIWM, ADC16471CIWM	72°C/W

Note 5: Human body model, 100 pF discharge through a 1.5 kΩ resistor. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 6: Typicals are at $T_A = 25°C$ and represent most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 8: The V_{IN}^+ pin is shorted to the V_{IN}^- pin.

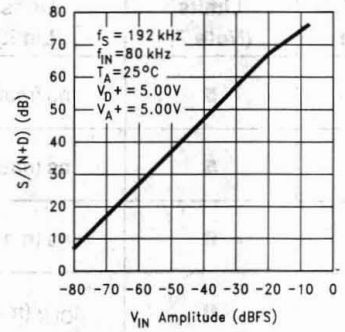
Note 9: The input impedance between V_{IN+} and V_{IN-} due to the effective resistance of the switch capacitor input varies as follows:

$$Z_{IN} = \frac{10^{12}}{2.35^* \left(\frac{f_{CLK}}{2}\right)}$$

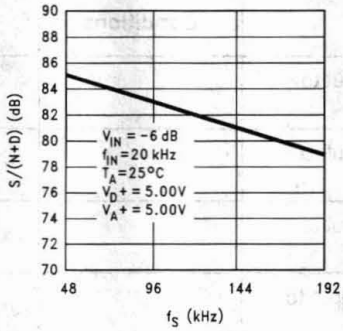
2

Typical Performance Characteristics

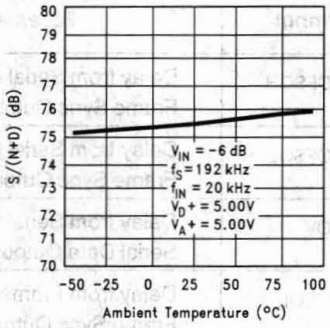
S/(N + D) vs V_{IN} Amplitude



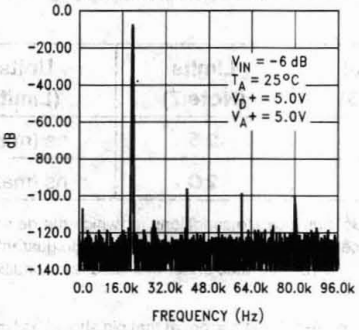
S/(N + D) vs Output Data Rate (fs)



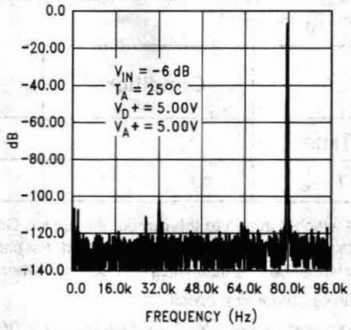
S/(N + D) vs Temperature



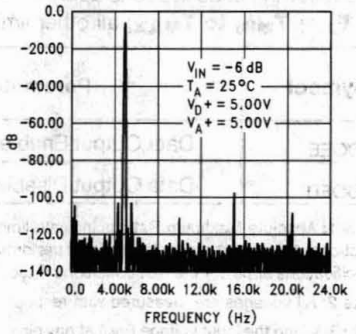
Spectral Response, f_S = 192 kHz, f_{IN} = 20 kHz



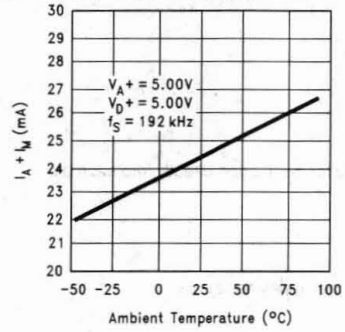
Spectral Response, f_S = 192 kHz, f_{IN} = 80 kHz



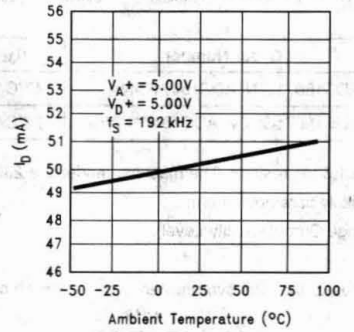
Spectral Response, f_S = 48 kHz, f_{IN} = 5 kHz



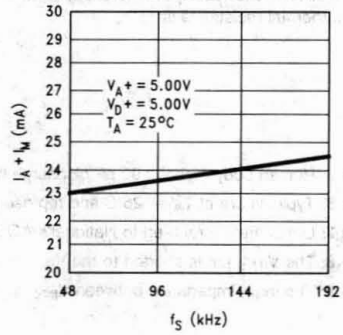
Analog Supply Current (I_A + I_M) vs Temperature



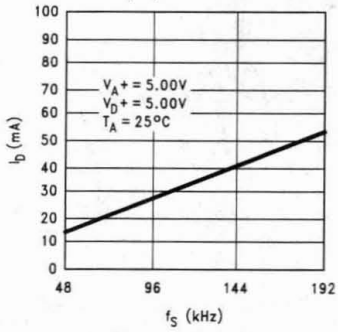
Digital Supply Current I_D vs Temperature



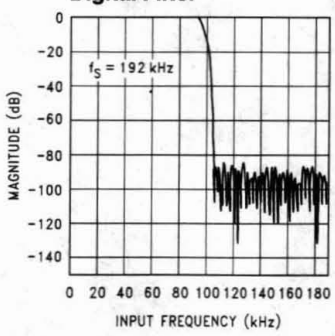
Analog Supply Current (I_A + I_M) vs Output Data Rate (fs)



Digital Supply Current (I_D) vs Output Data Rate (fs)



Frequency Response of Digital Filter



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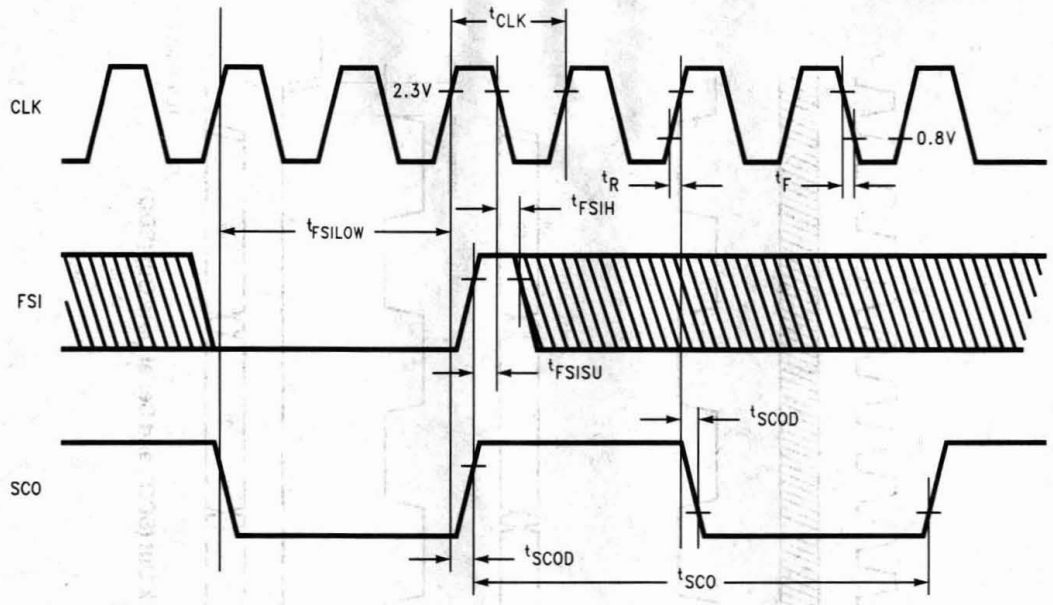

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FIGURE 1. Timing Diagrams for Clock Input (CLK), Frame Sync Input (FSI), and Serial Clock Output (SCO)

2

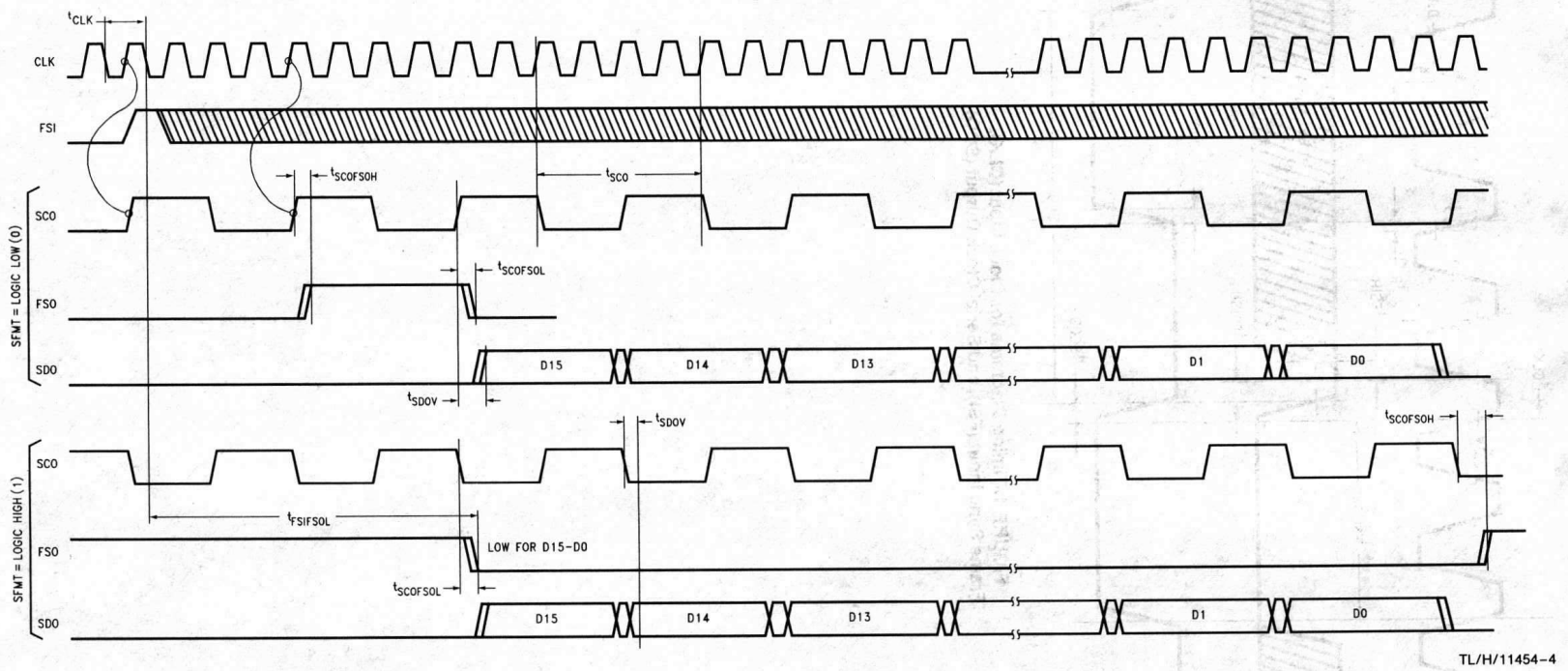

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FIGURE 2. Detailed Timing Diagrams for Frame Sync Input (FSI), Frame Sync Out (FSO), Serial Clock Out (SCO), and Serial Data Out (SDO)

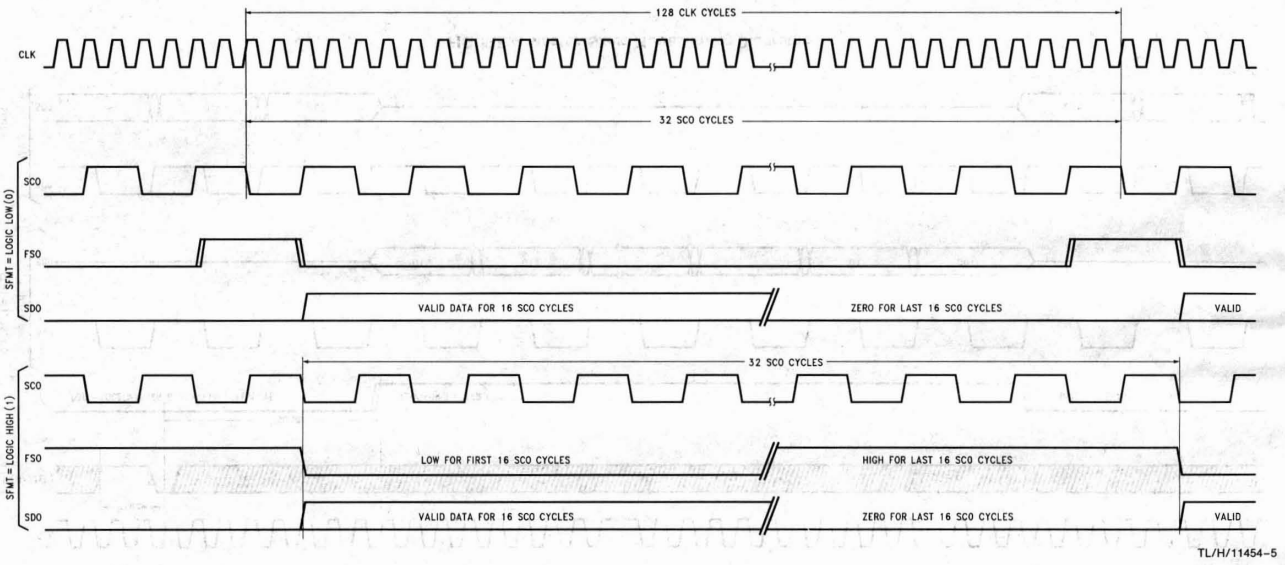

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FIGURE 3. Timing Diagrams for Frame Sync Out (FSO), Serial Clock Out (SCO), and Serial Data Out (SDO)

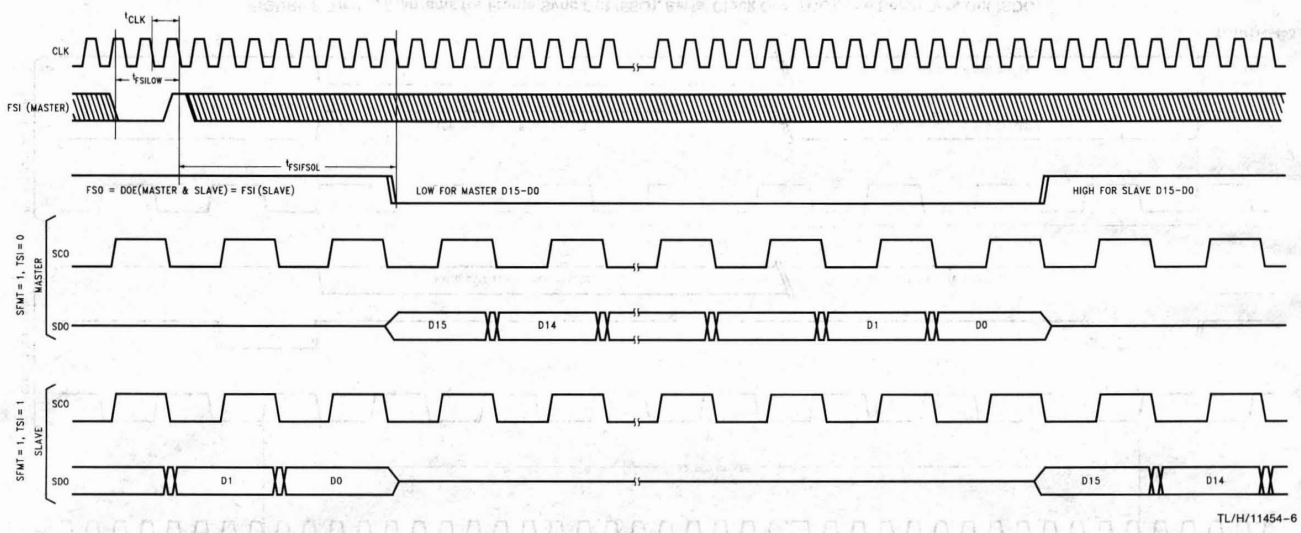

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FIGURE 4. Master/Slave Mode Timing Diagrams

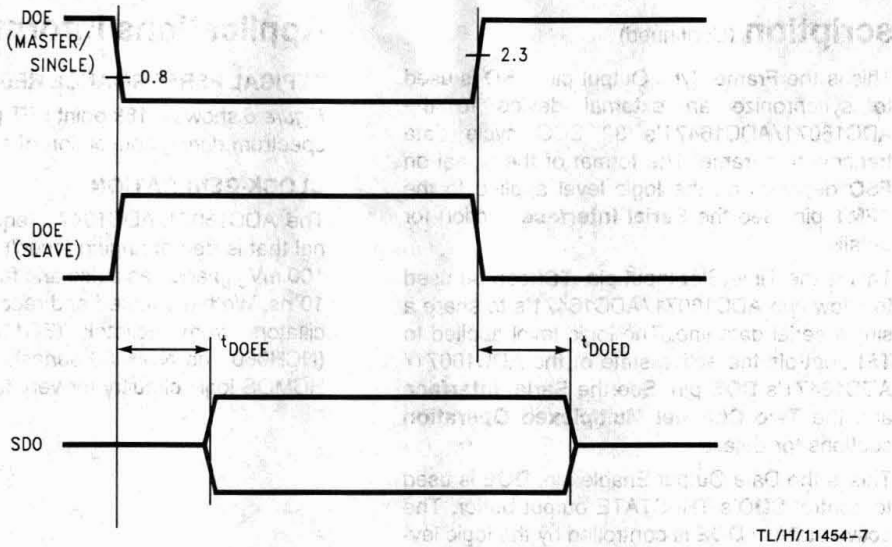

FIGURE 5. Timing Diagrams for Data Output Enable ($\overline{DOE}$) and Serial Data Out (SDO)

Pin Description

$V_{REF}+$, $V_{REF}-$ These are the ADC16471's internal differential reference's bypass pins. Their nominal output voltage is ±1.25V centered around the voltage at the V_{MID} pin, typically $V_A+/2$. V_{REF+}, V_{MID}, and V_{REF-} should be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors. For the ADC16071, these are the reference voltage inputs. V_{REF+} and V_{MID} should be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_{MID} This pin is the internal differential reference's $V_A+/2$ output pin. V_{MID} should be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

$V_{IN}+$, $V_{IN}-$ These are the ADC's differential input pins. Signals applied to these pins can be single-ended or differential with respect to the V_{MID} voltage.

$\overline{PD}$ This is the input pin used to activate the power-down mode. When a logic LOW (0) is applied to this pin the supply current drops from 100 mA (max) to 1.3 mA (max).

AGND This is the connection to system analog ground. Internally, this ground is connected to the analog circuitry, including the fourth-order modulator.

DGND This is the connection to system digital ground. Internally, this ground is connected to all digital circuitry except the modulator's clock.

MGND This is the ground pin for the modulator's clock. It should be connected to analog ground through its own connection that is separate from that used by AGND.

V_A+ This pin is the connection to the system analog voltage supply. Best performance is achieved when this pin is bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_M+ This is the modulator's supply pin. V_M+ should be connected to the system analog voltage supply with a circuit board trace or connection that is separate from that used to supply V_A+. Best performance is achieved when this pin is bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_D+ This pin is the connection to the system digital voltage supply. Best performance is achieved when this pin is bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

SFMT This is the Serial Format pin. The logic level applied to the **SFMT** pin determines whether conversion data shifted out of the **SDO** pin is valid on the rising or falling edge of **SCO**. It also controls the format of the Frame Sync Out **(FSO)** signal. See the **Serial Interface** section for details.

TM0, TM1 Used to enabled test mode during production. Connect both pins to DGND.

FSI This is the Frame Sync Input pin. **FSI** is an input used to synchronize the ADC16071/ADC16471's conversions to an external source. The state of **FSI** is sampled on the falling edge of **CLK**. See the **Serial Interface** section for details.

CLK This is the clock signal input pin. The signal applied to this pin sets the sample rate of the ADC16071/ADC16471's modulator to $f_{CLK}/2$. The frequency range can be 1 MHz ≤ f_{CLK} ≤ 25 MHz.

SCO This is the Serial Clock Output pin. The ADC16071/ADC16471's serial data transmission is synchronous with the **SCO** signal. **SCO** has a frequency of $f_{CLK}/4$. See the **Serial Interface** section for details.

SDO This is the Serial Data Output pin. The ADC16071/ADC16471's conversion data is shifted out from this pin synchronous to the **SCO** signal. See the **Serial Interface** section for details.

Pin Description (Continued)

FSO This is the Frame Sync Output pin. **FSO** is used to synchronize an external device to the ADC16071/ADC16471's 32 SCO cycle data transmission frame. The format of the signal on **FSO** depends on the logic level applied to the **SFMT** pin. See the **Serial Interface** section for details.

TSI This is the Time Slot Input pin. **TSI** can be used to allow two ADC16071/ADC16471's to share a single serial data line. The logic level applied to **TSI** controls the active state of the ADC16071/ADC16471's **DOE** pin. See the **Serial Interface** and the **Two Channel Multiplexed Operation** sections for details.

DOE This is the Data Output Enable pin. **DOE** is used to control **SDO**'s TRI-STATE output buffer. The active state of **DOE** is controlled by the logic level applied to the **TSI** pin. See the **Serial Interface** and the **Two Channel Multiplexed Operation** sections for details.

Applications Information

TYPICAL PERFORMANCE RESULTS

Figure 6 shows a 16k point FFT plot of the baseband output spectrum during conversion of a 24 kHz input signal.

CLOCK GENERATION

The ADC16071/ADC16471 requires a sampling-clock signal that is free of ringing (over/undershoot of no more than 100 mV_{p-p}) and has a rise and fall time in the range of 3 ns–10 ns. We have tested and recommended crystal clock oscillators from Ecliptek (EC1100 series) and SaRonix (NCH060 and NCH080 series). Both of these families use HCMOS logic circuitry for very fast rise and fall times.

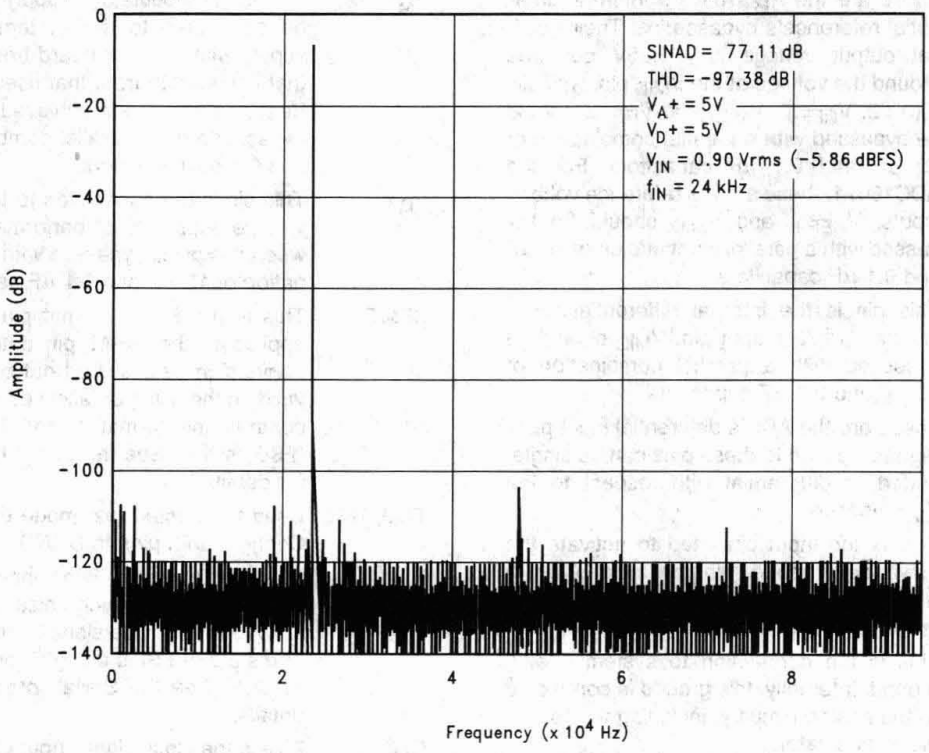

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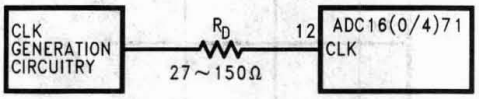
FIGURE 6. Typical Performance of the ADC16071/ADC16471 at f_S = 192 kHz, f_{IN} = 24 kHz

Applications Information (Continued)

Overshoot and ringing can be reduced by adding a series damping resistor between the crystal oscillator's output (pin 8) and the ADC16071/ADC16471's CLK (pin 12), as shown in *Figure 7*. The actual resistor value is dependent on the board layout and trace length that connects the oscillator or CLK source to the ADC. A typical starting value is 50Ω with a range of 27Ω to 150Ω.



TL/H/11454–23

FIGURE 7. Damping Resistor Reduces Clock Signal Overshoot

SERIAL INTERFACE

The ADC16071 and the ADC16471 have three serial interface output pins: Serial Data Output **(SDO)**, Frame Sync Output **(FSO)**, and Serial Clock Output **(SCO)**. **SCO** has a frequency of $f_{CLK}/4$. Each of the ADC16071/ADC16471's 16-bit conversions is transmitted within the first half of the **data transmission frame**. A data transmission frame is 32 SCO cycles in duration. Two's complement data shifts out on the **SDO** pin beginning with bit 15 (MSB) and ending with bit 0 (LSB), taking 16 **SCO** cycles. **SDO** then shifts out zeroes for the next 16 **SCO** cycles to maintain compatibility with two channel multiplexed operation.

The serial data that is shifted out of the **SDO** pin is synchronous with **SCO**. Depending on the logic level applied to the Serial Format pin **(SFMT)**, the data on the **SDO** pin is valid on either the falling or rising edge of **SCO**. If a logic Low is applied to **SFMT**, then the data on **SDO** is valid on the falling edge of **SCO**. If a logic High is applied to **SFMT**, then the data on **SDO** is valid on the rising edge of **SCO**. See *Figure 2*.

The **FSO** signal is used to synchronize other devices to the ADC16071/ADC16471's data transmission frame. Depending on the logic level applied to **SFMT**, the signal on **FSO** is either a short pulse (approximately one SCO cycle in duration) ending just before the transmission of bit 15 on **SDO**, or a square wave with a period of 32 SCO cycles going low just before the transmission of bit 15 and going high just after the transmission of bit 0. If a logic Low is applied to **SFMT**, **FSO** will be high for approximately one SCO cycle and fall low just before the transmission of bit 15 and stay low for the remainder of the transmission frame. If a logic High is applied to **SFMT**, **FSO** will be low during the transmission of bits 15–0 and high during the next 16 SCO cycles. See *Figure 3*.

The Frame Sync Input (**FSI**), is used to synchronize the ADC16071/ADC16471's conversions to an external source. The logic state of **FSI** is captured by the ADC16071/ADC16471 on the falling edge of **CLK**. If an **FSI** low to high transition is sensed between adjacent **CLK** falling edges, the ADC16071/ADC16471 will interrupt its current data transmission frame and begin a new one. See *Figure 4*.

Due to the data latency of the ADC16071/ADC16471's digital filters, the first 31 conversions following a frame sync input signal will represent inaccurate data, unless the frame syncs are applied at constant 32 SCO cycle intervals. If no **FSI** signal is applied (FSI is kept High or Low), the ADC16071/ADC16471 will internally create a frame sync every 32 SCO cycles.

The Data Output Enable pin (**DOE**), is used to enable and disable the output of data on **SDO**. When **DOE** is deactivated, **SDO** stops driving the serial data line by entering a high impedance TRI-STATE. **DOE**'s active state matches the logic level applied to the Time Slot Input pin (**TSI**). If a logic Low is applied to **TSI**, the ADC16071/ADC16471's **SDO** pin will shift out data when **DOE** is Low, and be in a high impedance TRI-STATE when **DOE** is High. If a logic High is applied to **TSI**, **SDO** will shift out data when **DOE** is High, and be in a high impedance TRI-STATE when **DOE** is Low.

TWO CHANNEL MULTIPLEXED OPERATION

Two ADC16071/ADC16471's can easily be configured to share a single serial data line and operate in a "stereo", or two channel multiplexed mode. They share the serial data bus by alternating transmission of conversion data on their respective **SDO** pins. One of the ADC16071/ADC16471's, the Master, shifts its conversion data out of **SDO** during the first 16 SCO cycles of the data transmission frame. The other ADC16071/ADC16471, the Slave, shifts its data out during the second 16 SCO cycles of the data transmission frame.

The Slave is selected by applying a logic High to its **TSI** pin and a logic High to its **SFMT** pin. The Master is chosen by applying a logic Low to its **TSI** pin and a logic High to its **SFMT** pin. As shown in *Figure 8*, the Master's **FSO** is used to control the **DOE** of both the Master and the Slave as well as to synchronize the two ADC16071/ADC16471's by driving the Slave's Frame Sync Input pin, **FSI**. As the Master finishes transmitting its 16 bits of conversion data, its **FSO** goes High. This triggers the Slave's **FSI**, causing the Slave to begin transmitting its 16 bits of conversion data.

The Master's **DOE** is active Low and the Slave's **DOE** is active High. Since the same signal, the Master's **FSO**, is connected to both of the converters' **DOE** pins, one converter will shift out data on its **SDO** pin while the other is in TRI-STATE, allowing the two ADC16071/ADC16471's to share the same serial data transmission line.

POWER SUPPLY AND GROUNDING

The ADC16071/ADC16471 has on-chip 50 pF bypass capacitors between the supply-pin bonding pads and their corresponding grounds. There are 24 of these capacitors, 6 for the analog section and 18 for the digital, resulting in a total value of 1200 pF. They help control ringing on the on-chip power supply busses, especially in the digital section. Further, they help enhance the baseband noise performance of the analog modulator.

Applications Information (Continued)

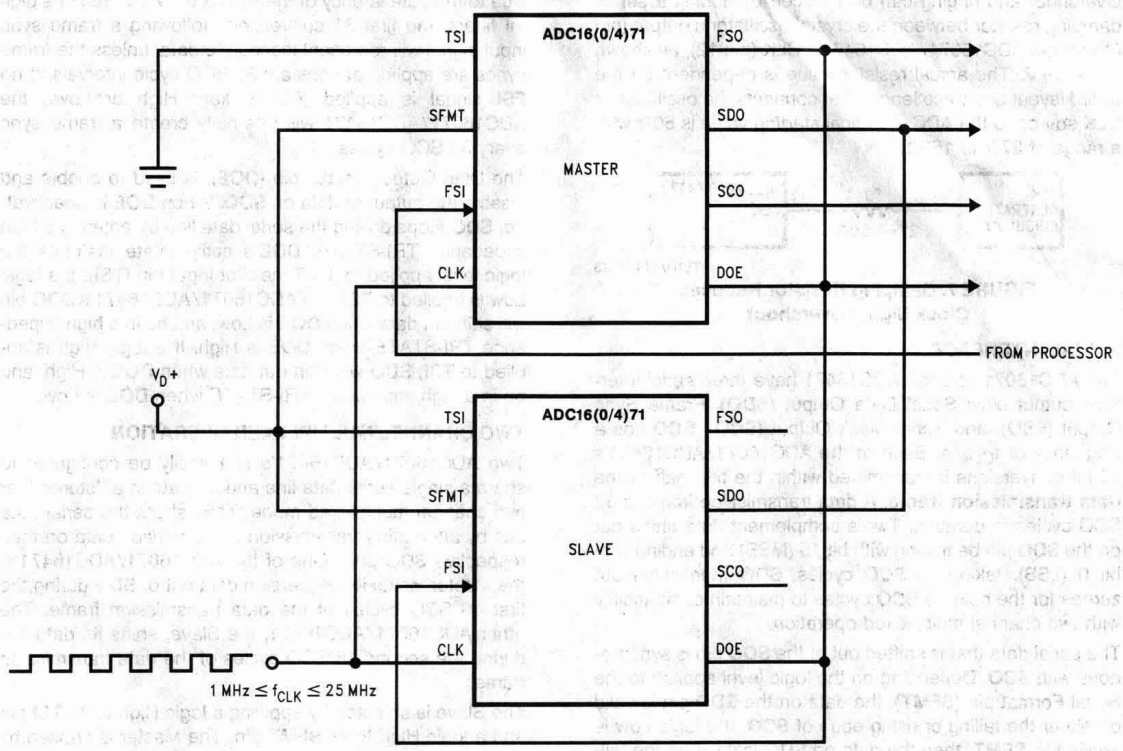


FIGURE 8. Two Channel Multiplexed Operation Connection Diagram

Best converter performance is achieved when these internal bypass capacitors are supplemented with additional external power-supply decoupling capacitors. This ensures the lowest ac-bypass impedance path for the ADC16071/ADC16471's dynamic current requirements. Each of the ADC16071/ADC16471's four supply pins should be individually bypassed, using a parallel combination of 10 μF (tantalum) and 0.1 μF (monolithic ceramic), to its corresponding ground pin:

V_A+ (Pin 21) $\rightarrow$ AGND (Pin 4)
V_M+ (Pin 20) $\rightarrow$ MGND (Pin 5)
V_D+ (Pin 19) $\rightarrow$ DGND (Pin 6)
V_D+ (Pin 18) $\rightarrow$ DGND (Pin 7)

Short lead lengths are mandatory. Therefore, surface mount capacitors are ***strongly*** recommended.

POWER SUPPLY VOLTAGES FOR BEST PERFORMANCE

While adequate performance will be achieved by operating the ADC16071/ADC16471 with +5V connected to V_A+, V_M+ and V_D+, dynamic performance, as measured by S/(N + D), can be further enhanced by slightly raising the analog supply voltage and lowering the digital supply voltage.

ANALOG INPUT

The ADC16071 and the ADC16471 generate a two's complement output determined by the following equation:

$$\text{Output Code} = \frac{(V_{IN}+ - V_{IN}-)\,(32768)}{(V_{REF}+ - V_{REF}-)}$$

Round off to the nearest integer value between −32768 and 32767.

The signals applied to V_{IN}^+ and V_{IN}^- must be between V_A^+ and analog ground. For accurate conversions, the absolute difference between V_{IN}^+ and V_{IN}^- should be less than the difference between V_{REF}^+ and V_{REF}^-. Best harmonic performance will result when a differential voltage is applied to V_{IN}^+ and V_{IN}^- that has a common mode voltage at or below V_{MID}.

Due to overloading in the ADC16071/ADC16471's ΔΣ modulator, performance degrades considerably as the input amplitude approaches full scale. With an input that peaks at −2 dB from full scale, S/(N + D) is about 2 dB worse than with a −6 dB input. With a −1 dB input, S/(N + D) can be 10 dB worse than with a −6 dB input.

Applications Information (Continued)

ANALOG SIGNAL CONDITIONING

The ADC16071/ADC16471's digital comb and FIR filter combine to create the band-limiting anti-aliasing filter, generating a steep cutoff at the upper range of the sampled baseband. Additional external filtering is needed to ensure that the best conversion performance is maintained. The external filtering uses a simple R-C lowpass filter. A suggested circuit is shown in *Figure 9.* The values of R_1, R_2, C_1, C_2, and C_3 are found using the following equation:

$$f_{c\,(-3\,dB)} = \frac{1}{6\pi RC}$$

where $R = R_1 = R_2$ and $C = C_1 = C_2 = C_3$.

The effects of the external filter are minimized by choosing a minimum cutoff frequency equal to $f_{CLK}/32$. As an example, for f_{CLK} equal to 6.144 MHz, set $R_1 = R_2 = 82.5\Omega$ and $C_1 = C_2 = C_3 = 3300$ pF. This sets the input network's cutoff frequency at 194 kHz. For f_{CLK} equal to 24.576 MHz, set $R_1 = R_2 = 20\Omega$ and $C_1 = C_2 = C_3 = 3300$ pF. This sets the input network's cutoff frequency at 803 kHz.

RELATION BETWEEN CAPACITOR DIELECTRIC AND SIGNAL DISTORTION

For any capacitors connected to the ADC16071/ADC16471's analog inputs, the dielectric plays an important role in determining the amount of distortion generated in the input signal. The capacitors used must have low dielectric absorption. This requirement is fulfilled using capacitors that have film dielectrics. Of these, polypropylene and polystyrene are the best. These are followed by polycarbonate and mylar. If ceramic capacitors are chosen, use only capacitors with NPO dielectrics.

INTERNAL DIFFERENTIAL BANDGAP REFERENCE

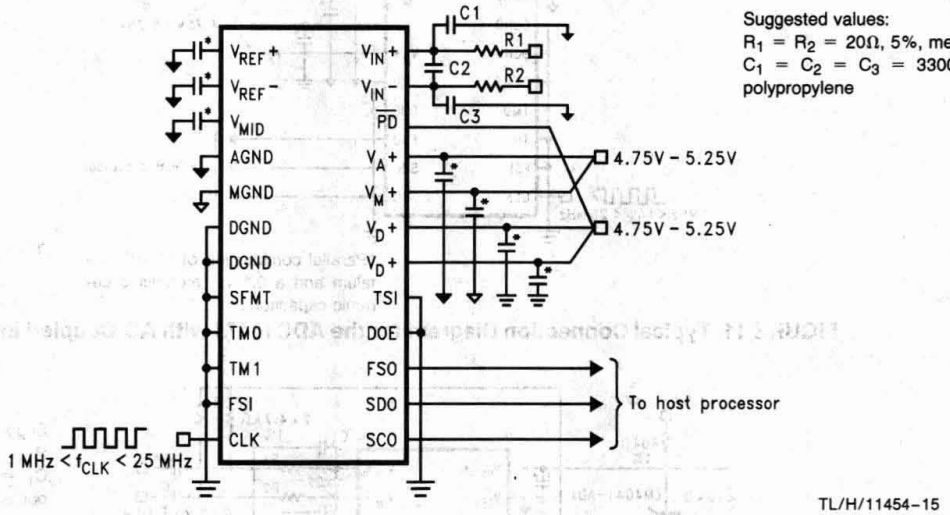
A fully differential bandgap reference generates local feedback voltages, $V_{REF}+$ and $V_{REF}-$, for the analog modulator. The outputs of this reference are trimmed to be equal to V_{MID} plus or minus 1.25V. This gives a differential reference voltage of 2.5V which results in a ±2.5V differential input range. The ADC16071 does not have the internal differential bandgap reference, allowing the user the flexibility to determine the full scale range by using an external voltage reference.

EXTERNAL VOLTAGE REFERENCE FOR THE ADC16071

Figure 10 shows the suggested connection diagram for the ADC16071. The LM4041-ADJ is set to 2.0V and is applied to the ADC16071's $V_{REF}+$ input.

The reference voltage must be free of noise. This is accomplished using the same capacitor combination used with the ADC16471's reference pins with the exception of $V_{REF}-$, which is connected to analog ground.

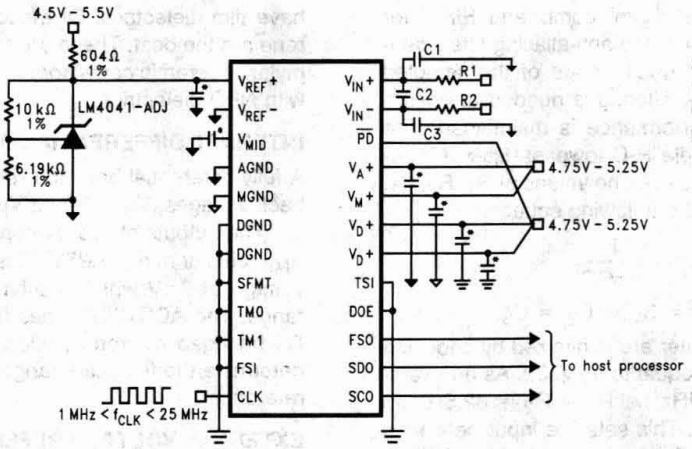
Figures 11 and *12* show the suggested circuits for ac-coupled applications.



*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

FIGURE 9. Typical Connection Diagram for the ADC16471

Applications Information (Continued)



Suggested values:
$R_1 = R_2 = 20\Omega$, 5%, metal film
$C_1 = C_2 = C_3 = 3300$ pF, 5%, polypropylene

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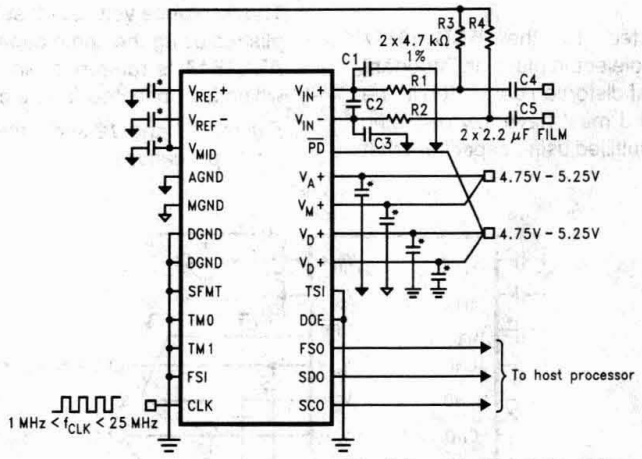
*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

FIGURE 10. Typical Connection Diagram for the ADC16071

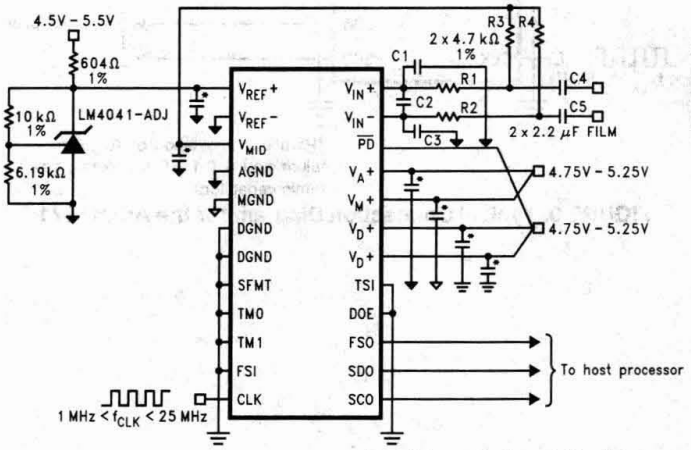


Suggested values:
$R_1 = R_2 = 20\Omega$, 5%, metal film
$C_1 = C_2 = C_3 = 3300$ pF, 5%, polypropylene

TL/H/11454–17

*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

FIGURE 11. Typical Connection Diagram for the ADC16471 with AC-Coupled Inputs



Suggested values:
$R_1 = R_2 = 20\Omega$, 5%, metal film
$C_1 = C_2 = C_3 = 3300$ pF, 5%, polypropylene

TL/H/11454–18

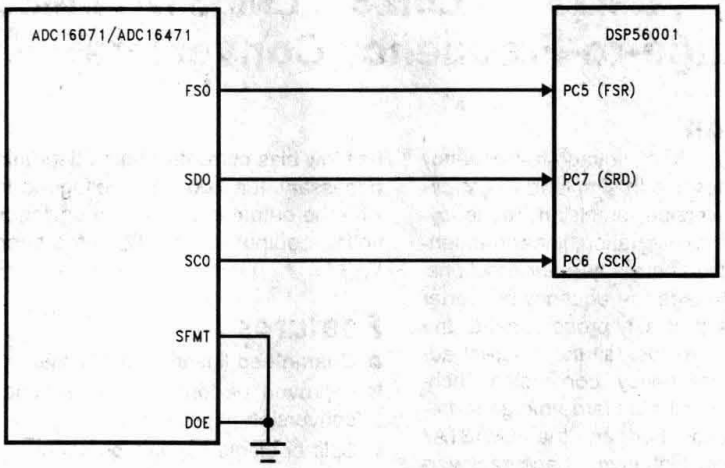
*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

FIGURE 12. Typical Connection Diagram for the ADC16071 with AC-Coupled Inputs

Applications Information (Continued)

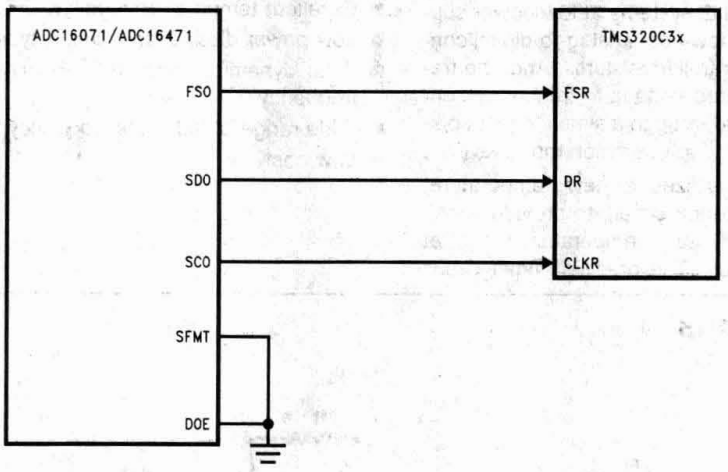
DSP INTERFACES

The ADC16071/ADC16471 was designed to connect to popular DSPs without intervening "glue logic". *Figures 13, 14,* and *15* show suggested connection schematics for the DSP56001, TMS320C3x, and the ADSP-2101 families.



TL/H/11454–19

FIGURE 13. Interface Connections between the ADC16071/ADC16471 and the Motorola DSP56001



TL/H/11454–20

FIGURE 14. Interface Connections between the ADC16071/ADC16471 and the Texas Instruments TMS320C3x

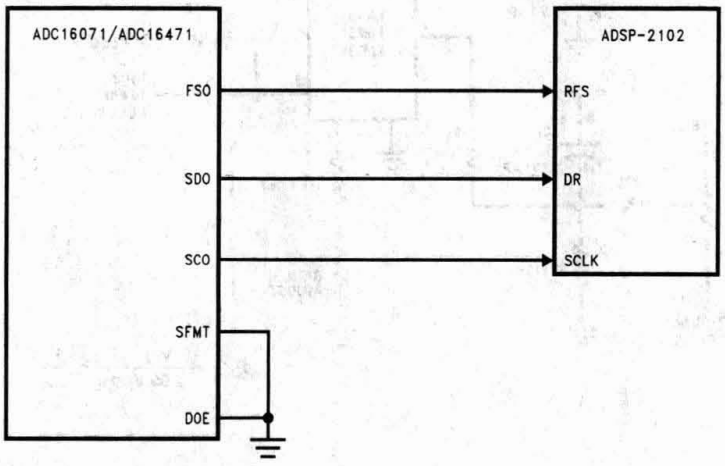


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FIGURE 15. Interface Connections between the ADC16071/ADC16471 and the Analog Devices ADSP-2101

National Semiconductor

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

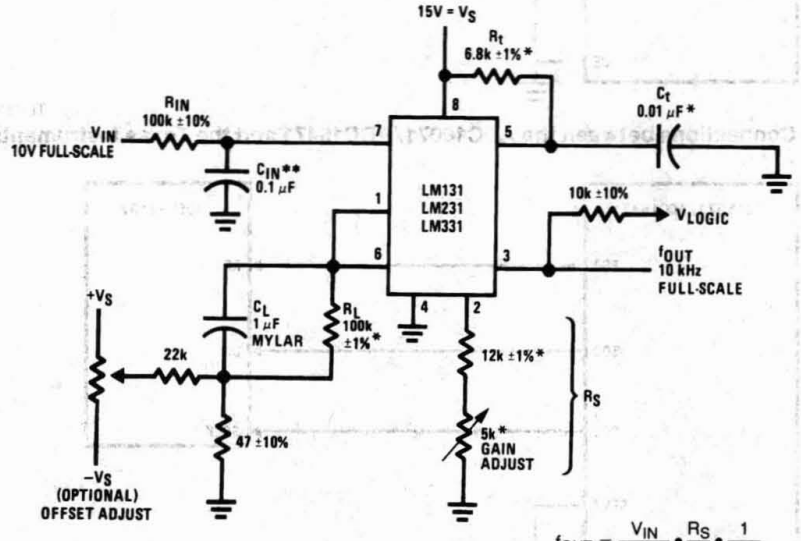
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



*Use stable components with low temperature coefficients. See Typical Applications section.

**0.1μF or 1μF, See "Principles of Operation."

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	−0.2V to $+V_S$	−0.2V to $+V_S$	−0.2V to $+V_S$
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW		
θ_{jA}	150°C/W		
(N Package) P_D		1.25W	1.25W
θ_{jA}		100°C/W	100°C/W
(M Package) P_D		1.25W	
θ_{JA}		85°C/W	
Lead Temperature (Soldering, 10 sec.)			
Dual-In-Line Package (Plastic)	260°C	260°C	260°C
Metal Can Package (TO-5)	260°C		
ESD Susceptibility (Note 4)			
Metal Can Package (TO-5)	2000V		
Other Packages		500V	500V

Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
VFC Non-Linearity (Note 3)	$4.5V \le V_S \le 20V$		±0.003	±0.01	% Full-Scale
	$T_{MIN} \le T_A \le T_{MAX}$		±0.006	±0.02	% Full-Scale
VFC Non-Linearity In Circuit of *Figure 1*	V_S = 15V, f = 10 Hz to 11 kHz		±0.024	±0.14	%Full-Scale
Conversion Accuracy Scale Factor (Gain)	V_{IN} = −10V, R_S = 14 kΩ				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	$T_{MIN} \le T_A \le T_{MAX}$, $4.5V \le V_S \le 20V$				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	$4.5V \le V_S \le 10V$		0.01	0.1	%/V
	$10V \le V_S \le 40V$		0.006	0.06	%/V
Rated Full-Scale Frequency	V_{IN} = −10V	10.0			kHz
Gain Stability vs Time (1000 Hrs)	$T_{MIN} \le T_A \le T_{MAX}$		±0.02		% Full-Scale
Overrange (Beyond Full-Scale) Frequency	V_{IN} = −11V	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	$T_{MIN} \le T_A \le T_{MAX}$		±4	±14	mV
LM131A/LM231A/LM331A	$T_{MIN} \le T_A \le T_{MAX}$		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	$T_{MIN} \le T_A \le T_{MAX}$	−0.2		V_{CC}−2.0	V

Electrical Characteristics $T_A = 25°C$ unless otherwise specified (Note 2) (Continued)

Parameter	Conditions	Min	Typ	Max	Units
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	$\times V_S$
Input Bias Current, Pin 5	V_S = 15V				
All Devices	$0V \le V_{PIN\ 5} \le 9.9V$		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\ 5}$ = 10V		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\ 5}$ = 10V		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\ 1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	$0V \le V_{PIN\ 1} \le 10V$		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	I = 5 mA		0.15	0.50	V
	I = 3.2 mA (2 TTL Loads), $T_{MIN} \le T_A \le T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231,	V_S = 5V	2.0	3.0	4.0	mA
LM231A	V_S = 40V	2.5	4.0	6.0	mA
LM331, LM331A	V_S = 5V	1.5	3.0	6.0	mA
	V_S = 40V	2.0	4.0	8.0	mA

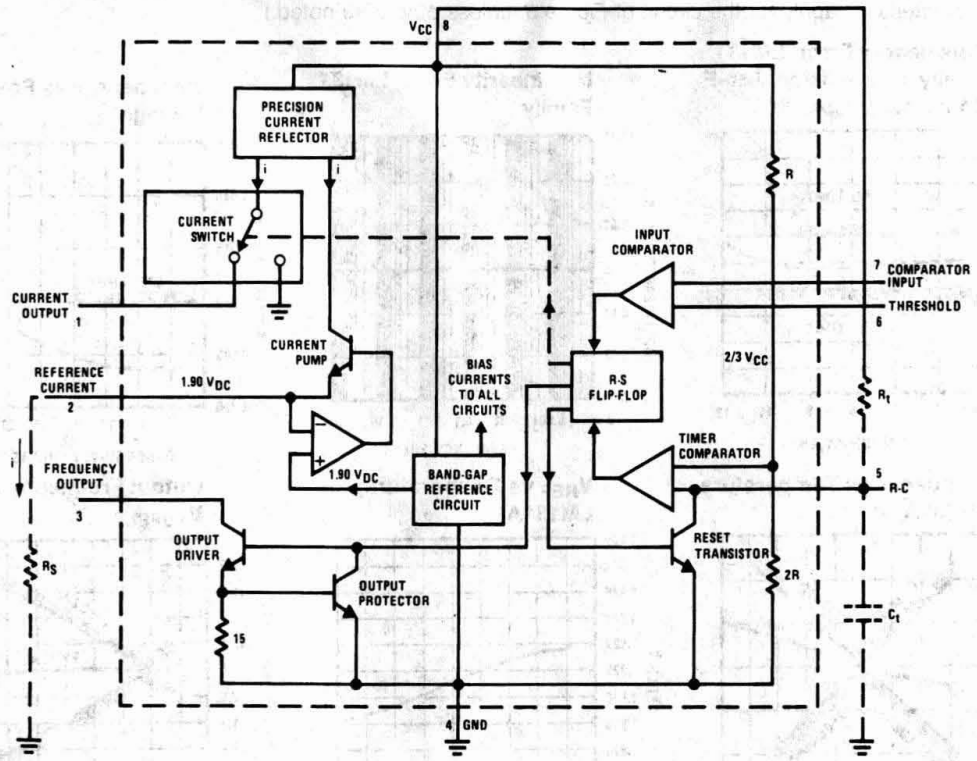
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All specifications apply in the circuit of *Figure 3*, with $4.0V \le V_S \le 40V$, unless otherwise noted.

Note 3: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times (10\ kHz/-10\ V_{DC})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon®, or polystyrene.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Block Diagram



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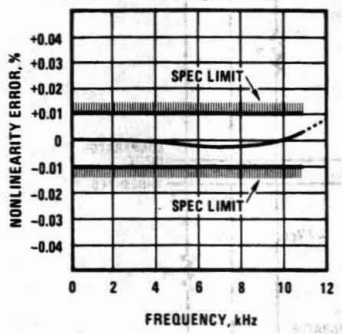
Pin numbers apply to 8-pin packages only. See connection diagram for LM231WM pin numbers.

FIGURE 1a

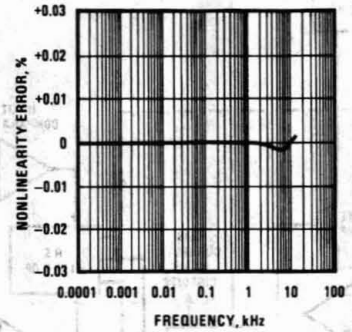
Typical Performance Characteristics

(All electrical characteristics apply for the circuit of *Figure 3*, unless otherwise noted.)

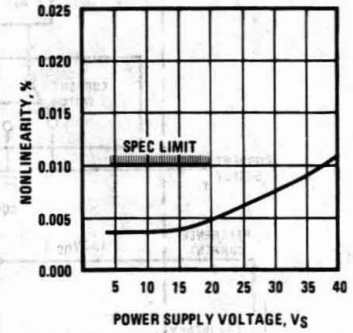
Nonlinearity Error, LM131 Family, as Precision V-to-F Converter (*Figure 3*)



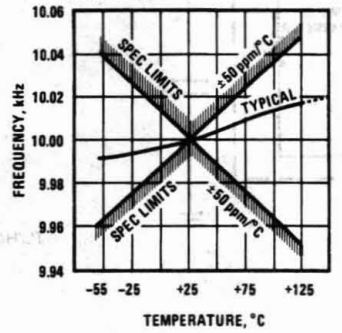
Nonlinearity Error, LM131 Family



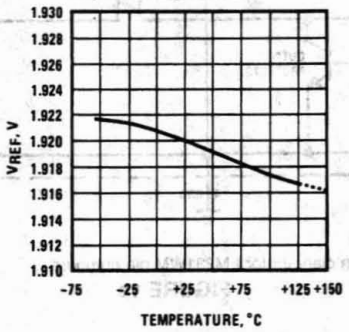
Nonlinearity vs Power Supply Voltage



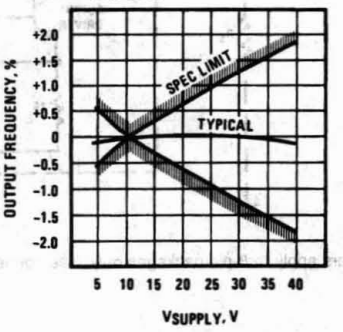
Frequency vs Temperature, LM131A



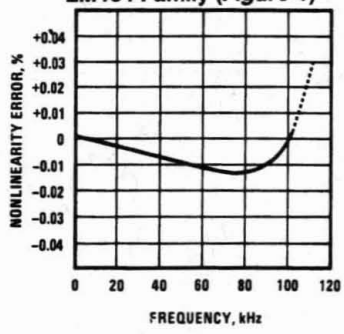
V_{REF} vs Temperature, LM131A



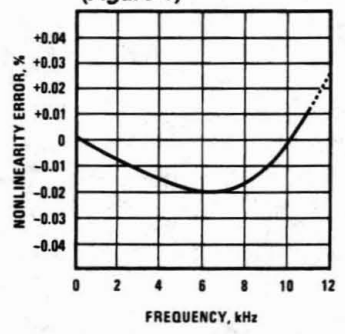
Output Frequency vs V_{SUPPLY}



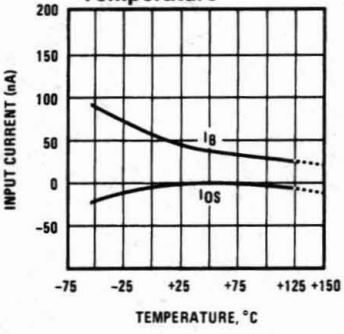
100 kHz Nonlinearity Error, LM131 Family (*Figure 4*)



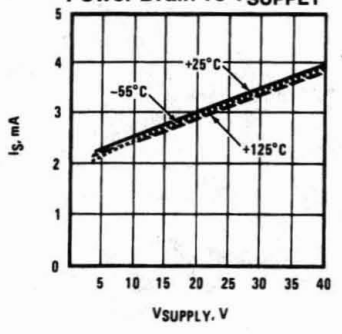
Nonlinearity Error, LM131 (*Figure 1*)



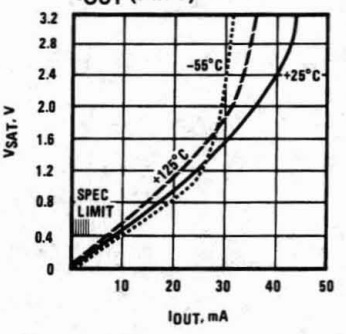
Input Current (Pins 6, 7) vs Temperature



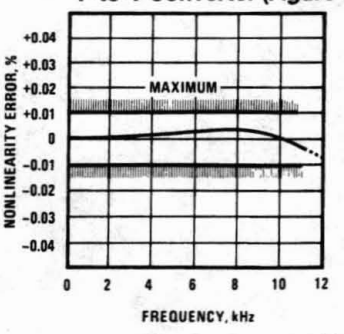
Power Drain vs V_{SUPPLY}



Output Saturation Voltage vs I_{OUT} (Pin 3)



Nonlinearity Error, Precision F-to-V Converter (*Figure 6*)



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Typical Applications (Continued)

PRINCIPLES OF OPERATION OF A SIMPLIFIED VOLTAGE-TO-FREQUENCY CONVERTER

The LM131 is a monolithic circuit designed for accuracy and versatile operation when applied as a voltage-to-frequency (V-to-F) converter or as a frequency-to-voltage (F-to-V) converter. A simplified block diagram of the LM131 is shown in *Figure 2* and consists of a switched current source, input comparator, and 1-shot timer.

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, *Figure 2*, which consists of the simplified block diagram of the LM131 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V1, at pin 7 to the voltage, V_x, at pin 6. If V1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1\ R_tC_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L. This will normally charge V_x up to a higher level than V1. At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_x falls to the level of V1. Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_tC_t) \times f$, and the current flowing out of C_L is exactly $V_x/R_L \cong V_{IN}/R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.

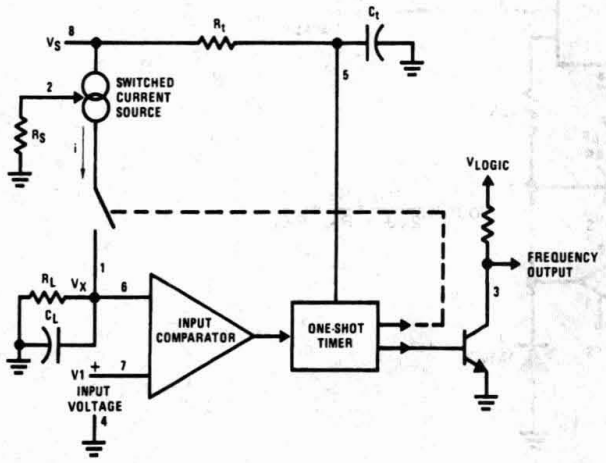

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FIGURE 2. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter Showing LM131 and External Components

DETAIL OF OPERATION, FUNCTIONAL BLOCK DIAGRAM (*FIGURE 1a*)

The block diagram shows a band gap reference which provides a stable 1.9 V_{DC} output. This 1.9 V_{DC} is well regulated over a V_S range of 3.9V to 40V. It also has a flat, low temperature coefficient, and typically changes less than ½% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9V, and causes a current $i = 1.90V/R_S$ to flow. For $R_S = 14k$, $i = 135\ \mu A$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground depending on the state of the R_S flip-flop.

The timing function consists of an R_S flip-flop, and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the R_S flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to ⅔ V_{CC}, the timer comparator causes the R_S flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects pin 7 higher than pin 6 when pin 5 crosses ⅔ V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, in its attempt to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. It should be noted that during this sort of overload, the output frequency will be 0; as soon as the signal is restored to the working range, the output frequency will be resumed.

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω. In case of overvoltage, the output current is actively limited to less than 50 mA.

The voltage at pin 2 is regulated at 1.90 V_{DC} for all values of i between 10 μA to 500 μA. It can be used as a voltage reference for other components, but care must be taken to ensure that current is not taken from it which could reduce the accuracy of the converter.

PRINCIPLES OF OPERATION OF BASIC VOLTAGE-TO-FREQUENCY CONVERTER (*FIGURE 1*)

The simple stand-alone V-to-F converter shown in *Figure 1* includes all the basic circuitry of *Figure 2* plus a few components for improved performance.

A resistor, $R_{IN} = 100\ k\Omega \pm 10\%$, has been added in the path to pin 7, so that the bias current at pin 7 (−80 nA typical) will cancel the effect of the bias current at pin 6 and help provide minimum frequency offset.

The resistance R_S at pin 2 is made up of a 12 kΩ fixed resistor plus a 5 kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LM131, and the tolerance of R_t, R_L and C_t.

2

Typical Applications (Continued)

For best results, all the components should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon or polypropylene are best suited.

A capacitor C_{IN} is added from pin 7 to ground to act as a filter for V_{IN}. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1 μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT}. If C_{IN} is much less than C_L, a step at V_{IN} may cause f_{OUT} to stop momentarily.

A 47Ω resistor, in series with the 1 μF C_L, is added to give hysteresis effect which helps the input comparator provide the excellent linearity (0.03% typical).

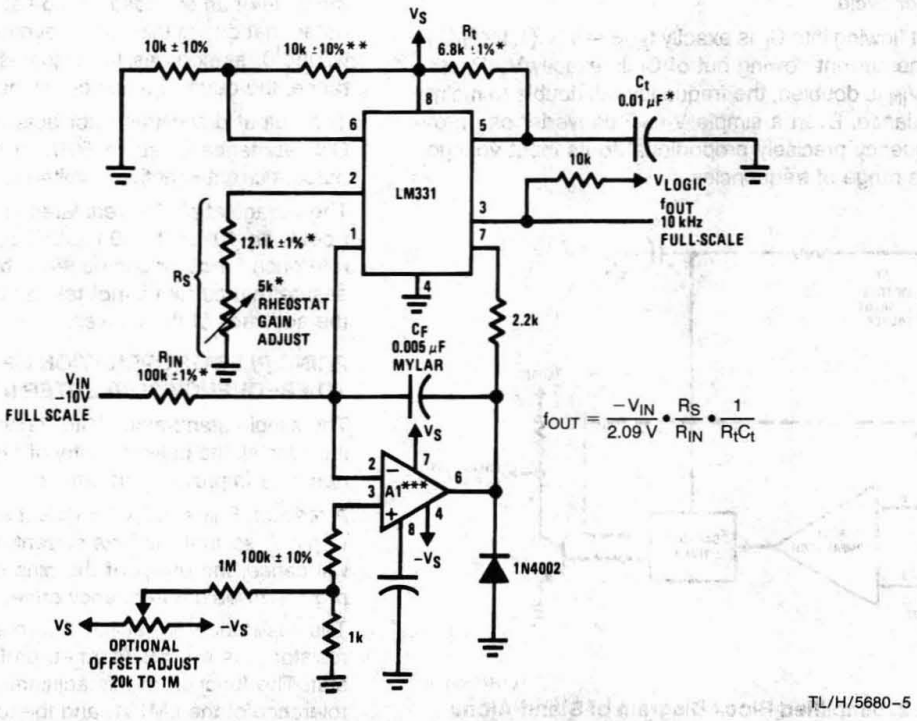
DETAIL OF OPERATION OF PRECISION V-TO-F CONVERTER (*FIGURE 3*)

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F. When the integrator's output crosses the nominal threshold level at pin 6 of the LM131, the timing cycle is initiated.

The average current fed into the op amp's summing point (pin 2) is $i \times (1.1\ R_tC_t) \times f$ which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LM131 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter; nor does the LM131 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN}, as quickly as 2 output pulses' spacing can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT}. (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of *Figure 4* operates in the same way as *Figure 3*, but with the necessary changes for high speed operation.



*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF411A

FIGURE 3. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

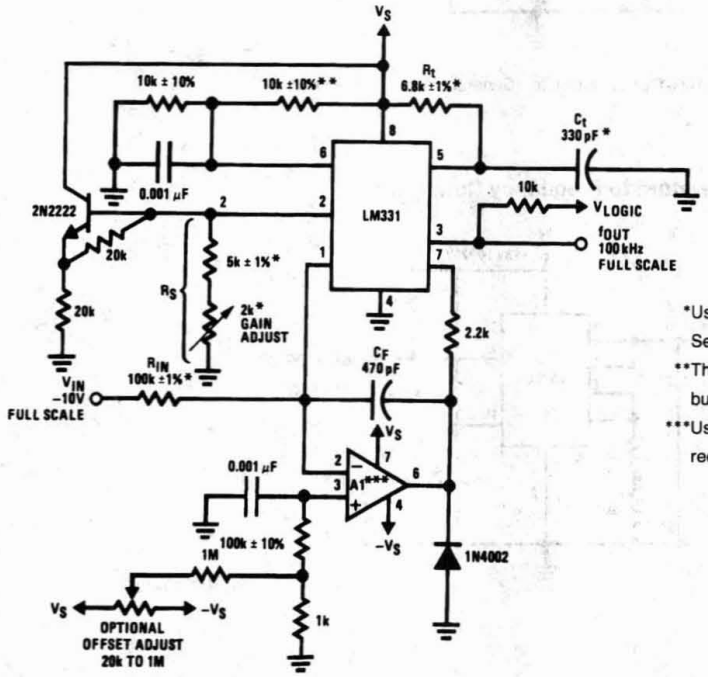
Typical Applications (Continued)

DETAILS OF OPERATION, FREQUENCY-TO-VOLTAGE CONVERTERS *(FIGURES 5 AND 6)*

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1\ R_tC_t) \times f$.

In the simple circuit of *FIGURE 5*, this current is filtered in the network $R_L = 100\ k\Omega$ and 1 μF. The ripple will be less than 10 mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5 mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in *Figure 5*. However, for input frequencies below 200 Hz, this circuit will have worse ripple than *Figure 5*. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.



*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LF411A or LF356.

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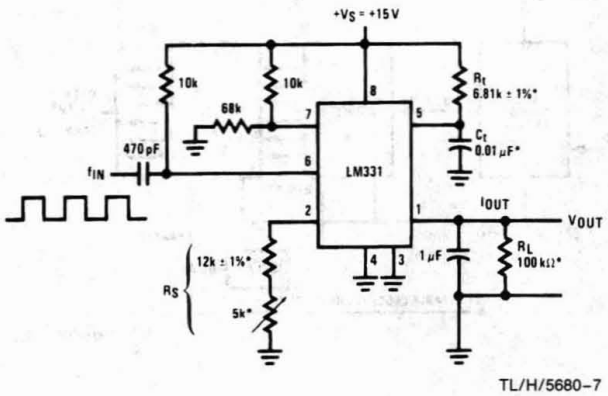
FIGURE 4. Precision Voltage-to-Frequency Converter, 100 kHz Full-Scale, ±0.03% Non-Linearity



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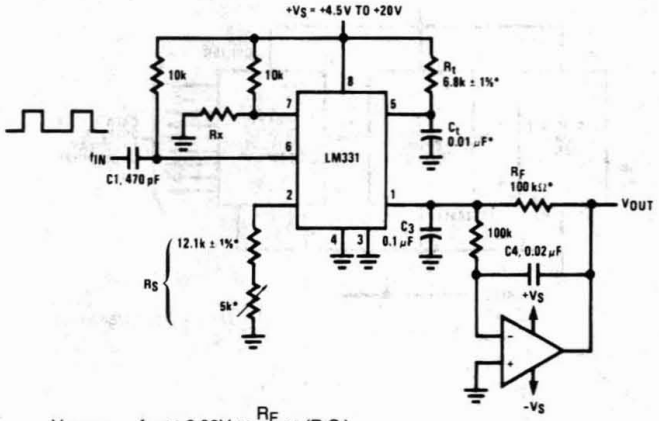
$$V_{OUT} = f_{IN} \times 2.09V \times \frac{R_L}{R_S} \times (R_tC_t)$$

*Use stable components with low temperature coefficients.

FIGURE 5. Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity



$$V_{OUT} = -f_{IN} \times 2.09V \times \frac{R_F}{R_S} \times (R_tC_t)$$

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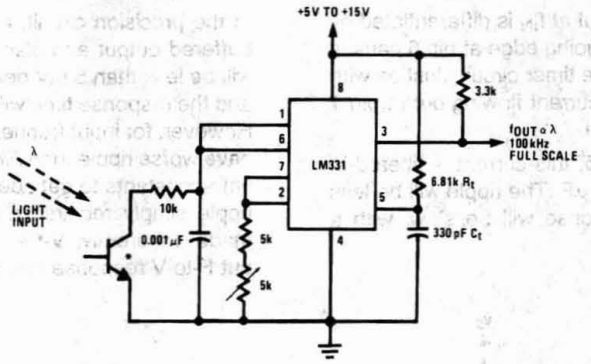
$$\text{SELECT } Rx = \frac{(V_S - 2V)}{0.2\ mA}$$

*Use stable components with low temperature coefficients.

FIGURE 6. Precision Frequency-to-Voltage Converter, 10 kHz Full-Scale with 2-Pole Filter, ±0.01% Non-Linearity Maximum

Typical Applications (Continued)

Light Intensity to Frequency Converter



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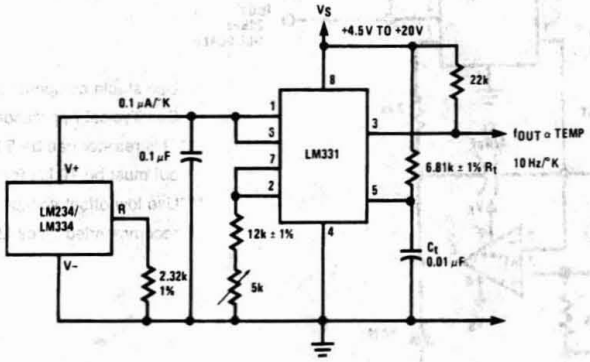
*L14F-1, L14G-1 or L14H-1, photo transistor (General Electric Co.) or similar

Temperature to Frequency Converter



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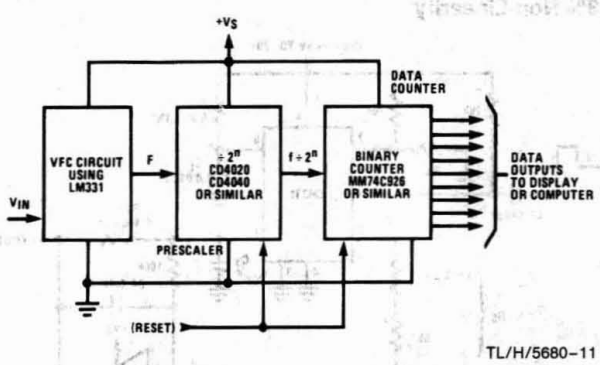
Long-Term Digital Integrator Using VFC



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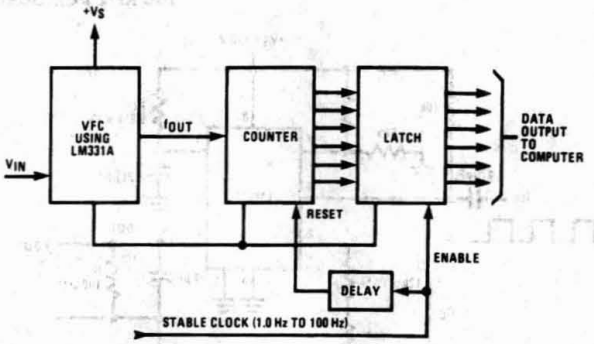
Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter



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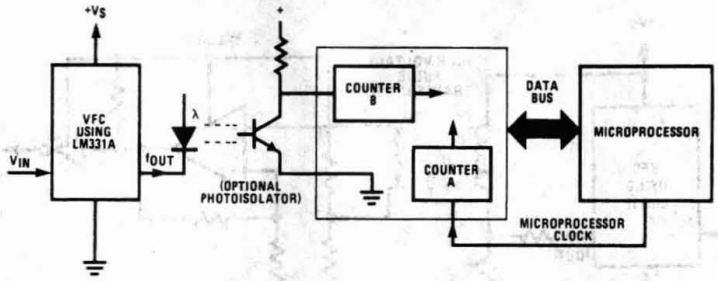
Typical Applications (Continued)

Analog-to-Digital Converter with Microprocessor



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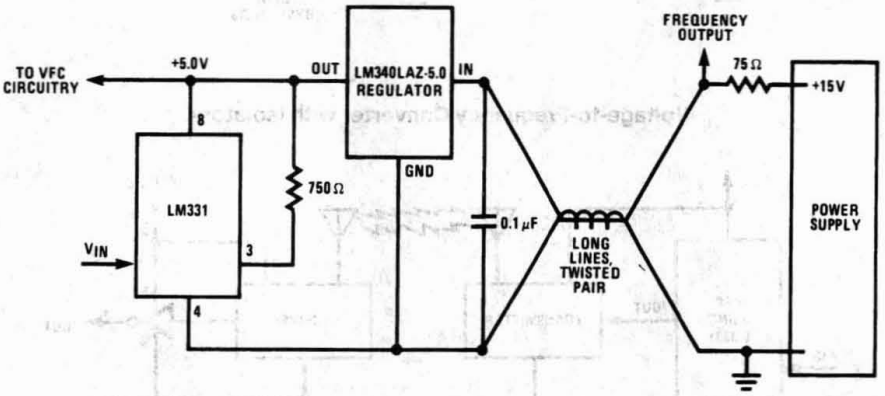
Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver



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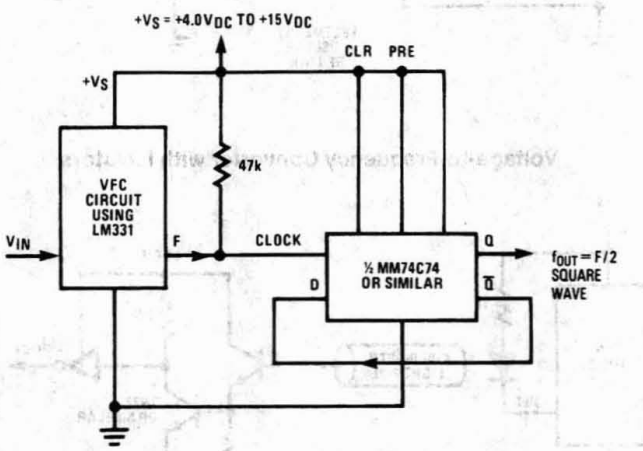
Voltage-to-Frequency Converter with Square-Wave Output Using ÷ 2 Flip-Flop



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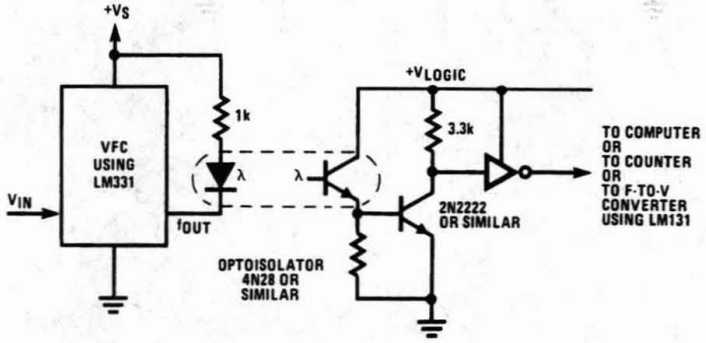
Voltage-to-Frequency Converter with Isolators



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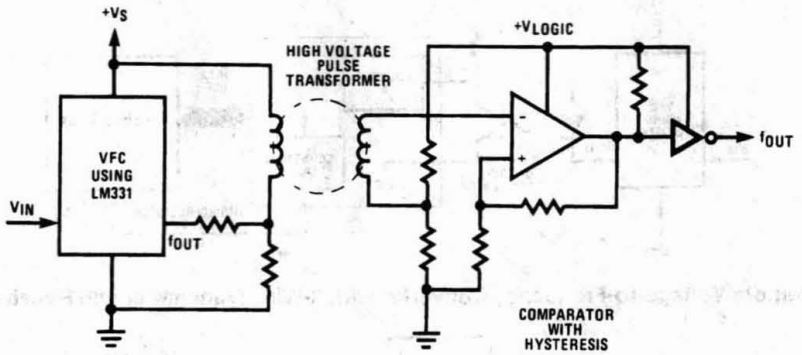
Typical Applications (Continued)

Voltage-to-Frequency Converter with Isolators



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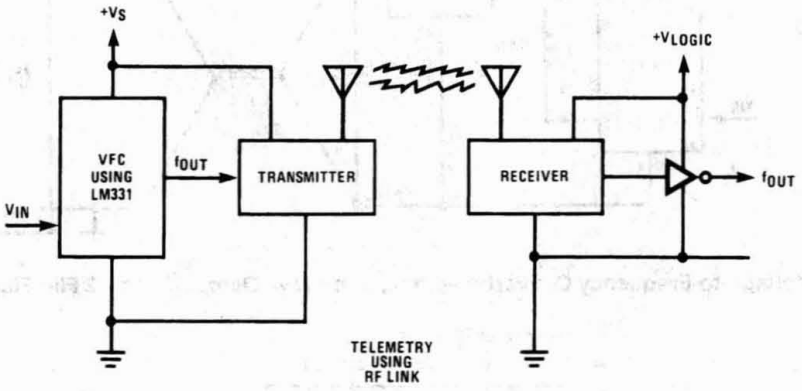
Voltage-to-Frequency Converter with Isolators



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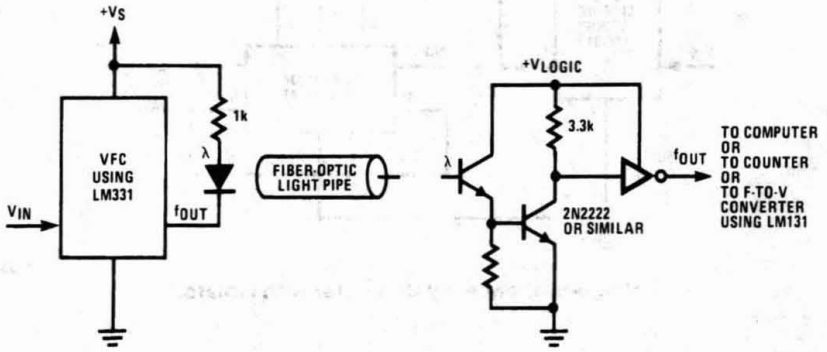
Voltage-to-Frequency Converter with Isolators



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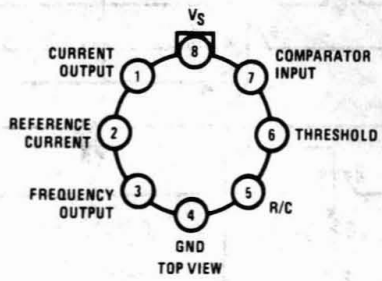
Connection Diagrams

Metal Can Package



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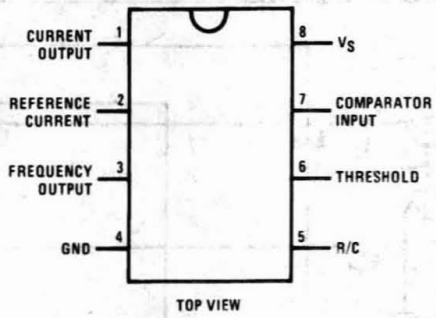
Note: Metal case is connected to pin 4 (GND.)

Order Number LM131H/883 or LM131AH/883
See NS Package Number H08C

Dual-In-Line Package



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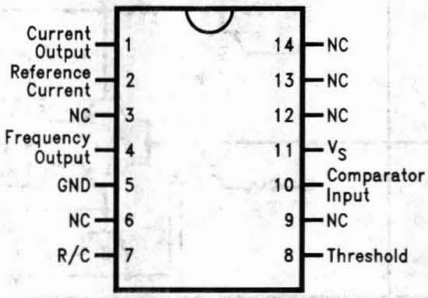
Order Number LM231AN, LM231N, LM331AN, or LM331N
See NS Package Number N08E

Small-Outline Package



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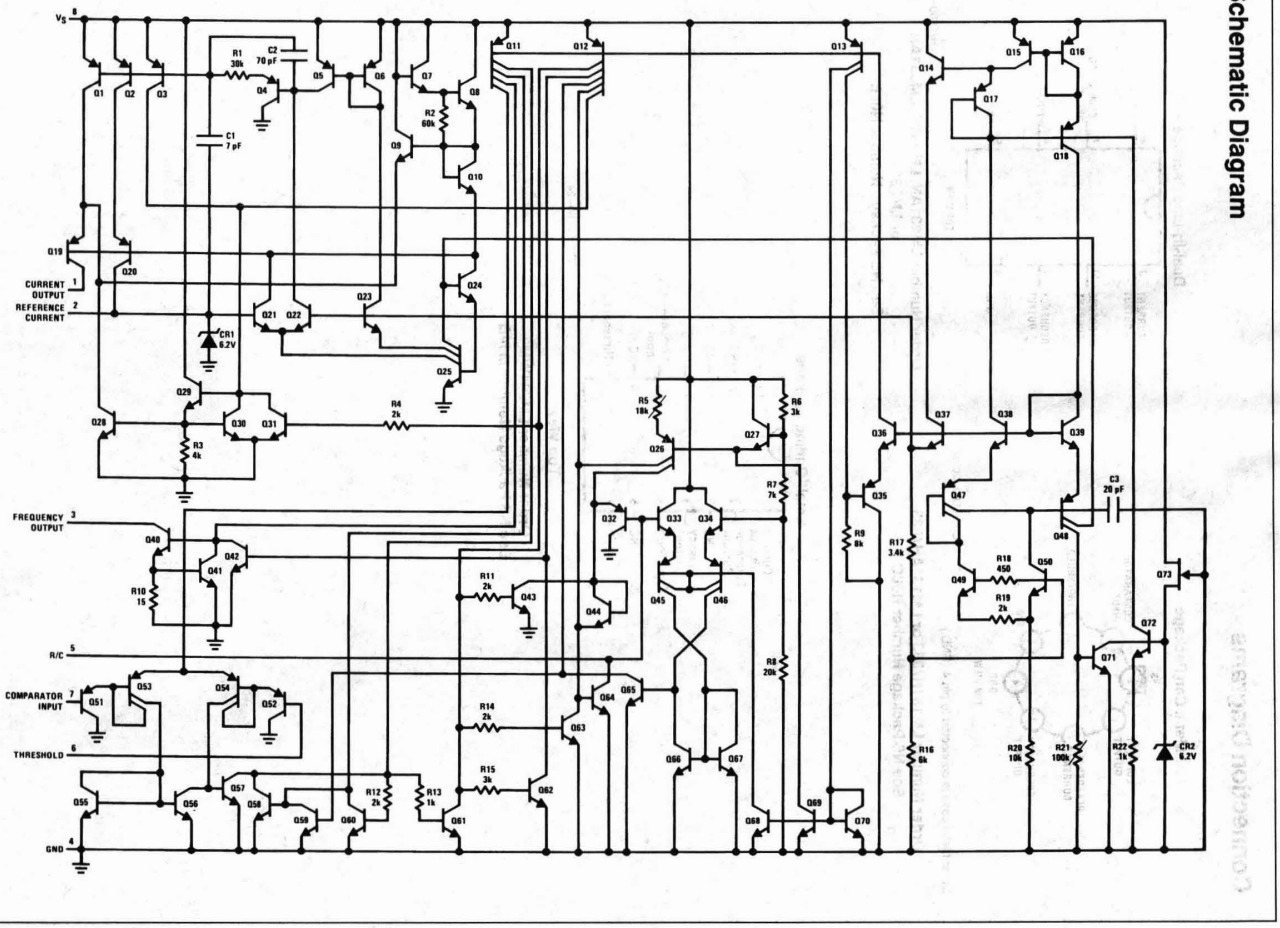
Top View

Order Number LM231WM
See NS Package Number M14B

Schematic Diagram



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Section 3
Digital-to-Analog Converters

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Definition of Terms
D/A Converters

Differential Nonlinearity: Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC.

Gain Error (Full Scale Error): The difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

LSB (Least-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Monotonicity: A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Multiplying DAC: In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by 2^n (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity, four quadrant multiplication exists.

Offset Error (Zero Error): The output voltage that exists when the input digital code is set to give an ideal output of zero volts. All the digital codes in the transfer curve are offset by the same value. Offset error is usually expressed in LSBs.

Power Supply Rejection (Power Supply Sensitivity): The sensitivity of a converter to changes in the dc power supply voltages.

Resolution: The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to 2^n.

Settling Time: The time from a change in input code until a DAC's output signal remains within ± ½ LSB (or some other specified tolerance) of the final value.

National Semiconductor

D/A Converter Selection Guide

Part No.	Resolution (Bits)	Linearity @ 25°C % (Max)	Settling Time (+½ LSB)	Supplies (V)	Temperature Range*			Package	Comments
					M	I	C		
ADC0852	8	0.19		5		•	•	8-Pin DIP	DAC, Comparator, Serial Input
ADC0854	8	0.19		5		•	•	14-Pin DIP	DAC, Comparator, Serial Input
DAC0800	8	0.19	100 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0801	8	0.39	100 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0802	8	0.10	100 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0806	8	0.78	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0807	8	0.39	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0808	8	0.19	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0830	8	0.05	1 μs	5 to 15		•	•	20-Pin DIP 20-Pin S.O. 20-Pin PCC	μP Compatible 4-Quadrant Multiplying
DAC0831	8	0.10	1 μs	5 to 15			•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0832	8	0.20	1 μs	5 to 15		•	•	20-Pin DIP 20-Pin S.O. 20-Pin PCC	μP Compatible 4-Quadrant Multiplying
DAC0854	8	0.19	2.7 μs	5	•	•		20-Pin DIP 20-Pin S.O.	Quad Serial DAC with Readback
DAC0890	8	0.19	2.7 μs	5 to 15		•		20-Pin DIP	Dual Voltage Output DAC
DAC1001	10	0.1	500 ns	5 to 15			•	24-Pin DIP	μP Compatible Double Buffered
DAC1002	10	0.2	500 ns	5 to 15			•	24-Pin DIP	μP Compatible Double Buffered
DAC1006	10	0.05	500 ns	5 to 15			•	20-Pin DIP	μP Compatible Double Buffered
DAC1007	10	0.1	500 ns	5 to 15			•	20-Pin DIP	μP Compatible Double Buffered
DAC1008	10	0.2	500 ns	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered

D/A Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Linearity @ 25°C % (Max)	Settling Time (+½ LSB)	Supplies (V)	Temperature Range*			Package	Comments
					M	I	C		
DAC1020	10	0.05	500 ns	5 to 15		•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1021	10	0.1	500 ns	5 to 15		•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1022	10	0.2	500 ns	5 to 15		•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1054	10	0.02	3.7 μs	5	•	•		24-Pin DIP 24-Pin SO	Quad Serial DAC with Readback
DAC1208	12	0.018	1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1209	12	0.024	1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1210	12	0.05	1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1218	12	0.012	1 μs	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1219	12	0.024	1 μs	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1220	12	0.05	500 ns	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1222	12	0.2	500 ns	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1230	12	0.018	1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1231	12	0.024	1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1232	12	0.05	1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying

*Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" 0°C to +70°C.

National Semiconductor

DAC0800/DAC0801/DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current — 100 ns
- Full scale error — ±1 LSB
- Nonlinearity over temperature — ±0.1%
- Full scale current drift — ±10 ppm/°C
- High output compliance — −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW at ±5V
- Low cost

Typical Applications

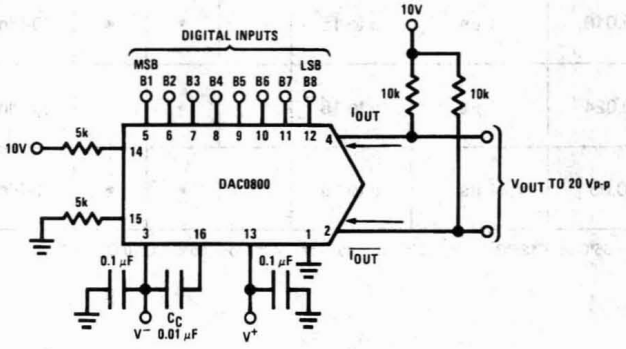

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FIGURE 1. ±20 V_{p-p} Output Digital-to-Analog Converter (Note 4)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A)*		N Package (N16A)*		SO Package (M16A)
±0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM
±0.39% FS	0°C ≤ T_A ≤ +70°C			DAC0801LCN	DAC-08CP	DAC0801LCM

*Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 2)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs ($V_S^- = -15V$)	4.25 mA
ESD Susceptibility (Note 3)	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Note 1)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0801LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19			±0.39	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", $T_A = 25°C$		100	135					100	150	ns
		DAC0800L					100	135				ns
		DAC0800LC					100	150				ns
tPLH, tPHL	Propagation Delay	$T_A = 25°C$										
	Each Bit			35	60		35	60		35	60	ns
	All Bits Switched			35	60		35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50		±10	±80	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, $R_{OUT} > 20$ MΩ Typ	−10		18	−10		18	−10		18	V
I_{FS4}	Full Scale Current	$V_{REF} = 10.000V$, R14 = 5.000 kΩ R15 = 5.000 kΩ, $T_A = 25°C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±1	±8.0		±2	±16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	$V^- = -5V$	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		$V^- = -8V$ to $-18V$	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels											
V_{IL}	Logic "0"	$V_{LC} = 0V$			0.8			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			2.0			V
	Logic Input Current	$V_{LC} = 0V$										
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	$V^- = -15V$	−10		18	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	$V_S = \pm 15V$	−10		13.5	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	*(Figure 12)*	4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \le V+ \le 18V$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \le V^- \le 18V$ $I_{REF} = 1mA$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
	Power Supply Current	$V_S = \pm 5V$, $I_{REF} = 1$ mA										
I+				2.3	3.8		2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
		$V_S = 5V, -15V$, $I_{REF} = 2$ mA										
I+				2.4	3.8		2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
		$V_S = \pm 15V$, $I_{REF} = 2$ mA										
I+				2.5	3.8		2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA

3

Electrical Characteristics (Continued)

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
P_D	Power Dissipation	$\pm 5V$, $I_{REF} = 1$ mA		33	48		33	48		33	48	mW
		$5V, -15V$, $I_{REF} = 2$ mA		108	136		108	136		108	136	mW
		$\pm 15V$, $I_{REF} = 2$ mA		135	174		135	174		135	174	mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

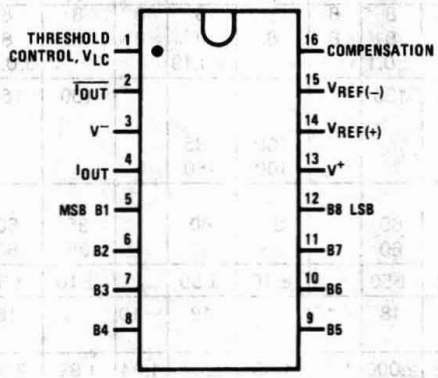
Note 2: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 4: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

Connection Diagrams

Dual-In-Line Package



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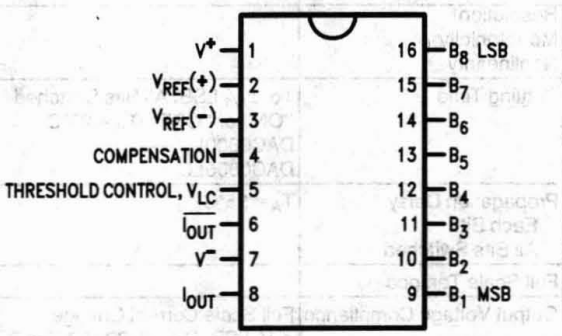
Top View

See Ordering Information

Small Outline Package



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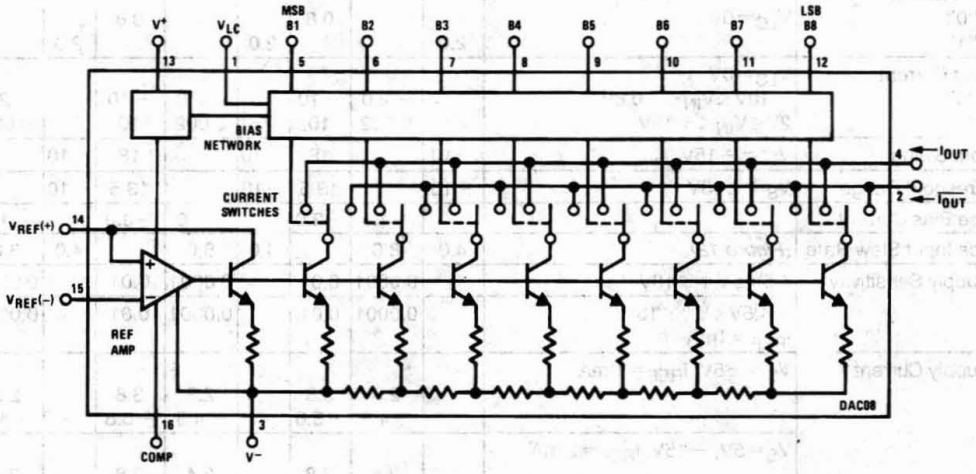
Top View

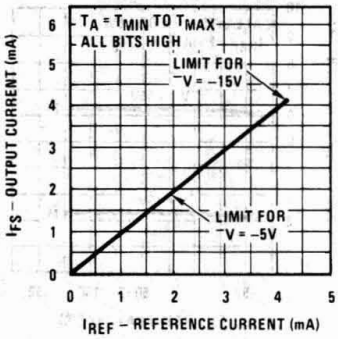
Block Diagram (Note 4)



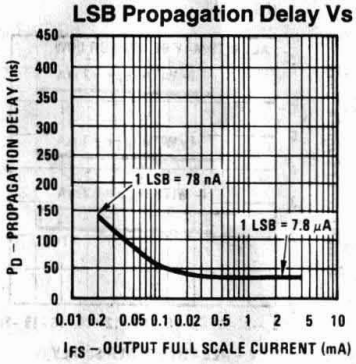
TL/H/5686–2

Typical Performance Characteristics

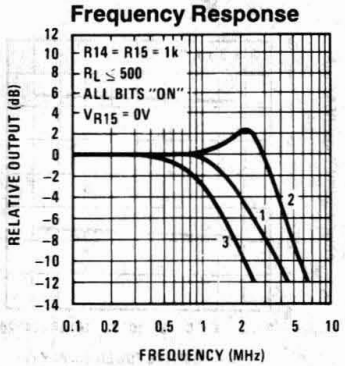
Full Scale Current vs Reference Current



LSB Propagation Delay Vs I_{FS}



Reference Input Frequency Response

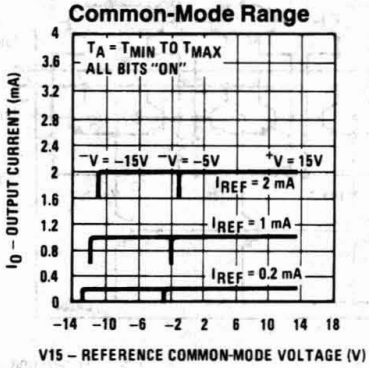


Curve 1: $C_C = 15$ pF, $V_{IN} = 2$ Vp-p centered at 1V.

Curve 2: $C_C = 15$ pF, $V_{IN} = 50$ mVp-p centered at 200 mV.

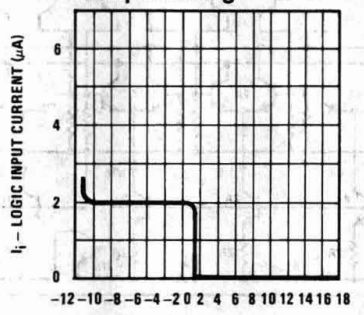
Curve 3: $C_C = 0$ pF, $V_{IN} = 100$ mVp-p at 0V and applied through 50 Ω connected to pin 14.2V applied to R14.

Reference Amp Common-Mode Range

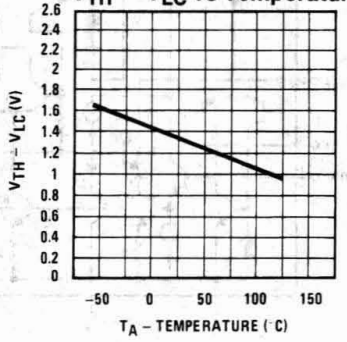

$T_A = T_{MIN}$ TO T_{MAX}
ALL BITS "ON"
$^-V = -15V$ $^-V = -5V$ $^+V = 15V$
$I_{REF} = 2$ mA
$I_{REF} = 1$ mA
$I_{REF} = 0.2$ mA
I_O – OUTPUT CURRENT (mA)
V15 – REFERENCE COMMON-MODE VOLTAGE (V)

Note. Positive common-mode range is always (V+) − 1.5V

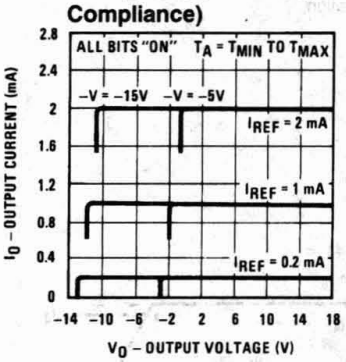
Logic Input Current vs Input Voltage



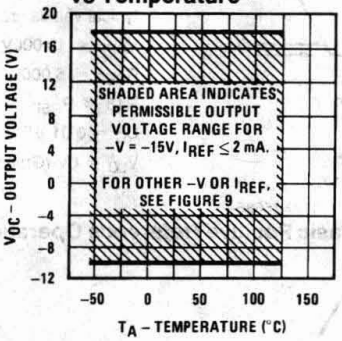
$V_{TH} - V_{LC}$ vs Temperature



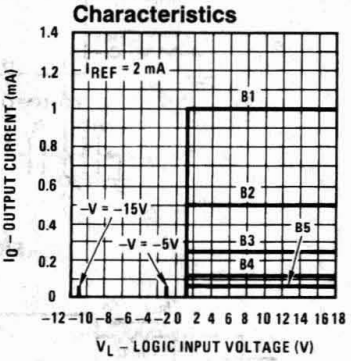
Output Current vs Output Voltage (Output Voltage Compliance)



Output Voltage Compliance vs Temperature


SHADED AREA INDICATES PERMISSIBLE OUTPUT VOLTAGE RANGE FOR $-V = -15V$, $I_{REF} \leq 2$ mA.
FOR OTHER $-V$ OR I_{REF}, SEE FIGURE 9
V_{OC} – OUTPUT VOLTAGE (V)
T_A – TEMPERATURE (°C)

Bit Transfer Characteristics



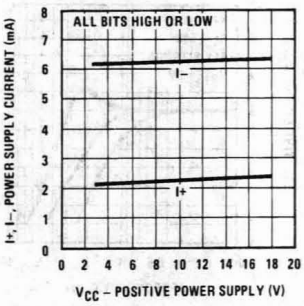
TL/H/5686–3

Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

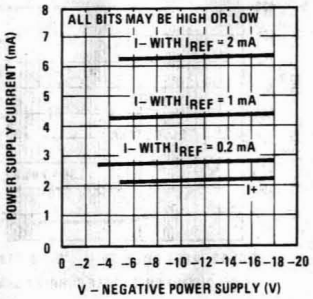
3

Typical Performance Characteristics (Continued)

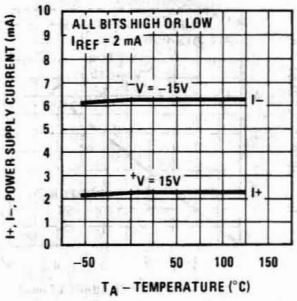
Power Supply Current vs +V



Power Supply Current vs −V

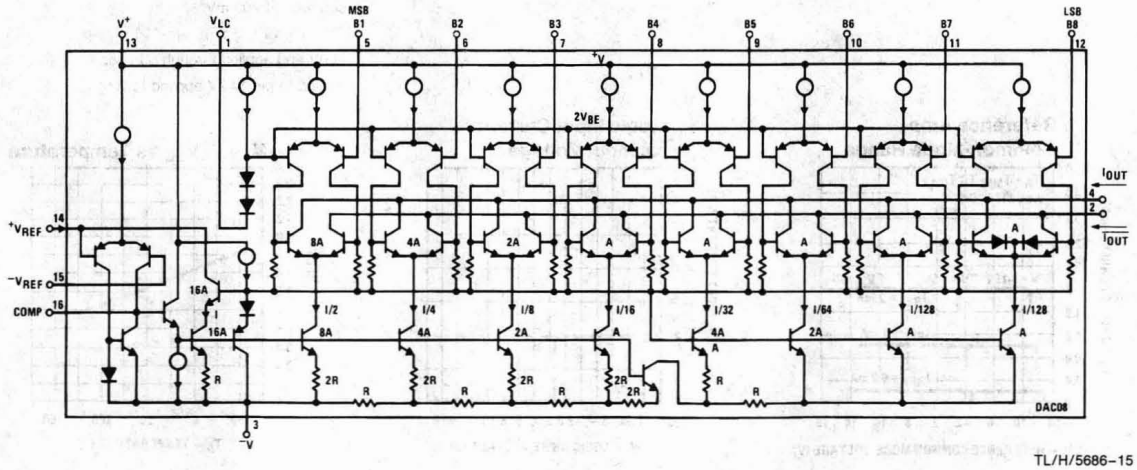

ALL BITS MAY BE HIGH OR LOW
I– WITH IREF = 2 mA
I– WITH IREF = 1 mA
I– WITH IREF = 0.2 mA
I+
POWER SUPPLY CURRENT (mA)
0 –2 –4 –6 –8 –10 –12 –14 –16 –18 –20
V – NEGATIVE POWER SUPPLY (V)

Power Supply Current vs Temperature



TL/H/5686–4

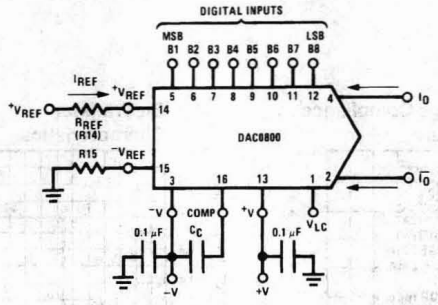
Equivalent Circuit



TL/H/5686–15

FIGURE 2

Typical Applications (Continued)



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$

$R_{REF} = 5.000k$

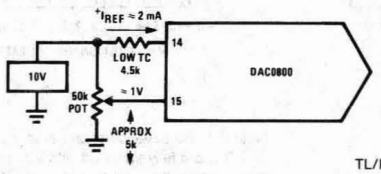
$R15 \approx R_{REF}$

$C_C = 0.01\ \mu F$

$V_{LC} = 0V$ (Ground)

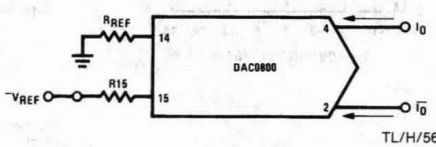
TL/H/5686–5

FIGURE 3. Basic Positive Reference Operation (Note 4)



TL/H/5686–21

FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 4)



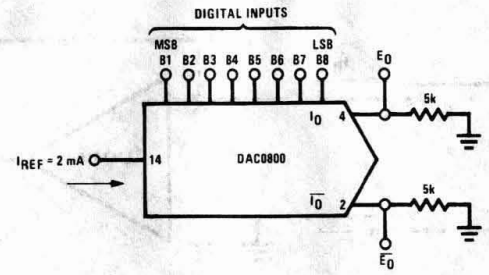
TL/H/5686–16

$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

FIGURE 5. Basic Negative Reference Operation (Note 4)

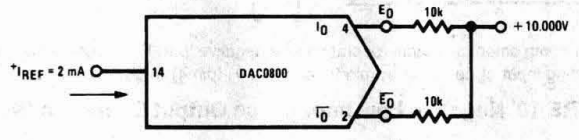
Typical Applications (Continued)



TL/H/5686-17

	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

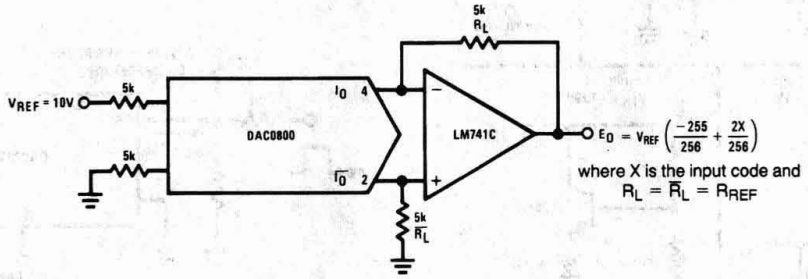
FIGURE 6. Basic Unipolar Negative Operation (Note 4)



TL/H/5686-6

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

FIGURE 7. Basic Bipolar Output Operation (Note 4)



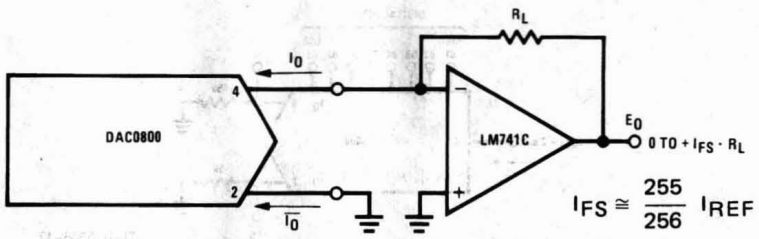
TL/H/5686-18

If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−)Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	−9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.960

FIGURE 8. Symmetrical Offset Binary Operation (Note 4)

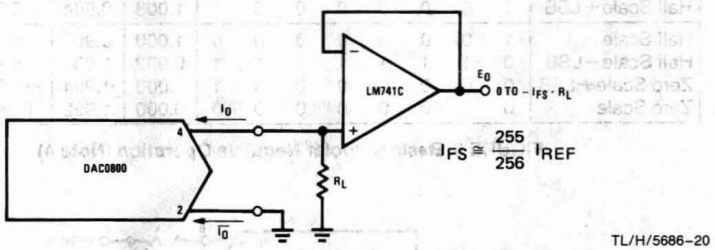
Typical Applications (Continued)



TL/H/5686–19

For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

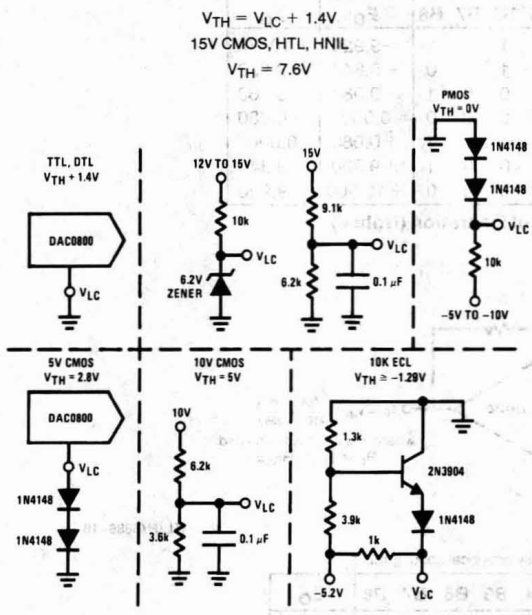
FIGURE 9. Positive Low Impedance Output Operation (Note 4)



TL/H/5686–20

For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

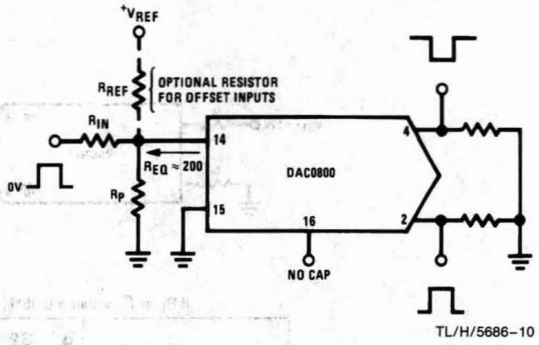
FIGURE 10. Negative Low Impedance Output Operation (Note 4)



TL/H/5686–9

Note. Do not exceed negative logic input range of DAC.

FIGURE 11. Interfacing with Various Logic Families



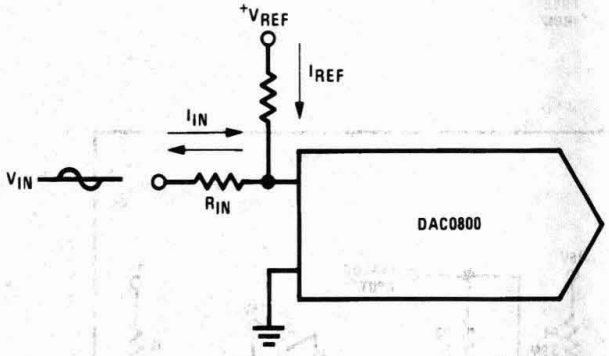
TL/H/5686–10

Typical values: $R_{IN} = 5k, +V_{IN} = 10V$

FIGURE 12. Pulsed Reference Operation (Note 4)

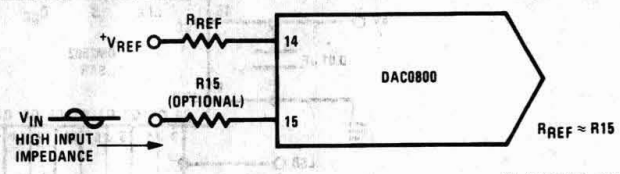
Typical Applications (Continued)

(a) $I_{REF} \geq$ peak negative swing of I_{IN}



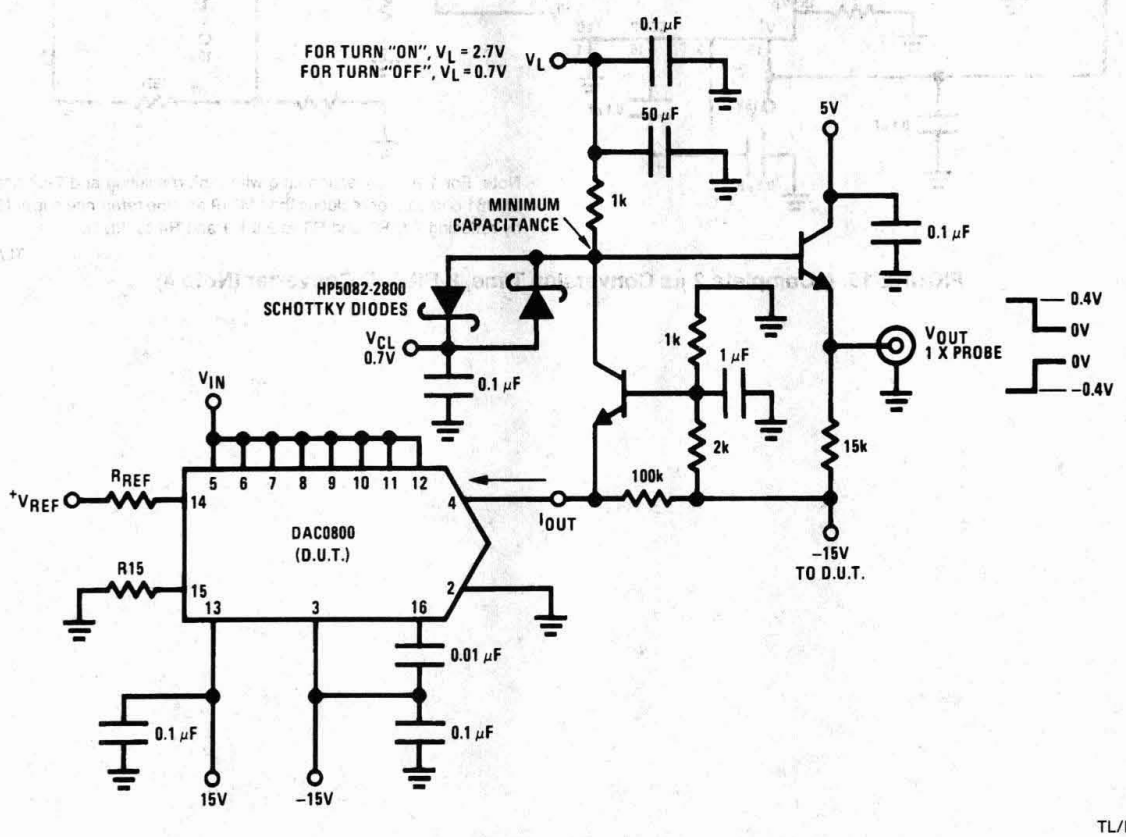
TL/H/5686–11

(b) $+V_{REF}$ must be above peak positive swing of V_{IN}



TL/H/5686–12

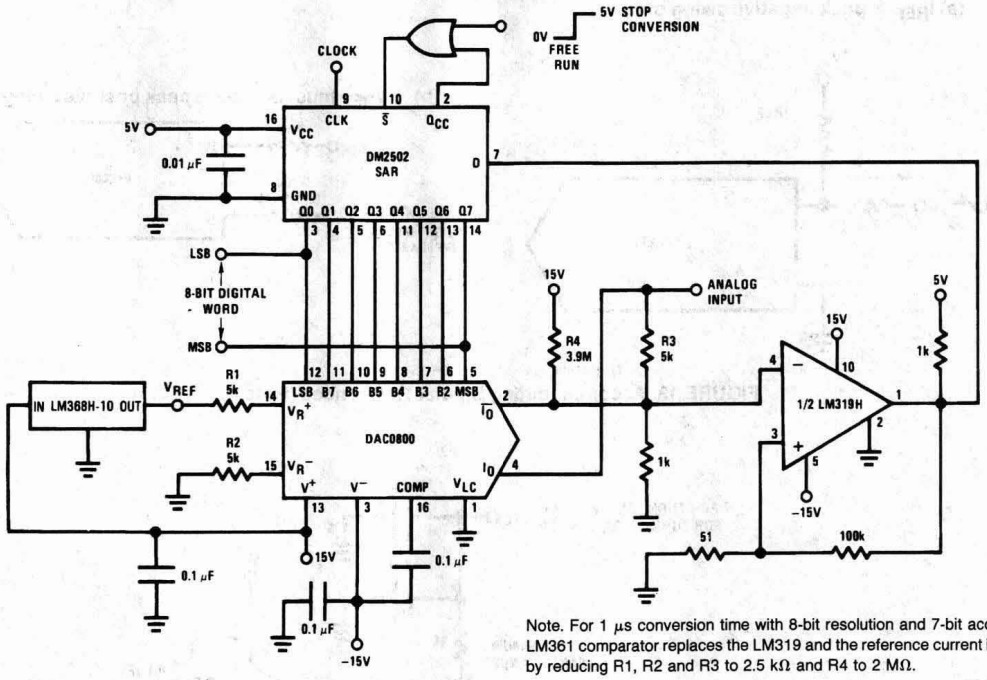
FIGURE 13. Accommodating Bipolar References (Note 4)



TL/H/5686–7

FIGURE 14. Settling Time Measurement (Note 4)

Typical Applications (Continued)



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

TL/H/5686–8

FIGURE 15. A Complete 2 μs Conversion Time, 8-Bit A/D Converter (Note 4)

National Semiconductor

DAC0808/DAC0807/DAC0806 8-Bit D/A Converters

General Description

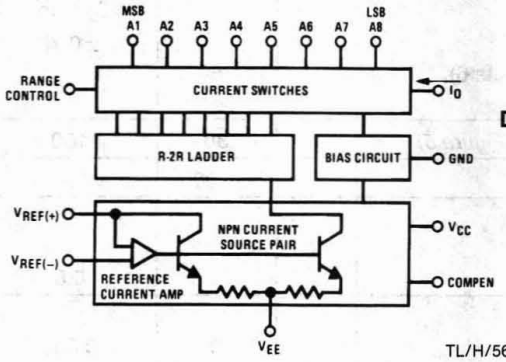
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/ 256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

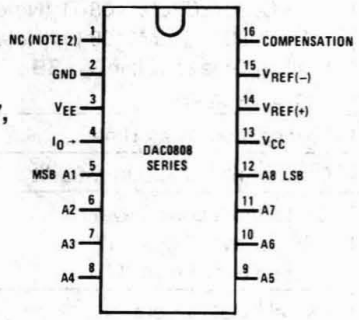
Block and Connection Diagrams



TL/H/5687–1

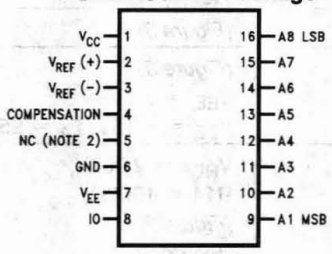
Order Number DAC0808, DAC0807, or DAC0806 See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/H/5687–2

Small-Outline Package



TL/H/5687–13

Top View

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS				
		J PACKAGE (J16A)*		N PACKAGE (N16A)*		SO PACKAGE (M16A)
7-bit	$0°C \leq T_A \leq +75°C$	DAC0807LCJ	MC1408L7	DAC0808LCN DAC0807LCN	MC1408P8 MC1408P7	DAC0808LCM DAC0807LCM
6-bit	$0°C \leq T_A \leq +75°C$	DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6	DAC0806LCM

***Note.** Devices may be ordered by using either order number.

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	$+18\ V_{DC}$
V_{EE}	$-18\ V_{DC}$
Digital Input Voltage, V5–V12	$-10\ V_{DC}$ to $+18\ V_{DC}$
Applied Output Voltage, V_O	$-11\ V_{DC}$ to $+18\ V_{DC}$
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 3)	1000 mW
ESD Susceptibility (Note 4)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808LC Series	$0 \le T_A \le +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808LC (LM1408-8)				**±0.19**	%
	DAC0807LC (LM1408-7), (Note 5)				±0.39	%
	DAC0806LC (LM1408-6), (Note 5)				±0.78	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A = 25°C (Note 6), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω,				
		(Figure 3)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance (Note 2)	$E_r \le 0.19\%$, T_A = 25°C				
	V_{EE} = −5V, I_{REF} = 1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maixmum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: All current switches are tested to guarantee at least 50% of rated current.

Note 6: All bits switched.

Note 7: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application

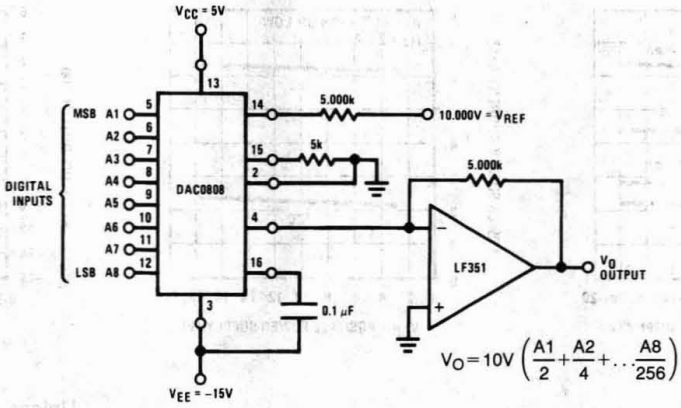


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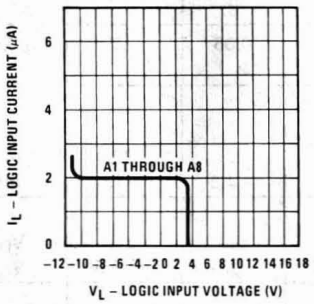
FIGURE 1. + 10V Output Digital to Analog Converter (Note 7)

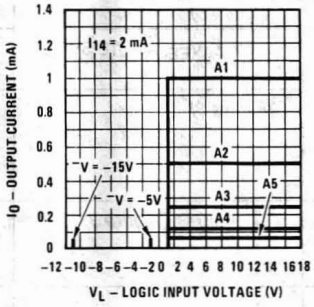
Typical Performance Characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

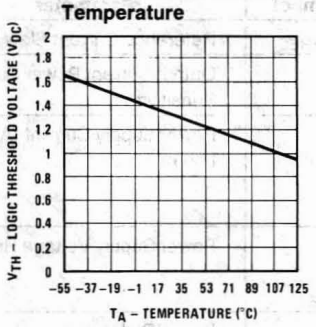
Logic Input Current vs Input Voltage



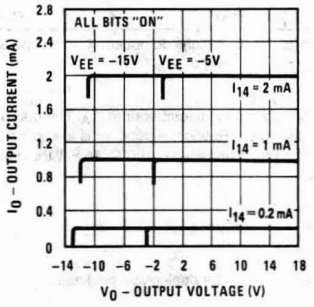
Bit Transfer Characteristics



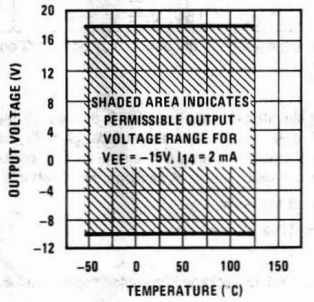
Logic Threshold Voltage vs Temperature



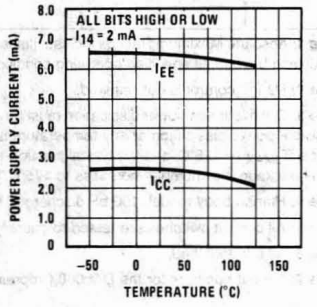
Output Current vs Output Voltage (Output Voltage Compliance)



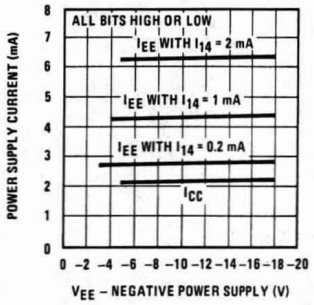
Output Voltage Compliance vs Temperature



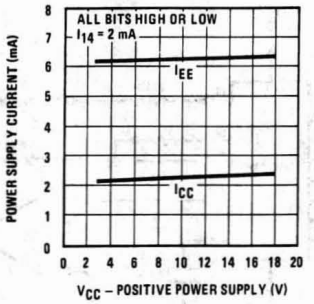
Typical Power Supply Current vs Temperature



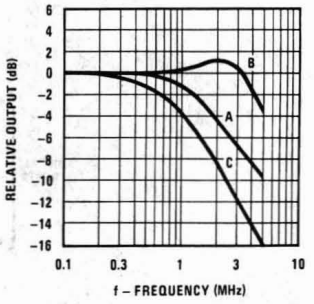
Typical Power Supply Current vs V_{EE}


ALL BITS HIGH OR LOW
I_{EE} WITH I_{14} = 2 mA
I_{EE} WITH I_{14} = 1 mA
I_{EE} WITH I_{14} = 0.2 mA
I_{CC}
POWER SUPPLY CURRENT (mA)
V_{EE} – NEGATIVE POWER SUPPLY (V)

Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



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Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

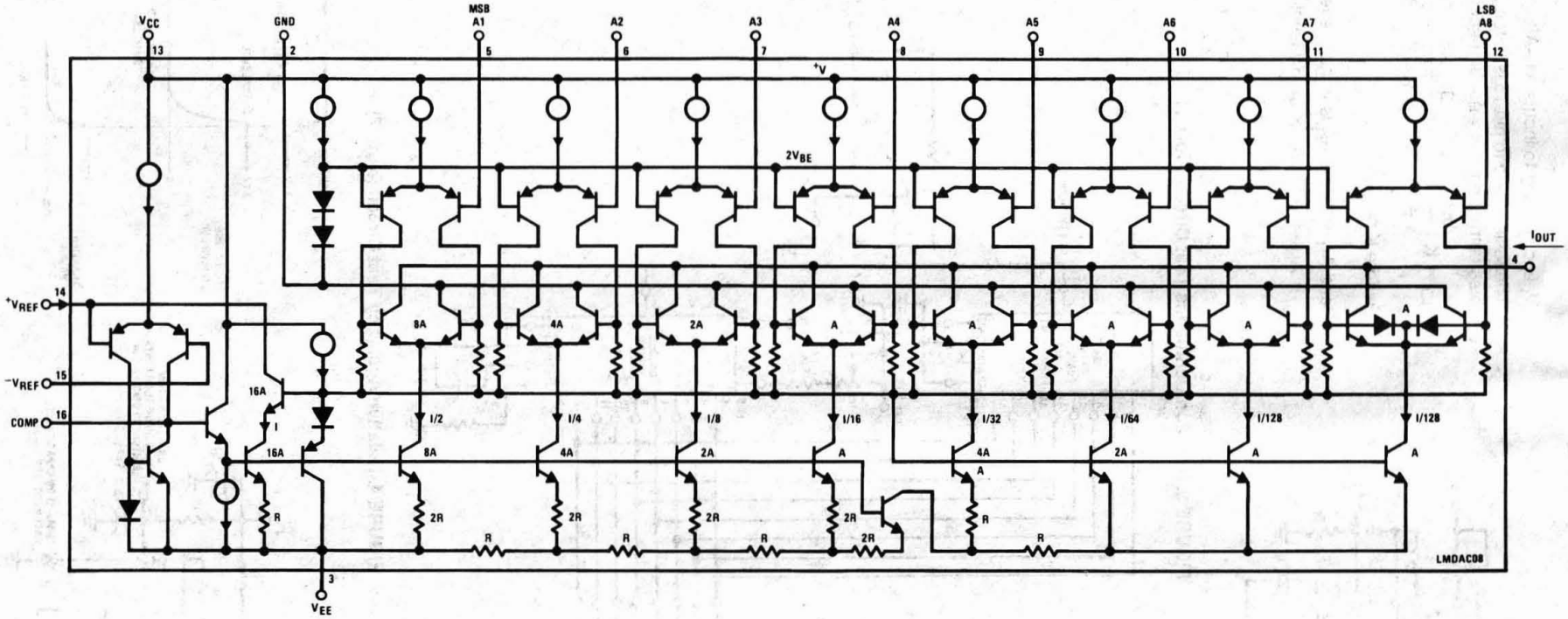
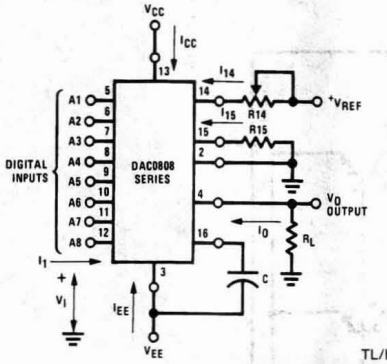


FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 7)

Test Circuits



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V_I and I_1 apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 7)

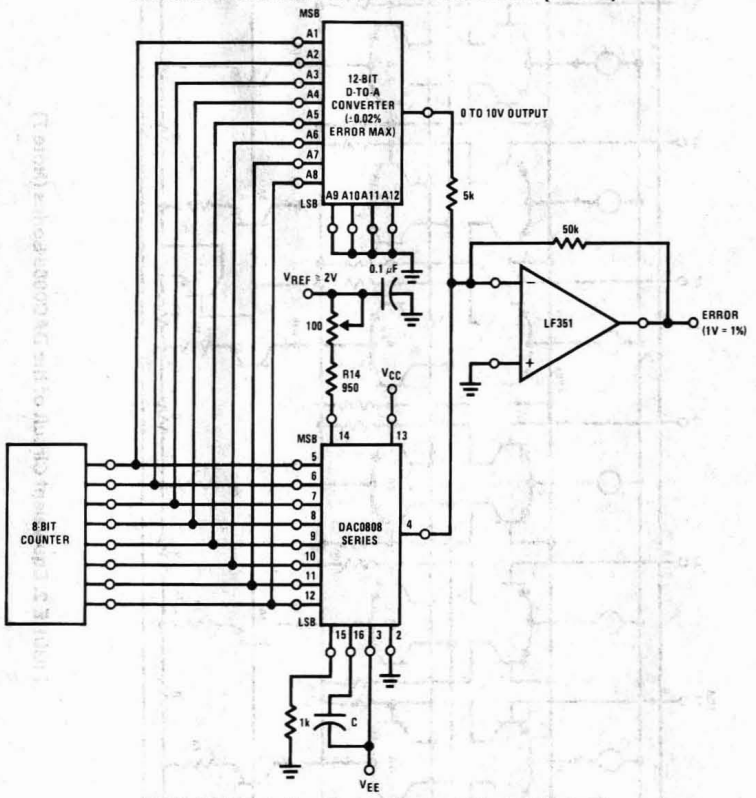

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FIGURE 4. Relative Accuracy Test Circuit (Note 7)

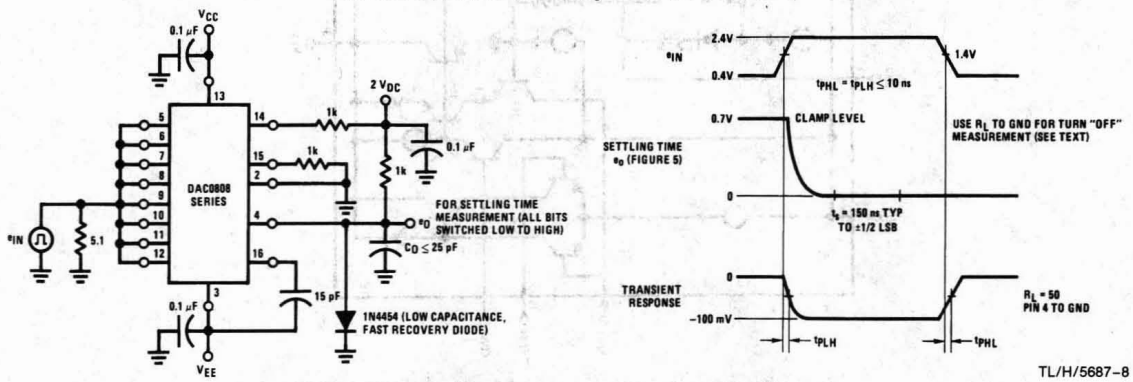

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FIGURE 5. Transient Response and Settling Time (Note 7)

Test Circuits (Continued)

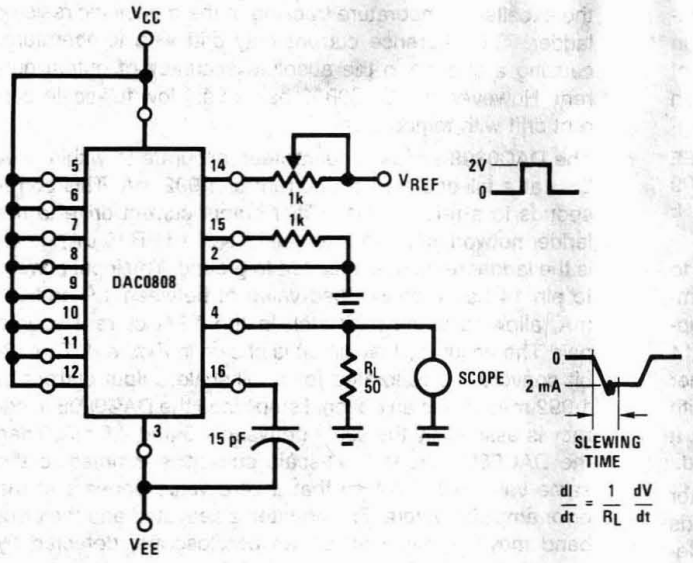

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FIGURE 6. Reference Current Slew Rate Measurement (Note 7)

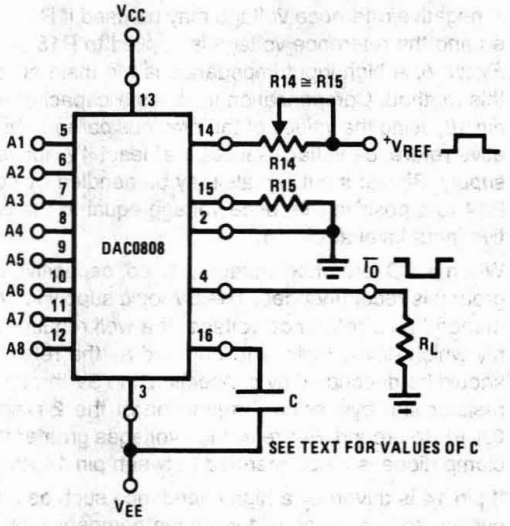

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FIGURE 7. Positive V_{REF} (Note 7)

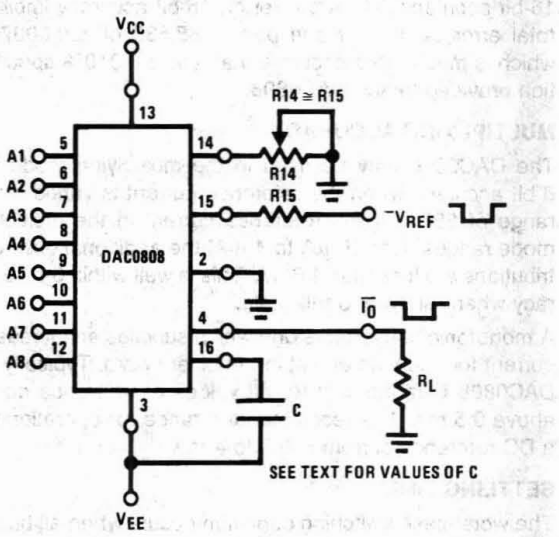

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FIGURE 8. Negative V_{REF} (Note 7)

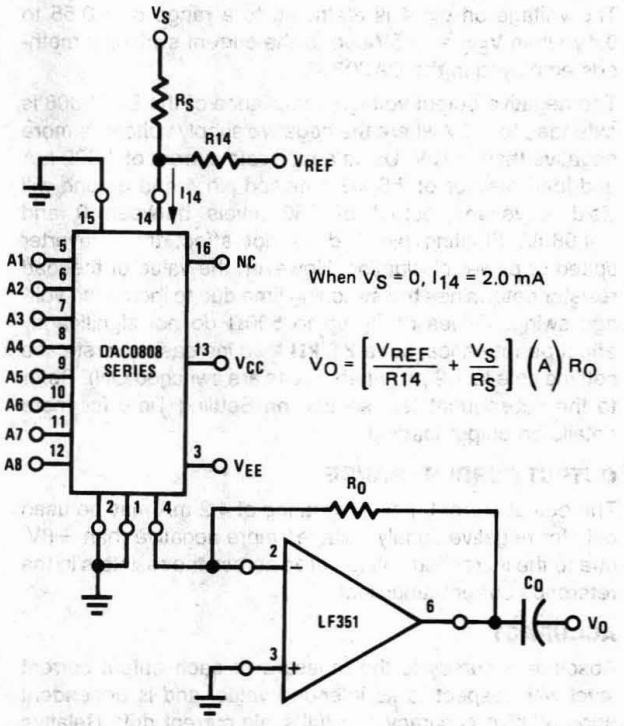

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FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 7)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input currrent, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

Application Hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of -0.55 to 0.4V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to $-5V$ where the negative supply voltage is more negative than $-10V$. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and $-4.980V$. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than $-8V$, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within $\pm\frac{1}{2}$ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of $\pm\frac{1}{2}$ of one part in 65,536 or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.019\%$ specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within $\pm\frac{1}{2}$ LSB, for 8-bit accuracy, and 100 ns to $\frac{1}{2}$ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

DAC0830/DAC0831/DAC0832 8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

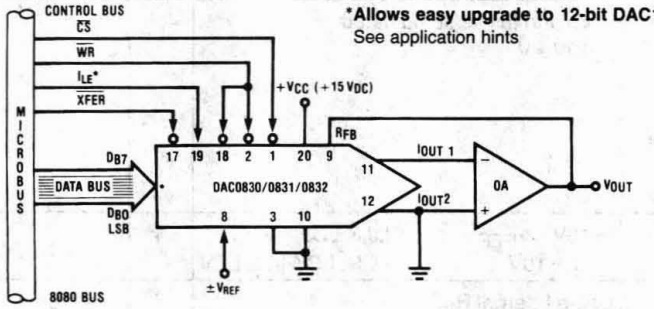
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired
- Available in 20-pin small-outline or molded chip carrier package

Key Specifications

■ Current settling time	1 μs
■ Resolution	8 bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application

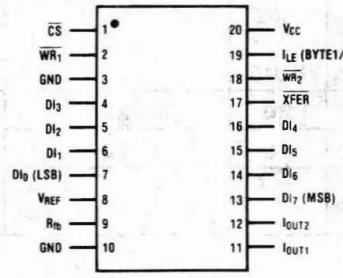


***Allows easy upgrade to 12-bit DAC1230,** See application hints

TL/H/5608–1

Connection Diagrams (Top Views)

Dual-In-Line and Small-Outline Packages



†This is necessary for the 12-bit DAC1230 series to permit interchanging from an 8-bit to a 12-bit DAC with **No PC board changes** and no software changes, See applications section.

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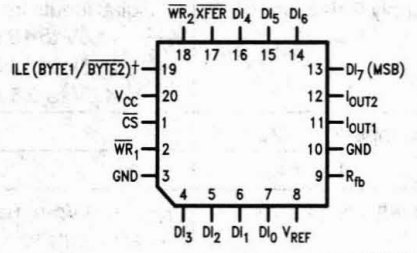
Molded Chip Carrier Package



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability (Note 14)	800V
Lead Temperature (soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Part numbers with 'LCN' suffix	0°C to +70°C
Part numbers with 'LCWM' suffix	0°C to +70°C
Part numbers with 'LCV' suffix	0°C to +70°C
Part numbers with 'LCJ' suffix	−40°C to +85°C
Part numbers with 'LJ' suffix	−55°C to +125°C
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

$V_{REF} = 10.000\ V_{DC}$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	$V_{CC} = 4.75\ V_{DC}$ $V_{CC} = 15.75\ V_{DC}$		$V_{CC} = 5\ V_{DC} \pm 5\%$ $V_{CC} = 12\ V_{DC} \pm 5\%$ to $15\ V_{DC} \pm 5\%$	Limit Units
			Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER CHARACTERISTICS						
Resolution			8	8	**8**	bits
Linearity Error Max	Zero and full scale adjusted $-10V \le V_{REF} \le +10V$	4, 8				
DAC0830LJ & LCJ				**0.05**	**0.05**	% FSR
DAC0832LJ & LCJ				**0.2**	**0.2**	% FSR
DAC0830LCN, LCWM & LCV				0.05	**0.05**	% FSR
DAC0831LCN				0.1	**0.1**	% FSR
DAC0832LCN, LCWM & LCV				0.2	**0.2**	% FSR
Differential Nonlinearity Max	Zero and full scale adjusted $-10V \le V_{REF} \le +10V$	4, 8				
DAC0830LJ & LCJ				**0.1**	**0.1**	% FSR
DAC0832LJ & LCJ				**0.4**	**0.4**	% FSR
DAC0830LCN, LCWM & LCV				0.1	**0.1**	% FSR
DAC0831LCN				0.2	**0.2**	% FSR
DAC0832LCN, LCWM & LCV				0.4	**0.4**	% FSR
Monotonicity	$-10V \le V_{REF} \le +10V$ LJ & LCJ	4		**8**	**8**	bits
	$-10V \le V_{REF} \le +10V$ LCN, LCWM & LCV			8	**8**	bits
Gain Error Max	Using Internal R_{fb} $-10V \le V_{REF} \le +10V$	7	±0.2	±1	**±1**	% FS
Gain Error Tempco Max	Using internal R_{fb}		**0.0002**		**0.0006**	% FS/°C
Power Supply Rejection	All digital inputs latched high					
	$V_{CC} = 14.5V$ to 15.5V		0.0002	0.0025		% FSR/V
	11.5V to 12.5V		0.0006			
	4.5V to 5.5V		0.013	0.015		
Reference Input Max			**15**	**20**	**20**	kΩ
Reference Input Min			**15**	**10**	**10**	kΩ
Output Feedthrough Error	$V_{REF} = 20$ Vp-p, f = 100 kHz All data inputs latched low		3			mVp-p

Electrical Characteristics $V_{REF} = 10.000\ V_{DC}$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$. (Continued)

Parameter		Conditions		See Note	$V_{CC} = 4.75\ V_{DC}$ $V_{CC} = 15.75\ V_{DC}$		$V_{CC} = 5\ V_{DC} \pm 5\%$ $V_{CC} = 12\ V_{DC} \pm 5\%$ to $15\ V_{DC} \pm 5\%$	Limit Units
					Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER CHARACTERISTICS (Continued)								
Output Leakage Current Max	I_{OUT1}	All data inputs latched low	LJ & LCJ	10		**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
	I_{OUT2}	All data inputs latched high	LJ & LCJ			**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
Output Capacitance	I_{OUT1} I_{OUT2}	All data inputs latched low			45 115			pF
	I_{OUT1} I_{OUT2}	All data inputs latched high			130 30			pF
DIGITAL AND DC CHARACTERISTICS								
Digital Input Voltages	Max	Logic Low	LJ 4.75V			**0.6**		V_{DC}
			LJ 15.75V			**0.8**		
			LCJ 4.75V			**0.7**		
			LCJ 15.75V			**0.8**		
			LCN, LCWM, LCV			0.95	**0.8**	
	Min	Logic High	LJ & LCJ			**2.0**	**2.0**	V_{DC}
			LCN, LCWM, LCV			1.9	**2.0**	
Digital Input Currents	Max	Digital inputs < 0.8V						
			LJ & LCJ		−50	**−200**	**−200**	μA
			LCN, LCWM, LCV			−160	**−200**	μA
		Digital inputs > 2.0V						
			LJ & LCJ		0.1	**+10**	**+10**	μA
			LCN, LCWM, LCV			+8	**+10**	
Supply Current Drain	Max		LJ & LCJ		1.2	**3.5**	**3.5**	mA
			LCN, LCWM, LCV			1.7	**2.0**	

3

Electrical Characteristics

$V_{REF} = 10.000\ V_{DC}$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	See Note	$V_{CC} = 15.75\ V_{DC}$		$V_{CC} = 12\ V_{DC} \pm 5\%$ to $15\ V_{DC} \pm 5\%$	$V_{CC} = 4.75\ V_{DC}$		$V_{CC} = 5\ V_{DC} \pm 5\%$	Limit Units
				Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
AC CHARACTERISTICS										
t_s	Current Setting Time	$V_{IL} = 0V$, $V_{IH} = 5V$		1.0			1.0			µs
t_W	Write and XFER Pulse Width Min	$V_{IL} = 0V$, $V_{IH} = 5V$	11 9	100	250 **320**	**320**	375	600 **900**	**900**	ns
t_{DS}	Data Setup Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9	100	250 **320**	**320**	375	600 **900**	**900**	ns
t_{DH}	Data Hold Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9		30 **30**			50 **50**		ns
t_{CS}	Control Setup Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9	110	250 **320**	**320**	600	900 **1100**	**1100**	ns
t_{CH}	Control Hold Time Min	$V_{IL} = 0V$, $V_{IH} = 5V$	9	0	0 **0**	**10**	0	0 **0**		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$ (plastic) or 150°C (ceramic), and the typical junction-to-ambient thermal resistance of the J package when board mounted is 80°C/W. For the N package, this number increases to 100°C/W and for the V package this number is 120°C/W.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Guaranteed at $V_{REF} = \pm 10\ V_{DC}$ and $V_{REF} = \pm 1\ V_{DC}$.

Note 8: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)". This guarantees that after performing a zero and full scale adjustment (see Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

Note 9: Boldface tested limits apply to the LJ and LCJ suffix parts only.

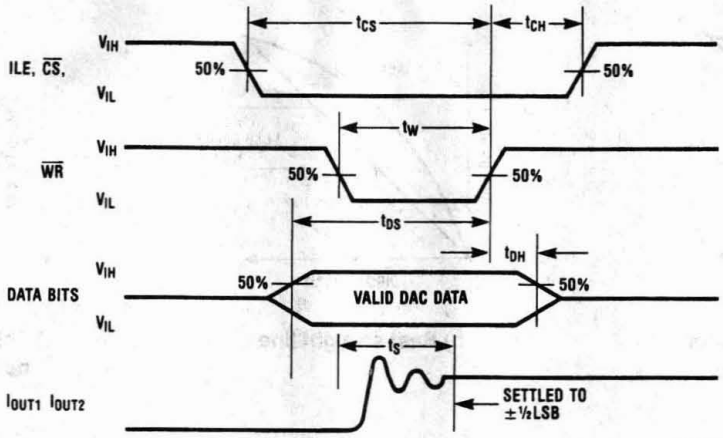
Note 10: A 100nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(100 \times 10^{-9} \times 20 \times 10^3) \times 100/10$ which is 0.02% of FS.

Note 11: The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 12: Typicals are at 25°C and represent most likely parametric norm.

Note 13: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Waveform



TL/H/5608–2

Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{CS}$: **Chip Select** (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: **Input Latch Enable** (active high). The ILE in combination with $\overline{CS}$ enables $\overline{WR_1}$.

$\overline{WR_1}$: **Write 1.** The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch—$\overline{CS}$ and $\overline{WR_1}$ must be low while ILE is high.

$\overline{WR_2}$: **Write 2** (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: **Transfer control signal** (active low). The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0-DI_7: **Digital Inputs.** DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: **DAC Current Output 1.** I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: **DAC Current Output 2.** I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} =$ constant (I full scale for a fixed reference voltage).

R_{fb}: **Feedback Resistor.** The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: **Reference Voltage Input.** This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: **Digital Supply Voltage.** This is the power supply pin for the part. V_{CC} can be from +5 to $+15V_{DC}$. Operation is optimum for $+15V_{DC}$.

GND: The pin 10 voltage must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications. Any difference of potential (V_{OS} pin 10) will result in a linearity change of

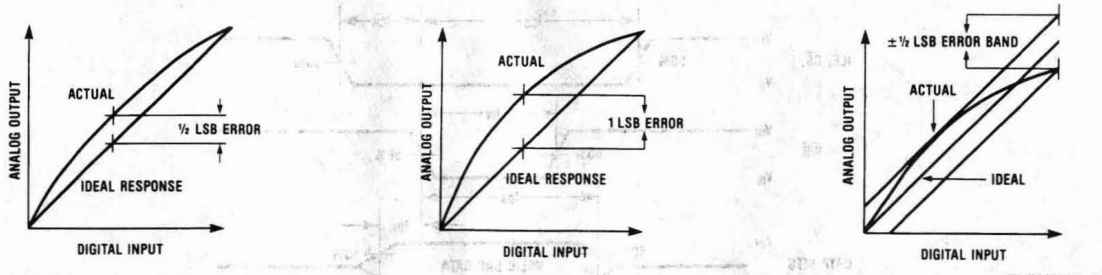
$$\frac{V_{OS} \text{ pin } 10}{3V_{REF}}$$

For example, if V_{REF} = 10V and pin 10 is 9mV offset from I_{OUT1} and I_{OUT2} the linearity change will be 0.03%.

Pin 3 can be offset ±100mV with no linearity change, but the logic input threshold will shift.

3

Linearity Error



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a) End point test after zero and fs adj.

b) Best straight line

c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within $\pm\frac{1}{2}$LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is $V_{REF} - 1$LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 39mV = 9.961V$. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

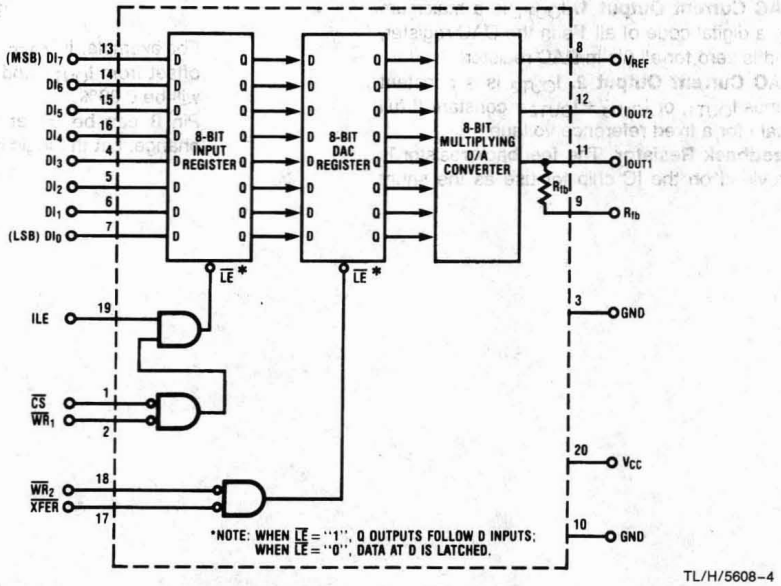

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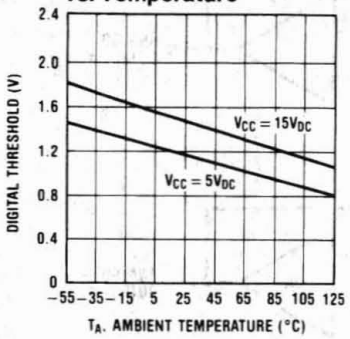
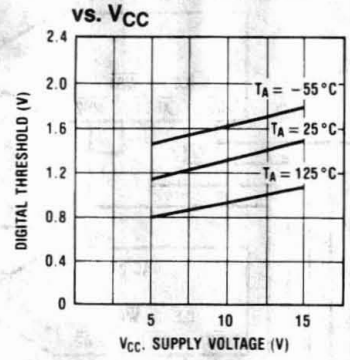
FIGURE 1. DAC0830 Functional Diagram

Typical Performance Characteristics

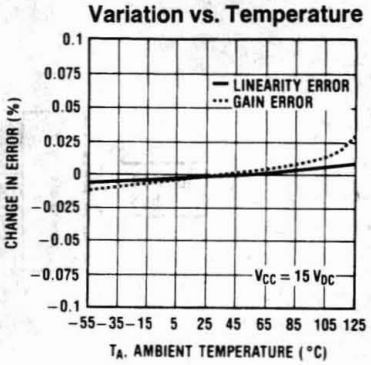
Digital Input Threshold vs. Temperature



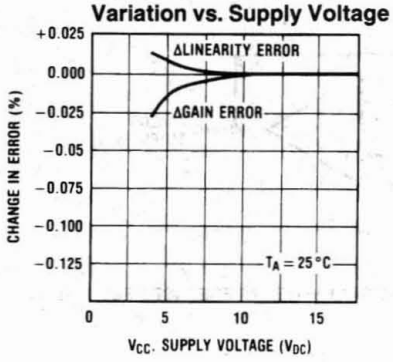
Digital Input Threshold vs. V_{CC}



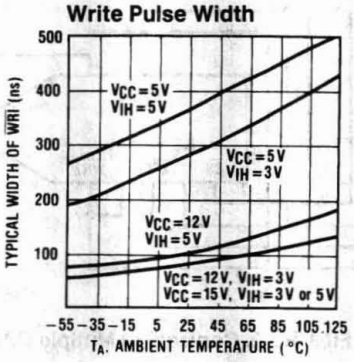
Gain and Linearity Error Variation vs. Temperature



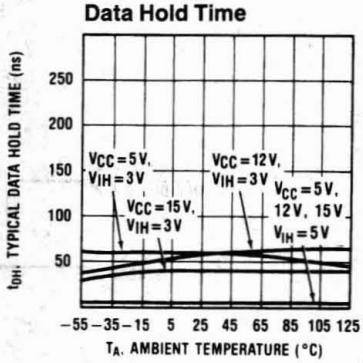
Gain and Linearity Error Variation vs. Supply Voltage



Write Pulse Width


TYPICAL WIDTH OF $\overline{WR1}$ (ns)
500
400
300
200
100
$V_{CC} = 5V$, $V_{IH} = 5V$
$V_{CC} = 5V$, $V_{IH} = 3V$
$V_{CC} = 12V$, $V_{IH} = 5V$
$V_{CC} = 12V$, $V_{IH} = 3V$
$V_{CC} = 15V$, $V_{IH} = 3V$ or 5V
−55 −35 −15 5 25 45 65 85 105 125
T_A, AMBIENT TEMPERATURE (°C)

Data Hold Time


t_{DH}, TYPICAL DATA HOLD TIME (ns)
250
200
150
100
50
$V_{CC} = 5V$, $V_{IH} = 3V$
$V_{CC} = 15V$, $V_{IH} = 3V$
$V_{CC} = 12V$, $V_{IH} = 3V$
$V_{CC} = 5V$, 12V, 15V $V_{IH} = 5V$
−55 −35 −15 5 25 45 65 85 105 125
T_A, AMBIENT TEMPERATURE (°C)

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DAC0830 Series Application Hints

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte μP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0 = "1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in section 1.1).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 DIGITAL CONSIDERATIONS

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

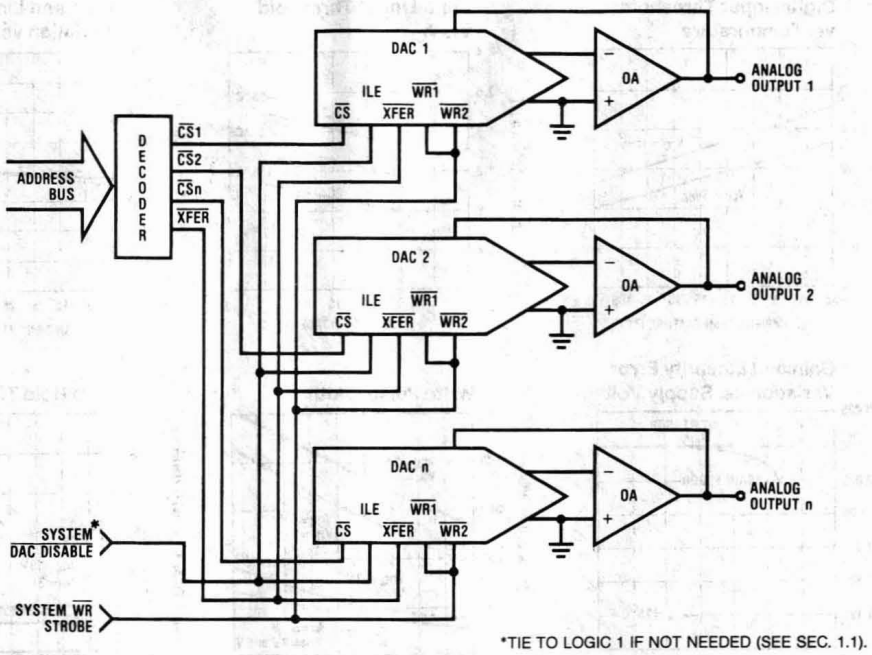
The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write-only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{CS}$ pin and a second for the DAC latch which is controlled by the $\overline{XFER}$ line. If more than one DAC is being driven, *Figure 2*, the $\overline{CS}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{XFER}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, *Figure 3*.

It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{XFER}$ command.

DAC0830 Series Application Hints (Continued)



*TIE TO LOGIC 1 IF NOT NEEDED (SEE SEC. 1.1).

FIGURE 2. Controlling Mutiple DACs

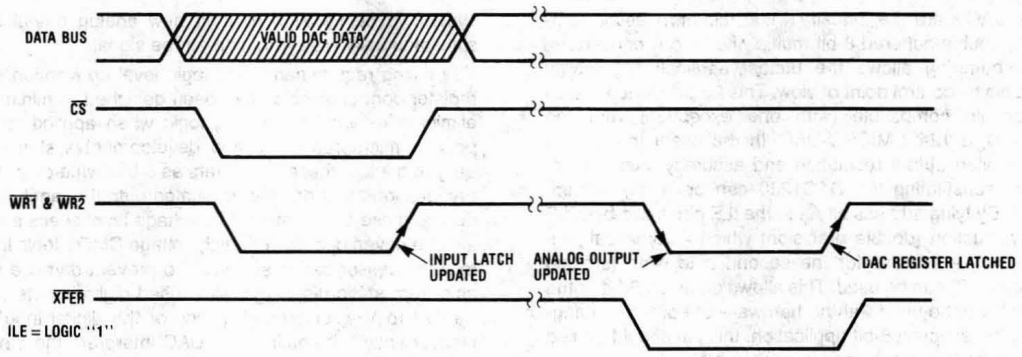


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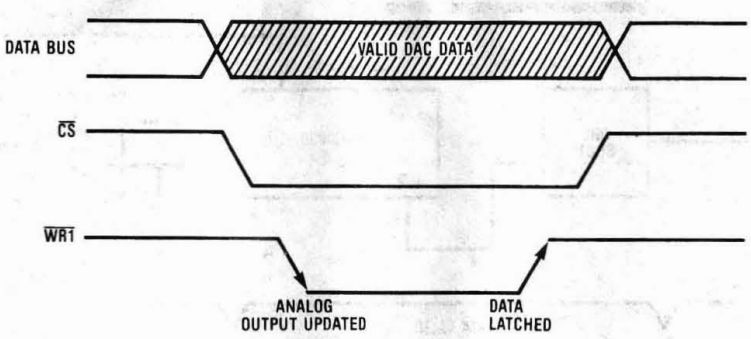
FIGURE 3

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{CS}$ signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

DAC0830 Series Application Hints (Continued)



ILE = LOGIC "1"; $\overline{WR2}$ and $\overline{XFER}$ GROUNDED

FIGURE 4

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughput to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in *Figure 4*.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR_1}$ low to update the DAC with $\overline{CS}$, $\overline{WR_2}$ and $\overline{XFER}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR_1}$, $\overline{WR_2}$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 900 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 180ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 50ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulsewidth. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 5* for an exemplary system which provides a 250ns $\overline{WR}$ strobe time with a data hold time of less than 10ns.

The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulsewidth is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (*Figure 8*) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

DAC0830 Series Application Hints (Continued)

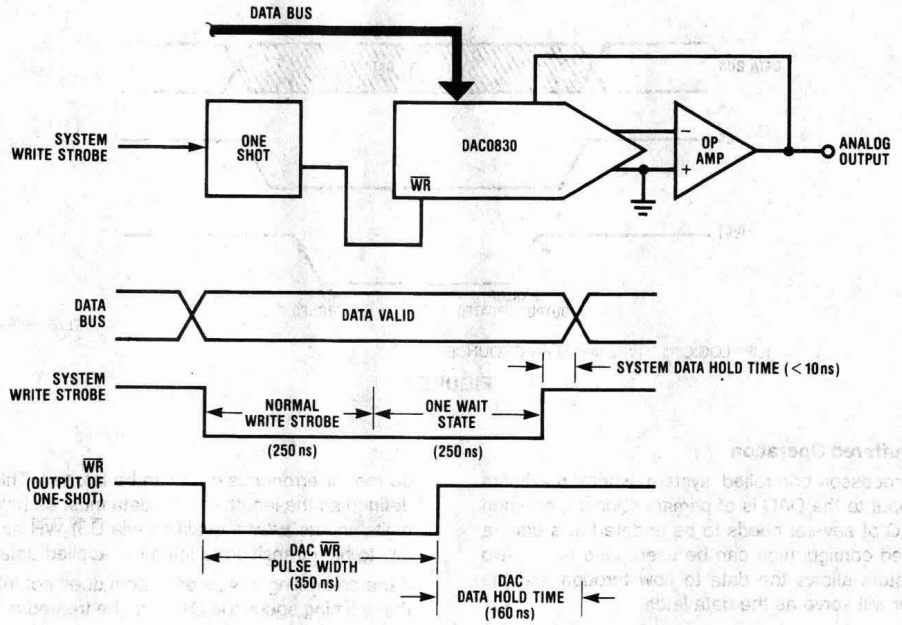


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FIGURE 5. Accommodating a High Speed System

2.0 ANALOG CONSIDERATIONS

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\ k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\ k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, *Figure 6*, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in *Figure 6*. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 7*.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15 kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

DAC0830 Series Application Hints (Continued)

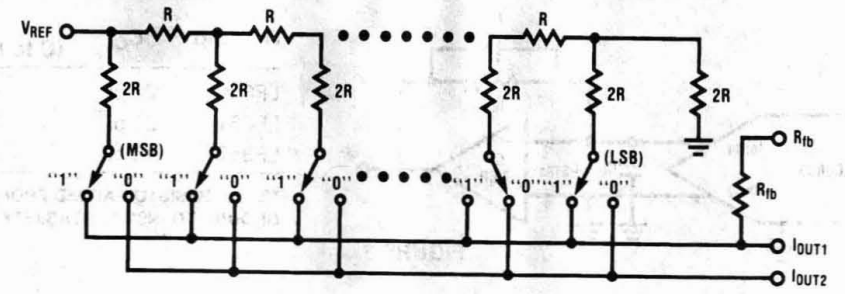

FIGURE 6

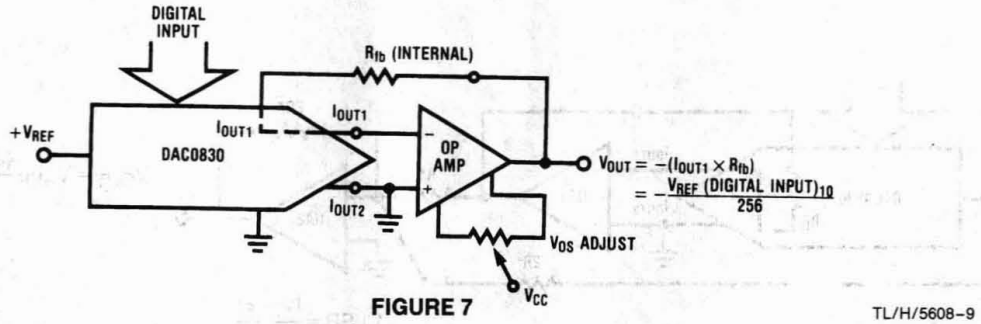

FIGURE 7

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2.3 Op Amp Considerations

The op amp used in *Figure 7* should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 8*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

2.4 Bipolar Output Voltage with a Fixed Reference

The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm$ Digital Code $= \pm V_{OUT}$. This circuit is shown in *Figure 9*.

This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DACs. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking temperature coefficient. Two of the four available 10 kΩ resistors can be paralleled to form R in *Figure 9* and the other two can be used independently as the resistances labeled 2R.

2.5 Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (*Figure 7*) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.

3

DAC0830 Series Application Hints (Continued)

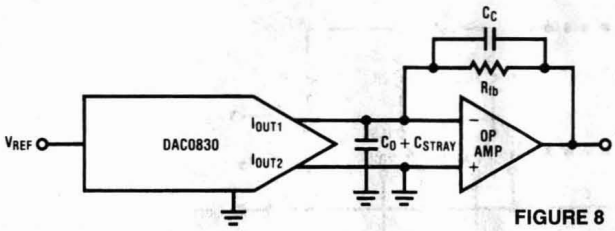
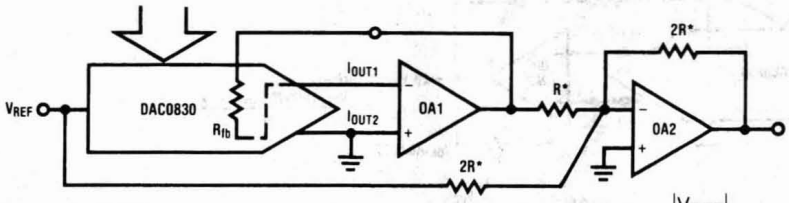


FIGURE 8

OP Amp	C_C	t_s (O to Full Scale)
LF356	22 pF	4 μs
LF351	22 pF	5 μs
LF357*	10 pF	2 μs

*2.4 kΩ RESISTOR ADDED FROM − INPUT TO GROUND TO INSURE STABILITY



$$V_{OUT} = V_{REF} \frac{(\text{DIGITAL CODE} - 128)}{128}$$

TL/H/5608–10

$$1\ \text{LSB} = \frac{|V_{REF}|}{128}$$

*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

Input Code MSB ..... LSB	IDEAL V_{OUT} $+V_{REF}$	IDEAL V_{OUT} $-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	−1 LSB	+1 LSB
0 0 1 1 1 1 1 1	$-\frac{\lvert V_{REF}\rvert}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0 0 0 0 0 0 0 0	$-\lvert V_{REF}\rvert$	$+\lvert V_{REF}\rvert$

FIGURE 9

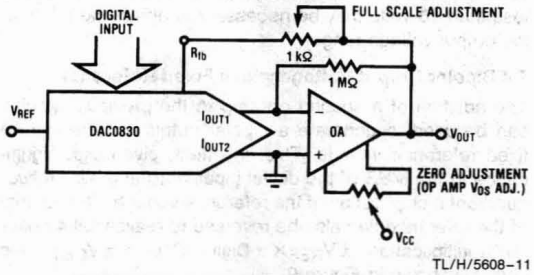
2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in *Figure 10* to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error temperature coefficient by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in *Figure 10*, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error temperature coefficent would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Using the DAC0830 in a Voltage Switching Configuration

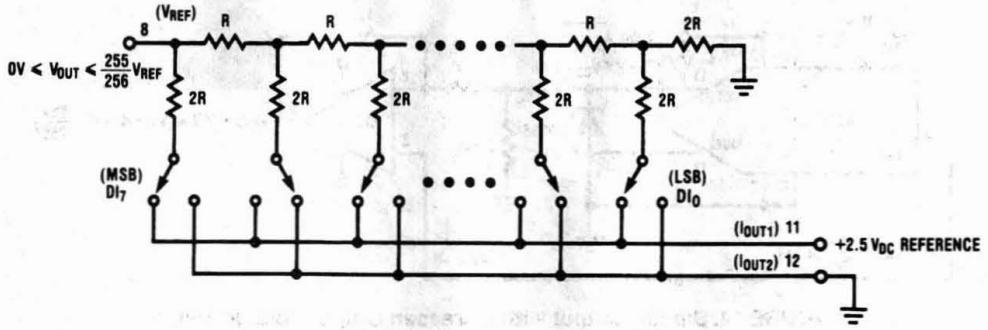
The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in *Figure 11*.



TL/H/5608–11

FIGURE 10. Adding Full-Scale Adjustment

DAC0830 Series Application Hints (Continued)

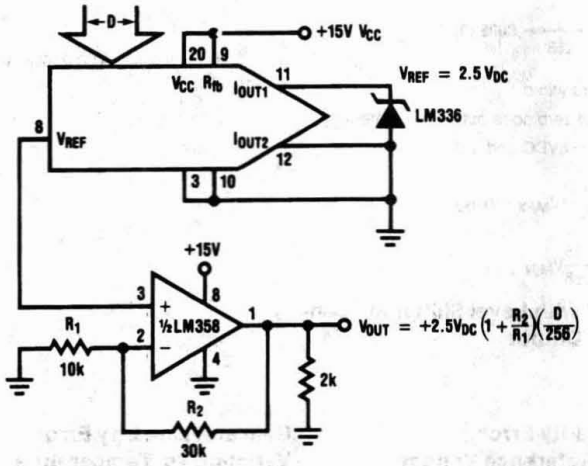


TL/H/5608–12

FIGURE 11. Voltage Mode Switching

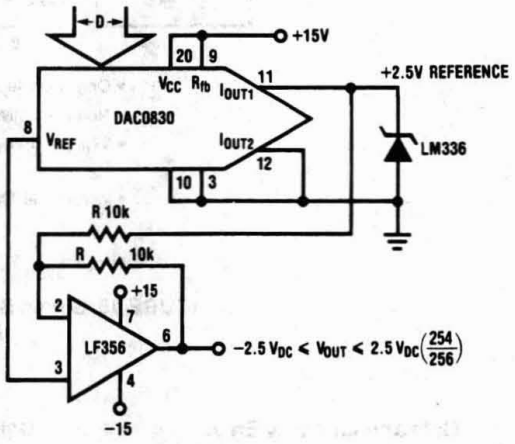
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in *Figures 12, 13, 14* and *15*.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drive requirements of the ladder switches. To ensure that all 8 switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions ensure less than 0.1% linearity and gain error change. *Figures 16, 17* and *18* characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.



- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

FIGURE 12. Single Supply DAC



TL/H/5608–13

- $V_{OUT} = 2.5V\left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 μs

FIGURE 13. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

3

DAC0830 Series Application Hints (Continued)

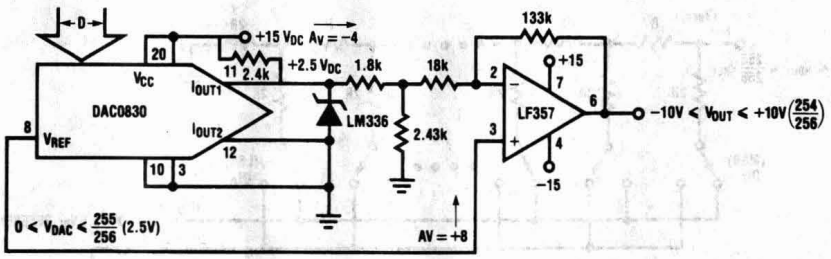
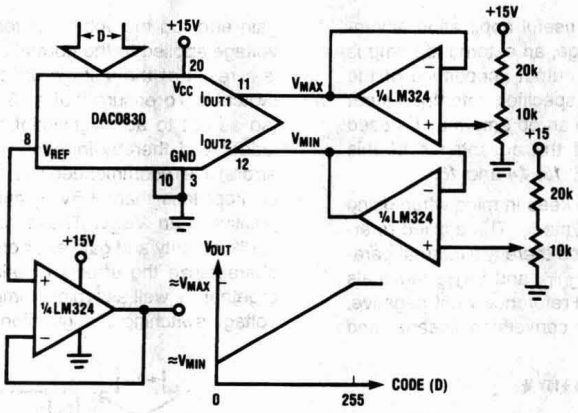


FIGURE 14. Bipolar Output with Increased Output Voltage Swing



TL/H/5608–14

- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be ≤ +5VDC and ≥0V.
- Incremental Output Step $= \frac{1}{256}(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}V_{MIN}$

FIGURE 15. Single Supply DAC with Level Shift and Span-Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage

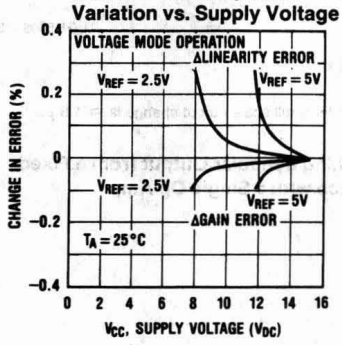


FIGURE 16

Gain and Linearity Error Variation vs. Reference Voltage

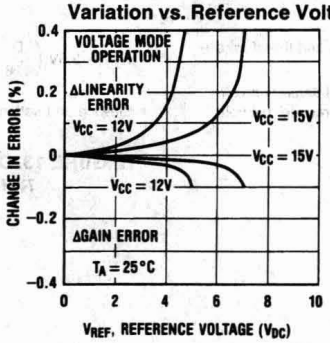
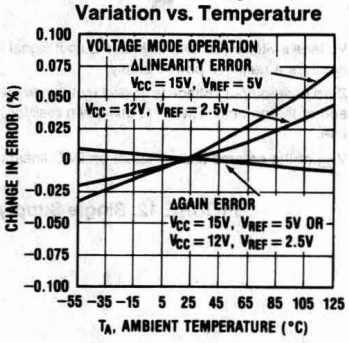


FIGURE 17

Note: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

Gain and Linearity Error Variation vs. Temperature



TL/H/5608–15

FIGURE 18

DAC0830 Series Application Hints (Continued)

2.8 Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DACs.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

3.0 GENERAL APPLICATION IDEAS

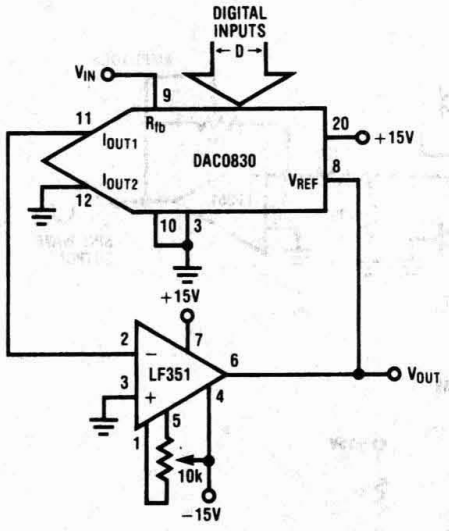
The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input								
Pin 13 MSB							Pin 7 LSB	D Decimal Equivalent
1	1	1	1	1	1	1	1	255
1	0	0	0	0	0	0	0	128
0	0	0	1	0	0	0	0	16
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0

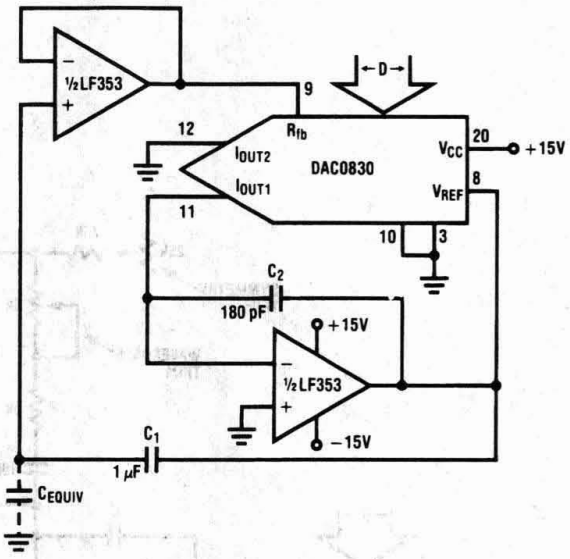
Applications

DAC Controlled Amplifier (Volume Control)



- $V_{OUT} = \frac{-V_{IN}(256)}{D}$
- When D = 0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the − input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.

Capacitance Multiplier

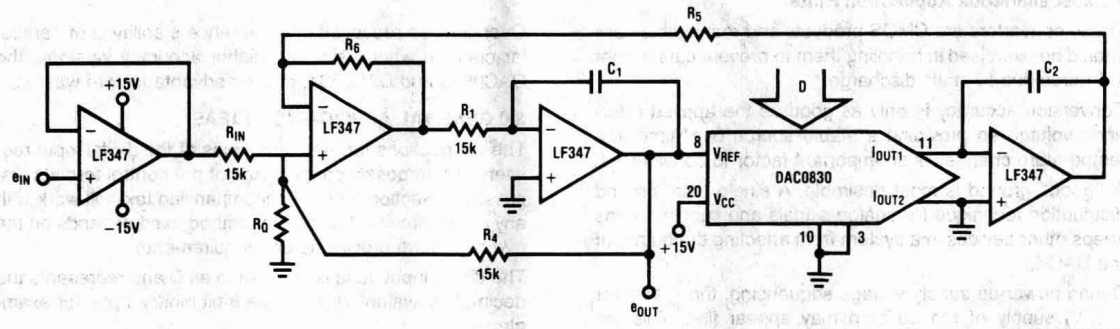


TL/H/5608–16

- $C_{EQUIV} = C_1\left(1 + \frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\ (\text{op amp})}{1 + \frac{256}{D}}$
- C_2 is used to improve settling time of op amp.

Applications (Continued)

Variable f_O, Variable Q_O, Constant BW Bandpass Filter



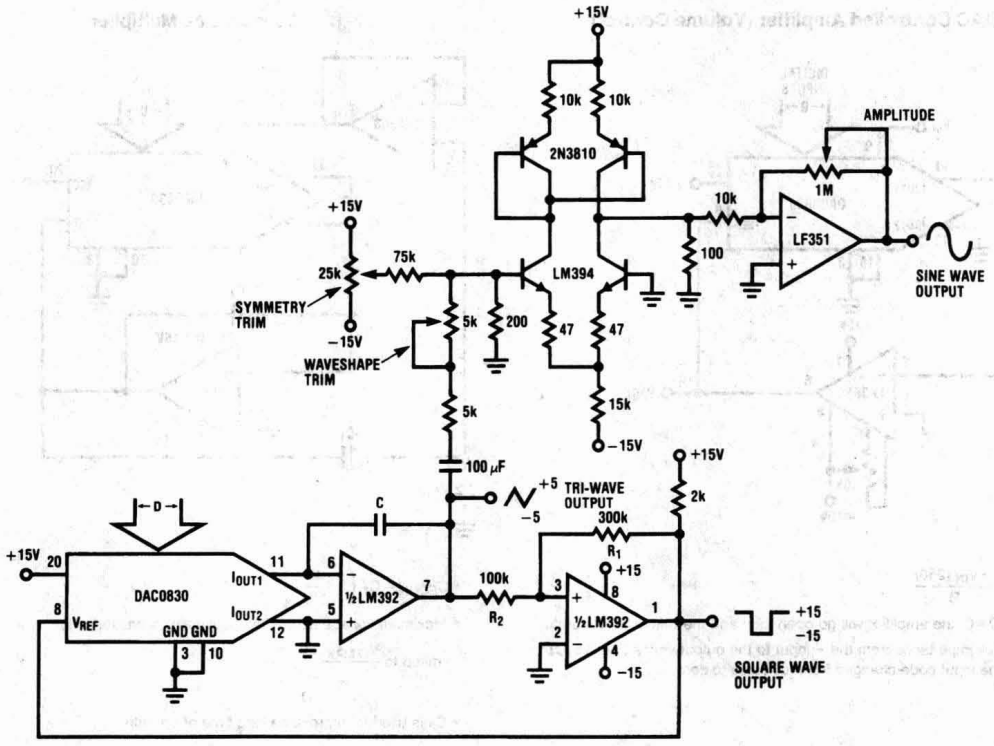
TL/H/5608–17

- $f_O = \frac{\sqrt{\frac{KD}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\frac{KD}{256}} \frac{(2R_Q + R_1)}{R_Q(K+1)}$; $3dbBW = \frac{R_Q(K+1)}{2\pi R_1 C(2R_Q + R_1)}$

  where $C_1 = C_2 = C$; $K = \frac{R_6}{R_5}$ and R_1 = R of DAC = 15k

- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be ≤200 kHz.

DAC Controlled Function Generator

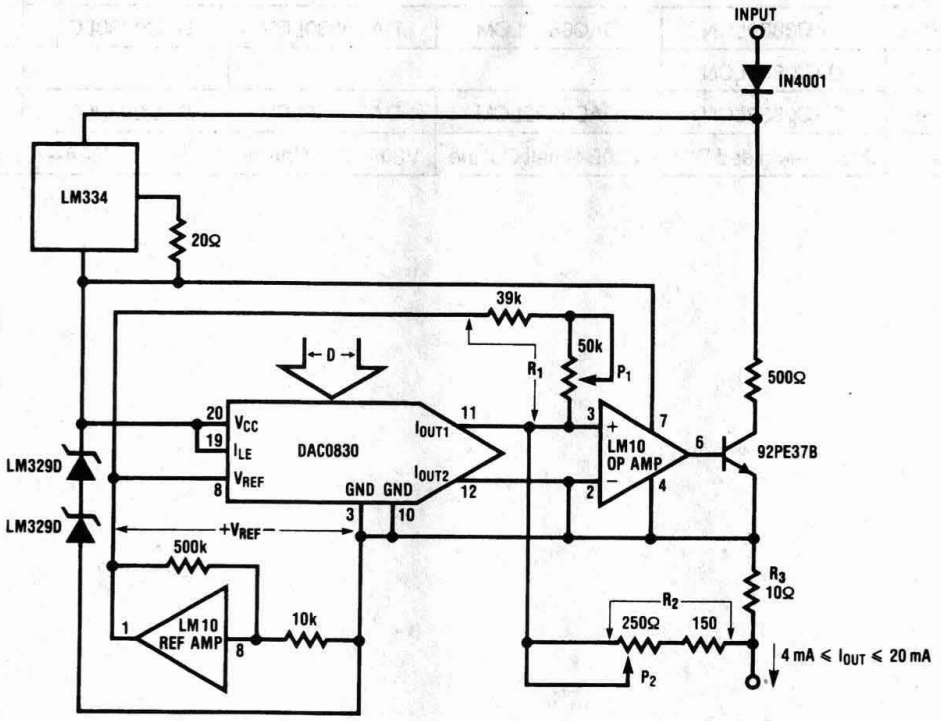


TL/H/5608–18

- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \frac{D}{256(20k)C}$ for $V_{OMAX} = V_{0MIN}$ of square wave output and $R_1 = 3\,R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave-shape for minimum sine wave distortion.

Applications (Continued)

Two Terminal Floating 4 to 20 mA Current Loop Controller

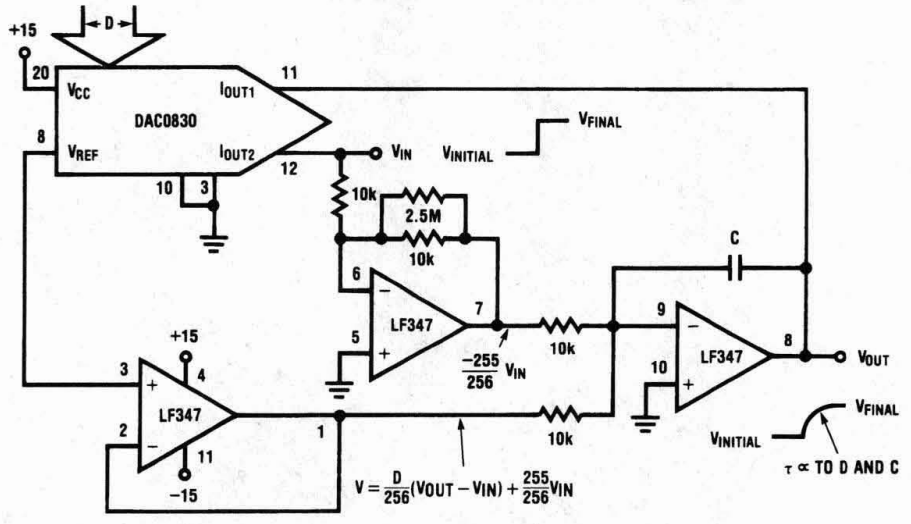


TL/H/5608–19

$$I_{OUT} = V_{REF}\left[\frac{1}{R_1} + \frac{D}{256\,R_{fb}}\right]\left[1 + \frac{R_2}{R_3}\right]$$

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D=0) to 19.94 mA (for D=255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).

DAC Controlled Exponential Time Response



TL/H/5608–20

- Output responds exponentially to input changes and automatically stops when $V_{OUT}=V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See section 2.7)

Ordering Information

Temperature Range		0°C to +70°			−40°C to +85°C	−55°C to +125°C
Non Linearity	0.05% FSR	DAC0830LCN	DAC0830LCM	DAC0830LCV	DAC0830LCJ	DAC0830LJ
	0.1% FSR	DAC0831LCN				
	0.2% FSR	DAC0832LCN	DAC0832LCM	DAC0832LCV	DAC0832LCJ	DAC0832LJ
Package Outline		N20A—Molded DIP	M20B Small Outline	V20A Chip Carrier	J20A—Ceramic DIP	

National Semiconductor

DAC0854 Quad 8-Bit Voltage-Output Serial D/A Converter with Readback

General Description

The DAC0854 is a complete quad 8-bit voltage-output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, internal voltage reference, and a serial microprocessor interface. By combining in one package the reference, amplifiers, and conversion circuitry for four D/A converters, the DAC0854 minimizes wiring and parts count and is hence ideally suited for applications where cost and board space are of prime concern.

The DAC0854 also has a data readback function, which can be used by the microprocessor to verify that the desired input word has been properly latched into the DAC0854's data registers. The data readback function simplifies the design and reduces the cost of systems which need to verify data integrity.

The logic comprises a MICROWIRE™-compatible serial interface and control circuitry. The interface allows the user to write to any one of the input registers or to all four at once. The latching registers are double-buffered, consisting of 4 separate input registers and 4 DAC registers. Double buffering allows all 4 DAC outputs to be updated simultaneously.

The four reference inputs allow the user to configure the system to have a separate output voltage range for each DAC. The output voltage of each DAC can range between 0.3V and 2.8V and is a function of V_{BIAS}, V_{REF}, and the input word.

Features

- Single +5V supply operation
- MICROWIRE serial interface allows easy interface to many popular microcontrollers including the COPS™ and HPC™ families of microcontrollers
- Data readback capability
- Output data can be formatted to read back MSB or LSB first
- Versatile logic allows selective or global update of the DACs
- Power fail flag
- Output amplifiers can drive 2 kΩ load
- Synchronous/asynchronous update of the DAC outputs

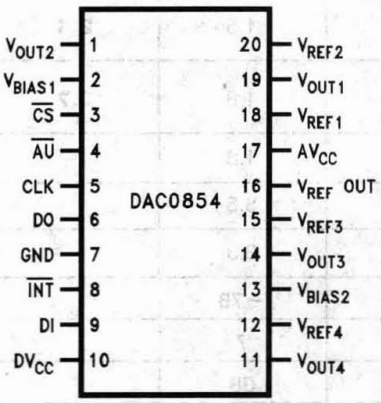
Key Specifications

■ Guaranteed monotonic over temperature	
■ Integral linearity error	±½ LSB max
■ Output settling time	2.7 μs max
■ Analog output voltage range	0.3V to 2.8V
■ Supply voltage range	4.5V to 5.5V
■ Clock frequency	10 MHz max
■ Power dissipation (f_{CLK} = 10 MHz)	95 mW max
■ On-board reference	2.65V ±2% max

Applications

- Automatic test equipment
- Industrial process controls
- Automotive controls and diagnostics
- Instrumentation

Connection Diagram



TL/H/11261–1

Top View

Ordering Information

Industrial (−40°C < T_A +85°C)	Package
DAC0854BIN, DAC0854CIN	N20A Molded DIP
DAC0854CIJ	J20A Ceramic DIP
DAC0854BIWM, DAC0854CIWM	M20B Small Outline
Military (−55°C < T_A < +125°C)	
DAC0854CMJ/883	J20A Ceramic DIP

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 24)

Supply Voltage (AV_{CC}, DV_{CC})	7V
Supply Voltage Difference ($AV_{CC}-DV_{CC}$)	±5.5V
Voltage at Any Pin (Note 3)	GND −0.3V to AV_{CC}/DV_{CC} +0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 4)	20 mA
Power Dissipation (Note 5)	105 mW
ESD Susceptibility (Note 6)	1250V
Soldering Information	
J Package (10 sec.)	300°C
N Package (10 sec.)	260°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Supply Voltage	4.5V to 5.5V
Supply Voltage Difference ($AV_{CC} - DV_{CC}$)	±IV
Temperature Range	$T_{MIN} < T_A < T_{MAX}$
DAC0854BIN, DAC0854CIN, DAC0854CIJ, DAC0854BIWM, DAC0854CIWM	$-40°C < T_A < 85°C$
DAC0854CMJ/883	$-55°C < T_A < 125°C$

Converter Electrical Characteristics

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 1, 11, 14, and 19) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
STATIC CHARACTERISTICS					
n	Resolution	$f_{CLK} = 10$ MHz	8	**8**	bits
	Monotonicity	(Note 10)	8	**8**	bits
	Integral Linearity Error DAC0854BIN, DAC0854BIWM DAC0854CIN, DAC0854CIJ, DAC0854CIWM, DAC0854CMJ	(Note 11)		**±0.5** **±1.0**	LSB (max) LSB (max)
	Differential Linearity Error			**±1.0**	LSB (max)
	Fullscale Error	(Note 12)		**±35**	mV
	Fullscale Error Tempco	(Note 13)	−30		ppm/°C
	Zero Error	(Note 14)		**±35**	mV
	Zero Error Tempco	(Note 13)	−30		ppm/°C
	Power Supply Sensitivity	(Note 15)	−42	**−34**	dB (max)
DYNAMIC CHARACTERISTICS					
t_{s+}	Positive Voltage Output Settling Time	(Note 16) $C_L = 200$ pF	1.5	**2.1**	μs
t_{s-}	Negative Voltage Output Settling Time	(Note 16) $C_L = 200$ pF	1.8	**2.7**	μs
	Digital Crosstalk	(Note 17)	1.8		mV_{p-p}
	Digital Feedthrough	(Note 18)	8.5		mV_{p-p}
	Clock Feedthrough	(Note 19)	3.3		mV_{p-p}
	Channel-to-Channel Isolation	(Note 20)	−78		dB
	Glitch Energy	(Note 21)	7		nV−s
	Peak Value of Largest Glitch		38		mV
PSRR	Power Supply Rejection Ratio	(Note 22)	−49		dB

Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\,k\Omega$ (R_L is the load resistor on the analog outputs – pins 1, 11, 14, and 19) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
DIGITAL AND DC ELECTRICAL CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$AV_{CC} = DV_{CC} = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$AV_{CC} = DV_{CC} = 4.5V$		**0.8**	V (max)
I_{IL}	Digital Input Leakage Current		1	**5**	μA (max)
C_{IN}	Input Capacitance		4		pF
C_{OUT}	Output Capacitance		5		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{SOURCE} = 0.8$ mA		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{SINK} = 3.2$ mA		**0.4**	V (max)
V_{INT}	Interrupt Pin Output Voltage	10 kΩ Pullup		**0.4**	V (max)
I_S	Supply Current	Outputs Unloaded	14	**19**	mA
REFERENCE INPUT CHARACTERISTICS					
V_{REF}	Input Voltage Range		0–2.75		V
R_{REF}	Input Resistance		7	**4** **10**	kΩ (min) kΩ (max)
C_{REF}	Input Capacitance	Full-Scale Data Input	40		pF
V_{BIAS} INPUT CHARACTERISTICS					
V_{BIAS}	V_{BIAS} Input Voltage Range		0.3–1.4		V
	Input Leakage		1		μA
C_{BIAS}	Input Capacitance		9		pF
BANDGAP REFERENCE CHARACTERISTICS ($C_L = 220\mu F$)					
$V_{REF}OUT$	Output Voltage			**2.65 ± 2%**	V
$\Delta V_{REF}/\Delta T$	Tempco	(Note 23)	22		ppm/°C
	Line Regulation	$4.5V < V_{CC} < 5.5V$, $I_L = 4$ mA	2	**5**	mV
$\Delta V_{REF}/\Delta I_L$	Load Regulation	$0 < I_L < 4$ mA $0 < I_L < 4$ mA; CMJ Suffix $-1 < I_L < 0$ mA	2 2 2.5	**6** **15**	mV mV mV
I_{SC}	Short Circuit Current	$V_{REF}OUT = 0V$	12		mA
AC ELECTRICAL CHARACTERISTICS					
t_{DS}	Data Setup Time			**10**	ns (min)
t_{DH}	Data Hold Time			**0**	ns (min)
t_{CS}	Control Setup Time			**15**	ns (min)
t_{CH}	Control Hold Time			**0**	ns (min)
t_{MIN}	Clock Frequency			**10**	MHz (max)
t_H	Minimum Clock High Time			**20**	ns (min)
t_L	Minimum Clock Low Time			**40**	ns (min)

Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 1, 11, 14, and 19) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS (Continued)					
t_{CZ1}	Output Hi-Z to Valid 1			**37**	ns (max)
t_{CZ0}	Output Hi-Z to Valid 0			**42**	ns (max)
t_{1H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF		**130**	ns (max)
t_{0H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF		**117**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Converter Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{Jmax} and Θ_{JA} for the various packages and versions of the DAC0854.

Part Number	T_{Jmax} (°C)	Θ_{JA} (°C/W)
DAC0854BIN, DAC0854CIN	125	46
DAC0854BIJ, DAC0854CIJ	125	53
DAC0854BIWM, DAC0854CIWM	125	64
DAC0854CMJ/883	150	53

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Production Reliability" of the section titled "Surface Mount" found in any current Linear Databook for other methods of soldering surface mount devices.

Note 8: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: A monotonicity of 8 bits for the DAC0854 means that the output voltage changes in the same direction (or remains constant) for each increase in the input code.

Note 11: Integral linearity error is the maximum deviation of the output from the line drawn between zero and full-scale (excluding the effects of zero error and full-scale error).

Note 12: Full-scale error is measured as the deviation from the ideal 2.800V full-scale output when $V_{REF} = 2.650V$ and $V_{BIAS} = 1.400V$.

Note 13: Full-scale error tempco and zero error tempco are defined by the following equation:

$$\text{Error tempco} = \left[\frac{\text{Error } (T_{MAX}) - \text{Error } (T_{MIN})}{V_{SPAN}}\right] \left[\frac{10^6}{T_{MAX} - T_{MIN}}\right]$$

where Error (T_{MAX}) is the zero error or full-scale error at T_{MAX} (in volts), and Error (T_{MIN}) is the zero error or full-scale error at T_{MIN} (in volts); V_{SPAN} is the output voltage span of the DAC0854, which depends on V_{BIAS} and V_{REF}.

Note 14: Zero error is measured as the deviation from the ideal 0.310V output when $V_{REF} = 2.650V$, $V_{BIAS} = 1.400V$, and the digital input word is all zeros.

Note 15: Power Supply Sensitivity is the maximum change in the offset error or the full-scale error when the power supply differs from its optimum 5V by up to 0.25V (5%). The load resistor $R_L = 5\ k\Omega$.

Note 16: Positive or negative settling time is defined as the time taken for the output of the DAC to settle to its final full-scale or zero output to within ±0.5 LSB. This time shall be referenced to the 50% point of the positive edge of $\overline{CS}$, which initiates the update of the analog outputs.

Note 17: Digital crosstalk is the glitch measured on the output of one DAC while applying an all 0s to all 1s transition at the input of the other DACs.

Note 18: All DACs have full-scale outputs latched and DI is clocked with no update of the DAC outputs. The glitch is then measured on the DAC outputs.

Note 19: Clock feedthrough is measured for each DAC with its output at full-scale. The serial clock is then applied to the DAC at a frequency of 10 MHz and the glitch on each DAC full-scale output is measured.

Note 20: Channel-to-channel isolation is a measure of the effect of a change in one DAC's output on the output of another DAC. The V_{REF} of the first DAC is varied between 1.4V and 2.65V at a frequency of 15 kHz while the change in full-scale output of the second DAC is measured. The first DAC is loaded with all 0s.

Note 21: Glitch energy is the difference between the positive and negative glitch areas at the output of the DAC when a 1 LSB digital input code change is applied to the input. The glitch energy will have its largest value at one of the three major transitions. The peak value of the maximum glitch is separately specified.

Note 22: Power Supply Rejection Ratio is measured by varying $AV_{CC} = DV_{CC}$ between 4.75V and 5.25V with a frequency of 10 kHz and measuring the proportion of this signal imposed on a full-scale output of the DAC under consideration.

Note 23: The bandgap reference tempco is defined by the following equation:

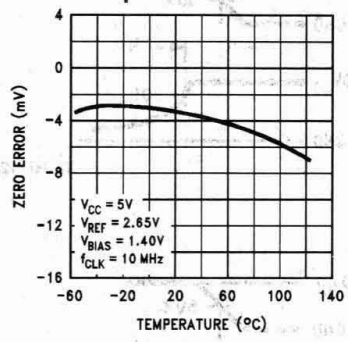
$$\text{Tempco} = \left[\frac{V_{REF}\ (T_{MAX}) - V_{REF}\ (T_{MIN})}{V_{REF}\ (T_{ROOM})}\right] \left[\frac{10^6}{T_{MAX} - T_{MIN}}\right]$$

where $T_{ROOM} = 25°C$, V_{REF} (T_{MAX}) is the reference output at T_{MAX}, and similarly for V_{REF} (T_{MIN}) and V_{REF} (T_{ROOM}).

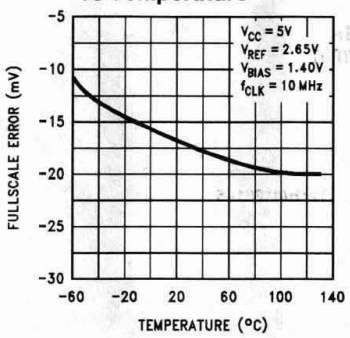
Note 24: A Military RETS specification is available upon request.

Typical Converter Performance Characteristics

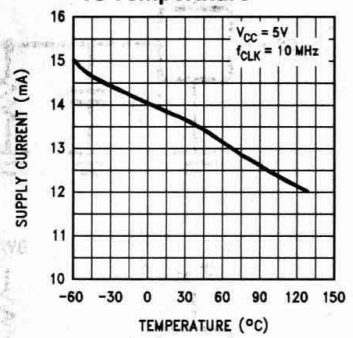
Zero Error vs Temperature



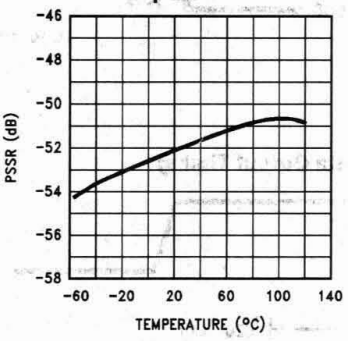
Full-Scale Error vs Temperature



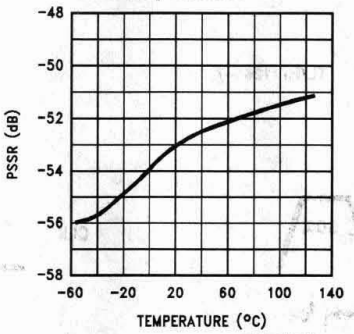
Supply Current vs Temperature



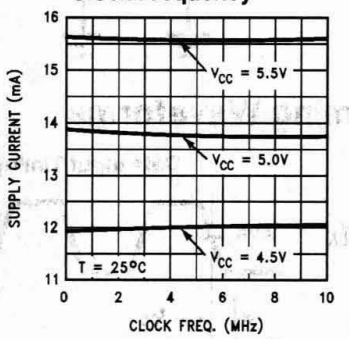
Zero Error PSRR vs Temperature



Full-Scale Error PSRR vs Temperature



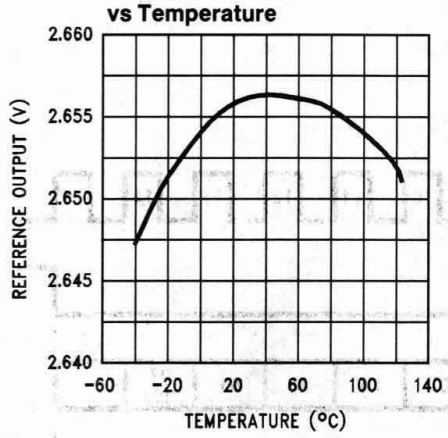
Supply Current vs Clock Frequency



TL/H/11261–2

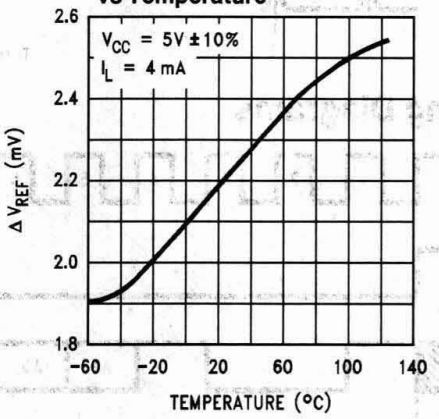
Typical Reference Performance Characteristics

Bandgap Voltage vs Temperature



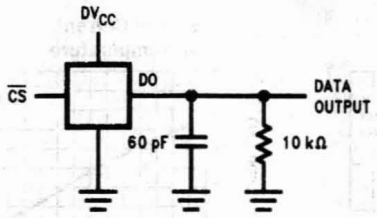
TL/H/11261–3

Line Regulation vs Temperature

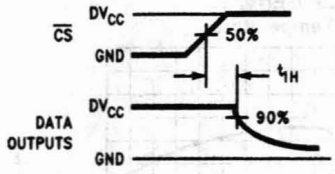


TL/H/11261–4

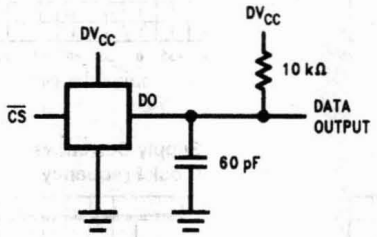
TRI-STATE Test Circuits and Waveforms



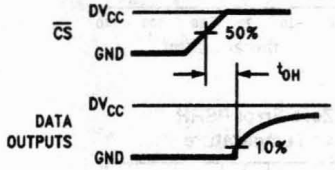
TL/H/11261-5



TL/H/11261-6



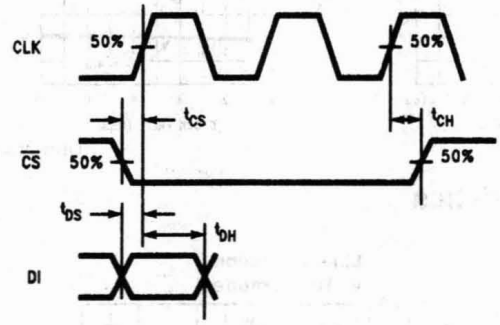
TL/H/11261-7



TL/H/11261-8

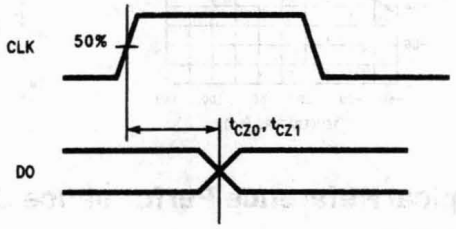
Timing Waveforms

Data Input Timing



TL/H/11261-9

Data Output Timing



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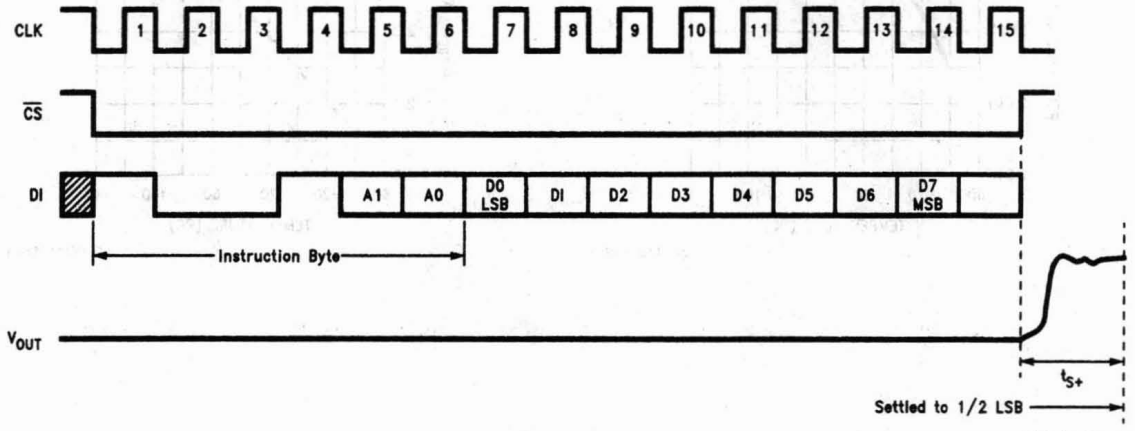
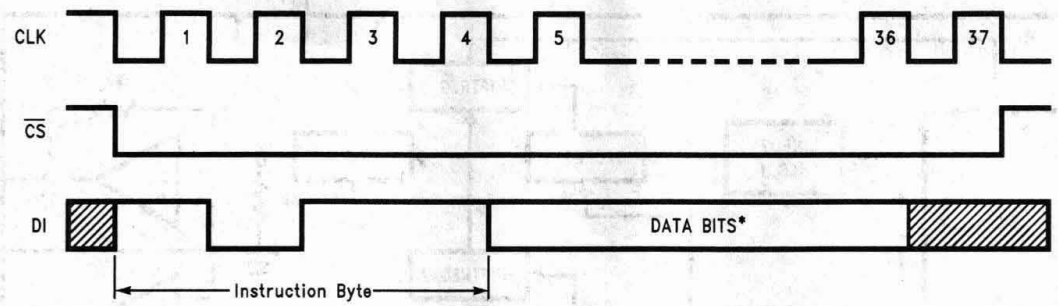
Timing Diagrams



TL/H/11261-11

FIGURE 1. Write to One DAC with Update of Output ($\overline{AU}$ = 1)

Timing Diagrams (Continued)



TL/H/11261–12

* DACs are written to LSB first.
DAC1 is written to first, then DACs 2, 3, and 4.

FIGURE 2. Write to All DACs with Update of Outputs ($\overline{AU}$ = 1)

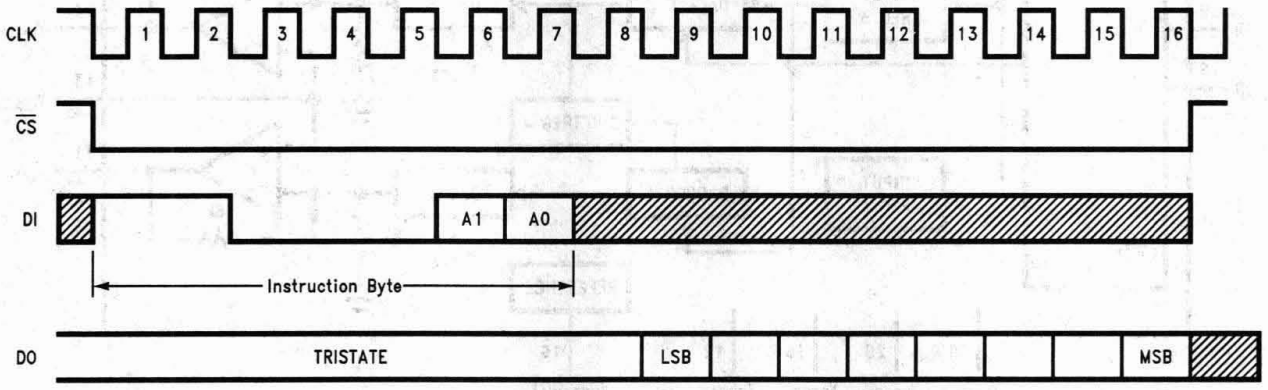


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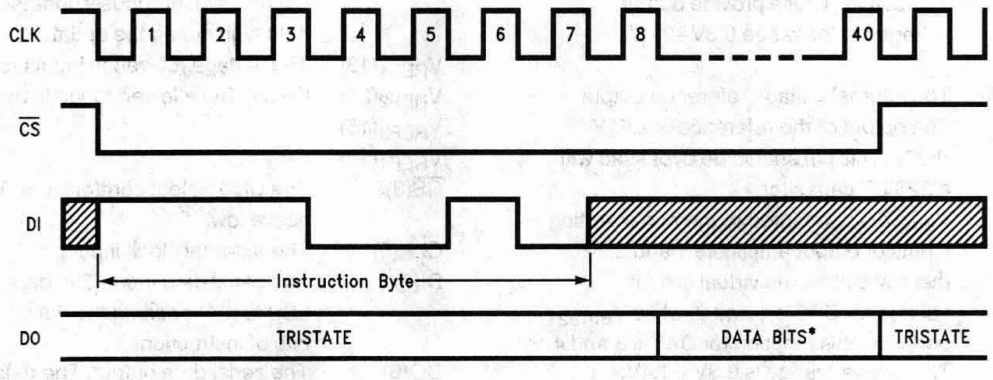
FIGURE 3. Read One DAC, DO Changes on Falling Edge, DO LSB First ($\overline{AU}$ = 1)



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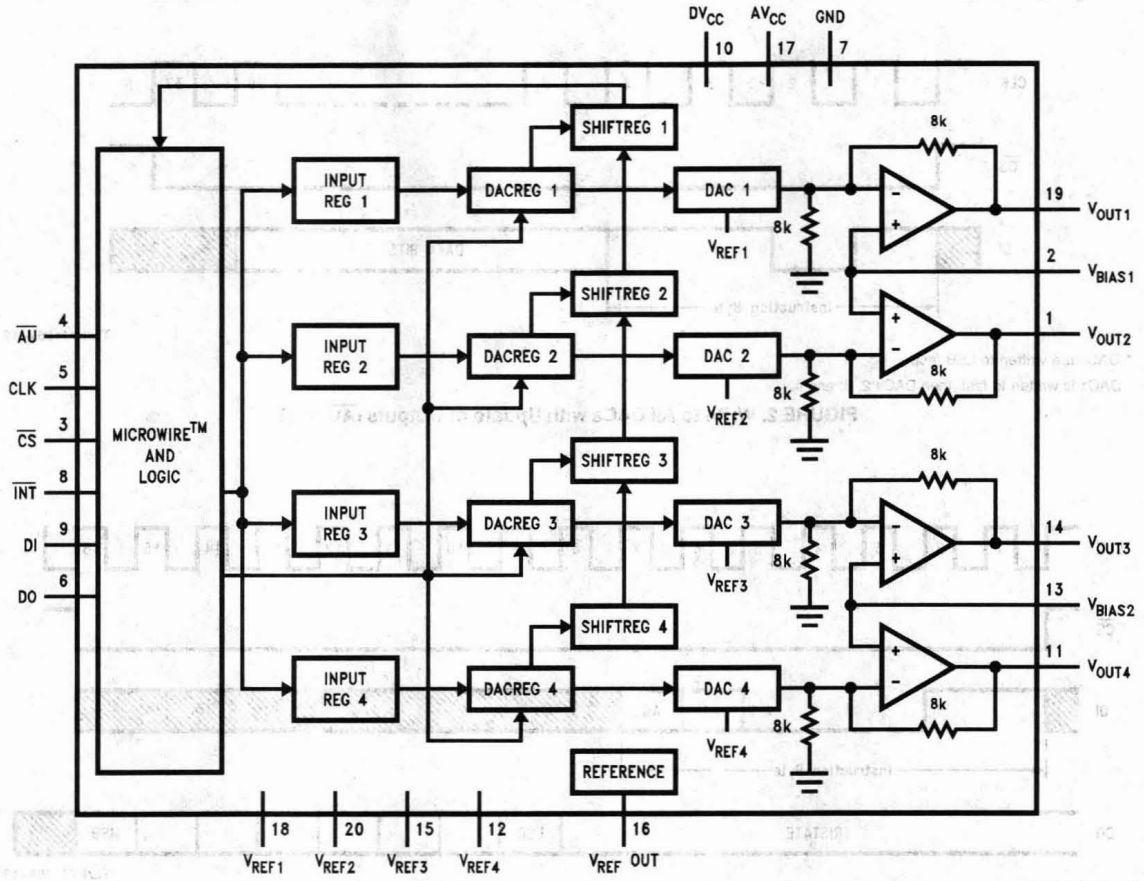
*DAC1 is read first, then DACs 2, 3, and 4.

FIGURE 4. Read All DACs, DO LSB First, DO Changes on Falling Edge ($\overline{AU}$ = 1)

Block Diagram



TL/H/11261–15

Pin Description

V_{OUT1}(19) V_{OUT2}(1) V_{OUT3}(14) V_{OUT4}(11)	The voltage output connections of the four DACS. These provide output voltages in the range 0.3V–2.8V.
V_{REF}OUT(16)	The internal voltage reference output. The output of the reference is 2.65V ±2%. This pin should be bypassed with a 220 μF capacitor.
V_{BIAS1}(2) V_{BIAS2}(13)	V_{BIAS1} is connected to the non-inverting inputs of output amplifiers 1 and 2, thereby setting the virtual ground voltage for DAC's 1 and 2, while V_{BIAS2} performs this function for DAC's 3 and 4. The allowed range is 0.3V –1.4V.
GND(7)	The system ground pin. Connect to clean ground point.
DV_{CC}(10) AV_{CC}(17)	The digital and analog power supply pins. The power supply range of the DAC0854 is 4.5V – 5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} pins be bypassed separately with bypass capacitors of 10 μF tantalum in parallel with 0.1 μF ceramic.
$\overline{AU}$(4)	When this pin is taken low, all DAC outputs will be asynchronously updated. $\overline{CS}$ must be held high during the update.
V_{REF1}(18) V_{REF2}(20) V_{REF3}(15) V_{REF4}(12)	The voltage reference inputs for the four DACs. The allowed range is 0V–2.75V.
$\overline{CS}$(3)	The Chip Select control input. This input is active low.
CLK(5)	The external clock input pin.
DI(9)	The serial data input. The data is clocked in LSB first. Preceding the data byte are 4 or 6 bits of instructions.
DO(6)	The serial data output. The data can be clocked out either MSB or LSB first, and on either the positive or negative edge of the clock.
$\overline{INT}$(8)	The power interrupt output. On an interruption of the power supply, this pin goes low. Since this pin has an open drain output, a 10 kΩ pull-up resistor must be connected to the supply.

Applications Information

FUNCTIONAL DESCRIPTION

The DAC0854 is a monolithic quad 8-bit digital-to-analog converter that is designed to operate on a single 5V supply. Each of the four units is comprised of an input register, a DAC register, a shift register, a current output DAC, and an output amplifier. In addition, the DAC0854 has an onboard bandgap reference and a logic unit which controls the internal operation of the DAC0854 and interfaces it to microprocessors.

Each of the four internal 8-bit DACs uses a modified R-2R ladder to effect the digital-to-analog conversion *(Figure 5)*. The resistances corresponding to the 2 most significant bits are segmented to reduce glitch energy and to improve matching. The bottom of the ladder has been modified so that the voltage across the LSB resistor is much larger than the input offset voltage of the buffer amplifier. The input digital code determines the state of the switches in the ladder network. The sum of currents I_{OUT1} and I_{OUT2} is fixed and is given by

$$I_{OUT1} + I_{OUT2} = \left(\frac{V_{REF} - V_{BIAS}}{R}\right)\frac{255}{256}$$

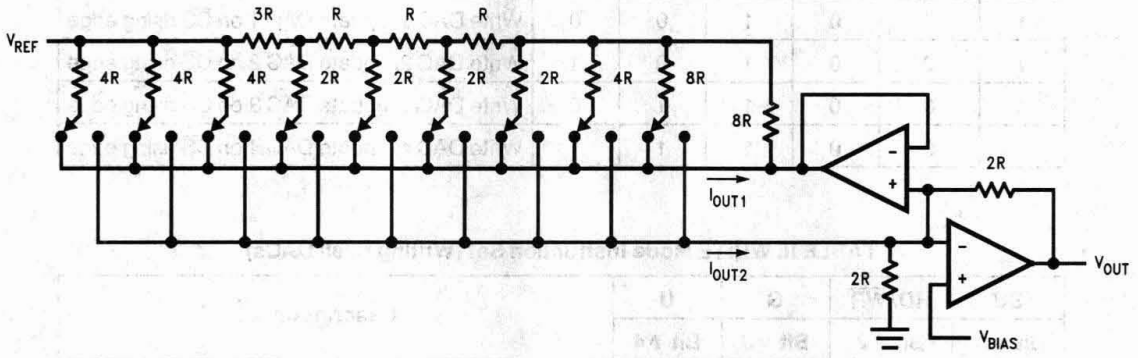
The current output I_{OUT2} is applied to the internal output amplifier and converted to a voltage. The output voltage of each DAC is a function of V_{BIAS}, V_{REF}, and the digital input word, and is given by

$$V_{OUT} = 2\,(V_{REF} - V_{BIAS})\frac{DATA}{256} + \frac{511}{128}V_{BIAS} - \frac{255}{128}V_{REF}$$

The output voltage range for each DAC is 0.3V–2.8V. This range can be achieved by using the internal 2.65V reference and a voltage divider network which provides a V_{BIAS} of 1.40V *(Figure 6)*. In this case the DAC transfer function is

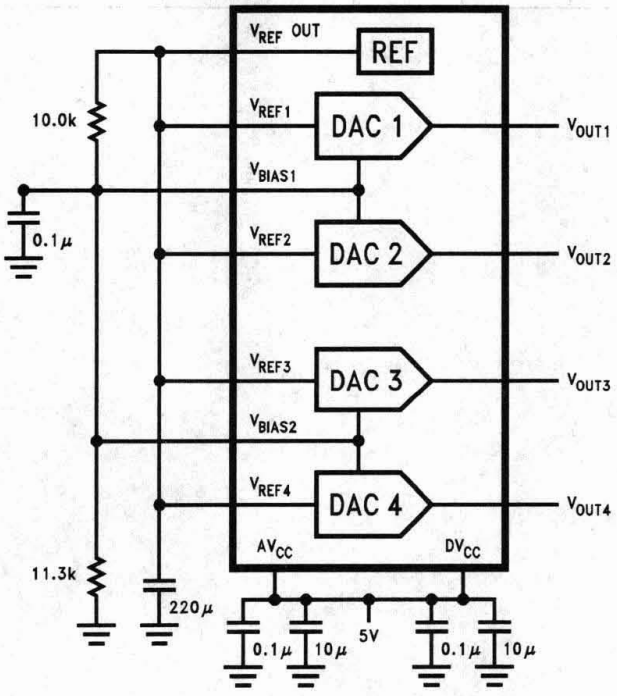
$$V_{OUT} = 2.5\frac{(DATA)}{256} + 0.310$$

The output impedance of any external reference that is used will affect the accuracy of the conversion. In order that this error be less than ½ LSB, the output impedance of the external reference must be less than 7.8Ω.



TL/H/11261–16

FIGURE 5. Equivalent Circuit of R-2R Ladder and Output Amplifier



TL/H/11261–17

FIGURE 6. Generating a V_{BIAS} = 1.40V from the Internal Reference

Digital Interface

The DAC0854 has two interface modes: a WRITE mode and a READ mode. The WRITE mode is used to convert an 8-bit digital input word into a voltage. The READ mode is used to read back the digital data that was sent to one or all of the DACs. These modes are selected by the appropriate setting of the RD/$\overline{WR}$ bit, which is part of the instruction byte. The instruction byte precedes the data byte at the DI pin. In both modes, a high level on the Start Bit (SB) alerts the DAC to respond to the remainder of the input stream.

Table I lists the instruction set for the WRITE mode when writing to only a single DAC, and Table II lists the instruction set for a global write. The DACs are always written to LSB first. All DACs will be written to if the global bit (G) is high; DAC 1 is written to first, then DACs 2, 3 and 4 (in that order). If the update bit is high, then the DAC output will be updated on the rising edge of $\overline{CS}$; otherwise, the new data byte will be placed only in the input register. Chip Select ($\overline{CS}$) must remain low for at least one clock cycle after the last data bit has been entered. (See *Figures 1* and *2*)

TABLE I. WRITE Mode Instruction Set (Writing to a Single DAC)

SB	RD/$\overline{WR}$	G	U	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	
1	0	0	0	0	0	Write DAC 1, no update of DAC outputs
1	0	0	0	0	1	Write DAC 2, no update of DAC outputs
1	0	0	0	1	0	Write DAC 3, no update of DAC outputs
1	0	0	0	1	1	Write DAC 4, no update of DAC outputs
1	0	0	1	0	0	Write DAC 1, update DAC 1 on $\overline{CS}$ rising edge
1	0	0	1	0	1	Write DAC 2, update DAC 2 on $\overline{CS}$ rising edge
1	0	0	1	1	0	Write DAC 3, update DAC 3 on $\overline{CS}$ rising edge
1	0	0	1	1	1	Write DAC 4, update DAC 4 on $\overline{CS}$ rising edge

TABLE II. WRITE Mode Instruction Set (Writing to all DACs)

SB	RD/$\overline{WR}$	G	U	Description
Bit # 1	Bit #2	Bit #3	Bit #4	
1	0	1	0	Write all DACs, no update of outputs
1	0	1	1	Write all DACs, update all outputs on $\overline{CS}$ rising edge

Digital Interface (Continued)

Table III lists the instruction set for the READ mode. By the appropriate setting of the global (G) and address (A1 and A0) bits, one can select a specific DAC to be read, or one can read all the DACs in succession, starting with DAC 1. The R/$\overline{F}$ bit determines whether the data changes on the rising or the falling edge of the system clock. With the R/$\overline{F}$ bit high, the data changes on the rising edge that occurs 1½ clock cycles after the end of the instruction byte. With the R/$\overline{F}$ bit low, the data changes on the falling edge that occurs 1 clock cycle after the end of the instruction byte. One can choose to read the data back MSB first or LSB first by setting the M/$\overline{L}$ bit. (See *Figures 3* and *4*)

An asynchronous update of all the DAC outputs can be achieved by taking $\overline{AU}$ low. The contents of the input registers are loaded into the DAC registers, with the update occurring on the falling edge of $\overline{AU}$. $\overline{CS}$ must be held high during an asynchronous update.

All DAC registers will have their contents reset to all zeros on power up.

TABLE III. READ MODE Instruction Set

SB	RD/$\overline{WR}$	G	R/$\overline{F}$	M/$\overline{L}$	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	Bit #7	
1	1	0	0	0	0	0	Read DAC 1, LSB first, data changes on the falling edge
1	1	0	0	0	0	1	Read DAC 2, LSB first, data changes on the falling edge
1	1	0	0	0	1	0	Read DAC 3, LSB first, data changes on the falling edge
1	1	0	0	0	1	1	Read DAC 4, LSB first, data changes on the falling edge
1	1	0	0	1	0	0	Read DAC 1, MSB first, data changes on the falling edge
1	1	0	0	1	0	1	Read DAC 2, MSB first, data changes on the falling edge
1	1	0	0	1	1	0	Read DAC 3, MSB first, data changes on the falling edge
1	1	0	0	1	1	1	Read DAC 4, MSB first, data changes on the falling edge
1	1	0	1	0	0	0	Read DAC 1, LSB first, data changes on the rising edge
1	1	0	1	0	0	1	Read DAC 2, LSB first, data changes on the rising edge
1	1	0	1	0	1	0	Read DAC 3, LSB first, data changes on the rising edge
1	1	0	1	0	1	1	Read DAC 4, LSB first, data changes on the rising edge
1	1	0	1	1	0	0	Read DAC 1, MSB first, data changes on the rising edge
1	1	0	1	1	0	1	Read DAC 2, MSB first, data changes on the rising edge
1	1	0	1	1	1	0	Read DAC 3, MSB first, data changes on the rising edge
1	1	0	1	1	1	1	Read DAC 4, MSB first, data changes on the rising edge
1	1	1	0	0	1	0	Read all DACs, LSB first, data changes on the falling edge
1	1	1	0	1	1	0	Read all DACs, MSB first, data changes on the falling edge
1	1	1	1	0	1	0	Read all DACs, LSB first, data changes on the rising edge
1	1	1	1	1	1	0	Read all DACs, MSB first, data changes on the rising edge

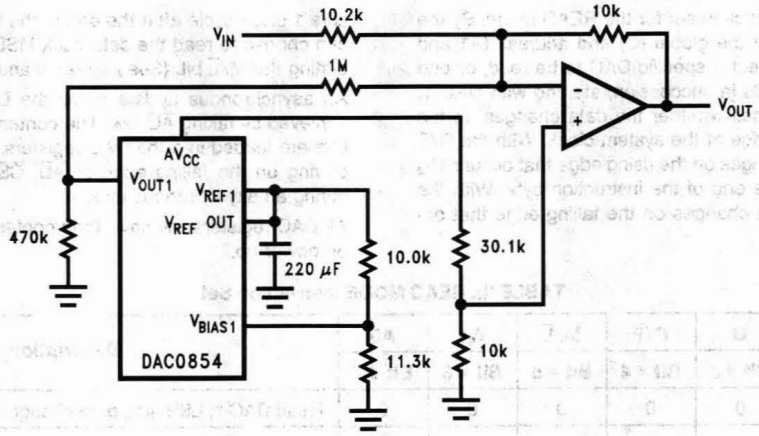
Power Fail Function

If a power failure occurs on the system using the DAC0854 then the $\overline{INT}$ pin will be pulled low on the next power-up cycle. To force this output high again and reset this flag, the $\overline{CS}$ pin will have to be brought low. When this is done the $\overline{INT}$ output will be pulled high again via an external 10 kΩ pull-up resistor. This feature may be used by the microprocessor to discard data whose integrity is in question.

Power Supplies

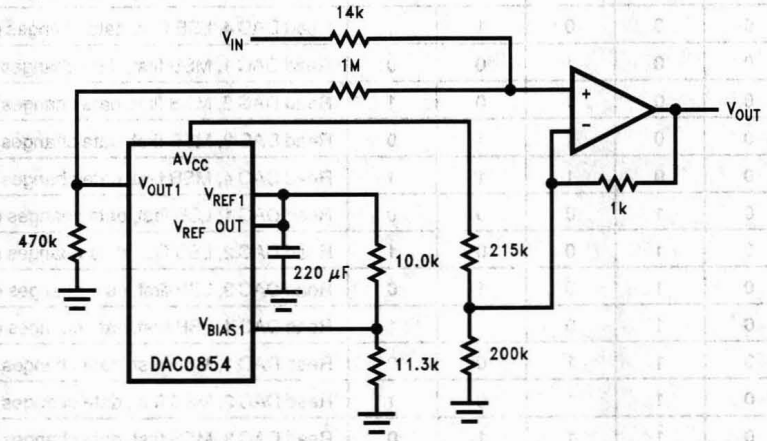
The DAC0854 is designed to operate from a +5V (nominal) supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should each be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

Typical Applications



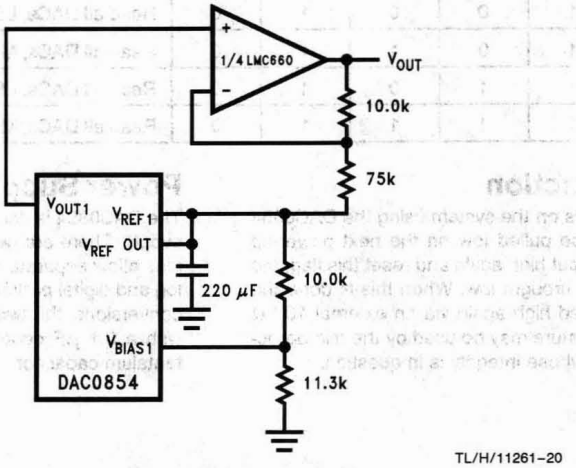
TL/H/11261–18

FIGURE 7. Trimming the Offset of a 5V Op Amp Biased at Mid Supply



TL/H/11261–19

FIGURE 8. Trimming the Offset of a Dual Supply Op Amp Biased at Ground



TL/H/11261–20

FIGURE 9. Bringing the Output Range Down to Ground

National Semiconductor

DAC0890
Dual 8-bit μP-Compatible Digital-to-Analog Converter

General Description

The DAC0890 is a complete dual 8-bit voltage output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, precision bandgap voltage reference, and full microprocessor interface.

Each DAC0890 output amplifier has two externally selectable output ranges, 0V to 2.55V and 0V to 10.2V. The amplifiers are internally trimmed for offset and full-scale accuracy and therefore require no external user trims.

The DAC0890 is supplied in 20-pin ceramic DIP package.

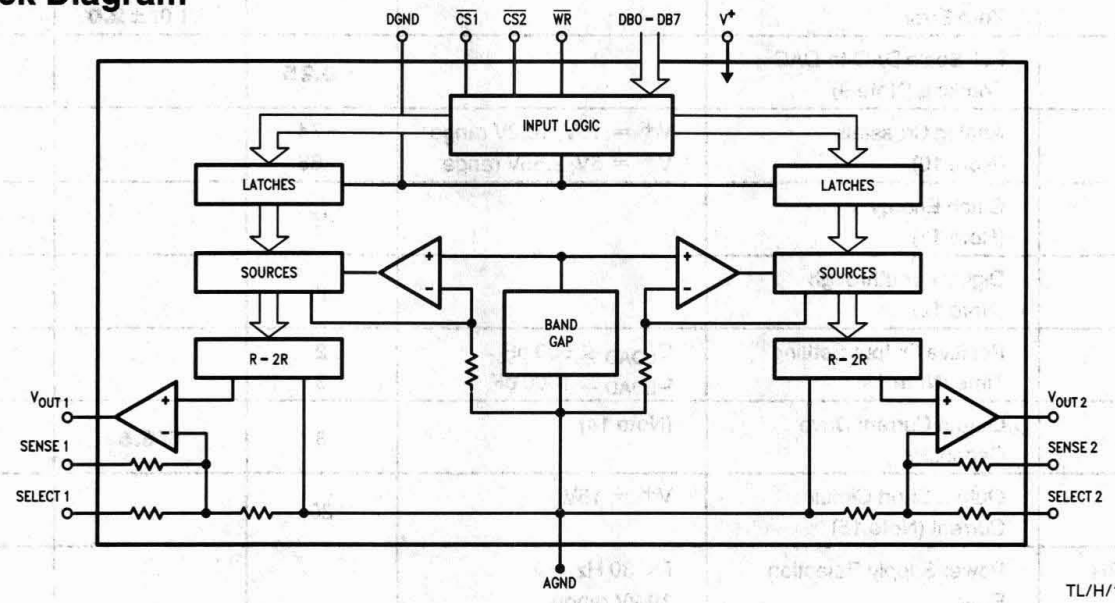
Features

- Two 8-bit voltage output DACs
- 4.75V to 16.5V single operation
- Guaranteed monotonic over temperature
- Internal precision bandgap reference
- Two calibrated output ranges; 2.55V and 10.2V
- 2 μs settling time for full-scale output change
- No external trims
- Microprocessor interface

Applications

- Industrial processing controls
- Automotive controls
- Disk drive motor controls
- Automatic test equipment

Block Diagram



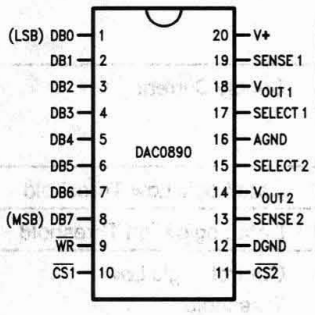
TL/H/10592–1

Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
DAC0890CIJ	J20A Cerdip

Connection Diagram

Dual-In-Line Package



TL/H/10592–2

Top View

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage (V^+)	20V
Voltage at Any Pin (Note 3)	GND −0.3 to V^+ +0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 4)	20 mA
Power Dissipation (Note 5)	1.0W
ESD Susceptability (Note 6)	2000V
Output Short-Circuit Protection Duration	Indefinite
Soldering Information	
J package (10 sec.)	300°C
Storage Temperature	−65°C to 150°C
Junction Temperature	(Note 5)

Operating Ratings (Notes 1 & 2)

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	
DAC0890CIJ	$-40°C \le T_A \le +85°C$
Positive Supply Voltage, V^+	4.75 to 16.5V

Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^+ = +15V$ and AGND = DGND = 0V, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units
	Resolution			**8**	Bits(min)
	Monotonicity			**8**	Bit(min)
	Integral Linearity Error		±0.16	±**0.5**	LSB(min)
	Fullscale Error			±1.5/±**2.5**	LSB(max)
	Zero Error			±1.0/±**2.0**	LSB(max)
	Full Scale DAC-to-DAC Tracking (Note 9)		±**0.25**		LSB
	Analog Crosstalk (Note 10)	$V^+ = 15V$, 10.2V range $V^+ = 5V$, 2.55V range	−74 −66		dB dB
	Glitch Energy (Note 11)		45		V-ns
	Digital Feedthrough (Note 12)		60		V-ns
t_S	Positive Output Settling Time (Note 13)	$C_{LOAD} \le 500$ pF $C_{LOAD} \le 1000$ pF	2 3		µs µs
I_O	Output Current Drive Capability	(Note 14)	8	5/**3.5**	mA(min)
I_{SC}	Output Short Circuit Current (Note 15)	$V^+ = 15V$	20		mA
PSRR	Power Supply Rejection Ratio (Note 16)	f < 30 Hz 10.2V range $13.5V \le V^+ \le 16.5V$	7	**15**	ppm/% (max)
		2.55V range $13.5V \le V^+ \le 16.5V$ $4.75V \le V^+ \le 5.25V$ $4.75V \le V^+ \le 16.5V$	 4 4 4	 **59** **20**	 ppm/% (max) ppm/% (max) ppm/%
I_S	Supply Current	All Inputs Low $V^+ = 16.5$ $V^+ = 4.75$	 25 23	 30/**35**	 mA (max) mA
V_{ILD}	Data Logic Low Threshold			**0.8**	V (max)
V_{IHD}	Data Logic High Threshold			**2.0**	V (min)
V_{ILC}	Control Logic Low Threshold			**0.8**	V (max)

Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$ and $V^+ = +15V$ and AGND = DGND = 0V, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units
V_{IHC}	Control Logic High Threshold			**2.2**	V (min)
	Digital Input Current	(Note 17)	2.2	**25**	μA (max)
t_{WR}	Write Time		18	40	ns (min)
t_{DS}	Data Setup Time		18	35	ns (min)
t_{DH}	Data Hold Time		3		ns (max)
t_{CS}	Control Setup Time		18	40	ns (min)
t_{CH}	Control Hold Time			**0**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ AGND or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The T_{JMAX}(°C) and θ_{JA}(°C/W) for the DAC0890CIJ are 125°C and 53°C/W, respectively.

Part Number	T_{JMAX}(°C)	θ_{JA}(°C/W)
DAC0890CIJ	125	53

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at 25°C, unless otherwise specified, and represent the most likely parametric norm.

Note 8: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Full Scale DAC-to-DAC Tracking is defined as the change in the voltage difference between the full scale output levels of DAC1 and DAC2. The result is expressed in LSBs and it referred to the full-scale voltage difference at 25°C.

Note 10: Analog Crosstalk is a measure of the change in one DAC's full scale output voltage as the second DAC's output voltage changes value. It is measured as the voltage change in one DAC's full scale output voltage divided by the voltage range through which the second DAC's output has changed (zero to full scale). This ratio is then expressed in dB.

Note 11: Glitch Energy is a worst case measurement, over the entire input code range, of transients that occur when changing code. The positive and negative areas of the transient waveforms are summed together to obtain the value listed.

Note 12: Digital Feedthrough is measured with both DAC outputs latched at full scale and a 2 ns, 5V step applied to all 8 data inputs. This gives the worst case digital feedthrough for the DAC0890.

Note 13: Settling Time is specified for a positive full scale step to ±½ LSB. Settling time for negative steps will be slower but may be improved with an external pull-down resistor. Negative settling time to ±½ LSB can be calculated for each range where $t_S = 6.23\ (C_{LOAD})\ (R_{LOAD}/10\ k\Omega)$ for the high range and $t_S = 6.23\ (C_{LOAD})\ (R_{LOAD}/2.5\ k\Omega)$ for the low range.

Note 14: Output Current Drive Capability is the minimum current that can be sourced by the output amplifiers with less than ½ LSB reduction in full scale. Current sinking capability is provided by a passive internal resistance of 10 kΩ in the high range and 2.5 kΩ in the low range.

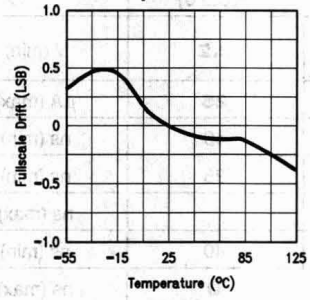
Note 15: Output Short Circuit Current is measured with the output at full-scale and shorted to AGND.

Note 16: Power Supply Rejection Ratio is a measure of how much the output voltage changes (in parts-per-million) per change (in percent) in the power supply voltage.

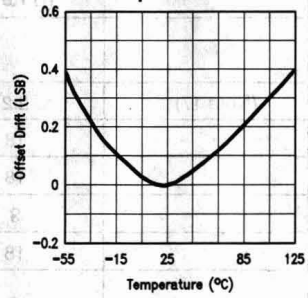
Note 17: Digital Input Current is measured with 0V and V^+ input levels. The limit specified is the higher of these two measurements.

Typical Performance Characteristics

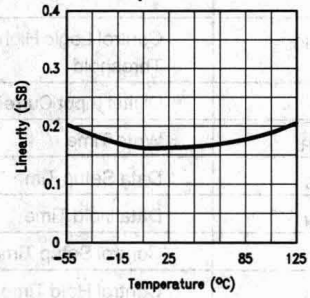
Fullscale Drift vs Temperature



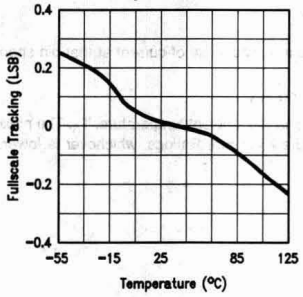
Offset Drift vs Temperature



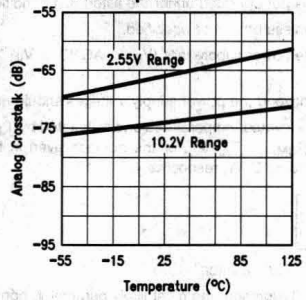
Integral Linearity vs Temperature



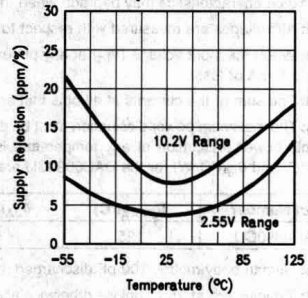
Fullscale Dac to Dac Tracking vs Temperature



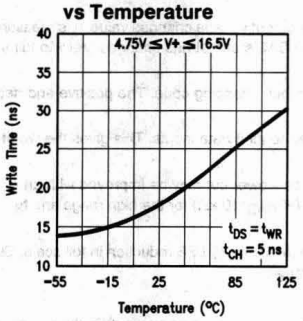
Analog Crosstalk vs Temperature



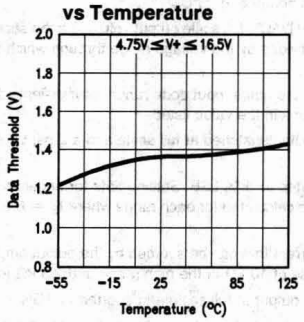
Power Supply Rejection vs Temperature



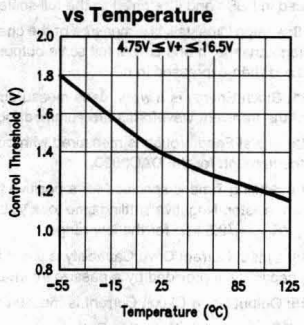
Write Time vs Temperature



Data Threshold vs Temperature



Control Threshold vs Temperature



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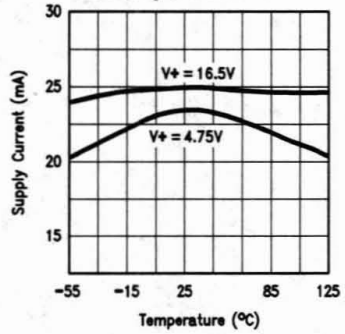
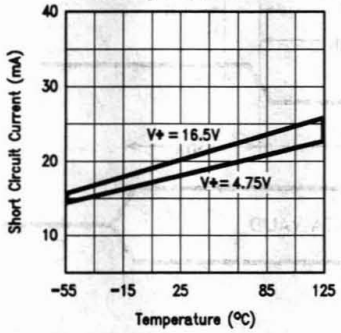
Typical Performance Characteristics

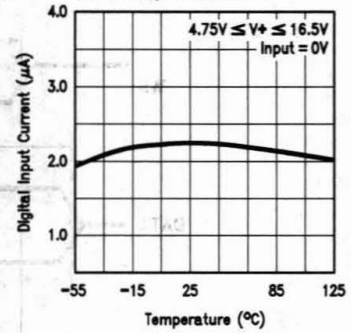
Supply Current vs Temperature



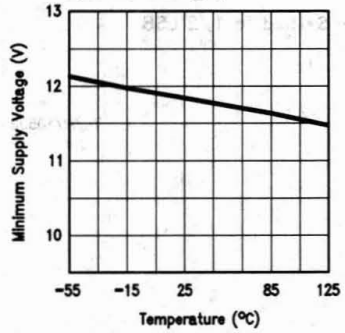
Short Circuit Current vs Temperature



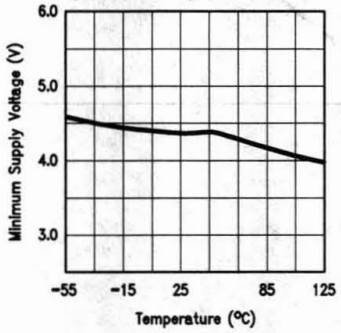
Digital Input Current vs Temperature



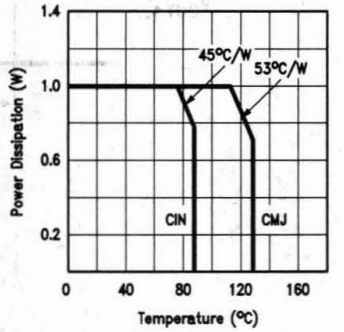
Minimum Supply Voltage vs Temperature (10.2V Range)



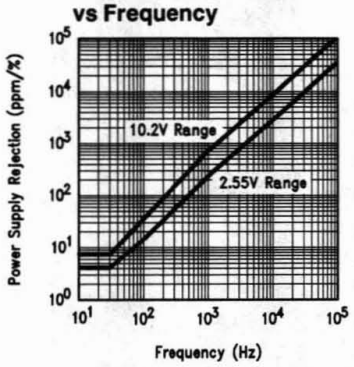
Minimum Supply Voltage vs Temperature (2.55V Range)



Max Power Dissipation vs Temperature



Power Supply Rejection vs Frequency



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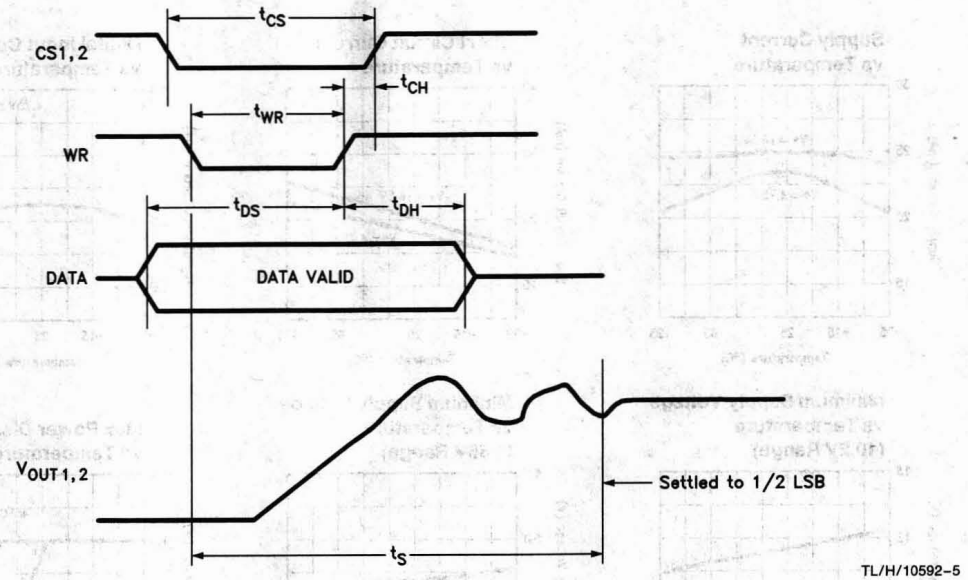
Timing Waveforms



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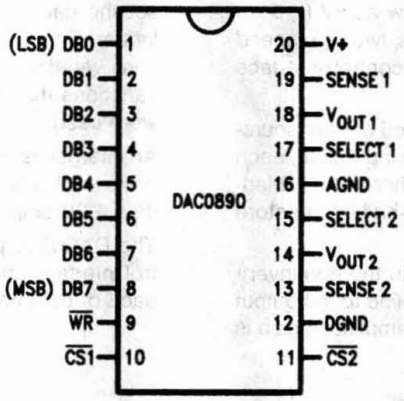
Connection Diagram

Dual-In-Line Package



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Pin Description

DB0–DB7 (1–8) These pins are data inputs for each of the internal 8-bit DACs. DB0 is the least-significant-bit.

$\overline{WR}$ (9) This is the WRITE command input pin. This input is used in conjunction with $\overline{CS1}$ and $\overline{CS2}$ to write data into either of the internal DACs. The data is latched into a selected DAC with the rising edge of either $\overline{WR}$ or $\overline{CS1}$ for DAC1 or $\overline{CS2}$ for DAC2, whichever occurs first.

$\overline{CS1}$ (10) This is the input pin used to select DAC1. This input is used in conjunction with the $\overline{WR}$ input to write data into either of the internal DACs. The data is latched into DAC1 with the rising edge of either CS1 or WR, whichever occurs first.

$\overline{CS2}$ (11) This is the input pin used to select DAC2. This input is used in conjunction with the $\overline{WR}$ input to write data into either of the internal DACs. The data is latched into DAC2 with the rising edge of either $\overline{CS2}$ or $\overline{WR}$, whichever occurs first.

DGND (12) The system digital ground is connected to this pin. For proper operation, this and AGND must be connected together.

SENSE 2 (13) DAC2's output sense connection. When this pin is connected to the VOUT2's load impedance, the feedback loop will compensate for any voltage drops between the VOUT2 pin and the load.

V_{OUT2} (14) DAC2's voltage output connection. It provides two full-scale output voltage ranges, 2.55V and 10.2V.

SELECT 2 (15) The two output voltage ranges available from DAC2 are selected by connecting this pin to SENSE2 for the 2.55V full-scale range and leaving it unconnected for the 10.2V full-scale range.

AGND (16) The system digital ground is connected to this pin. For proper operation, this and DGND must be connected together.

SELECT 1 (17) The two output voltage ranges available from DAC1 are selected by connecting this pin to SENSE1 for he 2.55V full-scale range and leaving it unconnected for the 10.2V full-scale range.

V_{OUT1} (18) DAC1's voltage output connection. It provides two full-scale output voltage ranges, 2.55V and 10.2V.

SENSE 1 (19) DAC1's output sense connection. When this pin is connected to the VOUT1's load impedance, the feedback loop will compensate for any voltage drops between the VOUT1 pin and the load.

V^+ (20) The power supply voltage, ranging from 4.75V to 16.5V, is applied to this pin. It should be bypassed, to AGND, with a 0.01 ~ 0.1 μF ceramic capacitor in parallel with a 2.2 ~ 22 μF electrolytic capacitor.

Functional Description

The DAC0890 is a monolithic dual 8-bit bipolar Digital-to-Analog converter comprising six major functional blocks designed to operate on a single supply as low as 5V (±5%). These include two latch/DAC combinations, two high-speed output amplifiers, band-gap reference, and control/interface logic.

The two internal 8-bit DACs use equal valued current sources. Controlled by a corresponding bit in the input data, each current source's output is switched into either an R/2R ladder or AGND. Each internal DAC has an 8-bit latch to store a digital input. See *Figure 1*.

The high-speed output amplifiers operate in the non-inverting mode. The R-2R's output current is applied to the output amplifier and converted to a voltage. The amplifier's gain is externally set through the range select pin. The two ranges are 0V to 2.55V and 0V to 10.2V. The internal resistors that set the gain are matched to the unit resistor of the R/2R ladder. This ensures that these resistors match over process variations and temperature. This greatly reduces gain variations that would exist if external gain setting resistors were used.

An internal band-gap reference and its control amplifier generate a full scale reference voltage for the DACs. It produces a 1.2V output from a single supply.

The DAC0890 provides a TTL and CMOS-compatible control interface and allows writing and latching digital values to each of the internal DACs.

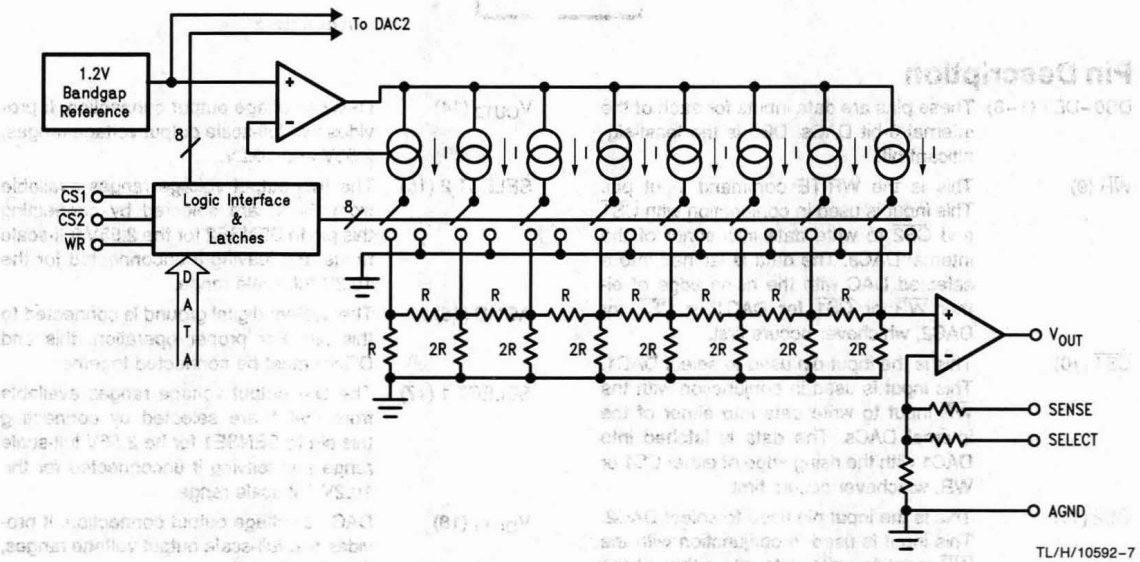


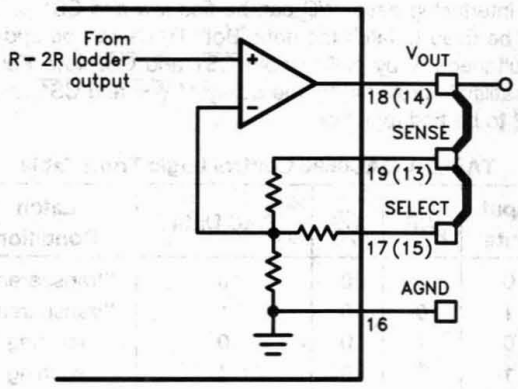
FIGURE 1. Simplified Internal Schematic (One DAC Shown)

Applications Information

Full-Scale Output Voltage Range Selection

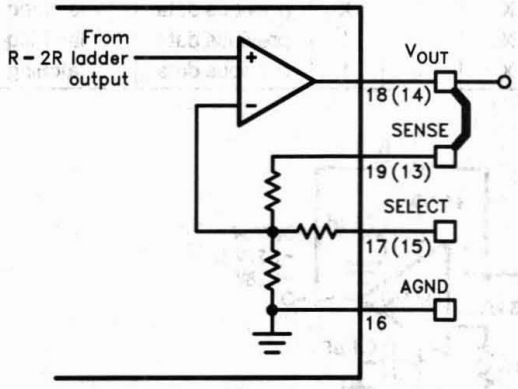
The DAC0890 has been designed for ease of use. All reference voltage and output amplifier connections are internal. All trims such as full-scale (gain) and zero (offset) are performed during manufacturing. Therefore, no external trimming is required to achieve the specified accuracy. The only external connections required select the desired full-scale output voltage range.

The two full-scale output voltage ranges are selected by connecting SENSE, SELECT and VOUT as shown in *Figure 2a, b*. The 2.55V range can be used with supply voltages as low as 4.75V. The 10.2V range can be selected with supplies as low as 12.0V.



TL/H/10592–8

FIGURE 2a. 0V to 2.55V Output Voltage Range



TL/H/10592–9

FIGURE 2b. 0V to 10.2V Output Voltage Range

Power Supply Voltage

The DAC0890 is designed to operate on a single power supply voltages +4.75V and +16.5V. For 2.55V full-scale operation the power supply voltage can be as low as +4.75V. When the 10.2V full-scale is used the supply voltage needs to be between +12V to +16.5V.

Grounding and Power Supply Bypassing

Proper grounding is essential to extract all the precision and full rated performance that the DAC0890 is capable of delivering. Typical applications for the DAC0890 include operation with a microprocessor. In this environment digital noise is prevalent and anticipated. Therefore, special care must be taken to ensure that proper operation will be achieved.

The DAC0890 uses two ground pins, AGND and DGND, to minimize ground drops and noise in the analog signal paths. *Figure 3* details the proper bypassing and ground connections.

The DAC0890's best performance can be ensured by connecting 0.01 μF to 0.1 μF ceramic capacitor in parallel with an electrolytic of 2.2 μF to 22 μF between the V^+ pin and AGND.

Sense Inputs

The SENSE inputs (pins 13 and 19) allow compensation for voltage drops in long output lines to remote loads. This places the drops in the internal amplifier's feedback loop. An example of this is shown in *Figure 3*. The I-R drop, which might be caused by printed circuit board traces or long cables, between the VOUT2 and the load impedance R_L is placed inside the feedback loop if SENSE1 is connected directly to the load. This forces the voltage at the load to be the correct value. It is important to remember that the voltage at the DAC0890's VOUT pins may become higher than the full-scale output voltage selected using the SELECT pins. Therefore, the power supply voltage applied to V^+ must be ≥2.2V above the resulting output voltage (at pins 14 and 18) when the SENSE inputs are used.

The SENSE inputs have a finite input impedance. The range-setting resistors load the output with 2.5 kΩ when the 0V to 2.55V range is selected and 10 kΩ when the 0V to 10.2V range is selected.

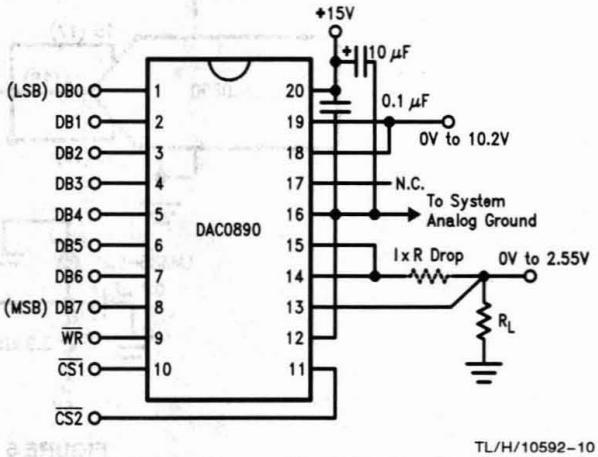


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FIGURE 3. Typical Connection Showing Power Supply Bypassing, and the Use of SENSE Inputs

Minimizing Settling Time

The DAC0890's output stage uses a passive pull-down resistor to achieve single supply operation and an output voltage range that includes ground. This results in a negative-going settling time that is longer than the settling time or positive-going signals. The actual settling time is dependant on the load resistance and capacitance. If available, a negative power supply can be used to improve the negative settling time by connecting a pull down resistor between the output and the negative supply. The resistor's value is chosen so that the current through the pull down resistor is not greater than 0.5 mA when the output voltage is 0V. See *Figure 4*.

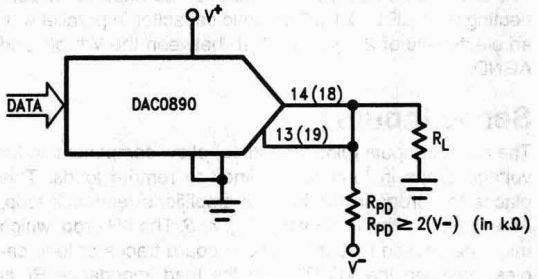

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FIGURE 4. Improving Negative Slew Rate

Bipolar Operation

While the DAC0890 was designed to operate on a single positive supply voltage and generate a unipolar output voltage, bipolar operation is still possible if a negative supply is available or added. As shown in *Figure 5*, the output voltage is offset and scaled to achieve a −1.27V to +1.28V output range with the addition of a −5V supply. The required offset is generated with an LM385–1.2V reference. The external output amplification is provided by the LMC660. The output voltage is generated with a complementary binary offset input code.

Microprocessor Interface

When interfacing with a microprocessor, the DAC0890 appears as a two byte write-only memory location for memory mapped and I/O mapped input-output. Each of the internal DACs is chosen through one of the two chips selects, CS1 or CS2. The action of the control signals is detailed in Table I. The data is latched on the rising edge of either Chip Select or $\overline{WR}$, whichever occurs first for a given selected DAC. For interfacing ease, $\overline{WR}$ can be tied low and $\overline{CS1}$ or $\overline{CS2}$ can be used to latch the data. Both DACs can be updated simultaneously by pulling both $\overline{CS1}$ and $\overline{CS2}$ low. Further versatility is provided by the ability of $\overline{WR}$ and $\overline{CS1}$ and/or $\overline{CS2}$ to be tied together.

TABLE I. DAC0890 Control Logic Truth Table

Input Data	$\overline{WR}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	↑	0	0	latching
1	↑	0	1	latching
0	0	↑	0	latching
1	0	↑	1	latching
X	1	X	previous data	latching
X	X	1	previous data	latching
X	1	1	previous data	latching

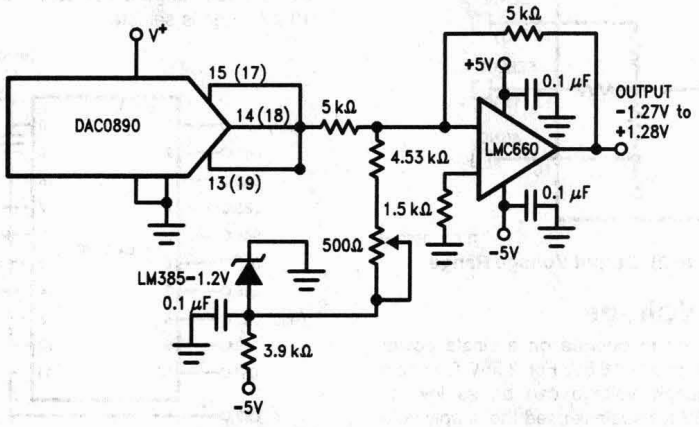

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FIGURE 5. Bipolar Operation

National Semiconductor

DAC1006/DAC1007/DAC1008 μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1006/7/8 are advanced CMOS/Si-Cr 10-, 9- and 8-bit accurate multiplying DACs which are designed to interface directly with the 8080, 8048, 8085, Z-80 and other popular microprocessors. These DACs appear as a memory location or an I/O port to the μP and no interfacing logic is needed.

These devices, combined with an external amplifier and voltage reference, can be used as standard D/A converters; and they are very attractive for multiplying applications (such as digitally controlled gain blocks) since their linearity error is essentially independent of the voltage reference. They become equally attractive in audio signal processing equipment as audio gain controls or as programmable attenuators which marry high quality audio signal processing to digitally based systems under microprocessor control.

All of these DACs are double buffered. They can load all 10 bits or two 8-bit bytes and the data format is left justified. The analog section of these DACs is essentially the same as that of the DAC1020.

The DAC1006 series are the 10-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC™'s). For applications requiring other resolutions, the DAC0830 series (8 bits) and the DAC1208 and DAC1230 (12 bits) are available alternatives.

Part #	Accuracy (bits)	Pin	Description
DAC1006	10	20	For left-justified data
DAC1007	9		
DAC1008	8		

Features

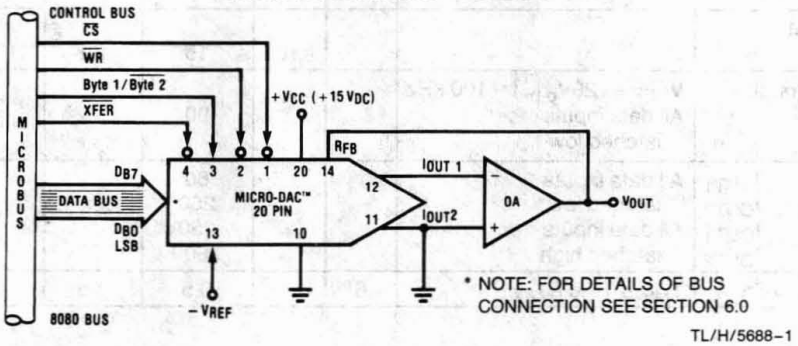
- Uses easy to adjust END POINT specs, NOT BEST STRAIGHT LINE FIT
- Low power consumption
- Direct interface to all popular microprocessors
- Integrated thin film on CMOS structure
- Double-buffered, single-buffered or flow through digital data inputs
- Loads two 8-bit bytes or a single 10-bit word
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates STAND ALONE (without μP) if desired
- Available in 0.3" standard 20-pin package
- Differential non-linearity selection available as special order

Key Specifications

■ Output Current Settling Time	500 ns
■ Resolution	10 bits
■ Linearity	10, 9, and 8 bits (guaranteed over temp.)
■ Gain Tempco	−0.0003% of FS/°C
■ Low Power Dissipation (including ladder)	20 mW
■ Single Power Supply	5 to 15 V_{DC}

Typical Application

DAC1006/1007/1008



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3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptibility (Note 11)	800V
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Part numbers with "LCN" and "LCWN" suffix	0°C to 70°C
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

Tested at V_{CC} = 4.75 V_{DC} and 15.75 V_{DC}, T_A = 25°C, V_{REF} = 10.000 V_{DC} unless otherwise noted

Parameter	Conditions	See Note	V_{CC} = 12V_{DC} ±5% to 15V_{DC} ±5%			V_{CC} = 5V_{DC} ±5%			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution					10			10	bits
Linearity Error	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1006				0.05			0.05	% of FSR
	DAC1007				0.1			0.1	% of FSR
	DAC1008				0.2			0.2	% of FSR
Differential Nonlinearity	Endpoint adjust only	4,7							
	$T_{MIN} < T_A < T_{MAX}$	6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1006				0.1			0.1	% of FSR
	DAC1007				0.2			0.2	% of FSR
	DAC1008				0.4			0.4	% of FSR
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6							
	$-10V \le V_{REF} \le +10V$	5							
	DAC1006		10			10			bits
	DAC1007		9			9			bits
	DAC1008		8			8			bits
Gain Error	Using internal R_{fb}								
	$-10V \le V_{REF} \le +10V$	5	−1.0	±0.3	1.0	−1.0	±0.3	1.0	% of FS
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6							
	Using internal R_{fb}	9		−0.0003	−0.001		−0.0006	−0.002	% of FS/°C
Power Supply Rejection	All digital inputs latched high								
	V_{CC} = 14.5V to 15.5V			0.003	0.008				% FSR/V
	11.5V to 12.5V			0.004	0.010				% FSR/V
	4.75V to 5.25V						0.033	0.10	% FSR/V
Reference Input Resistance			10	15	20	10	15	20	kΩ
Output Feedthrough Error	V_{REF} = 20V_{p-p}, f = 100 kHz All data inputs latched low			90			90		mV_{p-p}
Output Capacitance I_{OUT1}	All data inputs latched low			60			60		pF
I_{OUT2}				250			250		pF
I_{OUT1}	All data inputs latched high			250			250		pF
I_{OUT2}				60			60		pF
Supply Current Drain	$T_{MIN} \le T_A \le T_{MAX}$	6		0.5	3.5		0.5	3.5	mA

Electrical Characteristics

Tested at V_{CC} = 4.75 V_{DC} and 15.75 V_{DC}, T_A = 25°C, V_{REF} = 10.000 V_{DC} unless otherwise noted (Continued)

Parameter	Conditions	See Note	V_{CC} = 12V_{DC} ± 5% to 15V_{DC} ± 5%			V_{CC} = 5V_{DC} ± 5%			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current I_{OUT1}	$T_{MIN} \le T_A \le T_{MAX}$ All data inputs latched low	6 10			200			200	nA
I_{OUT2}	All data inputs latched high				200			200	nA
Digital Input Voltages	$T_{MIN} \le T_A \le T_{MAX}$ Low level	6							
	LCN and LCWM suffix				0.8, 0.8			0.7, 0.8	V_{DC}
	High level (all parts)		2.0			2.0			V_{DC}
Digital Input Currents	$T_{MIN} \le T_A \le T_{MAX}$	6							
	Digital inputs <0.8V			−40	−150		−40	−150	μA_{DC}
	Digital inputs >2.0V			1.0	+10		1.0	+10	μA_{DC}
Current Settling Time t_S	V_{IL} = 0V, V_{IH} = 5V			500			500		ns
Write and $\overline{XFER}$ Pulse Width t_W	V_{IL} = 0V, V_{IH} = 5V,								
	T_A = 25°C	8	150	60		320	200		ns
	$T_{MIN} \le T_A \le T_{MAX}$	9	320	100		500	250		ns
Data Set Up Time t_{DS}	V_{IL} = 0V, V_{IH} = 5V,								
	T_A = 25°C	9	150	80		320	170		ns
	$T_{MIN} \le T_A \le T_{MAX}$		320	120		500	250		ns
Data Hold Time t_{DH}	V_{IL} = OV, V_{IH} = 5V								
	T_A = 25°C	9	200	100		320	220		ns
	$T_{MIN} \le T_A \le T_{MAX}$		250	120		500	320		ns
Control Set Up Time t_{CS}	V_{IL} = 0V, V_{IL} = 5V,								
	T_A = 25°C	9	150	60		320	180		ns
	$T_{MIN} \le T_A \le T_{MAX}$		320	100		500	260		ns
Control Hold Time t_{CH}	V_{IL} = 0V, V_{IH} = 5V,								
	T_A = 25°C	9	10	0		10	0		ns
	$T_{MIN} \le T_A \le T_{MAX}$		10	0		10	0		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at V_{REF} = ±10 V_{DC} and V_{REF} = ±1 V_{DC}.

Note 6: T_{MIN} = 0°C and T_{MAX} = 70°C for "LCN" and "LCWM" suffix parts.

Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC1006 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6), the plot of the 1024 analog voltage outputs will each be within 0.05% × V_{REF} of a straight line which passes through zero and full scale.

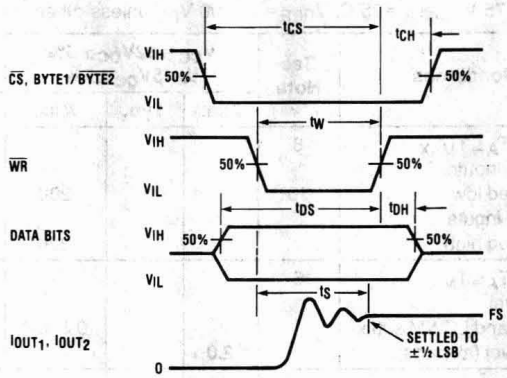
Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: Guaranteed by design but not tested.

Note 10: A 200 nA leakage current with R_{fb} = 20K and V_{REF} = 10V corresponds to a zero error of $(200 \times 10^{-9} \times 20 \times 10^3) \times 100 \div 10$ which is 0.04% of FS.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Waveforms



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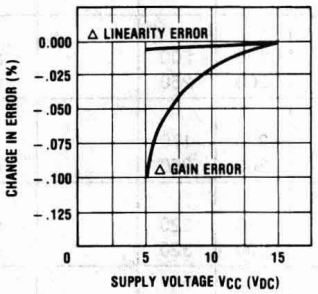
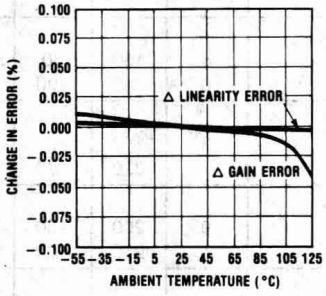
Typical Performance Characteristics

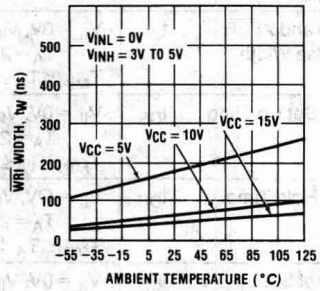
Errors vs. Supply Voltage



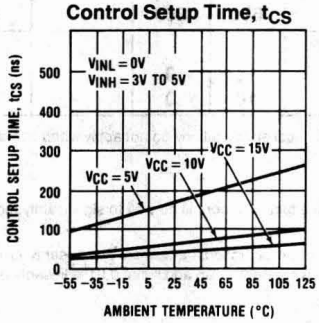
Errors vs. Temperature



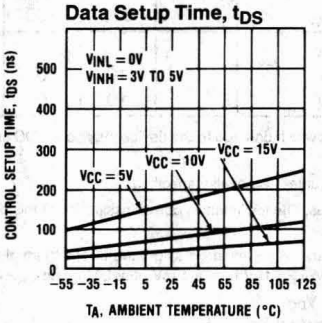
Write Width, t_W



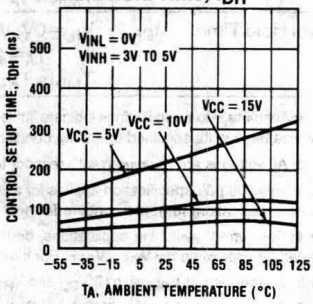
Control Setup Time, t_{CS}



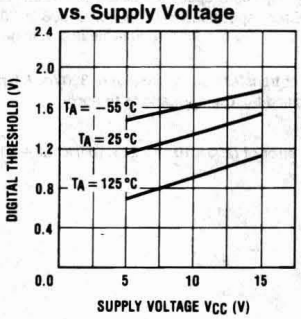
Data Setup Time, t_{DS}



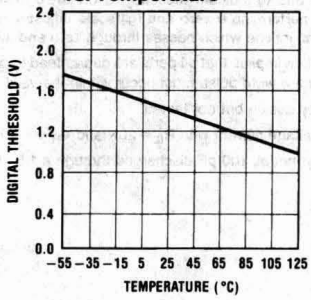
Data Hold Time, t_{DH}



Digital Threshold vs. Supply Voltage



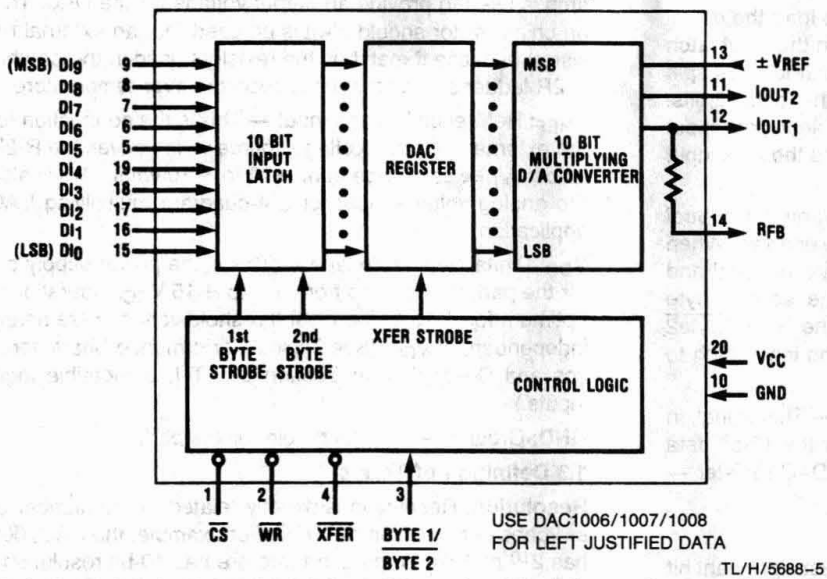
Digital Input Threshold vs. Temperature



TL/H/5688–3

Block and Connection Diagrams

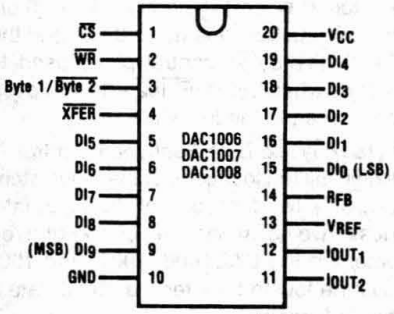
DAC1006/1007/1008 (20-Pin Parts)



USE DAC1006/1007/1008
FOR LEFT JUSTIFIED DATA

TL/H/5688–5

DAC1006/1007/1008
(20-Pin Parts)
Dual-In-Line Package

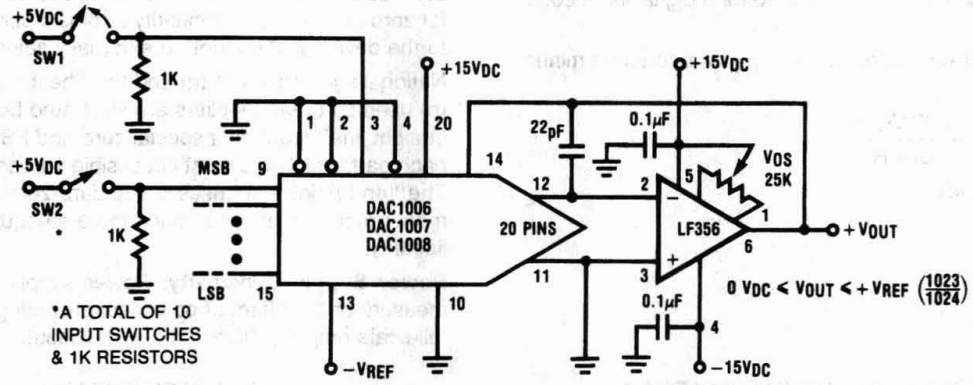


TL/H/5688–28

Top View

See Ordering Information

DAC1006/1007/1008—Simple Hookup for a "Quick Look"



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Notes:

1. For $V_{REF} = -10.240\ V_{DC}$ the output voltage steps are approximately 10 mV each.
2. SW1 is a normally closed switch. While SW1 is closed, the DAC register is latched and new data can be loaded into the input latch via the 10 SW2 switches.

When SW1 is momentarily opened the new data is transferred from the input latch to the DAC register and is latched when SW1 again closes.

1.0 DEFINITION OF PACKAGE PINOUTS

1.1 Control Signals (All control signals are level actuated.)

$\overline{CS}$: Chip Select — active low, it will enable $\overline{WR}$.

$\overline{WR}$: Write — The active low $\overline{WR}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR}$ is high. The 10-bit input latch is split into two latches; one holds 8 bits and the other holds 2 bits. The Byte1/$\overline{Byte2}$ control pin is used to select both input latches when Byte1/$\overline{Byte2}$ = 1 or to overwrite the 2-bit input latch when in the low state.

Byte1/$\overline{Byte2}$: Byte Sequence Control — When this control is high, all ten locations of the input latch are enabled. When low, only two locations of the input latch are enabled and these two locations are overwritten on the second byte write. On the DAC1006, 1007, and 1008, the Byte1/$\overline{Byte2}$ must be low to transfer the 10-bit data in the input latch to the DAC register.

$\overline{XFER}$: Transfer Control Signal, active low — This signal, in combination with others, is used to transfer the 10-bit data which is available in the input latch to the DAC register — see timing diagrams.

1.2 Other Pin Functions

DI_i (i = 0 to 9): Digital Inputs — DI_0 is the least significant bit (LSB) and DI_9 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1 — I_{OUT1} is a maximum for a digital input code of all 1s and is zero for a digital input code of all 0s.

I_{OUT2}: DAC Current Output 2 — I_{OUT2} is a constant minus I_{OUT1}, or

$$I_{OUT1} + I_{OUT2} = \frac{1023\ V_{REF}}{1024\ R}$$

where R ≅ 15 kΩ.

R_{FB}: Feedback Resistor — This is provided on the IC chip for use as the shunt feedback resistor when an external op amp is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) because it matches the resistors used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input — This is the connection for the external precision voltage source which drives the R-2R ladder. V_{REF} can range from −10 to +10 volts. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage — This is the power supply pin for the part. V_{CC} can be from +5 to +15 V_{DC}. Operation is optimum for +15V. The input threshold voltages are nearly independent of V_{CC}. (See Typical Performance Characteristics and Description in Section 3.0, T^2L compatible logic inputs.)

GND: Ground — the ground pin for the part.

1.3 Definition of Terms

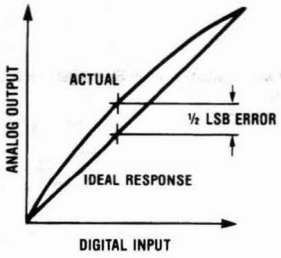
Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC1006 has 2^{10} or 1024 steps and therefore has 10-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

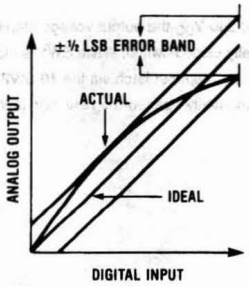
National's linearity test (a) and the "best straight line" test (b) used by other suppliers are illustrated below. The "best straight line" requires a special zero and FS adjustment for each part, which is almost impossible for user to determine. The "end point test" uses a standard zero and FS adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output (which is the worst case).

a. End Point Test After Zero and FS Adj.



b. Best Straight Line



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Settling Time: Settling time is the time required from a code transition until the DAC output reaches within $\pm 1/2$ LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1006 series, full-scale is $V_{REF}-1$ LSB. For $V_{REF}=-10V$ and unipolar operation, $V_{FULL\text{-}SCALE}=10.0000V-9.8mV=9.9902V$. Full-scale error is adjustable to zero.

Monotonicity: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 10-bit DAC with 10-bit monotonicity will produce an increasing analog output when all 10 digital inputs are exercised. A 10-bit DAC with 9-bit monotonicity will be monotonic when only the most significant 9 bits are exercised. Similarly, 8-bit monotonicity is guaranteed when only the most significant 8 bits are exercised.

2.0 DOUBLE BUFFERING

These DACs are double-buffered, microprocessor compatible versions of the DAC1020 10-bit multiplying DAC. The addition of the buffers for the digital input data not only allows for storage of this data, but also provides a way to assemble the 10-bit input data word from two write cycles when using an 8-bit data bus. Thus, the next data update for the DAC output can be made with the complete new set of 10-bit data. Further, the double buffering allows many DACs in a system to store current data and also the next data. The updating of the new data for each DAC is also not time critical. When all DACs are updated, a common strobe signal can then be used to cause all DACs to switch to their new analog output levels.

3.0 TTL COMPATIBLE LOGIC INPUTS

To guarantee TTL voltage compatibility of the logic inputs, a novel bipolar (NPN) regulator circuit is used. This makes the input logic thresholds equal to the forward drop of two diodes (and also matches the temperature variation) as occurs naturally in TTL. The basic circuit is shown in *Figure 1*. A curve of digital input threshold as a function of power supply voltage is shown in the Typical Performance Characteristics section.

4.0 APPLICATION HINTS

The DC stability of the V_{REF} source is the most important factor to maintain accuracy of the DAC over time and temperature changes. A good single point ground for the analog signals is next in importance.

These MICRO-DAC converters are CMOS products and reasonable care should be exercised in handling them prior to final mounting on a PC board. The digital inputs are protected, but permanent damage may occur if the part is subjected to high electrostatic fields. Store unused parts in conductive foam or anti-static rails.

4.1 Power Supply Sequencing & Decoupling

Some IC amplifiers draw excessive current from the Analog inputs to V− when the supplies are first turned on. To prevent damage to the DAC — an external Schottky diode connected from I_{OUT1} or I_{OUT2} to ground may be required to prevent destructive currents in I_{OUT1} or I_{OUT2}. If an LM741 or LF356 is used — these diodes are not required.

The standard power supply decoupling capacitors which are used for the op amp are adequate for the DAC.

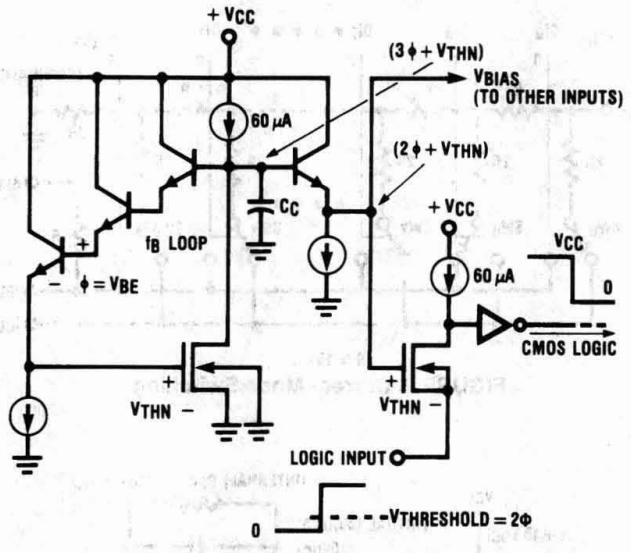

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FIGURE 1. Basic Logic Threshold Loop

4.2 Op Amp Bias Current & Input Leads

The op amp bias current (I_B) CAN CAUSE DC ERRORS. BI-FET™ op amps have very low bias current, and therefore the error introduced is negligible. BI-FET op amps are strongly recommended for these DACs.

The distance from the I_{OUT1} pin of the DAC to the inverting input of the op amp should be kept as short as possible to prevent inadvertent noise pickup.

5.0 ANALOG APPLICATIONS

The analog section of these DACs uses an R-2R ladder which can be operated both in the current switching mode and in the voltage switching mode.

The major product changes (compared with the DAC1020) have been made in the digital functioning of the DAC. The analog functioning is reviewed here for completeness. For additional analog applications, such as multipliers, attenuators, digitally controlled amplifiers and low frequency sine wave oscillators, refer to the DAC1020 data sheet. Some basic circuit ideas are presented in this section in addition to complete applications circuits.

5.1 Operation in Current Switching Mode

The analog circuitry, *Figure 2*, consists of a silicon-chromium (Si-Cr) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there is no parasitic diode connected to the V_{REF} pin as would exist if diffused resistors were used. The reference voltage input (V_{REF}) can therefore range from −10V to +10V.

The digital input code to the DAC simply controls the position of the SPDT current switches, SW0 to SW9. A logical 1 digital input causes the current switch to steer the available ladder current to the I_{OUT1} output pin. These MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

5.1.1 Providing a Unipolar Output Voltage with the DAC in the Current Switching Mode

A voltage output is provided by making use of an external op amp as a current-to-voltage converter. The idea is to use the internal feedback resistor, R_{FB}, from the output of the op amp to the inverting (−) input. Now, when current is entered at this inverting input, the feedback action of the op amp keeps that input at ground potential. This causes the applied input current to be diverted to the feedback resistor. The output voltage of the op amp is forced to a voltage given by:

$$V_{OUT} = -(I_{OUT1} \times R_{FB})$$

Notice that the sign of the output voltage depends on the direction of current flow through the feedback resistor.

In current switching mode applications, both current output pins (I_{OUT1} and I_{OUT2}) should be operated at 0 V_{DC}. This is accomplished as shown in *Figure 3*. The capacitor, C_C, is used to compensate for the output capacitance of the DAC and the input capacitance of the op amp. The required feedback resistor, R_{FB}, is available on the chip (one end is internally tied to I_{OUT1}) and must be used since an external resistor will not provide the needed matching and temperature tracking. This circuit can therefore be simplified as

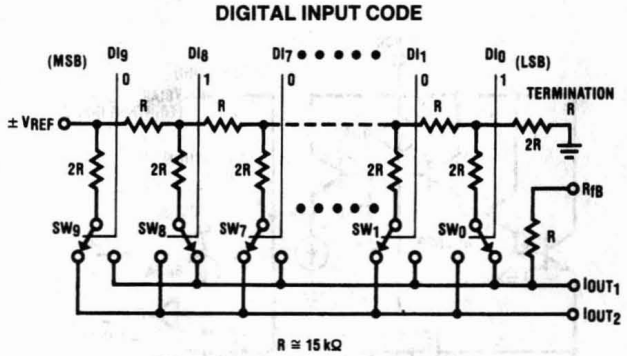

FIGURE 2. Current Mode Switching

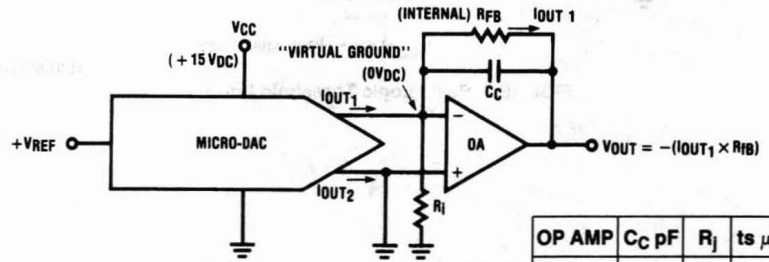

FIGURE 3. Converting I_{OUT} to V_{OUT}

OP AMP	C_C pF	R_j	ts μS
LF356	22	∞	3
LF351	24	∞	4
LF357	10	2.4k	1.5

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shown in *Figure 4*, where the sign of the reference voltage has been changed to provide a positive output voltage. Note that the output current, I_{OUT1}, now flows through the R_{FB} pin.

5.1.2 Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

The addition of a second op amp to the circuit of *Figure 4* can be used to generate a bipolar output voltage from a fixed reference voltage *Figure 5*. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize the full four-quadrant multiplication.

The applied digital word is offset binary which includes a code to output zero volts without the need of a large valued resistor common to existing bipolar multiplying DAC circuits. Offset binary code can be derived from 2's complement data (most common for signed processor arithmetic) by inverting the state of the MSB in either software or hardware. After doing this the output then responds in accordance to the following expression:

$$V_O = V_{REF} \times \frac{D}{512}$$

where V_{REF} can be positive or negative and D is the signed decimal equivalent of the 2's complement processor data. ($-512 \le D \le +511$ or $1000000000 \le D \le 0111111111$). If the applied digital input is interpreted as the decimal equivalent of a true binary word, V_{OUT} can be found by:

$$V_O = V_{REF}\left(\frac{D-512}{512}\right) \qquad 0 \le D \le 1023$$

With this configuration, only the offset voltage of amplifier 1 need be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp has no effect on linearity. It presents a constant output voltage error and should be nulled only if absolute accuracy is needed. Another advantage of this configuration is that the values of the external resistors required do not have to match the value of the internal DAC resistors; they need only to match and temperature track each other.

A thin film 4 resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four available 10 kΩ resistor can be paralleled to form R in *Figure 5* and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

2's Comp. (Decimal)	2's Comp. (Binary)	Applied Digital Input	Applied True Binary (Decimal)	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
+511	0111111111	1111111111	1023	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
+256	0100000000	1100000000	768	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
0	0000000000	1000000000	512	0	0
−1	1111111111	0111111111	511	−1 LSB	+1 LSB
−256	1100000000	0100000000	256	$-V_{REF}/2$	$+\lvert V_{REF}\rvert/2$
−512	1000000000	0000000000	0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

with: $1\ LSB = \frac{|V_{REF}|}{512}$

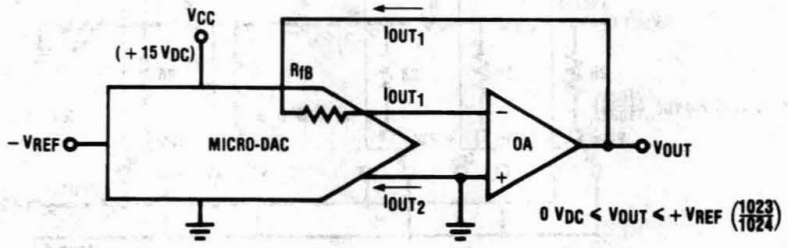

FIGURE 4. Providing a Unipolar Output Voltage

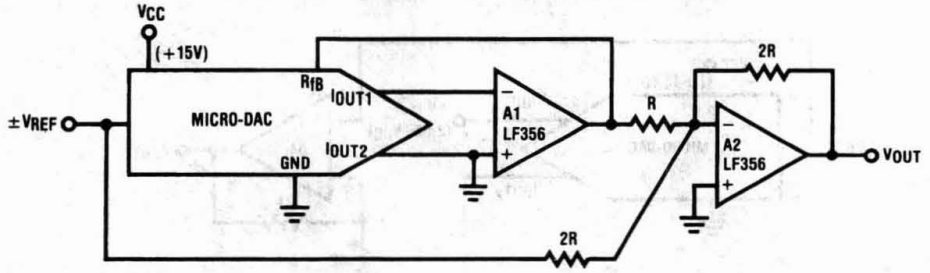

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FIGURE 5. Providing a Bipolar Output Voltage with the DAC in the Current Switching Mode

5.2 Analog Operation in the Voltage Switching Mode

Some useful application circuits result if the R-2R ladder is operated in the voltage switching mode. There are two very important things to remember when using the DAC in the voltage mode. The reference voltage (+V) must always be positive since there are parasitic diodes to ground on the I_{OUT1} pin which would turn on if the reference voltage went negative. To maintain a degradation of linearity less than ±0.005%, keep $+V \leq 3\ V_{DC}$ and V_{CC} at least 10V more positive than +V. *Figures 6* and *7* show these errors for the voltage switching mode. This operation appears unusual, since a reference voltage (+V) is applied to the I_{OUT1} pin and the voltage output is the V_{REF} pin. This basic idea is shown in *Figure 8*.

This V_{OUT} range can be scaled by use of a non-inverting gain stage as shown in *Figure 9*.

Notice that this is unipolar operation since all voltages are positive. A bipolar output voltage can be obtained by using a single op amp as shown in *Figure 10*. For a digital input code of all zeros, the output voltage from the V_{REF} pin is zero volts. The external op amp now has a single input of +V and is operating with a gain of −1 to this input. The output of the op amp therefore will be at −V for a digital input of all zeros. As the digital code increases, the output voltage at the V_{REF} pin increases.

Notice that the gain of the op amp to voltages which are applied to the (+) input is +2 and the gain to voltages which are applied to the input resistor, R, is −1. The output voltage of the op amp depends on both of these inputs and is given by:

$$V_{OUT} = (+V)(-1) + V_{REF}(+2)$$

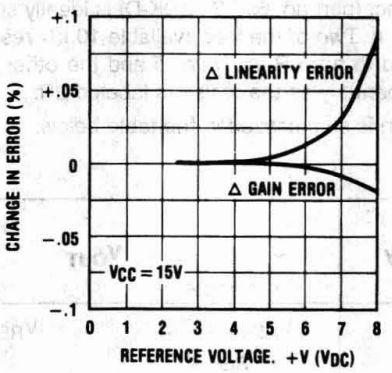

FIGURE 6

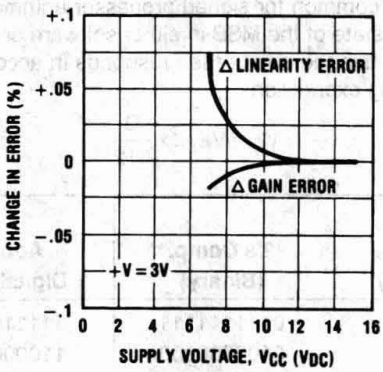

FIGURE 7

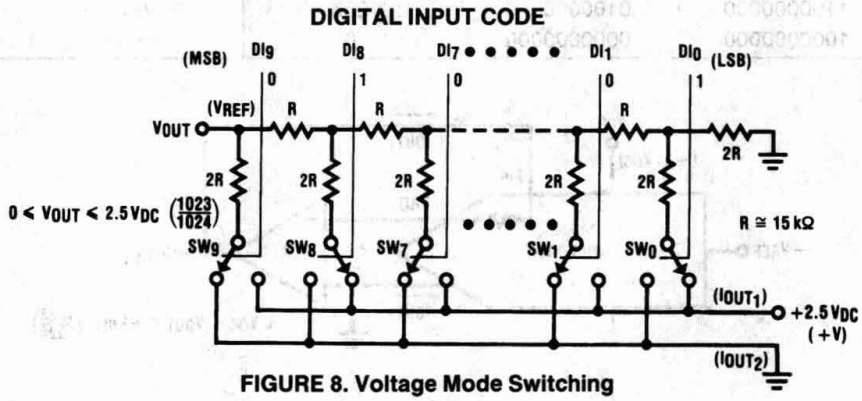

FIGURE 8. Voltage Mode Switching

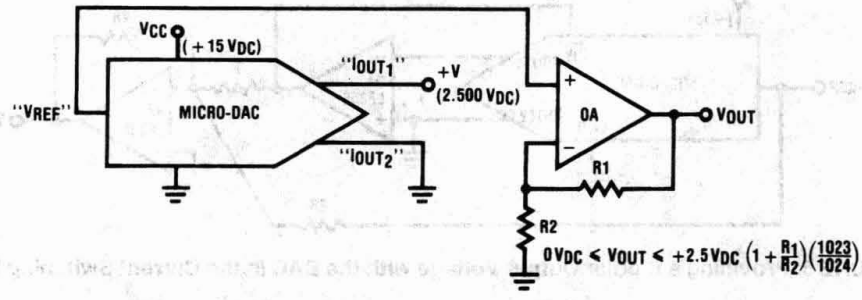

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FIGURE 9. Amplifying the Voltage Mode Output (Single Supply Operation)

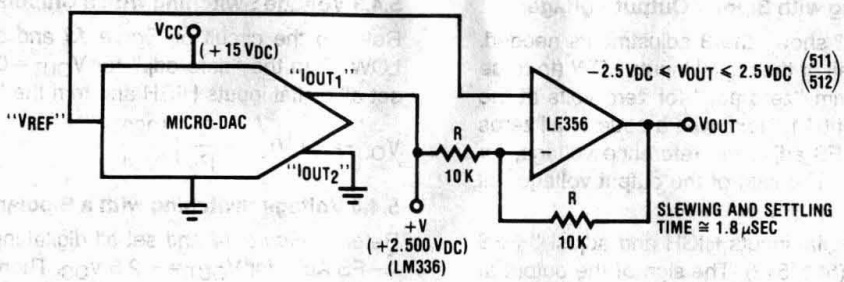

FIGURE 10. Providing a Bipolar Output Voltage with a Single Op Amp

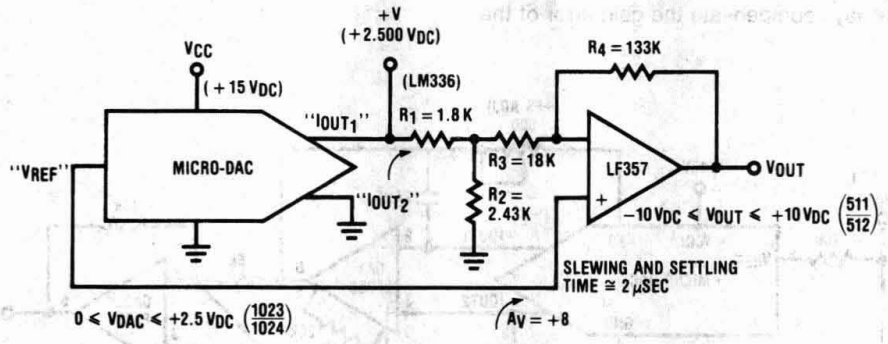

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FIGURE 11. Increasing the Output Voltage Swing

The output voltage swing can be expanded by adding 2 resistors to *Figure 10* as shown in *Figure 11*. These added resistors are used to attenuate the +V voltage. The overall gain, $A_V(-)$, from the +V terminal to the output of the op amp determines the most negative output voltage, $-4(+V)$ (when the V_{REF} voltage at the + input of the op amp is zero) with the component values shown. The complete dynamic range of V_{OUT} is provided by the gain from the (+) input of the op amp. As the voltage at the V_{REF} pin ranges from 0V to +V(1023/1024) the output of the op amp will range from -10 V_{DC} to +10V (1023/1024) when using a +V voltage of +2.500 V_{DC}. The 2.5 V_{DC} reference voltage can be easily developed by using the LM336 zener which can be biased through the R_{FB} internal resistor, connected to V_{CC}.

5.3 Op Amp V_{OS} Adjust (Zero Adjust) for Current Switching Mode

Proper operation of the ladder requires that all of the 2R legs always go to exactly 0 V_{DC} (ground). Therefore offset voltage, V_{OS}, of the external op amp cannot be tolerated as every millivolt of V_{OS} will introduce 0.01% of added linearity error. At first this seems unusually sensitive, until it becomes clear the 1 mV is 0.01% of the 10V reference! High resolution converters of high accuracy require attention to every detail in an application to achieve the available performance which is inherent in the part. To prevent this source of error, the V_{OS} of the op amp has to be initially zeroed. This is the "zero adjust" of the DAC calibration sequence and should be done first.

If the V_{OS} is to be adjusted there are a few points to consider. Note that no "dc balancing" resistance should be used in the grounded positive input lead of the op amp. This resistance and the input current of the op amp can also create errors. The low input biasing current of the BI-FET op amps makes them ideal for use in DAC current to voltage applications. The V_{OS} of the op amp should be adjusted with a digital input of all zeros to force $I_{OUT} = 0$ mA. A 1 kΩ resistor can be temporarily connected from the inverting input to ground to provide a dc gain of approximately 15 to the V_{OS} of the op amp and make the zeroing easier to sense.

5.4 Full-Scale Adjust

The full-scale adjust procedure depends on the application circuit and whether the DAC is operated in the current switching mode or in the voltage switching mode. Techniques are given below for all of the possible application circuits.

5.4.1 Current Switching with Unipolar Output Voltage

After doing a "zero adjust," set all of the digital input levels HIGH and adjust the magnitude of V_{REF} for

$$V_{OUT} = -(\text{ideal } V_{REF}) \frac{1023}{1024}$$

This completes the DAC calibration.

5.4.2 Current Switching with Bipolar Output Voltage

The circuit of *Figure 12* shows the 3 adjustments needed. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adj." for zero volts at the inverting input (pin 2) of 0A1. Next, with a code of all zeros still applied, adjust "−FS adj.", the reference voltage, for $V_{OUT} = \pm|\text{(ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+FS adj." for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. The addition of the 200Ω resistor in series with the V_{REF} pin of the DAC is to force the circuit gain error from the DAC to be negative. This insures that adding resistance to R_{fb}, with the 500Ω pot, will always compensate the gain error of the DAC.

5.4.3 Voltage Switching with a Unipolar Output Voltage

Refer to the circuit of *Figure 13* and set all digital inputs LOW. Trim the "zero adj." for $V_{OUT} = 0\ V_{DC} \pm 1$ mV. Then set all digital inputs HIGH and trim the "FS Adj." for:

$$V_{OUT} = (+V)\left(1 + \frac{R_1}{R_2}\right)\frac{1023}{1024}$$

5.4.4 Voltage Switching with a Bipolar Output Voltage

Refer to *Figure 14* and set all digital inputs LOW. Trim the "−FS Adj." for $V_{OUT} = -2.5\ V_{DC}$. Then set all digital inputs HIGH and trim the "+FS Adj." for $V_{OUT} = +2.5\ (511/512)\ V_{DC}$. Test the zero by setting the MS digital input HIGH and all the rest LOW. Adjust V_{OS} of amp #3, if necessary, and recheck the full-scale values.

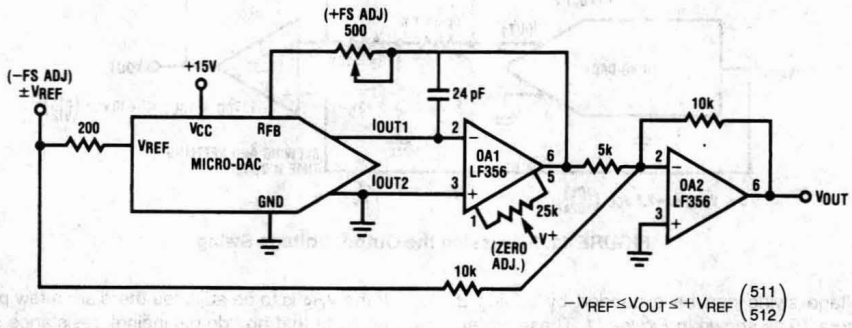

FIGURE 12. Full Scale Adjust — Current Switching with Bipolar Output Voltage

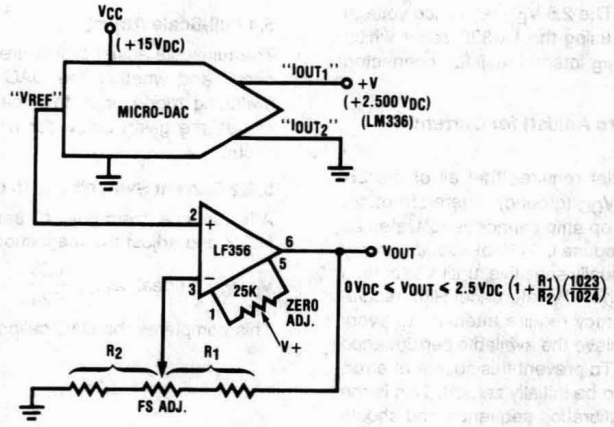

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FIGURE 13. Full Scale Adjust — Voltage Switching with a Unipolar Output Voltage

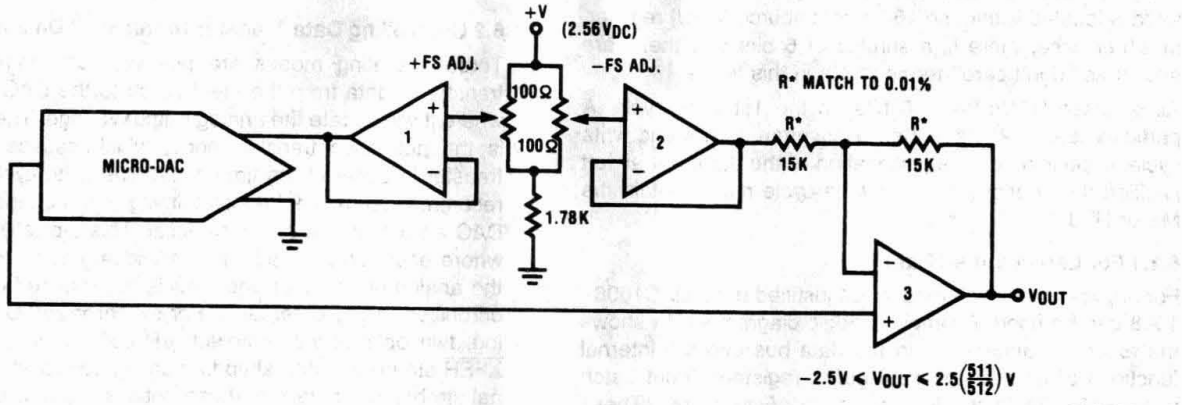

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FIGURE 14. Voltage Switching with a Bipolar Output Voltage

6.0 DIGITAL CONTROL DESCRIPTION

The DAC1006 series of products can be used in a wide variety of operating modes. Most of the options are shown in Table 1. Also shown in this table are the section numbers of this data sheet where each of the operating modes is discussed. For example, if your main interest in interfacing to a μP with an 8-bit data bus you will be directed to Section 6.1.0.

The first consideration is "will the DAC be interfaced to a μP with an 8-bit or a 16-bit data bus or used in the stand-alone mode?" For the 8-bit data bus, a second selection is made on how the 2nd digital data buffer (the DAC Latch) is updated by a transfer from the 1st digital data buffer (the Input Latch). Three options are provided: 1) an automatic transfer when the 2nd data byte is written to the DAC, 2) a transfer which is under the control of the μP and can include more than one DAC in a simultaneous transfer, or 3) a transfer which is under the control of external logic. Further, the data format can be either left justified or right justified.

When interfacing to a μP with a 16-bit data bus only two selections are available: 1) operating the DAC with a single digital data buffer (the transfer of one DAC does not have to be synchronized with any other DACs in the system), or 2) operating with a double digital data buffer for simultaneous transfer, or updating, of more than one DAC.

For operating without a μP in the stand alone mode, three options are provided: 1) using only a single digital data buffer, 2) using both digital data buffers — "double buffered," or 3) allowing the input digital data to "flow through" to provide the analog output without the use of any data latches.

To reduce the required reading, only the applicable sections of 6.1 through 6.4 need be considered.

6.1 Interfacing to an 8-Bit Data Bus

Transferring 10 bits of data over an 8-bit bus requires two write cycles and provides four possible combinations which depend upon two basic data format and protocol decisions:

1. Is the data to be left justified (considered as fractional binary data with the binary point to the left) or right justified (considered as binary weighted data with the binary point to the right)?
2. Which byte will be transferred first, the most significant byte (MS byte) or the least significant byte (LS byte)?

Table 1

Operating Mode / Data Bus	Automatic Transfer		μP Control Transfer		External Transfer	
	Section	Figure No.	Section	Figure No.	Section	Figure No.
8-Bit Data Bus (6.1.0) Left Justified (6.1.1)	6.2.1	16	6.2.2	16	6.2.3	16
16-Bit Data Bus (6.3.0)	Single Buffered		Double Buffered		Flow Through	
	6.3.1	17	6.3.2	17	Not Applicable	
Stand Alone (6.4.0)	Single Buffered		Double Buffered		Flow Through	
	6.4.1	17	6.4.2	17	NA	

These data possibilities are shown in *Figure 15*. Note that the justification of data depends on how the 10-bit data word is located within the 16-bit data source (CPU) register. In either case, there is a surplus of 6 bits and these are shown as "don't care" terms ("×") in this figure.

All of these DACs load 10 bits on the 1st write cycle. A particular set of 2 bits is then overwritten on the 2nd write cycle, depending on the justification of the data. For all left justified data options, the 1st write cycle must contain the MS or Hi Byte data group.

6.1.1 For Left Justified Data

For applications which require left justified data, DAC1006–1008 can be used. A simplified logic diagram which shows the external connections to the data bus and the internal functions of both of the data buffer registers (Input Latch and DAC Register) is shown in *Figure 16*. These parts require the MS or Hi Byte data group to be transferred on the 1st write cycle.

6.2 Controlling Data Transfer for an 8-Bit Data Bus

Three operating modes are possible for controlling the transfer of data from the Input Latch to the DAC Register, where it will update the analog output voltage. The simplest is the automatic transfer mode, which causes the data transfer to occur at the time of the 2nd write cycle. This is recommended when the exact timing of the changes of the DAC analog output are not critical. This typically happens where each DAC is operating individually in a system and the analog updating of one DAC is not required to be synchronized to any other DAC. For synchronized DAC updating, two options are provided: μP control via a common $\overline{\text{XFER}}$ strobe or external update timing control via an external strobe. The details of these options are now shown.

DAC1006/1007/1008 (20-Pin Parts for Left Justified Data)

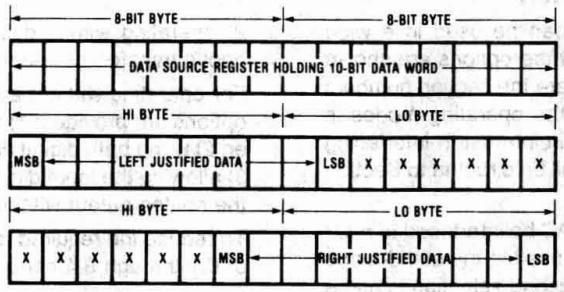

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FIGURE 15. Fitting a 10-Bit Data Word into 16 Available Bit Locations

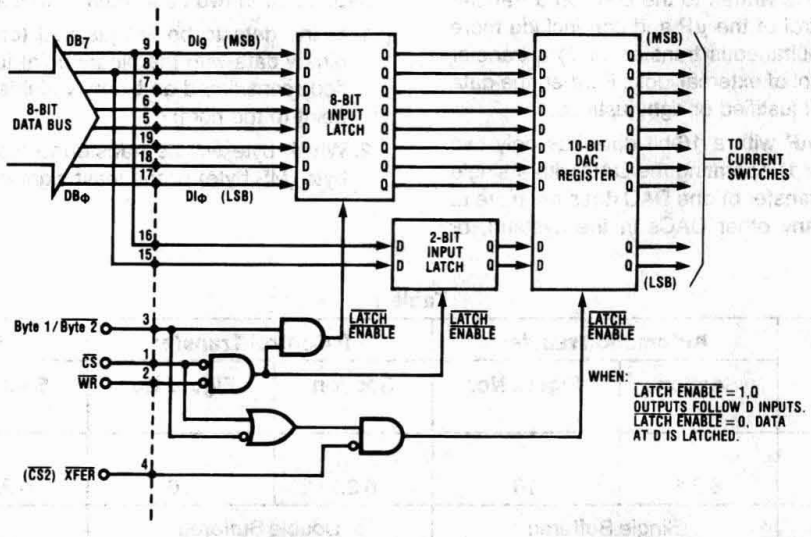

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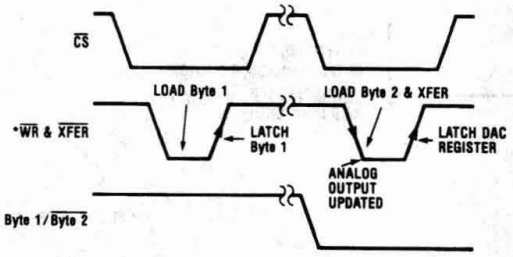
FIGURE 16. Input Connections and Controls for DAC1006/1007/1008 Left Justified Data

6.2.1 Automatic Transfer

This makes use of a double byte (double precision) write. The first byte (8 bits) is strobed into the input latch and the second byte causes a simultaneous strobe of the two remaining bits into the input latch and also the transfer of the complete 10-bit word from the input latch to the DAC register. This is shown in the following timing diagram; the point in time where the analog output is updated is also indicated on this diagram.

DAC1006/1007/1008 (20-Pin Parts)



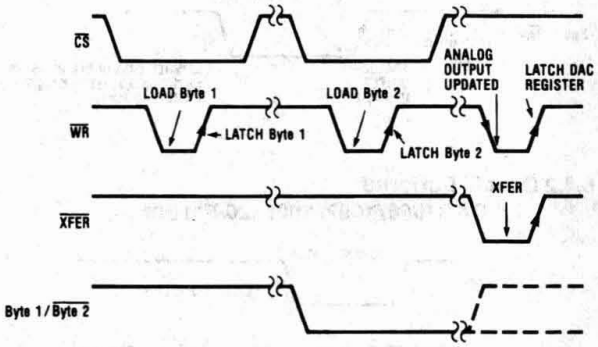
TL/H/5688–18

*SIGNIFIES CONTROL INPUTS WHICH ARE DRIVEN IN PARALLEL

6.2.2 Transfer Using μP Write Stroke

The input latch is loaded with the first two write strobes. The XFER signal is provided by external logic, as shown below, to cause the transfer to be accomplished on a third write strobe. This is shown in the following diagram:

DAC1006/1007/1008 (20-Pin Parts)



WHERE THE XFER CONTROL CAN BE GENERATED BY USING A SECOND CHIP SELECT AS:

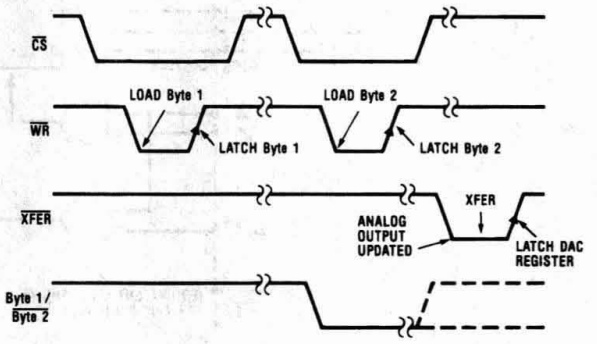
AND THE BYTE CONTROL CAN BE DERIVED FROM THE ADDRESS BUS SIGNALS.

TL/H/5688–19

6.2.3 Transfer Using an External Strobe

This is similar to the previous operation except the XFER signal is not provided by the μP. The timing diagram for this is:

DAC1006/1007/1008 (20-Pin Parts)

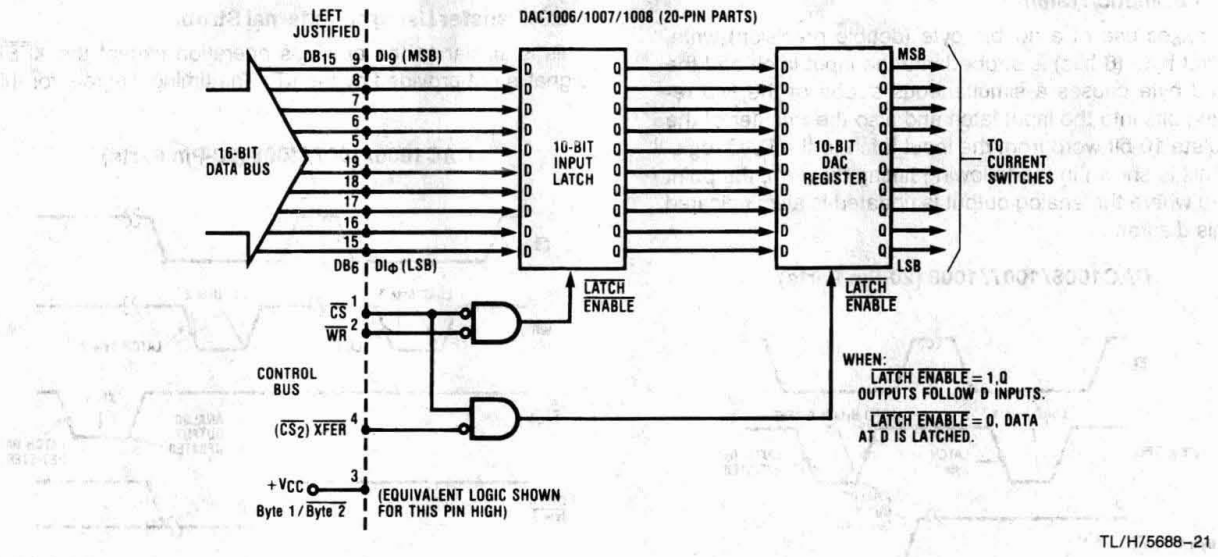


TL/H/5688–20

6.3 Interfacing to a 16-Bit Data Bus

The interface to a 16-bit data bus is easily handled by connecting to 10 of the available bus lines. This allows a wiring selected right justified or left justified data format. This is shown in the connection diagram of *Figure 17*, where the use of DB6 to DB15 gives left justified data operation. Note that any part number can be used and the Byte1/Byte2 control should be wired Hi.

3

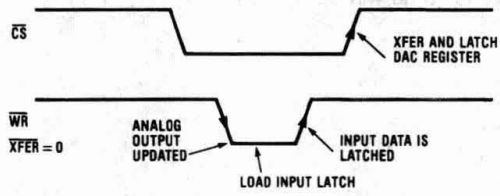


TL/H/5688–21

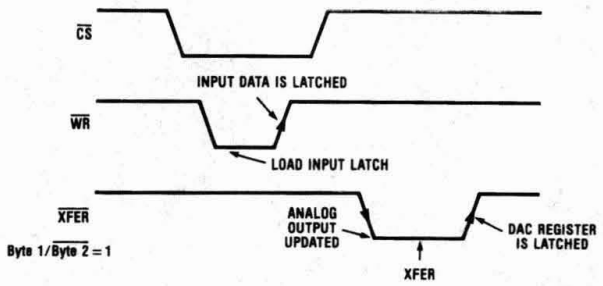
FIGURE 17. Input Connections and Logic for DAC1006/1007/1008 with 16-Bit Data Bus

Three operating modes are possible: flow through, single buffered, or double buffered. The timing diagrams for these are shown below:

6.3.1 Single Buffered
DAC1006/1007/1008 (20-Pin Parts)



6.3.2 Double Buffered
DAC1006/1007/1008 (20-Pin Parts)



TL/H/5688–22

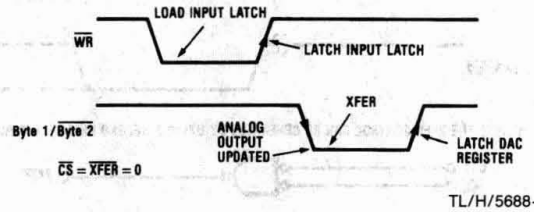
6.4 Stand Alone Operation

For applications for a DAC which are not under μP control (stand alone) there are two basic operating modes, single buffered and double buffered. The timing diagrams for these are shown below:

6.4.1 Single Buffered
DAC1006/1007/1008 (20-Pin Parts)

XFER TO DAC REGISTER
Byte 1/Byte 2
LOAD INPUT LATCH
ANALOG OUTPUT UPDATED
LATCHES DATA IN DAC REGISTER (INPUT DATA MUST REMAIN VALID UNTIL THIS TIME)

6.4.2 Double Buffered
DAC1006/1007/1008 (20-Pin Parts)*



TL/H/5688–23

*For a connection diagram of this operating mode use *Figure 16* for the Logic and *Figure 17* for the Data Input connections.

7.0 MICROPROCESSOR INTERFACE

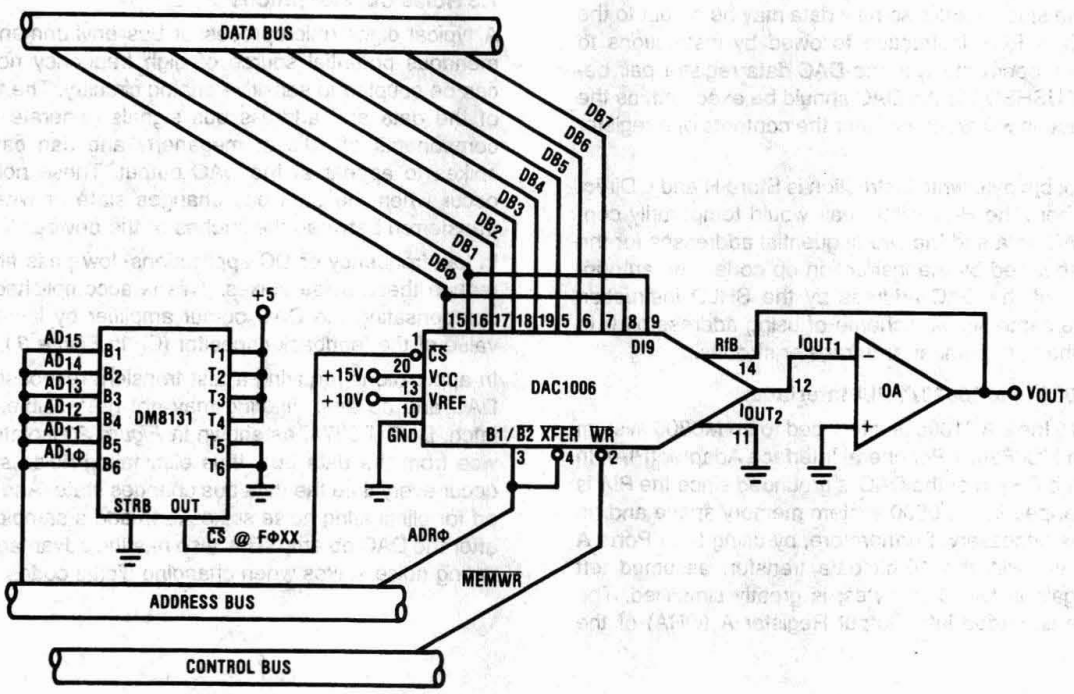
The logic functions of the DAC1006 family have been oriented towards an ease of interface with all popular μPs. The following sections discuss in detail a few useful interface schemes.

7.1 DAC1001/1/2 to INS8080A Interface

Figure 18 illustrates the simplicity of interfacing the DAC1006 to an INS8080A based microprocessor system.

The circuit will perform an automatic transfer of the 10 bits of output data from the CPU to the DAC register as outlined in Section 6.2.1, "Controlling Data Transfer for an 8-Bit Data Bus."

Since a double byte write is necessary to control the DAC with the INS8080A, a possible instruction to achieve this is a PUSH of a register pair onto a "stack" in memory. The 16-bit register pair word will contain the 10 bits of the eventual DAC input data in the proper sequence to conform to both



TL/H/5688–24

NOTE: DOUBLE BYTE STORES CAN BE USED.
e.g. THE INSTRUCTION SHLD F001 STORES THE L REG INTO B1 AND THE H REG INTO B2 AND TRANSFERS THE RESULT TO THE DAC REGISTER. THE OPERAND OF THE SHLD INSTRUCTION MUST BE AN ODD ADDRESS FOR PROPER TRANSFER.

FIGURE 18. Interfacing the DAC1000 to the INS8080A CPU Group

the requirements of the DAC (with regard to left justified data) and the implementation of the PUSH instruction which will output the higher order byte of the register pair (i.e., register B of the BC pair) first. The DAC will actually appear as a two-byte "stack" in memory to the CPU. The auto-decrementing of the stack pointer during a PUSH allows using address bit 0 of the stack pointer as the Byte1/$\overline{\text{Byte2}}$ and $\overline{\text{XFER}}$ strobes if bit 0 of the stack pointer address -1, (SP-1), is a "1" as presented to the DAC. Additional address decoding by the DM8131 will generate a unique DAC chip select (CS) and synchronize this CS to the two memory write strobes of the PUSH instruction.

To reset the stack pointer so new data may be output to the same DAC, a POP instruction followed by instructions to insure that proper data is in the DAC data register pair before it is "PUSHED" to the DAC should be executed, as the POP instruction will arbitrarily alter the contents of a register pair.

Another double byte write instruction is Store H and L Direct (SHLD), where the HL register pair would temporarily contain the DAC data and the two sequential addresses for the DAC are specified by the instruction op code. The auto incrementing of the DAC address by the SHLD instruction permits the same simple scheme of using address bit 0 to generate the byte number and transfer strobes.

7.2 DAC1006 to MC6820/1 PIA Interface

In *Figure 19* the DAC1006 is interfaced to an M6800 system through an MC6820/1 Peripheral Interface Adapter (PIA). In this case the CS pin of the DAC is grounded since the PIA is already mapped in the 6800 system memory space and no decoding is necessary. Furthermore, by using both Ports A and B of the PIA the 10-bit data transfer, assumed left justified again in two 8-bit bytes, is greatly simplified. The HIGH byte is loaded into Output Register A (ORA) of the PIA, and the LOW byte is loaded into ORB. The 10-bit data transfer to the DAC and the corresponding analog output change occur simultaneously upon CB2 going LOW under program control. The 10-bit data word in the DAC register will be latched (and hence V_{OUT} will be fixed) when CB2 is brought back HIGH.

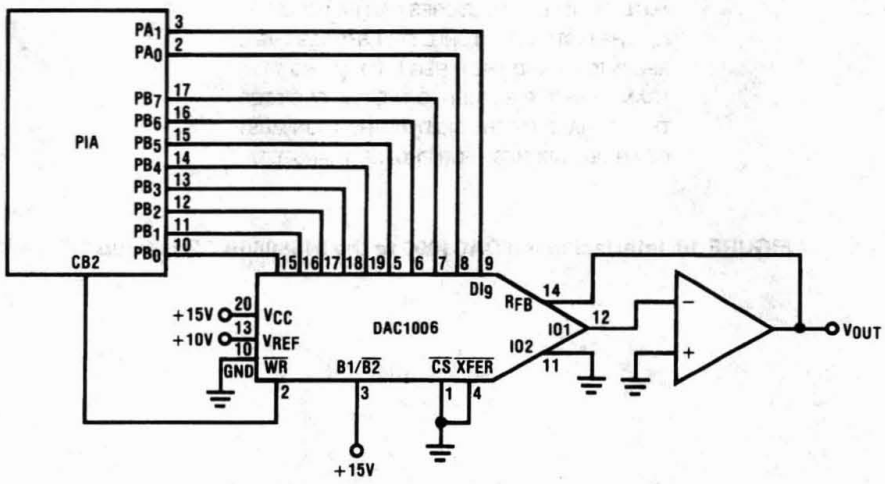
If both output ports of the PIA are not available, it is possible to interface the DAC1006 through a single port without much effort. However, additional logic at the CB2(or CA2) lines or access to some of the 6800 system control lines will be required.

7.3 Noise Considerations

A typical digital/microprocessor bus environment is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and can cause noise spikes to appear at the DAC output. These noise spikes occur when the data bus changes state or when data is transferred between the latches of the device.

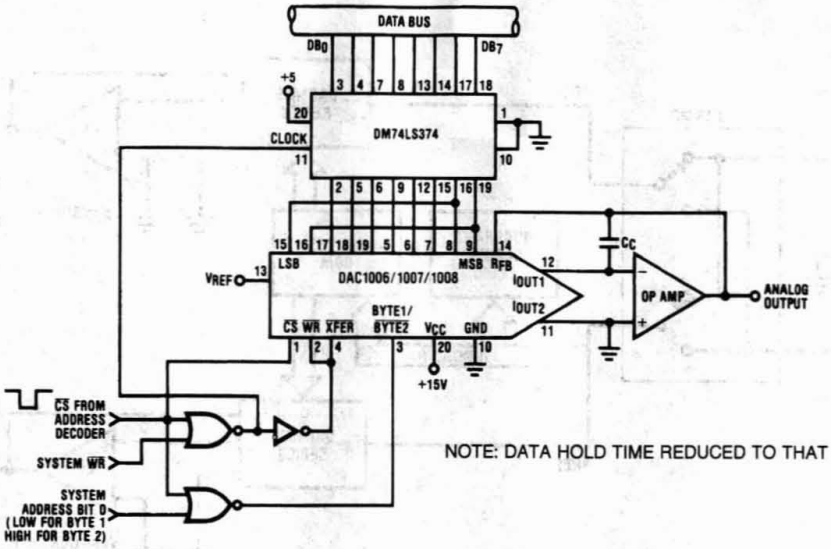
In low frequency or DC applications, low pass filtering can reduce these noise spikes. This is accomplished by overcompensating the DAC output amplifier by increasing the value of the feedback capacitor (C_C in *Figure 3*).

In applications requiring a fast transient response from the DAC and op amp, filtering may not be feasible. Adding a latch, DM74LS374, as shown in *Figure 20* isolates the device from the data bus, thus eliminating noise spikes that occur every time the data bus changes state. Another method for eliminating noise spikes is to add a sample and hold after the DAC op amp. This also has the advantage of eliminating noise spikes when changing digital codes.



TL/H/5688–25

FIGURE 19. DAC1000 to MC6820/1 PIA Interface



NOTE: DATA HOLD TIME REDUCED TO THAT OF DM74LS374 (≈ 10 ns)

FIGURE 20. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

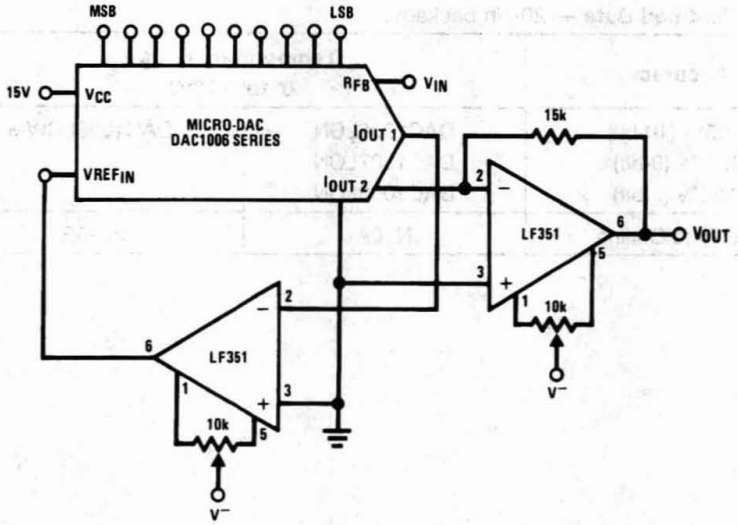


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FIGURE 21. Digitally Controlled Amplifier/Attenuator

7.4 Digitally Controlled Amplifier/Attenuator

An unusual application of the DAC, *Figure 21*, applies the input voltage via the on-chip feedback resistor. The lower op amp automatically adjusts the $V_{REF\ IN}$ voltage such that I_{OUT1} is equal to the input current (V_{IN}/Rf_B). The magnitude of this $V_{REF\ IN}$ voltage depends on the digital word which is in the DAC register. I_{OUT2} then depends upon both the magnitude of V_{IN} and the digital word. The second op amp converts I_{OUT2} to a voltage, V_{OUT}, which is given by:

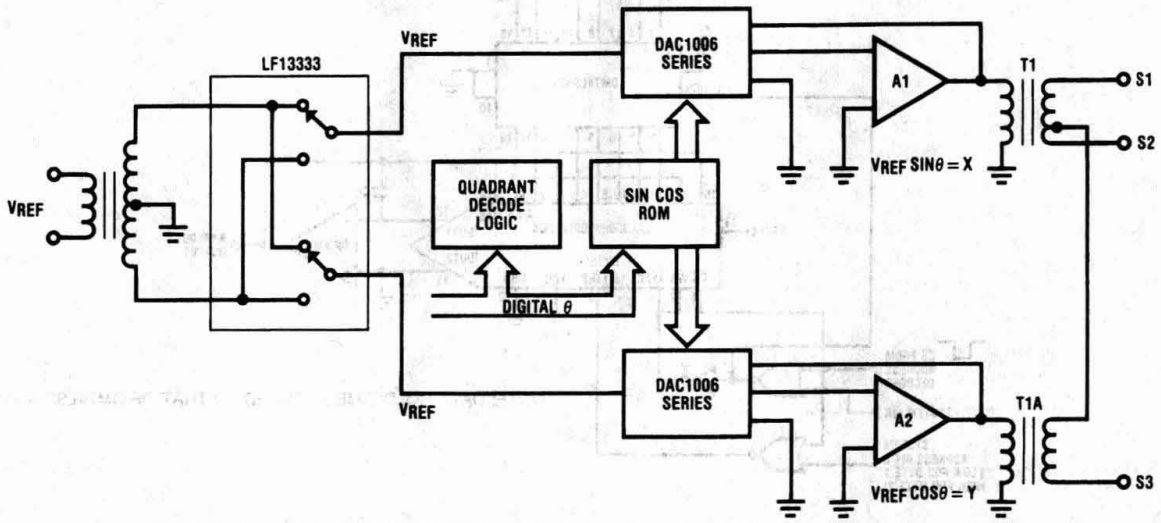
$$V_{OUT} = V_{IN}\left(\frac{1023-N}{N}\right), \text{ where } 0 < N \leq 1023.$$

Note that N = 0 (or a digital code of all zeros) is not allowed or this will cause the output amplifier to saturate at either $\pm V_{MAX}$, depending on the sign of V_{IN}.

To provide a digitally controlled divider, the output op amp can be eliminated. Ground the I_{OUT2} pin of the DAC and V_{OUT} is now taken from the lower op amp (which also drives the V_{REF} input of the DAC). The expression for V_{OUT} is now given by

$$V_{OUT} = -\frac{V_{IN}}{M}$$ where M = Digital input (expressed as a fractional binary number).

$0 < M < 1$.



TL/H/5688–27

FIGURE 22. Digital to Synchro Converter

Ordering Information

For Left Justified Data — 20-pin package.

Accuracy	Temperature Range 0° to +70°C	
0.05% (10-bit) 0.10% (9-bit) 0.20% (8-bit)	DAC1006LCN DAC1007LCN DAC1008LCN	DAC1006LCWM
Package Outline	N20A	M20B

National Semiconductor

DAC1020/DAC1021/DAC1022
10-Bit Binary Multiplying D/A Converter
DAC1220/DAC1222
12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

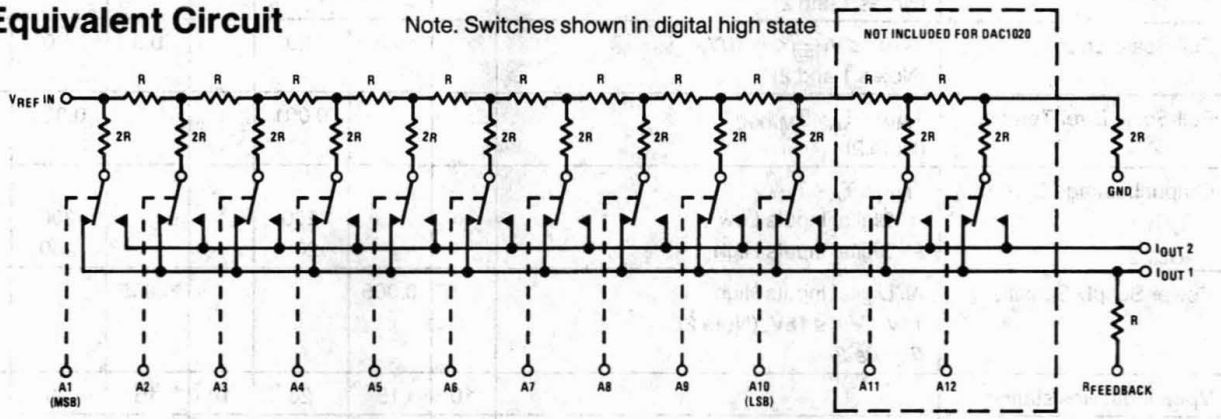
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guaranteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021 and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 and equivalent to the AD7533 family. The DAC1220 and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

- Linearity specified with zero and full-scale adjust only
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq 25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—½ LSB @100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



TL/H/5689–1

Ordering Information

10-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C			−40°C to 85°C
Non-Linearity	0.05%	DAC1020LCN	AD7520LN,AD7530LN	DAC1020LCV	DAC1020LIV
	0.10%	DAC1021LCN	AD7520KN,AD7530KN		
	0.20%	DAC1022LCN	AD7520JN,AD7530JN		
Package Outline		N16A		V20A	

12-BIT D/A CONVERTERS

Temperature Range		0°C to 70°C		−40°C to +85°C	
Non-Linearity	0.05%	DAC1220LCN	AD7521LN,AD7531LN	DAC1220LCJ	AD7521LD,AD7531LD
	0.20%	DAC1222LCN	AD7521JN,AD7531JN	DAC1222LCJ	AD7521JD,AD7531JD
Package Outline		N18A		J18A	

Note. Devices may be ordered by either part number.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^+ to Gnd	17V
V_{REF} to Gnd	±25V
Digital Input Voltage Range	V^+ to Gnd
DC Voltage at Pin 1 or Pin 2 (Note 3)	−100 mV to V^+
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
ESD Susceptibility (Note 4)	800V

Operating Ratings

	Min	Max	Units
Temperature (T_A)			
DAC1020LIV, DAC1220LCJ, DAC1222LCJ	−40	+85	°C
DAC1020LCN, DAC1020LCV, DAC1021LCN	0	+70	°C
DAC1022LCN, DAC1220LCN	0	+70	°C
DAC1222LCN	0	+70	°C

Electrical Characteristics ($V^+ = 15V$, $V_{REF} = 10.000V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		10			12			Bits
Linearity Error	$T_{MIN} < T_A < T_{MAX}$, $-10V < V_{REF} < +10V$, (Note 1) End Point Adjustment Only (See Linearity Error in Definition of Terms)							
10-Bit Parts	DAC1020, DAC1220			0.05			0.05	% FSR
9-Bit Parts	DAC1021			0.10			0.10	% FSR
8-Bit Parts	DAC1022, DAC1222			0.20			0.20	% FSR
Linearity Error Tempco	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)			0.0002			0.0002	% FS/°C
Full-Scale Error	$-10V \le V_{REF} \le +10V$, (Notes 1 and 2)		0.3	1.0		0.3	1.0	% FS
Full-Scale Error Tempco	$T_{MIN} < T_A < T_{MAX}$, (Note 2)			0.001			0.001	% FS/°C
Output Leakage Current	$T_{MIN} \le T_A \le T_{MAX}$							
$I_{OUT\,1}$	All Digital Inputs Low			200			200	nA
$I_{OUT\,2}$	All Digital Inputs High			200			200	nA
Power Supply Sensitivity	All Digital Inputs High, $14V \le V^+ \le 16V$, (Note 2), *(Figure 2)*		0.005			0.005		% FS/V
V_{REF} Input Resistance		10	15	20	10	15	20	kΩ
Full-Scale Current Settling Time	$R_L = 100\Omega$ from 0 to 99. 95% FS							
	All Digital Inputs Switched Simultaneously		500			500		ns
V_{REF} Feedthrough	All Digital Inputs Low, $V_{REF} = 20$ Vp-p @ 100 kHz			10			10	mVp-p
	J Package (Note 4)		6	9		6	9	mVp-p
	N Package		2	5		2	5	mVp-p
Output Capacitance								
$I_{OUT\,1}$	All Digital Inputs Low		40			40		pF
	All Digital Inputs High		200			200		pF
$I_{OUT\,2}$	All Digital Inputs Low		200			200		pF
	All Digital Inputs High		40			40		pF

Electrical Characteristics ($V^+ = 15V$, $V_{REF} = 10.000V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter	Conditions	DAC1020, DAC1021, DAC1022			DAC1220, DAC1222			Units
		Min	Typ	Max	Min	Typ	Max	
Digital Input	*(Figure 1)*							
Low Threshold	$T_{MIN} < T_A < T_{MAX}$			0.8			0.8	V
High Threshold	$T_{MIN} < T_A < T_{MAX}$	2.4			2.4			V
Digital Input Current	$T_{MIN} \leq T_A \leq T_{MAX}$							
	Digital Input High		1	100		1	100	μA
	Digital Input Low		−50	−200		−50	−200	μA
Supply Current	All Digital Inputs High		0.2	1.6		0.2	1.6	mA
	All Digital Inputs Low		0.6	2		0.6	2	mA
Operating Power Supply Range	*(Figures 1 and 2)*	5		15	5		15	V

Note 1: $V_{REF} = \pm 10V$ and $V_{REF} = \pm 1V$. A linearity error temperature coefficient of 0.0002% FS for a 45°C rise only guarantees 0.009% maximum change in linearity error. For instance, if the linearity error at 25°C is 0.045% FS it could increase to 0.054% at 70°C and the DAC will be no longer a 10-bit part. Note, however, that the linearity error is specified over the device full temperature range which is a more stringent specification since *it includes* the linearity error temperature coefficient.

Note 2: Using internal feedback resistor as shown in *Figure 3.*

Note 3: Both $I_{OUT\ 1}$ and $I_{OUT\ 2}$ must go to ground or the virtual ground of an operational amplifier. If $V_{REF} = 10V$, every millivolt offset between $I_{OUT\ 1}$ or $I_{OUT\ 2}$, 0.005% linearity error will be introduced.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 6: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temepature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the J18 package when board mounted is 85°C/W. For the N18 package, θ_{JA} is 120°C/W, for the N16 this number is 125°C/W, and for the V20 this number is 95°C/W.

Typical Performance Characteristics

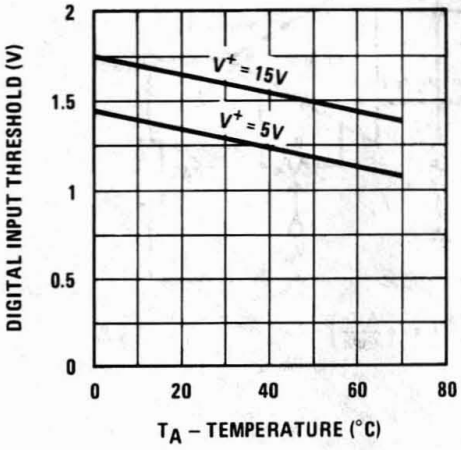
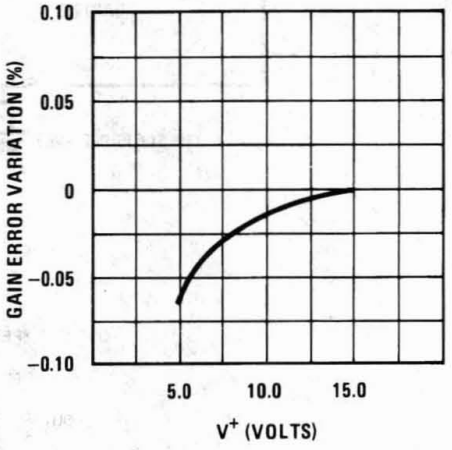


FIGURE 1. Digital Input Threshold vs Ambient Temperature



TL/H/5689–2

FIGURE 2. Gain Error Variation vs V^+

Typical Applications

The following applications are also valid for 12-bit systems using the DAC1220 and 2 additional digital inputs.

Operational Amplifier Bias Current (*Figure 3*)

The op amp bias current, I_b, flows through the 15k internal feedback resistor. BI-FET op amps have low I_b and, therefore, the 15k $\times$ I_b error they introduce is negligible; they are strongly recommended for the DAC1020 applications.

V_{OS} Considerations

The output impedance, R_{OUT}, of the DAC is modulated by the digital input code which causes a modulation of the operational amplifier output offset. It is therefore recommended to adjust the op amp V_{OS}. R_{OUT} is ~15k if more than 4 digital inputs are high; R_{OUT} is ~45k if a single digital input is high, and R_{OUT} approaches infinity if all inputs are low.

Operational Amplifier V_{OS} Adjust (*Figure 3*)

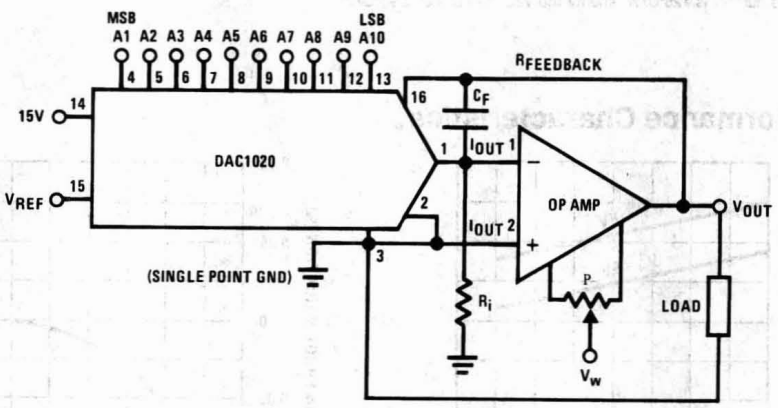
Connect all digital inputs, A1–A10, to ground and adjust the potentiometer to bring the op amp V_{OUT} pin to within ± 1 mV from ground potential. If V_{REF} is less than 10V, a finer V_{OS} adjustment is required. It is helpful to increase the resolution of the V_{OS} adjust procedure by connecting a 1 kΩ resistor between the inverting input of the op amp to ground. After V_{OS} has been adjusted, remove the 1 kΩ.

Full-Scale Adjust (*Figure 4*)

Switch high all the digital inputs, A1–A10, and measure the op amp output voltage. Use a 500Ω potentiometer, as shown, to bring $\|V_{OUT}\|$ to a voltage equal to $V_{REF} \times 1023/1024$.

SELECTING AND COMPENSATING THE OPERATIONAL AMPLIFIER

Op Amp Family	C_F	R_i	P	V_W	Circuit Settling Time, t_s	Circuit Small Signal BW
LF357	10 pF	2.4k	25k	V^+	1.5 μs	1M
LF356	22 pF	∞	25k	V^+	3 μs	0.5M
LF351	24 pF	∞	10k	V^-	4 μs	0.5M
LM741	0	∞	10k	V^-	40 μs	200 kHz



TL/H/5689–3

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \bullet\bullet\bullet \frac{A10}{1024}\right)$$

$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

where A_N = 1 if the A_N digital input is high

A_N = 0 if the A_N digital input is low

FIGURE 3. Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

Typical Applications (Continued)

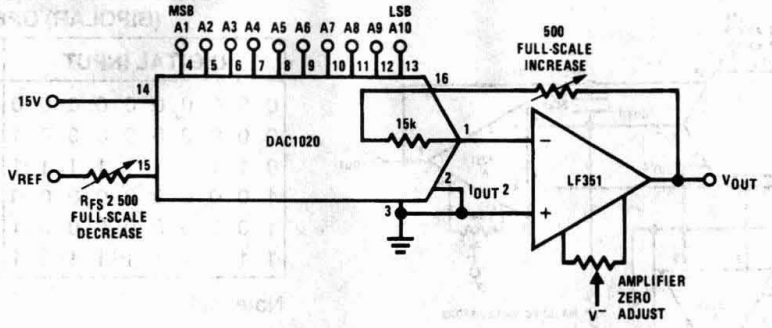


FIGURE 4. Full-Scale Adjust

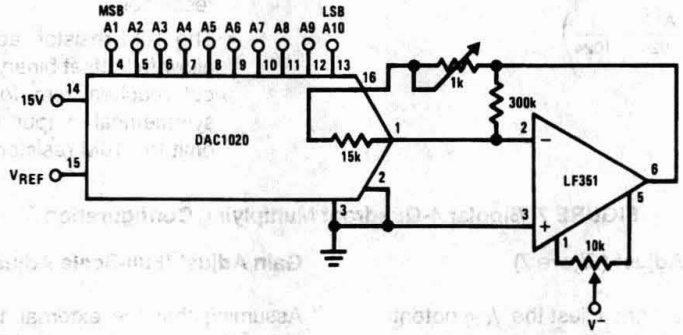
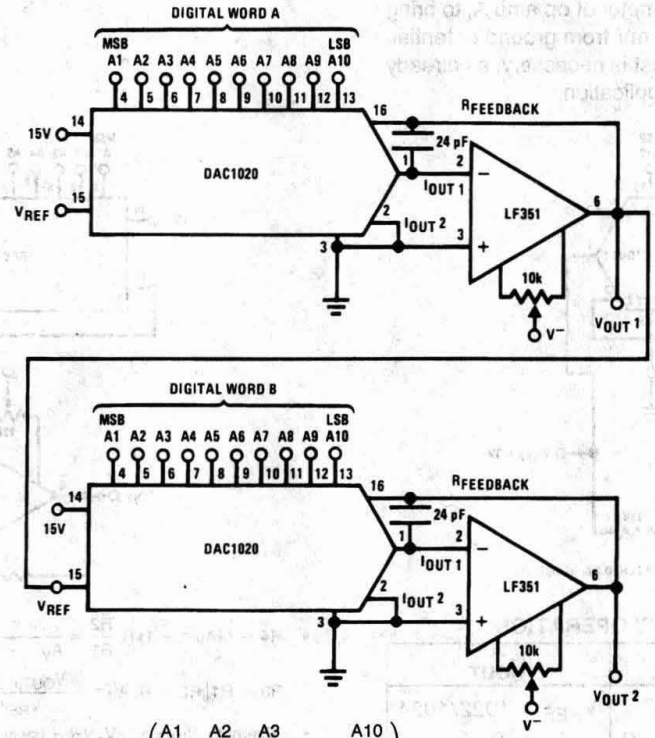


FIGURE 5. Alternate Full-Scale Adjust: (Allows Increasing or Decreasing the Gain)



TL/H/5689–4

$$V_{OUT\,1} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \bullet\bullet\bullet \frac{A10}{1024}\right)$$

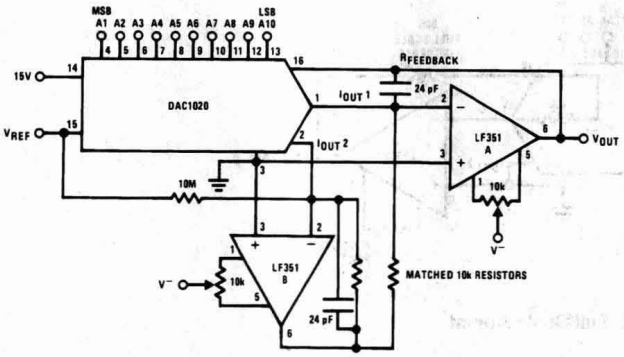
$$V_{OUT2} = V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \bullet\bullet\bullet \frac{A10}{1024}\right) \times \left(\frac{B1}{2} + \frac{B2}{4} + \frac{B3}{8} + \bullet\bullet\bullet \frac{B10}{1024}\right)$$

where V_{REF} can be an AC signal

FIGURE 6. Precision Analog-to-Digital Multiplier

3

Typical Applications (Continued)



TL/H/5689–5

$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \bullet\bullet\bullet + \frac{A10}{1024} - \frac{1}{1024}\right)$$

where: AN = +1 if A_N input is high
AN = −1 if A_N input is low

COMPLEMENTARY OFFSET BINARY (BIPOLAR) OPERATION

DIGITAL INPUT	V_{OUT}
0 0 0 0 0 0 0 0 0 0	$+V_{REF}$
0 0 0 0 0 0 0 0 0 1	$V_{REF} \times 1022/1024$
0 1 1 1 1 1 1 1 1 1	$V_{REF} \times 2/1024$
1 0 0 0 0 0 0 0 0 0	0
1 0 0 0 0 0 0 0 0 1	$-V_{REF} \times 2/1024$
1 1 1 1 1 1 1 1 1 1	$-V_{REF}$ (1022/1024)

Note that:

- $I_{OUT\,1} + I_{OUT\,2} = \frac{V_{REF}}{R_{LADDER}} \times \left(\frac{1023}{1024}\right)$
- By doubling the output range we get half the resolution
- The 10M resistor, adds a 1 LSB "thump", to allow full offset binary operation where the output reaches zero for the half-scale code. If symmetrical output excursions are required, omit the 10M resistor.

FIGURE 7. Bipolar 4-Quadrant Multiplying Configuration

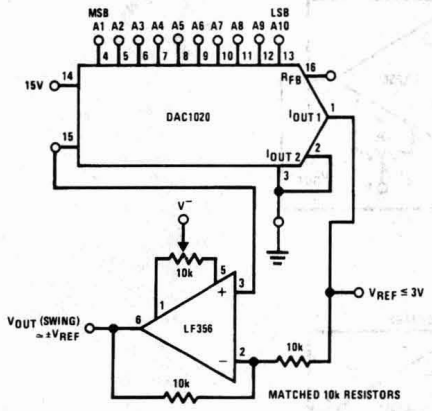
Operational Amplifiers V_{OS} Adjust (*Figure 7*)

a) Switch all the digital inputs high; adjust the V_{OS} potentiometer of op amp B to bring its output to a value equal to $-(V_{REF}/1024)$ (V).

b) Switch the MSB high and the remaining digital inputs low. Adjust the V_{OS} potentiometer of op amp A, to bring its output value to within a 1 mV from ground potential. For $V_{REF} < 10V$, a finer adjust is necessary, as already mentioned in the previous application.

Gain Adjust (Full-Scale Adjust)

Assuming that the external 10k resistors are matched to better than 0.1%, the gain adjust of the circuit is the same with the one previously discussed.

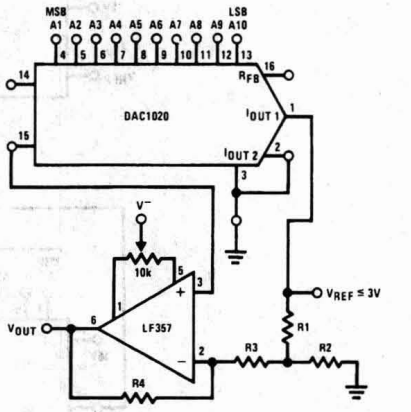


TRUE OFFSET BINARY OPERATION

DIGITAL INPUT	V_{OUT}
1 1 1 1 1 1 1 1 1 1	$V_{REF} \times 1022/1024$
1 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 0 0	$-V_{REF}$

t_s = 1.8 μs
use LM336 for a voltage reference

FIGURE 8. Bipolar Configuration with a Single Op Amp



TL/H/5689–6

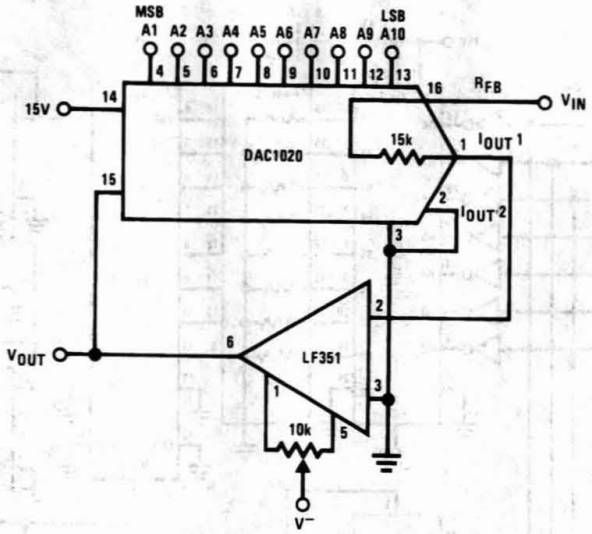
- $R4 = (2A_V^- - 1)\,R, \frac{R2}{R1} = \frac{A_V^-}{A_V^- - 1}$,

  $R3 + R1 \| R2 = R; A_V^- = \frac{V_{OUT(PEAK)}}{V_{REF}}, R = 20k$

- Example: $V_{REF} = 2V$, V_{OUT} (swing) ≅ ±10V: $A_V^- = 5V$
  Then R4 = 9R, R1 = 0.8 R2. If R1 = 0.2R then R2 = 0.25R, R3 = 0.64R

FIGURE 9. Bipolar Configuration with Increased Output Swing

Typical Applications (Continued)

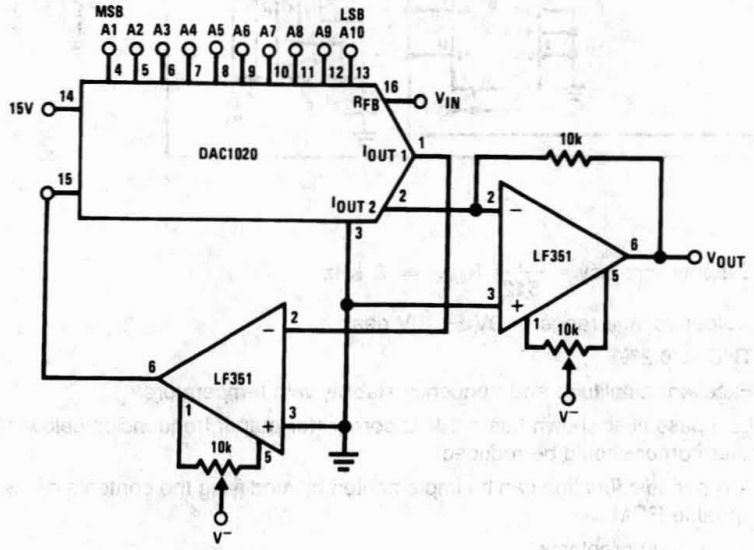


$$V_{OUT} = \frac{-V_{REF}}{\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)}$$

where: V_{REF} can be an AC signal

- By connecting the DAC in the feedback loop of an operational amplifier a linear digitally control gain block can be realized
- Note that with all digital inputs low, the gain of the amplifier is infinity, that is, the op amp will saturate. In other words, we cannot divide the V_{REF} by zero!

FIGURE 10. Analog-to-Digital Divider (or Digitally Gain Controlled Amplifier)



TL/H/5689–7

$$V_{OUT} = V_{REF}\left[\frac{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \ldots + \frac{\overline{A10}}{1024}}{\frac{A1}{2} + \frac{A2}{4} + \ldots + \frac{A10}{1024}}\right] \text{ or } V_{OUT} = V_{REF}\left(\frac{1023 - N}{N}\right)$$

where: $0 \leq N \leq 1023$

$N = 0$ for A_N = all zeros

$N = 1$ for A10 = 1, A1–A9 = 0

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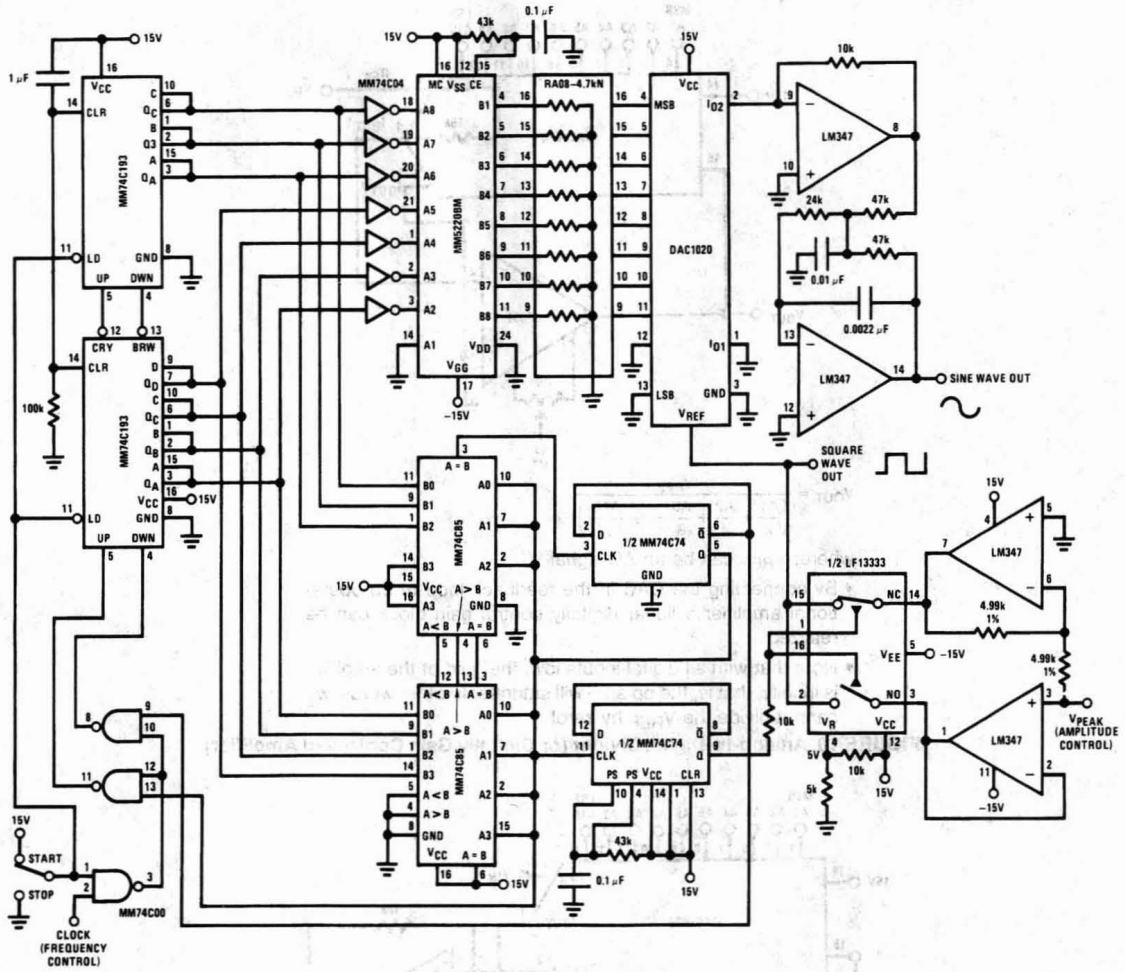
$N = 1023$ for A_N = all 1's

FIGURE 11. Digitally controlled Amplifier-Attenuator

Typical Applications (Continued)

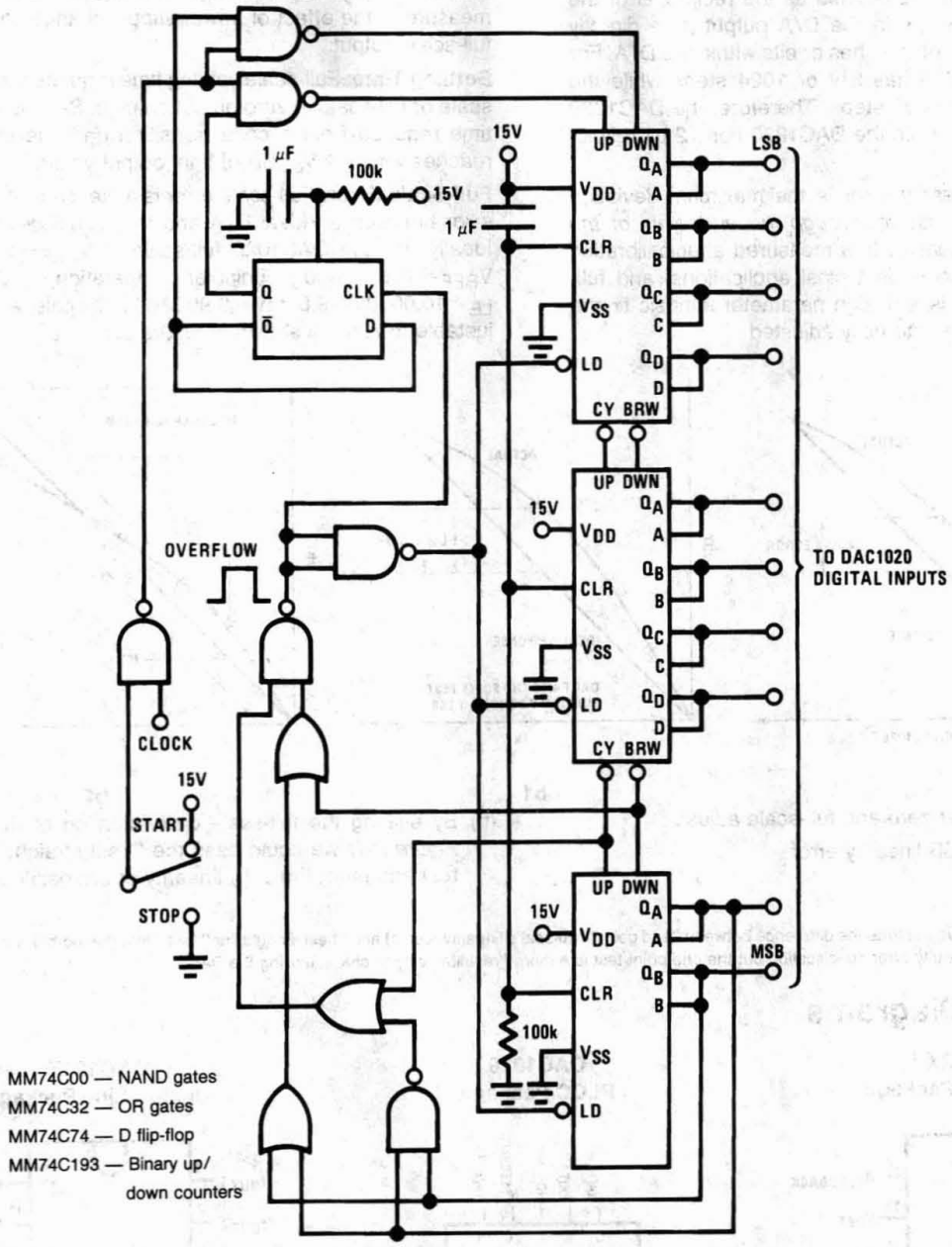


TL/H/5689–8

- Output frequency = $\frac{f_{CLK}}{512}$; $f_{MAX} \cong 2$ kHz
- Output voltage range = 0V − 10V peak
- THD < 0.2%
- Excellent amplitude and frequency stability with temperature
- Low pass filter shown has a 1 kHz corner (for output frequencies below 10 Hz, filter corner should be reduced)
- Any periodic function can be implemented by modifying the contents of the look up table ROM
- No start up problems

FIGURE 12. Precision Low Frequency Sine Wave Oscillator Using Sine Look-Up ROM

Typical Applications (Continued)



TL/H/5689–9

- Binary up/down counter digitally "ramps" the DAC output
- Can stop counting at any desired 10-bit input code
- Senses up or down count overflow and automatically reverses direction of count

FIGURE 13. A Useful Digital Input Code Generator for DAC Attenuator or Amplifier Circuits

Definition of Terms

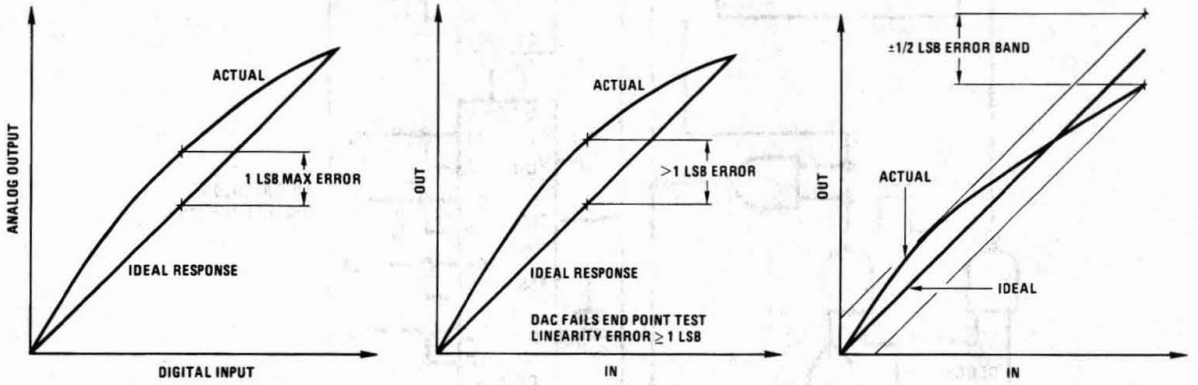
Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the D/A output. It is directly related to the number of switches or bits within the D/A. For example, the DAC1020 has 2^{10} or 1024 steps while the DAC1220 has 2^{12} or 4096 steps. Therefore, the DAC1020 has 10-bit resolution, while the DAC1220 has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from *a straight line passing through the endpoints of the D/A transfer characteristic.* It is measured after calibrating for zero (see V_{OS} adjust in typical applications) and full-scale. Linearity error is a design parameter intrinsic to the device and cannot be externally adjusted.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the D/A full-scale output.

Settling Time: Full-scale settling time requires a zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the D/A output reaches within $\pm 1/2$ LSB of final output value.

Full-Scale Error: Full-scale error is a measure of the output error between an ideal D/A and the actual device output. Ideally, for the DAC1020 full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 9.8\ mV = 9.9902V$. Full-scale error is adjustable to zero as shown in *Figure 5*.



TL/H/5689–10

a

(a) End point test after zero and full-scale adjust. The DAC has 1 LSB linearity error.

b1

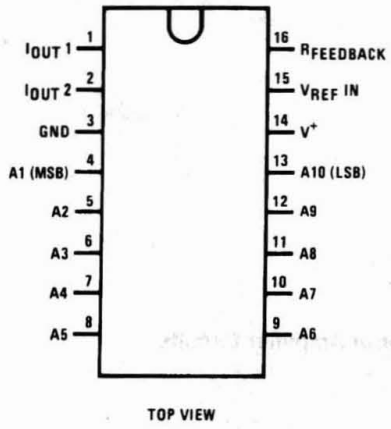
b2

(b) By shifting the full-scale calibration on of the DAC of *Figure (b1)* we could pass the "best straight line" (b2) test and meet the $\pm 1/2$ linearity error specification.

Note. (a), (b1) and (b2) above illustrate the difference between "end point" National's linearity test (a) and "best straight line" test. Note that both devices in (a) and (b2) meet the $\pm 1/2$ LSB linearity error specification but the end point test is a more "real life" way of characterizing the DAC.

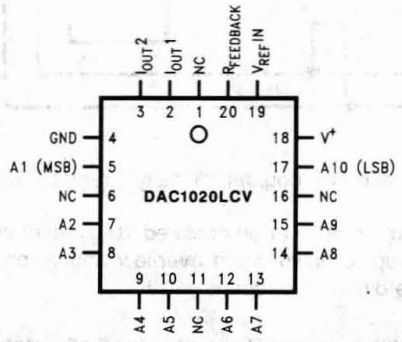
Connection Diagrams

DAC102X
Dual-In-Line Package



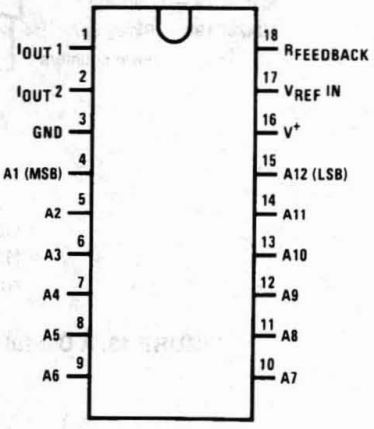
TL/H/5689–13

DAC1020
PLCC Package



TL/H/5689–12

DAC122X
Dual-In-Line Package



TL/H/5689–11

National Semiconductor

DAC1054 Quad 10-Bit Voltage-Output Serial D/A Converter with Readback

General Description

The DAC1054 is a complete quad 10-bit voltage-output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, internal voltage reference, and serial microprocessor interface. By combining in one package the reference, amplifiers, and conversion circuitry for four D/A converters, the DAC1054 minimizes wiring and parts count and is hence ideally suited for applications where cost and board space are of prime concern.

The DAC1054 also has a data readback function, which can be used by the microprocessor to verify that the desired input word has been properly latched into the DAC1054's data registers. The data readback function simplifies the design and reduces the cost of systems which need to verify data integrity.

The logic comprises a MICROWIRE™-compatible serial interface and control circuitry. The interface allows the user to write to any one of the input registers or to all four at once. The latching registers are double-buffered, consisting of 4 separate input registers and 4 DAC registers. Each DAC register may be written to individually. Double buffering allows all 4 DAC outputs to be updated simultaneously or individually.

The four reference inputs allow the user to configure the system to have a separate output voltage range for each DAC. The output voltage of each DAC can range between 0.3V and 2.8V and is a function of V_{BIAS}, V_{REF}, and the input word.

Features

- Single +5V supply operation
- MICROWIRE serial interface allows easy interface to many popular microcontrollers including the COPS™ and HPC™ families of microcontrollers
- Data readback capability
- Output data can be formatted to read back MSB or LSB first
- Versatile logic allows selective or global update of the DACs
- Power fail flag
- Output amplifiers can drive 2 kΩ load
- Synchronous/asynchronous update of the DAC outputs

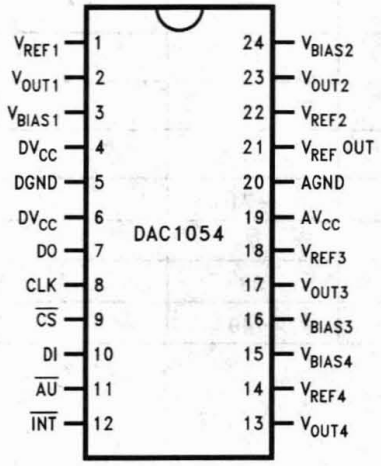
Key Specifications

■ Guaranteed monotonic over temperature	
■ Integral linearity error	±¾ LSB max
■ Output settling time	3.7 μs max
■ Analog output voltage range	0.3V to 2.8V
■ Supply voltage range	4.5V to 5.5V
■ Clock frequency for write	10 MHz max
■ Clock frequency for read back	5 MHz max
■ Power dissipation (f_{CLK} = 10 MHz)	100 mW max
■ On-board reference	2.65V ±2% max

Applications

- Automatic test equipment
- Industrial process controls
- Automotive controls and diagnostics
- Instrumentation

Connection Diagram



TL/H/11437–1

Top View

Ordering Information

Industrial ($-40°C < T_A < +85°C$)	Package
DAC1054CIN	N24A Molded DIP
DAC1054CIWM	M24B Small Outline
Military ($-55°C < T_A < +125°C$)	
DAC1054CMJ/883 or 5962-9466201MJA	J24A Ceramic DIP

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (AV_{CC}, DV_{CC})	7V
Supply Voltage Difference ($AV_{CC}-DV_{CC}$)	±5.5V
Voltage at Any Pin (Note 3)	GND −0.3V to AV_{CC}/DV_{CC} +0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 4)	30 mA
Power Dissipation (Note 5)	950 mW
ESD Susceptibility (Note 6)	
Human Body Model	2000V
Machine Model	200V
Soldering Information	
N Package (10 sec.)	260°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1 & 2)

Supply Voltage	4.5V to 5.5V
Supply Voltage Difference ($AV_{CC} - DV_{CC}$)	±1V
Temperature Range	$T_{MIN} < T_A < T_{MAX}$
DAC1054CIN, DAC1054CIWM	−40°C < T_A < 85°C
DAC1054CMJ/883	−55°C < T_A < 125°C

Converter Electrical Characteristics

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\,k\Omega$ (R_L is the load resistor on the analog outputs – pins 2, 13, 17, and 23) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
STATIC CHARACTERISTICS					
n	Resolution		10	**10**	bits
	Monotonicity	(Note 10)	10	**10**	bits
	Integral Linearity Error DAC1054CIN, DAC1054CIWM	(Note 11)		**±0.75**	LSB (max)
	Differential Linearity Error			**±1.0**	LSB (max)
	Fullscale Error	(Note 12)		**±30**	mV
	Fullscale Error Tempco	(Note 13)	−38		ppm/°C
	Zero Error	(Note 14)		**±25**	mV
	Zero Error Tempco	(Note 13)	−38		ppm/°C
	Power Supply Sensitivity	(Note 15)		**−34**	dB (max)
DYNAMIC CHARACTERISTICS					
t_{s+}	Positive Voltage Output Settling Time	(Note 16) C_L = 200 pF	1.8	**3.2**	µs
t_{s-}	Negative Voltage Output Settling Time	(Note 16) C_L = 200 pF	2.3	**3.7**	µs
	Digital Crosstalk	(Note 17)	15		mV_{p-p}
	Digital Feedthrough	(Note 18)	15		mV_{p-p}
	Clock Feedthrough	(Note 19)	20		mV_{p-p}
	Channel-to-Channel Isolation	(Note 20)	−71		dB
	Glitch Energy	(Note 21)	7		nV−s
	Peak Value of Largest Glitch		38		mV
PSRR	Power Supply Rejection Ratio	(Note 22)	−49		dB

Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\,k\Omega$ (R_L is the load resistor on the analog outputs – pins 2, 13, 17, and 23) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
DIGITAL AND DC ELECTRICAL CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$AV_{CC} = DV_{CC} = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$AV_{CC} = DV_{CC} = 4.5V$		**0.8**	V (max)
I_{IL}	Digital Input Leakage Current			**1**	μA (max)
C_{IN}	Input Capacitance		4		pF
C_{OUT}	Output Capacitance		5		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{SOURCE} = 0.8$ mA		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{SINK} = 3.2$ mA		**0.4**	V (max)
V_{INT}	Interrupt Pin Output Voltage	10 kΩ Pullup		**0.4**	V (max)
I_S	Supply Current	Outputs Unloaded	14	**20**	mA
REFERENCE INPUT CHARACTERISTICS					
V_{REF}	Input Voltage Range		0–2.75		V
R_{REF}	Input Resistance		7	**4** **9**	kΩ (min) kΩ (max)
C_{REF}	Input Capacitance	Full-Scale Data Input	25		pF
V_{BIAS} INPUT CHARACTERISTICS					
V_{BIAS}	V_{BIAS} Input Voltage Range		0.3–1.4		V
	Input Leakage		1		μA
C_{BIAS}	Input Capacitance		9		pF
BANDGAP REFERENCE CHARACTERISTICS ($C_L = 220\mu F$)					
$V_{REF}OUT$	Output Voltage			**2.65 ± 2%**	V
$\Delta V_{REF}/\Delta T$	Tempco	(Note 23)	29		ppm/°C
	Line Regulation	$4.5V < V_{CC} < 5.5V$, $I_L = 4$ mA		**5**	mV
$\Delta V_{REF}/\Delta I_L$	Load Regulation	$0 < I_L < 4$ mA $-1 < I_L < 0$ mA	 2.5	**10**	mV mV
I_{SC}	Short Circuit Current	$V_{REF}OUT = 0V$	12		mA
AC ELECTRICAL CHARACTERISTICS					
t_{DS}	Data Setup Time			**15**	ns (min)
t_{DH}	Data Hold Time			**0**	ns (min)
t_{CS}	Control Setup Time			**15**	ns (min)
t_{CH}	Control Hold Time			**0**	ns (min)
f_{WMAX}	Clock Frequency Write			**10**	MHz (max)
f_{RMAX}	Clock Frequency Readback			**5**	MHz (max)
t_H	Minimum Clock High Time			**20**	ns (min)
t_L	Minimum Clock Low Time			**20**	ns (min)

Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 2, 13, 17, and 23) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS (Continued)					
t_{CZ1}	Output Hi-Z to Valid 1	$f_{CLK} = 5$ MHz		**70**	ns (max)
t_{CZ0}	Output Hi-Z to Valid 0	$f_{CLK} = 5$ MHz		**70**	ns (max)
t_{1H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF, $f_{CLK} = 5$ MHz		**150**	ns (max)
t_{0H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF, $f_{CLK} = 5$ MHz		**130**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Converter Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 30 mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{Jmax} and Θ_{JA} for the various packages and versions of the DAC1054.

Part Number	T_{Jmax} (°C)	Θ_{JA} (°C/W)
DAC1054CIN	125	42
DAC1054CIWM	125	57

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Production Reliability" of the section titled "Surface Mount" found in any current Linear Databook for other methods of soldering surface mount devices.

Note 8: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: A monotonicity of 10 bits for the DAC1054 means that the output voltage changes in the same direction (or remains constant) for each increase in the input code.

Note 11: Integral linearity error is the maximum deviation of the output from the line drawn between zero and full-scale (excluding the effects of zero error and full-scale error).

Note 12: Full-scale error is measured as the deviation from the ideal 2.800V full-scale output when $V_{REF} = 2.650V$ and $V_{BIAS} = 1.400V$.

Note 13: Full-scale error tempco and zero error tempco are defined by the following equation:

$$\text{Error tempco} = \left[\frac{\text{Error } (T_{MAX}) - \text{Error } (T_{MIN})}{V_{SPAN}}\right] \left[\frac{10^6}{T_{MAX} - T_{MIN}}\right]$$

where Error (T_{MAX}) is the zero error or full-scale error at T_{MAX} (in volts), and Error (T_{MIN}) is the zero error or full-scale error at T_{MIN} (in volts); V_{SPAN} is the output voltage span of the DAC1054, which depends on V_{BIAS} and V_{REF}.

Note 14: Zero error is measured as the deviation from the ideal 0.302V output when $V_{REF} = 2.650V$, $V_{BIAS} = 1.400V$, and the digital input word is all zeros.

Note 15: Power Supply Sensitivity is the maximum change in the offset error or the full-scale error when the power supply differs from its optimum 5V by up to 0.50V (10%). The load resistor $R_L = 2\ k\Omega$.

Note 16: Positive or negative settling time is defined as the time taken for the output of the DAC to settle to its final full-scale or zero output to within ±0.5 LSB. This time shall be referenced to the 50% point of the positive edge of $\overline{CS}$, which initiates the update of the analog outputs.

Note 17: Digital crosstalk is the glitch measured on the output of one DAC while applying an all 0s to all 1s transition at the input of the other DACs.

Note 18: All DACs have full-scale outputs latched and DI is clocked with no update of the DAC outputs. The glitch is then measured on the DAC outputs.

Note 19: Clock feedthrough is measured for each DAC with its output at full-scale. The serial clock is then applied to the DAC at a frequency of 10 MHz and the glitch on each DAC full-scale output is measured.

Note 20: Channel-to-channel isolation is a measure of the effect of a change in one DAC's output on the output of another DAC. The V_{REF} of the first DAC is varied between 1.4V and 2.65V at a frequency of 15 kHz while the change in full-scale output of the second DAC is measured. The first DAC is loaded with all 0s.

Note 21: Glitch energy is the difference between the positive and negative glitch areas at the output of the DAC when a 1 LSB digital input code change is applied to the input. The glitch energy will have its largest value at one of the three major transitions. The peak value of the maximum glitch is separately specified.

Note 22: Power Supply Rejection Ratio is measured by varying $AV_{CC} = DV_{CC}$ between 4.50V and 5.50V with a frequency of 10 kHz and measuring the proportion of this signal imposed on a full-scale output of the DAC under consideration.

Note 23: The bandgap reference tempco is defined by the largest value from the following equations:

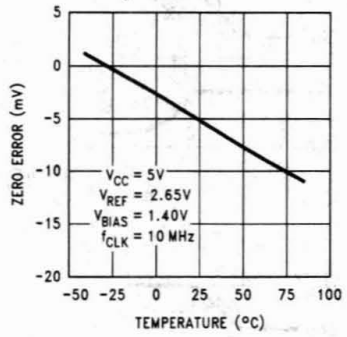
$$\text{Tempco } (T_{MAX}) = \left[\frac{V_{REF}\ (T_{MAX}) - V_{REF}\ (T_{ROOM})}{V_{REF}\ (T_{ROOM})}\right] \left[\frac{10^6}{T_{MAX} - T_{ROOM}}\right] \text{ or Tempco } (T_{MIN}) = \left[\frac{V_{REF}\ (T_{MIN}) - V_{REF}\ (T_{ROOM})}{V_{REF}\ (T_{ROOM})}\right] \left[\frac{10^6}{T_{ROOM} - T_{MIN}}\right]$$

where $T_{ROOM} = 25°C$, V_{REF} (T_{MAX}) is the reference output at T_{MAX}, and similarly for V_{REF} (T_{MIN}) and V_{REF} (T_{ROOM}).

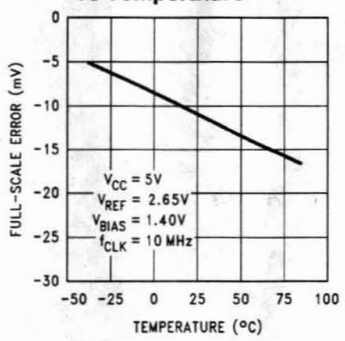
Note 24: A Military RETS specification is available upon request.

Typical Converter Performance Characteristics

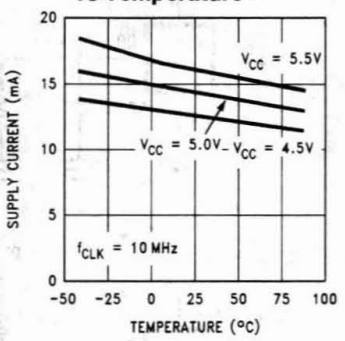
Zero Error vs Temperature



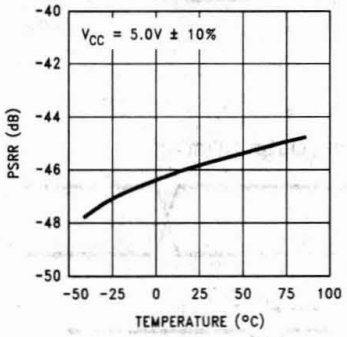
Full-Scale Error vs Temperature



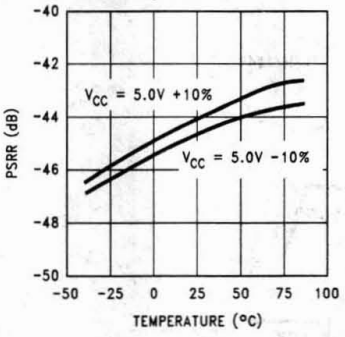
Supply Current vs Temperature



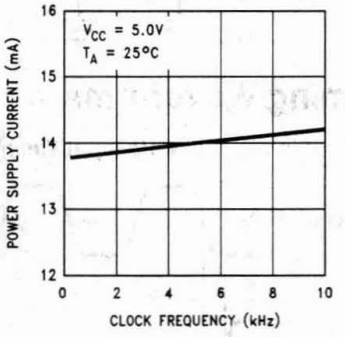
Zero Error PSRR vs Temperature



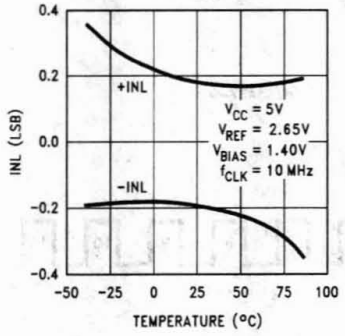
Full-Scale Error PSRR vs Temperature



Supply Current vs Clock Frequency



Integral Non-Linearity Error vs Temperature



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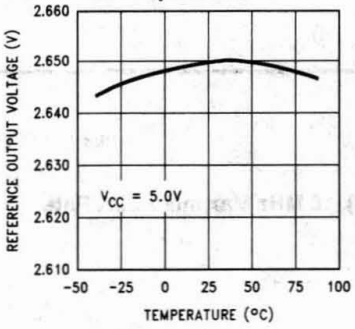
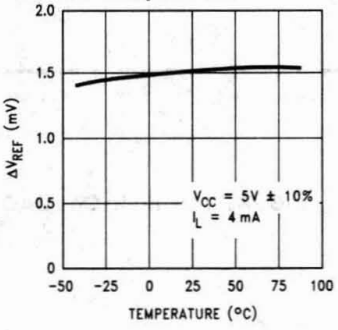
Typical Reference Performance Characteristics

Bandgap Voltage vs Temperature



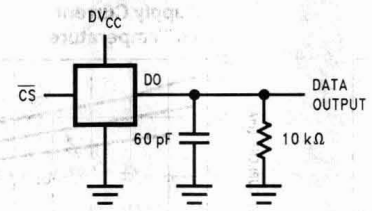
TL/H/11437–3

Line Regulation vs Temperature



TL/H/11437–4

TRI-STATE Test Circuits and Waveforms



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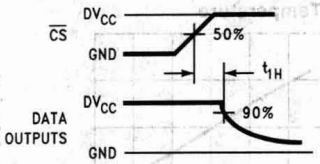

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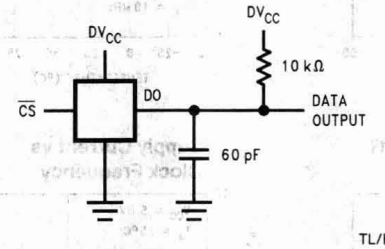

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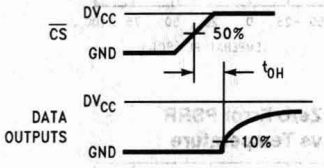

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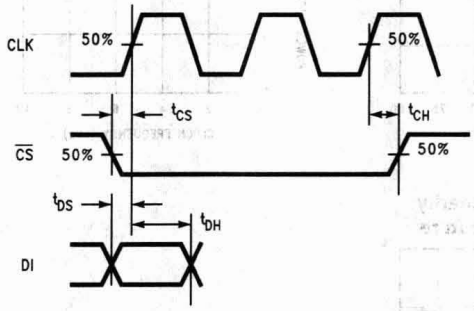
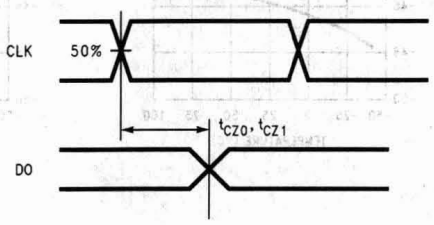
Timing Waveforms

Data Input Timing



TL/H/11437-9

Data Output Timing



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Timing Diagrams

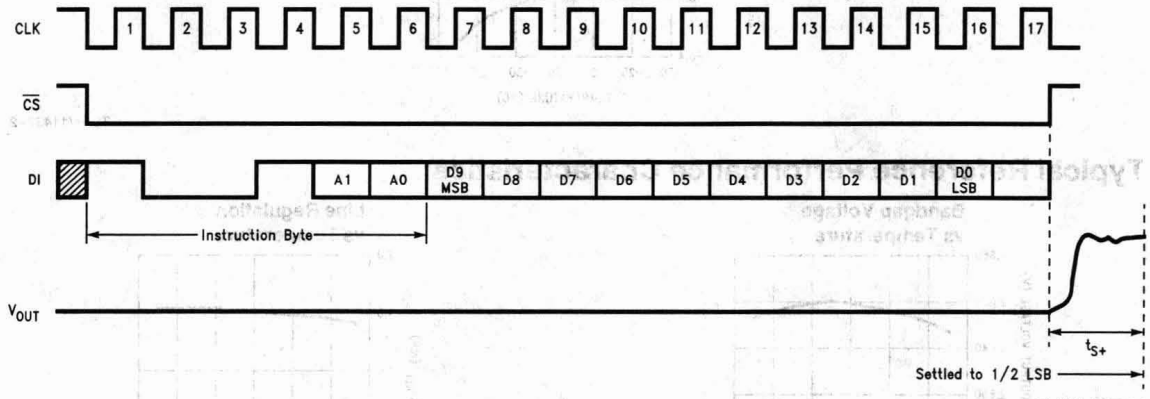

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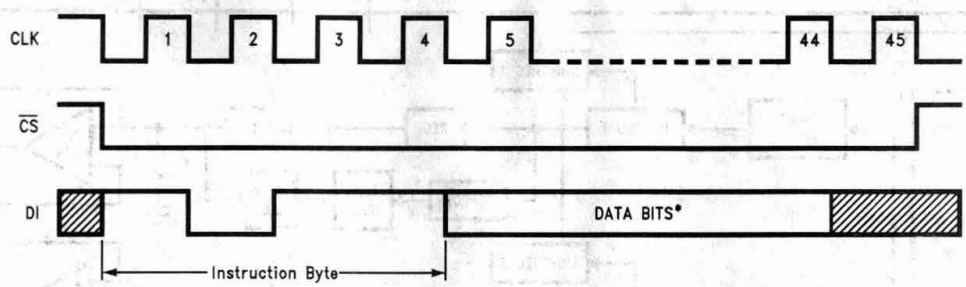
FIGURE 1. Write to One DAC with Update of Output ($\overline{AU}$ = 1), 10 MHz Maximum CLK Rate

Timing Diagrams (Continued)



* DACs are written to MSB first.
DAC1 is written to first, then DACs 2, 3, and 4.

FIGURE 2. Write to All DACs with Update of Outputs ($\overline{AU}$ = 1), 10 MHz Maximum CLK Rate

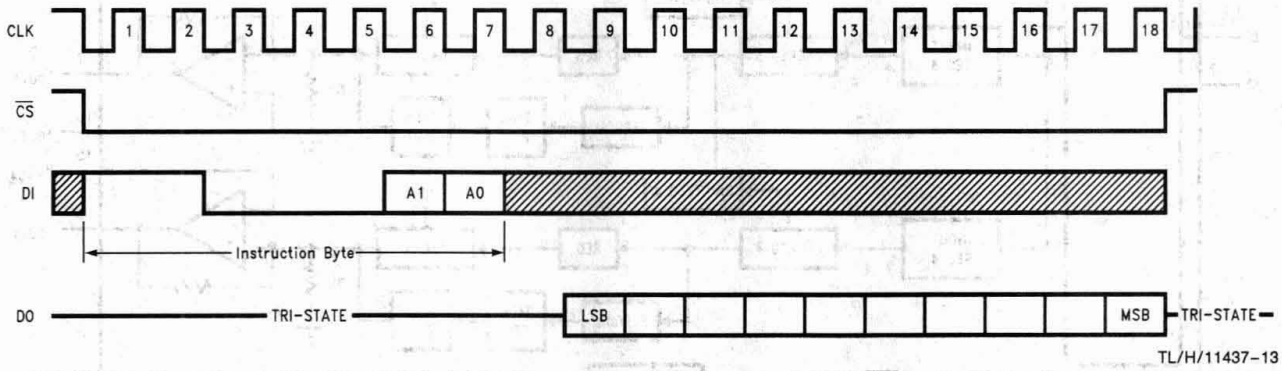
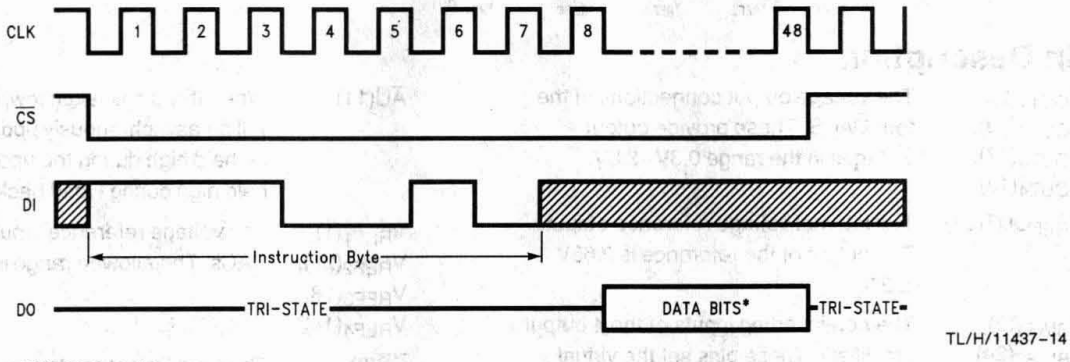


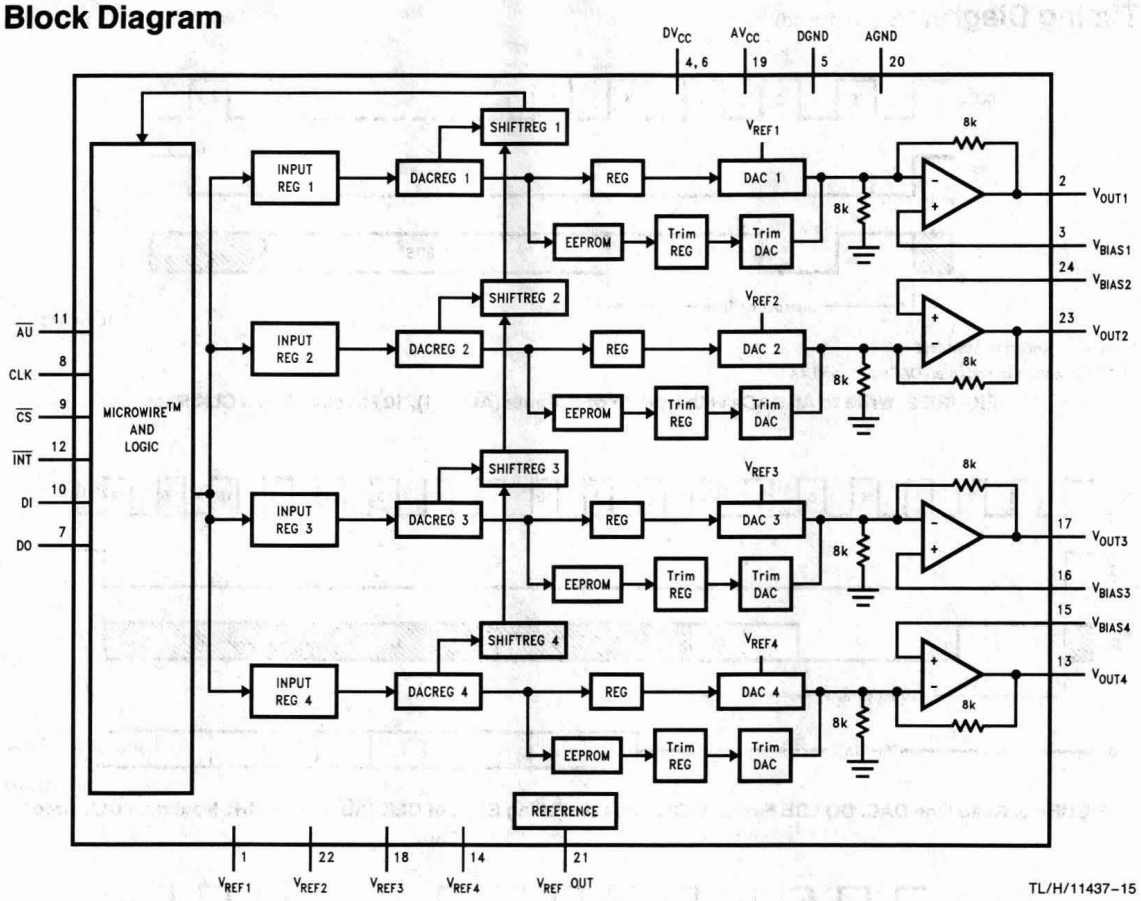
FIGURE 3. Read One DAC, DO LSB First, DO Changes on Falling Edge of CLK ($\overline{AU}$ = 1), 5 MHz Maximum CLK Rate



*DAC1 is read first, then DACs 2, 3, and 4.

FIGURE 4. Read All DACs, DO LSB First, DO Changes on Falling Edge of CLK ($\overline{AU}$ = 1), 5 MHz Maximum CLK Rate

Block Diagram



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Pin Description

V_{OUT1}(2), V_{OUT2}(23), V_{OUT3}(17), V_{OUT4}(13)	The voltage output connections of the four DACS. These provide output voltages in the range 0.3V–2.8V.
V_{REF}OUT(21)	The internal voltage reference output. The output of the reference is 2.65V ±2%.
V_{BIAS1}(3), V_{BIAS2}(24), V_{BIAS3}(16), V_{BIAS4}(15)	The non-inverting inputs of the 4 output amplifiers. These pins set the virtual ground voltage for the respective DACs. The allowed range is 0.3V–1.4V.
AGND(20), DGND(5)	The analog and digital ground pins.
DV_{CC}(4, 6), AV_{CC}(19)	The digital and analog power supply pins. The power supply range of the DAC1054 is 4.5V–5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} pins be bypassed separately with bypass capacitors of 10 μF tantalum in parallel with 0.1 μF ceramic.
$\overline{AU}$(11)	When this pin is taken low, all DAC outputs will be asynchronously updated. $\overline{CS}$ must be held high during the update. $\overline{AU}$ must be held high during Read back.
V_{REF1}(1), V_{REF2}(22), V_{REF3}(18), V_{REF4}(14)	The voltage reference inputs for the four DACs. The allowed range is 0V–2.75V.
$\overline{CS}$(9)	The Chip Select control input. This input is active low.
CLK(8)	The external clock input pin.
DI(10)	The serial data input. The data is clocked in MSB first. Preceding the data byte are 4 or 6 bits of instructions. The read back command requires 7 bits of instructions.
DO(7)	The serial data output. The data can be clocked out either MSB or LSB first, and on either the positive or negative edge of the clock.
$\overline{INT}$(12)	The power interrupt output. On an interruption of the digital power supply, this pin goes low. Since this pin has an open drain output, a 10 kΩ pull-up resistor must be connected to the supply.

Applications Information

FUNCTIONAL DESCRIPTION

The DAC1054 is a monolithic quad 10-bit digital-to-analog converter that is designed to operate on a single 5V supply. Each of the four units is comprised of an input register, a DAC register, a shift register, a current output DAC, and an output amplifier. In addition, the DAC1054 has an onboard bandgap reference and a logic unit which controls the internal operation of the DAC1054 and interfaces it to microprocessors.

Each of the four internal 10-bit DACs uses a modified R-2R ladder to effect the digital-to-analog conversion *(Figure 5)*. The resistances corresponding to the 2 most significant bits are segmented to reduce glitch energy and to improve matching. The bottom of the ladder has been modified so that the voltage across the LSB resistor is much larger than the input offset voltage of the buffer amplifier. The input digital code determines the state of the switches in the ladder network. An internal EEPROM, which is programmed at the factory, is used to correct for linearity errors in the resistor ladder of each of the four internal DACs. The codes stored in the EEPROM's memory locations are converted to a current, I_{EEPROM}, with a small trim DAC. The sum of currents I_{OUT1} and I_{OUT2} is fixed and is given by

$$I_{OUT1} + I_{OUT2} = \left(\frac{V_{REF} - V_{BIAS}}{R}\right)\frac{1023}{1024}$$

The current output I_{OUT2}, summed with the correction current I_{EEPROM}, is applied to the internal output amplifier and converted to a voltage. The output voltage of each DAC is a function of V_{BIAS}, V_{REF}, and the digital input word, and is given by

$$V_{OUT} = 2\,(V_{REF} - V_{BIAS})\frac{DATA}{1024} + \frac{2047}{512}V_{BIAS} - \frac{1023}{512}V_{REF}$$

The output voltage range for each DAC is 0.3V–2.8V. This range can be achieved by using the internal 2.65V reference and a voltage divider network which provides a V_{BIAS} of 1.40V *(Figure 6)*. In this case the DAC transfer function is

$$V_{OUT} = 2.5\frac{(DATA)}{1024} + 0.30244$$

The output impedance of any external reference that is used will affect the accuracy of the conversion. In order that this error be less than ½ LSB, the output impedance of the external reference must be less than 2Ω.

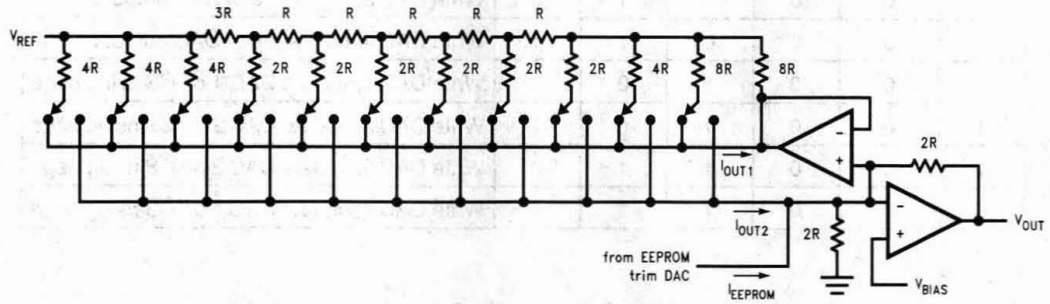

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FIGURE 5. Equivalent Circuit of R-2R Ladder and Output Amplifier

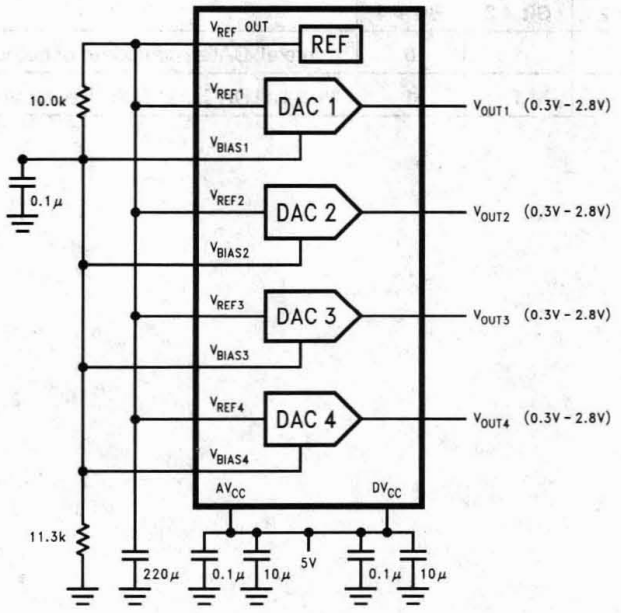

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FIGURE 6. Generating a V_{BIAS} = 1.40V from the Internal Reference, Typical Application

Digital Interface

The DAC1054 has two interface modes: a WRITE mode and a READ mode. The WRITE mode is used to convert a 10-bit digital input word into a voltage. The READ mode is used to read back the digital data that was sent to one or all of the DACs. The WRITE mode maximum clock rate is 10 MHz. READ mode is limited to a 5 MHz maximum clock rate. These modes are selected by the appropriate setting of the RD/$\overline{WR}$ bit, which is part of the instruction byte. The instruction byte precedes the data byte at the DI pin. In both modes, a high level on the Start Bit (SB) alerts the DAC to respond to the remainder of the input stream.

Table I lists the instruction set for the WRITE mode when writing to only a single DAC, and Table II lists the instruction set for a global write. Bits A0 and A1 select the DAC to be written to. The DACs are always written to MSB first. All DACs will be written to sequentially if the global bit (G) is high; DAC 1 is written to first, then DACs 2, 3 and 4 (in that order). For a global write bits A0 and A1 of the instruction byte are not required (see *Figure 2* timing diagram). If the update bit (U) is high, then the DAC output(s) will be updated on the rising edge of $\overline{CS}$; otherwise, the new data byte will be placed only in the input register. Chip Select ($\overline{CS}$) must remain low for at least one clock cycle after the last data bit has been entered. (See *Figures 1* and *2*)

When the U bit is set low an asynchronous update of all the DAC outputs can be achieved by taking $\overline{AU}$ low. The contents of the input registers are loaded into the DAC registers, with the update occurring on the falling edge of $\overline{AU}$. $\overline{CS}$ must be held high during an asynchronous update.

All DAC registers will have their contents reset to all zeros on power up.

TABLE I. WRITE Mode Instruction Set (Writing to a Single DAC)

SB	RD/$\overline{WR}$	G	U	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	
1	0	0	0	0	0	Write DAC 1, no update of DAC outputs
1	0	0	0	0	1	Write DAC 2, no update of DAC outputs
1	0	0	0	1	0	Write DAC 3, no update of DAC outputs
1	0	0	0	1	1	Write DAC 4, no update of DAC outputs
1	0	0	1	0	0	Write DAC 1, update DAC 1 on $\overline{CS}$ rising edge
1	0	0	1	0	1	Write DAC 2, update DAC 2 on $\overline{CS}$ rising edge
1	0	0	1	1	0	Write DAC 3, update DAC 3 on $\overline{CS}$ rising edge
1	0	0	1	1	1	Write DAC 4, update DAC 4 on $\overline{CS}$ rising edge

TABLE II. WRITE Mode Instruction Set (Writing to all DACs)

SB	RD/$\overline{WR}$	G	U	Description
Bit # 1	Bit #2	Bit #3	Bit #4	
1	0	1	0	Write all DACs, no update of outputs
1	0	1	1	Write all DACs, update all outputs on $\overline{CS}$ rising edge

Digital Interface (Continued)

Table III lists the instruction set for the READ mode. By the appropriate setting of the global (G) and address (A1 and A0) bits, one can select a specific DAC to be read, or one can read all the DACs in succession, starting with DAC 1. The R/$\overline{F}$ bit determines whether the data changes on the rising or the falling edge of the system clock. With the R/$\overline{F}$ bit high, DO goes out of TRI-STATE on the rising edge that occurs 1½ clock cycles after the end of the instruction byte; the data will continue to be sequentially clocked out by the following rising clock edges. With the R/$\overline{F}$ bit low, DO goes out of TRI-STATE on the falling edge that occurs 1 clock cycle after the end of the instruction byte; the data will continue to be sequentially clocked by the next falling clock edges. The rising edge of $\overline{CS}$ returns DO to TRI-STATE. Read back with the R/$\overline{F}$ bit set high is not MICROWIRE compatible. One can choose to read the data back MSB first or LSB first by setting the M/$\overline{L}$ bit. (See *Figures 3* and *4*)

TABLE III. READ MODE Instruction Set

SB	RD/$\overline{WR}$	G	R/$\overline{F}$	M/$\overline{L}$	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	Bit #7	
1	1	0	0	0	0	0	Read DAC 1, LSB first, data changes on the falling edge
1	1	0	0	0	0	1	Read DAC 2, LSB first, data changes on the falling edge
1	1	0	0	0	1	0	Read DAC 3, LSB first, data changes on the falling edge
1	1	0	0	0	1	1	Read DAC 4, LSB first, data changes on the falling edge
1	1	0	0	1	0	0	Read DAC 1, MSB first, data changes on the falling edge
1	1	0	0	1	0	1	Read DAC 2, MSB first, data changes on the falling edge
1	1	0	0	1	1	0	Read DAC 3, MSB first, data changes on the falling edge
1	1	0	0	1	1	1	Read DAC 4, MSB first, data changes on the falling edge
1	1	0	1	0	0	0	Read DAC 1, LSB first, data changes on the rising edge
1	1	0	1	0	0	1	Read DAC 2, LSB first, data changes on the rising edge
1	1	0	1	0	1	0	Read DAC 3, LSB first, data changes on the rising edge
1	1	0	1	0	1	1	Read DAC 4, LSB first, data changes on the rising edge
1	1	0	1	1	0	0	Read DAC 1, MSB first, data changes on the rising edge
1	1	0	1	1	0	1	Read DAC 2, MSB first, data changes on the rising edge
1	1	0	1	1	1	0	Read DAC 3, MSB first, data changes on the rising edge
1	1	0	1	1	1	1	Read DAC 4, MSB first, data changes on the rising edge
1	1	1	0	0	1	0	Read all DACs, LSB first, data changes on the falling edge
1	1	1	0	1	1	0	Read all DACs, MSB first, data changes on the falling edge
1	1	1	1	0	1	0	Read all DACs, LSB first, data changes on the rising edge
1	1	1	1	1	1	0	Read all DACs, MSB first, data changes on the rising edge

Power Fail Function

The DAC1054 powers up with the $\overline{INT}$ pin in a Low state. To force this output high and reset this flag, the $\overline{CS}$ pin will have to be brought low. When this is done the $\overline{INT}$ output will be pulled high again via an external 10 kΩ pull-up resistor. Anytime a power failure occurs on the DV_{CC} line, the $\overline{INT}$ will be set low when power is reapplied. This feature may be used by the microprocessor to discard data whose integrity is in question.

Power Supplies

The DAC1054 is designed to operate from a +5V (nominal) supply. There are two supply lines, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply lines should each be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

3

Typical Applications

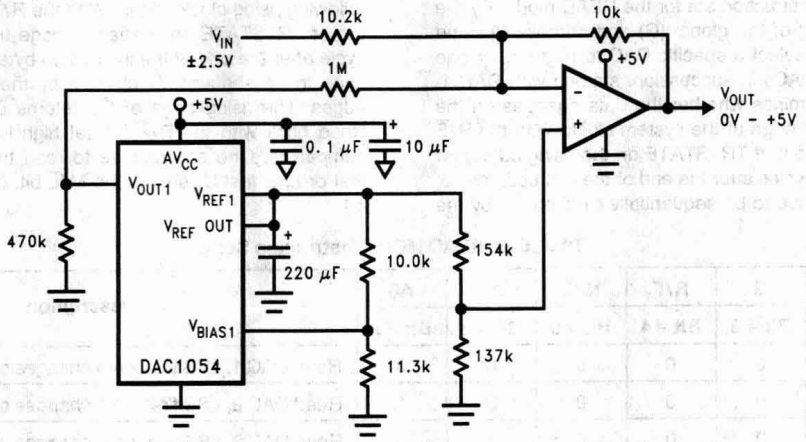

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FIGURE 7. Trimming the Offset of a 5V Op Amp Whose Output is Biased at 2.5V

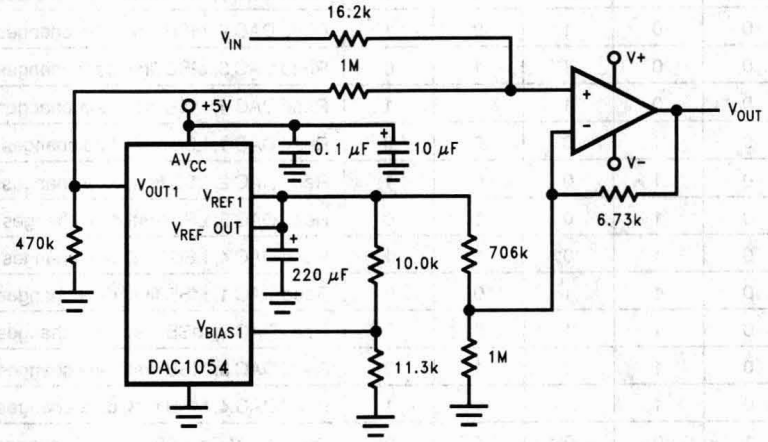

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FIGURE 8. Trimming the Offset of a Dual Supply Op Amp (V_{IN} is Ground Referenced)

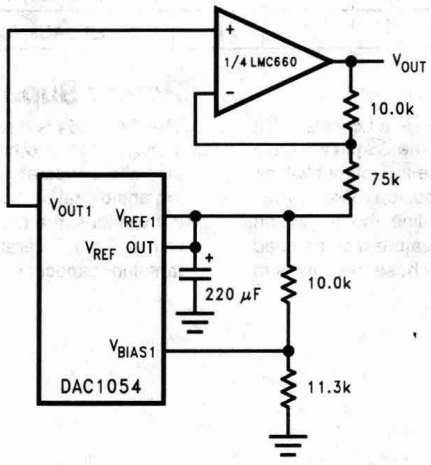

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FIGURE 9. Bringing the Output Range Down to Ground

National Semiconductor

MICRO-DAC™ DAC1208/DAC1209/DAC1210/DAC1230/DAC1231/DAC1232 12-Bit, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

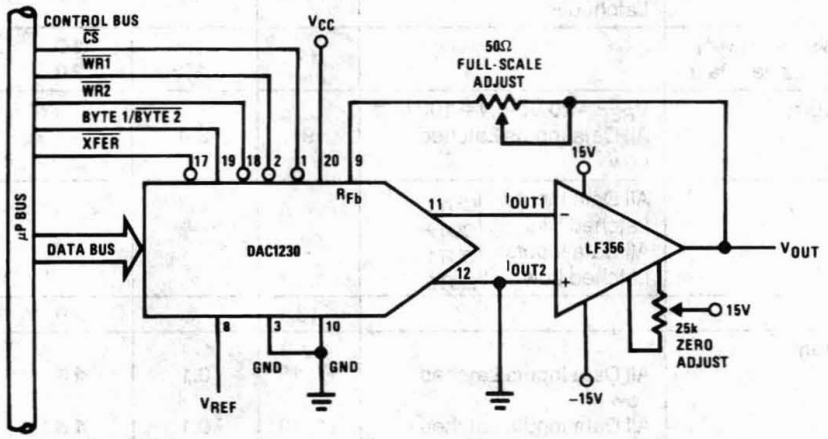
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
■ Gain Tempco	1.3 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at $T_A = 25°C$ (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability	800V

Operating Conditions

Lead Temperature (Soldering, 10 sec.)	300°C
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1208LCJ, DAC1209LCJ, DAC1210LCJ, DAC1230LCJ, DAC1231LCJ, DAC1232LCJ, DAC1231LIN, DAC1232LIN	$-40°C \le T_A \le +85°C$
DAC1208LCJ-1, DAC1210LCJ-1, DAC1230LCJ-1, DAC1231LCJ-1, DAC1232LCJ-1, DAC1231LCN, DAC1232LCN, DAC1231LCWM, DAC1232LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

$V_{REF} = 10.000\ V_{DC}$, $V_{CC} = 11.4\ V_{DC}$ to $15.75\ V_{DC}$ unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted	4, 7, 13				
	DAC1208, DAC1230			**±0.018**	**±0.018**	% of FSR
	DAC1209, DAC1231			**±0.024**	**±0.024**	% of FSR
	DAC1210, DAC1232			**±0.050**	**±0.05**	% of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted	4, 7, 13				
	DAC1208, DAC1230			**±0.018**	**±0.018**	% of FSR
	DAC1209, DAC1231			**±0.024**	**±0.024**	% of FSR
	DAC1210, DAC1232			**±0.050**	**±0.05**	% of FSR
Monotonicity		4	12	**12**	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb} $V_{ref} = \pm 10V, \pm 1V$	7	−0.1	0.0		% of FSR
Gain Error (Max)		7	−0.1	−0.2		% of FSR
Gain Error Tempco		7	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs Latched High	7	±3.0	±30		ppm of FSR/V
Reference Input Resistance (Min)		13	15	**10**	**10**	kΩ
Reference Input Resistance (Max)			15	**20**	**20**	kΩ
Output Feedthrough Error	$V_{REF} = 20$ Vp-p, f = 100 kHz All Data Inputs Latched Low	9	3.0			mVp-p
Output Capacitance	All Data Inputs Latched High	I_{OUT1}			200	pF
		I_{OUT2}			70	pF
	All Data Inputs Latched Low	I_{OUT1}			70	pF
		I_{OUT2}			200	pF
Supply Current Drain		13		2.0	**2.5**	mA
Output Leakage Current I_{OUT1}	All Data Inputs Latched Low	11, 13	0.1	**15**	**15**	nA
I_{OUT2}	All Data Inputs Latched High	11, 13	0.1	**15**	**15**	nA
Digital Input Threshold	Low Threshold	13		**0.8**	**0.8**	V_{DC}
	High Threshold	13		**2.2**	**2.2**	V_{DC}
Digital Input Currents	Digital Inputs <0.8V	13		**−200**	**−200**	μA_{DC}
	Digital Inputs >2.2V	13		**10**	**10**	μA_{DC}

Electrical Characteristics (Continued)

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	See Note	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
AC CHARACTERISTICS							
t_s	Current Setting Time	V_{IL} = 0V, V_{IH} = 5V		1.0			µs
t_W	Write and XFER Pulse Width Min.	V_{IL} = 0V, V_{IH} = 5V	8	50		320 **320**	ns
t_{DS}	Data Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		70		320 **320**	
t_{DH}	Data Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		30		90 **90**	
t_{CS}	Control Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		60		320 **320**	
t_{CH}	Control Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		0		10	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels. Guaranteed for V_{CC} = 11.4V to 15.75V and V_{REF} = −10V to +10V.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR(parts per million of full-scale range) and ppm of FS(parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of ±(6)($V_{REF}/10^6$)(125°C) or ±0.75 (10^{-3}) V_{REF} which is ±0.075% of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Typicals are at 25°C and represent the most likely parametric norm.

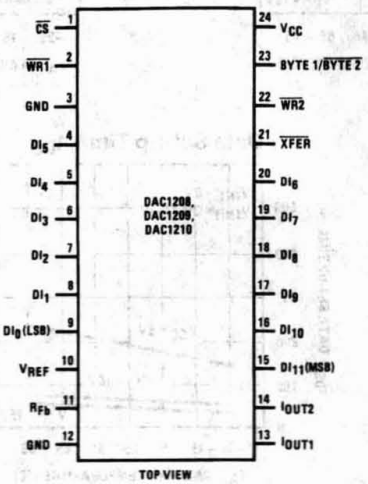
Note 11: A 10 nA leakage current with R_{Fb} = 20k and V_{REF} = 10V corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Note 12: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 13: Tested limit for −1 suffix parts applies only at 25°C.

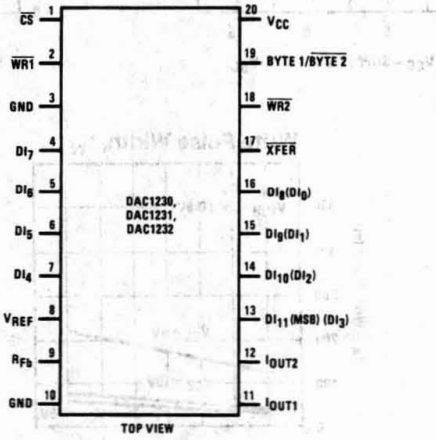
Connection Diagrams

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

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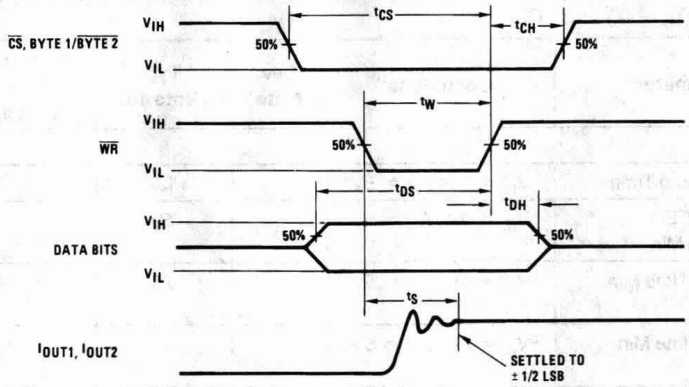
See Ordering Information

Switching Waveforms



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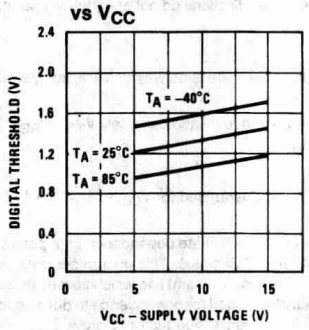
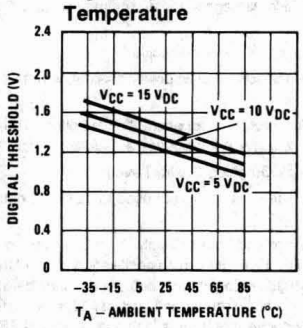
Typical Performance Characteristics

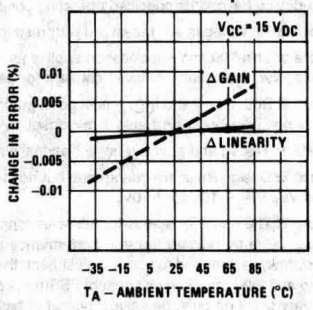
Digital Input Threshold vs V_{CC}



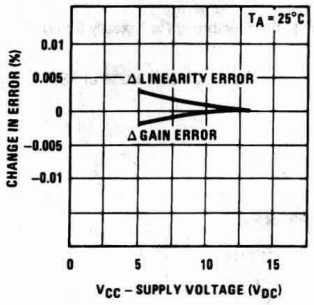
Digital Input Threshold vs Temperature



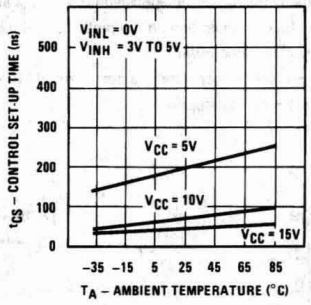
Gain and Linearity Error Variation vs Temperature



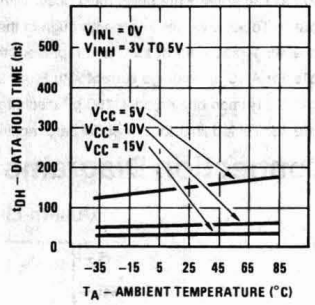
Gain and Linearity Error Variation vs Supply Voltage



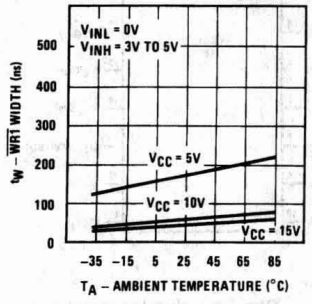
Control Set-Up Time, t_{CS}



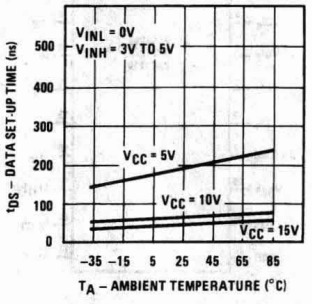
Data Hold Time, t_{DH}



Write Pulse Width, t_W



Data Set-Up Time, t_{DS}



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Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated)

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1. The active low $\overline{WR1}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR1}$ is high. The 12-bit input latch is split into two latches. One holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{Byte\ 2}$ control pin is used to select both latches when Byte 1/$\overline{Byte\ 2}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{Byte\ 2}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{WR2}$: Write 2 (active low). The $\overline{WR2}$ will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer Control Signal (active low). This signal, in combination with $\overline{WR2}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Pins 3 and 12 of the DAC1208, DAC1209, and DAC1210 must be connected to ground. Pins 3 and 10 of the DAC1230, DAC1231, and DAC1232 must be connected to ground. It is important that I_{OUT_1} and I_{OUT_2} are at ground potential for current switching applications. Any difference of potential (V_{OS} on these pins) will result in a linearity change of

$$\frac{V_{OS}}{3\ V_{REF}}$$

For example, if $V_{REF} = 10V$ and these ground pins are 9 mV offset from I_{OUT_1} and I_{OUT_2}, the linearity change will be 0.03%.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

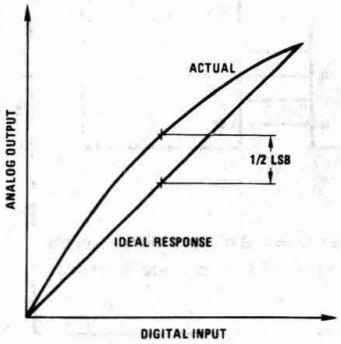
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ±½ LSB of the final output value.

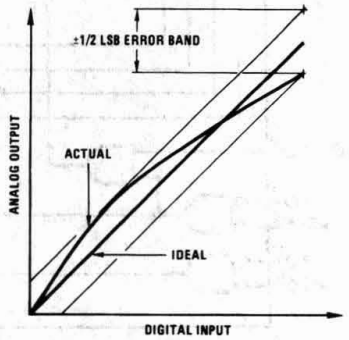
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End Point Test After Zero and FS Adjust



b) Shifting FS Adjust to Pass Best Straight Line Test

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Application Hints

1.0 DIGITAL INTERFACE

These DACs are designed to provide all of the necessary digital input circuitry to permit a direct interface to a wide variety of microprocessor systems. The timing and logic level convention of the input control signals allow the DACs to be treated as a typical memory device or I/O peripheral with no external logic required in most systems. Essentially these DACs can be mapped as a two-byte stack in memory (or I/O space) to receive their 12 bits of input data in two successive 8-bit data writing sequences. The DAC1230 series is intended for use in systems with an 8-bit data bus. The DAC1208 series provides all 12 digital input lines which can be externally configured to be controlled from an 8-bit bus or can be driven directly from a 16-bit data bus.

All of the digital inputs to these DACs contain a unique threshold regulator circuit to maintain TTL voltage level compatibility independent of the applied V_{CC} to the DAC. Any input can also be driven from higher voltage CMOS logic levels in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. As a troubleshooting aid, if any digital input is inadvertently left floating, the DAC will interpret the pin as a logic "1".

Double buffered digital inputs allow the DAC to internally format the 12-bit word used to set the current switching R-2R ladder network (see section 2.0) from two 8-bit data write cycles. *Figures 1* and *2* show the internal data registers and their controlling logic circuitry. The timing diagrams for updating the DAC output are shown in sections 1.1, 1.2 and 1.3 for three possible control modes. The method used depends strictly upon the particular application.

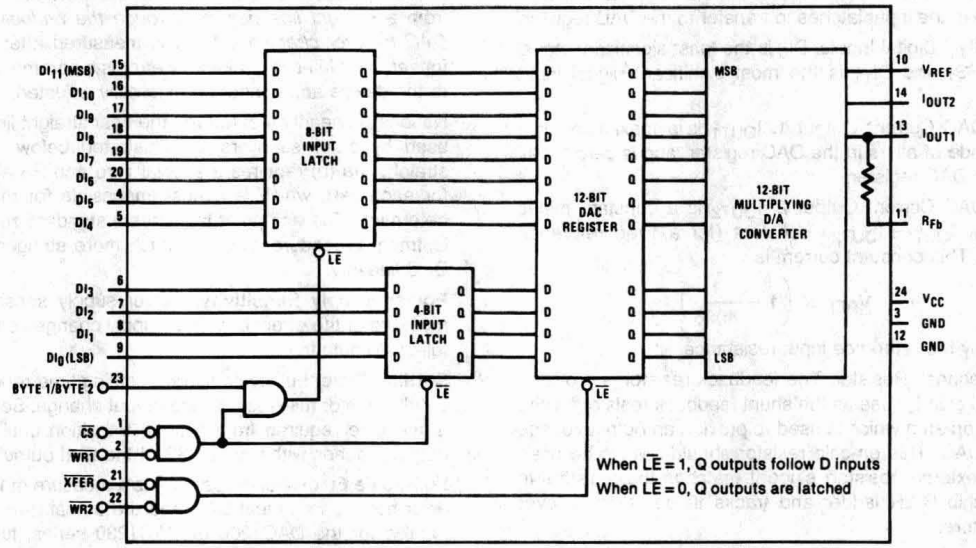

FIGURE 1. DAC1208, DAC1209, DAC1210 Functional Diagram

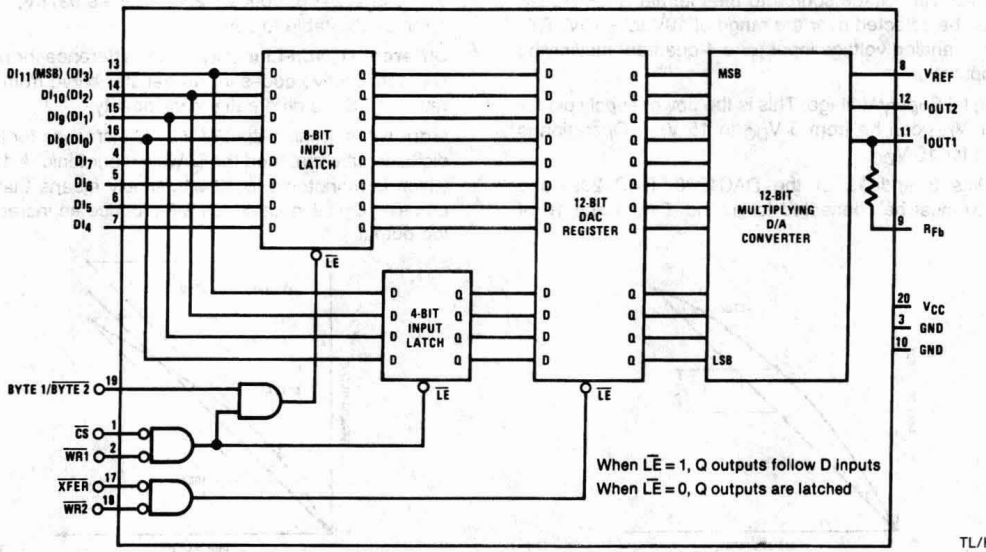

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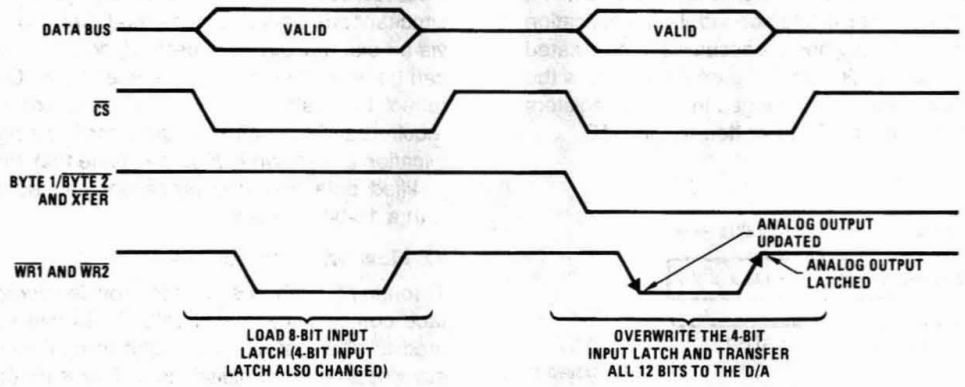
FIGURE 2. DAC1230, DAC1231, DAC1232 Functional Diagram

Application Hints (Continued)

1.1 Automatic Transfer

The 12-bit DAC word is automatically transferred to the DAC register and the R-2R ladder when the second write (the 4 LSBs of the data) occurs.


DATA BUS
VALID
VALID
CS
BYTE 1/BYTE 2 AND XFER
WR1 AND WR2
ANALOG OUTPUT UPDATED
ANALOG OUTPUT LATCHED
LOAD 8-BIT INPUT LATCH (4-BIT INPUT LATCH ALSO CHANGED)
OVERWRITE THE 4-BIT INPUT LATCH AND TRANSFER ALL 12 BITS TO THE D/A

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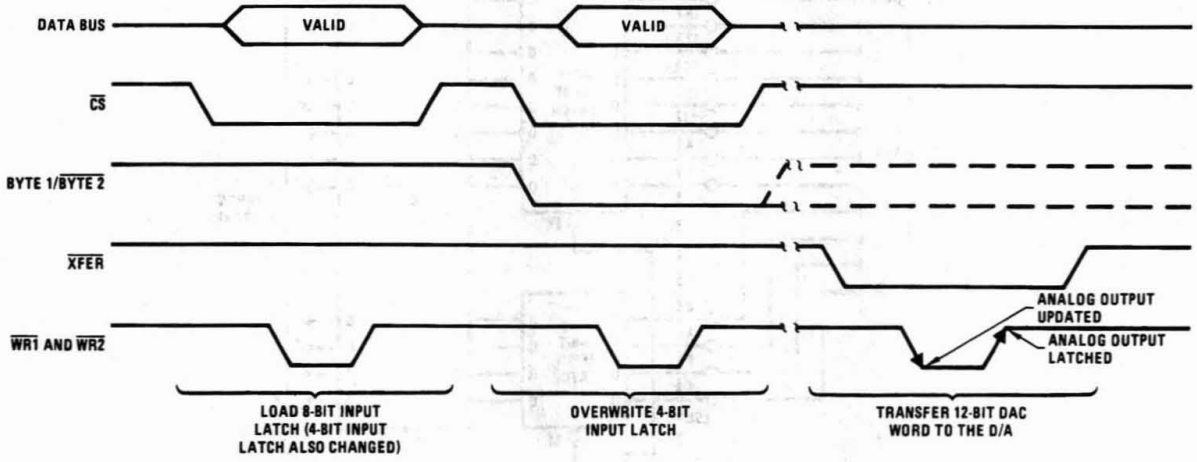
1.2 Independent Processor Transfer Control

In this case a separate address is decoded to provide the $\overline{XFER}$ signal. This allows the processor to load the next required DAC word but not change the analog output until some time later, most useful for the simultaneous updating of several DACs in a system where their $\overline{XFER}$ lines would be tied together.



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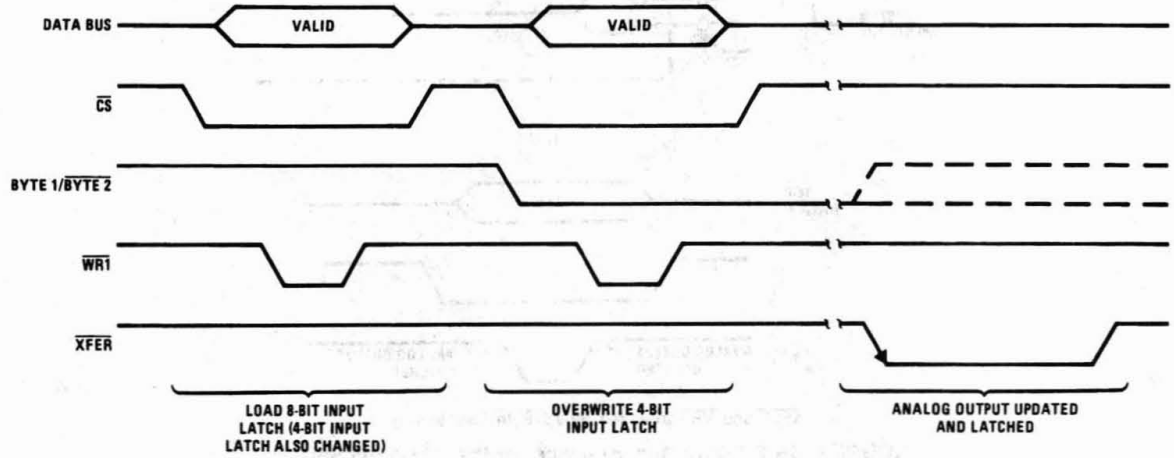
1.3 Transfer via an External Strobe

This method is basically the same as the previous operation except the $\overline{XFER}$ signal is provided by a device other than the processor. This allows the DAC to hold the code for a conditional analog output signal which will be required on demand from an external monitoring device (an analog voltage comparator for instance).



$\overline{WR2}$ tied to a logic low (0V)

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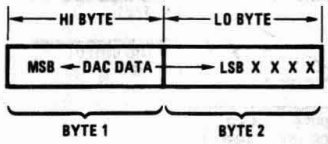
Application Hints (Continued)

1.4 Left-Justified Data Format

It is important to realize that the input registers of these DACs are arranged to accept a left-justified data word from the microprocessor with the most significant 8 bits coming first (Byte 1) and the lower 4 bits second. Left justification simply means that the binary point is assumed to be located to the left of the most significant bit. *Figure 3* shows how the 12 bits of DAC data should be arranged in 2 8-bit registers of an 8-bit processor before being written to the DAC.



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X = don't care

FIGURE 3. Left-Justified Data Format

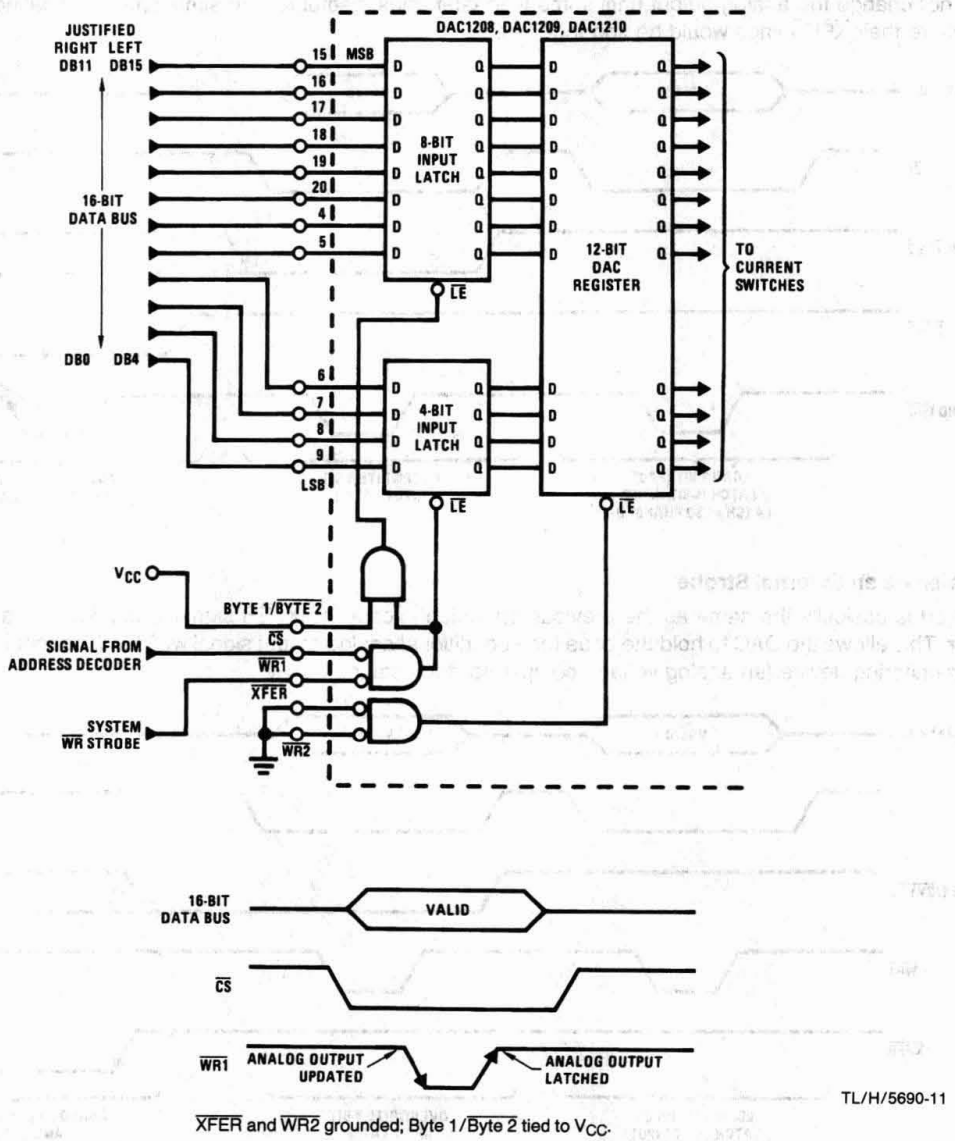
1.5 16-Bit Data Bus Interface

The DAC1208 series provides all 12 digital input lines to permit a direct parallel interface to a 16-bit data bus. In this instance, double buffering is not always necessary (unless a simultaneous updating of several DACs or a data transfer via an external strobe is desired) so the 12-bit DAC register can be wired to flow-through whereby its Q outputs always reflect the state of its D inputs. The external connections required and the timing diagram for this single buffered application are shown in *Figure 4*. Note that either left or right-justified data from the processor can be accommodated with a 16-bit data bus.

1.6 Flow-Through Operation

Through primarily designed to provide microprocessor interface compatibility, the MICRO-DACs can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in appli-

Interface Timing



TL/H/5690-11

XFER and WR2 grounded; Byte 1/Byte 2 tied to V_{CC}.

FIGURE 4. 16-Bit Data Bus Interface for the DAC1208 Series

Application Hints (Continued)

cations where the DAC is used in a continuous feedback control loop and is driven by a binary up/down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Only the DAC1208, DAC1209, DAC1210 devices can have all 12 inputs flow-through. Simply grounding $\overline{CS}$, $\overline{WR1}$, $\overline{WR2}$ and $\overline{XFER}$ and tying Byte 1/$\overline{Byte\ 2}$ high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.7 Address Decoding Tips

It is possible to map the MICRO-DACs into system ROM space to allow more efficient use of existing address decoding hardware. The DAC in effect can share the same addresses of any number of ROM locations. The ROM outputs will only be enabled by a READ of its address (gated by the system READ strobe) and the DAC will only accept data that is written to the same address (gated by the system WRITE strobe).

The Byte 1/$\overline{Byte\ 2}$ control function can easily be generated by the processor's least significant address bit (A0) by placing the DAC at two consecutive address locations and utilizing double-byte WRITE instructions which automatically increment or decrement the address. The $\overline{CS}$ and $\overline{XFER}$ signals can then be decoded from the remaining address bits. Care must be taken in selecting the actual address used for Byte 1 of the DAC to prevent a carry (as a result of incrementing the address for Byte 2) from propagating through the address word and changing any of the bits decoded for $\overline{CS}$ or $\overline{XFER}$. *Figure 5* shows how to prevent this effect.

The same problem can occur from a borrow when an auto-decremented address is used; but only if the processor's address outputs are inverted before being decoded.

1.8 Control Signal Timing

When interfacing these MICRO-DACs to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 320 ns for V_{CC} = 11.4V to 15.75V and operation over temperature, but typically a pulse width of only 250 ns is adequate. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulse

Write Cycle	Address Bits			
	15 ... 2		1*	0**
First (Byte 1)	Decoded to Address DAC		0	1
Second (Byte 2)			1	0

*Starting with a 0 prevents a carry on address incrementing.

**Used as Byte 1/$\overline{Byte2}$ Control.

FIGURE 5

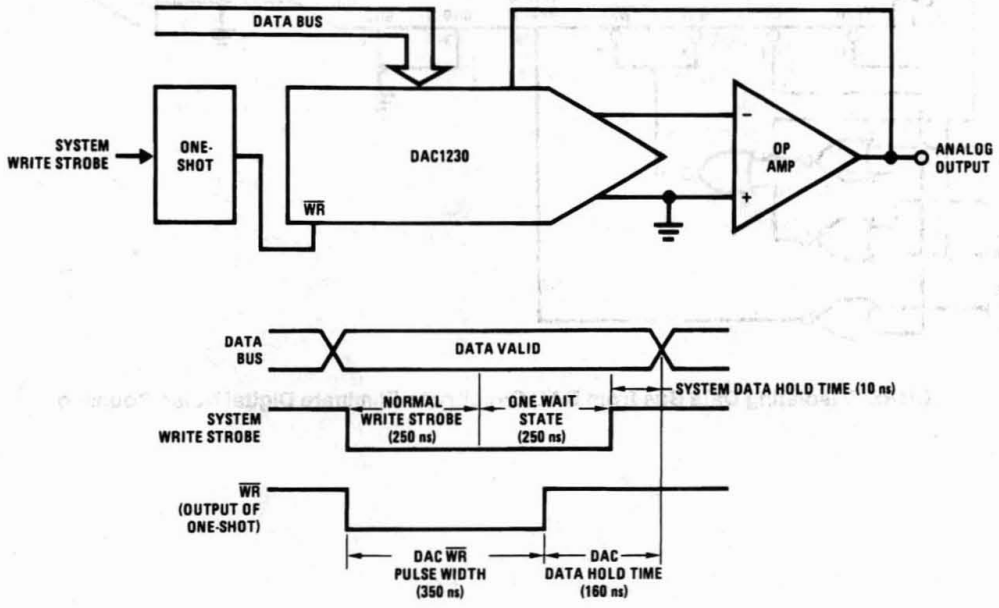


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FIGURE 6. Accommodating a High Speed System

Application Hints (Continued)

width. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 6* for an exemplary system which provides a 250 ns $\overline{WR}$ strobe time with a data hold time of only 10 ns.

The proper data set-up time prior to the latching edge (low to high transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulse width is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.9 Digital Signal Feedthrough

A typical microprocessor is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and may cause fast transients to appear at the DAC output, even when data is latched internally.

In low frequency or DC applications, low pass filtering can reduce the magnitude of any fast transients. This is most easily accomplished by over-compensating the DAC output amplifier by increasing the value of its feedback capacitor.

In applications requiring a fast output response from the DAC and op amp, filtering may not be feasible. In this event, digital signals can be completely isolated from the DAC circuitry, by the use of a DM74LS374 latch, until a valid $\overline{CS}$ signal is applied to update the DAC. This is shown in *Figure 7*.

A single TRI-STATE® data buffer such as the DM81LS95 can be used to isolate any number of DACs in a system. *Figure 8* shows this isolating circuitry and decoding hardware for a multiple DAC analog output card. Pull-up resistors are used on the buffer outputs to limit the impedance at the DAC digital inputs when the card is not selected. A unique feature of this card is that the DAC $\overline{XFER}$ strobes are controlled by the data bus. This allows a very flexible update of any combination of analog outputs via a transfer word which would contain a zero in the bit position assigned to any of the DACs required to change to a new output value.

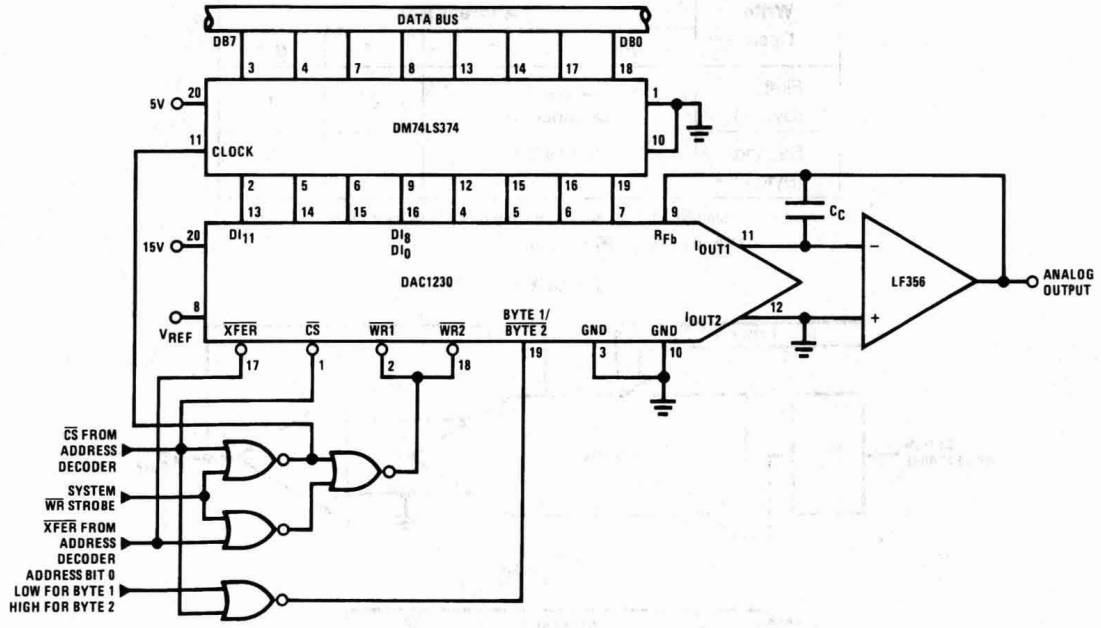

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FIGURE 7. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

Application Hints (Continued)

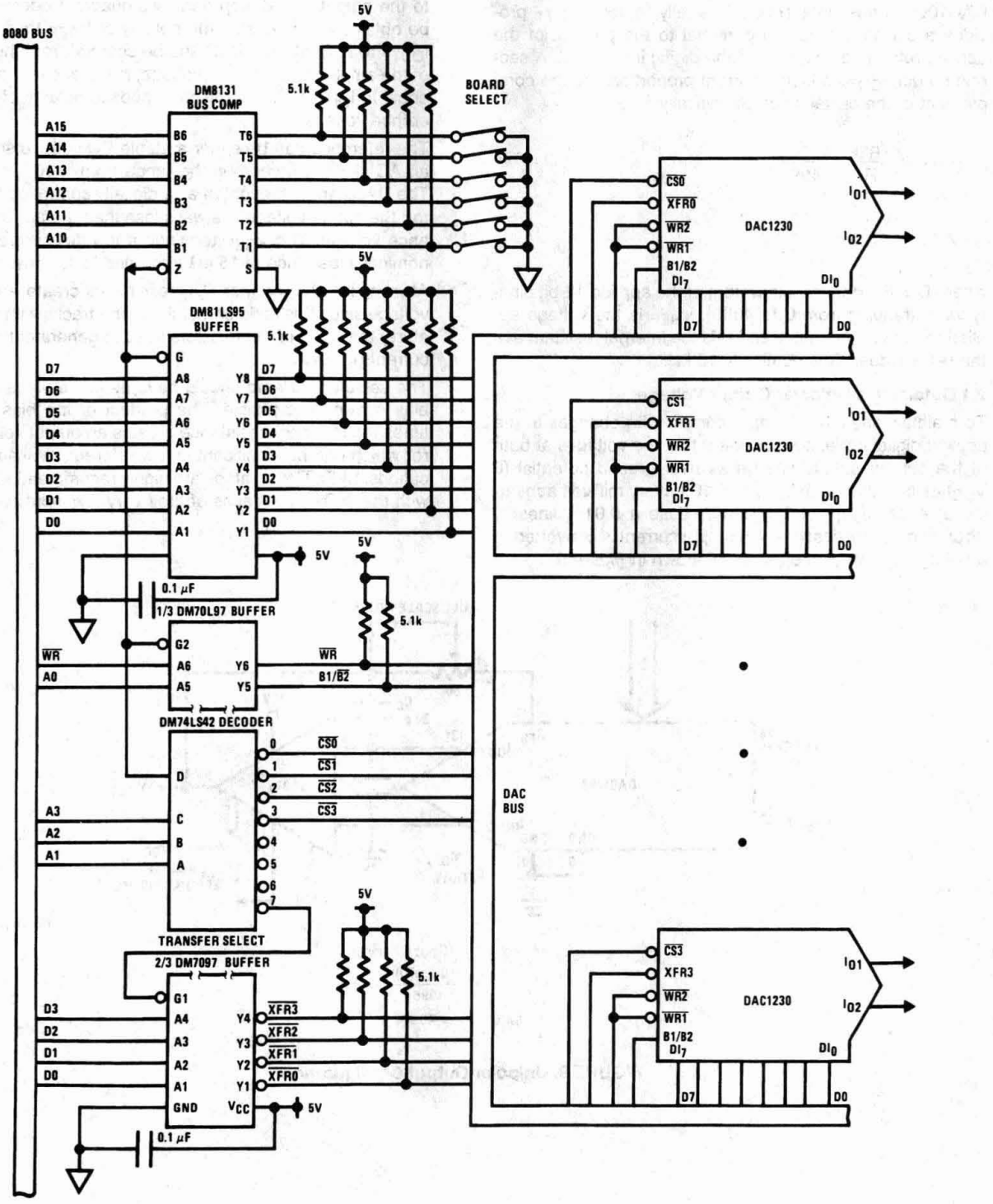

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FIGURE 8. TRI-STATE® Buffers Isolate the Data and Control Lines from the DACs. A Transfer Word Provides a Flexible Update.

Application Hints (Continued)

2.0 ANALOG APPLICATIONS

The analog output signal for these DACs is derived from a conventional R-2R current switching ladder network. A detailed description of this network can be found on the DAC1000 series data sheet. Basically, output I_{OUT1} provides a current directly proportional to the product of the applied reference voltage and the digital input word. A second output, I_{OUT2} will be a current proportional to the complement of the digital input. Specifically:

$$I_{OUT1} = \frac{V_{REF}}{R} \times \frac{D}{4096};$$

$$I_{OUT2} = \frac{V_{REF}}{R} \times \frac{4095 - D}{4096}$$

where D is the decimal equivalent of the applied 12-bit binary word (ranging from 0 to 4095), V_{REF} is the voltage applied to the V_{REF} terminal and R is the internal resistance of the R-2R ladder. R is nominally 15 kΩ.

2.1 Obtaining a Unipolar Output Voltage

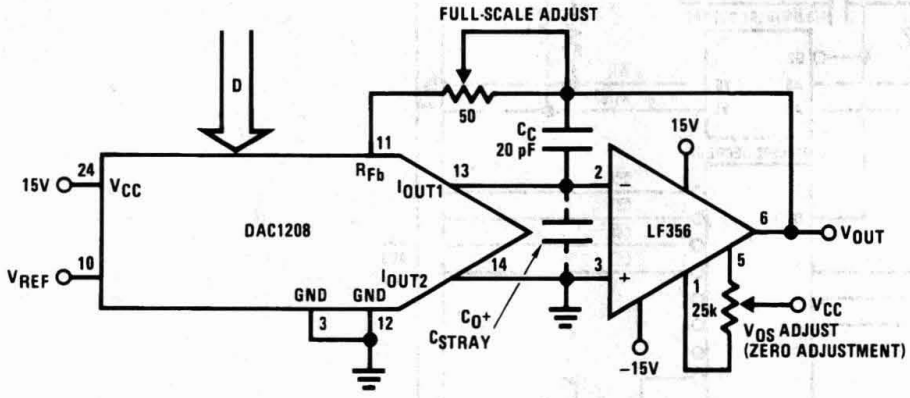
To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential (0 V_{DC}) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 9*.

The inverting input of the op amp is a virtual ground created by the feedback from its output through the internal 15 kΩ resistor, R_{Fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{Fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{Fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{Fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™ op amps are highly recommended for use with these DACs because of their very low input current.



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$$V_{OUT} = -(I_{OUT1} \times R_{Fb})$$

$$= \frac{-V_{REF}(D)}{4096}$$

for $0 \leq D \leq 4095$

FIGURE 9. Unipolar Output Configuration

Application Hints (Continued)

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{Fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 9*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

2.1.1 Zero and Full-Scale Adjustments

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

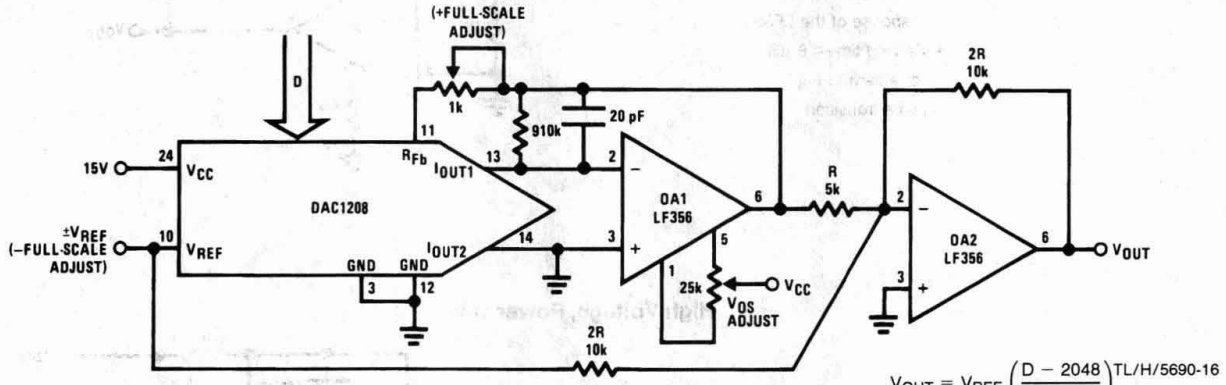
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near 0 V_{DC} as possible. This is accomplished by shorting out R_{Fb}, the amplifier feedback resistor, and adjusting the v_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The short around R_{Fb} is then removed and the converter is zero adjusted.

A unique feature of this series of DACs is that the full-scale or gain error is guaranteed to be negative. The gain error specification is a measure of how close the value of the internal feedback resistor, R_{Fb}, matches the R-2R ladder resistors. A negative gain error indicates that R_{Fb} is a smaller resistance value than it should be. To adjust this gain error, some resistance must always be added in series with R_{Fb}. The 50Ω potentiometer shown is sufficient to adjust the worst-case gain error for these devices.

2.2 Bipolar Output Voltage from a Fixed Reference

The addition of a second op amp to the unipolar circuit can generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication. This circuit is shown in *Figure 10*.

This configuration features several improvements over existing circuits for a bipolar output shown with other multiplying DACs. Only the offset voltage of amplifier 1 affects the linearity of the DAC. The offset voltage error of the second op amp (although a constant output error) has no effect on linearity. In addition, this configuration offers a non-interactive positive and negative full-scale calibration procedure.



$$V_{OUT} = V_{REF}\left(\frac{D - 2048}{2048}\right)$$

for $0 \leq D \leq 4095$

$$1\ LSB = \frac{|V_{REF}|}{2048}$$

Input Code MSB.....LSB	Ideal V_{OUT}	
	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1 1 0 0 0 0 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1 1 1 1 1	−1 LSB	+1 LSB
0 0 1 1 1 1 1 1 1 1 1 1	$-\frac{V_{REF}}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}$	$+\lvert V_{REF}\rvert$

FIGURE 10. Bipolar Output Voltage Configuration

Application Hints (Continued)

2.2.1 Zero and Full-Scale Adjustments

To calibrate the bipolar output circuit, three adjustments are required. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) then null the V_{OS} of amplifier 1 by setting the voltage at its inverting input (pin 2) to zero volts. Next, with a code of all zeros still applied, adjust "−full-scale adjust", the reference voltage, for $V_{OUT} = \pm|V_{REF}$ ideal|. The polarity of the output voltage at this time will be opposite that of the applied reference. Finally, set all of the digital inputs HIGH and adjust "+full-scale adjust" for

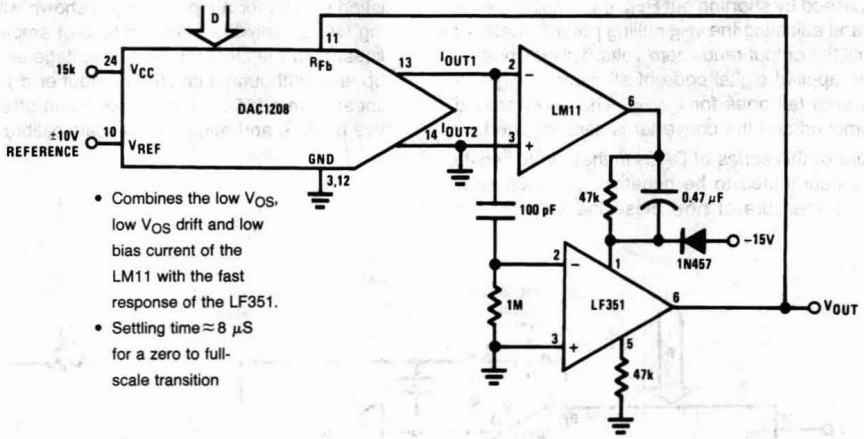
$$V_{OUT} = V_{REF}\frac{2047}{2048}.$$

The polarity of the output will be the same as that of the reference voltage.

3.0 APPLICATION IDEAS

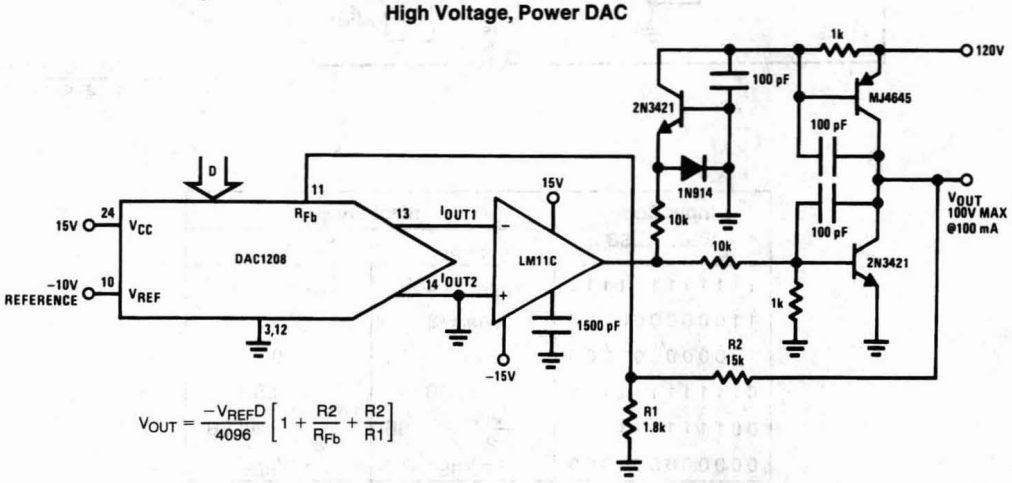
In this section the digital input word is represented by the letter D and is equal to the decimal equivalent of the 12-bit binary input. Hence D can be any integer value between 0 and 4095.

Composite Amplifier for Good DC Characteristics and Fast Output Response



- Combines the low V_{OS}, low V_{OS} drift and low bias current of the LM11 with the fast response of the LF351.
- Settling time ≈ 8 μS for a zero to full-scale transition

High Voltage, Power DAC



$$V_{OUT} = \frac{-V_{REF}D}{4096}\left[1 + \frac{R2}{R_{Fb}} + \frac{R2}{R1}\right]$$

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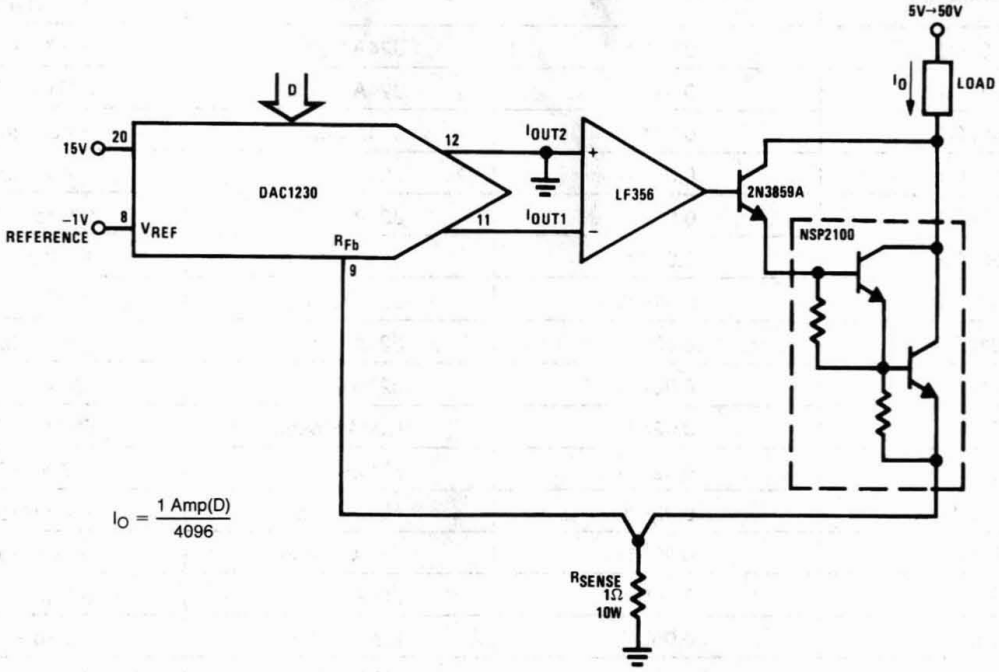
Application Hints (Continued)

High Current Controller



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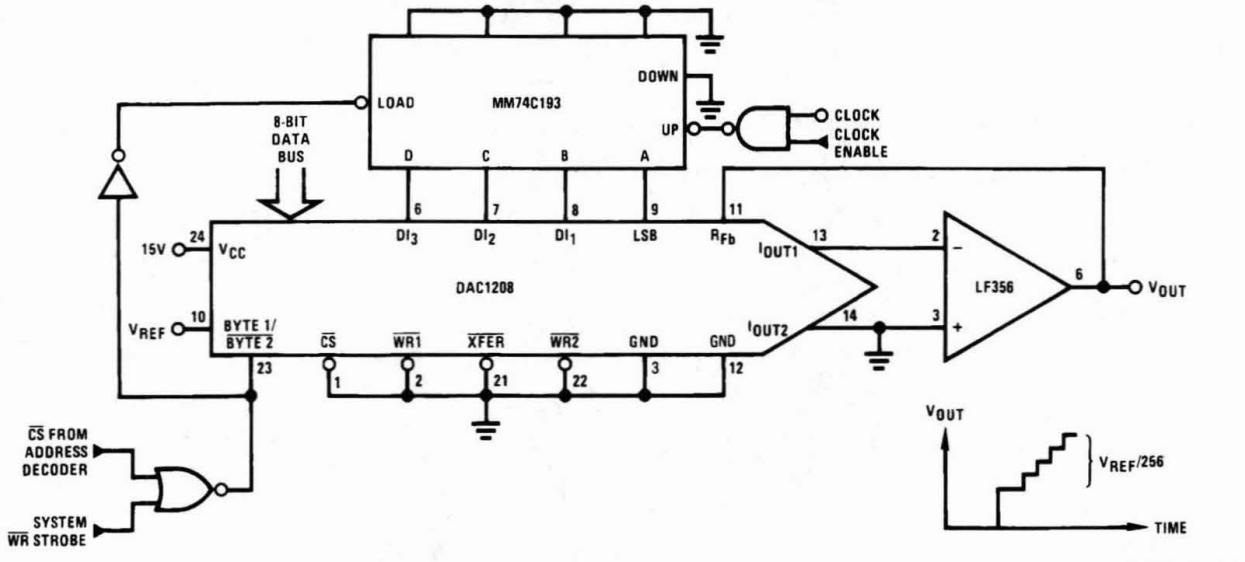
8-Bit Course, 4-Bit Vernier DAC



TL/H/5690–20

Ordering Information

Part Number	Non-Linearity	Package	Temperature Range
DAC1208LCJ	0.018%	J24A Cerdip	−40°C to +85°C
DAC1208LCJ-1	0.018%	J24A Cerdip	0°C to +70°C
DAC1209LCJ	0.024%	J24A Cerdip	−40°C to +85°C
DAC1210LCJ	0.050%	J24A Cerdip	−40°C to +85°C
DAC1210LCJ-1	0.050%	J24A Cerdip	0°C to +70°C
DAC1230LCJ	0.018%	J20A Cerdip	−40°C to +85°C
DAC1230LCJ-1	0.018%	J20A Cerdip	0°C to +70°C
DAC1231LCJ	0.024%	J20A Cerdip	−40°C to +85°C
DAC1231LCJ-1	0.024%	J20A Cerdip	0°C to +70°C
DAC1231LCN	0.024%	N20A Plastic	0°C to +70°C
DAC1231LCWM	0.024%	M20B SO	0°C to +70°C
DAC1231LIN	0.024%	N20A Plastic	−40°C to +85°C
DAC1232LCJ	0.050%	J20A Cerdip	−40°C to +85°C
DAC1232LCJ-1	0.050%	J20A Cerdip	0°C to +70°C
DAC1232LCN	0.050%	N20A Plastic	0°C to +70°C
DAC1232LCWM	0.050%	M20B SO	0°C to +70°C
DAC1232LIN	0.050%	N20A Plastic	−40°C to +85°C

National Semiconductor

DAC1218/DAC1219
12-Bit Binary Multiplying D/A Converter

General Description

The DAC1218 and the DAC1219 are 12-bit binary, 4-quadrant multiplying D to A converters. The linearity, differential non-linearity and monotonicity specifications for these converters are all guaranteed over temperature. In addition, these parameters are specified with standard zero and full-scale adjustment procedures as opposed to the impractical best fit straight line guarantee.

This level of precision is achieved though the use of an advanced silicon-chromium (SiCr) R-2R resistor ladder network. This type of thin-film resistor eliminates the parasitic diode problems associated with diffused resistors and allows the applied reference voltage to range from −25V to 25V, independent of the logic supply voltage.

CMOS current switches and drive circuitry are used to achieve low power consumption (20 mW typical) and minimize output leakage current errors (10 nA maximum). Unique digital input circuitry maintains TTL compatible input threshold voltages over the full operating supply voltage range.

The DAC1218 and DAC1219 are direct replacements for the AD7541 series, AD7521 series, and AD7531 series with a significant improvement in the linearity specification. In applications where direct interface of the D to A converter to a microprocessor bus is desirable, the DAC1208 and DAC1230 series eliminate the need for additional interface logic.

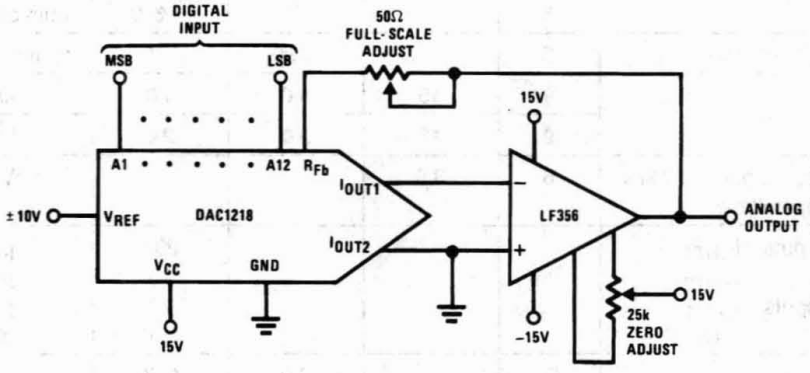
Features

- Linearity specified with zero and full-scale adjust only
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- All parts guaranteed 12-bit monotonic

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	12 Bits (DAC1218) 11 Bits (DAC1219)
■ Gain Tempco	1.5 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



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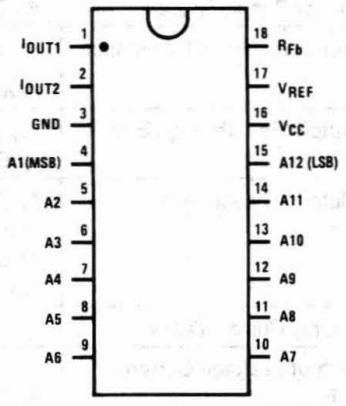
$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

Connection Diagram

Dual-In-Line Package



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Top View

Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	Package Outline
Non Linearity	0.012%	DAC1218LCJ-1	DAC1218LCJ	J18A Cerdip
	0.024%		DAC1219LCJ	J18A Cerdip

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead Temp. (Soldering, 10 seconds)	300°C
ESD Susceptibility (Note 11)	800V

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1218LCJ, DAC1219LCJ	−40°C ≤ T_A ≤ +85°C
DAC1218LCJ-1	0°C ≤ T_A ≤ 70°C
Range of V_{CC}	5 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 9);** all other limits T_A = T_J = 25°C.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted DAC1218 DAC1219	4, 5, 9		 **±0.018** **±0.024**	 **±0.018** **±0.024**	 % of FSR % of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted DAC1218 DAC1219	4, 5, 9		 **±0.018** **±0.024**	 **±0.018** **±0.024**	 % of FSR % of FSR
Monotonicity		4	12	12	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb}, V_{REF} = ±10V, ±1V	5	−0.1	0.0		% of FSR
Gain Error (Max)		5	−0.1	−0.2		% of FSR
Gain Error Tempco		5	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs High	5	±3.0	±30		ppm of FSR/V
Reference Input Resistance	(Min)	9	15	**10**	**10**	kΩ
	(Max)	9	15	**20**	**20**	kΩ
Output Feedthrough Error	V_{REF} = 120 Vp-p, f = 100 kHz All Data Inputs Low	6	3.0			mVp-p
Output Capacitance	All Data Inputs High I_{OUT1} I_{OUT2} All Data Inputs Low I_{OUT1} I_{OUT2}				200 70 70 200	pF pF pF pF
Supply Current Drain		9		2.0	**2.5**	mA
Output Leakage Current I_{OUT1} I_{OUT2}	 All Data Inputs Low All Data Inputs High	7, 9		 **10** **10**	 **10** **10**	 nA nA
Digital Input Threshold	Low Threshold High Threshold	9		**0.8** **2.2**	**0.8** **2.2**	V_{DC} V_{DC}
Digital Input Currents	Digital Inputs <0.8V Digital Inputs >2.2V	9		**−200** **10**	**−200** **10**	μA_{DC} μA_{DC}
t_s Current Settling Time	R_L = 100Ω, Output Settled to 0.01%, All Digital Inputs Switched Simultaneously		1			μs

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1218 is 0.012% of FSR. This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% $\times$ V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR (parts per million of full-scale range) and ppm of FS (parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ± 6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from -40°C to $+85$°C of $\pm(6)(V_{REF}/10^6)(125°C)$ or $\pm 0.75\ (10^{-3})\ V_{REF}$ which is $\pm 0.075\%$ of V_{REF}.

Note 6: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 7: A 10 nA leakage current with $R_{Fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Note 8: Human body model, 100 pF discharged through 1.5 kΩ resistor.

Note 9: Tested limit for -1 suffix parts applies only at 25°C.

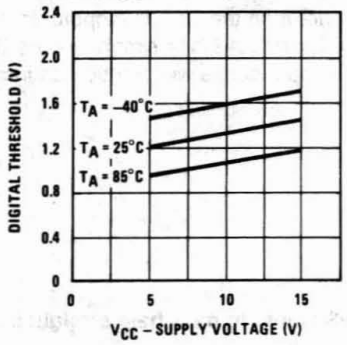
Note 10: Typicals are at 25°C and represent the most likely parametric norm.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

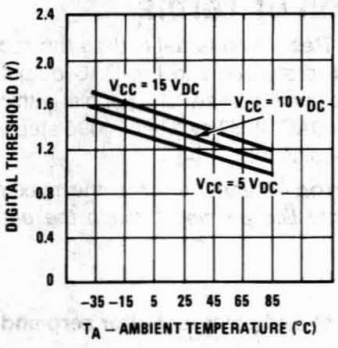
Note 12: Design limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

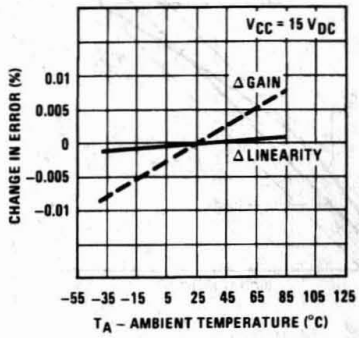
Digital Input Threshold vs V_{CC}



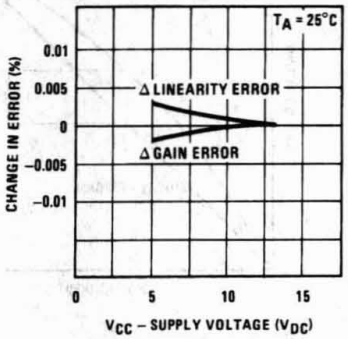
Digital Input Threshold vs Temperature



Gain and Linearity Error Variation vs Temperature



Gain and Linearity Error Variation vs Supply Voltage



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3

Definition of Package Pinouts

(A1–A12): Digital Inputs. A12 is the least significant digital input (LSB) and A1 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital input of all 1s, and is zero for a digital input of all 0s.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage).

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects to an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Ground. This is the ground for the circuit.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1218 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error in the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

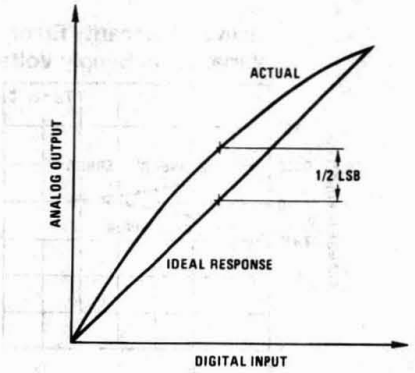
Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± 1/2 LSB of the final output value.

Full-scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1218 full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

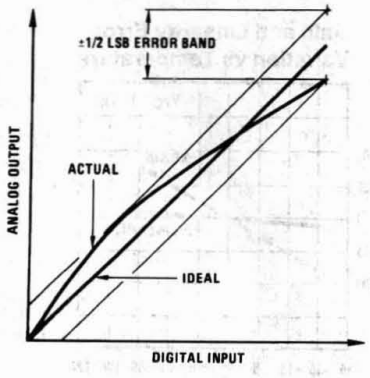
Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.

a) End point test after zero and FS adjust



b) Shifting FS adjust to pass best straight line test



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Application Hints

The DAC1218 and DAC1219 are pin-for-pin compatible with the DAC1220 series but feature 12 and 11-bit linearity specifications. To preserve this degree of accuracy, care must be taken in the selection and adjustments of the output amplifier and reference voltage. Careful PC board layout is important, with emphasis made on compactness of components to prevent inadvertent noise pickup and utilization of single point grounding and supply distribution.

1.0 BASIC CIRCUIT DESCRIPTION

Figure 1 illustrates the R-2R current switching ladder network used in the DAC1218 and DAC1219. As a function of the logic state of each digital input, the binarily weighted current in each leg of the ladder is switched to either I_{OUT1} or I_{OUT2}. The voltage potential at I_{OUT1} and I_{OUT2} must be at zero volts to keep the current in each leg the same, independent of the switch state.

The switches operate with a small voltage drop across them and can therefore conduct currents of either polarity. This permits the reference to be positive or negative, thereby allowing 4-quadrant multiplication by the digital input word. The reference can be a stable DC source or a bipolar AC signal within the range of $\pm 10V$, for specified accuracy, with an absolute maximum range of $\pm 25V$. The reference can also exceed the applied V_{CC} of the DAC.

The maximum output current from either I_{OUT1} or I_{OUT2} is equal to

$$\frac{V_{REF(max)}}{R}\left(\frac{4095}{4096}\right),$$

where R is the reference input resistance (typically 15 kΩ). A high level on any digital input steers current to I_{OUT1} and a low level steers current to I_{OUT2}.

2.0 CREATING A UNIPOLAR OUTPUT VOLTAGE (A DIGITAL ATTENUATOR)

To generate an output voltage and keep the potential at the current output terminals at 0V, an op amp current to voltage converter is used. As shown in *Figure 2*, the current from I_{OUT1} flows through the feedback resistor, forcing a proportional voltage at the amplifier output. The voltage at I_{OUT1} is held at a virtual ground potential. The feedback resistor is provided on the chip and should always be used as it matches and tracks the R value of the R-2R ladder. The output voltage is the opposite polarity of the applied reference voltage.

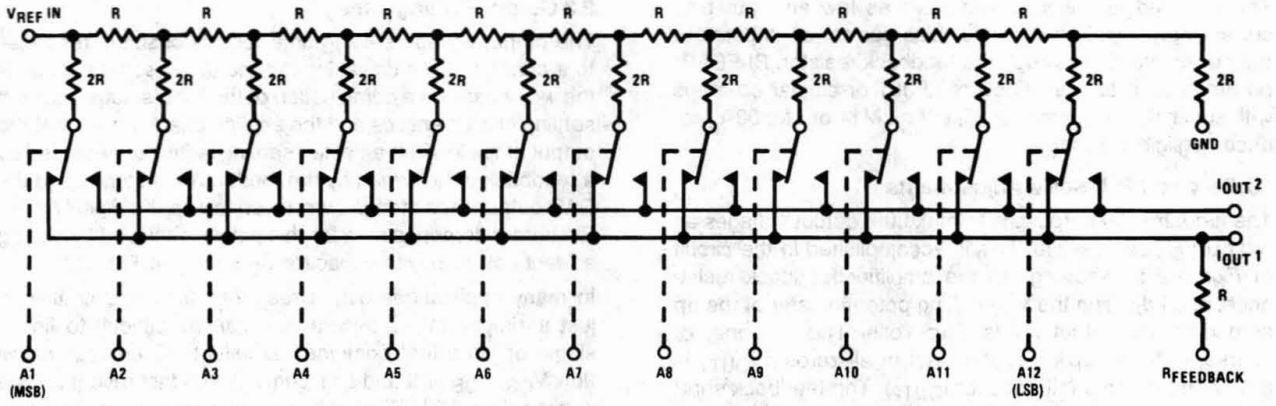
2.1 Amplifier Considerations

To maintain linearity of the output voltage with changing digital input codes the input offset voltage of the amplifier must be nulled. The resistance from I_{OUT1} to ground ($R_{I_{OUT1}}$) varies non-linearly with the applied digital code from a minimum of R with all ones applied to the input to near ∞ with an all zeros code. Any offset voltage between the amplifier inputs appears at the output with a gain of

$$1 + \frac{R_F}{R_{I_{OUT1}}}.$$

Since $R_{I_{OUT1}}$ varies with the input code, any offset will degrade output linearity. (See Note 4 of Electrical Characteristics.)

If the desired amplifier does not have offset balancing pins available (it could be part of a dual or quad package) the nulling circuit of *Figure 3* can be used. The voltage at the non-inverting input will be set to $-V_{OS}$ initially to force the inverting input to 0V. The common technique of summing current into the amplifier summing junction cannot be used as it directly introduces a zero code output current error.



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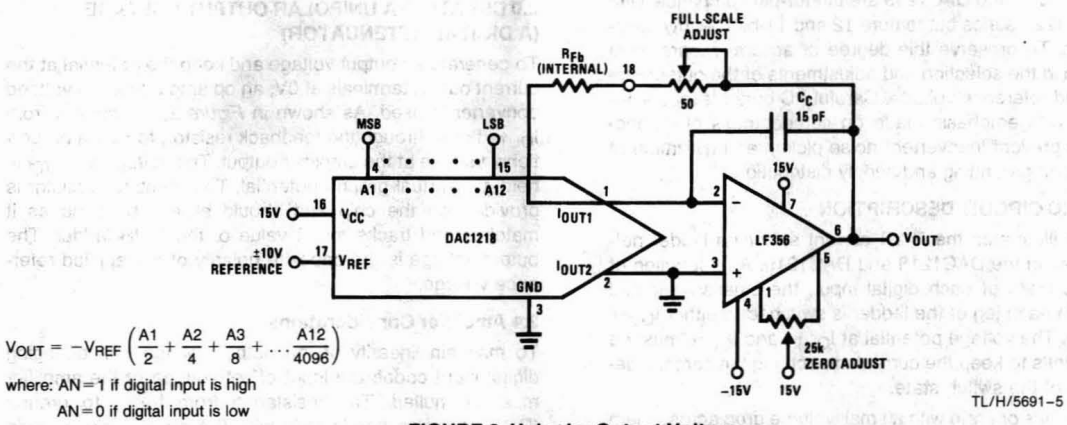
Note: Switches shown in digital high state.

FIGURE 1. The R-2R Current Switching Ladder Network

Application Hints (Continued)



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A12}{4096}\right)$$

where: AN = 1 if digital input is high
AN = 0 if digital input is low

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FIGURE 2. Unipolar Output Voltage

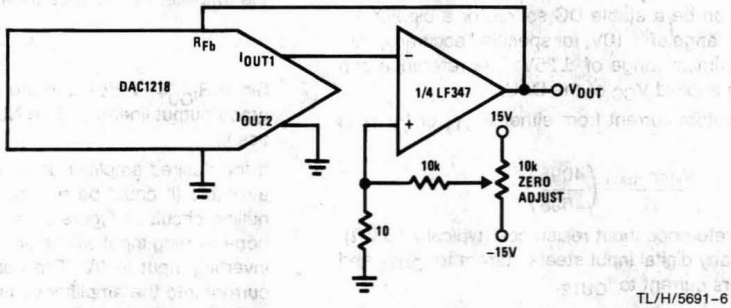

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FIGURE 3. Zeroing an Amplifier Which Does Not Have Balancing Provisions

The selected amplifier should have as low an input bias current as possible since input bias current contributes to the current flowing through the feedback resistor. BI-FET™ op amps such as the LF356 or LF351 or bipolar op amps with super β input transistors like the LM11 or LM308A produce negligible errors.

2.2 Zero and Full-Scale Adjustments

The fundamental purpose is to make the output voltages as near 0 V_{DC} as possible. This is accomplished in the circuit of *Figure 2* by shorting out the amplifier feedback resistance, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital input of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The feedback short is then removed and the converter is zero adjusted.

A unique characteristic of these DACs is that any full-scale or gain error is always negative. This means that for a full-scale input code the output voltage, if not inherently correct, will always be less than what it should be. This ensures that adding an appropriate resistance in series with the internal feedback resistor, R_{Fb}, will always correct for any gain error. The 50Ω potentiometer in *Figure 2* is all that is needed to adjust the worst case DAC gain error.

Conversion accuracy is only as good as the applied reference voltage, so providing a source that is stable over time and temperature is important.

2.3 Output Settling Time

The output voltage settling time for this circuit in response to a change of the digital input code (a full-scale change is the worst case) is a combination of the DAC's output current settling characteristics and the settling characteristics of the output amplifier. The amplifier settling is further degraded by a feedback pole formed by the feedback resistance and the DAC output capacitance (which varies with the digital code). First order compensation for this pole is achieved by adding a feedback zero with capacitor C_C shown in *Figure 2*.

In many applications output response time and settling is just as important as accuracy. It can be difficult to find a single op amp that combines excellent DC characteristics (low V_{OS}, V_{OS} drift and bias current) with fast response and settling time. BI-FET op amps offer a reasonable compromise of high speed and good DC characteristics. The circuit of *Figure 4* illustrates a composite amplifier connection that combines the speed of a BI-FET LF351 with the excellent DC input characteristics of the LM11. If output settling time is not so critical, the LM11 can be used alone.

Figure 5 is a settling time test circuit for the complete voltage output DAC circuit. The circuit allows the settling time of the DAC amplifier to be measured to a resolution of 1 mV out of a zero to ±10V full-scale output change on an oscilloscope. *Figure 6* summarizes the measured settling times for several output amplifiers and feedback compensation capacitors.

Application Hints (Continued)

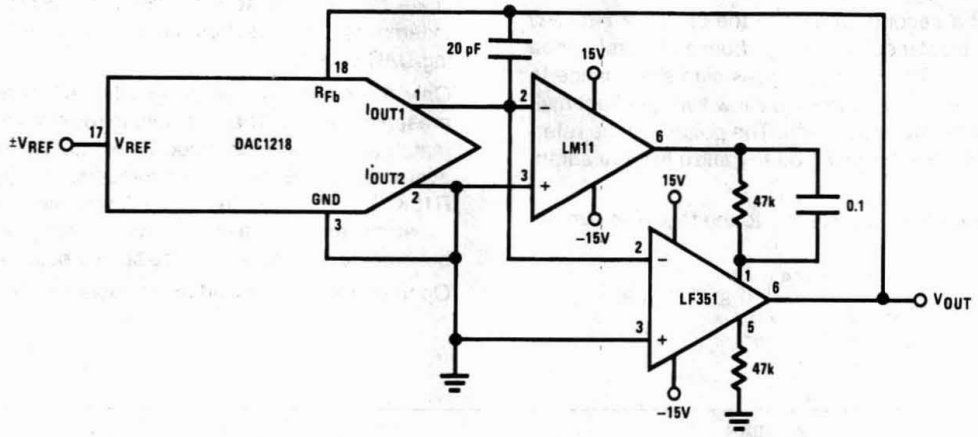

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FIGURE 4. Composite Output Amplifier Connection

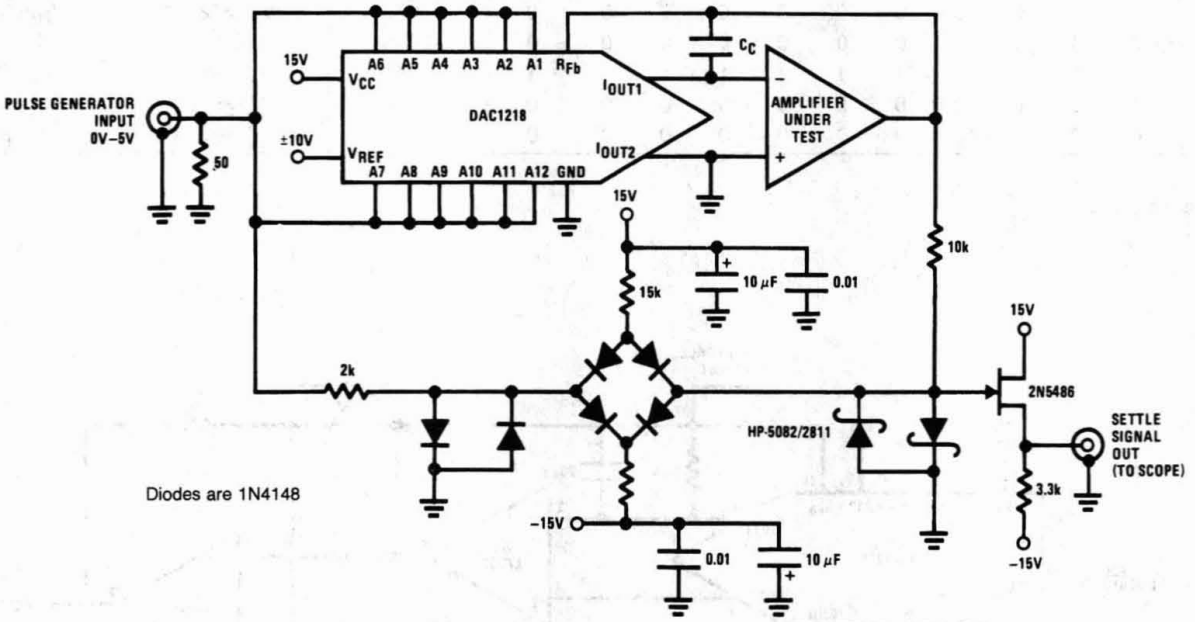

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FIGURE 5. DAC Settling Time Test Circuit

Amplifier	C_C	Settling Time to 0.01%
LM11	20 pF	30 µs
LF351	15 pF	8 µs
LF351	30 pF	5 µs
Composite LM11-LF351	20 pF	8 µs
LF356	15 pF	6 µs

FIGURE 6. Some Measured Settling Times

Application Hints (Continued)

3.0 OBTAINING A BIPOLAR OUTPUT VOLTAGE FROM A FIXED REFERENCE

The addition of a second op amp to the circuit of *Figure 2* can generate a bipolar output voltage from a fixed reference voltage (*Figure 7*). This, in effect gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference voltage can also be reversed to realize full 4-quadrant multiplication.

The output responds in accordance to the following expression:

$$V_O = V_{REF}\left(\frac{D - 2048}{2048}\right), 0 \le D \le 4095$$

where D is the decimal equivalent of the true binary input word. This configuration inherently accepts a code (half-scale or D = 2048) to provide 0V out without requiring an external ½ LSB offset as needed by other bipolar multiplying DAC circuits.

Only the offset voltage of amplifier A1 need be nulled to preserve linearity. The gain setting resistors around A2 must match and track each other. A thin film, 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. Two of the four resistors can be paralleled to form R and the other two can be used separately as the resistors labeled 2R.

Operation is summarized in the table below:

Applied Digital Input MSB											LSB	Decimal Equivalent	V_{OUT} $+V_{REF}$	V_{OUT} $-V_{REF}$
1	1	1	1	1	1	1	1	1	1	1	1	4095	V_{REF} − 1 LSB	$-\|V_{REF}\|$ + 1 LSB
1	1	0	0	0	0	0	0	0	0	0	0	3072	$V_{REF}/2$	$-\|V_{REF}\|/2$
1	0	0	0	0	0	0	0	0	0	0	0	2048	0	0
0	1	1	1	1	1	1	1	1	1	1	1	2047	−1 LSB	+1 LSB
0	1	0	0	0	0	0	0	0	0	0	0	1024	$-V_{REF}/2$	$+\|V_{REF}\|/2$
0	0	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}$	$+\|V_{REF}\|$

Where 1 LSB = $\frac{|V_{REF}|}{2048}$

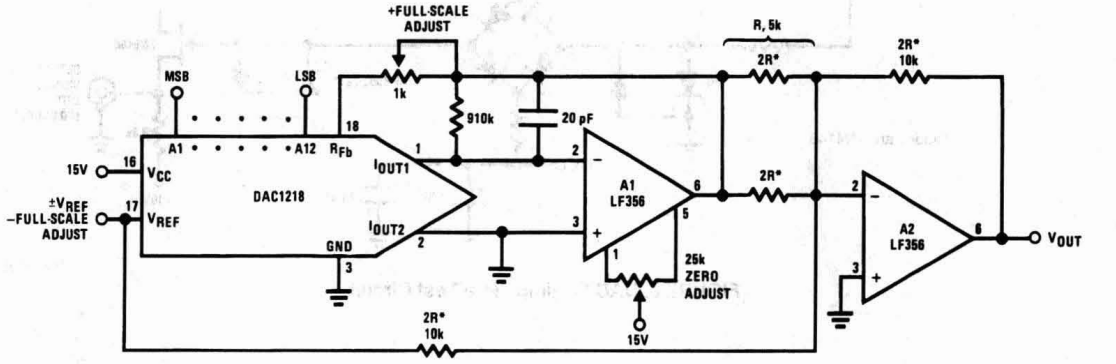

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FIGURE 7. Obtaining a Bipolar Output from a Fixed Reference

Application Hints (Continued)

3.1 Zero and Full-Scale Adjustments

The three adjustments needed for this circuit are shown in *Figure 7*. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) and then trim "zero adjust" for zero volts at the inverting input (pin 2) of OA1. Next, with a code of all zeros still applied, adjust "- full-scale adjust", the reference voltage, for $V_{OUT} = \pm|(\text{ideal } V_{REF})|$. The sign of the output voltage will be opposite that of the applied reference.

Finally, set all of the digital inputs HIGH and adjust "+ full-scale adjust" for $V_{OUT} = V_{REF}$ (511/512). The sign of the output at this time will be the same as that of the reference voltage. This + full-scale adjustment scheme takes into account the effects of the V_{OS} of amplifier A2 (as long as this offset is less than 0.1% of V_{REF}) and any gain errors due to external resistor mismatch.

4.0 MISCELLANEOUS APPLICATION HINTS

The devices are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to electrostatic discharge.

During power-up supply voltage sequencing, the negative supply of the output amplifier may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is clamped to one diode drop below ground.

As a general rule, any unused digital inputs should be tied high or low as required by the application. As a troubleshooting aid, if any digital input is left floating, the DAC will interpret that input as a logical 1 level.

Additional Application Ideas

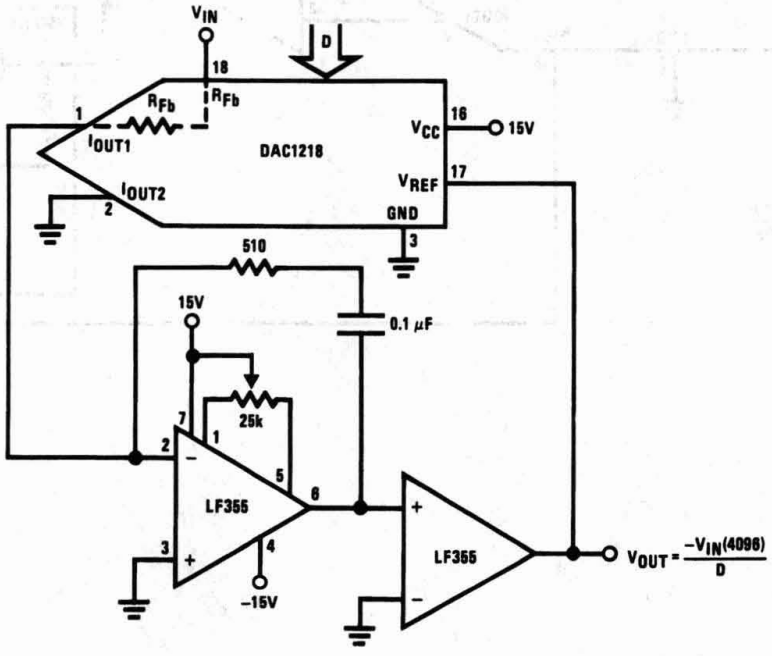
For the circuits shown, D represents the decimal equivalent of the binary digital input code. D ranges from 0 (for an all zeros input code) to 4095 (for an all ones input code) and for any code can be determined from:

$$D = 2048(A1) + 1024(A2) + 512(A2) + \ldots 2(A11) + 1(A12)$$

where AN = 1 if that input is high

AN = 0 if that input is low

DAC Controlled Amplifier



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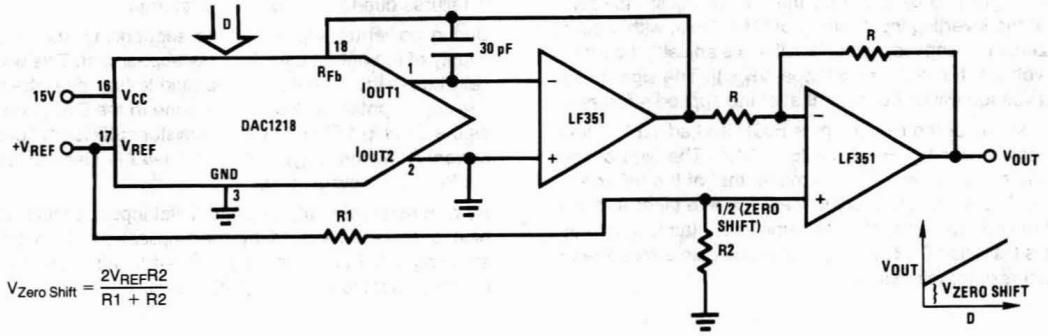
Additional Application Ideas (Continued)

Offsetting the Zero Code Output Voltage



$$V_{Zero\ Shift} = \frac{2V_{REF}R2}{R1 + R2}$$

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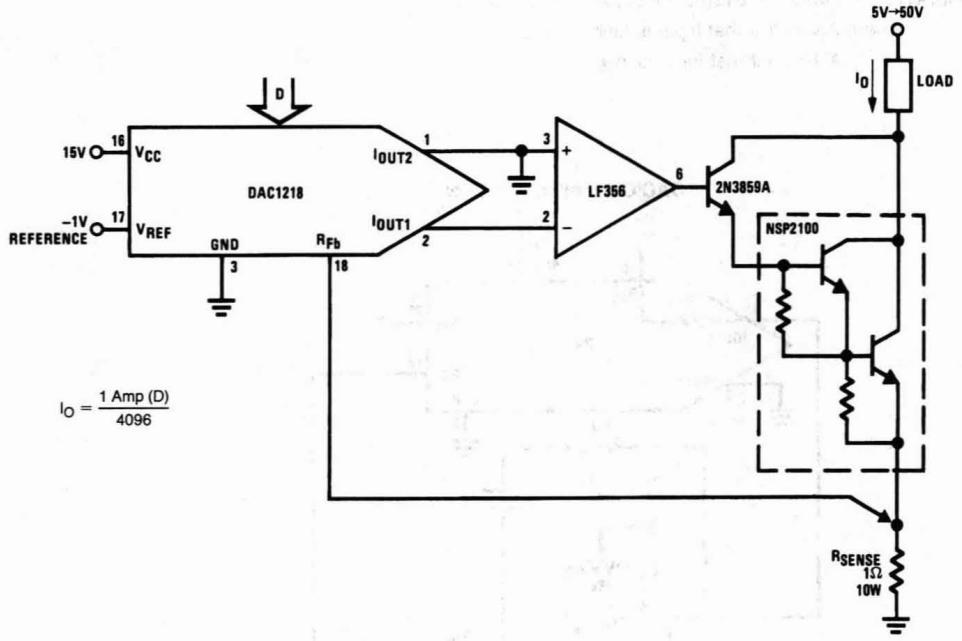
High Current Controller



$$I_O = \frac{1\ Amp\ (D)}{4096}$$

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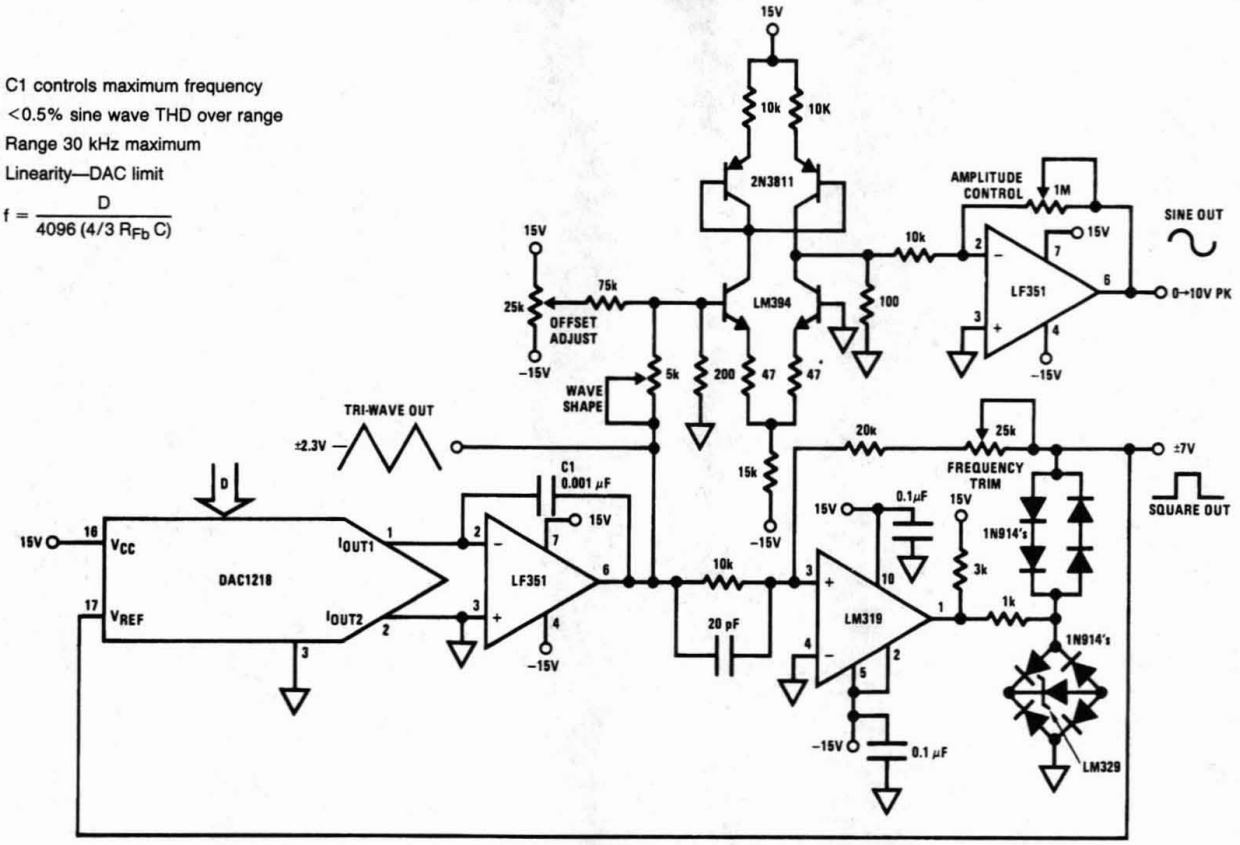
Additional Application Ideas (Continued)

DAC Controlled Function Generator

- C1 controls maximum frequency
- <0.5% sine wave THD over range
- Range 30 kHz maximum
- Linearity—DAC limit
- $f = \frac{D}{4096\,(4/3\,R_{Fb}\,C)}$



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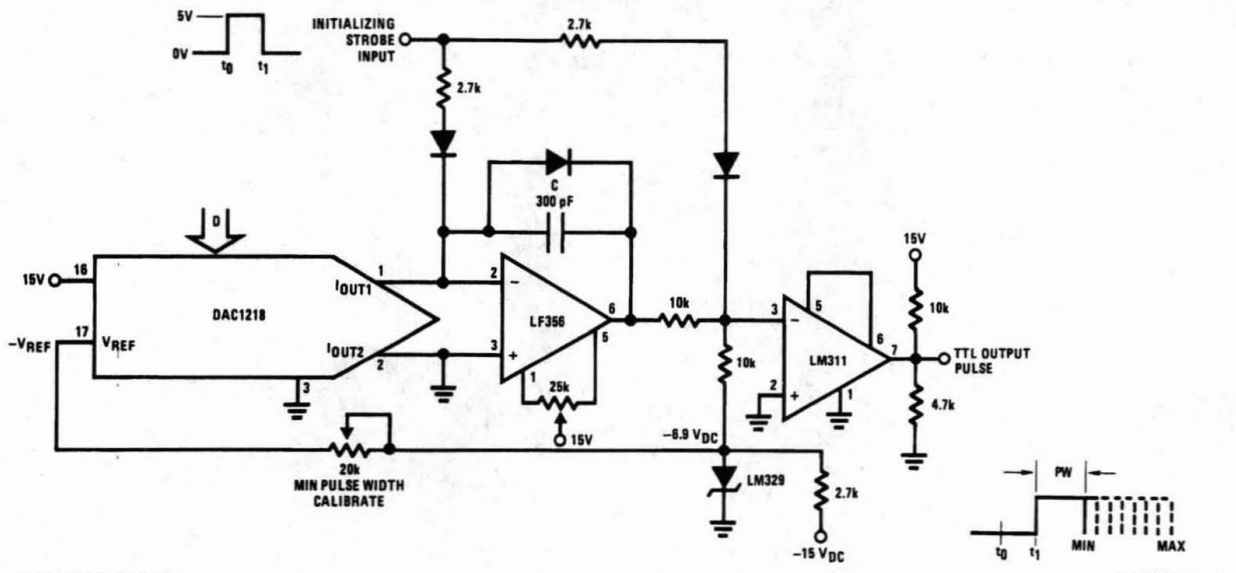
Digitally Programmable Pulse-Width Generator



$$PW \cong \frac{C(7.5V)\,(4096)\,(R_{Fb})}{D|V_{REF}}$$

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Section 4

Voltage References

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LM4431 Micropower Shunt Voltage Reference 4-125
LM9140 Precision Micropower Shunt Voltage Reference 4-131

National Semiconductor

Voltage Reference Selection Guide

Shunt Type

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
1.2**	LM4041A-1.2	I	±0.1%	100	−40°C to +85°C	60 μA to 12 mA	1.5 Max
1.2**	LM4041B-1.2	I	±0.2%	100	−40°C to +85°C	60 μA to 12 mA	1.5 Max
1.2**	LM4041C-1.2	I	±0.5%	100	−40°C to +85°C	60 μA to 12 mA	1.5 Max
1.2**	LM4041D-1.2	I	±1.0%	150	−40°C to +85°C	65 μA to 12 mA	2.0 Max
1.2**	LM4041E-1.2	I	±2.0%	150	−40°C to +85°C	65 μA to 12 mA	2.0 Max
1.22	LM113-2	M	±1%	100 (Typ)	−55°C to +125°C	500 μA to 20 mA	1.0 Max
1.22	LM113-1	M	±2%	100 (Typ)	−55°C to +125°C	500 μA to 20 mA	1.0 Max
1.22	LM113	M	±5%	100 (Typ)	−55°C to +125°C	500 μA to 20 mA	1.0 Max
1.22	LM313	C	±5%	100 (Typ)	0°C to +70°C	500 μA to 20 mA	1.0 Max
1.235	LM185BX-1.2	M	±1%	30	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM185BY-1.2	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM185-1.2	M	±1%	150	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM285AX-1.2	I	±0.32%	30	−40°C to +85°C	10 μA to 20 mA	0.2
1.235	LM285AY-1.2	I	±0.32%	50	−40°C to +85°C	10 μA to 20 mA	0.2
1.235	LM285A-1.2	I	±0.32%	150	−40°C to +85°C	10 μA to 20 mA	0.2
1.235	LM285BX-1.2	I	±1%	30	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM285BY-1.2	I	±1%	50	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM285-1.2	I	±1%	150	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM385AX-1.2	C	±0.32%	30	0°C to +70°C	10 μA to 20 mA	0.2
1.235	LM385AY-1.2	C	±0.32%	50	0°C to +70°C	10 μA to 20 mA	0.2
1.235	LM385A-1.2	C	±0.32%	150	0°C to +70°C	10 μA to 20 mA	0.2
1.235	LM385BX-1.2	C	±1%	30	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385BY-1.2	C	±1%	50	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385B-1.2	C	±1%	150	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385-1.2	C	+2%, −2.4%	150	0°C to +70°C	15 μA to 20 mA	1
1.24 to 5.3 (Adj.)	LM185B	M	±1%	150	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM185BX	M	±1%	30	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM185BY	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285BX	I	±1%	30	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285BY	I	±1%	50	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285	I	±2%	150	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385BX	C	±1%	30	0°C to +70°C	13 μA to 20 mA	0.4
1.24 to 5.3 (Adj.)	LM385BY	C	±1%	50	0°C to +70°C	13 μA to 20 mA	0.4
1.24 to 5.3 (Adj.)	LM385	C	±2%	150	0°C to +70°C	13 μA to 20 mA	0.4
1.225V to 10V (Adj)	LM4041D-ADJ	I	±0.5%	150	−40°C to +85°C	60 μA to 12 mA	2.0
1.225V to 10V (Adj)	LM4041C-ADJ	I	±1.0%	100	−40°C to +85°C	65 μA to 12 mA	2.0
1.24 to 6.3 (Adj.)	LM611AM	M	±0.6%	80	−55°C to +125°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	†LM611M	M	±0.6%	150	−55°C to +125°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM611AI	I	±0.6%	80	−40°C to +85°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM611I	I	±2.0%	150	−40°C to +85°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM611C	C	±2.0%	150	0°C to +70°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	††LM613AM	M	±0.6%	80	−55°C to +125°C	16 μA to 10 mA	0.2

Shunt Type (Continued)

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
1.24 to 6.3 (Adj.)	††LM613M	M	±2.0%	150	−55°C to +125°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM613AI	I	±0.6%	80	−40°C to +85°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM613I	I	±2.0%	150	−40°C to +85°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM613C	C	±2.0%	150	0°C to +70°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM614AM	M	±0.6%	80	−55°C to +125°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	‡LM614M	M	±2.0%	150	−55°C to +125°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM614AI	I	±0.6%	80	−40°C to +85°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM614I	I	±2.0%	150	−40°C to +85°C	16 μA to 10 mA	0.2
1.24 to 6.3 (Adj.)	LM614C	C	±2.0%	150	0°C to +70°C	16 μA to 10 mA	0.2
2.49	LM136A	M	±1%	72	−55°C to +125°C	400 μA to 10 mA	0.4
2.49	LM136	M	±2%	72	−55°C to +125°C	400 μA to 10 mA	0.4
2.49	LM236A	I	±1%	72	−25°C to +85°C	400 μA to 10 mA	0.4
2.49	LM236	I	±2%	72	−25°C to +85°C	400 μA to 10 mA	0.4
2.49	LM336	I	±4%	54	0°C to +70°C	400 μA to 10 mA	0.4
2.49	LM336B	C	±2%	54	0°C to +70°C	400 μA to 10 mA	0.4
2.5**	LM4040A-2.5	I	±0.1%	100	−40°C to +85°C	65 μA to 15 mA	0.8 Max
2.5**	LM4040B-2.5	I	±0.2%	100	−40°C to +85°C	65 μA to 15 mA	0.8 Max
2.5**	LM4040C-2.5	I	±0.5%	100	−40°C to +85°C	65 μA to 15 mA	0.8 Max
2.5**	LM4040D-2.5	I	±1.0%	150	−40°C to +85°C	70 μA to 15 mA	0.9 Max
2.5**	LM4040E-2.5	I	±2.0%	150	−40°C to +85°C	70 μA to 15 mA	1.1 Max
2.5**	LM4431-2.5	C	±2.0%	30 Typ.	0°C to +70°C	100 μA to 15 mA	1.0
2.5	LM9140BY-2.5	I	±0.5%	25	−40°C to +85°C	60 μA to 15 mA	0.8 Max
2.5	LM185BX-2.5	M	±1.5%	30	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM185BY-2.5	M	±1.5%	50	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM185B-2.5	M	±1.5%	150	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM285AX-2.5	I	±0.8%	30	−40°C to +85°C	20 μA to 20 mA	0.2
2.5	LM285AY-2.5	I	±0.8%	50	−40°C to +85°C	20 μA to 20 mA	0.2
2.5	LM285A-2.5	I	±0.8%	150	−40°C to +85°C	20 μA to 20 mA	0.2
2.5	LM285BX-2.5	I	±1.5%	30	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM285BY-2.5	I	±1.5%	50	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM285-2.5	I	±1.5%	150	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM385AX-2.5	C	±0.8%	30	−40°C to +85°C	20 μA to 20 mA	0.2
2.5	LM385AY-2.5	C	±0.8%	50	−40°C to +85°C	20 μA to 20 mA	0.2
2.5	LM385A-2.5	C	±0.8%	150	−40°C to +85°C	20 μA to 20 mA	0.2
2.5	LM385BX-2.5	C	±1.5%	30	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385BY-2.5	C	±1.5%	50	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385B-2.5	C	±1.5%	150	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385-2.5	C	±3%	150	0°C to +70°C	20 μA to 20 mA	1
4.1**	LM4040A-4.1	I	±0.1%	100	−40°C to +85°C	68 μA to 15 mA	1.0 Max
4.1**	LM4040B-4.1	I	±0.2%	100	−40°C to +85°C	68 μA to 15 mA	1.0 Max
4.1**	LM4040C-4.1	I	±0.5%	100	−40°C to +85°C	68 μA to 15 mA	1.0 Max
4.1**	LM4040D-4.1	I	±1.0%	150	−40°C to +85°C	73 μA to 15 mA	1.3 Max
4.1	LM9140BY-4.1	I	±0.5%	25	−40°C to +85°C	68 μA to 15 mA	1.0 Max
5.0	LM136A	M	±1%	72	−55°C to +125°C	400 μA to 10 mA	1.0 Max
5.0	LM136	M	±2%	72	−55°C to +125°C	400 μA to 10 mA	1.0 Max
5.0	LM236A	I	±1%	72	−25°C to +85°C	400 μA to 10 mA	1.0 Max
5.0	LM236	I	±2%	72	−25°C to +85°C	400 μA to 10 mA	1.0 Max
5.0	LM336B	C	±2%	54	0°C to +70°C	400 μA to 10 mA	1.4 Max
5.0	LM336	C	±4%	54	0°C to +70°C	400 μA to 10 mA	1.4 Max
5.0**	LM4040A-5.0	I	±0.1%	100	−40°C to +85°C	74 μA to 15 mA	1.1 Max
5.0**	LM4040B-5.0	I	±0.2%	100	−40°C to +85°C	74 μA to 15 mA	1.1 Max
5.0**	LM4040C-5.0	I	±0.5%	100	−40°C to +85°C	74 μA to 15 mA	1.1 Max

Shunt Type (Continued)

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift ppm/°C (Max)	Temperature Drift Over Range	Operating Current Range, I_R	Output Dynamic Impedance (Typ)
5.0**	LM4040D-5.0	I	±1.0%	150	−40°C to +85°C	79 μA to 15 mA	1.5 Max
5.0	LM9140BY-5.0	I	±0.5%	25	−40°C to +85°C	74 μA to 15 mA	1.1 Max
6.9	LM129A	M	+3%, −2%	10	−55°C to +125°C	600 μA to 15 mA	0.6
6.9	LM129B	M	+3%, −2%	20	−55°C to +125°C	600 μA to 15 mA	0.6
6.9	LM129C	M	+3%, −2%	50	−55°C to +125°C	600 μA to 15 mA	0.6
6.9	LM329A	C	±5%	50	0°C to +70°C	600 μA to 15 mA	0.8
6.9	LM329B	C	±5%	50	0°C to +70°C	600 μA to 15 mA	0.8
6.9	LM329C	C	±5%	20	0°C to +70°C	600 μA to 15 mA	0.8
6.9	LM329D	C	±5%	100	0°C to +70°C	600 μA to 15 mA	0.8
6.95	LM199A	M	±2%	0.5	−55°C to +125°C	500 μA to 10 mA	0.5
6.95	LM199A-20	M	Same as LM199A with 20 ppm guaranteed long term drift.				
6.95	LM199	M	±2%	1.0	−55°C to +125°C	500 μA to 10 mA	0.5
6.95	LM299A	I	±2%	0.5	−25°C to +85°C	500 μA to 10 mA	0.5
6.95	LM299A-20	I	Same as LM299A with 20 ppm guaranteed long term drift.				
6.95	LM299	I	±2%	1	−25°C to +85°C	500 μA to 10 mA	0.5
6.95	LM399A	C	±5%	1	0°C to +70°C	500 μA to 10 mA	0.5
6.95	LM399A-50	C	Same as LM399A with 50 ppm guaranteed long term drift.				
6.95	LM399	C	±5%	2	0°C to +70°C	500 μA to 10 mA	0.5
6.95	LM3999	C	±5%	5	0°C to +70°C	600 μA to 10 mA	0.6
8.2**	LM4040A-8.2	I	±0.1%	100	−40°C to +85°C	91 μA to 15 mA	1.5 Max
8.2**	LM4040B-8.2	I	±0.2%	100	−40°C to +85°C	91 μA to 15 mA	1.5 Max
8.2**	LM4040C-8.2	I	±0.5%	100	−40°C to +85°C	91 μA to 15 mA	1.5 Max
8.2**	LM4040D-8.2	I	±1.0%	150	−40°C to +85°C	96 μA to 15 mA	1.9 Max
10.0**	LM4040A-10.0	I	±0.1%	100	−40°C to +85°C	100 μA to 15 mA	1.7 Max
10.0**	LM4040B-10.0	I	±0.2%	100	−40°C to +85°C	100 μA to 15 mA	1.7 Max
10.0**	LM4040C-10.0	I	±0.5%	100	−40°C to +85°C	100 μA to 15 mA	1.7 Max
10.0**	LM4040D-10.0	I	±1.0%	150	−40°C to +85°C	110 μA to 15 mA	2.3 Max
10.0	LM9140BY-10.0	I	±0.5%	25	−40°C to +85°C	100 μA to 15 mA	1.7 Max

*C (Commercial) = 0°C to 70°C, I (Industrial) = −25°C to +85°C for the LM236 and LM299, I = −40°C to +85°C for all others.
M (Military) = −55°C to +125°C

**Available in SOT-23 Package.

†LM611 has on-board Op Amp.

††LM613 has on-board Dual Op Amp and Dual Comparator.

‡LM614 has on-board Quad Op Amp.

Current References

Output Current Range	Device	Operating Temperature Range	Set Current Error 2 μA to 10 μA	Set Current Error 10 μA to 1 mA	Set Current Error 1 mA to 5 mA	Operating Voltage Range	Set Current Temperature Dependence*
2 μA to 10 mA	LM134	−55°C to +125°C	±8%	±3%	±5%	1V to 40V	0.96T to 0.104T
2 μA to 10 mA	LM134-3	−55°C to +125°C	N/A	±1%	N/A	1V to 40V	0.98T to 0.102T
2 μA to 10 mA	LM134-6	−55°C to +125°C	N/A	±2%	N/A	1V to 40V	0.97T to 0.103T
2 μA to 10 mA	LM234	−25°C to +100°C	±8%	±3%	±5	1V to 40V	0.96T to 0.104T
2 μA to 10 mA	LM234-3	−25°C to +100°C	N/A	±1%	N/A	1V to 40V	0.98T to 0.102T
2 μA to 10 mA	LM234-6	−25°C to +100°C	N/A	±2%	N/A	1V to 40V	0.97T to 0.103T
2 μA to 10 mA	LM334	0°C to +70°C	±12%	±6%	±8%	1V to 40V	0.96T to 0.104T

*Set current changes linearly with temperature at a rate of 0.33%/°C.

Series Type (Buffered Output)

Output Voltage	Device	Oper. Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Load Reg. ppm/mA	Operating Current Range	Quiescent Current (mA)
				ppm/°C (Max)	Over Range			
0.2 (Adj)	†LM10	M	±2.5%	20 typ	−55°C to +125°C	100	0 mA to +1 mA	0.27
0.2 (Adj)	†LM10B	I	±2.5%	20 typ	−25°C to +85°C	100	0 mA to +1 mA	0.27
0.2 (Adj)	†LM10C	C	±5.0%	30 typ	0°C to +70°C	100	0 mA to +1 mA	0.30
2.5	LM368Y-2.5	C	±0.2%	20	0°C to +70°C	25	0 mA to +10 mA	0.55
2.5	LM368-2.5	C	±0.2%	30	0°C to +70°C	25	0 mA to +10 mA	0.55
5.0	LM368BY-5.0	C	±0.1%	20	0°C to +70°C	10	−10 mA to +10 mA	0.35
5.0	LM368-5.0	C	±0.1%	30	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM169B	M	±0.05%	3	−55°C to +125°C	8	−10 mA to +10 mA	1.8
10	LM169	M	±0.05%	5	−55°C to +125°C	8	−10 mA to +10 mA	1.8
10	LH0070-2	M	±0.05%	8	−25°C to +25°C	60	0 to 5 mA	5
10	LH0070-0	M	±0.1%	40	−25°C to +25°C	60	0 mA to 5 mA	5
10	LH0070-1	M	±0.1%	20	−25°C to +25°C	60	0 mA to 5 mA	5
10	LM369B	C	±0.05%	3	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM369	C	±0.05%	5	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM369C	C	±0.05%	10	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM368Y-10	C	±0.1%	20	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM368-10	C	±0.1%	30	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM369D	C	±0.1%	30	0°C to +70°C	8	−10 mA to +10 mA	2
10.24	LH0071-2	M	±0.05%	8	−40°C to +85°C	60	0 mA to 5 mA	5
10.24	LH0071-1	M	±0.1%	20	−40°C to +85°C	60	0 mA to 5 mA	5
10.24	LH0071-0	M	±0.1%	40	−25°C to +25°C	60	0 mA to 5 mA	5

*C (Commercial) = 0°C to 70°C, I (Industrial) = −40°C to +85°C, M (Military) = −55°C to +125°C

†Reference has on-board Op Amp.

Low Current Reference Diodes

Output Voltage	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
3.0	LM103-3.0	M	±10%	−1700	−55°C to +125°C	10 μA to 10 mA	25
3.3	LM103-3.3	M	±10%	−1500	−55°C to +125°C	10 μA to 10 mA	25
3.6	LM103-3.6	M	±10%	−1400	−55°C to +125°C	10 μA to 10 mA	25
3.9	LM103-3.9	M	±10%	−1300	−55°C to +125°C	10 μA to 10 mA	25

*M (Military) = −55°C to +125°C

"Reference Grade" Voltage Regulators

Output Voltage	Device	Operating Temperature Range	Voltage Tolerance Max, T_A = 25°C	Output Variation Over Operating Range	Load Reg. ppm/mA	Line Reg. ppm/V	Output Current (Max)	Quiescent Current
Adjustable:	LP2951	−55°C to +150°C	±0.5%	±0.5%	100	42	100 mA	120 μA
1.235V to 30V	LP2951AC	−40°C to +125°C	±0.5%	±0.5%	100	42	100 mA	120 μA
	LP2951C	−40°C to +125°C	±1%	±1%	200	83	100 mA	120 μA
5V, 3.3V, 3.0V	LP2950AC	−40°C to +125°C	±0.5%	±0.5%	100	42	100 mA	120 μA
5V, 3.3V, 3.0V	LP2950C	−40°C to +125°C	±1%	±1%	200	83	100 mA	120 μA
5V, 3.3V, 3.0V	LP2980A	−25°C to +125°C	±0.5%	2.5%	*	140	50 mA	95 μA
5V, 3.3V, 3.0V	LP2980	−25°C to +125°C	±1%	3.5%	*	140	50 mA	95 μA

* Included in Output Variation Over Operating Range specification.

National Semiconductor

LH0070 Series Precision BCD Buffered Reference
LH0071 Series Precision Binary Buffered Reference

General Description

The LH0070 and LH0071 are precision, three terminal, voltage references consisting of a temperature compensated zener diode driven by a current regulator and a buffer amplifier. The devices provide an accurate reference that is virtually independent of input voltage, load current, temperature and time. The LH0070 has a 10.000V nominal output to provide equal step sizes in BCD applications. The LH0071 has a 10.240V nominal output to provide equal step sizes in binary applications.

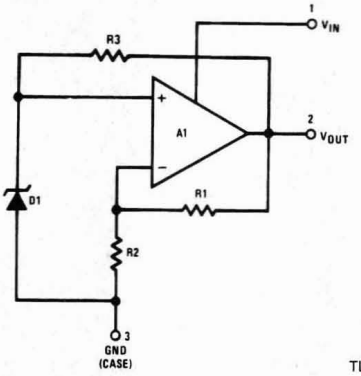
The output voltage is established by trimming ultra-stable, low temperature drift, thin film resistors under actual operating circuit conditions. The devices are shortcircuit proof in both the current sourcing and sinking directions.

The LH0070 and LH0071 series combine excellent long term stability, ease of application, and low cost, making them ideal choices as reference voltages in precision D to A and A to D systems.

Features

- Accuracy output voltage
  - LH0070 10V ± 0.02%
  - LH0071 10.24V ± 0.02%
- Single supply operation 11.4V to 40V
- Low output impedance 0.2Ω
- Excellent line regulation 0.1 mV/V
- Low zener noise 20 μVp-p
- 3-lead TO-5 (pin compatible with the LM109)
- Short circuit proof
- Low standby current 3 mA

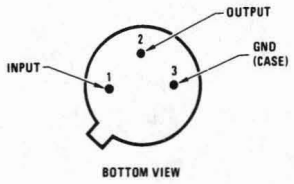
Equivalent Schematic



TL/H/5550–1

Connection Diagram

TO-5 Metal Can Package

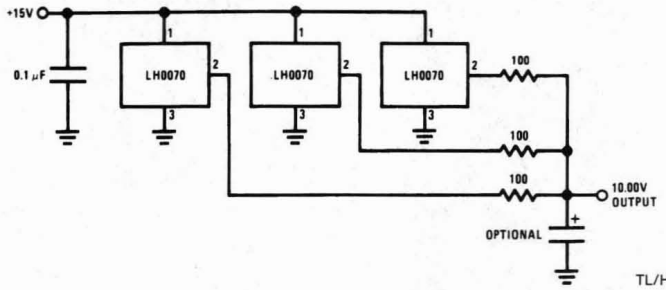


TL/H/5550–7

Order Number LH0070-0H, LH0071-0H, LH0070-1H, LH0071-1H, LH0070-2H or LH0071-2H
See NS Package Number H03B

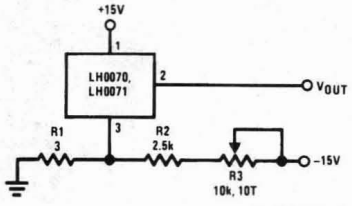
Typical Applications

Statistical Voltage Standard



TL/H/5550–8

***Output Voltage Fine Adjustment**



TL/H/5550–9

***Note:** The output of the LH0070 and LH0071 may be adjusted to a precise voltage by using the above circuit since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to 0.01%/V change in V_{OUT} for changes in V_{IN} and V^-.

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature of the LH0070 and LH0071. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Supply Voltage	40V
Power Dissipation (See Curve)	600 mW
Short Circuit Duration	Continuous
Output Current	± 20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to ±150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	$T_A = 25°C$				
LH0070			10.000		V
LH0071			10.24		V
Output Accuracy	$T_A = 25°C$				
−0, −1			±0.03	±0.1	%
−2			±0.02	±0.05	%
Output Accuracy	$T_A = -55°C, 125°C$				
−0, −1				±0.3	%
−2				±0.2	%
Output Voltage Change With Temperature	(Note 2)				
−0				±0.2	%
−1			±0.02	±0.1	%
−2			±0.01	±0.04	%
Line Regulation	$13V \le V_{IN} \le 33V$, $T_C = 25°C$				
−0, −1			0.02	0.1	%
−2			0.01	0.03	%
Input Voltage Range	$R_L = 50\ k\Omega$	11.4		40	V
Load Regulation	$0\ mA \le I_{OUT} \le 5\ mA$		0.01	0.03	%
Quiescent Current	$13V \le V_{IN} \le 33V$, $I_{OUT} = 0\ mA$	1	3	5	mA
Change In Quiescent Current	$\Delta V_{IN} = 20V$ From 23V To 33V		0.75	1.5	mA
Output Noise Voltage	BW = 0.1 Hz To 10 Hz, $T_A = 25°C$		20		μVp-p
Ripple Rejection	f = 120 Hz		0.01		%/Vp-p
Output Resistance			0.2	0.6	Ω
Long Term Stability	$T_A = 25°C$ (Note 3)				
−0, −1				±0.2	%/yr.
−2				±0.05	%/yr.
Thermal Resistance	$T_j = 150°C$				
θ_{ja} (Junction to Ambient)			200		°C/W
θ_{jc} (Junction to Case)			100		°C/W

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} = 15.0V$, $R_L = 10\ k\Omega$, and over the temperature range of $-55°C \le T_A \le +125°C$.

Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

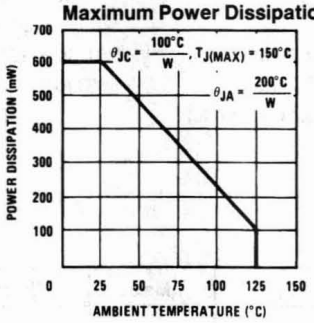
Note 3: This parameter is guaranteed by design and not tested.

Note 4: Refer to the following RETS drawings for military specifications:

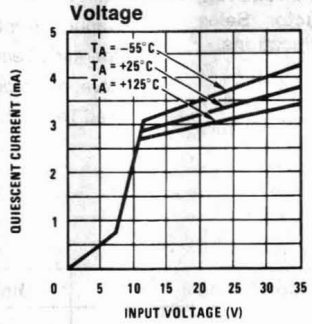
RETS0070-0H for LH0070-0H	RETS0071-0H for LH0071-0H
RETS0070-1H for LH0070-1H	RETS0071-1H for LH0071-1H
RETS0070-2H for LH0070-2H	RETS0071-2H for LH0071-2H

Typical Performance Characteristics

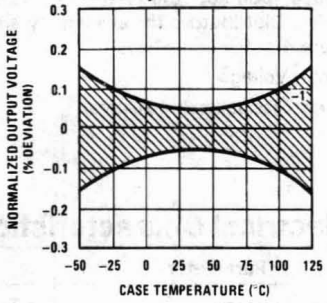
Maximum Power Dissipation



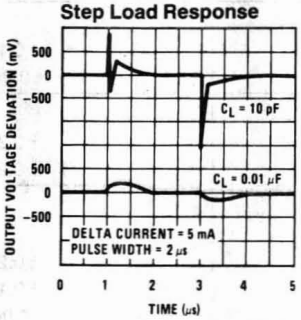
Quiescent Current vs Input Voltage



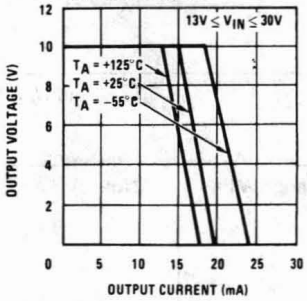
Normalized Output Voltage vs Temperature



Step Load Response

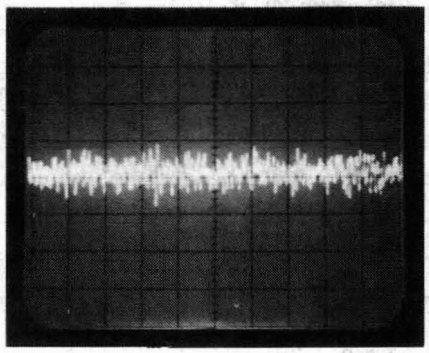


Output Short Circuit Characteristics



TL/H/5550–2

Noise Voltage

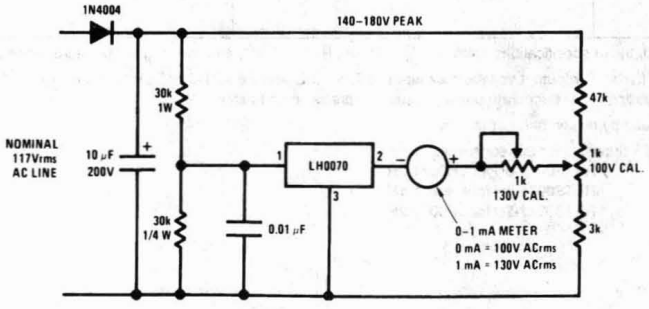


BW = 0.1 Hz TO 10 Hz

TL/H/5550–6

Typical Applications (Continued)

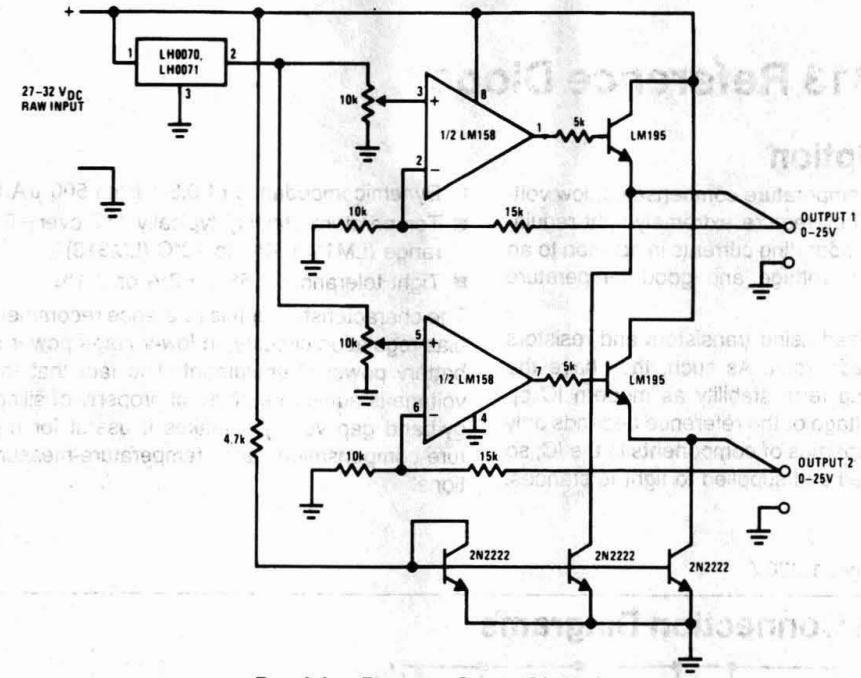
Expanded Scale AC Voltmeter



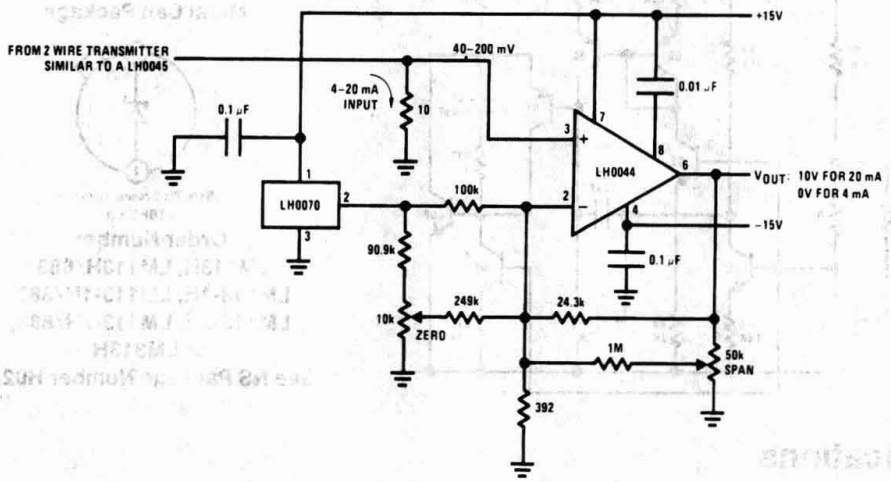
TL/H/5550–4

Typical Applications (Continued)

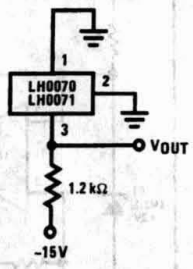
Dual Output Bench Power Supply



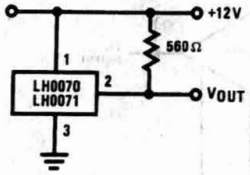
Precision Process Control Interface



Negative 10V Reference



Boosted Reference For Low Input Voltages



TL/H/5550–5

National Semiconductor

LM113/LM313 Reference Diode

General Description

The LM113/LM313 are temperature compensated, low voltage reference diodes. They feature extremely-tight regulation over a wide range of operating currents in addition to an unusually-low breakdown voltage and good temperature stability.

The diodes are synthesized using transistors and resistors in a monolithic integrated circuit. As such, they have the same low noise and long term stability as modern IC op amps. Further, output voltage of the reference depends only on highly-predictable properties of components in the IC; so they can be manufactured and supplied to tight tolerances.

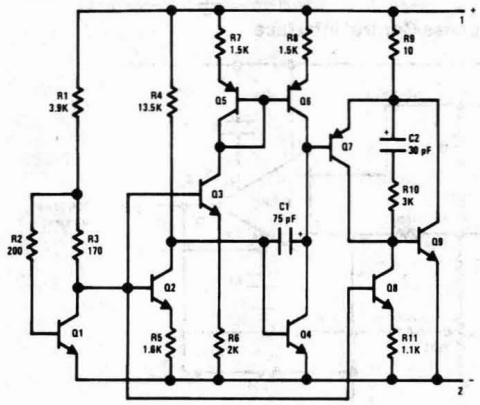
- Dynamic impedance of 0.3Ω from 500 μA to 20 mA
- Temperature stability typically 1% over −55°C to 125°C range (LM113), 0°C to 70°C (LM313)
- Tight tolerance: ±5%, ±2% or ±1%

The characteristics of this reference recommend it for use in bias-regulation circuitry, in low-voltage power supplies or in battery powered equipment. The fact that the breakdown voltage is equal to a physical property of silicon—the energy-band gap voltage—makes it useful for many temperature-compensation and temperature-measurement functions.

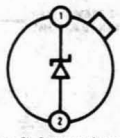
Features

- Low breakdown voltage: 1.220V

Schematic and Connection Diagrams



Metal Can Package



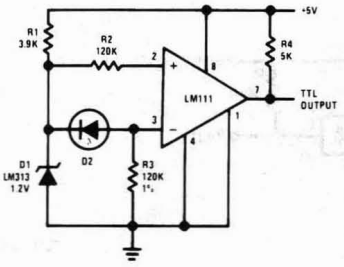
Note: Pin 2 connected to case.
TOP VIEW

Order Number
LM113H, LM113H/883,
LM113-1H, LM113-1H/883,
LM113-2H, LM113-2H/883,
or LM313H
See NS Package Number H02A

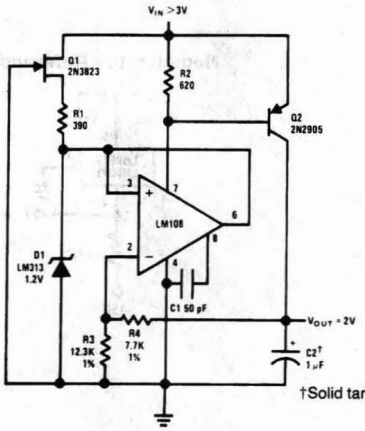
TL/H/5713–1

Typical Applications

Level Detector for Photodiode



Low Voltage Regulator



†Solid tantalum.

TL/H/5713–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Power Dissipation (Note 1)	100 mW
Reverse Current	50 mA
Forward Current	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature Range	
LM113	−55°C to +125°C
LM313	0°C to +70°C

Electrical Characteristics (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Reverse Breakdown Voltage					
LM113/LM313	I_R = 1 mA	1.160	1.220	1.280	V
LM113-1		1.210	1.22	1.232	V
LM113-2		1.195	1.22	1.245	V
Reverse Breakdown Voltage Change	0.5 mA ≤ I_R ≤ 20 mA		6.0	15	mV
Reverse Dynamic Impedance	I_R = 1 mA		0.2	1.0	Ω
	I_R = 10 mA		0.25	0.8	Ω
Forward Voltage Drop	I_F = 1.0 mA		0.67	1.0	V
RMS Noise Voltage	10 Hz ≤ f ≤ 10 kHz, I_R = 1 mA		5		μV
Reverse Breakdown Voltage Change with Current	0.5 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}			15	mV
Breakdown Voltage Temperature Coefficient	1.0 mA ≤ I_R ≤ 10 mA, T_{MIN} ≤ T_A ≤ T_{MAX}		0.01		%/°C

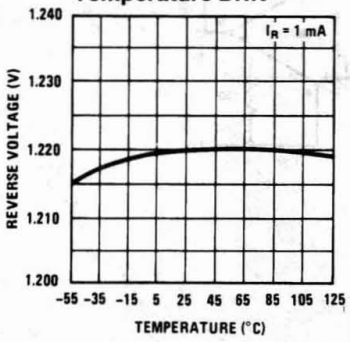
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction and a thermal resistance of 80°C/W junction to case or 440°C/W junction to ambient.

Note 2: These specifications apply for T_A = 25°C, unless stated otherwise. At high currents, breakdown voltage should be measured with lead lengths less than ¼ inch. Kelvin contact sockets are also recommended. The diode should not be operated with shunt capacitances between 200 pF and 0.1 μF, unless isolated by at least a 100Ω resistor, as it may oscillate at some currents.

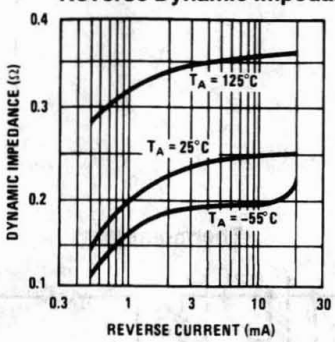
Note 3: Refer to the following RETS drawings for military specifications: RETS113-1X for LM113-1, RETS113-2X for LM113-2 or RETS113X for LM113.

Typical Performance Characteristics

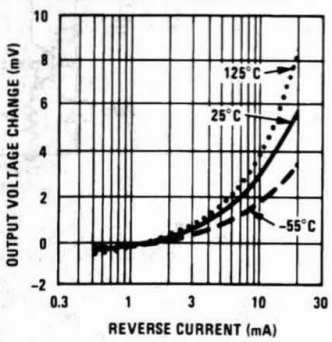
Temperature Drift



Reverse Dynamic Impedance



Reverse Characteristics

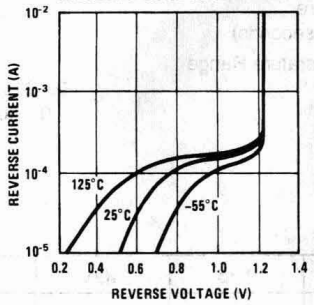


TL/H/5713–3

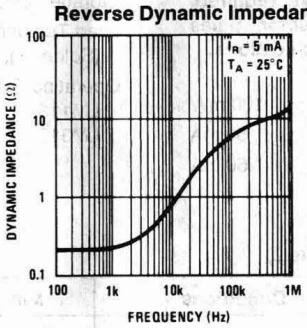
4

Typical Performance Characteristics (Continued)

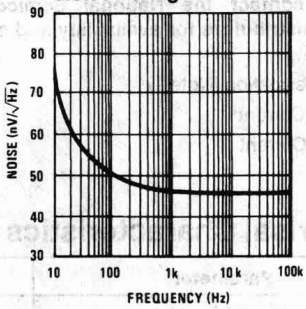
Reverse Characteristics



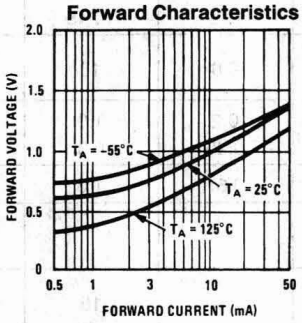
Reverse Dynamic Impedance



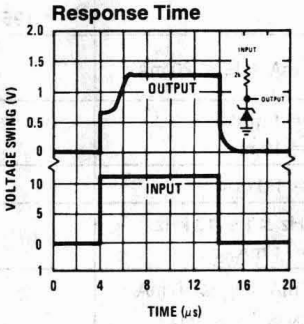
Noise Voltage



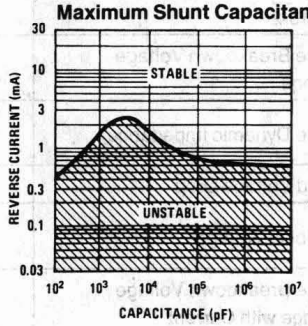
Forward Characteristics



Response Time



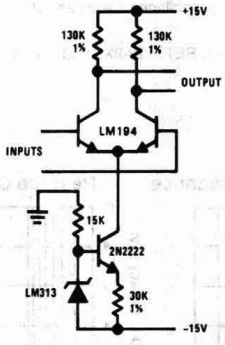
Maximum Shunt Capacitance



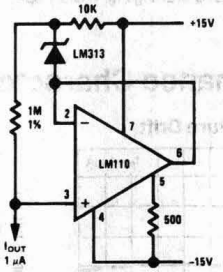
TL/H/5713–4

Typical Applications (Continued)

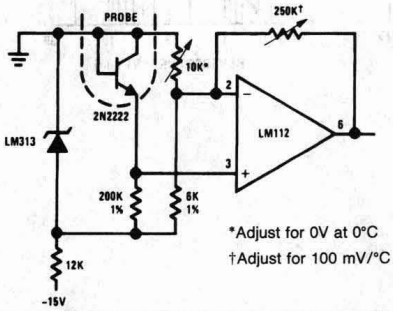
Amplifier Biasing for Constant Gain with Temperature



Constant Current Source



Thermometer



*Adjust for 0V at 0°C
†Adjust for 100 mV/°C

TL/H/5713–5

National Semiconductor

LM129/LM329 Precision Reference

General Description

The LM129 and LM329 family are precision multi-current temperature-compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long-term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shift in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

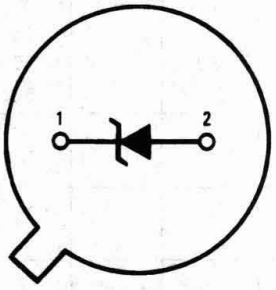
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0°C to 70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

Features

- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

Connection Diagrams

Metal Can Package (TO-46)



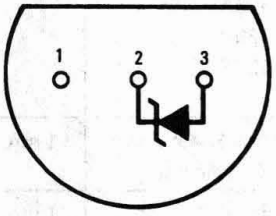
TL/H/5714–6

Bottom View

Pin 2 is electrically connected to case

Order Number LM129AH, LM129AH/883, LM129BH, LM129BH/883, LM129CH, LM329AH, LM329BH, LM329CH or LM329DH
See NS Package H02A

Plastic Package (TO-92)



TL/H/5714–4

Bottom View

Order Number LM329BZ, LM329CZ or LM329DZ
See NS Package Z03A

Typical Applications

Simple Reference

TL/H/5714–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Reverse Breakdown Current	30 mA
Forward Current	2 mA
Operating Temperature Range	
LM129	−55°C to +125°C
LM329	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
TO-92 package: 10 sec.	260°C
TO-46 package: 10 sec.	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM129A, B, C			LM329A, B, C, D			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6\ mA \le I_R \le 15\ mA$	6.7	6.9	7.2	6.6	6.9	7.25	V
Reverse Breakdown Change with Current (Note 3)	$T_A = 25°C$, $0.6\ mA \le I_R \le 15\ mA$		9	14		9	20	mV
Reverse Dynamic Impedance (Note 3)	$T_A = 25°C$, $I_R = 1\ mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \le F \le 10\ kHz$		7	20		7	100	μV
Long Term Stability (1000 hours)	$T_A = 45°C \pm 0.1°C$, $I_R = 1\ mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1\ mA$							
LM129A, LM329A			6	10		6	10	ppm/°C
LM129B, LM329B			15	20		15	20	ppm/°C
LM129C, LM329C			30	50		30	50	ppm/°C
LM329D						50	100	ppm/°C
Change In Reverse Breakdown Temperature Coefficient	$1\ mA \le I_R \le 15\ mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1\ mA \le I_R \le 15\ mA$		12			12		mV
Reverse Dynamic Impedance	$1\ mA \le I_R \le 15\ mA$		0.8			1		Ω

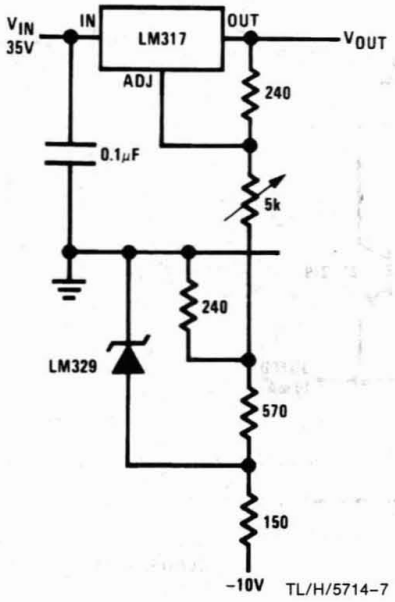
Note 1: These specifications apply for $-55°C \le T_A \le +125°C$ for the LM129 and $0°C \le T_A \le +70°C$ for the LM329 unless otherwise specified. The maximum junction temperature for an LM129 is 150°C and LM329 is 100°C. For operating at elevated temperature, devices in TO-46 package must be derated based on a thermal resistance of 440°C/W junction to ambient or 80°C/W junction to case. For the TO-92 package, the derating is based on 180°C/W junction to ambient with 0.4″ leads from a PC board and 160°C/W junction to ambient with 0.125″ lead length to a PC board.

Note 2: Refer to RETS129H for LM129 family military specifications.

Note 3: These changes are tested on a pulsed basis with a low duty-cycle. For changes versus temperature, compute in terms of tempco.

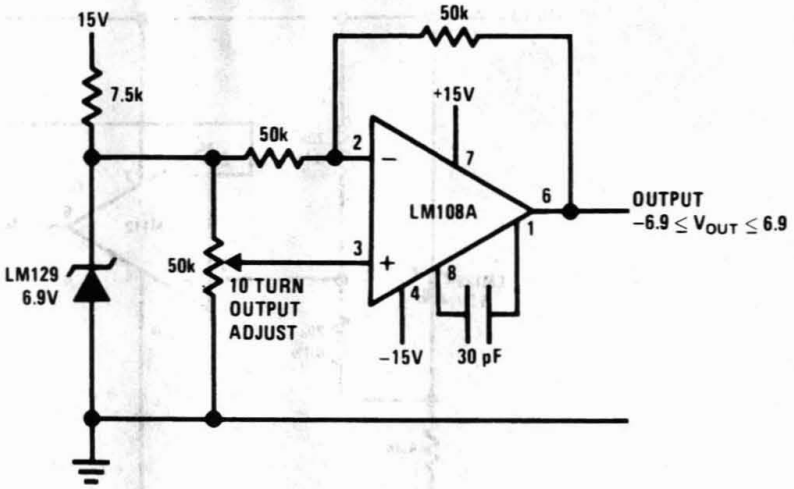
Typical Applications (Continued)

Low Cost 0–25V Regulator



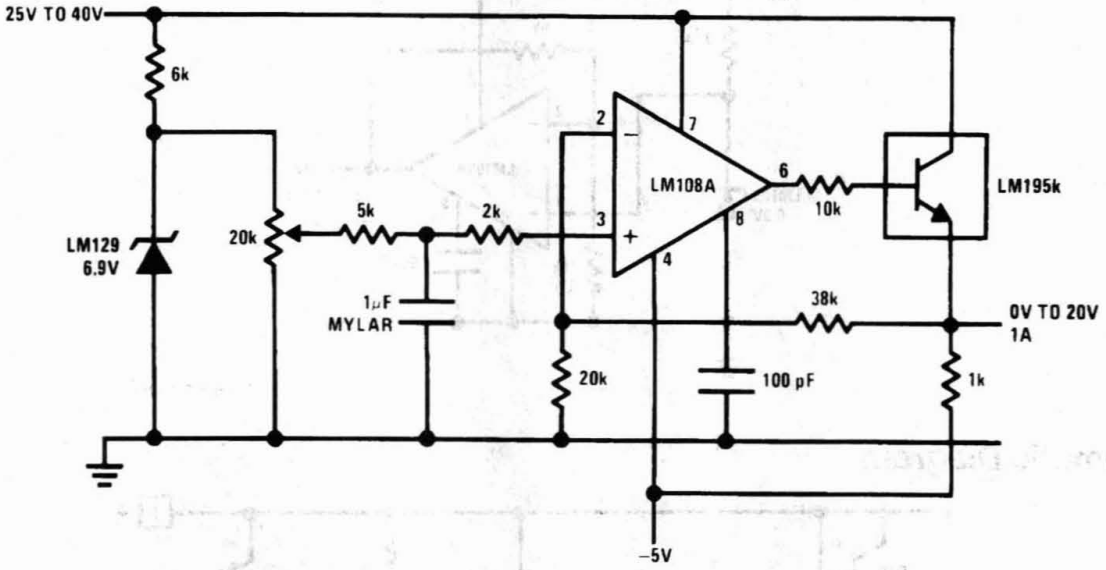
TL/H/5714–7

Adjustable Bipolar Output Reference



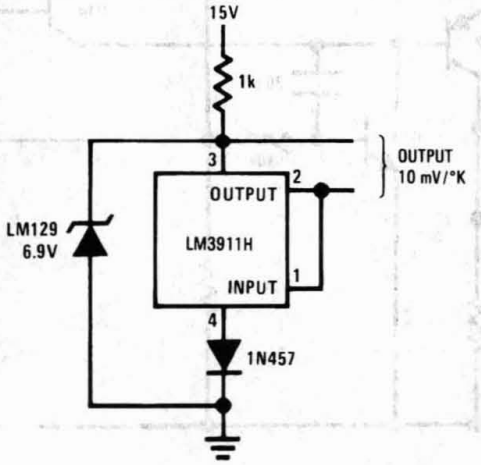
TL/H/5714–8

0V to 20V Power Reference



TL/H/5714–9

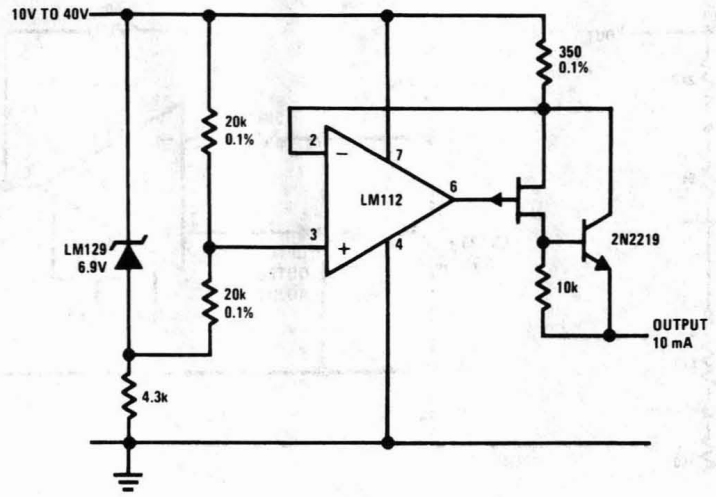
External Reference for Temperature Transducer



TL/H/5714–2

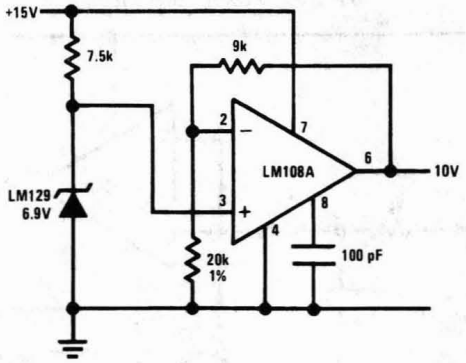
Typical Applications (Continued)

Positive Current Source



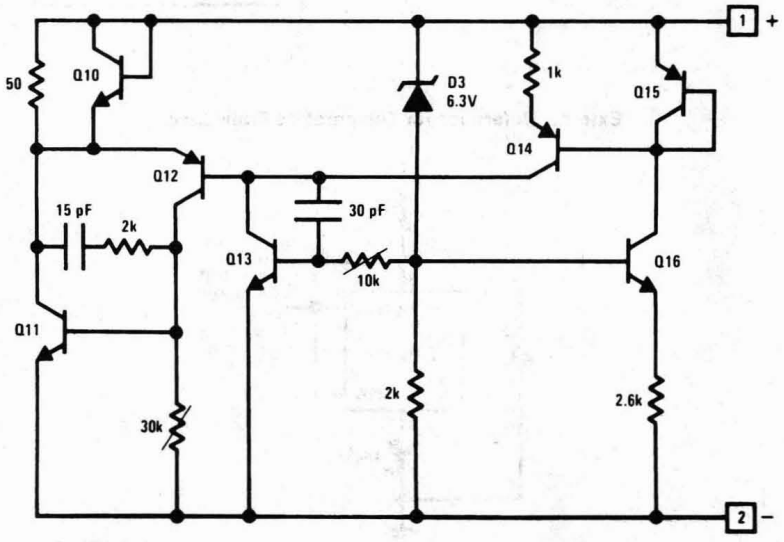
TL/H/5714–11

Buffered Reference with Single Supply



TL/H/5714–3

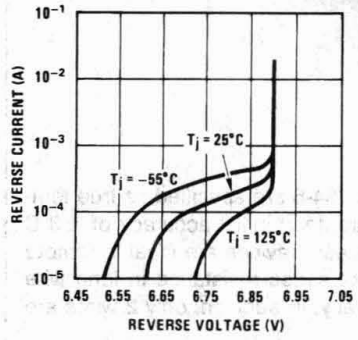
Schematic Diagram



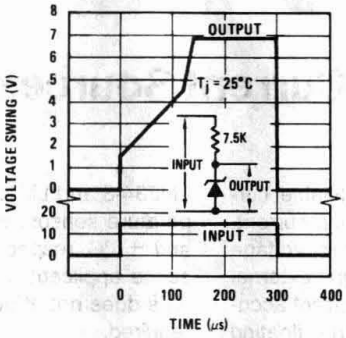
TL/H/5714–10

Typical Performance Characteristics

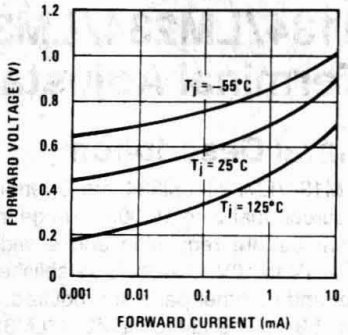
Reverse Characteristics



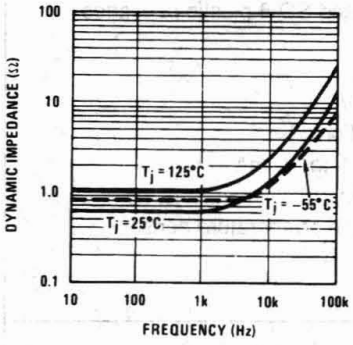
Response Time



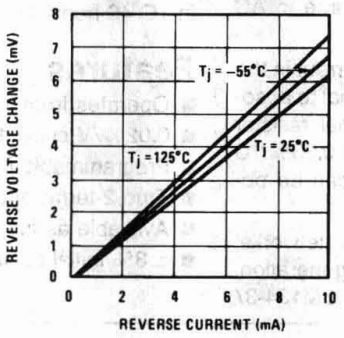
Forward Characteristics



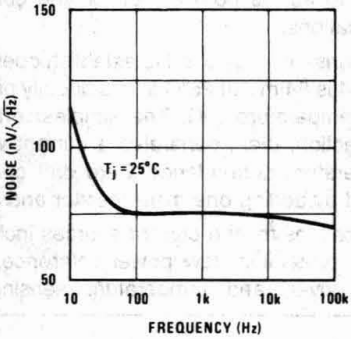
Dynamic Impedance



Reverse Voltage Change

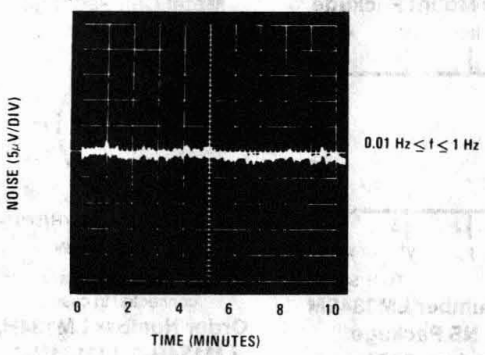


Zener Noise Voltage



TL/H/5714–12

Low Frequency Noise Voltage



TL/H/5714–5

National Semiconductor

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈ +0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

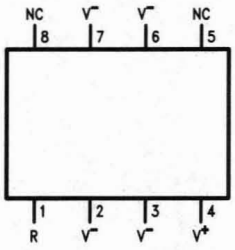
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic, TO-92 and SO-8 plastic packages.

Features

- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Connection Diagrams

SO-8
Surface Mount Package



TL/H/5697–24

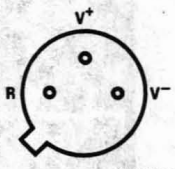
Order Number LM334M
See NS Package
Number M08A

SO-8 Alternative Pinout
Surface Mount Package

TL/H/5697–25

Order Number LM334SM
See NS Package
Number M08A

TO-46
Metal Can Package



TL/H/5697–12

Bottom View

V⁻ Pin is electrically connected to case.

Order Number LM134H, LM134H-3, LM134H-6, LM234H or LM334H
See NS Package
Number H03H

TO-92
Plastic Package

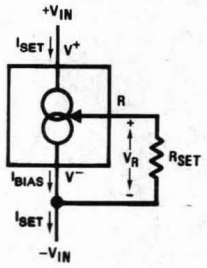
TL/H/5697–10

Bottom View

Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package
Number Z03A

Typical Application

Basic 2-Terminal Current Source



TL/H/5697–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^+ to V^- Forward Voltage	
LM134/LM234/LM334	40V
LM134-3/LM134-6/LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage	20V
R Pin to V^- Voltage	5V
Set Current	10 mA
Power Dissipation	400 mW
ESD Susceptibility (Note 5)	2000V

Operating Temperature Range (Note 4)	
LM134/LM134-3/LM134-6	−55°C to +125°C
LM234/LM234-3/LM234-6	−25°C to +100°C
LM334	0°C to +70°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM134/LM234			LM334			Units
		Min	Typ	Max	Min	Typ	Max	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$10\ \mu A \le I_{SET} \le 1$ mA			3			6	%
	1 mA $< I_{SET} \le 5$ mA			5			8	%
	$2\ \mu A \le I_{SET} < 10\ \mu A$			8			12	%
Ratio of Set Current to Bias Current	$100\ \mu A \le I_{SET} \le 1$ mA	14	18	23	14	18	26	
	1 mA $\le I_{SET} \le 5$ mA		14			14		
	$2\ \mu A \le I_{SET} \le 100\ \mu A$		18	23		18	26	
Minimum Operating Voltage	$2\ \mu A \le I_{SET} \le 100\ \mu A$		0.8			0.8		V
	$100\ \mu A < I_{SET} \le 1$ mA		0.9			0.9		V
	1 mA $< I_{SET} \le 5$ mA		1.0			1.0		V
Average Change in Set Current with Input Voltage	$2\ \mu A \le I_{SET} \le 1$ mA							
	$1.5V \le V^+ \le 5V$		0.02	0.05		0.02	0.1	%/V
	$5V \le V^+ \le 40V$		0.01	0.03		0.01	0.05	%/V
	1 mA $< I_{SET} \le 5$ mA							
	$1.5V \le V \le 5V$		0.03			0.03		%/V
	$5V \le V \le 40V$		0.02			0.02		%/V
Temperature Dependence of Set Current (Note 3)	$25\ \mu A \le I_{SET} \le 1$ mA	0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25°C$ with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. For the Basic 2-Terminal Current Source circuit shown on the first page of this data sheet. I_{SET} is determined by the following formula: $I_{SET} = 67.7\ mV/R_{SET}$ (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ $T_j = 25°C$ (227 μV/°C).

Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o\ (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Note 4: For elevated temperature operation, T_j max is:

LM134	150°C
LM234	125°C
LM334	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" leads) 160°C/W (0.125" leads)	440°C/W	165°C/W
θ_{jc} (Junction to Case)	N/A	32°C/W	80°C/W

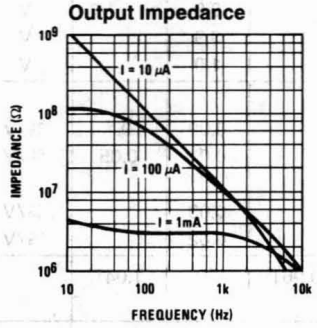
Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Electrical Characteristics (Note 1) (Continued)

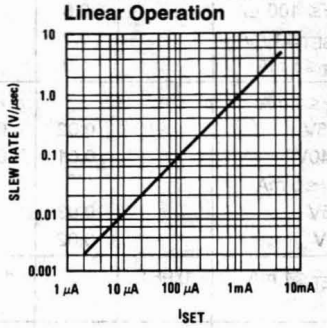
Parameter	Conditions	LM134-3, LM234-3			LM134-6, LM234-6			Units
		Min	Typ	Max	Min	Typ	Max	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$100\ \mu A \leq I_{SET} \leq 1\ mA$, $T_j = 25°$			±1			±2	%
Equivalent Temperature Error				±3			±6	°C
Ratio of Set Current to Bias Current	$100\ \mu A \leq I_{SET} \leq 1\ mA$	14	18	26	14	18	26	
Minimum Operating Voltage	$100\ \mu A\ I_{SET} \leq 1\ mA$		0.9			0.9		V
Average Change in Set Current with Input Voltage	$100\ \mu A \leq I_{SET} \leq 1\ mA$ $1.5 \leq V^+ \leq 5V$ $5V \leq V^+ \leq 30V$		0.02 0.01	0.05 0.03		0.02 0.01	0.01 0.05	%/V %/V
Temperature Dependence of Set Current (Note 3) and	$100\ \mu A \leq I_{SET} \leq 1\ mA$	0.98T	T	1.02T	0.97T	T	1.03T	
Equivalent Slope Error				±2			±3	%
Effective Shunt Capacitance			15			15		pF

Typical Performance Characteristics

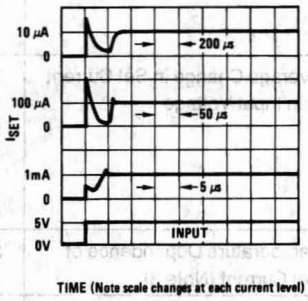
Output Impedance



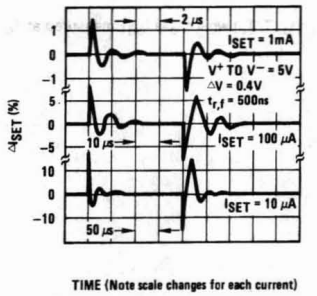
Maximum Slew Rate for Linear Operation



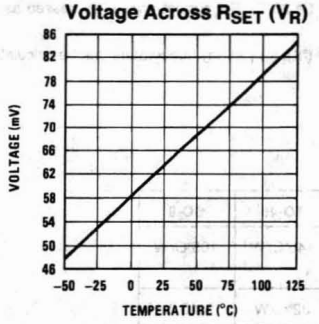
Start-Up



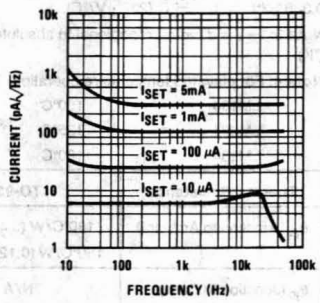
Transient Response



Voltage Across R_{SET} (V_R)



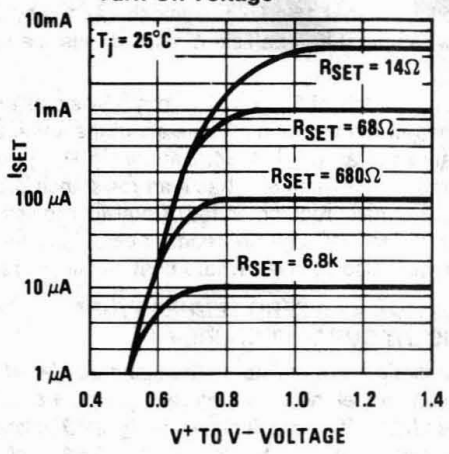
Current Noise



TL/H/5697–2

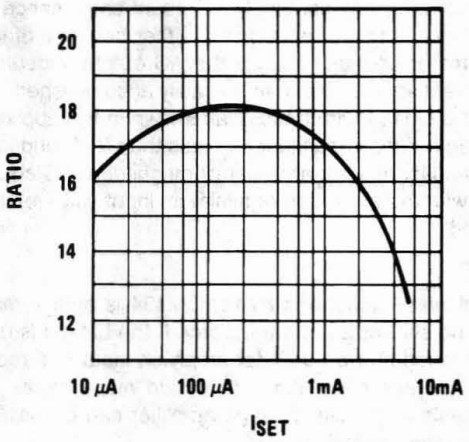
Typical Performance Characteristics (Continued)

Turn-On Voltage



TL/H/5697–29

Ratio of I_{SET} to I_{BIAS}



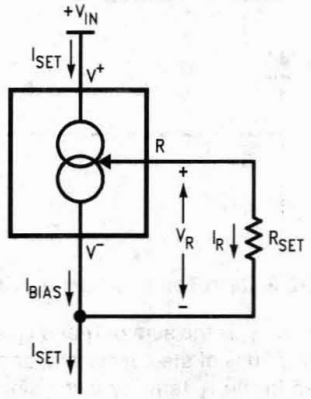
TL/H/5697–3

Application Hints

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

CALCULATING R_{SET}

The total current through the LM134 (I_{SET}) is the sum of the current going through the SET resistor (I_R) and the LM134's bias current (I_{BIAS}), as shown in *Figure 1.*



TL/H/5697–27

FIGURE 1. Basic Current Source

A graph showing the ratio of these two currents is supplied under **Ratio of I_{SET} to I_{BIAS}** in the Typical Performance Characteristics section. The current flowing through R_{SET} is determined by V_R, which is approximately 214 μV/°K (64 mV/298°K ~ 214 μV/°K).

$$I_{SET} = I_R + I_{BIAS} = \frac{V_R}{R_{SET}} + I_{BIAS}$$

Since (for a given set current) I_{BIAS} is simply a percentage of I_{SET}, the equation can be rewritten

$$I_{SET} = \left(\frac{V_R}{R_{SET}}\right)\left(\frac{n}{n-1}\right)$$

where n is the ratio of I_{SET} to I_{BIAS} as specified in the Electrical Characteristics Section and shown in the graph. Since n is typically 18 for 2 μA ≤ I_{SET} ≤ 1 mA, the equation can be further simplified to

$$I_{SET} = \left(\frac{V_R}{R_{SET}}\right)(1.059) = \frac{227\ \mu V/°K}{R_{SET}}$$

for most set currents.

SLEW RATE

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At I_{SET} = 10 μA, maximum dV/dt is 0.01V/μs; at I_{SET} = 1 mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100 μA. For example, each 1V increase across the LM134 at I_{SET} = 1 mA will increase junction temperature by ≈0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈0.33%/°C, so the change in current due to temperature rise will be (0.4) (0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100 μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

4

Application Hints (Continued)

SHUNT CAPACITANCE

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

NOISE

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12 dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

LEAD RESISTANCE

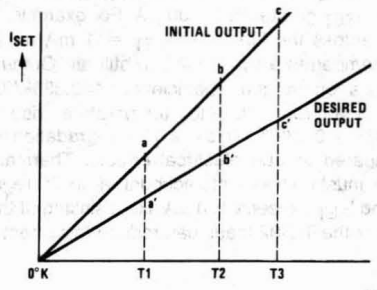
The sense voltage which determines operating current of the LM134 is less than 100 mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

SENSING TEMPERATURE

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\ \mu V/°K)\ (T)}{R_{SET}}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.



TL/H/5697–4

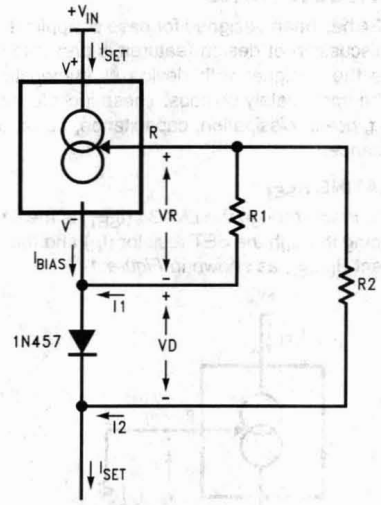
FIGURE 2. Gain Adjustment

This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before trimming. Line a′b′c′ is the desired output. A gain trim done at T2 will move the output from b to b′ and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

APPLICATION AS A ZERO TEMPERATURE COEFFICENT CURRENT SOURCE

Adding a diode and a resistor to the standard LM134 configuration can cancel the temperature-dependent characteristic of the LM134. The circuit shown in *Figure 3* balances the positive tempco of the LM134 (about +0.23 mV/°C) with the negative tempco of a forward-biased silicon diode (about −2.5 mV/°C).



TL/H/5697–28

FIGURE 3. Zero Tempco Current Source

The set current (I_{SET}) is the sum of I_1 and I_2, each contributing approximately 50% of the set current, and I_{BIAS}. I_{BIAS} is usually included in the I_1 term by increasing the V_R value used for calculations by 5.9%. (See **CALCULATING R_{SET}**.)

$$I_{SET} = I_1 + I_2 + I_{BIAS}, \text{ where}$$

$$I_1 = \frac{V_R}{R_1} \quad \text{and} \quad I_2 = \frac{V_R + V_D}{R_2}$$

The first step is to minimize the tempco of the circuit, using the following equations. An example is given using a value of +227 μV/°C as the tempco of the LM134 (which includes the I_{BIAS} component), and −2.5 mV/°C as the tempco of the diode (for best results, this value should be directly measured or obtained from the manufacturer of the diode).

$$I_{SET} = I_1 + I_2$$

$$\frac{dI_{SET}}{dT} = \frac{dI_1}{dT} + \frac{dI_2}{dT}$$

$$\approx \frac{227\ \mu V/°C}{R_1} + \frac{227\ \mu V/°C - 2.5\ mV/°C}{R_2}$$

$$= 0 \text{ (solve for tempco = 0)}$$

Application Hints (Continued)

$$\frac{R_2}{R_1} \approx \frac{2.5\ mV/°C - 227\ \mu V/°C}{227\ \mu V/°C} \approx 10.0$$

With the R_1 to R_2 ratio determined, values for R_1 and R_2 should be determined to give the desired set current. The formula for calculating the set current at T = 25°C is shown below, followed by an example that assumes the forward voltage drop across the diode (V_D) is 0.6V, the voltage across R_1 is 67.7 mV (64 mV + 5.9% to account for I_{BIAS}), and $R_2/R_1 = 10$ (from the previous calculations).

$$I_{SET} = I_1 + I_2 + I_{BIAS}$$

$$= \frac{V_R}{R_1} + \frac{V_R + V_D}{R_2}$$

$$\approx \frac{67.7\ mV}{R_1} + \frac{67.7\ mV + 0.6V}{10.0\ R_1}$$

$$I_{SET} \approx \frac{0.134V}{R_1}$$

This circuit will eliminate most of the LM134's temperature coefficient, and it does a good job even if the estimates of the diode's characteristics are not accurate (as the following example will show). For lowest tempco with a specific diode at the desired I_{SET}, however, the circuit should be built and tested over temperature. If the measured tempco of I_{SET} is positive, R_2 should be reduced. If the resulting tempco is negative, R_2 should be increased. The recommended diode for use in this circuit is the 1N457 because its tempco is centered at 11 times the tempco of the LM134, allowing $R_2 = 10\ R_1$. You can also use this circuit to create a current source with non-zero tempcos by setting the tempco component of the tempco equation to the desired value instead of 0.

EXAMPLE: A 1 mA, Zero-Tempco Current Source

First, solve for R_1 and R_2:

$$I_{SET} \approx 1\ mA = \frac{0.134V}{R_1}$$

$$R_1 = 134\Omega = 10\ R_2$$

$$R_2 = 1340\Omega$$

The values of R_1 and R_2 can be changed to standard 1% resistor values ($R_1 = 133\Omega$ and $R_2 = 1.33\ k\Omega$) with less than a 0.75% error.

If the forward voltage drop of the diode was 0.65V instead of the estimate of 0.6V (an error of 8%), the actual set current will be

$$I_{SET} = \frac{67.7\ mV}{R_1} + \frac{67.7\ mV + 0.65V}{R_2}$$

$$= \frac{67.7\ mV}{133} + \frac{67.7\ mV + 0.65V}{1330}$$

$$= 1.049\ mA$$

an error of less than 5%.

If the estimate for the tempco of the diode's forward voltage drop was off, the tempco cancellation is still reasonably effective. Assume the tempco of the diode is 2.6 mV/°C instead of 2.5 mV/°C (an error of 4%). The tempco of the circuit is now:

$$\frac{dI_{SET}}{dT} = \frac{dI_1}{dT} + \frac{dI_2}{dT}$$

$$= \frac{227\ \mu V/°C}{133\Omega} + \frac{227\ \mu V/°C - 2.6\ mV/°C}{1330\Omega}$$

$$= -77\ nA/°C$$

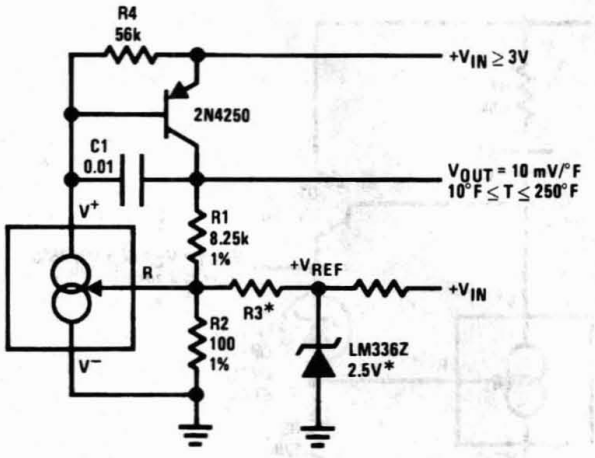
A 1 mA LM134 current source with no temperature compensation would have a set resistor of 68Ω and a resulting tempco of

$$\frac{227\ \mu V/°C}{68\Omega} = 3.3\ \mu A/°C$$

So even if the diode's tempco varies as much as ±4% from its estimated value, the circuit still eliminates 98% of the LM134's inherent tempco.

Typical Applications

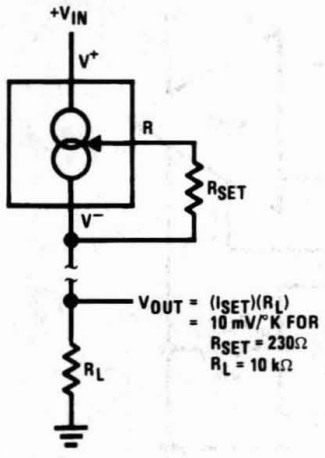
Ground Referred Fahrenheit Thermometer



TL/H/5697–15

*Select R3 = V_{REF}/583 μA. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

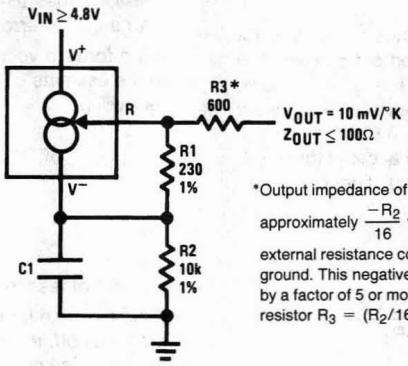
Terminating Remote Sensor for Voltage Output



TL/H/5697–14

Typical Applications (Continued)

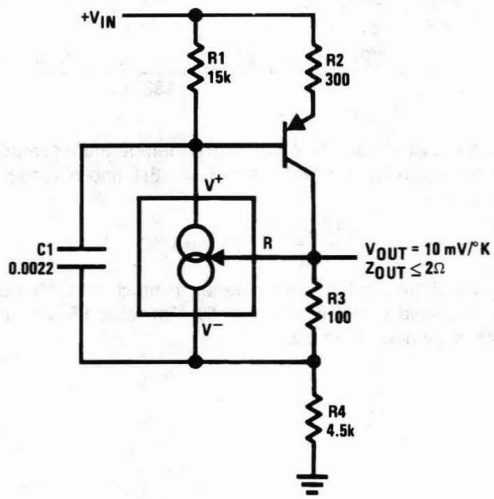
Low Output Impedance Thermometer



*Output impedance of the LM134 at the "R" pin is approximately $\frac{-R_2}{16}$ where R_2 is the equivalent external resistance connected from the V^- pin to ground. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor $R_3 = (R_2/16)$ in series with the output.

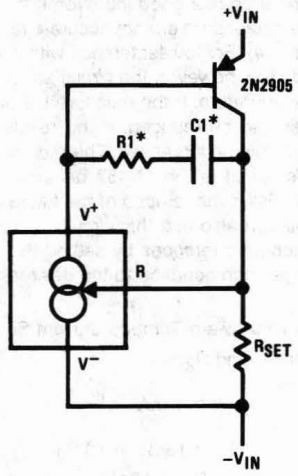
TL/H/5697–6

Low Output Impedance Thermometer



TL/H/5697–16

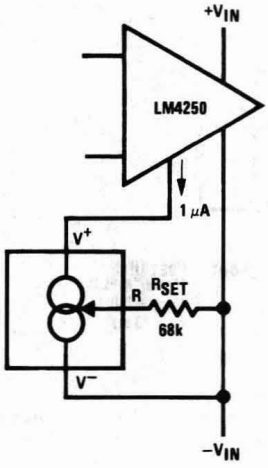
Higher Output Current



TL/H/5697–5

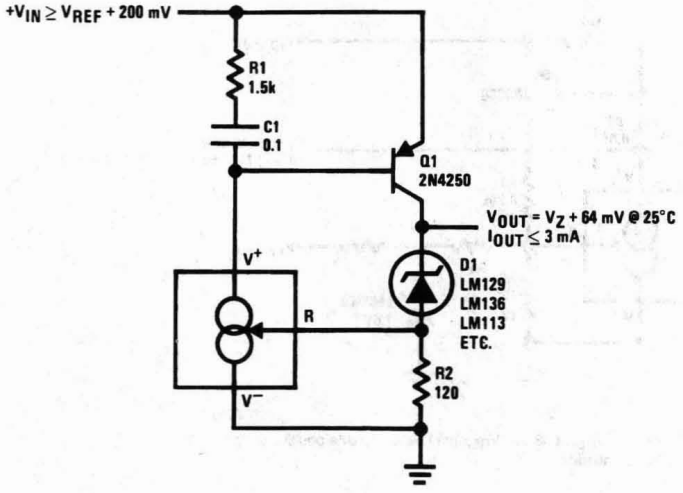
*Select R1 and C1 for optimum stability

Micropower Bias



TL/H/5697–17

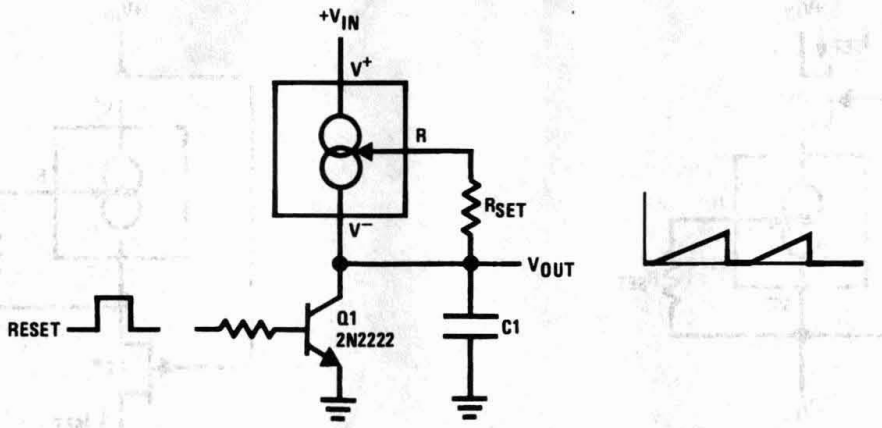
Low Input Voltage Reference Driver



TL/H/5697–18

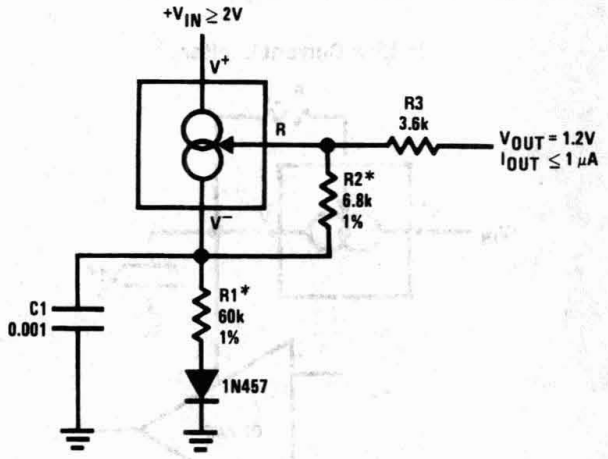
Typical Applications (Continued)

Ramp Generator



TL/H/5697–19

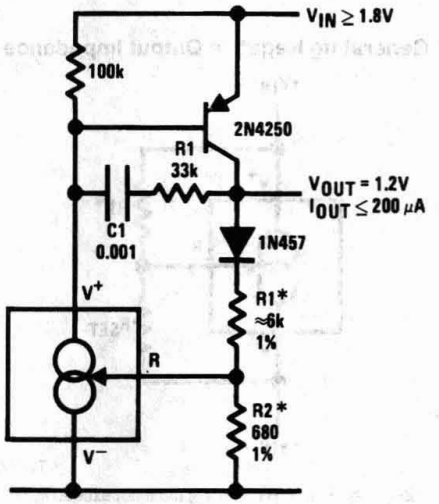
1.2V Reference Operates on 10 μA and 2V



TL/H/5697–20

*Select ratio of R1 to R2 to obtain zero temperature drift

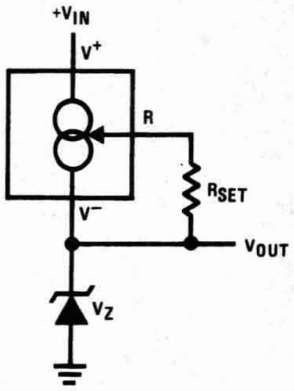
1.2V Regulator with 1.8V Minimum Input



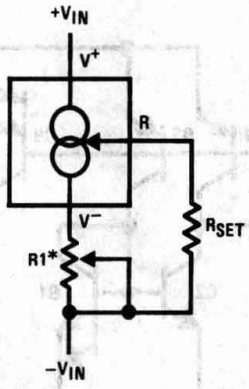
TL/H/5697–7

*Select ratio of R1 to R2 for zero temperature drift

Zener Biasing

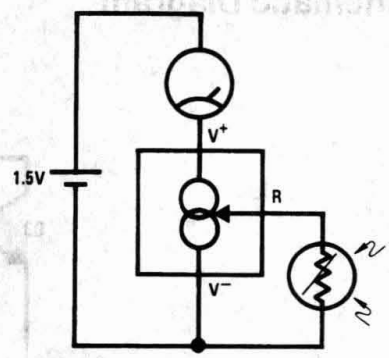


Alternate Trimming Technique



*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

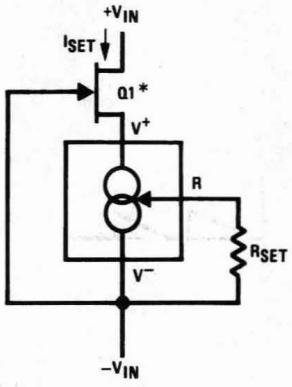
Buffer for Photoconductive Cell



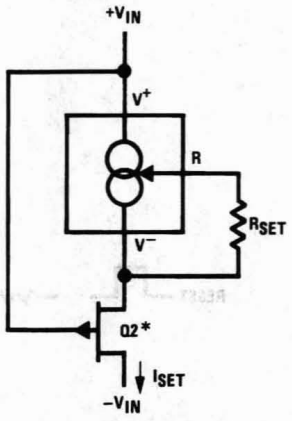
TL/H/5697–8

Typical Applications (Continued)

FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



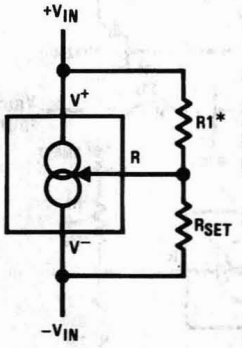
TL/H/5697–21



TL/H/5697–22

*Select Q1 or Q2 to ensure at least 1V across the LM134. $V_p\ (1 - I_{SET}/I_{DSS}) \geq 1.2V$.

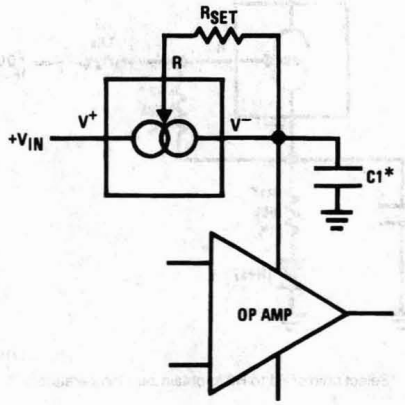
Generating Negative Output Impedance



TL/H/5697–23

*$Z_{OUT} \approx -16 \bullet R1\ (R1/V_{IN}$ must not exceed $I_{SET})$

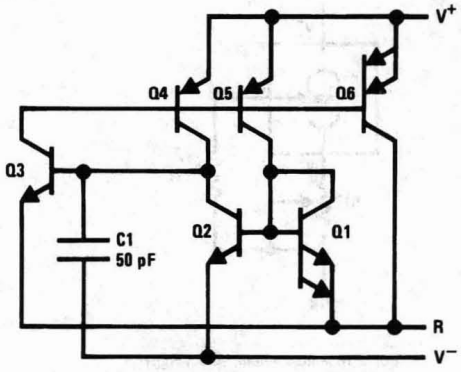
In-Line Current Limiter



TL/H/5697–9

*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

Schematic Diagram



TL/H/5697–11

National Semiconductor

LM136-2.5/LM236-2.5/LM336-2.5V Reference Diode

General Description

The LM136-2.5/LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low-temperature-coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-2.5 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136-2.5 is rated for operation over −55°C to +125°C while the LM236-2.5 is rated over a −25°C to +85°C temperature range.

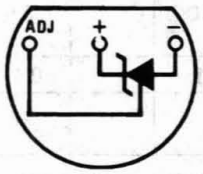
The LM336-2.5 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages.

Features

- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

TO-92
Plastic Package

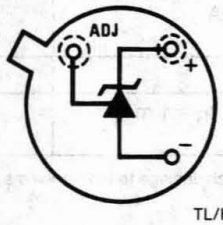


TL/H/5715–8

Bottom View

Order Number LM236Z-2.5, LM236AZ-2.5, LM336Z-2.5 or LM336BZ-2.5
See NS Package Number Z03A

TO-46
Metal Can Package

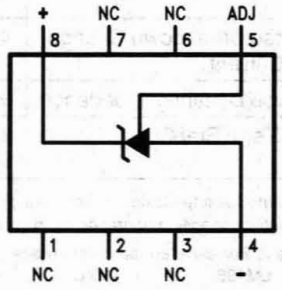


TL/H/5715–20

Bottom View

Order Number LM136H-2.5, LM136H-2.5/883, LM236H-2.5, LM136AH-2.5, LM136AH-2.5/883 or LM236AH-2.5
See NS Package Number H03H

SO Package



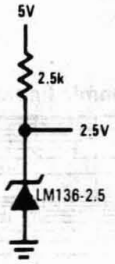
TL/H/5715–12

Top View

Order Number LM236M-2.5, LM236AM-2.5, LM336M-2.5 or LM336BM-2.5
See NS Package Number M08A

Typical Applications

2.5V Reference



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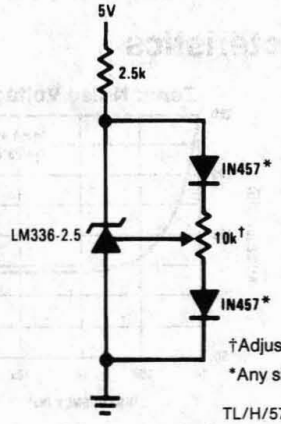
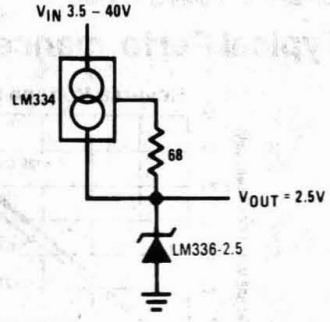
2.5V Reference with Minimum Temperature Coefficient



†Adjust to 2.490V
*Any silicon signal diode

TL/H/5715–10

Wide Input Range Reference



TL/H/5715–11

4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	−60°C to +150°C
Operating Temperature Range (Note 2)	
LM136	−55°C to +150°C
LM236	−25°C to +85°C
LM336	0°C to +70°C

Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM136A-2.5/LM236A-2.5 LM136-2.5/LM236-2.5			LM336B-2.5 LM336-2.5			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136, LM236, LM336	2.440	2.490	2.540	2.390	2.490	2.590	V
	LM136A, LM236A, LM336B	2.465	2.490	2.515	2.440	2.490	2.540	V
Reverse Breakdown Change With Current	$T_A = 25°C$, 400 $\mu A \le I_R \le 10$ mA		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA, f = 100 Hz		0.2	0.6		0.2	1	Ω
Temperature Stability (Note 4)	V_R Adjusted to 2.490V							
	$I_R = 1$ mA, *(Figure 2)*							
	$0°C \le T_A \le 70°C$ (LM336)					1.8	6	mV
	$-25°C \le T_A \le +85°C$ (LM236H, LM236Z)		3.5	9				mV
	$-25°C \le T_A \le +85°C$ (LM236M)		7.5	18				mV
	$-55°C \le T_A \le +125°C$ (LM136)		12	18				mV
Reverse Breakdown Change With Current	400 $\mu A \le I_R \le 10$ mA		3	10		3	12	mV
Reverse Dynamic Impedance	$I_R = 1$ mA		0.4	1		0.4	1.4	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA, t = 1000 hrs		20			20		ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: For elevated temperature operation, T_j max is:

LM136	150°C
LM236	125°C
LM336	100°C

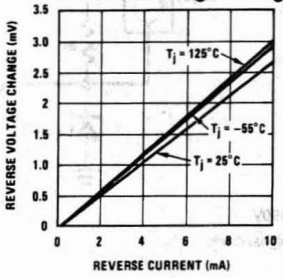
Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" leads) 170°C/W (0.125" lead)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	n/a	80°C/W	n/a

Note 3: Unless otherwise specified, the LM136-2.5 is specified from $-55°C \le T_A \le +125°C$, the LM236-2.5 from $-25°C \le T_A \le +85°C$ and the LM336-2.5 from $0°C \le T_A \le +70°C$.

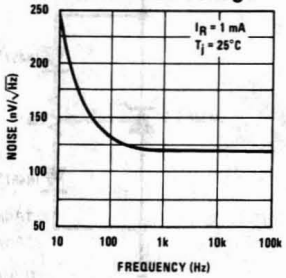
Note 4: Temperature stability for the LM336 and LM236 family is guaranteed by design. Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Stability is defined as the maximum change in V_{ref} from 25°C to T_A (min) or T_A (max).

Typical Performance Characteristics

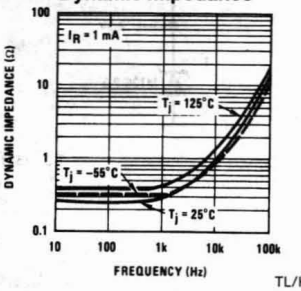
Reverse Voltage Change



Zener Noise Voltage



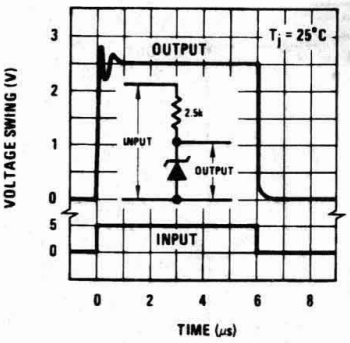
Dynamic Impedance



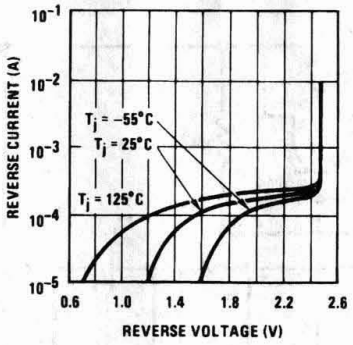
TL/H/5715–2

Typical Performance Characteristics (Continued)

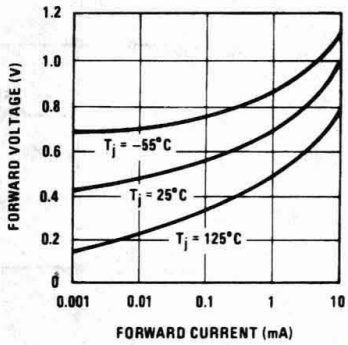
Response Time



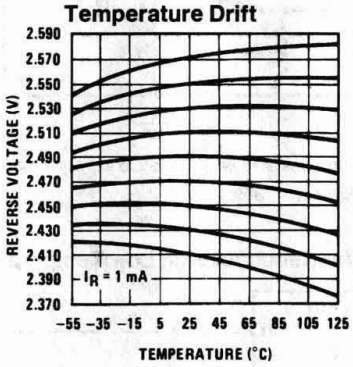
Reverse Characteristics



Forward Characteristics



Temperature Drift



TL/H/5715–3

Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

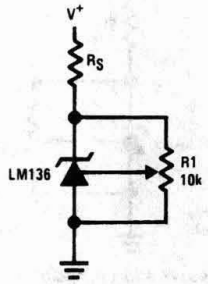


FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage (Trim Range = ±120 mV typical)

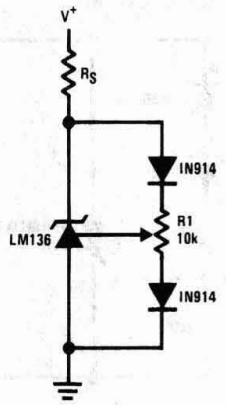


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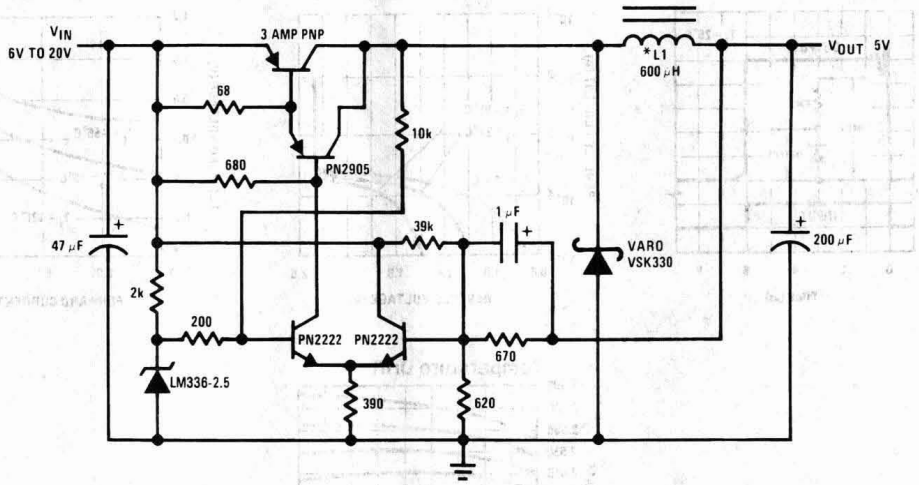
FIGURE 2. Temperature Coefficient Adjustment (Trim Range = ±70 mV typical)

4

Typical Applications (Continued)

Low Cost 2 Amp Switching Regulator†

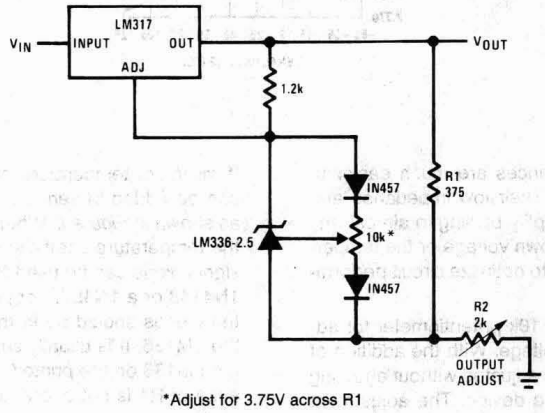


*L1 60 turns #16 wire on Arnold Core A-254168-2

†Efficiency ≈ 80%

TL/H/5715–5

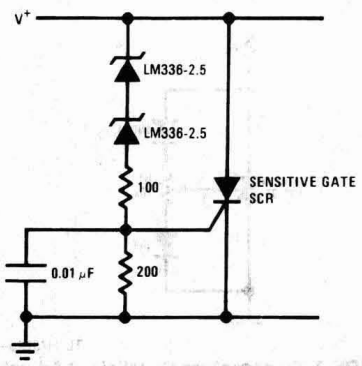
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75V across R1

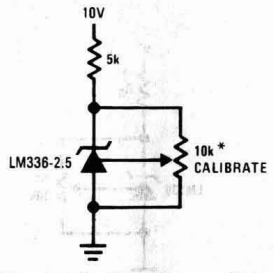
TL/H/5715–13

5V Crowbar



TL/H/5715–14

Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage

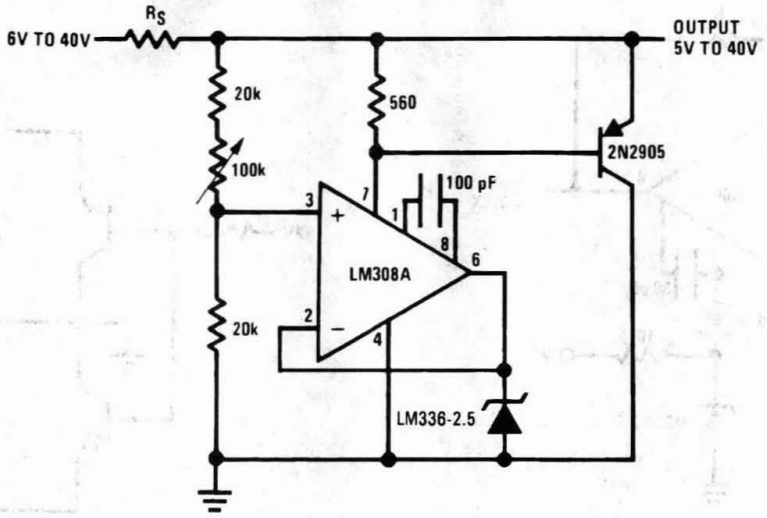


*Does not affect temperature coefficient

TL/H/5715–15

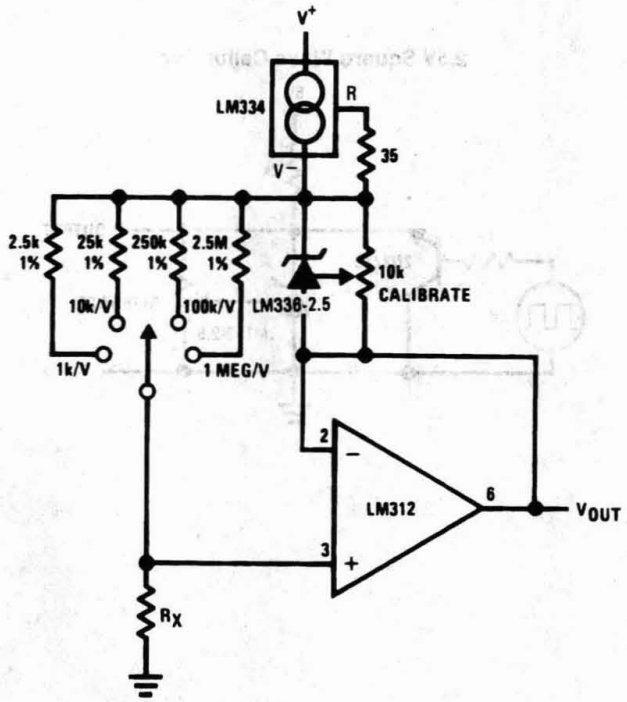
Typical Applications (Continued)

Adjustable Shunt Regulator



TL/H/5715–6

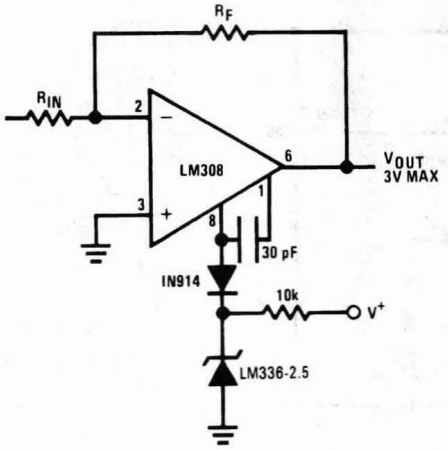
Linear Ohmmeter



TL/H/5715–16

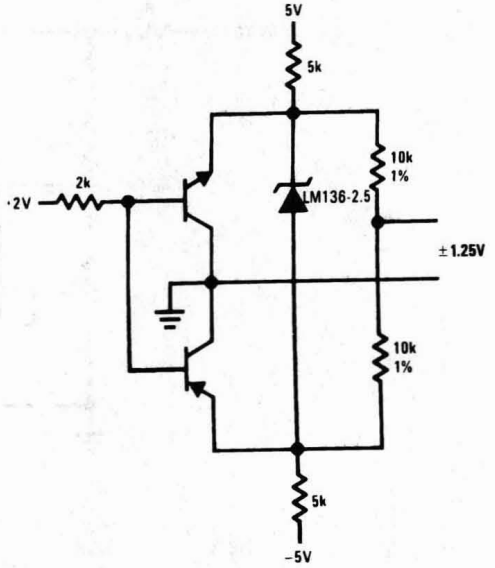
Typical Applications (Continued)

Op Amp with Output Clamped



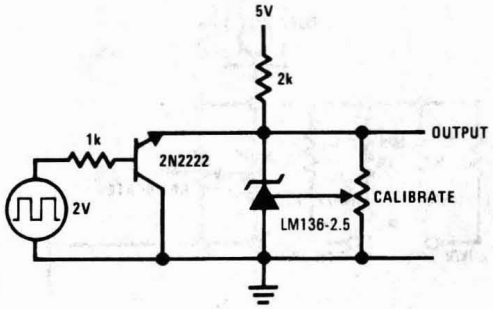
TL/H/5715–17

Bipolar Output Reference



TL/H/5715–18

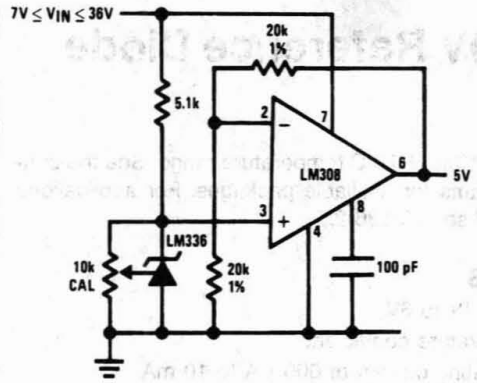
2.5V Square Wave Calibrator



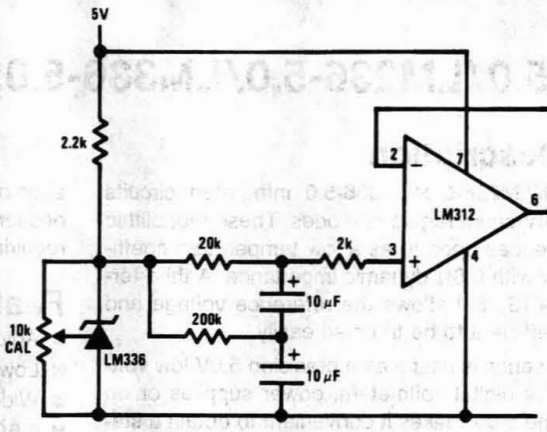
TL/H/5715–19

Typical Applications (Continued)

5V Buffered Reference

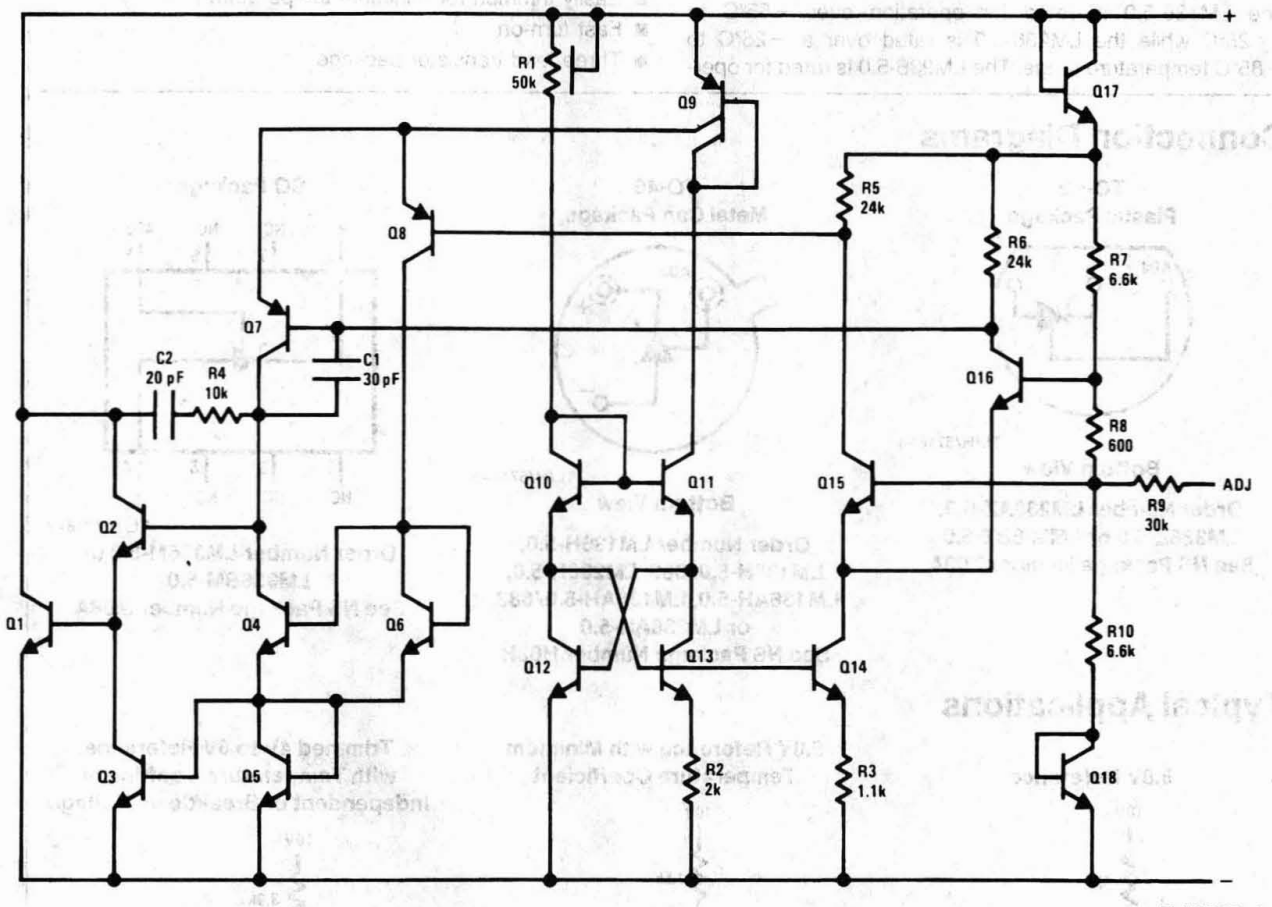


Low Noise Buffered Reference



TL/H/5715–7

Schematic Diagram



TL/H/5715–1

National Semiconductor

LM136-5.0/LM236-5.0/LM336-5.0, 5.0V Reference Diode

General Description

The LM136-5.0/LM236-5.0/LM336-5.0 integrated circuits are precision 5.0V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 5.0V zener with 0.6Ω dynamic impedance. A third terminal on the LM136-5.0 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-5.0 series is useful as a precision 5.0V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 5.0V makes it convenient to obtain a stable reference from low voltage supplies. Further, since the LM136-5.0 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

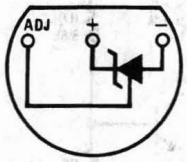
The LM136-5.0 is rated for operation over −55°C to +125°C while the LM236-5.0 is rated over a −25°C to +85°C temperature range. The LM336-5.0 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages. For applications requiring 2.5V see LM136-2.5.

Features

- Adjustable 4V to 6V
- Low temperature coefficient
- Wide operating current of 600 μA to 10 mA
- 0.6Ω dynamic impedance
- ± 1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

TO-92
Plastic Package

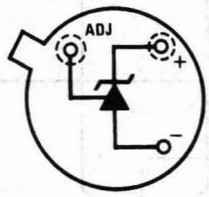


TL/H/5716–4

Bottom View

Order Number LM236AZ-5.0, LM336Z-5.0 or LM336BZ-5.0
See NS Package Number Z03A

TO-46
Metal Can Package

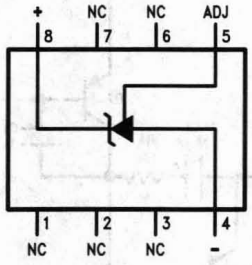


TL/H/5716–5

Bottom View

Order Number LM136H-5.0, LM136H-5.0/883, LM236H-5.0, LM136AH-5.0, LM136AH-5.0/883, or LM236AH-5.0
See NS Package Number H03H

SO Package

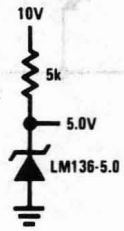


TL/H/5716–7

Order Number LM336M-5.0 or LM336BM-5.0
See NS Package Number M08A

Typical Applications

5.0V Reference



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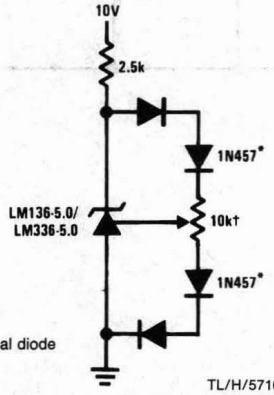
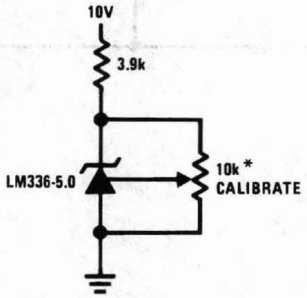
5.0V Reference with Minimum Temperature Coefficient



†Adjust to 5.00V
*Any silicon signal diode

TL/H/5716–15

Trimmed 4V to 6V Reference with Temperature Coefficient Independent of Breakdown Voltage



TL/H/5716–3

*Does not affect temperature coefficient

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	15mA
Forward Current	10mA
Storage Temperature	−60°C to +150°C
Operating Temperature Range (Note 2)	
LM136-5.0	−55°C to +150°C
LM236-5.0	−25°C to +85°C
LM336-5.0	0°C to +70°C

Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM136A-5.0/LM236A-5.0 LM136-5.0/LM236-5.0			LM336B-5.0 LM336-5.0			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1$ mA							
	LM136-5.0/LM236-5.0/LM336-5.0	4.9	5.00	5.1	4.8	5.00	5.2	V
	LM136A-5.0/LM236A-5.0, LM336B-5.0	4.95	5.00	5.05	4.90	5.00	5.1	V
Reverse Breakdown Change With Current	$T_A = 25°C$, 600 $\mu A \le I_R \le 10$ mA		6	12		6	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1$ mA, f = 100 Hz		0.6	1.2		0.6	2	Ω
Temperature Stability (Note 4)	V_R Adjusted 5.00V, $I_R = 1$ mA, (*Figure 2*)							
	$0°C \le T_A \le 70°C$ (LM336-5.0)					4	12	mV
	$-25°C \le T_A \le +85°C$ (LM236-5.0)		7	18				mV
	$-55°C \le T_A \le +125°C$ (LM136-5.0)		20	36				mV
Reverse Breakdown Change With Current	600 $\mu A \le I_R \le 10$ mA		6	17		6	24	mV
Adjustment Range	Circuit of *Figure 1*		±1			±1		V
Reverse Dynamic Impedance	I_R = 1 mA		0.8	1.6		0.8	2.5	Ω
Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA, t = 1000 hrs		20			20		ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: For elevated temperature operation, T_j max is:

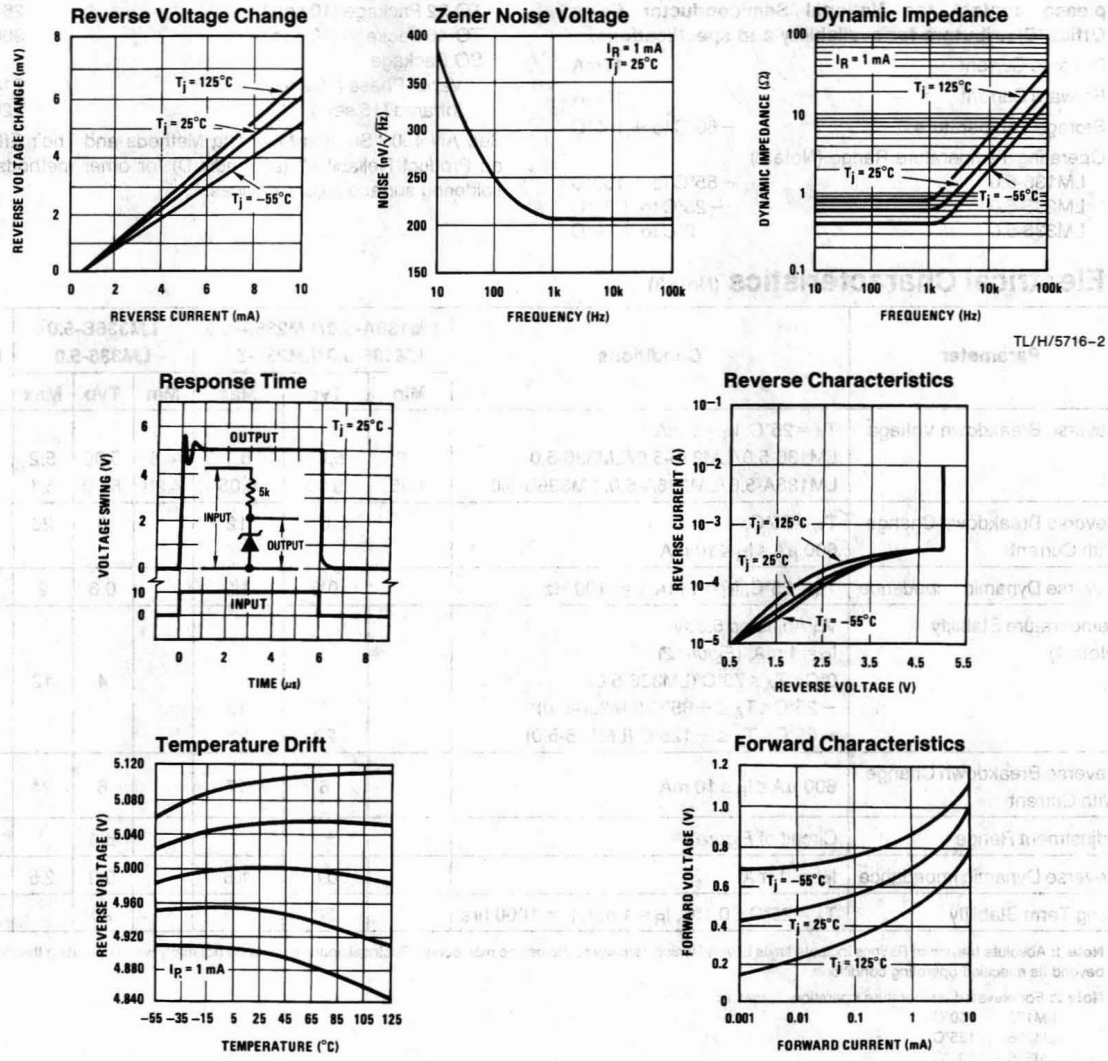
LM136	150°C
LM236	125°C
LM336	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" Leads) 170°C/W (0.125" Leads)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	N/A	80°C/W	N/A

Note 3: Unless otherwise specified, the LM136-5.0 is specified from $-55°C \le T_A \le +125°C$, the LM236-5.0 from $-25°C \le T_A \le +85°C$ and the LM336-5.0 from $0°C \le T_A \le +70°C$.

Note 4: Temperature stability for the LM336 and LM236 family is guaranteed by design. Design limits are guaranteed (but not 100% percent production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Stability is defined as the maximum charge in V_{REF} from 25°C to T_A(min) or T_A(max).

Typical Performance Characteristics



TL/H/5716–2

TL/H/5716–8

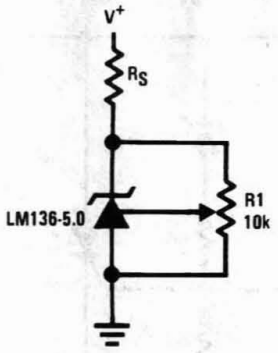
Application Hints

The LM136-5.0 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

Figure 1 shows an LM136-5.0 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

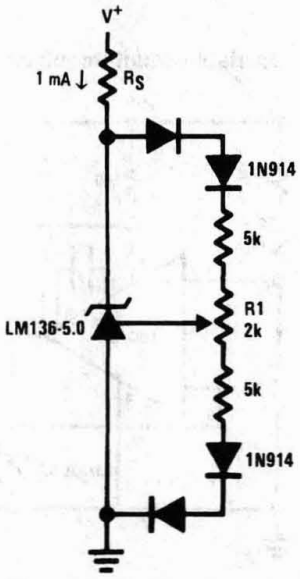
If minimum temperature coefficient is desired, four diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 5.00V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136-5.0. It is usually sufficient to mount the diodes near the LM136-5.0 on the printed circuit board. The absolute resistance of the network is not critical and any value from 2k to 20k will work. Because of the wide adjustment range, fixed resistors should be connected in series with the pot to make pot setting less critical.

Application Hints (Continued)



TL/H/5716–9

FIGURE 1. LM136-5.0 with Pot for Adjustment of Breakdown Voltage (Trim Range = ±1.0V Typical)

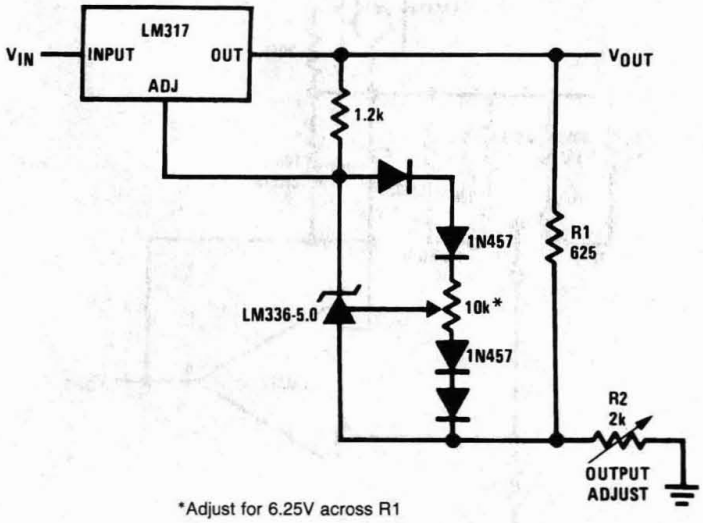


TL/H/5716–10

FIGURE 2. Temperature Coefficient Adjustment (Trim Range = ±0.5V Typical)

Typical Applications (Continued)

Precision Power Regulator with Low Temperature Coefficient

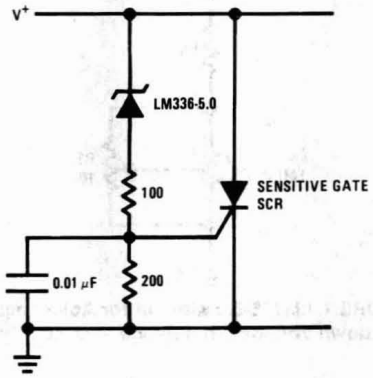


*Adjust for 6.25V across R1

TL/H/5716–11

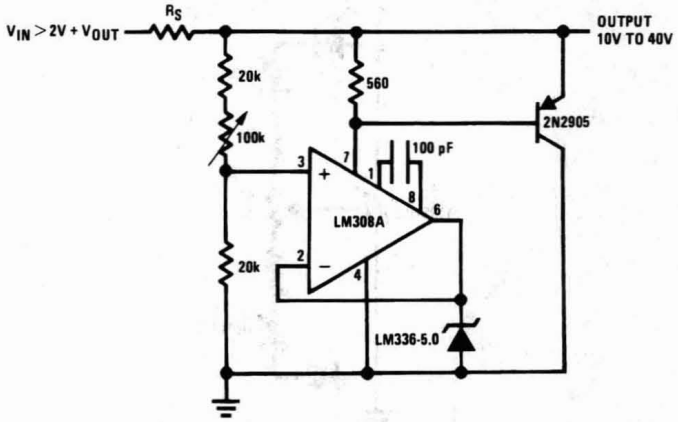
Typical Applications (Continued)

5V Crowbar



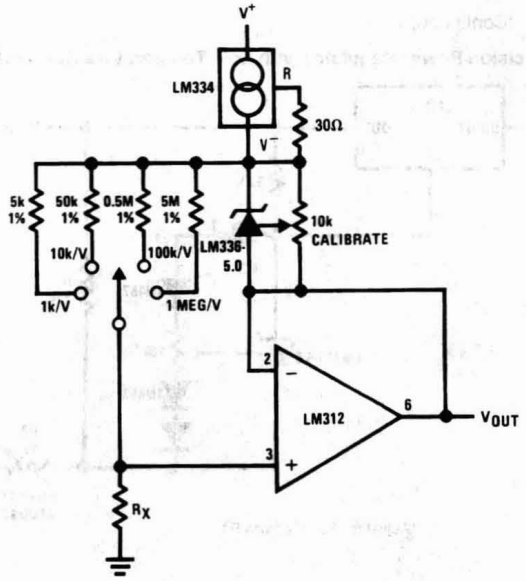
TL/H/5716–12

Adjustable Shunt Regulator



TL/H/5716–13

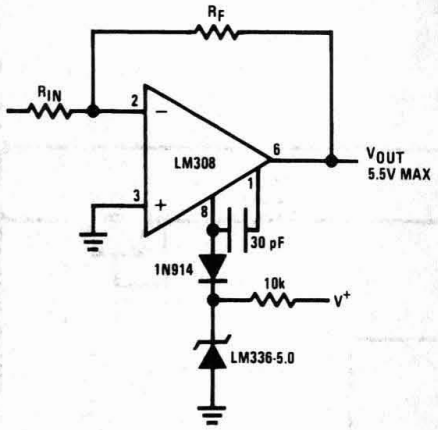
Linear Ohmmeter



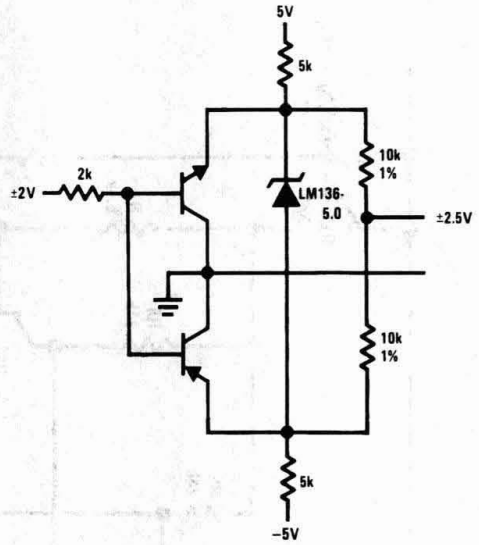
TL/H/5716–14

Typical Applications (Continued)

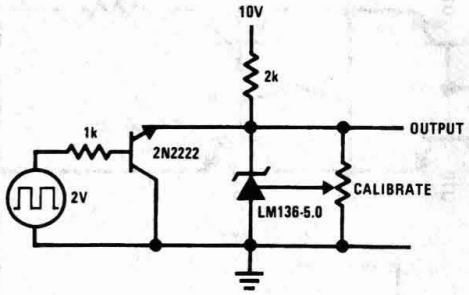
Op Amp with Output Clamped



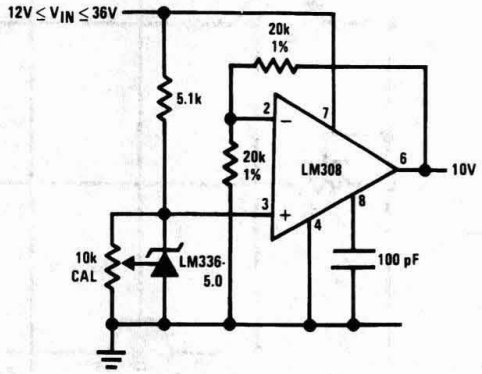
Bipolar Output Reference



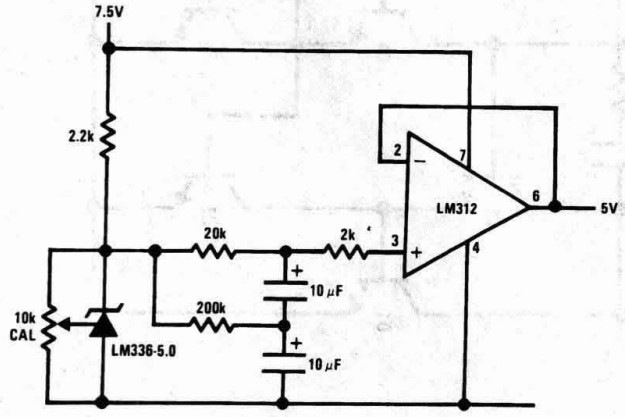
5.0V Square Wave Calibrator



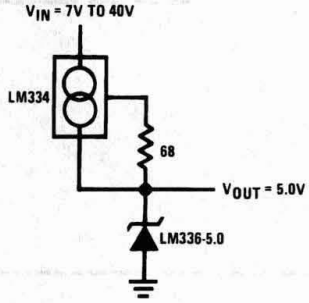
10V Buffered Reference



Low Noise Buffered Reference

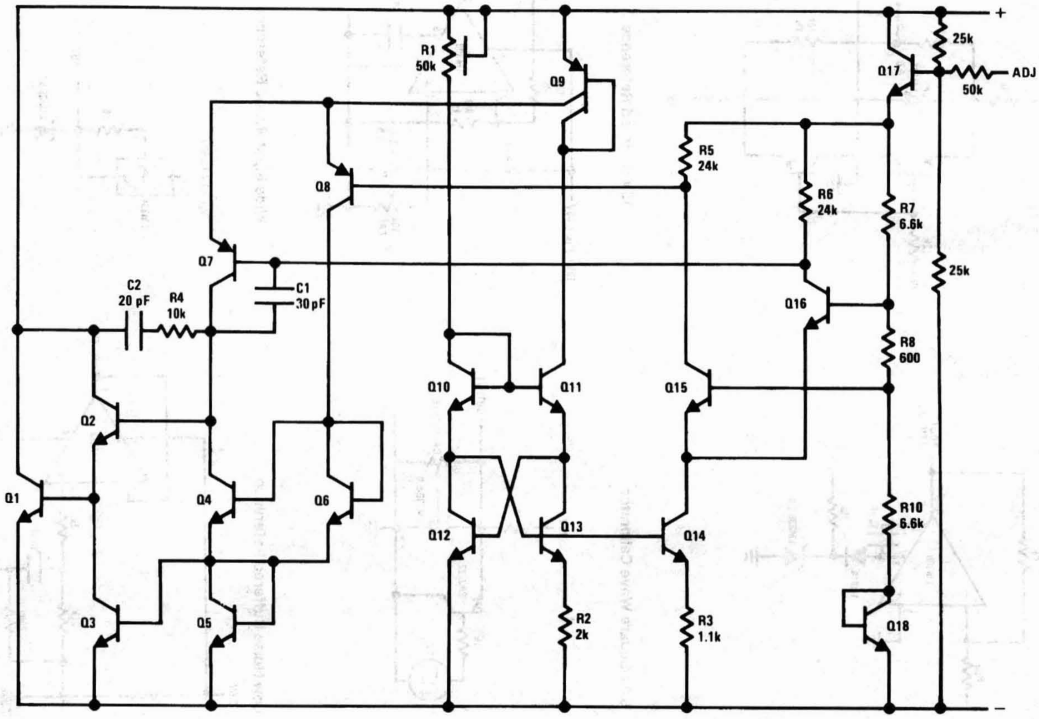


Wide Input Range Reference



TL/H/5716–6

Schematic Diagram



TL/H/5716–16

National Semiconductor

LM169/LM369 Precision Voltage Reference

General Description

The LM169/LM369 are precision monolithic temperature-compensated voltage references. They are based on a buried zener reference as pioneered in the LM199 references, but do not require any heater, as they rely on special temperature-compensation techniques (Patent Pending). The LM169 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{out} (as low as 1 ppm/°C), along with tight initial tolerances (as low as 0.05% max). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM169 also provides excellent stability vs. changes in input voltage and output current (both sourcing and sinking). The devices have a 10.000V output and will operate in either series or shunt mode; the output is short-circuit-proof to ground. A trim pin is available which permits fine-trimming of V_{out}, and also permits filtering to greatly decrease the output noise by adding a small capacitor (0.05 to 0.5 μF).

Features

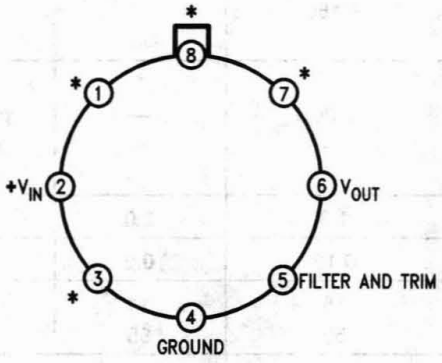
- Low Tempco — 3 ppm/°C (max)
- Excellent initial accuracy — ±5 mV (max)
- Excellent line regulation — 4 ppm/V (max)
- Excellent output impedance — ±0.8Ω (max)
- Excellent thermal regulation — ±20 ppm/100 mW (max)
- Low noise
- Easy to filter output noise
- Operates in series or shunt mode

Applications

- High-Resolution Data Acquisition Systems
- Digital volt meters
- Weighing systems
- Precision current sources
- Test Equipment

Connection Diagrams

Metal Can Package (H)



TL/H/9110–1

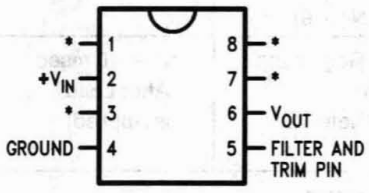
Top View

(Case is connected to ground.)

*Do not connect; internal connection for factory trims.

Order Number LM169H, LM169BH, LM169H/883, LM369H or LM369BH
See NS Package Number H08C

Dual-In-Line Package (N) or S.O. Package (M)



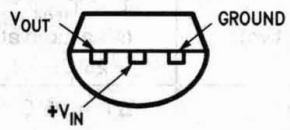
TL/H/9110–5

Top View

Order Number LM369DM, LM369DMX, LM369N, LM369BN, LM369CN or LM369DN**
See NS Package Number M08A or N08E

**X denotes 2500 units on Tape and Reel and is not included in the device part number marking

TO-226 Plastic Package (RC)



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Bottom View

Order Number LM369DRC
See NS Package Number RC03A

4

Absolute Maximum Ratings (Note 8)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (Series Mode)	35V
Reverse Current (Shunt Mode)	50 mA
Power Dissipation (Note 7)	600 mW
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	(T_j min to T_j max)
LM169H, LM169H/883	−55°C to +125°C
LM369	0°C to +70°C

Soldering Information

DIP (N) or Plastic (RC) Package, 10 sec.	+260°C
H08 (H) Package, 10 sec.	+300°C
SO (M) Package, Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

ESD Tolerance

C_{zap} = 100 pF, R_{zap} = 1.5k 800V

Electrical Characteristics, LM169, LM369 (Note 1)

Parameter	Conditions	Typical	Tested Limits (Notes 2, 13)	Design Limit (Note 3)	Units (Max Unless Noted)
V_{out} Nominal		+10.000			V
V_{out} Error	(Note 11)	50 0.50	±500 ±5		ppm mV
V_{out} Tempco LM169B, LM369B LM169, LM369 LM369C (Note 6) (Note 11)	 $T_{min} < T_j < T_{max}$ $T_{min} < T_j < T_{max}$ $T_{min} < T_j < T_{max}$	 1.0 2.7 6	 **3.0** **5.0** **10**	 — — —	 ppm/°C ppm/°C ppm/°C
Line Regulation	13V ≤ V_{IN} ≤ 30V	2.0	4.0	**8.0**	ppm/V
Load Regulation Sourcing Sinking (Note 12) (Note 4, Note 9)	 0 to 10 mA 0 to −10 mA	 +3 +80	 ±8.0 +150	 **20.0**	 ppm/mA ppm/mA
Thermal Regulation Sourcing Sinking (Note 12) (Note 5)	(t = 10 msec After Load is Applied)	 3.0 3.0	 ±20 —	 — —	 ppm/100 mW ppm/100 mW
Supply Current		1.4	1.8	**2.0**	mA
ΔSupply Current	13V ≤ V_{IN} ≤ 30V	0.06	0.12	**0.2**	mA
Short Circuit Current		27	15 50	**11** **65**	mA min mA max
Noise Voltage	10 Hz to 1 kHz 0.1 Hz to 10 Hz (10 Hz to 10 kHz, C_{filter} = 0.1 μF)	10 4 4	30 — —	— — —	μV rms μV p-p μV rms
Long-term Stability (Non-Cumulative) (Note 10)	1000 hours, $T_j < T_{max}$ (Measured at +25°C)	6	—	—	ppm
Temperature Hysteresis of V_{out}	ΔT = 25°C	3	—	—	ppm
Output Shift per 1 μA at Pin 5		1500	2600	—	ppm

Electrical Characteristics LM369D (Note 1)

Parameter	Conditions	Typical	Tested Limits (Notes 2, 13)	Design Limit (Note 3)	Units (Max Unless Noted)
V_{out} Nominal		+10.000			V
V_{out} Error, LM369D		70 0.7	±1000 ±10.0	— —	ppm mV
V_{out} Tempco (Note 6)	$T_{min} \le T_j \le T_{max}$	5		**30**	ppm/°C
Line Regulation	$13V \le V_{IN} \le 30V$	2.4	±6.0	**12**	ppm/V
Load Regulation Sourcing Sinking (Note 12) (Note 4, Note 9)	 0 to 10 mA 0 to −10 mA	 +3 +80	 ±12 +160	 **±25**	 ppm/mA ppm/mA
Thermal Regulation Sourcing Sinking (Note 12) (Note 5)	(t = 10 msec After Load is Applied)	 4.0 4.0	 ±25 —	 — —	 ppm/100 mW ppm/100 mW
Supply Current		1.5	2.0	**2.4**	mA
ΔSupply Current	$13V \le V_{IN} \le 30V$	0.06	0.16	**0.3**	mA
Short Circuit Current		27	14 50	**10** **65**	mA min mA max
Noise Voltage	10 Hz to 1 kHz 0.1 Hz to 10 Hz (10 Hz to 10 kHz, C_{filter} = 0.1 μF)	10 4 4	30 — —	— — —	μV rms μV p-p μV rms
Long-Term Stability (Non-Cumulative)	1000 Hours, $T_j < T_{max}$ (Measured at +25°C)	8	—	—	ppm
Temperature Hysteresis of V_{out}	ΔT = 25°C	5	—	—	ppm
Output Shift Per 1 μA at Pin 5		1500	2800	—	ppm

Note 1: Unless otherwise noted, these conditions apply: T_j = +25°C, $13V \le V_{in} \le 17V$, $0 \le I_{load} \le 1.0$ mA, C_L = ≤ 200 pF. Specifications in **BOLDFACED TYPE** apply over the rated operating temperature range.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not to be used to calculate outgoing quality levels.

Note 4: The LM169 has a Class B output, and will exhibit transients at the crossover point. This point occurs when the device is required to sink approximately 1.0 mA. In some applications it may be advantageous to pre-load the output to either V_{in} or to ground, to avoid this crossover point.

Note 5: Thermal regulation is defined as the change in the output voltage at a time T after a step change of power dissipation of 100 mW.

Note 6: Temperature Coefficient of V_{OUT} is defined as the worst-case ΔV_{out} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (see graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

Note 7: In metal can (H), $\theta_{J\text{-}C}$ is 75°C/W and $\theta_{J\text{-}A}$ is 150°C/W. In plastic DIP, $\theta_{J\text{-}A}$ is 160°C/W. In S0-8, $\theta_{J\text{-}A}$ is 180°C/W, in TO-226, $\theta_{J\text{-}A}$ is 160°C/W.

Note 8: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not guaranteed beyond the Rated Operating Conditions.

Note 9: Regulation is measured at constant temperature using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for Thermal Regulation and Tempco. Load Regulation is measured at a point on the output pin 1/8" below the bottom of the package.

Note 10: Consult factory for availability of devices with Guaranteed Long-term Stability.

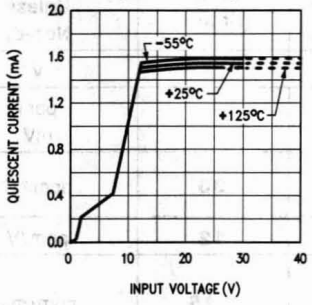
Note 11: Consult factory for availability of devices with tighter Accuracy and Tempco Specifications.

Note 12: In Sinking mode, connect 0.1 μF tantalum capacitor from output to ground.

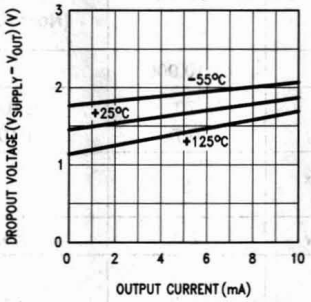
Note 13: A military RETS electrical test specification is available on request.

Typical Performance Characteristics (Note 1)

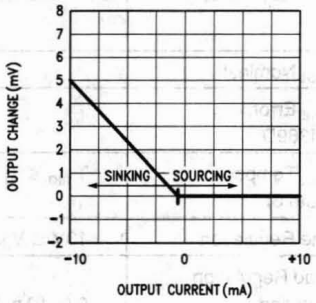
Quiescent Current vs Input Voltage and Temperature



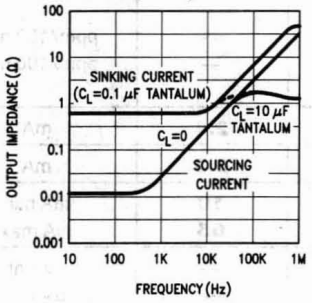
Dropout Voltage vs Output Current (Series Mode Sourcing Current)



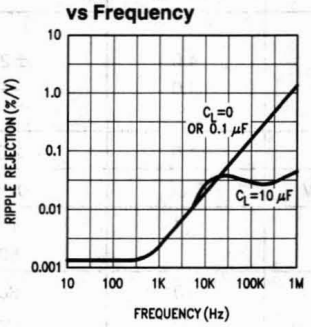
Output Change vs Output Current



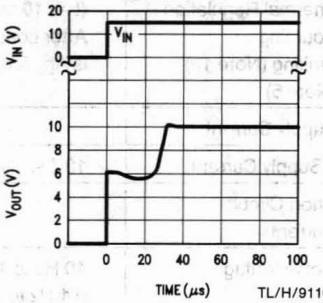
Output Impedance vs Frequency



Ripple Rejection vs Frequency



Start-up Response



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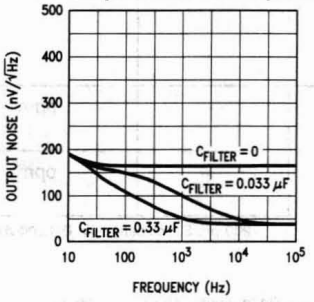
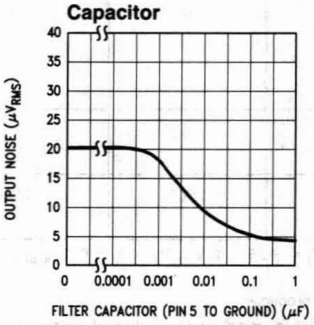
Output Noise vs Frequency



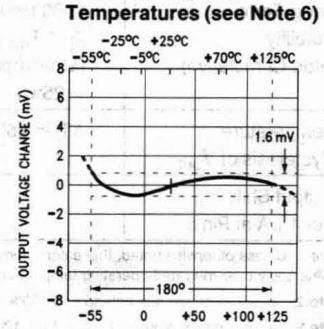
TL/H/9110–24

Output Noise vs Filter Capacitor



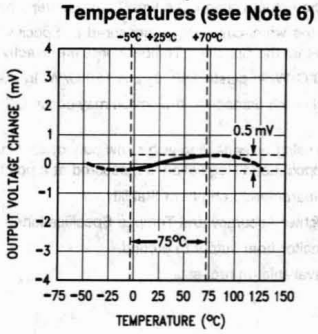
TL/H/9110–25

LM169 Temperature Coefficient Specified Temperatures (see Note 6)



TL/H/9110–26

LM369 Temperature Coefficient Specified Temperatures (see Note 6)



TL/H/9110–27

Typical Temperature Coefficient Calculations:

LM169 (see curve above):
T.C. = 1.6 mV/(180° × 10V)
= 8.9×10^{-7} = 0.89 ppm/°C

LM369 (see curve at left):
T.C. = 0.5 mV/(75° × 10V)
= 6.7×10^{-7} = 0.67 ppm/°C

Application Hints

The LM169/LM369 can be applied in the same way as any other voltage reference. The adjacent Typical Applications Circuits suggest various uses for the LM169/LM369. The LM169 is recommended for applications where the highest stability and lowest noise is required over the full military temperature range. The LM369 is suitable for limited-temperature operation. The curves showing the Noise vs. Capacitance in the Typical Performance Characteristics section show graphically that a modest capacitance of 0.1 to 0.3 microfarads can cut the broadband noise down to a level of only a few microvolts, less than 1 ppm of the output voltage. The capacitor used should be a low-leakage type. For the temperature range 0 to 50°C, polyester or Mylar® will be suitable, but at higher temperatures, a premium film capacitor such as polypropylene is recommended. For operation at +125°C, a Teflon® capacitor would be required, to ensure sufficiently low leakage. Ceramic capacitors may seem to do the job, but are not recommended for production use, as the high-K ceramics cannot be guaranteed for low leakage, and may exhibit piezo-electric effects, converting vibration or mechanical stress into excessive electrical noise.

Additionally, the inherent superiority of the LM169/369's buried Zener diode provides freedom from low-frequency noise, wobble, and jitter, in the frequency range 0.01 to 10 Hertz, where capacitive filtering is not feasible.

Pins 1, 3, 7, and 8 of the LM169/369 are connected to internal trim circuits which are used to trim the device's output voltage and Tempco during final testing at the factory. Do not connect anything to these pins, or improper operation may result. These pins would not be damaged by a short to ground, or by Electrostatic Discharges; however, keep them away from large transients or AC signals, as stray capacitance could couple noises into the output. These pins may be cut off if desired. Alternatively, a shield foil can be laid out on the printed circuit board, surrounding these pins and pin 5, and this guard foil can be connected to ground or to V_{out}, effectively acting as a guard against AC coupling and DC leakages.

The trim pin (pin 5) should also be guarded away from noise signals and leakages, as it has a sensitivity of 15 millivolts of ΔV_{out} per microampere. The trim pin can also be used in the circuits shown, to provide an output trim range of ±10 millivolts. Trimming to a wider range is possible, but is not recommended as it may degrade the Tempco and the Tempco linearity at temperature extremes. For example, if the output were trimmed up to 10.240V, the Tempco would be degraded by 8 ppm/°C. As a general rule, Tempco will be degraded by 1 ppm/°C per 30 mV of output adjustment.

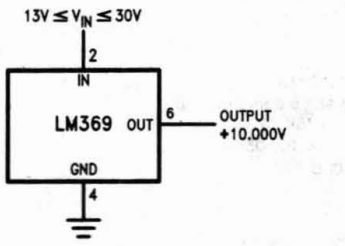
The output can sink current as well as source it, but the output impedance is much better for sourcing current. Also, the LM169/369 requires a 0.1 μF tantalum capacitor (or, 0.1 μF in series with 10Ω) bypass from the output to ground, for stable operation in shunt mode (output sinking current). The output has a class-B stage, so if the load current changes from sourcing to sinking, an output transient will occur. To avoid this transient, it may be advisable to preload the output with a few milliamperes of load to ground. The LM169/369 does have an excellent tolerance of load capacitance, and in cases of load transients, electrolytic or tantalum capacitors in the range 1 to 500 microfarads have been shown to improve the output impedance without degrading the dynamic stability of the device. The LM169/369 are rated to drive an output of ±10 mA, but for best accuracy, any load current larger than 1 mA can cause thermal errors (such as, 1 mA × 5V × 4 ppm/100 mW = 0.2 ppm or 2 microvolts) and degrade the ultimate precision of the output voltage.

The output is short-circuit-proof to ground. However, avoid overloads at high ambient temperatures, as a prolonged short-circuit may cause the junction temperature to exceed the Absolute Maximum Temperature. The device does not include a thermal shut-down circuit. If the output is pulled to a positive voltage such as +15 or +20V, the output current will be limited, but overheating may occur. Avoid such overloads for voltages higher than +20 V, for more than 5 seconds, or, at high ambient temperatures.

The LM169/369 has an excellent long-term stability, and is suitable for use in high-resolution Digital Voltmeters or Data Acquisition systems. Its long-term stability is typically 3 to 10 ppm per 1000 hours when held near T_{max}, and slightly better when operated at room temperature. Contact the factory for availability of devices with proven long-term stability.

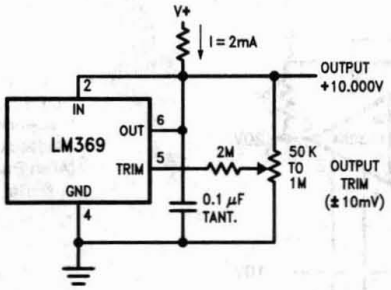
Typical Applications

Series Reference



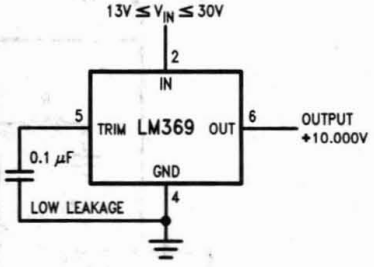
TL/H/9110–2

Shunt Reference with Optional Trim



TL/H/9110–3

Series Reference with Optional Filter for Reduced Noise

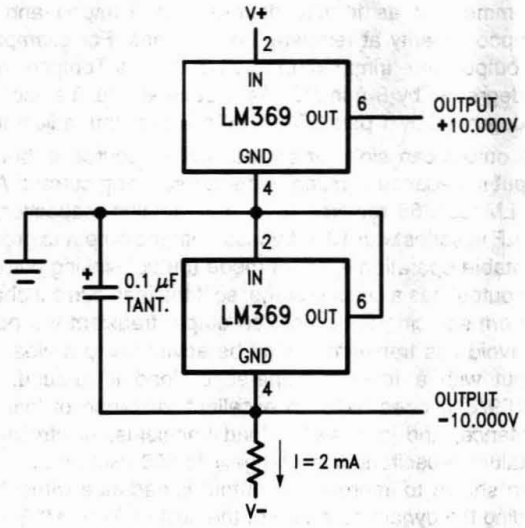


TL/H/9110–4

NOTE: Pin numbers for H, M or N packages.

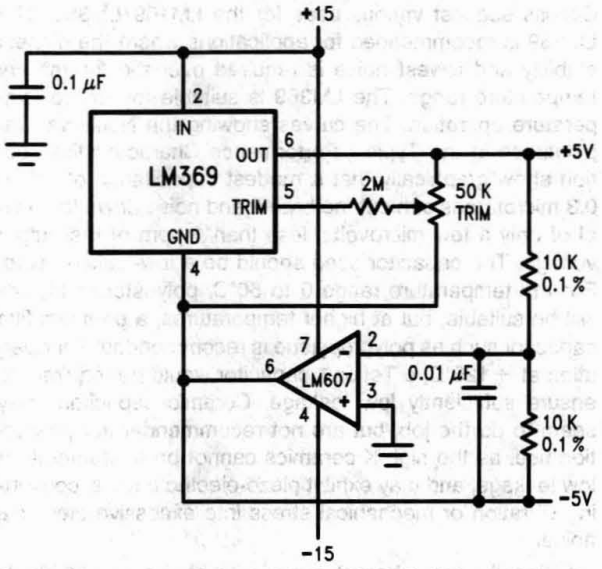
Typical Applications (Continued)

±10V Reference



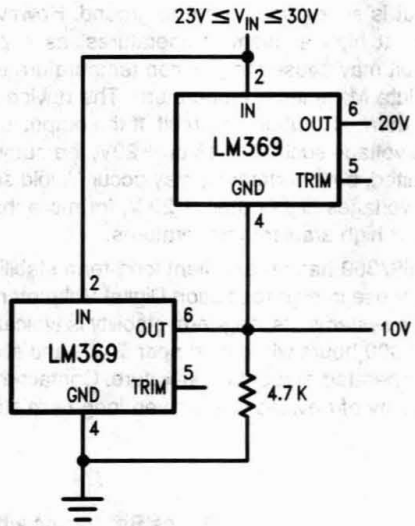
TL/H/9110–7

±5V Reference

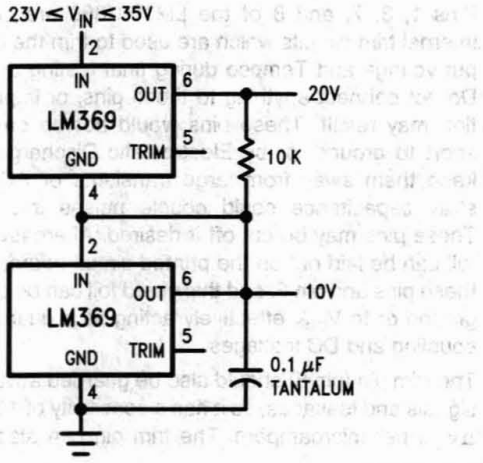


TL/H/9110–8

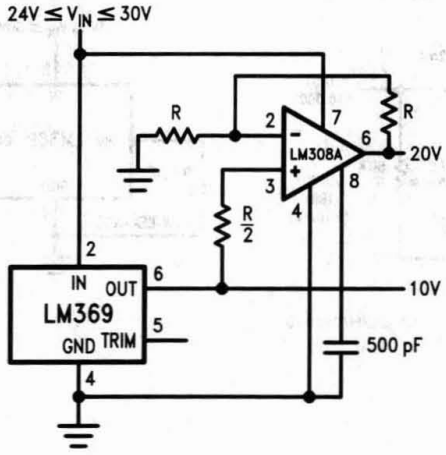
Multiple Output Voltages



TL/H/9110–9



TL/H/9110–10



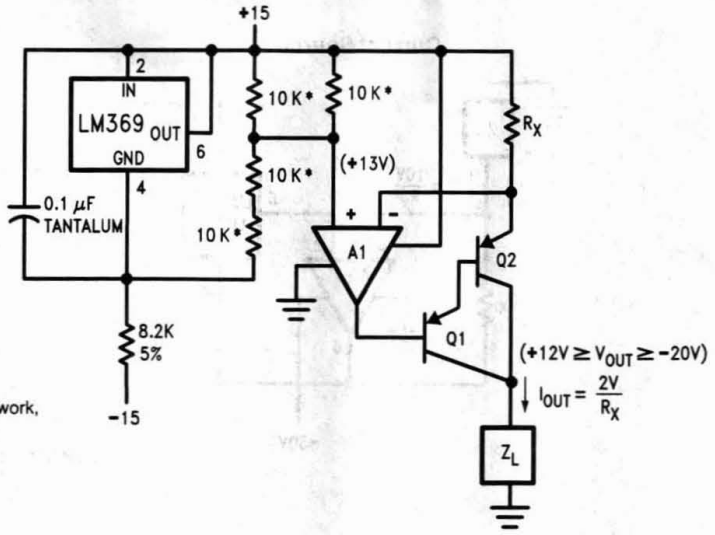
TL/H/9110–11

R = Thin Film Resistor Network
0.05% Matching and 5 ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
(Allen Bradley F08B103A)
or similar.

NOTE: Pin numbers for H, M or N packages.

Typical Applications (Continued)

Precision Wide-Range Current Source



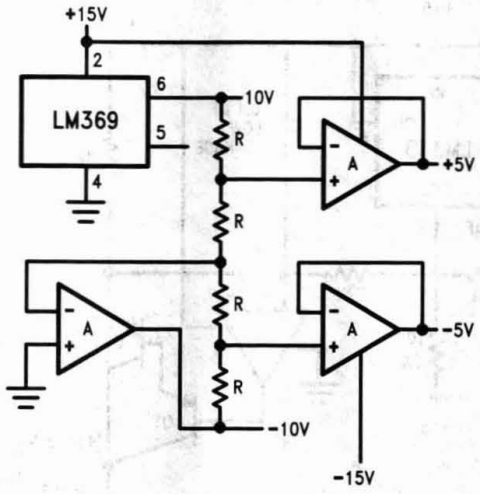
A_1 = LF411A, LM607, LM308A or similar

Q_1, Q_2 = high β PNP, PN4250, 2N3906, or similar

* = Part of Precision Resistor Network, ±0.05% Matching, (Allen Bradley F08B103A) (Caddock T-914-10K-100-05) (Beckman 694-3-R-10K-A) or similar

TL/H/9110–18

±10V, ±5V References

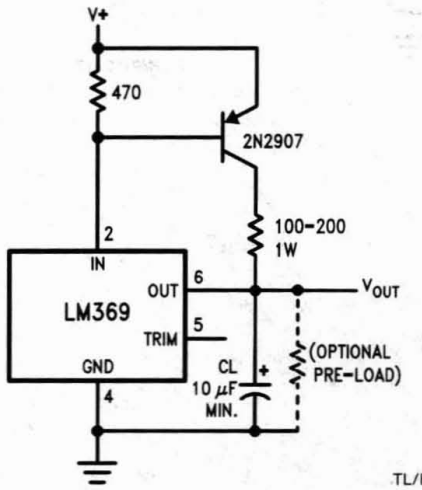


A = ¼ LF444A or ½ LF412A or LM607

R = Thin Film Resistor Network 0.05% Matching and 5 ppm Tracking (Beckman 694-3-R-10K-A), (Caddock T-914-10K-100-05) (Allen Bradley F08B103A) or similar.

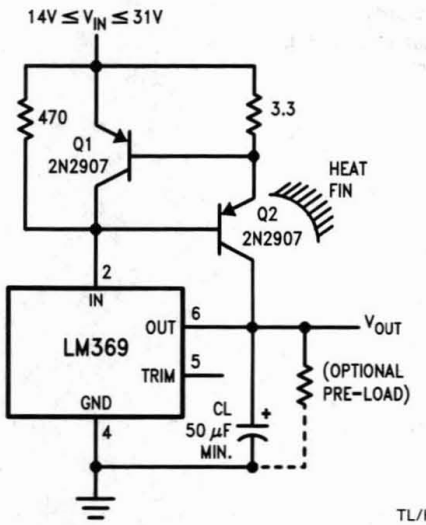
TL/H/9110–12

Reference with Booster



TL/H/9110–13

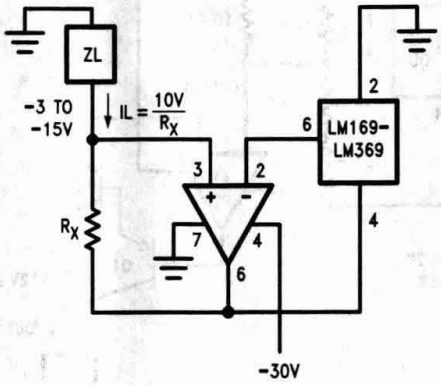
100 mA Boosted Reference



TL/H/9110–14

Typical Applications (Continued)

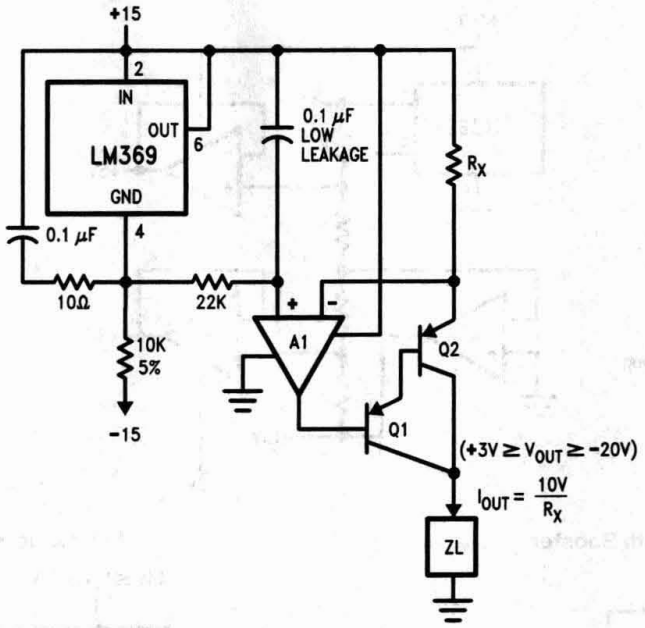
Current Source



$2k \leq Rx \leq 10M$

TL/H/9110-16

Precision Current Source



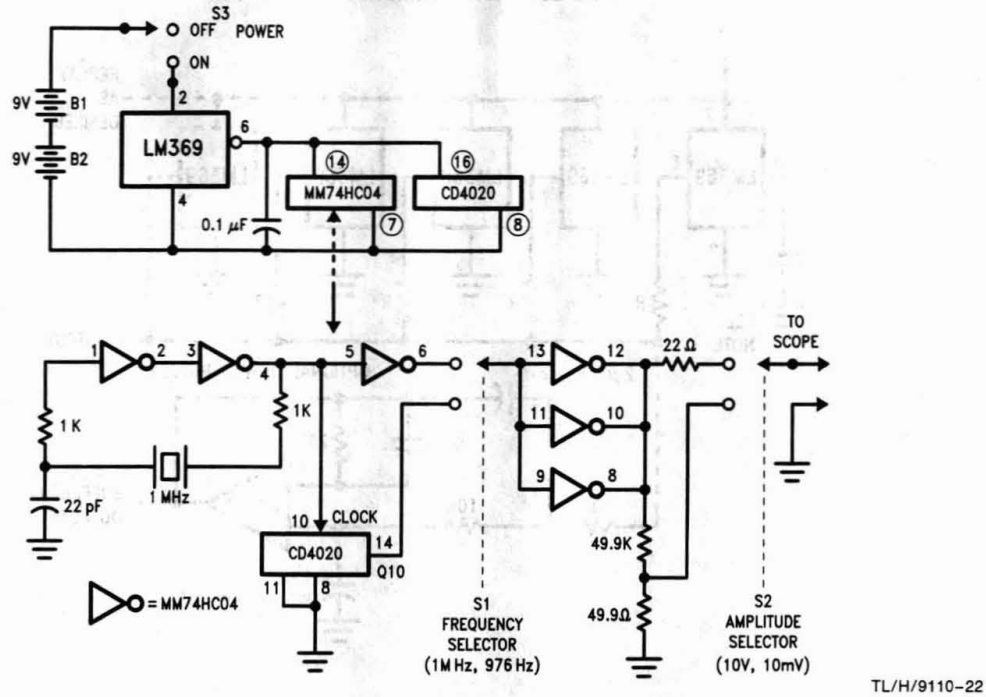
Q_1, Q_2 = high β PNP, PN4250, 2N3906 or similar

A_1 = LM607, LM11, LF411A or similar

TL/H/9110-17

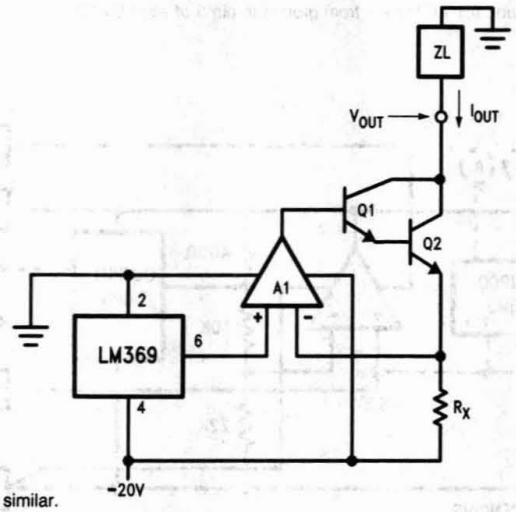
Typical Applications (Continued)

Oscilloscope Calibrator



TL/H/9110–22

Precision Wide-Range Current Sink

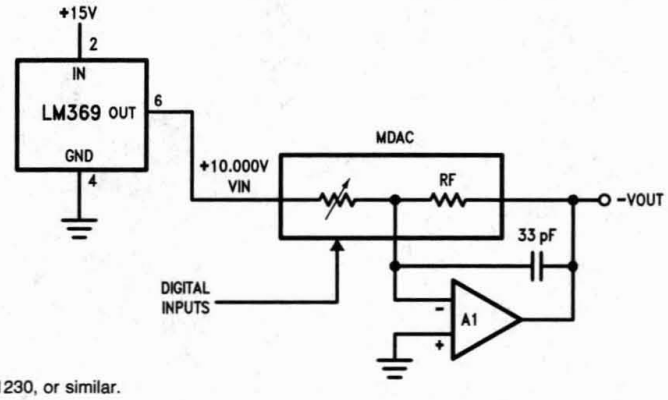


$I_{out} = \frac{10V}{Rx}$

A_1 = LM11, LM607 or similar.
$(V3 + 2V) \leq V_{out} \leq +20V$.
Q1, Q2 = high Beta NPN, 2N3707, 2N3904 or similar.

TL/H/9110–19

Digitally Variable Supply

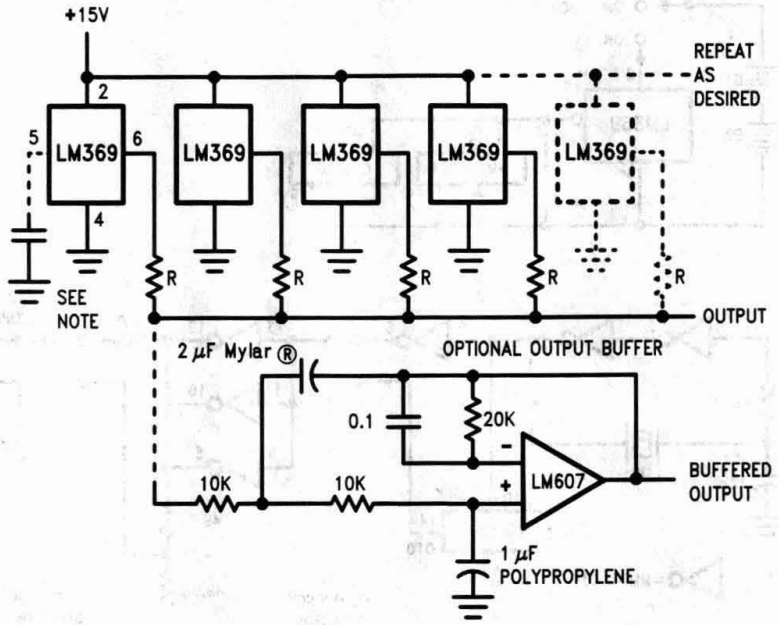


$V_{out} = -10V \times$ (Digitally Set Gain).
A_1 = LM11A, LM607, or similar.
MDAC = DAC1220, DAC1208, DAC1230, or similar.

TL/H/9110–20

Typical Applications (Continued)

Ultra-Low-Noise Statistical Reference



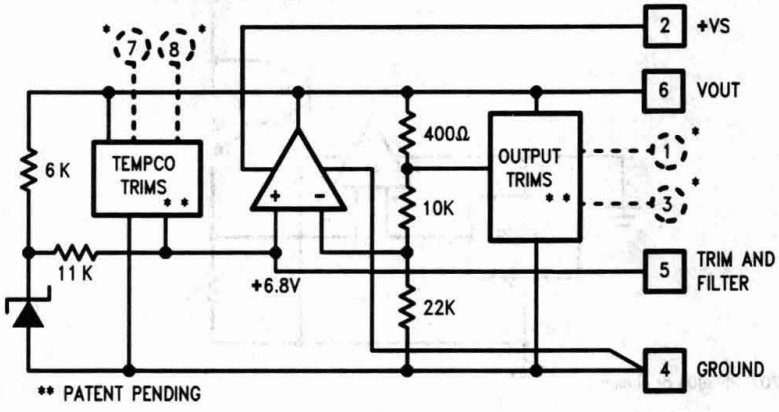
TL/H/9110–23

$200\Omega \leq R \leq 1k$

When N pieces of LM369 are used, the V_{out} noise is decreased by a factor of $\frac{1}{\sqrt{N}}$

If the output buffer is not used, for lowest noise add 0.1 μF Mylar® from ground to pin 5 of each LM369.

LM169 Block Diagram



TL/H/9110–15

*Do not connect; internal connection for factory trim.

National Semiconductor

LM185/LM285/LM385
Adjustable Micropower Voltage References

General Description

The LM185/LM285/LM385 are micropower 3-terminal adjustable band-gap voltage reference diodes. Operating from 1.24 to 5.3V and over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185 band-gap reference uses only transistors and resistors, low noise and good long-term stability result.

Careful design of the LM185 has made the device tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

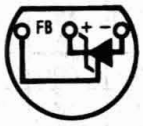
The LM185 is rated for operation over a −55°C to 125°C temperature range, while the LM285 is rated −40°C to 85°C and the LM385 0°C to 70°C. The LM185 is available in a hermetic TO-46 package and a leadless chip carrier package, while the LM285/LM385 are available in a low-cost TO-92 molded package, as well as S.O.

Features

- Adjustable from 1.24V to 5.30V
- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1 Ω dynamic impedance
- Low temperature coefficient

Connection Diagrams

TO-92
Plastic Package



TL/H/5250–9

Bottom View

Order Number LM285BXZ, LM285BYZ, LM285Z, LM385BXZ, LM385BYZ, LM385BZ or LM385Z
See NS Package Number Z03A

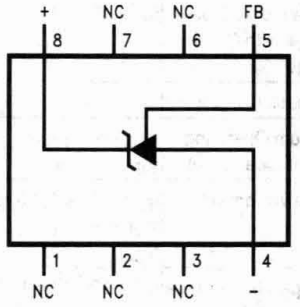
TO-46
Metal Can Package

TL/H/5250–1

Bottom View

Order Number LM185BH, LM185BH/883, LM185BYH or LM185BYH/883
See NS Package Number H03H

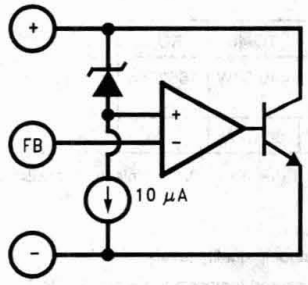
SO Package



TL/H/5250–10

Order Number LM285M, LM285BYM, LM385BM or LM385M
See NS Package Number M08A

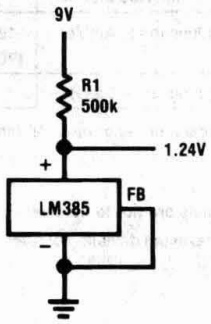
Block Diagram



TL/H/5250–13

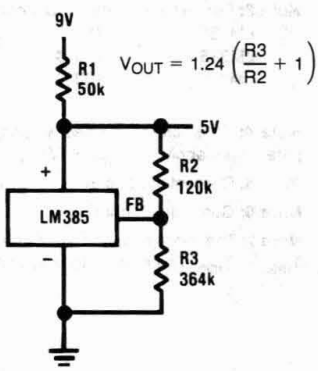
Typical Applications

1.2V Reference



TL/H/5250–14

5.0V Reference



TL/H/5250–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range (Note 3)	
LM185 Series	−55°C to 125°C
LM285 Series	−40°C to 85°C
LM385 Series	0°C to 70°C
Storage Temperature	−55°C to 150°C

Soldering Information

TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM185, LM285					LM385					Units (Limit)
		Typ	LM185BX, LM185BY LM185B, LM285BX, LM285BY		LM285		Typ	LM385BX, LM385BY		LM385		
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)		Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reference Voltage	I_R = 100 μA	1.240	1.252 **1.255** 1.228 **1.215**		1.265 1.215	**1.270** **1.205**	1.240	1.252 1.228	**1.255** **1.215**	1.265 1.215	**1.270** **1.205**	V (max) V (min)
Reference Voltage Change with Current	$I_{MIN} < I_R < 1$ mA 1 mA < I_R < 20 mA	0.2 4	1 10	**1.5** **20**	1 10	**1.5** **20**	0.2 5	1 15	**1.5** **25**	1 15	**1.5** **25**	mV (max)
Dynamic Output Impedance	I_R = 100 μA, f = 100 Hz I_{AC} = 0.1 I_R $V_{OUT} = V_{REF}$ V_{OUT} = 5.3V	 0.3 0.7					 0.4 1					Ω
Reference Voltage Change with Output Voltage	I_R = 100 μA	1	3	**6**	3	**6**	2	5	**10**	5	**10**	mV (max)
Feedback Current		13	20	**25**	20	**25**	16	30	**35**	30	**35**	nA (max)
Minimum Operating Current (see curve)	$V_{OUT} = V_{REF}$ V_{OUT} = 5.3V	6 30	9 45	**10** **50**	9 45	**10** **50**	7 35	11 55	**13** **60**	11 55	**13** **60**	μA (max)
Output Wideband Noise	I_R = 100 μA, 10 Hz < f < 10 kHz $V_{OUT} = V_{REF}$ V_{OUT} = 5.3V	 50 170					 50 170					μV_{rms}
Average Temperature Coefficient (Note 7)	I_R = 100 μA X Suffix Y Suffix All Others		**30** **50**	 **150**	**30** **50**	 **150**		**30** **50**	 **150**	**30** **50**	 **150**	ppm/°c (max)
Long Term Stability	I_R = 100 μA, T = 1000 Hr, T_A = 25°C ± 0.1°C	20					20					ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS185H for military specifications.

Note 3: For elevated temperature operation, T_j max is:

LM185	150°C
LM285	125°C
LM385	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4″ leads) 170°C/W (0.125″ leads)	440°C/W	165°C/W
θ_{jc} (Junction to Case)	N/A	80°C/W	N/A

Note 4: Parameters identified with **boldface type** apply at temperature extremes. All other numbers apply at $T_A = T_J$ = 25°C. Unless otherwise specified, all parameters apply for $V_{REF} < V_{OUT} < 5.3V$.

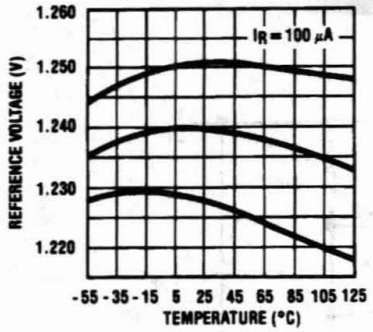
Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed, but not 100% production tested. These limits are not to be used to calculate average outgoing quality levels.

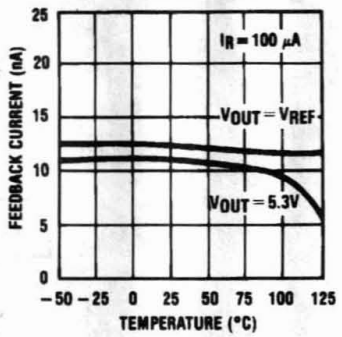
Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures from T_{min} to T_{max}, divided by $T_{max} - T_{min}$. The measured temperatures are −55, −40, 0, 25, 70, 85, 125°C.

Typical Performance Characteristics

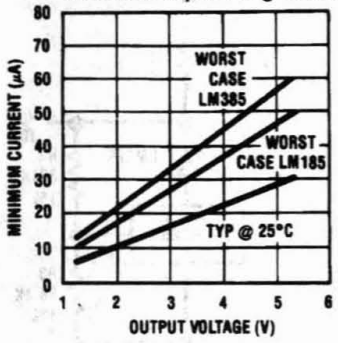
Temperature Drift of 3 Representative Units



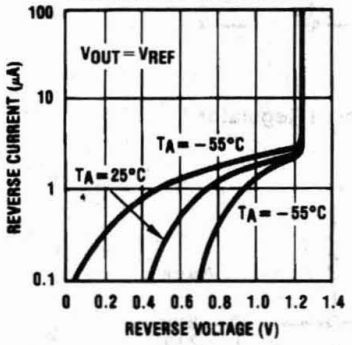
Feedback Current



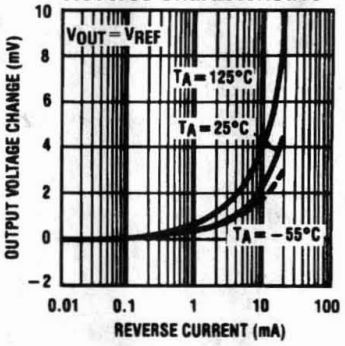
Minimum Operating Current



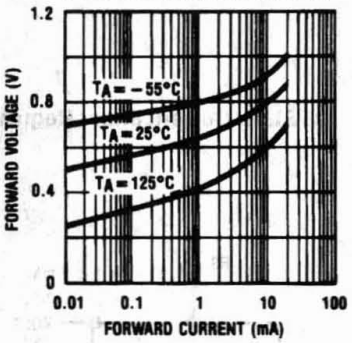
Reverse Characteristics



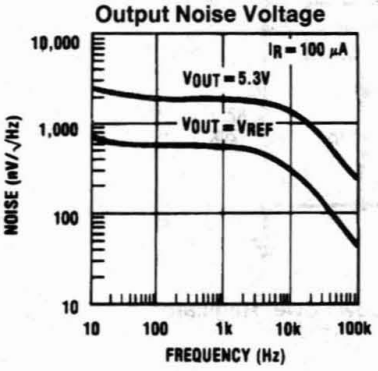
Reverse Characteristics



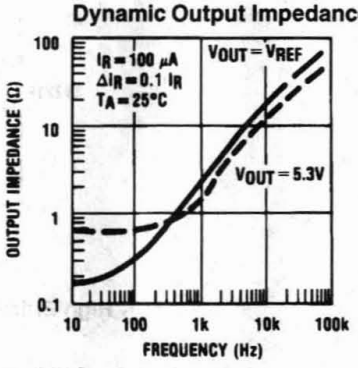
Forward Characteristics



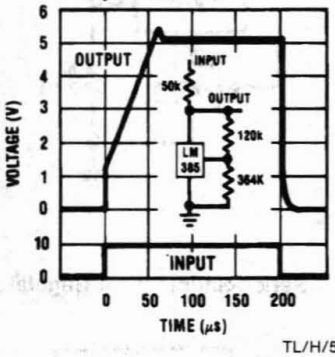
Output Noise Voltage



Dynamic Output Impedance

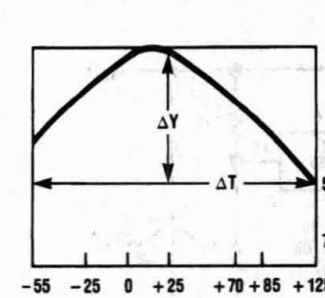


Response Time

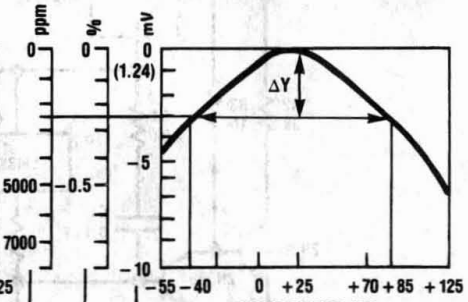


TL/H/5250–3

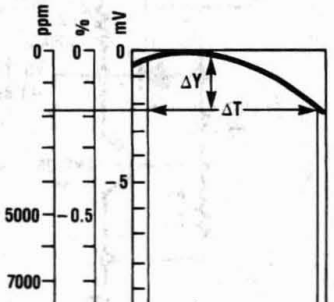
LM185
Temperature Coefficient Typical

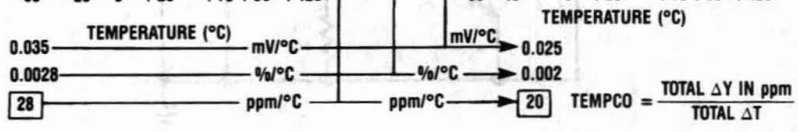


LM285
Temperature Coefficient Typical



LM385
Temperature Coefficient Typical



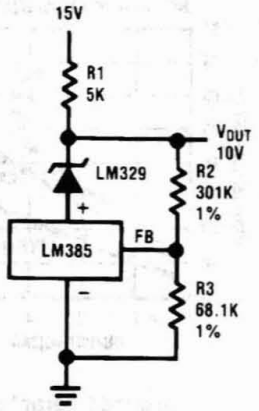


TL/H/5250–4

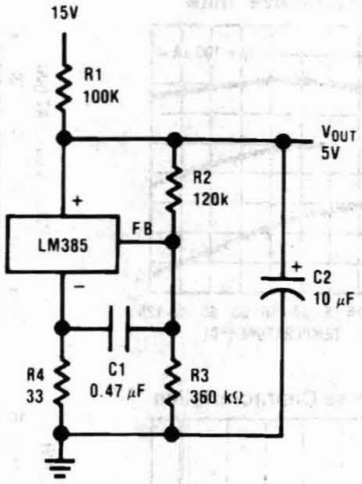
4

Typical Applications (Continued)

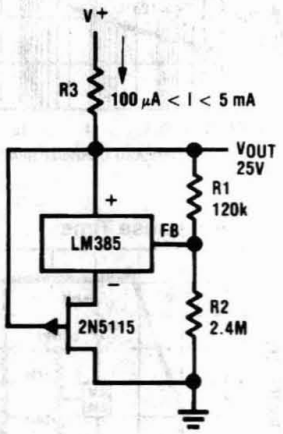
Precision 10V Reference



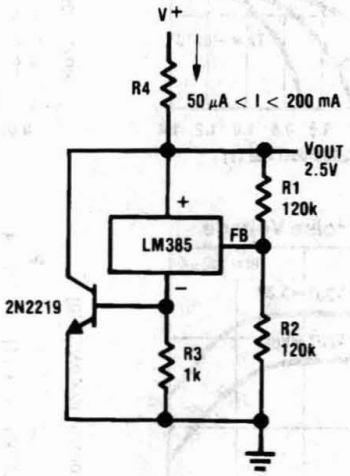
Low AC Noise Reference



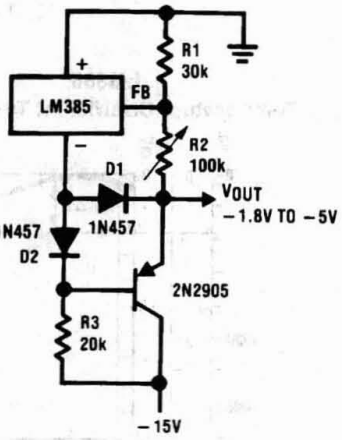
25V Low Current Shunt Regulator



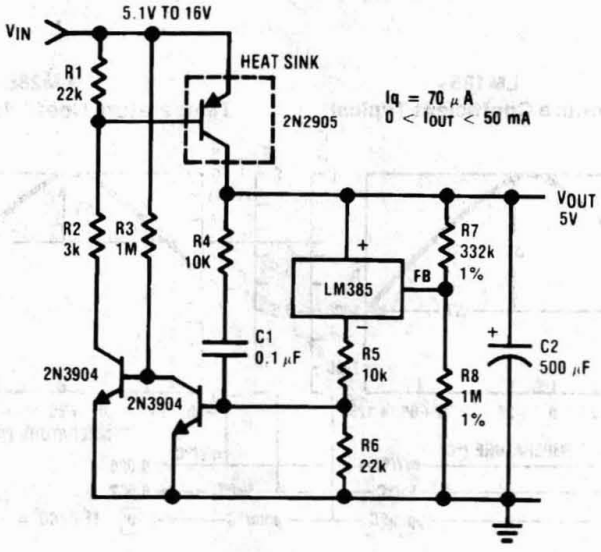
200 mA Shunt Regulator



Series-Shunt 20 mA Regulator



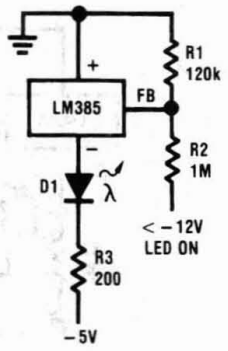
High Efficiency Low Power Regulator



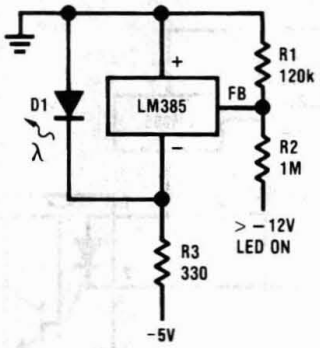
TL/H/5250–5

Typical Applications (Continued)

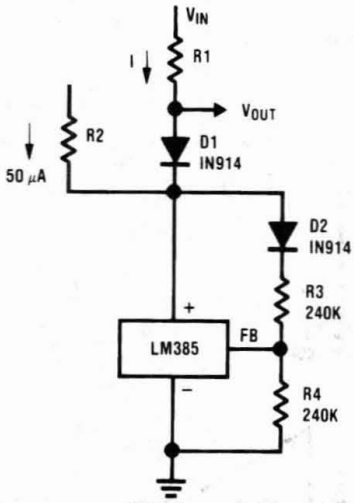
Voltage Level Detector



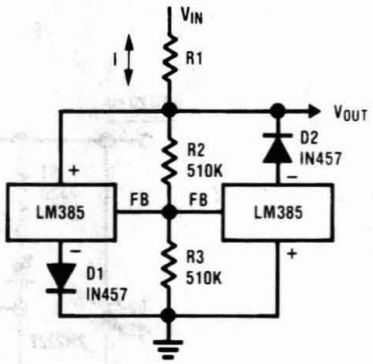
Voltage Level Detector



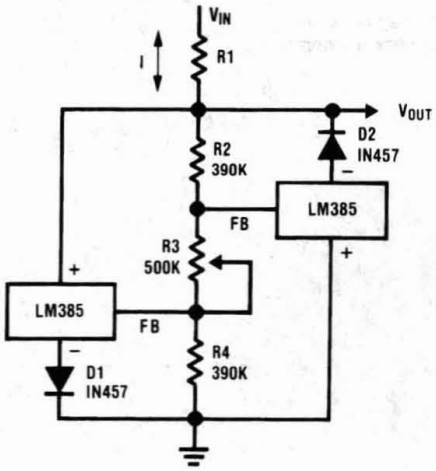
Fast Positive Clamp
$2.4V + \Delta V_{D1}$



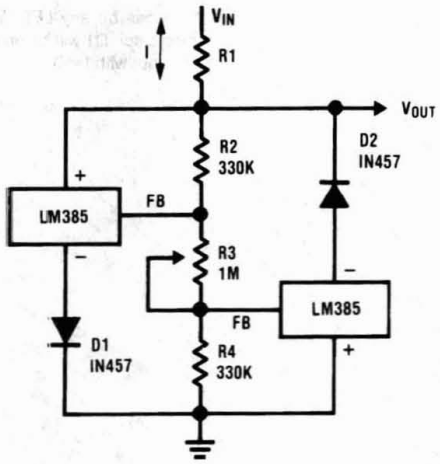
Bidirectional Clamp
±2.4V



Bidirectional Adjustable Clamp
±1.8V to ±2.4V



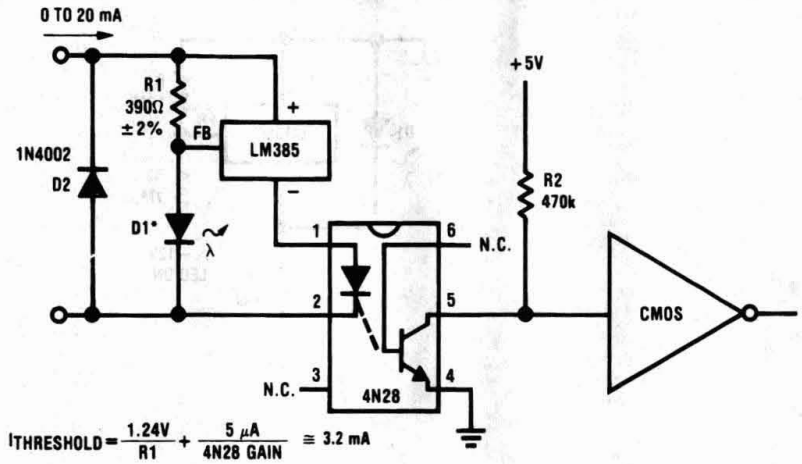
Bidirectional Adjustable Clamp
±2.4V to ±6V



TL/H/5250–6

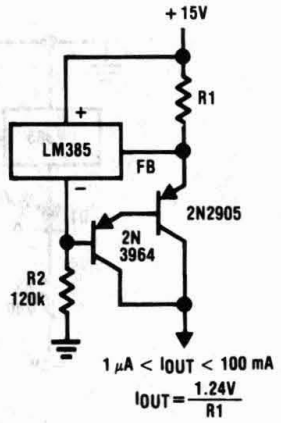
Typical Applications (Continued)

Simple Floating Current Detector



$$I_{THRESHOLD} = \frac{1.24V}{R1} + \frac{5\ \mu A}{4N28\ GAIN} \cong 3.2\ mA$$

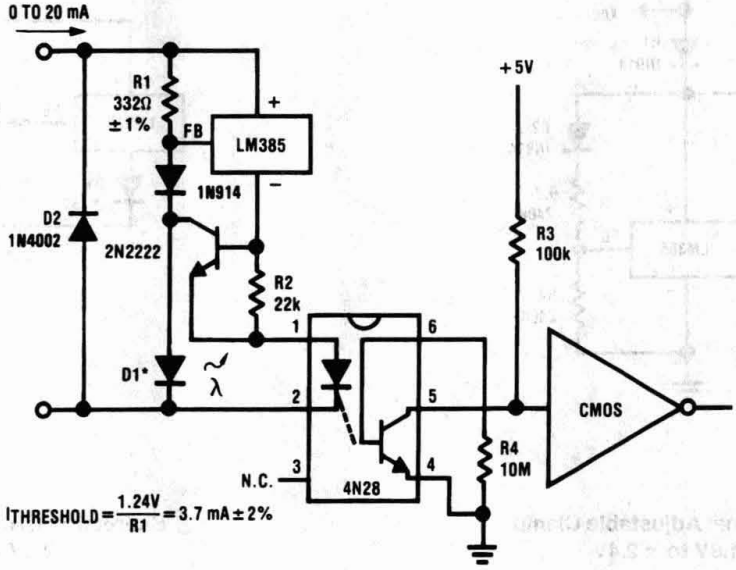
Current Source



$$1\ \mu A < I_{OUT} < 100\ mA$$

$$I_{OUT} = \frac{1.24V}{R1}$$

Precision Floating Current Detector



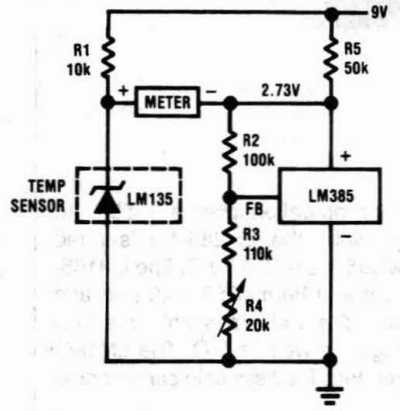
$$I_{THRESHOLD} = \frac{1.24V}{R1} = 3.7\ mA \pm 2\%$$

TL/H/5250–7

* D1 can be any LED, $V_F = 1.5V$ to 2.2V at 3 mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

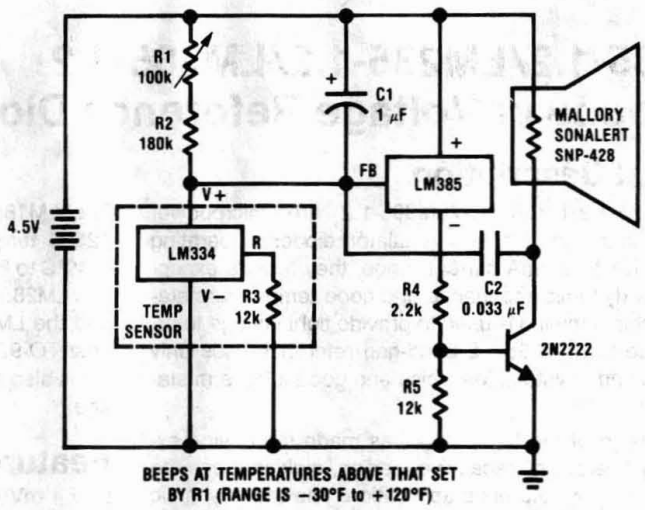
Typical Applications (Continued)

Centigrade Thermometer, 10 mV/°C



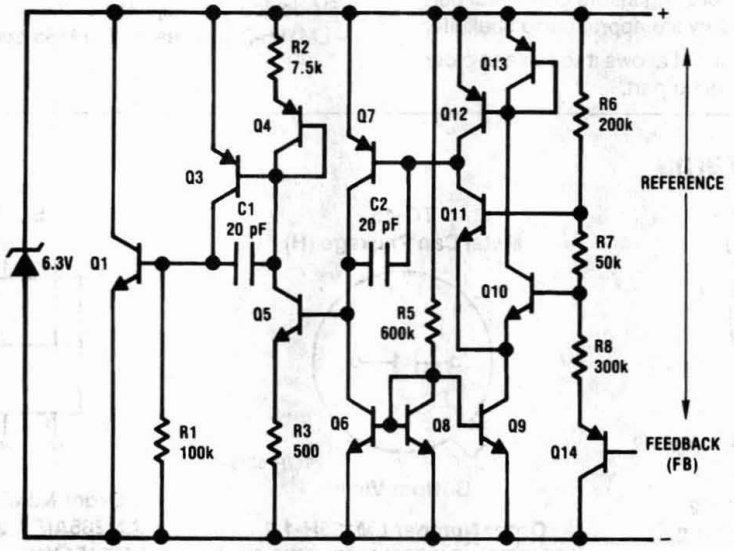
TL/H/5250–11

Freezer Alarm



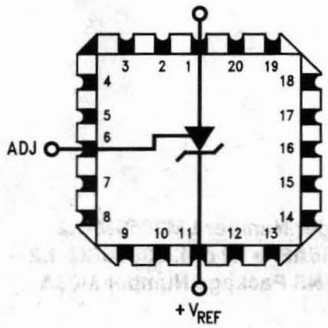
TL/H/5250–12

Schematic Diagram



TL/H/5250–8

Connection Diagrams (Continued)



TL/H/5250–15

Order Number LM185BE/883
See NS Package Number E20A

National Semiconductor

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life.

Further, the wide operating current allows it to replace older references with a tighter tolerance part.

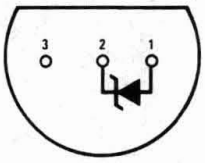
The LM185-1.2 is rated for operation over a −55°C to 125°C temperature range while the LM285-1.2 is rated −40°C to 85°C and the LM385-1.2 0°C to 70°C. The LM185-1.2/LM285-1.2 are available in a hermetic TO-46 package and the LM285-1.2/LM385-1.2 are also available in a low-cost TO-92 molded package, as well as S.O. The LM185-1.2 is also available in a hermetic leadless chip carrier package.

Features

- ±4 mV (±0.3%) max. initial tolerance (A grade)
- Operating current of 10 μA to 20 mA
- 0.6Ω max dynamic impedance (A grade)
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device and adjustable device also available — LM185-2.5 series and LM185 series, respectively

Connection Diagrams

TO-92
Plastic Package (Z)

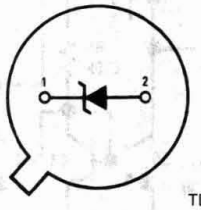


TL/H/5518–10

Bottom View

Order Number LM285Z-1.2, LM285AZ-1.2, LM285AXZ-1.2, LM285AYZ-1.2, LM285BXZ-1.2, LM285BYZ-1.2, LM385Z-1.2, LM385AZ-1.2, LM385AXZ-1.2, LM385AYZ-1.2, LM385BZ-1.2, LM385BXZ-1.2 or LM385BYZ-1.2
See NS Package Number Z03A

TO-46
Metal Can Package (H)

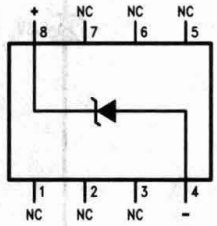


TL/H/5518–6

Bottom View

Order Number LM185H-1.2, LM185H-1.2/883, LM185BXH-1.2, LM185BYH-1.2/883, LM285H-1.2, LM285BXH-1.2 or LM285BYH-1.2
See NS Package Number H02A

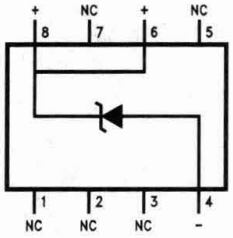
SO Package



TL/H/5518–9

Order Number LM285M-1.2, LM285AM-1.2, LM285AXM-1.2, LM285AYM-1.2, LM285BXM-1.2, LM285BYM-1.2, LM385M-1.2, LM385AM-1.2, LM385AXM-1.2, LM385AYM-1.2, LM385BM-1.2, LM385BXM-1.2 or LM385BYM-1.2
See NS Package Number M08A

SO Package
Alternate Pinout

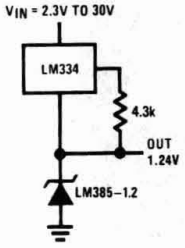


TL/H/5518–11

Order Number LM385SM-1.2, LM385ASM-1.2 or LM385BSM-1.2
See NS Package Number M08A

Typical Application

Wide Input Range Reference



TL/H/5518–8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 2)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range (Note 3)	
LM185-1.2	−55°C to +125°C
LM285-1.2	−40°C to +85°C
LM385-1.2	0°C to 70°C
Storage Temperature	−55°C to +150°C
Soldering Information	
TO-92 package: 10 sec.	260°C
TO-46 package: 10 sec.	300°C
SO package: Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM285A-1.2 LM285AX-1.2 LM285AY-1.2			LM385A-1.2 LM385AX-1.2 LM385AY-1.2			Units (Limit)
		Typ	Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	I_R = 100 μA	1.235 **1.230**	1.231 1.239	 **1.220** **1.245**	1.235 **1.235**	1.231 1.239	 **1.225** **1.245**	V(Min) V(Max) V(Min) V(Max)
Minimum Operating Current		7	8	**10**	7	8	**10**	μA (Max)
Reverse Breakdown Voltage Change with Current	$I_{MIN} \le I_R \le 1$ mA		1	**1.5**		1	**1.5**	mV (Max)
	1 mA ≤ I_R ≤ 20 mA		10	**20**		10	**20**	mV (Max)
Reverse Dynamic Impedance	I_R = 100 μA, f = 20 Hz	0.2		0.6 **1.5**	0.2		0.6 **1.5**	Ω (Max)
Wideband Noise (rms)	I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	60			60			μV
Long Term Stability	I_R = 100 μA, T = 1000 Hr, T_A = 25°C ±0.1°C	20			20			ppm
Average Temperature Coefficient (Note 7)	$I_{MIN} \le I_R \le 20$ mA X Suffix Y Suffix All Others		 **30** **50**	 **150**		 **30** **50**	 **150**	ppm/°C (Max)

4

Electrical Characteristics (Continued) (Note 4)

Parameter	Conditions	Typ	LM185-1.2 LM185BX-1.2 LM185BY-1.2 LM285-1.2 LM285BX-1.2 LM285BY-1.2		LM385B-1.2 LM385BX-1.2 LM385BY-1.2		LM385-1.2		Units (Limit)
			Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	$T_A = 25°C$, $10\ \mu A \le I_R \le 20\ mA$	1.235	1.223 1.247		1.223 1.247		1.205 1.260		V(Min) V(Max)
Minimum Operating Current		8	10	**20**	15	**20**	15	**20**	μA (Max)
Reverse Breakdown Voltage Change with Current	$10\ \mu A \le I_R \le 1\ mA$		1	**1.5**	1	**1.5**	1	**1.5**	mV (Max)
	$1\ mA \le I_R \le 20\ mA$		10	**20**	20	**25**	20	**25**	mV (Max)
Reverse Dynamic Impedance	$I_R = 100\ \mu A$, f = 20 Hz	1							Ω
Wideband Noise (rms)	$I_R = 100\ \mu A$, 10 Hz ≤ f ≤ 10 kHz	60							μV
Long Term Stability	$I_R = 100\ \mu A$, T = 1000 Hr, $T_A = 25°C \pm 0.1°C$	20							ppm
Average Temperature Coefficient (Note 7)	$I_R = 100\ \mu A$ X Suffix Y Suffix All Others		 **30** **50**	 **150**	 **30** **50**	 **150**	 	 **150**	 ppm/°C ppm/°C ppm/°C (Max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS185H-1.2 for military specifications.

Note 3: For elevated temperature operation, T_j max is:

LM185	150°C
LM285	125°C
LM385	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{JA} (junction to ambient)	180°C/W (0.4" leads) 170°C/W (0.125" leads)	440°C/W	165°C/W
θ_{JC} (junction to case)	N/A	80°C/W	N/A

Note 4: Parameters identified with **boldface type** apply at temperature extremes. All other numbers apply at $T_A = T_J = 25°C$.

Note 5: Guaranteed and 100% production tested.

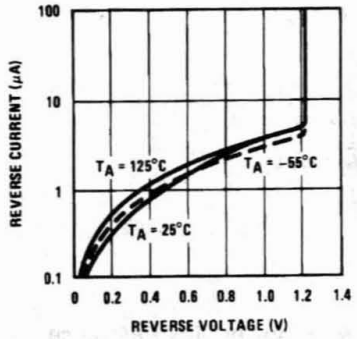
Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate average outgoing quality levels.

Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX} - T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

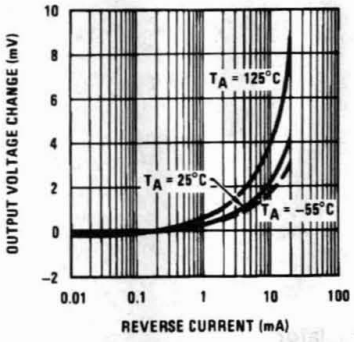
Note 8: A military RETS electrical specification is available on request.

Typical Performance Characteristics

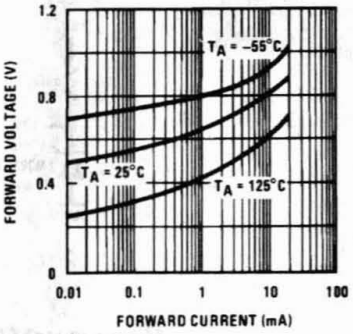
Reverse Characteristics



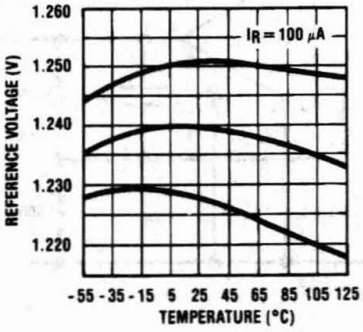
Reverse Characteristics



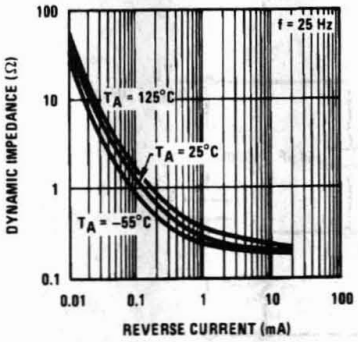
Forward Characteristics



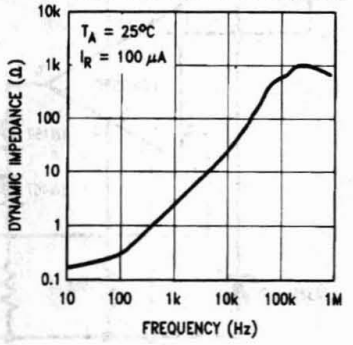
Temperature Drift of 3 Representative Units



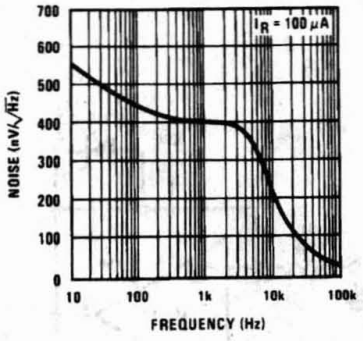
Reverse Dynamic Impedance



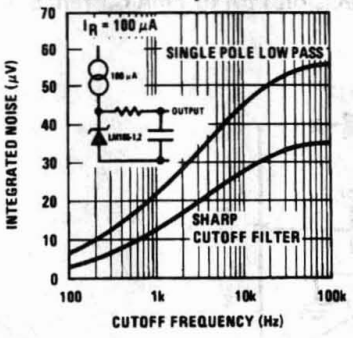
Reverse Dynamic Impedance



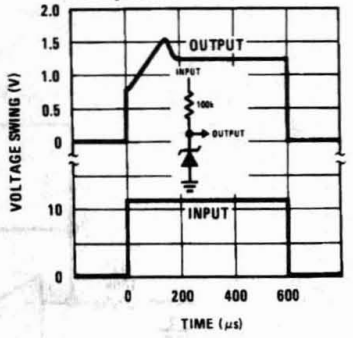
Noise Voltage



Filtered Output Noise



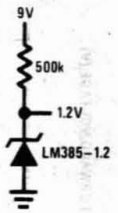
Response Time



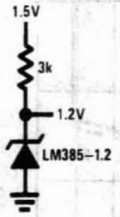
TL/H/5518–3

Typical Applications (Continued)

Micropower Reference from 9V Battery

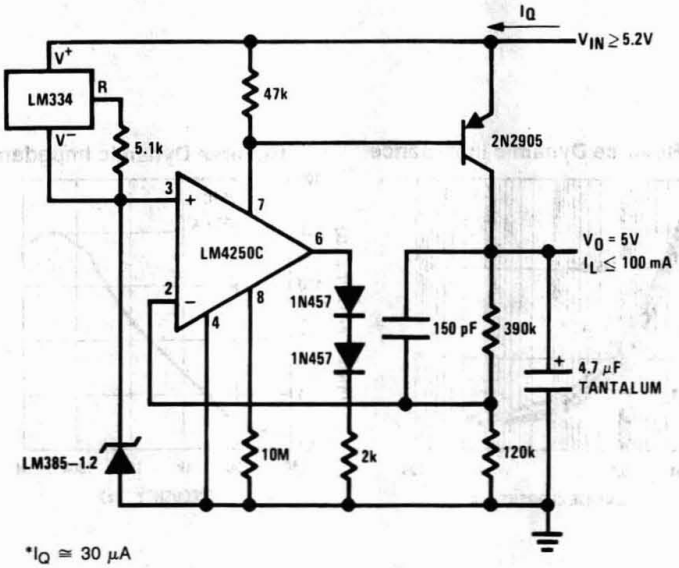


Reference from 1.5V Battery



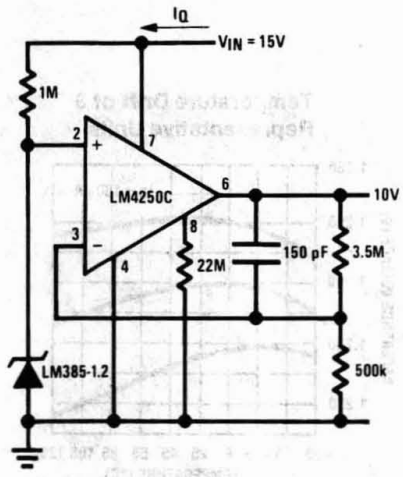
TL/H/5518–2

Micropower* 5V Regulator



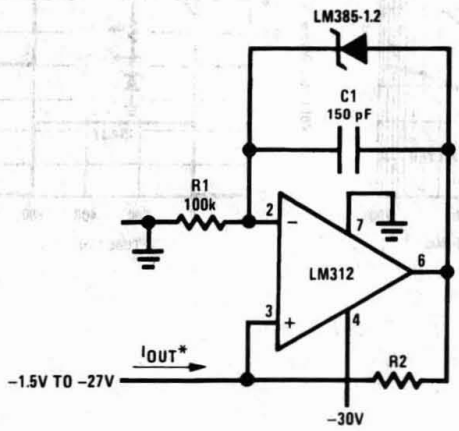
*$I_Q \cong 30\ \mu A$

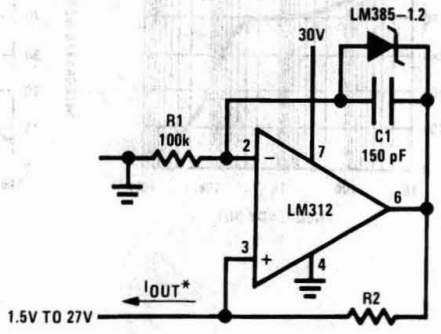
Micropower* 10V Reference



*$I_Q \cong 20\ \mu A$ standby current

Precision 1 μA to 1 mA Current Sources





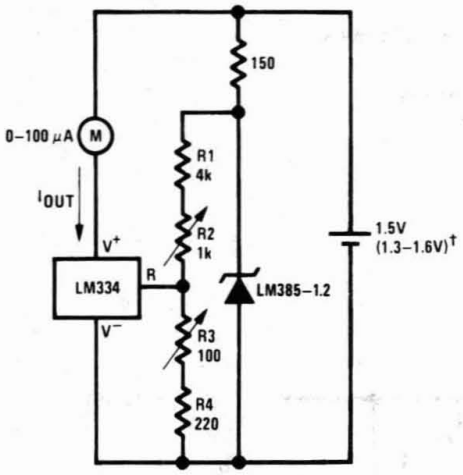
$$*I_{OUT} = \frac{1.23V}{R2}$$

TL/H/5518–4

Typical Applications (Continued)

METER THERMOMETERS

0°C – 100°C Thermometer



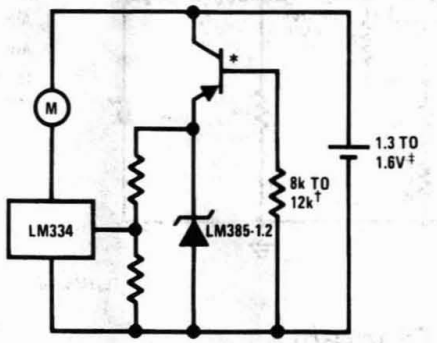
Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

†I_Q at 1.3V ≅ 500 μA

I_Q at 1.6V ≅ 2.4 mA

Lower Power Thermometer

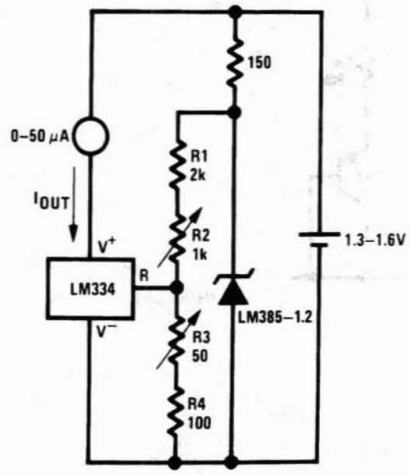


* 2N3638 or 2N2907 select for inverse H_{FE} ≅ 5

† Select for operation at 1.3V

‡ I_Q ≅ 600 μA to 900 μA

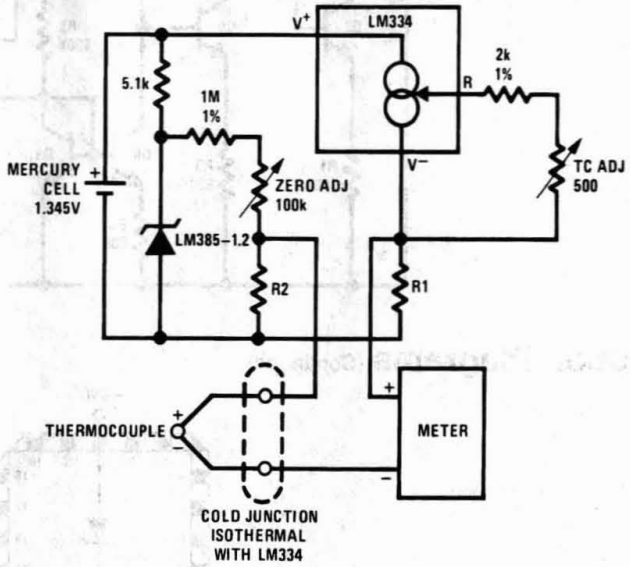
0°F – 50°F Thermometer



Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

Micropower Thermocouple Cold Junction Compensator



TL/H/5518–5

Adjustment Procedure

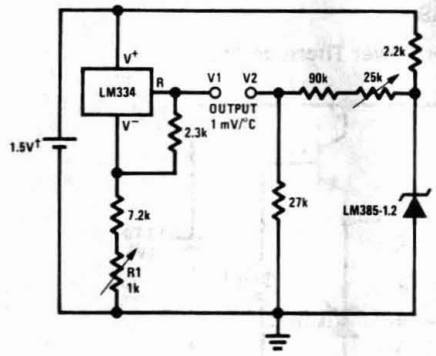
1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @ 25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

Typical supply current 50 μA

Typical Applications (Continued)

Centigrade Thermometer



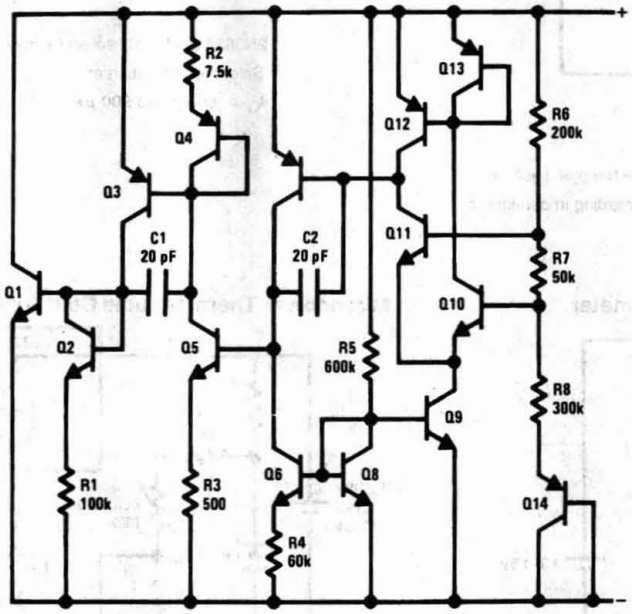
Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

†I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

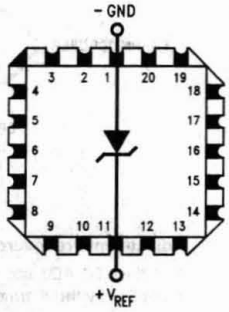
TL/H/5518–1

Schematic Diagram



TL/H/5518–7

Connection Diagrams (Continued)



TL/H/5518–12

Order Number LM185E-1.2/883
See NS Package Number E20A

National Semiconductor

LM185-2.5/LM285-2.5/LM385-2.5 Micropower Voltage Reference Diode

General Description

The LM185-2.5/LM285-2.5/LM385-2.5 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 20 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM-185-2.5 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-2.5 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-2.5 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life.

Further, the wide operating current allows it to replace older references with a tighter tolerance part. For applications requiring 1.2V see LM185-1.2.

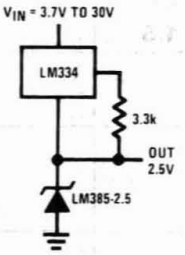
The LM185-2.5 is rated for operation over a −55°C to 125°C temperature range while the LM285-2.5 is rated −40°C to 85°C and the LM385-2.5 0°C to 70°C. The LM185-2.5/LM285-2.5 are available in a hermetic TO-46 package and the LM285-2.5/LM385-2.5 are also available in a low-cost TO-92 molded package, as well as S.O. The LM185-25 is also available in a hermetic leadless chip carrier package.

Features

- ±20 mV (±0.8%) max. initial tolerance (A grade)
- Operating current of 20 μA to 20 mA
- 0.6Ω dynamic impedance (A grade)
- Low temperature coefficient
- Low voltage reference—2.5V
- 1.2V device and adjustable device also available—LM185-1.2 series and LM185 series, respectively

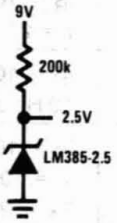
Applications

Wide Input Range Reference



TL/H/5519–12

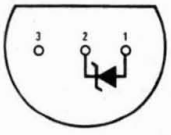
Micropower Reference from 9V Battery



TL/H/5519–2

Connection Diagrams

TO-92
Plastic Package

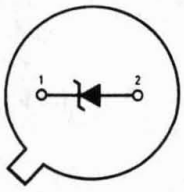


TL/H/5519–8

Bottom View

Order Number LM285Z-2.5, LM285AZ-2.5, LM285AXZ-2.5, LM285AYZ-2.5, LM285BXZ-2.5, LM285BYZ-2.5, LM385Z-2.5, LM385AZ-2.5, LM385AXZ-2.5, LM385AYZ-2.5, LM385BZ-2.5, LM385BXZ-2.5 or LM385BYZ-2.5
See NS Package Number Z03A

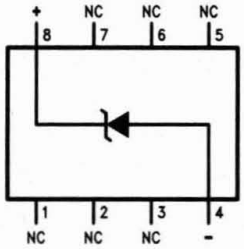
TO-46
Metal Can Package



TL/H/5519–13

Bottom View
Order Number LM185H-2.5, LM185H-2.5/883 LM185BXH-2.5, LM185BXH-2.5/883, LM185BYH-2.5, LM185BYH2.5/883, LM285H-2.5, LM285BXH-2.5 or LM285BYH-2.5
See NS Package Number H02A

SO Package



TL/H/5519–11

Order Number LM285M-2.5, LM285AM-2.5, LM285AXM-2.5, LM285AYM-2.5, LM285BXM-2.5, LM285BYM-2.5, LM385M-2.5, LM385AM-2.5, LM385AXM-2.5, LM385AYM-2.5, LM385BM-2.5, LM385BXM-2.5 or LM385BYM-2.5
See NS Package Number M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 2)

Reverse Current	30 mA
Forward Current	10 mA
Operating Temperature Range (Note 3)	
LM185-2.5	−55°C to + 125°C
LM285-2.5	−40°C to + 85°C
LM385-2.5	0°C to 70°C
Storage Temperature	−55°C to + 150°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	Typ	LM285A-2.5 LM285AX-2.5 LM285AY-2.5		LM385A-2.5 LM385AX-2.5 LM385AY-2.5		Units (Limits)
			Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	I_R = 100 μA	2.500	2.480 2.520		2.480 2.520		V(Min) V(Max)
		2.500		**2.460** **2.535**		**2.470** **2.530**	V(Min) V(Max)
Minimum Operating Current		12	18	**20**	18	**20**	μA (Max)
Reverse Breakdown Voltage Change with Current	$I_{MIN} \le I_R \le$ 1mA		1	**1.5**	1	**1.5**	mV (Max)
	1 mA ≤ I_R ≤ 20 mA		10	**20**	10	**20**	mV (Max)
Reverse Dynamic Impedance	I_R = 100 μA, f = 20 Hz	0.2		0.6 **1.5**		0.6 **1.5**	Ω
Wideband Noise (rms)	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	120					μV
Long Term Stability	I_R = 100 μA, T = 1000 Hr, T_A = 25°C ±0.1°C	20					ppm
Average Temperature Coefficient (Note 7)	$I_{MIN} \le I_R \le$ 20 mA X Suffix Y Suffix All Others		**30** **50**	 **150**	**30** **50**	 **150**	ppm/°C (Max)

Electrical Characteristics (Continued) (Note 4)

Parameter	Conditions	Typ	LM185-2.5 LM185BX-2.5 LM185BY-2.5 LM285-2.5 LM285BX-2.5 LM285BY-2.5		LM385B-2.5 LM385BX-2.5 LM385BY-2.5		LM385-2.5		Units (Limit)
			Tested Limit (Notes 5, 8)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Reverse Breakdown Voltage	T_A = 25°C, 20 μA ≤ I_R ≤ 20 mA	2.5	2.462 2.538		2.462 2.538		2.425 2.575		V(Min) V(Max)
Minimum Operating Current		13	20	**30**	20	**30**	20	**30**	μA (Max)
Reverse Breakdown Voltage Change with Current	20 μA ≤ I_R ≤ 1 mA		1	**1.5**	2.0	**2.5**	2.0	**2.5**	mV (Max)
	1 mA ≤ I_R ≤ 20 mA		10	**20**	20	**25**	20	**25**	mV (Max)
Reverse Dynamic Impedance	I_R = 100 μA, f = 20 Hz	1							Ω
Wideband Noise (rms)	I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	120							μV
Long Term Stability	I_R = 100 μA, T = 1000 Hr, T_A = 25°C ±0.1°C	20							ppm
Average Temperature Coefficient (Note 7)	I_R = 100 μA X Suffix Y Suffix All Others		 **30** **50**	 **150**	 **30** **50**	 **150**	 	 **150**	 ppm/°C ppm/°C ppm/°C (Max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS185H-2.5 for military specifications.

Note 3: For elevated temperature operation, $T_{J\ MAX}$ is:

LM185	150°C
LM285	125°C
LM385	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" Leads) 170°C/W (0.125" Leads)	440°C/W	165°C/W
θ_{ja} (Junction to Case)	N/A	80°C/W	N/A

Note 4: Parameters identified with **boldface type** apply at temperature extremes. All other numbers apply at T_A = T_J = 25°C.

Note 5: Guaranteed and 100% production tested.

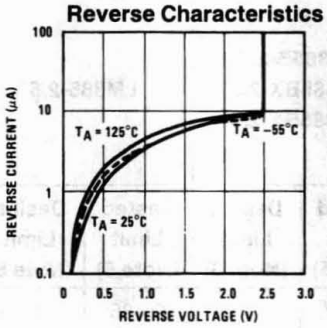
Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate average outgoing quality levels.

Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX}-T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

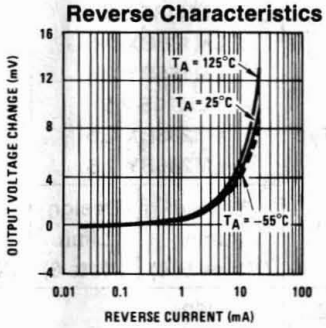
Note 8: A military RETS electrical specification available on request.

Typical Performance Characteristics

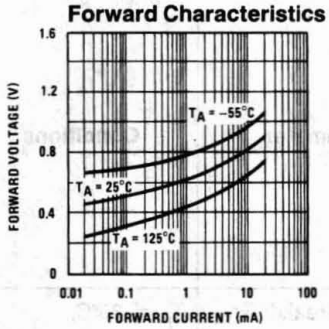
Reverse Characteristics



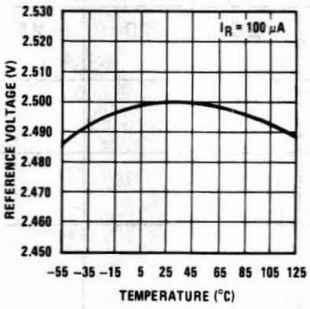
Reverse Characteristics



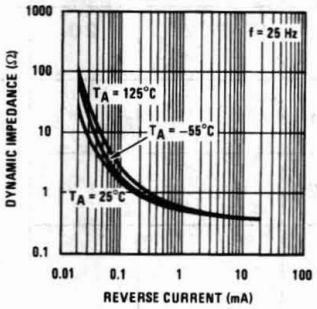
Forward Characteristics



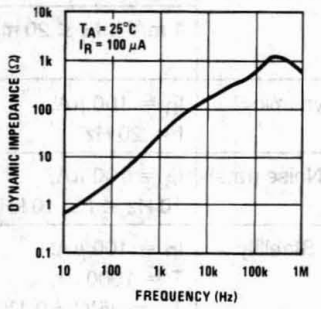
Temperature Drift



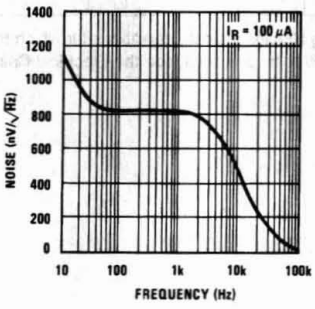
Reverse Dynamic Impedance



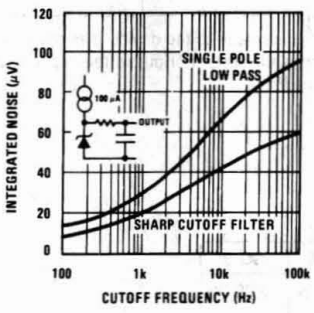
Reverse Dynamic Impedance



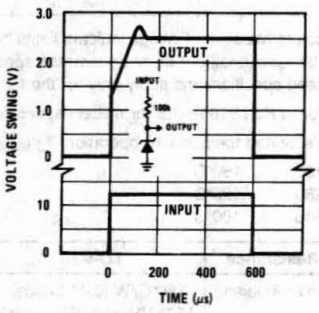
Noise Voltage



Filtered Output Noise

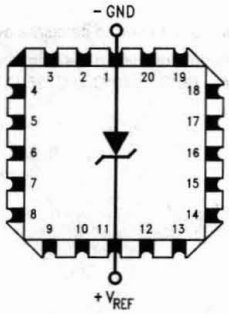


Response Time



TL/H/5519–3

Connection Diagram

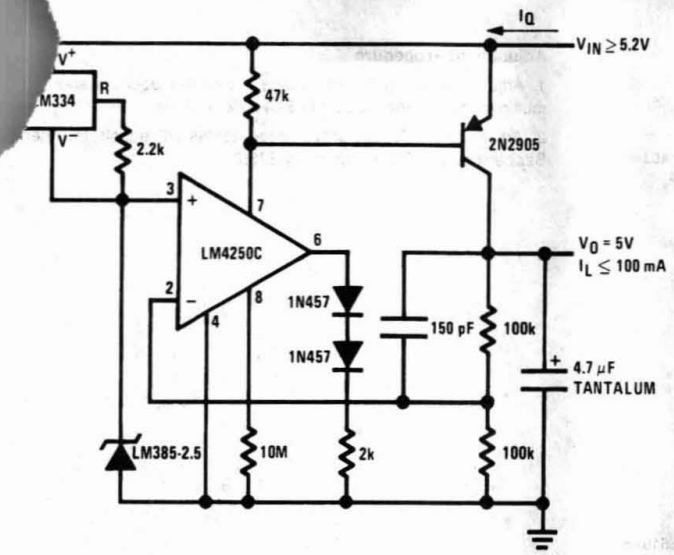


TL/H/5519–14

Order Number LM185E-2.5/883
See NS Package Number E20A

385-2.5 Applications

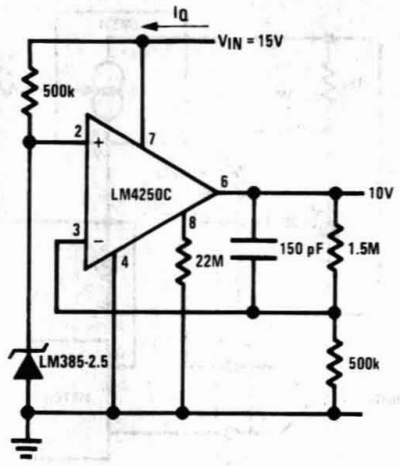
Micropower* 5V Regulator



*$I_Q \cong 40\ \mu A$

TL/H/5519–9

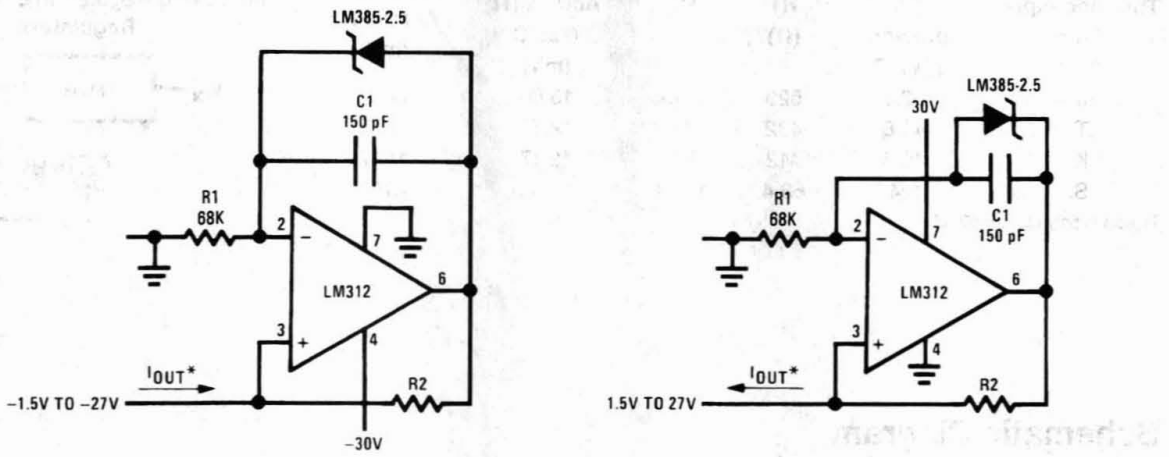
Micropower* 10V Reference



TL/H/5519–10

*$I_Q \cong 30\ \mu A$ standby current

Precision 1 μA to 1 mA Current Sources

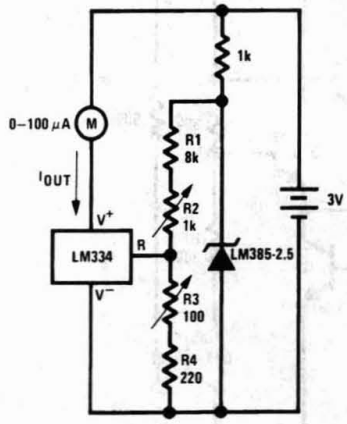


*$I_{OUT} = \frac{2.5V}{R2}$

TL/H/5519–4

METER THERMOMETERS

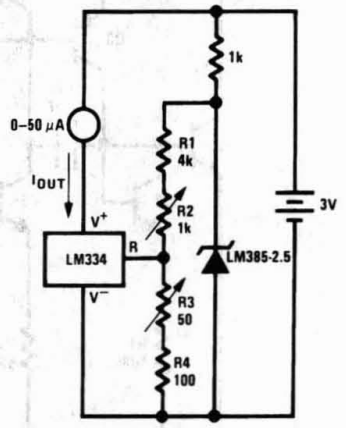
0°C–100°C Thermometer



Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

0°F–50°F Thermometer



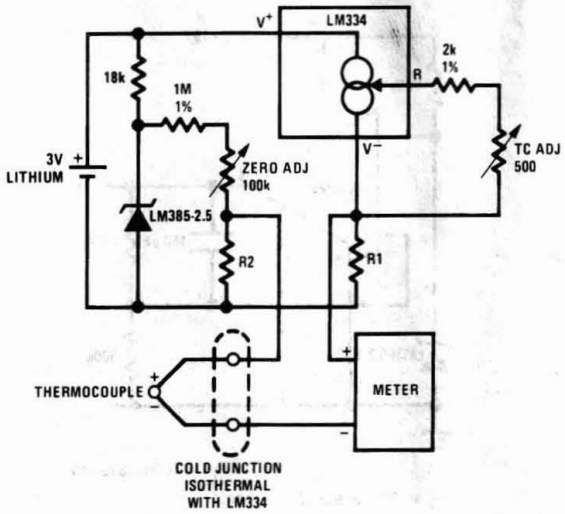
TL/H/5519–5

Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

LM385-2.5 Applications (Continued)

Micropower Thermocouple Cold Junction Compensator



TL/H/5519–6

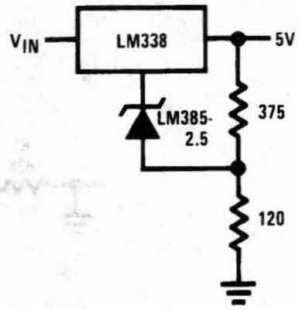
Adjustment Procedure

1. Adjust TC ADJ pot until voltage across R1 equals Kelvin multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the ther Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

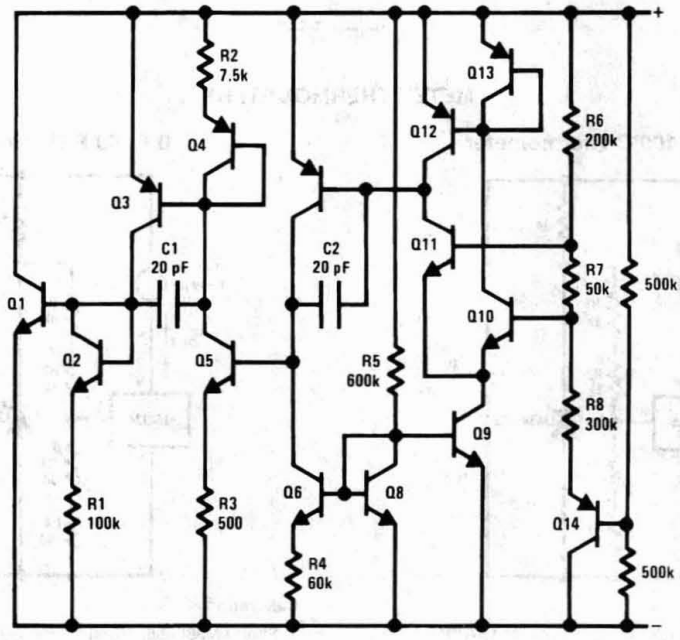
Typical supply current 50 μA

Improving Regulation of Adjustable Regulators



TL/H/5519–7

Schematic Diagram



TL/H/5519–1

National Semiconductor

LM199/LM299/LM399/LM3999 Precision Reference

General Description

The LM199 series are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

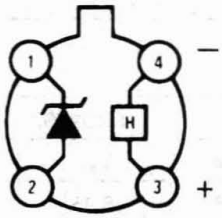
The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C

Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400 μA
- Wide operating current — 500 μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm
- Proven reliability, low-stress packaging in TO-46 integrated-circuit hermetic package, for low hysteresis after thermal cycling. 33 million hours MTBF at $T_A = +25°C$ ($T_J = +86°C$)
- Certified long term stability available
- MIL-STD-883 compliant

Connection Diagrams

Metal Can Package (TO-46)

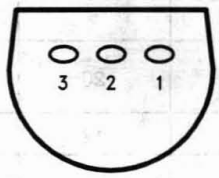


TL/H/5717–14

Top View

LM199/LM299/LM399 (See Table on fourth page)
NS Package Number H04D

Plastic Package TO-92



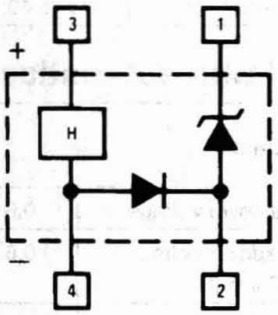
TL/H/5717–10

Bottom View

LM3999 (See Table on fourth page)
NS Package Number Z03A

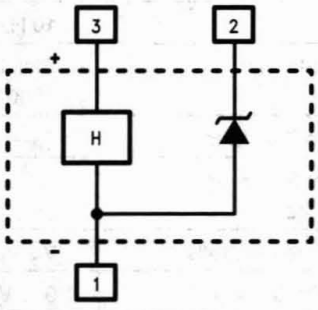
Functional Block Diagrams

LM199/LM299/LM399



TL/H/5717–15

LM3999



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4

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the following Reliability Electrical Test Specifications documents: RETS199X for LM199, RETS199AX for LM199A.

Temperature Stabilizer Voltage
- LM199/LM299/LM399 40V
- LM3999 36V

Reverse Breakdown Current 20 mA

Forward Current
- LM199/LM299/LM399 1 mA
- LM3999 −0.1 mA

Reference to Substrate Voltage $V_{(RS)}$ (Note 1) 40V, −0.1V

Operating Temperature Range
- LM199 −55°C to +125°C
- LM299 −25°C to +85°C
- LM399/LM3999 −0°C to +70°C

Storage Temperature Range −55°C to +150°C

Soldering Information
- TO-92 package (10 sec.) +260°C
- TO-46 package (10 sec.) +300°C

Electrical Characteristics (Notes 2, 5)

Parameter	Conditions	LM199H/LM299H			LM399H			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	$0.5\ mA \le I_R \le 10\ mA$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le +85°C$ LM199		0.00003	0.0001				%/°C
	$+85°C \le T_A \le +125°C$ LM199		0.0005	0.0015				%/°C
	$-25°C \le T_A \le 85°C$ LM299		0.00003	0.0001				%/°C
	$0°C \le T_A \le +70°C$ LM399					0.00003	0.0002	%/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
	$T_A = -55°C$		22	28				
Temperature Stabilizer Supply Voltage		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		sec.
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = +25°C$, (Note 3)		140	200		140	200	mA

Electrical Characteristics (Note 2)

Parameter	Conditions	LM3999Z			Units
		Min	Typ	Max	
Reverse Breakdown Voltage	$0.6\ mA \le I_R \le 10\ mA$	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	$0.6\ mA \le I_R \le 10\ mA$		6	20	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	$0°C \le T_A \le 70°C$		0.0002	0.0005	%/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$		7		μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20		ppm
Temperature Stabilizer	$T_A = 25°C$, Still Air, $V_S = 30V$		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		5		sec.
Initial Turn-On Current	$9 \le V_S \le 40$, $T_A = 25°C$		140	200	mA

Electrical Characteristics (Notes 2, 5)

Parameter	Conditions		LM199AH, LM299AH			LM399AH			Units
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	$0.5\ mA \le I_R \le 10\ mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le +85°C$	LM199A		0.00002	0.00005				%/°C
	$+85°C \le T_A \le +125°C$	LM199A		0.0005	0.0010				%/°C
	$-25°C \le T_A \le 85°C$	LM299A		0.00002	0.00005				%/°C
	$0°C \le T_A \le +70°C$	LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$			7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = -55°C$			22	28				
Temperature Stabilizer Supply Voltage			9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		sec.
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = +25°C$, (Note 3)			140	200		140	200	mA

Electrical Characteristics (Notes 2, 5)

Parameter	Conditions		LM199AH-20, LM299AH-20			LM399AH-50			Units
			Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \le I_R \le 10\ mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le 85°$	LM199A		0.00002	0.00005				%/°C
	$85°C \le T_A \le 125°C$	LM199A		0.0005	0.0010				%/°C
	$-25°C \le T_A \le 85°C$	LM299A		0.00002	0.00005				%/°C
	$0°C \le T_A \le 70°C$	LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$			7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$			8	20		9	50	ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = 55°C$			22	28				
Temperature Stabilizer Supply Voltage			9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		s
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = 25°C$, (Note 3)			140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \le T_A \le +125°C$ for the LM199; $-25°C \le T_A \le +85°C$ for the LM299 and $0°C \le T_A \le +70°C$ for the LM399 and LM3999.

Note 3: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

Note 4: Do not wash the LM199 with its polysulfone thermal shield in TCE.

Note 5: A military RETS electrical test specification is available for the LM199H/883, LM199AH/883, and LM199AH-20/883 on request.

Ordering Information

Initial Tolerance	0°C to +70°C	−25°C to +85°C	−55°C to +125°C	NS Package
2%		LM299AH	LM199AH, LM199AH/883	H04D
5%	LM399H LM399AH	LM299H	LM199H, LM199H/883	H04D
5%	LM3999Z			Z03A
Guaranteed Long Term Stability	LM399AH-50	LM299AH-20	LM199AH-20, LM199AH-20/883	H04D

Certified Long Term Drift

The National Semiconductor LM199AH-20, LM299AH-20, and LM399AH-50 are ultra-stable Zener references specially selected from the production runs of LM199AH, LM299AH, LM399AH and tested to confirm a long-term stability of 20, 20, or 50 ppm per 1000 hours, respectively. The devices are measured every 168 hours and the voltage of each device is logged and compared in such a way as to show the deviation from its initial value. Each measurement is taken with a probable-worst-case deviation of ±2 ppm, compared to the Reference Voltage, which is derived from several groups of NBS-traceable references such as LM199AH-20's, 1N827's, and saturated standard cells, so that the deviation of any one group will not cause false indications. Indeed, this comparison process has recently been automated using a specially prepared computer program which is custom-designed to reject noisy data (and require a repeat reading) and to record the average of the best 5 of 7 readings, just as a sagacious standards engineer will reject unbelievable readings.

The typical characteristic for the LM199AH-20 is shown below. This computerized print-out form of each reference's stability is shipped with the unit.

Typical Characteristics

National Semiconductor
Certified Long Term Drift

Hrs	Drift
168	−20
336	−24
504	−36
672	−34
840	−40
1008	−36

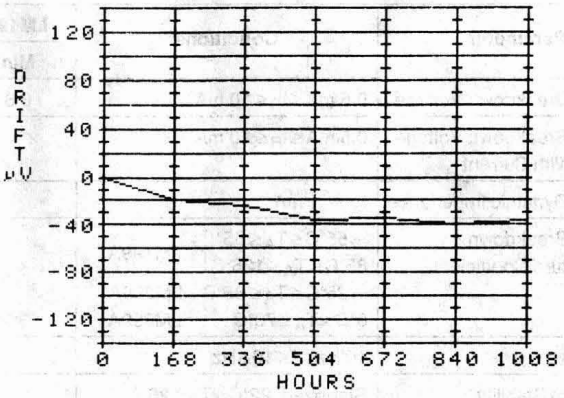
LM199AH-20
Part #6849

Limits

LM199AH-20	140 μV
LM299AH-20	140 μV
LM399AH-20	350 μV

Testing Conditions

Heater Voltage	30V
Zener Current	1 mA
Ambient Temp.	25°C



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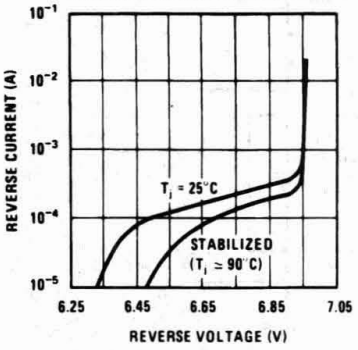
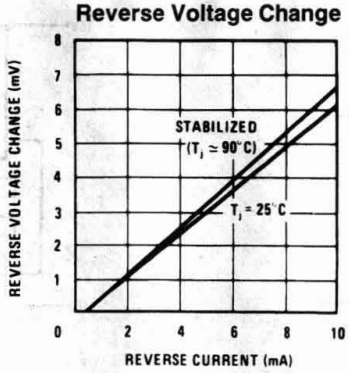
Typical Performance Characteristics

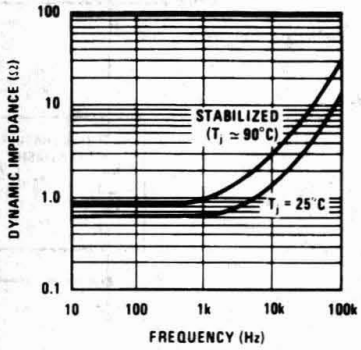
Reverse Characteristics



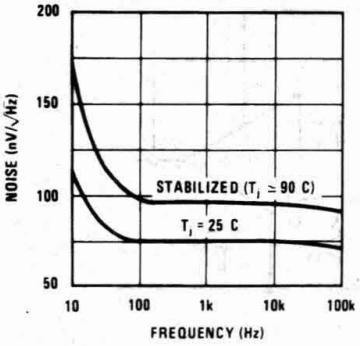
Reverse Voltage Change



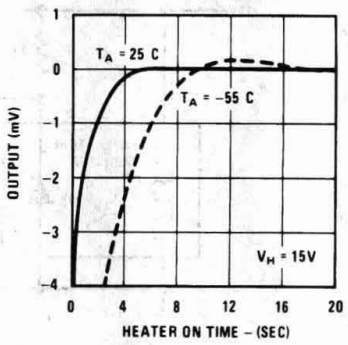
Dynamic Impedance



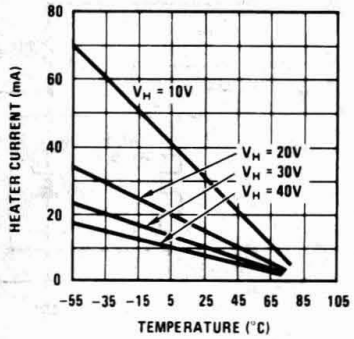
Zener Noise Voltage



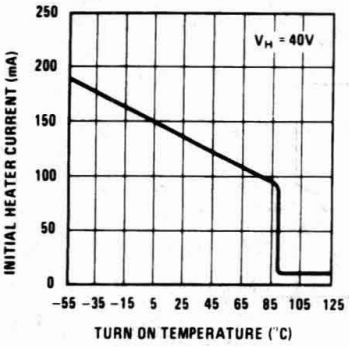
Stabilization Time



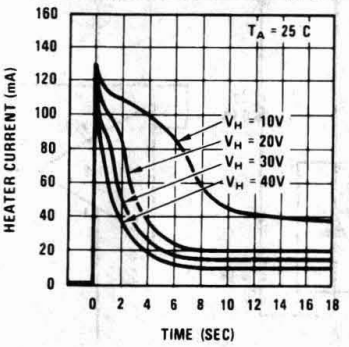
Heater Current



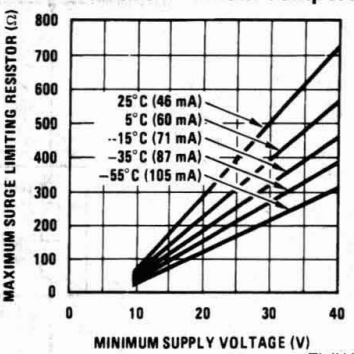
Initial Heater Current



Heater Current (To Limit This Surge, See Next Graph)



Heater Surge Limit Resistor vs Minimum Supply Voltage at Various Minimum Temperatures



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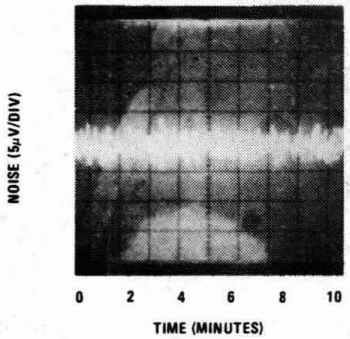
*Heater must be bypassed with a 2 μF or larger tantalum capacitor if resistors are used.

Low Frequency Noise Voltage



0.01 Hz ≤ f ≤ 1 Hz
STABILIZED
($T_j \simeq$ 90°C)

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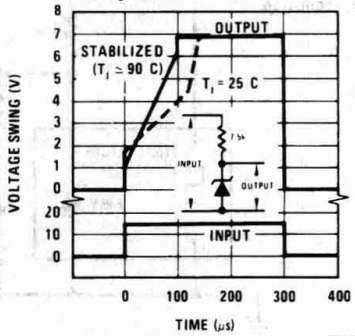
Response Time



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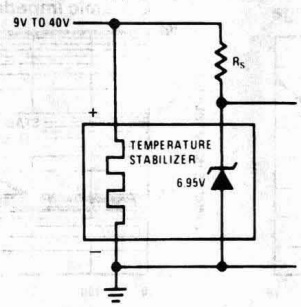
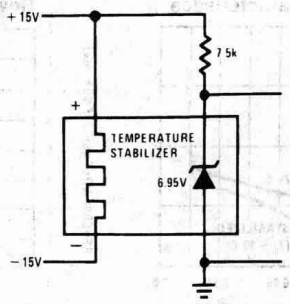
Typical Applications

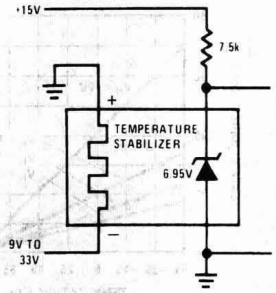
Single Supply Operation



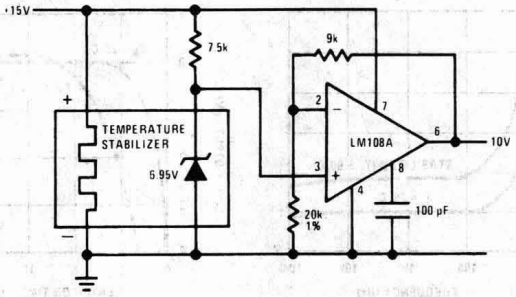
Split Supply Operation



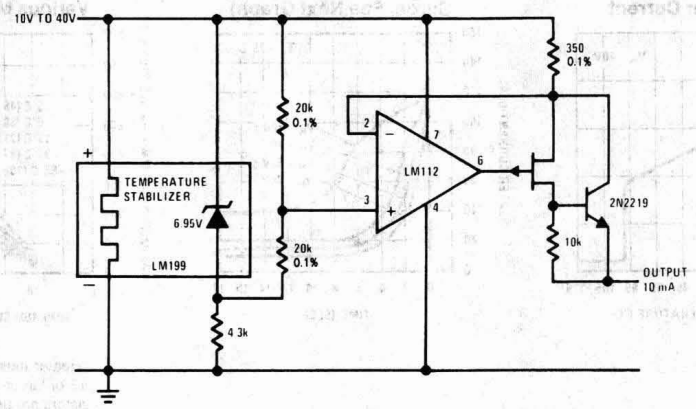
Negative Heater Supply with Positive Reference



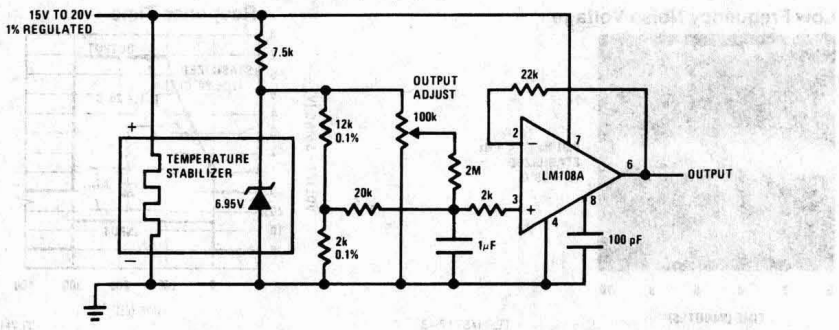
Buffered Reference With Single Supply



Positive Current Source



Standard Cell Replacement



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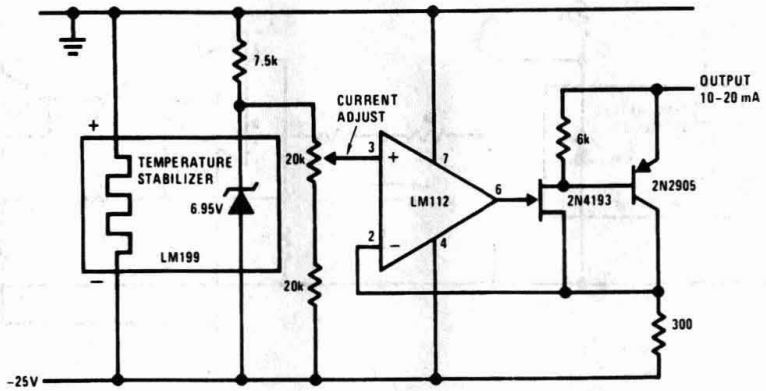
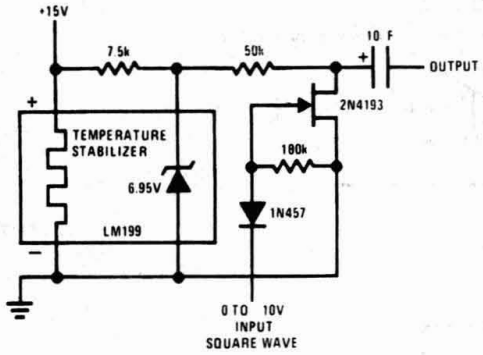
Typical Applications (Continued)

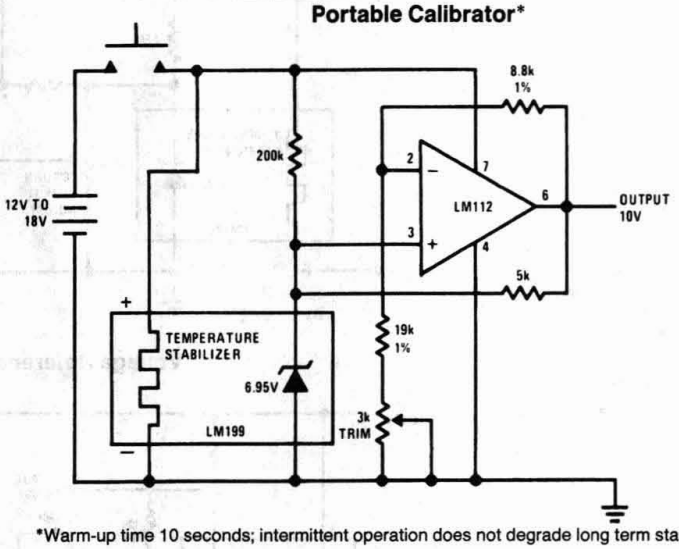
Negative Current Source



Square Wave Voltage Reference

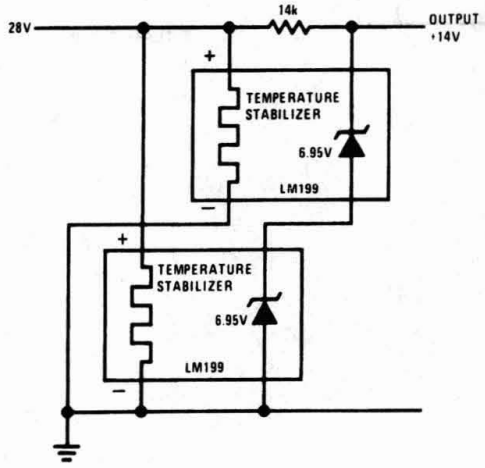


Portable Calibrator*

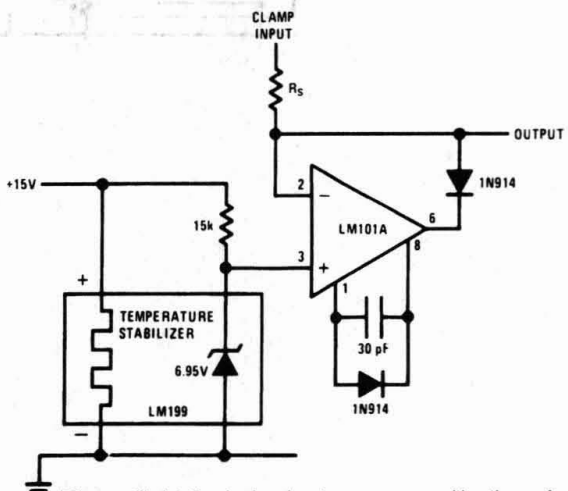


*Warm-up time 10 seconds; intermittent operation does not degrade long term stability.

14V Reference



Precision Clamp*



*Clamp will sink 5 mA when input goes more positive than reference

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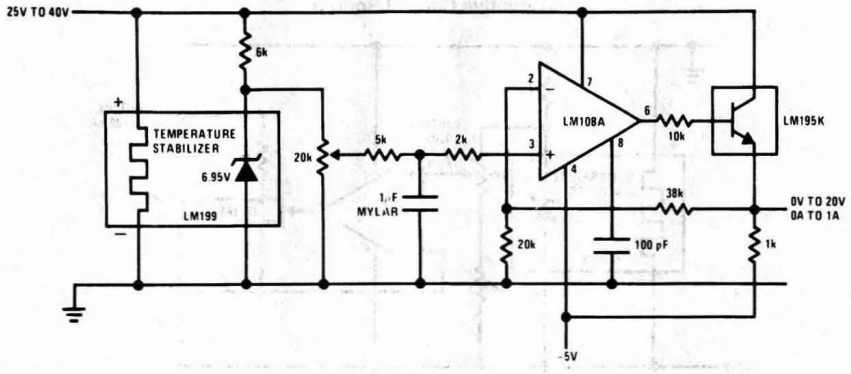
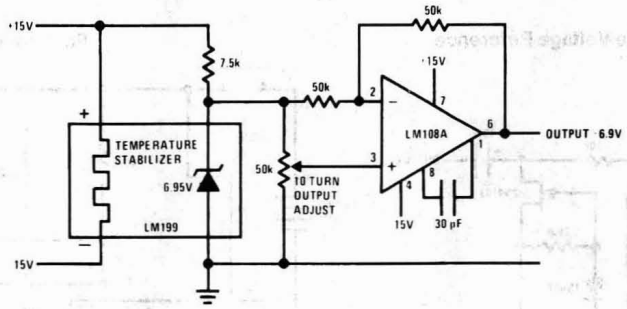
Typical Applications (Continued)

0V to 20V Power Reference



Bipolar Output Reference



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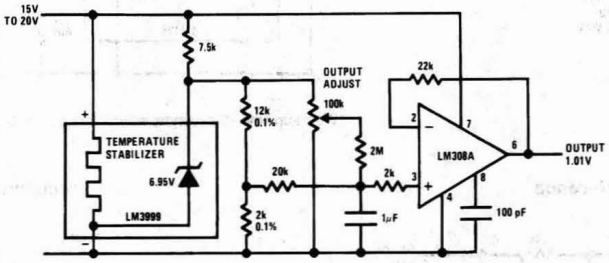
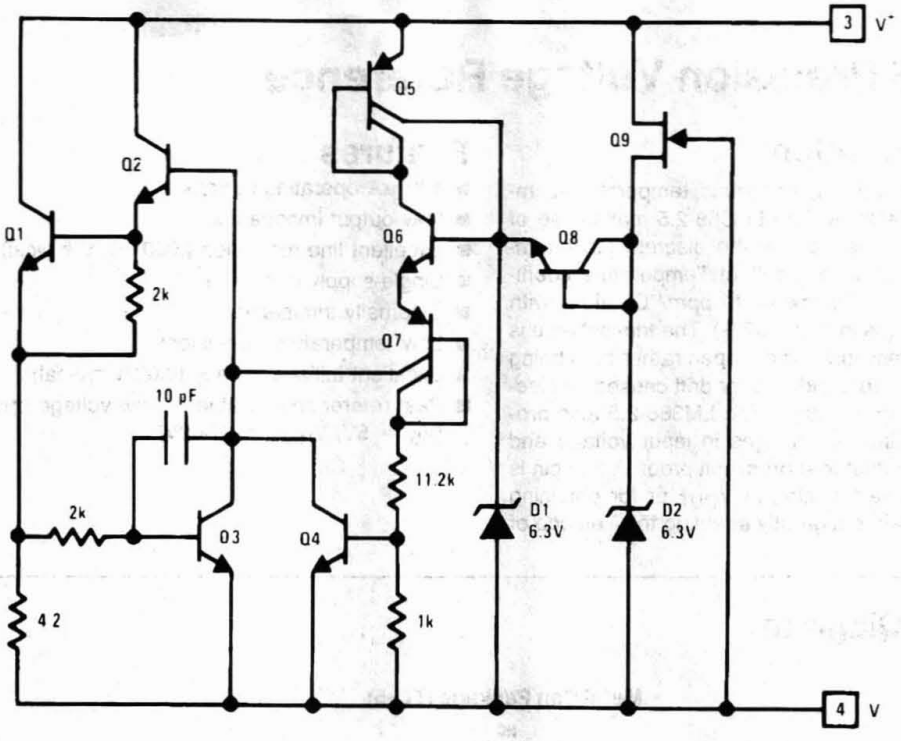
Voltage Reference



TL/H/5717–9

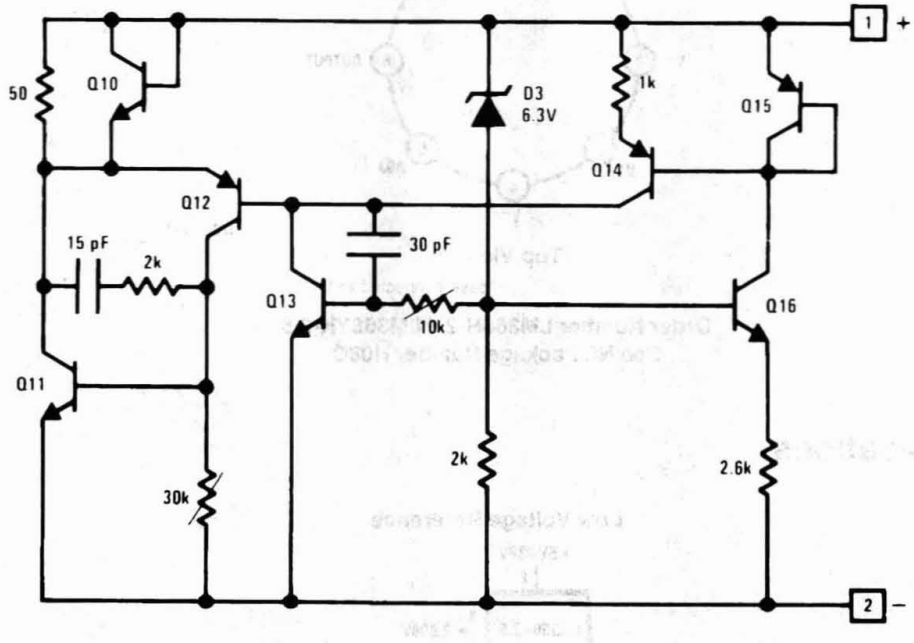
Schematic Diagrams

Temperature Stabilizer



TL/H/5717–01

Reference



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National Semiconductor

LM368-2.5 Precision Voltage Reference

General Description

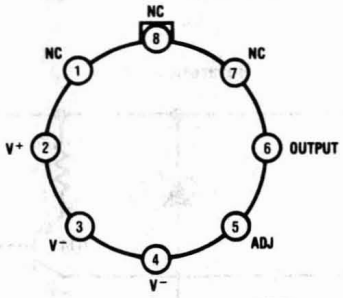
The LM368-2.5 is a precision, monolithic, temperature-compensated voltage reference. The LM368-2.5 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{OUT} (as low as 11 ppm/°C), along with tight initial tolerance, (as low as 0.02%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM368-2.5 also provides excellent stability vs. changes in input voltage and output current. The output is short circuit proof. A trim pin is made available for fine trimming of V_{OUT} or for obtaining intermediate values without greatly affecting the Tempco of the device.

Features

- 400 μA operating current
- Low output impedance
- Excellent line regulation (.0001%/V typical)
- Single-supply operation
- Externally trimmable
- Low temperature coefficient
- Excellent initial accuracy (0.02% typical)
- Best reference available for low-voltage operation (V_S = 5V, V_{REF} = 2.500V)

Connection Diagram

Metal Can Package (TO-5)



TL/H/8446–1

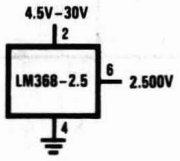
Top View

*case connected to V−

Order Number LM368H-2.5 LM368YH-2.5
See NS Package Number H08C

Typical Applications

Low Voltage Reference



TL/H/8446–2

Absolute Maximum Ratings (Note 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	35V
Power Dissipation	600 mW
Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	0°C to +70°C

Soldering Information

TO-5 (H) Package (10 sec.) +300°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM368-2.5			
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Max. unless noted)
V_{OUT} Error: LM368		±0.02	±0.2		%
Line Regulation	5.0V ≤ V_{IN} ≤ 30V	±0.0001	±0.0005		%/V
Load Regulation (Note 8)	0 mA ≤ I_{SOURCE} ≤ 10 mA	±0.0003	±0.0025		%/mA
Thermal Regulation	T = 20 mS (Note 4)	±0.005	±0.02		%/100 mW
Quiescent Current		350	550		μA
Change of Quiescent Current vs. V_{IN}	5.0V ≤ V_{IN} ≤ 30V	3	5		μA/V
Temperature Coefficient of V_{OUT} (see graph): LM368Y-2.5	0°C ≤ T_A ≤ 70°C	±11	±20		ppm/°C
(Note 5) LM368-2.5	0°C ≤ T_A ≤ 70°C	±15		±30	ppm/°C
Short Circuit Current	V_{OUT} = 0	30	70	100	mA
Noise: 0.1–10 Hz		12			uVp-p
100 Hz–10 kHz		420			nV/$\sqrt{Hz}$
V_{OUT} Adjust Range	0 ≤ V_{PIN5} ≤ V_{OUT}	1.9–5.2		2.2–5.0	V min.

Note 1: Unless otherwise noted, these specifications apply: T_A = 25°C, 4.9V ≤ V_{IN} ≤ 10.5V, 0 ≤ I_{LOAD} ≤ 0.5 mA, 0≤ C_L ≤ 200 pF.

Note 2: Tested Limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: Thermal Regulation is defined as the change in the output Voltage at a time T after a step change in power dissipation of 100 mW.

Note 5: Temperature Coefficient of V_{OUT} is defined as the worst case delta-V_{OUT} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (See graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

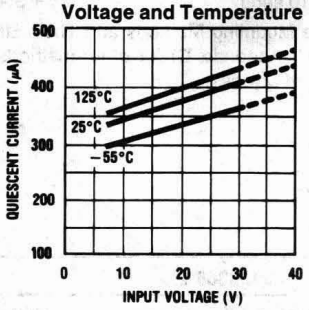
Note 6: In metal can (H), $\theta_{J\text{-}C}$ is 75°C/W and $\theta_{J\text{-}A}$ is 150°C/W.

Note 7: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its Rated Operating Conditions (see Note 1 and Conditions).

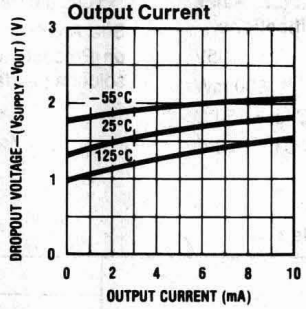
Note 8: Load regulation is measured on the output pin at a point 1/8" below the base of the package. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Typical Performance Characteristics (Note 1)

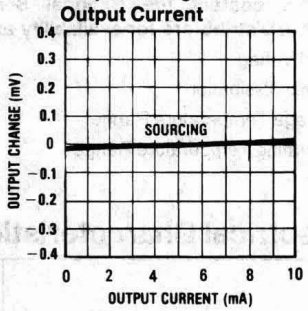
Quiescent Current vs. Input Voltage and Temperature



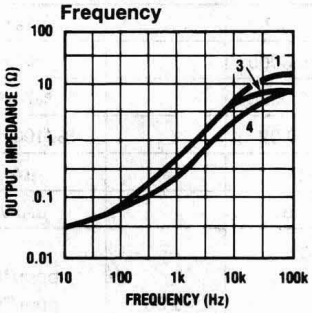
Dropout Voltage vs. Output Current



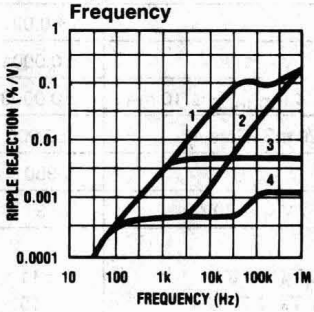
Output Change vs. Output Current



Output Impedance vs. Frequency

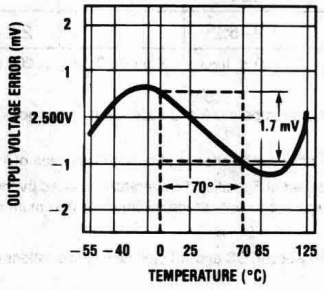


Ripple Rejection vs. Frequency

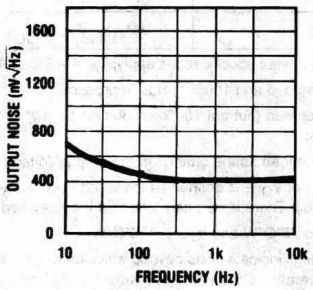


(1) LM368 as is.
(2) with 0.01 μf Mylar, Trim to Gnd.
(3) with 10Ω in series with 10 μf, V_{OUT} to Gnd.
(4) with Both.

Temperature Coefficient: LM368-2.5 (Curve A)



Output Noise vs. Frequency

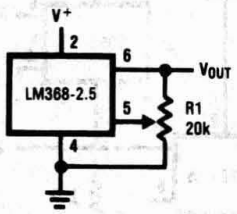


TL/H/8446–3

Typical Temperature Coefficient Calculations:
LM368-2.5 (see Curve A)
T.C. = 1.7 mV/(70° × 2.5V)
= 9.7 ppm/°C

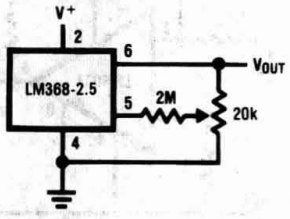
Typical Applications

Wide Range Trimmable Regulator



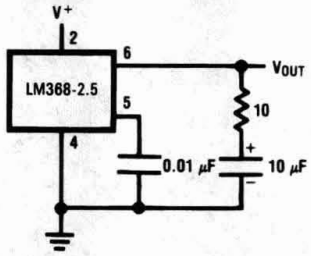
TL/H/8446–5

Narrow Range Trimmable Regulator (±1% min.)



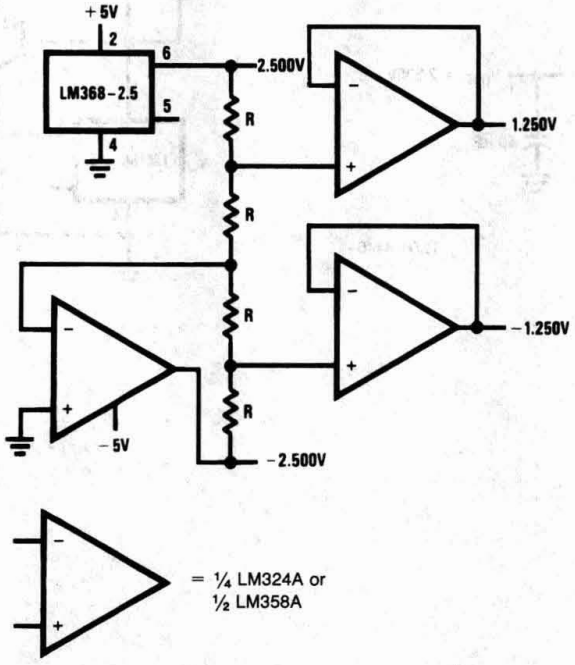
TL/H/8446–6

Improved Noise Performance



TL/H/8446–7

±2.5V, ±1.25V References

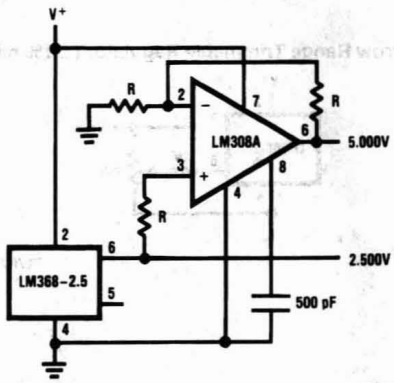


TL/H/8446–8

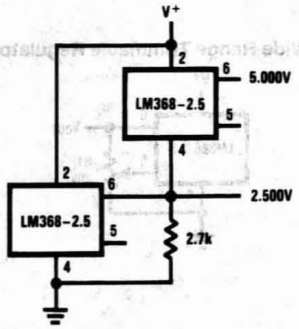
R= Thin Film Resistor Network,
±0.05% Matching and 5 ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Typical Applications (Continued)

Multiple Output Voltages



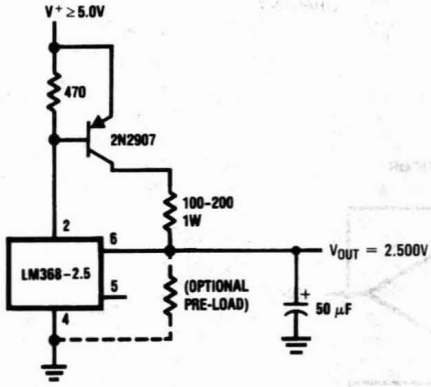
TL/H/8446–10



TL/H/8446–9

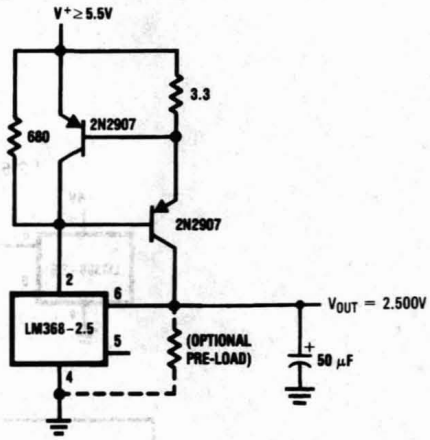
R = Thin Film Resistor Network
0.05% Matching and 5 ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Reference with Booster



TL/H/8446–11

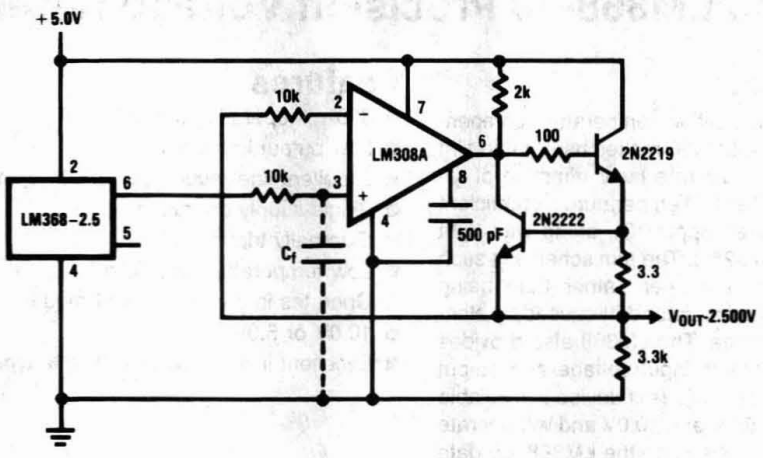
100 mA Boosted Reference



TL/H/8446–12

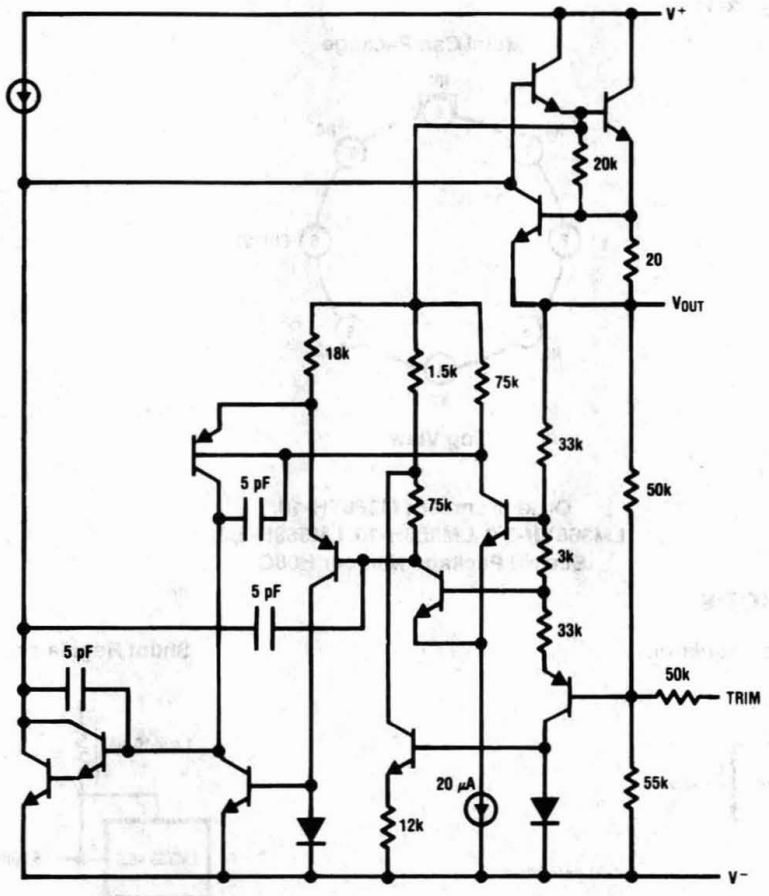
Typical Applications (Continued)

Buffered High-Current Reference with Filter



TL/H/8446–13

Simplified Schematic Diagram



TL/H/8446–14

*Reg. U.S. Pat. Off.

National Semiconductor

LM368-5.0 and LM368-10 Precision Voltage References

General Description

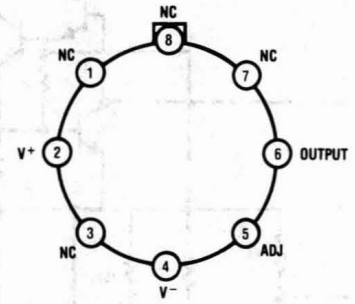
The LM368 is a precision, monolithic, temperature-compensated voltage reference. The LM368 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{OUT} (as low as 5ppm/°C), along with tight initial tolerance, (as low as 0.02%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM368 also provides excellent stability vs. changes in input voltage and output current (both sourcing and sinking). This device is available in output voltage options of 5.0V and 10.0V and will operate in both series or shunt mode. Also see the LM368-2.5 data sheet for a 2.5V output. The devices are short circuit proof when sourcing current. A trim pin is made available for fine trimming of V_{OUT} or for obtaining intermediate values without greatly affecting the Tempco of the device.

Features

- 300 μA operating current
- Low output impedance
- Excellent line regulation (.0001%/V typical)
- Single-supply operation
- Externally trimmable
- Low temperature coefficient
- Operates in series or shunt mode
- 10.0V or 5.0V
- Excellent initial accuracy (0.02% typical)

Connection Diagram

Metal Can Package



TL/H/5522–1

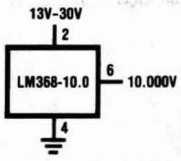
Top View

*case connected to V−

Order Number LM368YH-10, LM368YH-5.0, LM368H-10, LM368H-5.0
See NS Package Number H08C

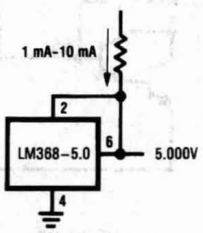
Typical Applications

Series Regulator



TL/H/5522–2

Shunt Regulator



TL/H/5522–3

Absolute Maximum Ratings (Note 8)

Input Voltage (Series Mode) 35V
Reverse Current (Shunt Mode) 50 mA
Power Dissipation 600 mW
Storage Temperature Range −60°C to +150°C
Operating Temperature Range
LM368 0°C to +70°C

Soldering Information
TO-5 (H) Package, 10 sec. +300°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM368			
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Max. unless noted)
V_{OUT} Error		±0.02	±0.1		%
Line Regulation	$(V_{OUT} + 3V) \le V_{IN} \le 30V$	±0.0001	±0.0005		%/V
Load Regulation (Note 4)	$0\ mA \le I_{SOURCE} \le 10\ mA$	±0.0003	±0.001		%/mA
	$-10\ mA \le I_{SINK} \le 0\ mA$	±0.003	±0.008		%/mA
Thermal Regulation	T = 20 mS (Note 5)	±0.005	±0.01		%/100 mW
Quiescent Current		250	350		μA
Change of Quiescent Current vs. V_{IN}	$(V_{OUT} + 3V) \le V_{IN} \le 30V$	3	5		μA/V
Temperature Coefficient of V_{OUT} (see graph): LM368Y	$0°C \le T_A \le 70°C$	±11	±20		ppm/°C
(Note 6) LM368	$0°C \le T_A \le 70°C$	±15		±30	ppm/°C
Short Circuit Current	$V_{OUT} = 0$	30	70	100	mA
Noise: 10.0V: 0.1 - 10Hz		30			uVp-p
100Hz - 10 kHz		1100			nV/√Hz
6.2V: 0.1 - 10Hz		20			uVp-p
100Hz - 10 kHz		700			nV/√Hz
5.0V: 0.1 - 10Hz		16			uVp-p
100Hz - 10 kHz		575			nV/√Hz
V_{OUT} Adjust Range: 10.000V	$0V \le V_{PIN5} \le V_{OUT}$	4.5-17.0		6.0-15.5	V min.
5.000V		4.4-7.0		4.5-6.0	V min.

Note 1: Unless otherwise noted, these specifications apply: $T_A = 25°C$, $V_{IN} = 15V$, $I_{LOAD} = 0$, $0 \le C_L \le 200$ pF, Circuit is operating in Series Mode. Or, circuit is operating in Shunt Mode, $V_{IN} = +15V$ or $V_{IN} = V_{OUT}$, $TA = +25°C$, $I_{LOAD} = -1.0$ mA, $0 \le C_L \le 200$ pF.

Note 2: Tested Limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: The LM368 has a Class B output, and will exhibit transients at the crossover point. This point occurs when the device is asked to sink approximately 120 μA. In some applications it may be advantageous to preload the output to either V_{IN} or Ground, to avoid this crossover point.

Note 5: Thermal Regulation is defined as the change in the output Voltage at a time T after a step change in power dissipation of 100 mW.

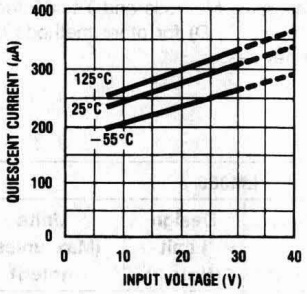
Note 6: Temperature Coefficient of V_{OUT} is defined as the worst case delta-V_{OUT} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (See graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

Note 7: In metal can (H), θ_{J-C} is 75°C/W and θ_{J-A} is 150°C/W.

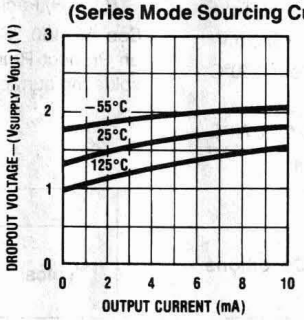
Note 8: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its Rated Operating Conditions (see Note 1 and Conditions).

Typical Performance Characteristics (Note 1)

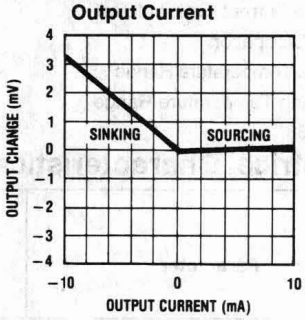
Quiescent Current vs. Input Voltage and Temperature



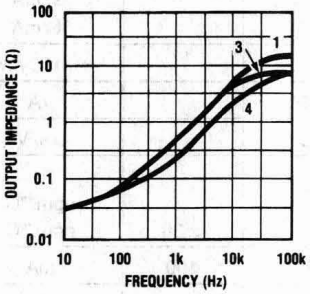
Dropout Voltage vs. Output Current (Series Mode Sourcing Current)



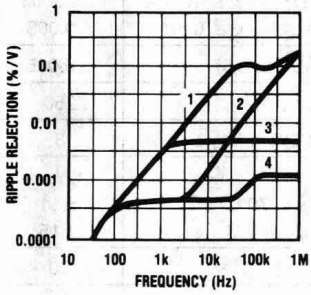
Output Change vs. Output Current



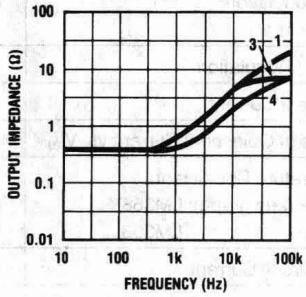
Output Impedance vs. Frequency (Sourcing Current)



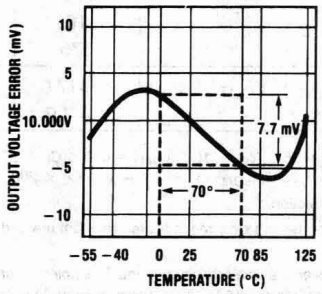
Ripple Rejection vs. Frequency



Output Impedance vs. Frequency (Sinking Current)



Temperature Coefficient: LM368-10 (Curve A)



Typical Temperature Coefficient Calculations:

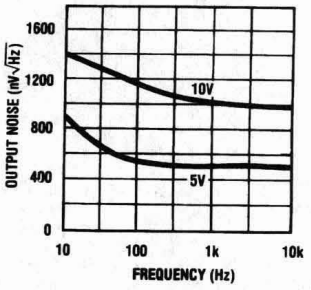
LM368-10 (see Curve A)

T.C. = 7.7 mV/(70° × 10V)

= 11 × 10E-6 = 11ppm/°C

TL/H/5522–4

Output Noise vs. Frequency



TL/H/5522–5

(1) LM368 alone.

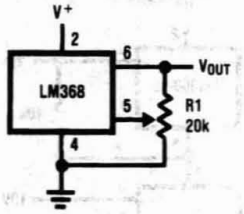
(2) with 0.01 μf Mylar, Trim to Gnd.

(3) with 10Ω in series with 10 μf, V_{OUT} to Gnd.

(4) with Both.

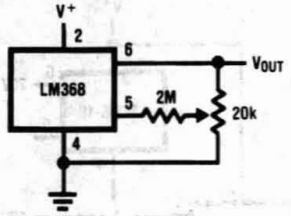
Typical Applications

Wide Range Trimmable Regulator



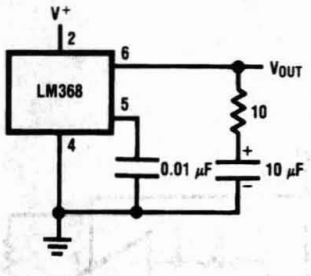
TL/H/5522–7

Narrow Range Trimmable Regulator (±1% min.)



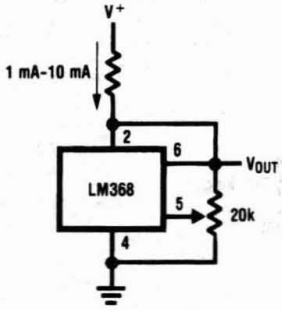
TL/H/5522–8

Improved Noise Performance



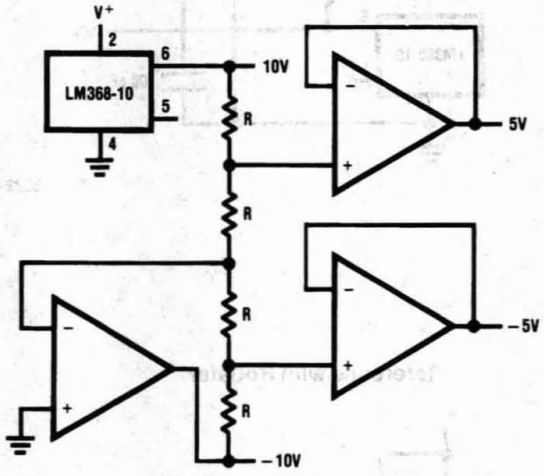
TL/H/5522–10

Adjustable Zener



TL/H/5522–9

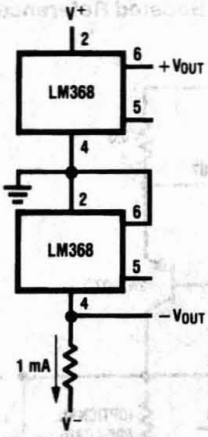
±10V, ±5V References



= ¼ LF444A or
½ LF412A

TL/H/5522–12

± Reference

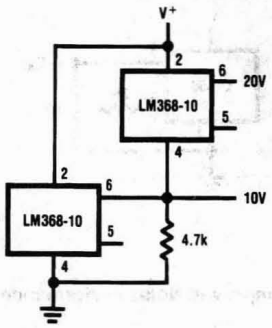


TL/H/5522–11

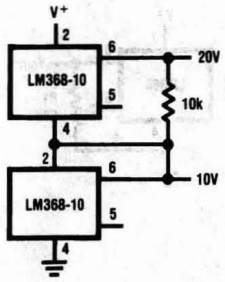
R= Thin Film Resistor Network,
±0.05% Matching and 5ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Typical Applications (Continued)

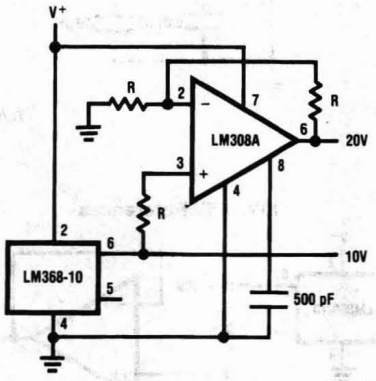
Multiple Output Voltages



TL/H/5522–13



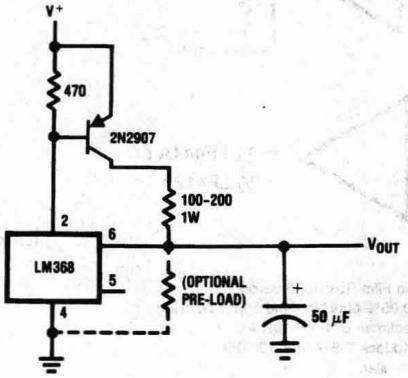
TL/H/5522–14



TL/H/5522–15

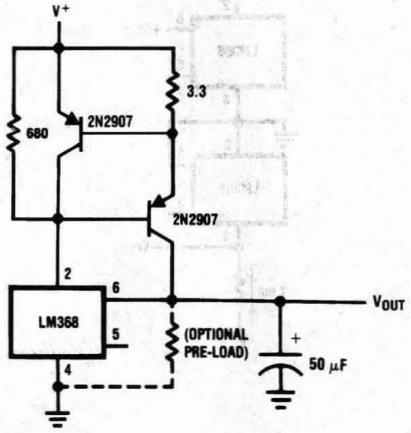
R= Thin Film Resistor Network
0.05% Matching and 5ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Reference with Booster



TL/H/5522–16

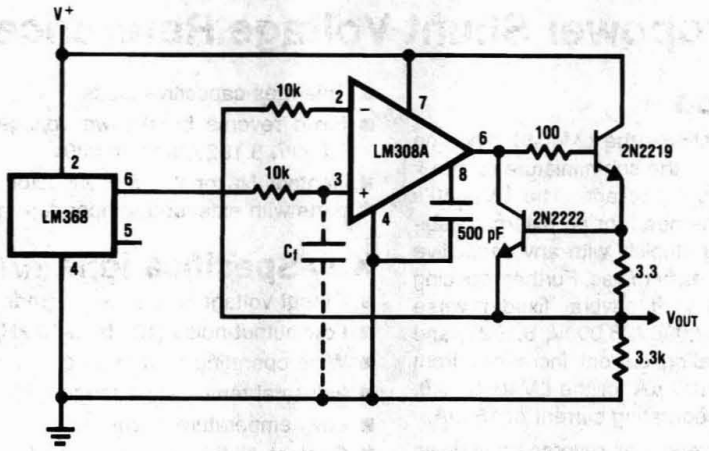
100 mA Boosted Reference



TL/H/5522–17

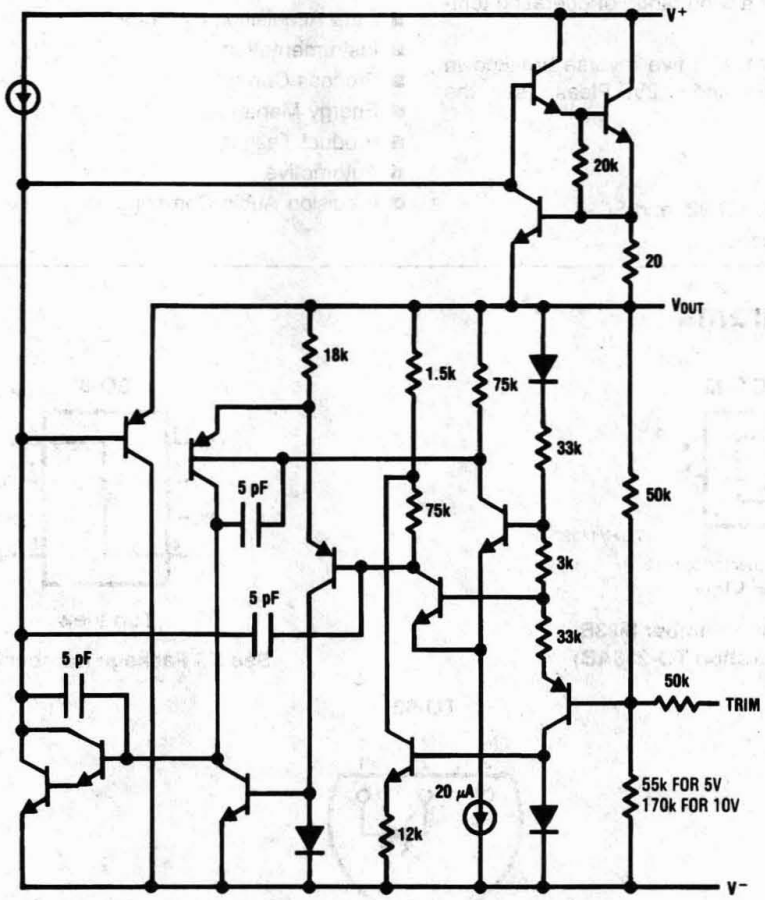
Typical Applications (Continued)

Buffered High-Current Reference with Filter



TL/H/5522–18

Simplified Schematic Diagram



TL/H/5522–6

*Reg. U.S. Pat. Off.

National Semiconductor

LM4040
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4040 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4040's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4040 easy to use. Further reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 μA for the LM4040-2.5 to 100 μA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

The LM4040 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Also available is the LM4041 with two reverse breakdown voltage versions: adjustable and 1.2V. Please see the LM4041 data sheet.

Features

- Small packages: SOT-23, TO-92, and SO-8
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V
- Contact National Semiconductor Analog Marketing for parts with extended temperature range

Key Specifications (LM4040-2.5)

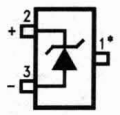
- Output voltage tolerance (A grade, 25°C) ±0.1% (max)
- Low output noise (10 Hz to 10 kHz) 35 μV_{rms} (typ)
- Wide operating current range 60 μA to 15 mA
- Industrial temperature range −40°C to +85°C
- Low temperature coefficient 100 ppm/°C (max)
- Contact National Semiconductor Analog Marketing for parts with lower temperature coefficient

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams

SOT-23



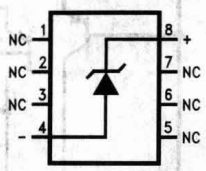
TL/H/11323–1

*This pin must be left floating or connected to pin 3.

Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)

SO-8

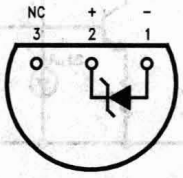


TL/H/11323–2

Top View

See NS Package Number M08A

TO-92



TL/H/11323–3

Bottom View

See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package		
	M3 (SOT-23)	**Z (TO-92)**	**M (SO-8)**
±0.1%, 100 ppm/°C max (A grade)	LM4040AIM3-2.5, LM4040AIM3-4.1, LM4040AIM3-5.0, LM4040AIM3-8.2, LM4040AIM3-10.0 **See NS Package Number M03B**	LM4040AIZ-2.5, LM4040AIZ-4.1, LM4040AIZ-5.0, LM4040AIZ-8.2, LM4040AIZ-10.0 **See NS Package Number Z03A**	LM4040AIM-2.5, LM4040AIM-4.1, LM4040AIM-5.0, LM4040AIM-8.2, LM4040AIM-10.0 **See NS Package Number M08A**
±0.2%, 100 ppm/°C max (B grade)	LM4040BIM3-2.5, LM4040BIM3-4.1, LM4040BIM3-5.0, LM4040BIM3-8.2, LM4040BIM3-10.0 **See NS Package Number M03B**	LM4040BIZ-2.5, LM4040BIZ-4.1, LM4040BIZ-5.0, LM4040BIZ-8.2, LM4040BIZ-10.0 **See NS Package Number Z03A**	LM4040BIM-2.5, LM4040BIM-4.1, LM4040BIM-5.0, LM4040BIM-8.2, LM4040BIM-10.0 **See NS Package Number M08A**
±0.5%, 100 ppm/°C max (C grade)	LM4040CIM3-2.5, LM4040CIM3-4.1, LM4040CIM3-5.0, LM4040CIM3-8.2, LM4040CIM3-10.0 **See NS Package Number M03B**	LM4040CIZ-2.5, LM4040CIZ-4.1, LM4040CIZ-5.0, LM4040CIZ-8.2, LM4040CIZ-10.0 **See NS Package Number Z03A**	LM4040CIM-2.5, LM4040CIM-4.1, LM4040CIM-5.0, LM4040CIM-8.2, LM4040CIM-10.0 **See NS Package Number M08A**
±1.0%, 150 ppm/°C max (D grade)	LM4040DIM3-2.5, LM4040DIM3-4.1, LM4040DIM3-5.0, LM4040DIM3-8.2, LM4040DIM3-10.0 **See NS Package Number M03B**	LM4040DIZ-2.5, LM4040DIZ-4.1, LM4040DIZ-5.0, LM4040DIZ-8.2, LM4040DIZ-10.0, **See NS Package Number Z03A**	LM4040DIM-2.5, LM4040DIM-4.1, LM4040DIM-5.0, LM4040DIM-8.2, LM4040DIM-10.0 **See NS Package Number M08A**
±2.0%, 150 ppm/°C max (E grade)	LM4040EIM3-2.5 **See NS Package Number M03B**	LM4040EIZ-2.5 **See NS Package Number Z03A**	

SOT-23 Package Marking Information

Only three fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
R2A R4A R5A R8A R0A	First Field: R = Reference Second Field: 2 = 2.500V Voltage Option 4 = 4.096V Voltage Option 5 = 5.000V Voltage Option 8 = 8.192V Voltage Option 0 = 10.000V Voltage Option Third Field: A–E = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance A = ±0.1%, B = ±0.2%, C = +0.5%, D = ±1.0%, E = ±2.0%
R2B R4B R5B R8B R0B	
R2C R4C R5C R8C R0C	
R2D R4D R5D R8D R0D	
R2E	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Power Dissipation (T_A = 25°C) (Note 2)	
M Package	540 mW
M3 Package	306 mW
Z Package	550 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
M and M3 Packages	
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Z Package	
Soldering (10 seconds)	+260°C
ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	$-40°C \le T_A \le +85°C$
Reverse Current	
LM4040-2.5	60 μA to 15 mA
LM4040-4.1	68 μA to 15 mA
LM4040-5.0	74 μA to 15 mA
LM4040-8.2	91 μA to 15 mA
LM4040-10.0	100 μA to 15 mA

LM4040-2.5

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±2.5 **±19**	±5.0 **±21**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±20 ±15 ±15	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.3	 0.8 **1.0**	 0.8 **1.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5	 6.0 **8.0**	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.3	 0.8	 0.8	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

4

LM4040-2.5 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C, D and E designate initial Reverse Breakdown Voltage tolerances of ±0.5%, ±1.0% and ±2.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	LM4040EIM3 LM4040EIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500				V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±12 **±29**	±25 **±49**	±50 **±74**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	 65 **70**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±20 ±15 ±15	 **±100**	 **±150**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.4	 0.8 **1.0**	 1.0 **1.2**	 1.0 **1.2**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5	 6.0 **8.0**	 8.0 **10.0**	 8.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz I_{AC} = 0.1 I_R	0.3	 0.9	 1.1	 1.1	Ω Ω(max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35				μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120				ppm

LM4040-4.1

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	4.096			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±4.1 **±31**	±8.2 **±35**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 68 **73**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.5	 0.9 **1.2**	 0.9 **1.2**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	3.0	 7.0 **10.0**	 7.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R	0.5	1.0	1.0	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-4.1 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	4.096			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±20 **±47**	±41 **±81**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 73 **78**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 0.9 **1.2**	 1.2 **1.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.0	 7.0 **10.0**	 9.0 **13.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.0	 1.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-5.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	5.000			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±5.0 **±38**	±10 **±43**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 74 **80**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.5	 1.0 **1.4**	 1.0 **1.4**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	3.5	 8.0 **12.0**	 8.0 **12.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.1	 1.1	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	40			ppm

LM4040-5.0 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	5.000			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±25 **±58**	±50 **±99**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 79 **85**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 1.0 **1.3**	 1.3 **1.8**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.5	 8.0 **12.0**	 10.0 **15.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	1.1	1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-8.2

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	8.192			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±8.2 **±61**	±16 **±70**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 91 **95**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.6	 1.3 **2.5**	 1.3 **2.5**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	7.0	 10.0 **18.0**	 10.0 **18.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.6	 1.5	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	130			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-8.2 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	8.192			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±41 **±94**	±82 **±162**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 96 **100**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	**±100**	**±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.6	 1.3 **2.5**	 1.7 **3.0**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	7.0	 10.0 **18.0**	 15.0 **24.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.6	1.5	1.9	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	130			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-10.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	10.00			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±10 **±75**	±20 **±85**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 100 **103**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	**±100**	**±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.8	 1.5 **3.5**	 1.6 **3.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	8.0	 12.0 **23.0**	 12.0 **23.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.7	 1.7	 1.7	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	180			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-10.0 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	10.00			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±50 **±115**	±100 **±198**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 110 **113**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.8	 1.5 **3.5**	 2.0 **4.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	8.0	 12.0 **23.0**	 18.0 **29.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.7	 1.7	 2.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	180			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4040, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 185°C/W for the M package, 326°C/W for the SOT-23 package, and 180°C/W with 0.4″ lead length and 170°C/W with 0.125″ lead length for the TO-92 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at T_J = 25°C and represent most likely parametric norm.

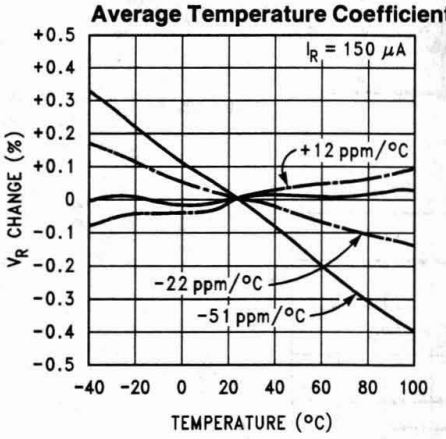
Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ± $[(\Delta V_R/\Delta T)(65°C)(V_R)]$. $\Delta V_R/\Delta T$ is the V_R temperature coefficient, 65°C is the temperature range from −40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades is shown below:

A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C
Therefore, as an example, the A-grade LM4040-2.5 has an over-temperature Reverse Breakdown Voltage tolerance of ±2.5V × 0.75% = ±19 mV.

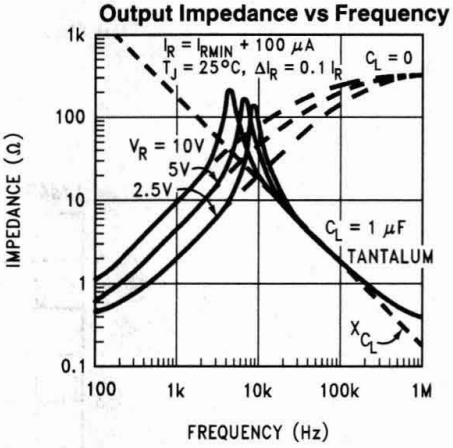
Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



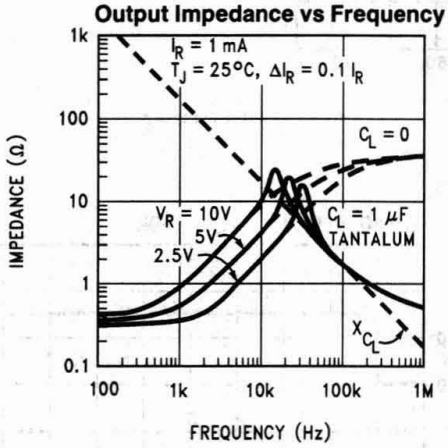
TL/H/11323-4

Output Impedance vs Frequency



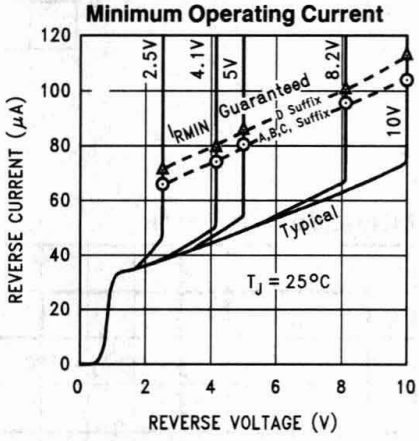
TL/H/11323-10

Output Impedance vs Frequency



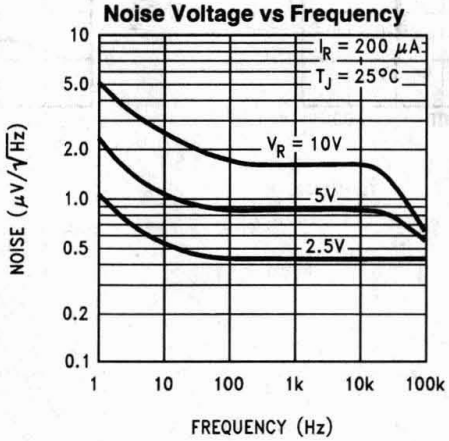
TL/H/11323-11

Reverse Characteristics and Minimum Operating Current



TL/H/11323-12

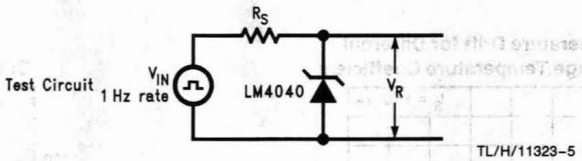
Noise Voltage vs Frequency



TL/H/11323-13

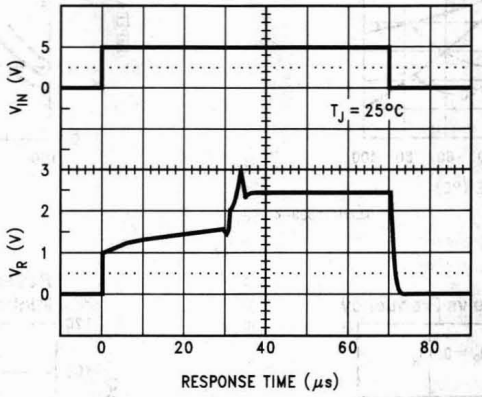
4

Start-Up Characteristics



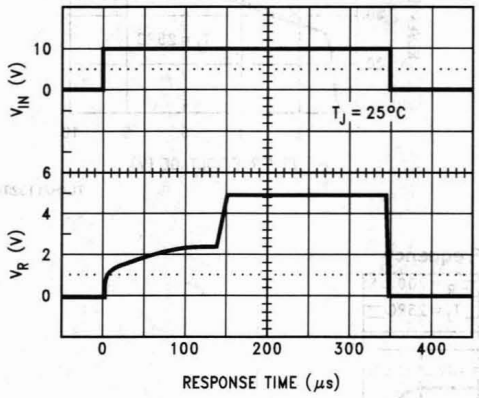
TL/H/11323-5

LM4040-2.5 R_S = 30k



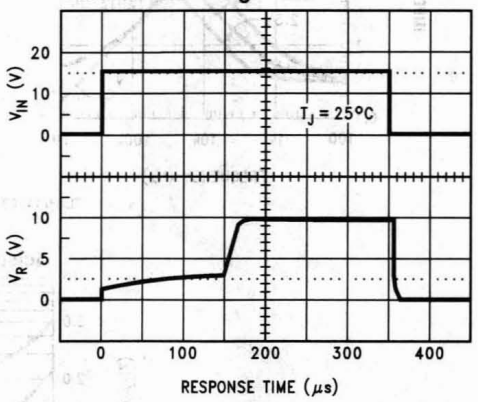
TL/H/11323-7

LM4040-5.0 R_S = 30k



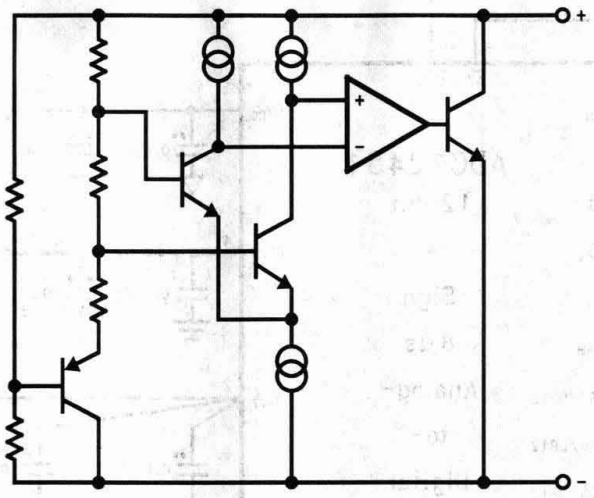
TL/H/11323-8

LM4040-10.0 R_S = 30k



TL/H/11323-9

Functional Block Diagram



TL/H/11323–14

Applications Information

The LM4040 is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4040 is available in the sub-miniature SOT-23 surface-mount package. The LM4040 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4040 remains stable. Reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 μA for the LM4040-2.5 to 100 μA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

LM4040s in the SOT-23 packages have a parasitic Schottky diode between pin 3 (−) and pin 1 (Die attach interface contact). Therefore, pin 1 of the SOT-23 package must be left floating or connected to pin 3.

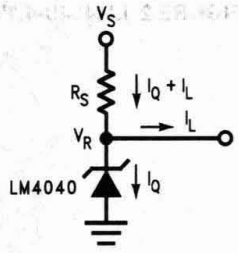
The 4.096V version allows single +5V 12-bit ADCs or DACs to operate with an LSB equal to 1 mV. For 12-bit ADCs or DACs that operate on supplies of 10V or greater, the 8.192V version gives 2 mV per LSB.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4040. R_S determines the current that flows through the load (I_L) and the LM4040 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4040 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4040 is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4040's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

Typical Applications



TL/H/11323–15

FIGURE 1. Shunt Regulator

Typical Applications (Continued)

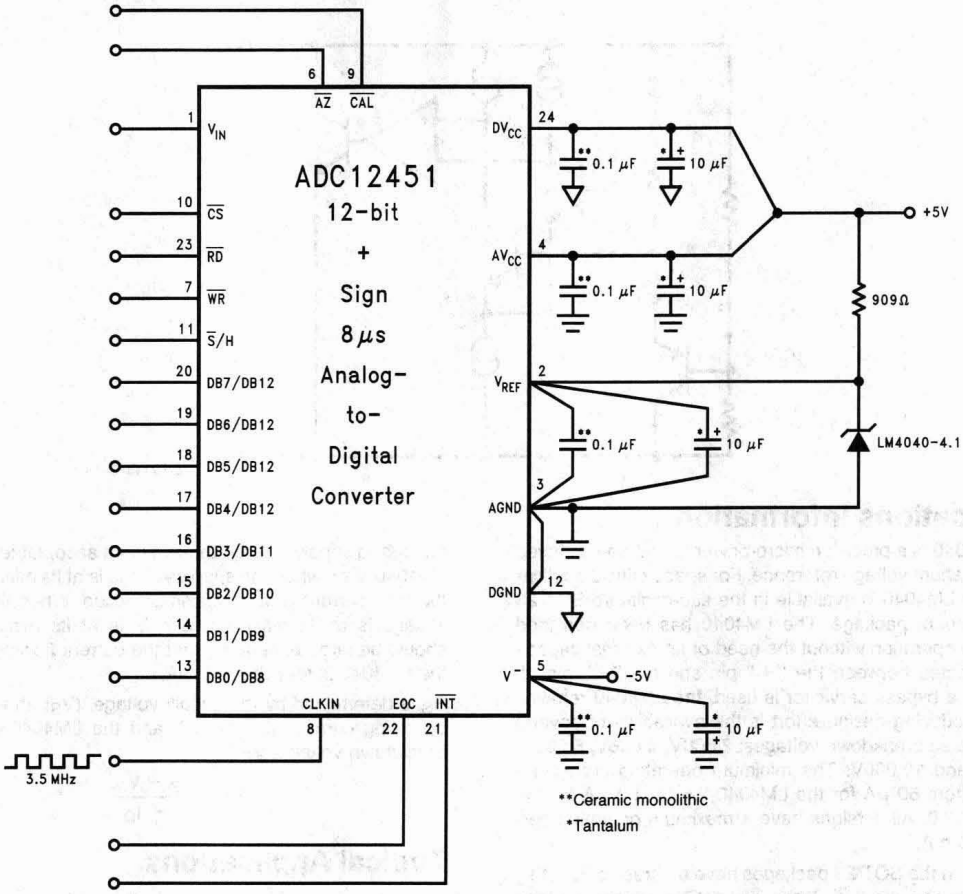
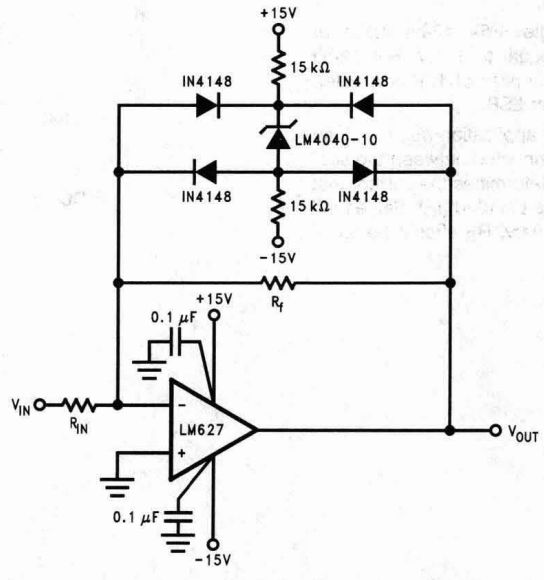


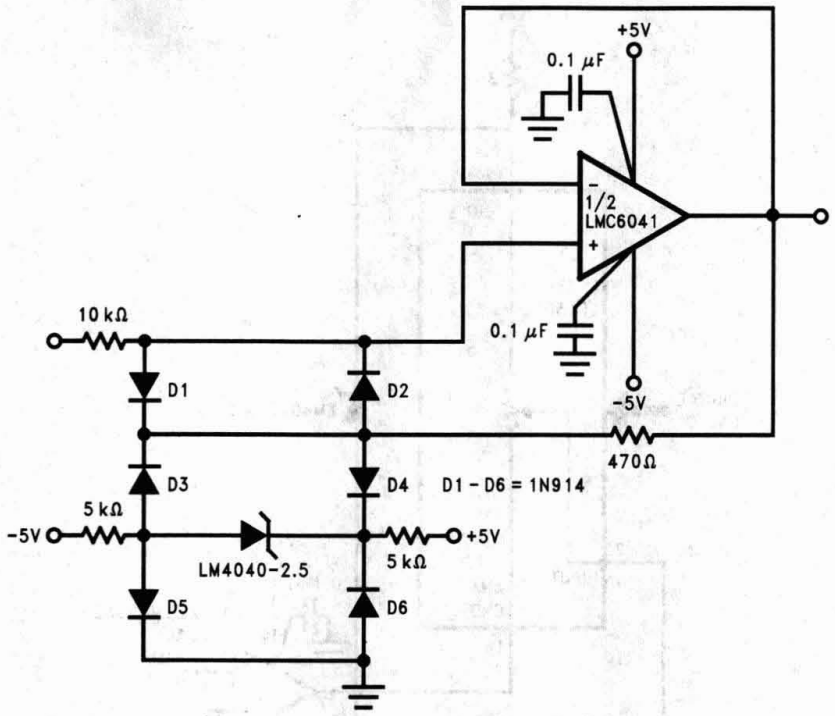
FIGURE 2. LM4040-4.1's Nominal 4.096 breakdown voltage gives ADC12451 1 mV/LSB TL/H/11323-16



TL/H/11323-17

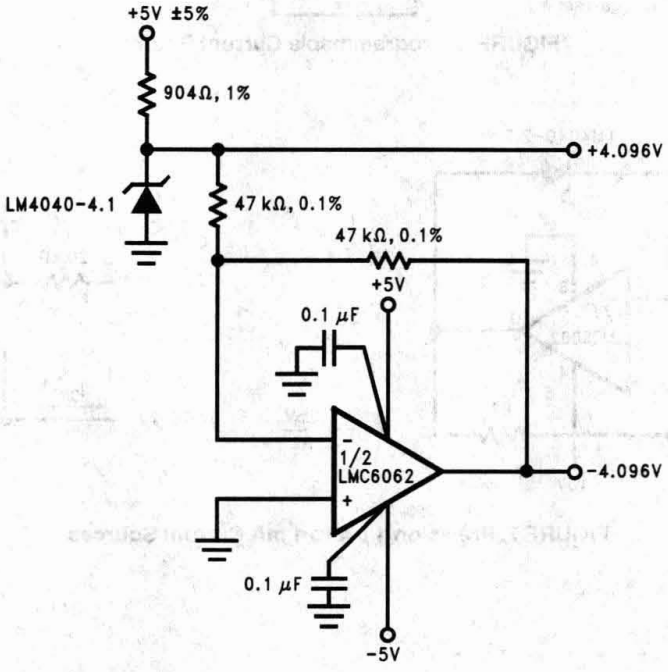
FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is ±11.5V (LM4040's reverse breakdown voltage + 2 diode V_F).

Typical Applications (Continued)



TL/H/11323–18

FIGURE 4. Protecting Op Amp input. The bounding voltage is ±4V with the LM4040-2.5 (LM4040's reverse breakdown voltage + 3 diode V_F).



TL/H/11323–19

FIGURE 5. Precision ±4.096V Reference

Typical Applications (Continued)

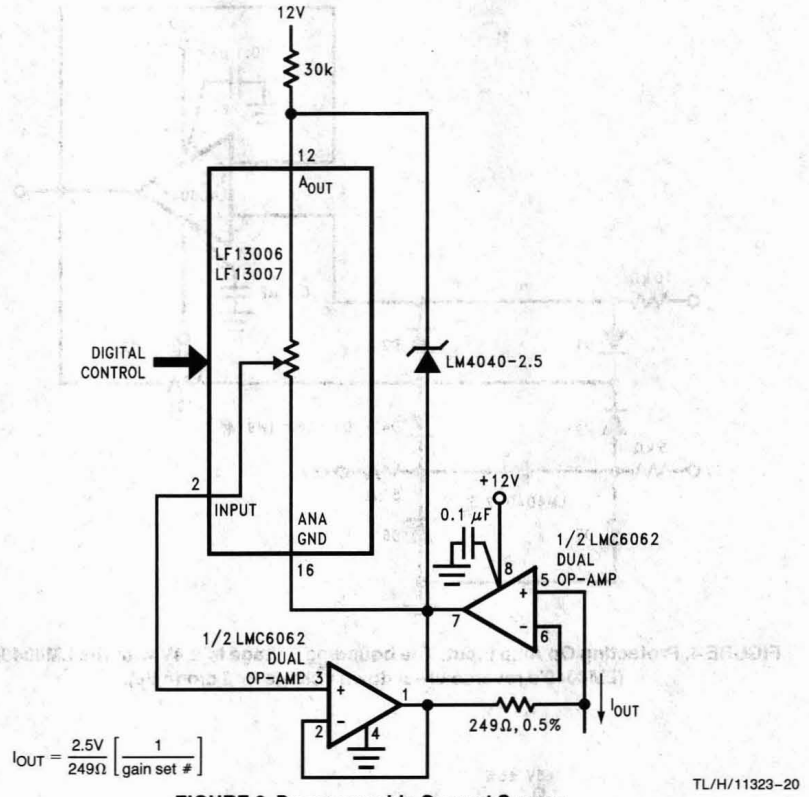


FIGURE 6. Programmable Current Source

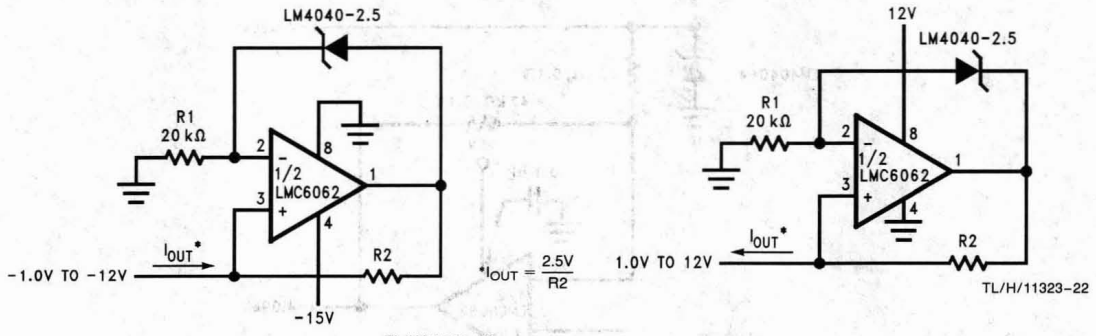


FIGURE 7. Precision 1 μA to 1 mA Current Sources

National Semiconductor

LM4041
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4041 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4041's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4041 easy to use. Further reducing design effort is the availability of a fixed (1.225V) and adjustable reverse breakdown voltage. The minimum operating current is 60 μA for the LM4041-1.2 and the LM4041-ADJ. Both versions have a maximum operating current of 12 mA.

The LM4041 utilizes fuse and zener-zap reverse breakdown or reference voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features

- Small packages: SOT-23, TO-92, and SO-8
- No output capacitor required
- Tolerates capacitive loads
- Reverse breakdown voltage options of 1.225V and adjustable
- Contact National Semiconductor Analog Marketing for parts with extended temperature range

Key Specifications (LM4041-1.2)

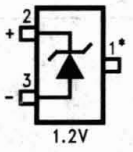
- Output voltage tolerance (A grade, 25°C) ±0.1% (max)
- Low output noise (10 Hz to 10 kHz) 20 μV_{rms} (typ)
- Wide operating current range 60 μA to 12 mA
- Industrial temperature range −40°C to +85°C
- Low temperature coefficient 100 ppm/°C (max)

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams

SOT-23

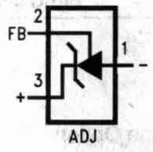


TL/H/11392-1

*This pin must be left floating or connected to pin 3.

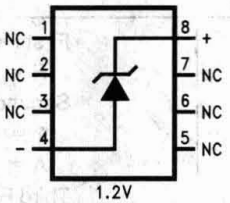
Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)



TL/H/11392-40

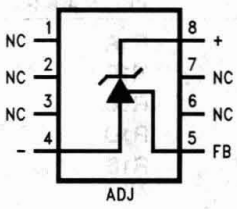
SO-8



TL/H/11392-2

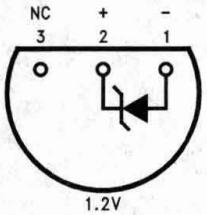
Top View

See NS Package Number M08A

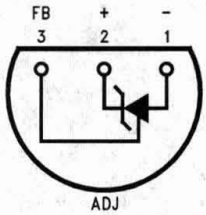


TL/H/11392-31

TO-92



TL/H/11392-3



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Bottom View
See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package		
	M3 (SOT-23)	Z (TO-92)	M (SO-8)
±0.1%, 100 ppm/°C max (A grade)	LM4041AIM3-1.2 **See NS Package Number M03B**	LM4041AIZ-1.2 **See NS Package Number Z03A**	LM4041AIM-1.2 **See NS Package Number M08A**
±0.2%, 100 ppm/°C max (B grade)	LM4041BIM3-1.2 **See NS Package Number M03B**	LM4041BIZ-1.2 **See NS Package Number Z03A**	LM4041BIM-1.2 **See NS Package Number M08A**
±0.5%, 100 ppm/°C max (C grade)	LM4041CIM3-1.2 LM4041CIM3-ADJ **See NS Package Number M03B**	LM4041CIZ-1.2, LM4041CIZ-ADJ **See NS Package Number Z03A**	LM4041CIM-1.2, LM4041CIM-ADJ **See NS Package Number M08A**
±1.0%, 150 ppm/°C max (D grade)	LM4041DIM3-1.2 LM4041DIM3-ADJ **See NS Package Number M03B**	LM4041DIZ-1.2, LM4041DIZ-ADJ **See NS Package Number Z03A**	LM4041DIM-1.2, LM4041DIM-ADJ **See NS Package Number M08A**
±2.0%, 150 ppm/°C max (E grade)	LM4041EIM3-1.2 **See NS Package Number M03B**	LM4041EIZ-1.2 **See NS Package Number Z03A**	

SOT-23 Package Marking Information

Only three fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
R1A R1B R1C R1D R1E	First Field: R = Reference Second Field: 1 = 1.225V Voltage Option A = Adjustable Third Field: A–E = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance A = ±0.1%, B = ±0.2%, C = ±0.5%, D = ±1.0%, E = ±2.0%
RAC RAD	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Maximum Output Voltage (LM4041-ADJ)	15V
Power Dissipation (T_A = 25°C) (Note 2)	
M Package	540 mW
M3 Package	306 mW
Z Package	550 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
M and M3 Packages	
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Z Package	
Soldering (10 seconds)	+260°C
ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	$-40°C \le T_A \le +85°C$
Reverse Current	
LM4041-1.2	60 μA to 12 mA
LM4041-ADJ	60 μA to 12 mA
Output Voltage Range	
LM4041-ADJ	1.24V to 10V

LM4041-1.2

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041AIM LM4041AIM3 LM4041AIZ Limits (Note 5)	LM4041BIM LM4041BIM3 LM4041BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	1.225			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±1.2 **±9.2**	±2.4 **±10.4**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±20 ±15 ±15	**±100**	**±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.7	 1.5 **2.0**	 1.5 **2.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 12 mA	4.0	 6.0 **8.0**	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.5	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	20			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4041-1.2 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C, D and E designate initial Reverse Breakdown Voltage tolerances of ±0.5%, ±1.0% and ±2.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ Limits (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ Limits (Note 5)	LM4041EIM3 LM4041EIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 µA	1.225				V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 µA		±6 **±14**	±12 **±24**	±25 **±36**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	 65 **70**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 µA	±20 ±15 ±15	 **±100**	 **±150**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.7	 1.5 **2.0**	 2.0 **25**	 2.0 **2.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 12 mA	2.5	 6.0 **8.0**	 8.0 **10.0**	 8.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz $I_{AC} = 0.1\ I_R$	0.5	 1.5	 2.0	 2.0	Ω Ω(max)
e_N	Wideband Noise	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz	20				μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 µA	120				ppm

LM4041-ADJ (Adjustable)

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$ unless otherwise specified (SOT-23, see Note 7), $I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10V$. The grades C and D designates initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for V_{OUT} = 5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ (Note 5)	Units (Limit)
V_{REF}	Reference Voltage	I_R = 100 µA, V_{OUT} = 5V	1.233			V
	Reference Voltage Tolerance (Note 8)	I_R = 100 µA, V_{OUT} = 5V		±6.2 **±14**	±12 **±24**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	µA µA (max) µA (max)

LM4041-ADJ (Adjustable) (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$ unless otherwise specified (SOT-23, see Note 7), $I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10V$. The grades C and D designates initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for $V_{OUT} = 5V$.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ (Note 5)	Units (Limit)
$\Delta V_{REF}/\Delta I_R$	Reference Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA SOT-23: $V_{OUT} \ge 1.6V$ (Note 7)	0.7	1.5 **2.0**	2.0 **2.5**	mV mV (max) mV (max)
		1 mA $\le I_R \le$ 12 mA SOT-23: $V_{OUT} \ge 1.6V$ (Note 7)	2	4 **6**	6 **8**	mV mV (max) mV (max)
$\Delta V_{REF}/\Delta V_O$	Reference Voltage Change with Output Voltage Change	$I_R = 1$ mA	−1.3	−2.0 **−2.5**	−2.5 **−3.0**	mV/V mV/V (max) mV/V (max)
I_{FB}	Feedback Current		60	100 **120**	150 **200**	nA nA (max) nA (max)
$\Delta V_{REF}/\Delta T$	Average Reference Voltage Temperature Coefficient (Note 8)	$V_{OUT} = 5V$, $I_R = 10$ mA $I_R = 1$ mA $I_R = 100\ \mu A$	20 15 15	**±100**	**±150**	ppm/°C ppm/°C (max) ppm/°C
Z_{OUT}	Dynamic Output Impedance	$I_R = 1$ mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$ $V_{OUT} = V_{REF}$ $V_{OUT} = 10V$	 0.3 2			 Ω Ω
e_N	Wideband Noise	$I_R = 100\ \mu A$ $V_{OUT} = V_{REF}$ 10 Hz ≤ f ≤ 10 kHz	20			μV_{rms}
ΔV_{REF}	Reference Voltage Long Term Stability	t = 1000 hrs, $I_R = 100\ \mu A$ T = 25°C ±0.1°C	120			ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4041, $T_{Jmax} = 125°C$, and the typical thermal resistance (θ_{JA}), when board mounted, is 185°C/W for the M package, 326°C/W for the SOT-23 package, and 180°C/W with 0.4" lead length and 170°C/W with 0.125" lead length for the TO-92 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ±[($\Delta V_R/\Delta T$)(65°C)(V_R)]. $\Delta V_R/\Delta T$ is the V_R temperature coefficient, 65°C is the temperature range from −40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades is shown below:

A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C

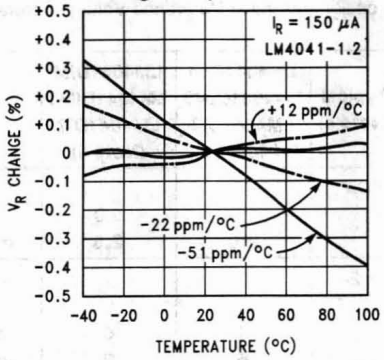
Therefore, as an example, the A-grade LM4041-1.2 has an over-temperature Reverse Breakdown Voltage tolerance of ±1.2V × 0.75% = ±9.2 mV.

Note 7. When $V_{OUT} \le 1.6V$, the LM4041-ADJ in the SOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (-) output and the package (-) output pin. See the Output Saturation (SOT-23 only) curve in the Typical Performance Characteristics section.

Note 8. Reference voltage and temperature coefficient will change with output voltage. See Typical Performance Characteristics curves.

Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



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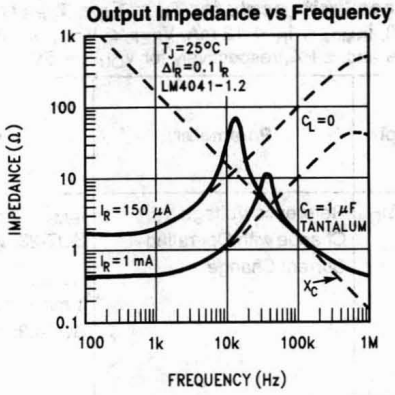
Output Impedance vs Frequency



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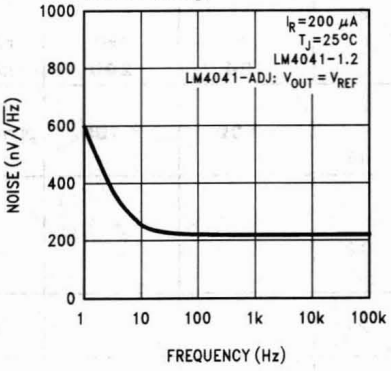
Noise Voltage



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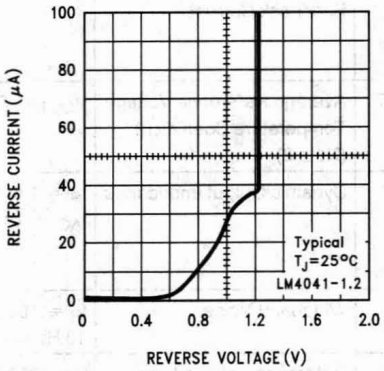
Reverse Characteristics and Minimum Operating Current



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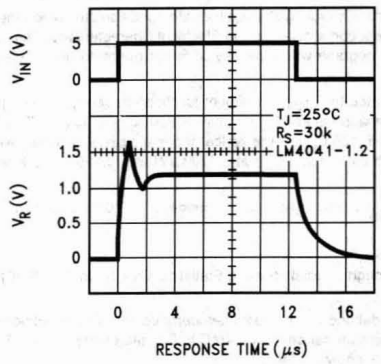

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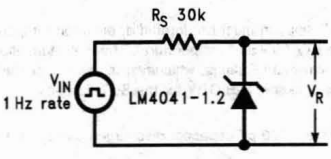

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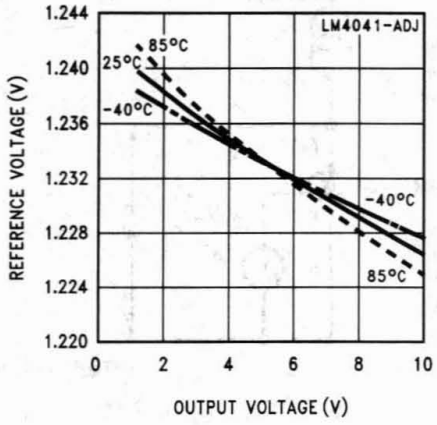
Typical Performance Characteristics (Continued)

Reference Voltage vs Output Voltage and Temperature



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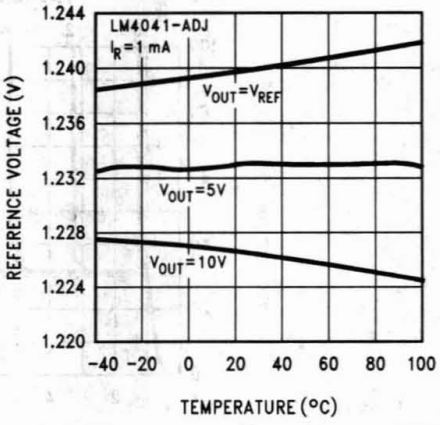
Reference Voltage vs Temperature and Output Voltage



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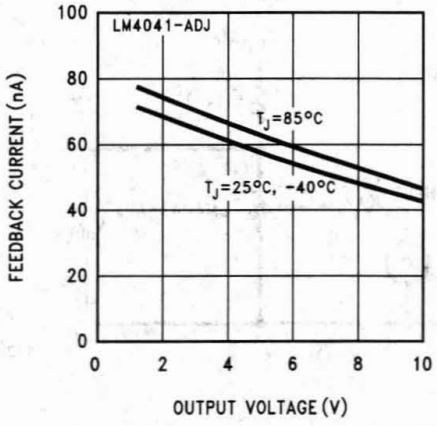
Feedback Current vs Output Voltage and Temperature



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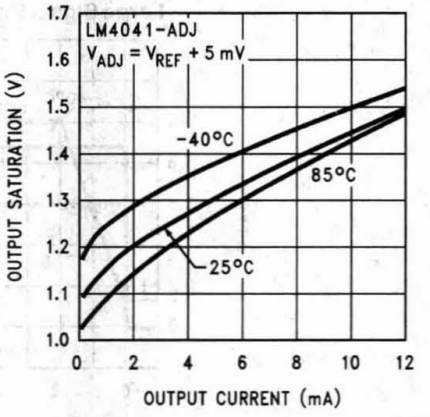
Output Saturation (SOT-23 Only)



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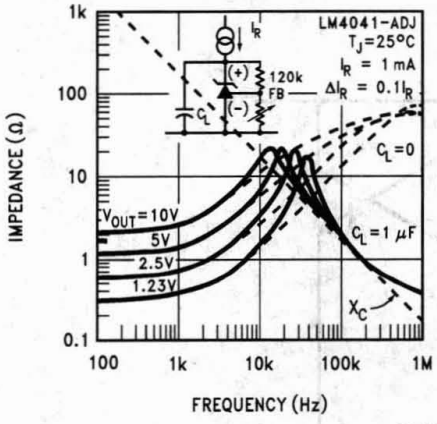
Output Impedance vs Frequency



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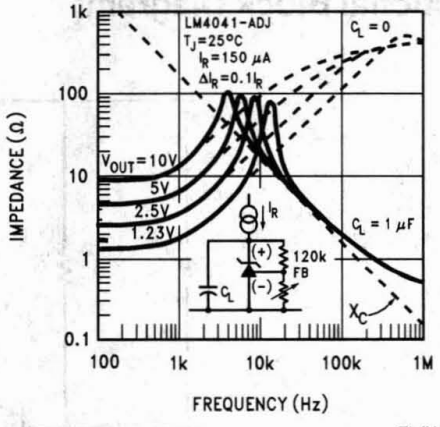
Output Impedance vs Frequency



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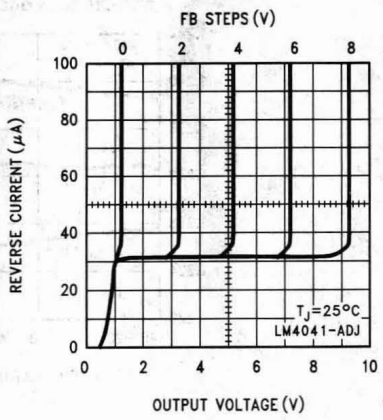
Typical Performance Characteristics (Continued)

Reverse Characteristics



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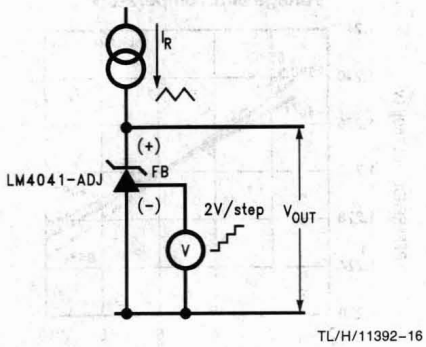

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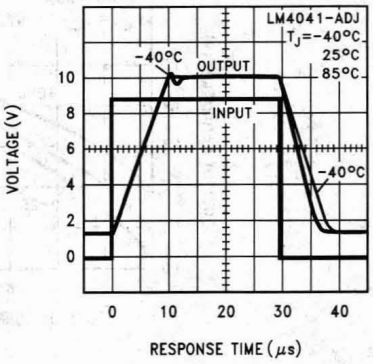
Large Signal Response



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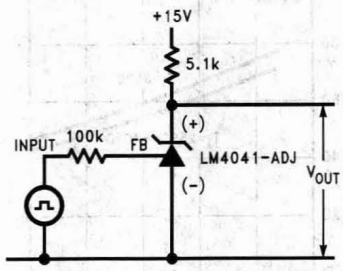

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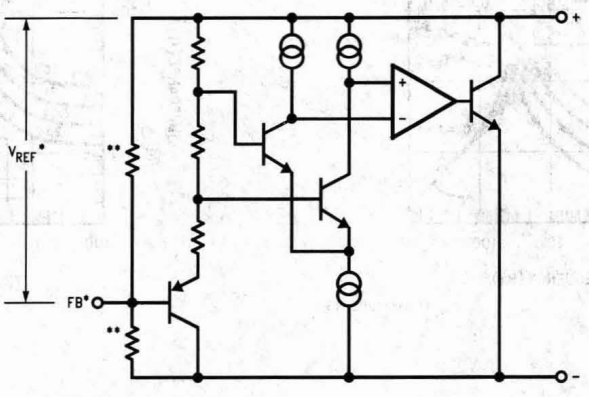
Functional Block Diagram



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*LM4041-ADJ only
**LM4041-1.2 only

Applications Information

The LM4041 is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4041 is available in the sub-miniature SOT-23 surface-mount package. The LM4041 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4041 remains stable. Design effort is further reduced with the choice of either a fixed 1.2V or an adjustable reverse breakdown voltage. The minimum operating current is 60 μA for the LM4041-1.2 and the LM4041-ADJ. Both versions have a maximum operating current of 12 mA.

LM4041s using the SOT-23 package have pin 1 connected as the (-) output through the package's die attach interface. Therefore, the LM4041-1.2's pin 1 must be left floating or connected to pin 3 and the LM4041-ADJ's pin 1 is the (-) output.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4041. R_S determines the current that flows through the load (I_L) and the LM4041 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4041 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4041 is less than 12 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4041's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

The LM4041-ADJ's output voltage can be adjusted to any value in the range of 1.24V through 10V. It is a function of the internal reference voltage (V_{REF}) and the ratio of the external feedback resistors as shown in *Figure 2*. The output is found using the equation

$$V_O = V_{REF}' \left(\frac{R2}{R1} + 1\right) \quad (1)$$

where V_O is the desired output voltage. The actual value of the internal V_{REF} is a function of V_O. The "corrected" V_{REF} is determined by

$$V_{REF}' = V_O (\Delta V_{REF}/\Delta V_O) + V_Y \quad (2)$$

where V_O is the desired output voltage. $\Delta V_{REF}/\Delta V_O$ is found in the Electrical Characteristics and it typically −1.3 mV/V and V_Y is equal to 1.240V. Replace the value of V_{REF}' in equation (1) with the value found using equation (2).

Note that the actual output voltage can deviate from that predicted using the typical $\Delta V_{REF}/\Delta V_O$ in equation (2): for C-grade parts, the worst-case $\Delta V_{REF}/\Delta V_O$ is −2.5 mV/V and V_Y = 1.246V. For D-grade parts, the worst-case $\Delta V_{REF}/\Delta V_O$ is −3.0 mV/V and V_Y = 1.248V.

The following example shows the difference in output voltage resulting from the typical and worst case values of $\Delta V_{REF}/\Delta V_O$. Let V_O = +9V. Using the typical value of $\Delta V_{REF}/\Delta V_O$, V_{REF} is 1.228V. Choosing a value of R1 = 10 kΩ, R2 = 63.272 kΩ. Using the worst case $\Delta V_{REF}/\Delta V_O$ for the C-grade and D-grade parts, the output voltage is actually 8.965V and 8.946V, respectively. This results in possible errors as large as 0.39% for the C-grade parts and 0.59% for the D-grade parts. Once again, resistor values found using the typical value of $\Delta V_{REF}/\Delta V_O$ will work in most cases, requiring no further adjustment.

Typical Applications

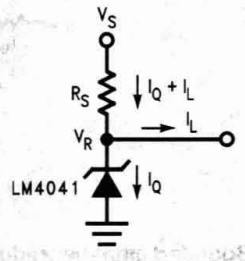

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FIGURE 1. Shunt Regulator

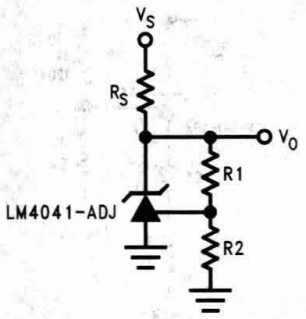

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FIGURE 2. Adjustable Shunt Regulator

4

Typical Applications (Continued)

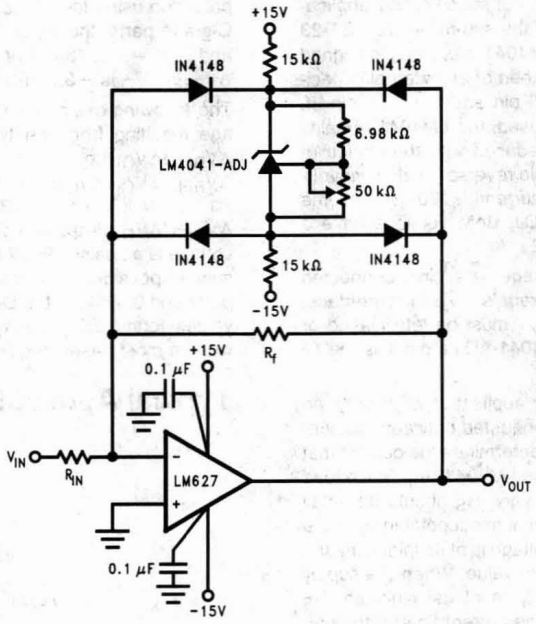

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FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is $\pm V_O$ (LM4041's reverse breakdown voltage) + 2 diode V_F.

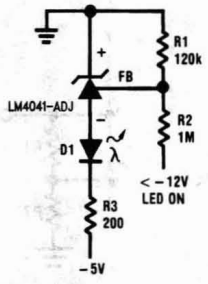

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FIGURE 4. Voltage Level Detector

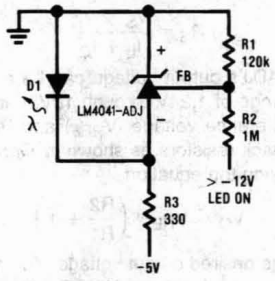

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FIGURE 5. Voltage Level Detector

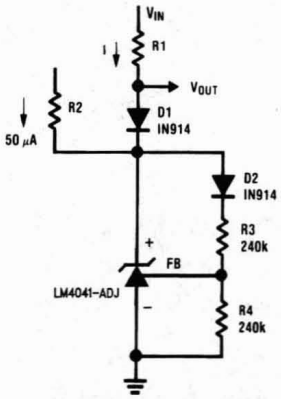

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FIGURE 6. Fast Positive Clamp
2.4V + ΔV_{D1}

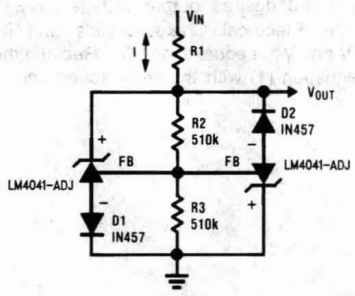

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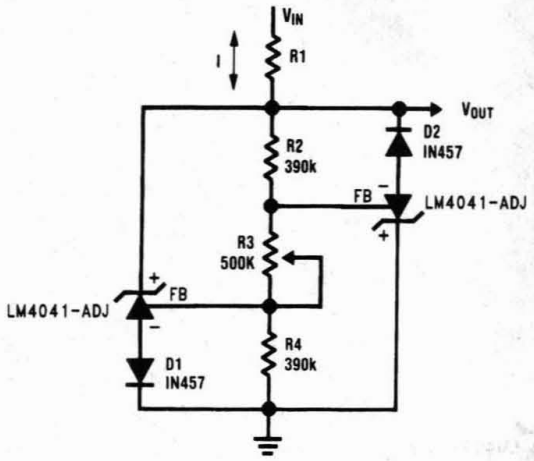
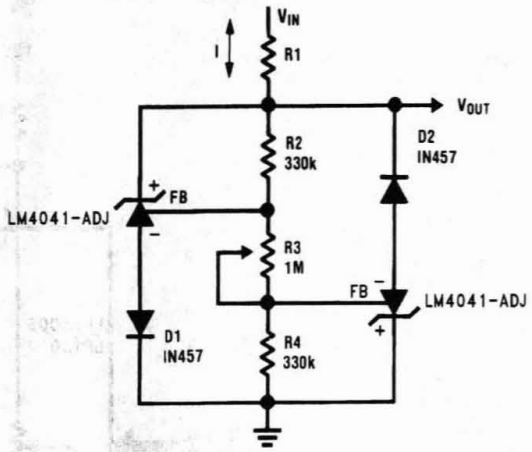
FIGURE 7. Bidirectional Clamp ±2.4V

Typical Applications (Continued)



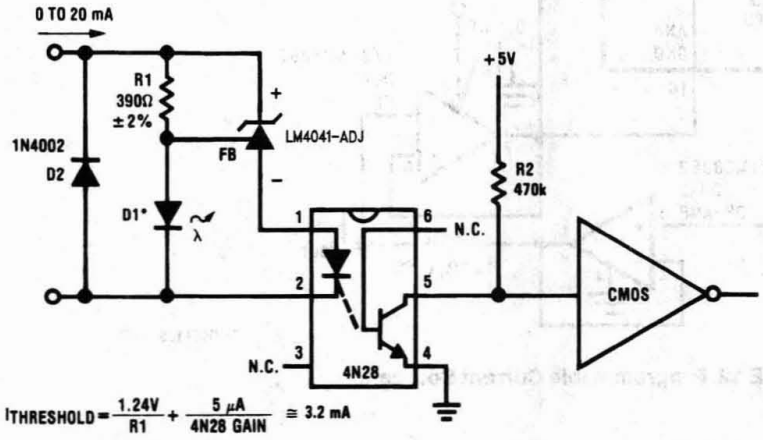
TL/H/11392–35

FIGURE 7. Bidirectional Adjustable Clamp ±18V to ±2.4V



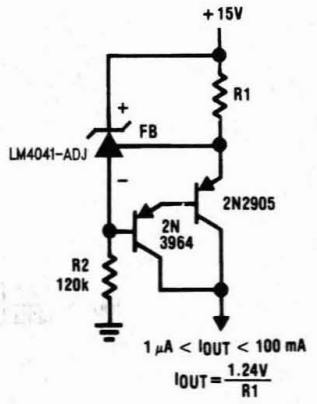
TL/H/11392–36

FIGURE 8. Bidirectional Adjustable Clamp ±2.4V to ±6V



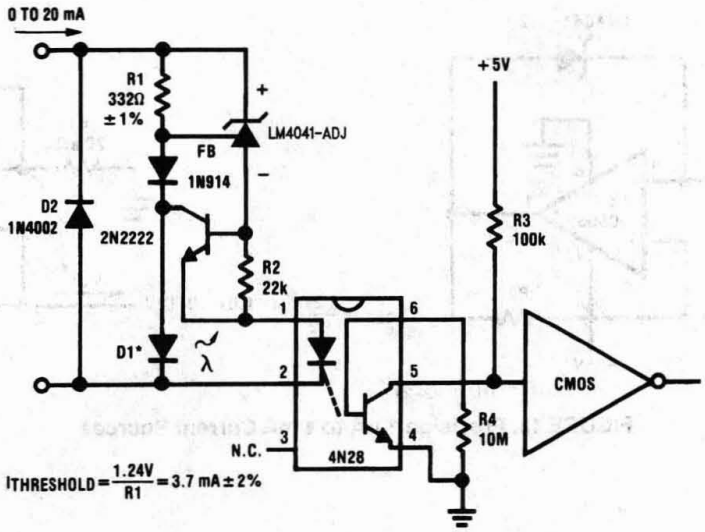
TL/H/11392–37

FIGURE 9. Simple Floating Current Detector



TL/H/11392–38

FIGURE 10. Current Source



TL/H/11392–39

FIGURE 11. Precision Floating Current Detector

*D1 can be any LED, V_F = 1.5V to 2.2V at 3 mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

Typical Applications (Continued)

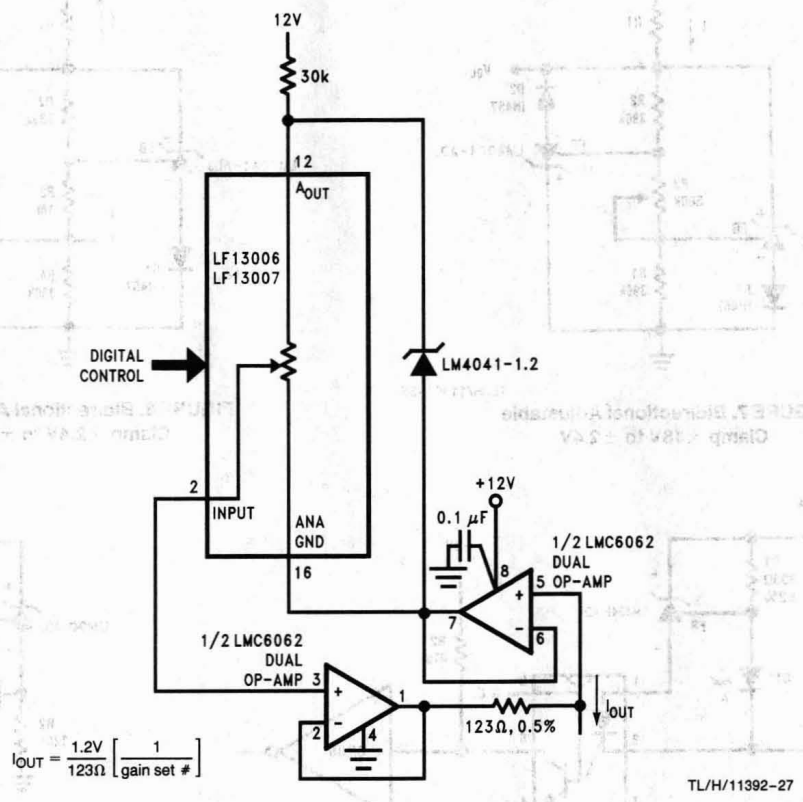


FIGURE 12. Programmable Current Source

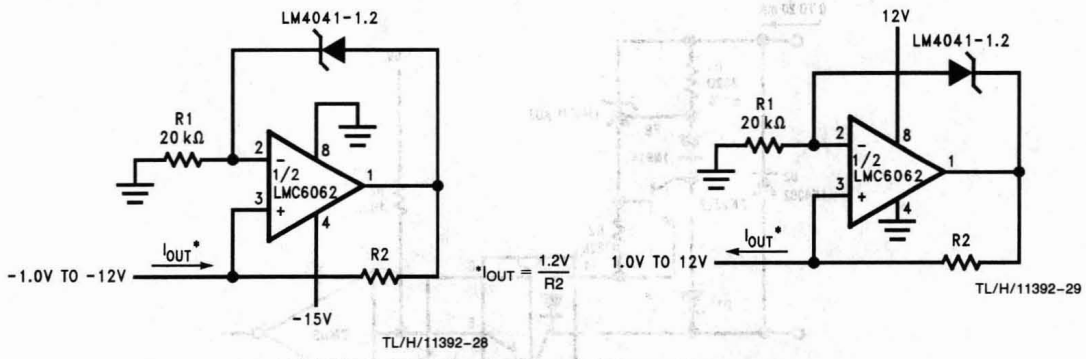


FIGURE 13. Precision 1 μA to 1 mA Current Sources

National Semiconductor

LM4431
Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4431 voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4431's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4431 easy to use. The operating current range is 100 μA to 15 mA.

The LM4431 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the parts have an accuracy of better than ±2.0% at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Key Specifications

- Output voltage tolerance 25°C ±2.0% (max)
- Low output noise (10 Hz to 10 kHz) 35 μV_{rms} (typ)
- Wide operating current range 100 μA to 15 mA
- Commercial temperature range 0°C to +70°C
- Low temperature coefficient 30 ppm/°C (typ)

Applications

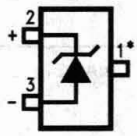
- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Power Supplies

Features

- Small package: SOT-23
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltage of 2.50V

Connection Diagram

SOT-23



TL/H/11374–1

*This pin must be left floating or connected to pin 3.

Top View

Order Number LM4431M3-2.5
See NS Package Number M03B
(JEDEC Registration TO-236AB)

SOT-23 Package Marking Information

Only three fields of marking are possible on the SOT-23's small surface. The following table gives the meaning of the three fields.

Part Marking	Field Definition
S2E	First Field: S = Reference Second Field: 2 = 2.500V Voltage Option Third Field: E = Initial Reverse Breakdown Voltage Tolerance of ±2.0%

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Power Dissipation (T_A = 25°C) (Note 2)	
M3 Package	306 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
M3 Package	
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range	
($T_{min} \le T_A \le T_{max}$)	$0°C \le T_A \le +70°C$
Reverse Current	
LM4431-2.5	100 μA to 15 mA

LM4431-2.5

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4431M3 Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500		V
	Reverse Breakdown Voltage Tolerance	I_R = 100 μA		±50	mV (max)
I_{RMIN}	Minimum Operating Current		45		μA
				100	μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA	±30		ppm/°C
		I_R = 1 mA	±30		ppm/°C
		I_R = 100 μA	±30		ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.4		mV
				1.0	mV (max)
				1.2	mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5		mV
				8.0	mV (max)
				25	mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz $I_{AC} = 0.1\ I_R$	1.0		Ω
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35		μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120		ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4431, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 326°C/W for the SOT-23 package.

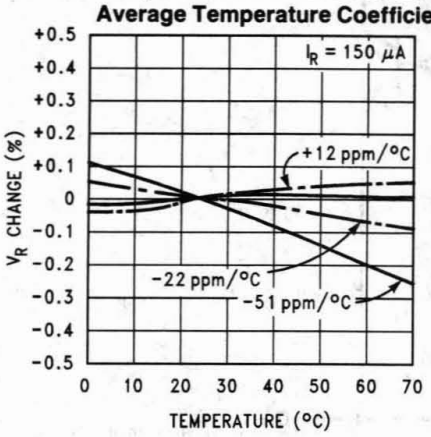
Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

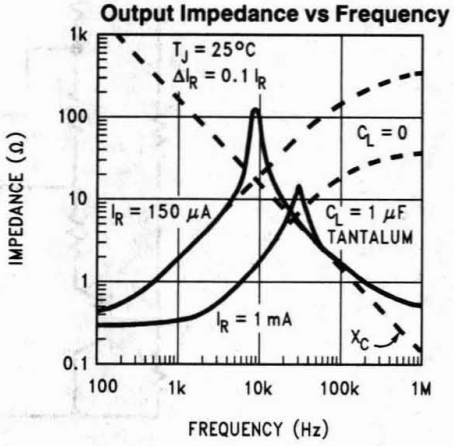
Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



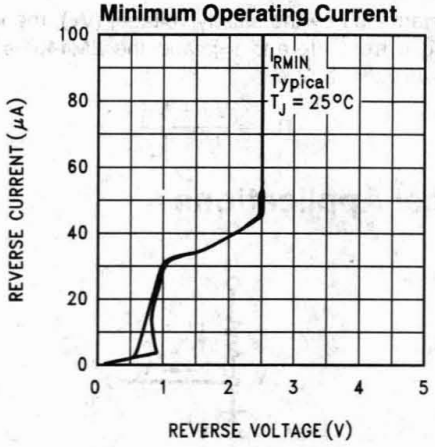
TL/H/11374–2

Output Impedance vs Frequency



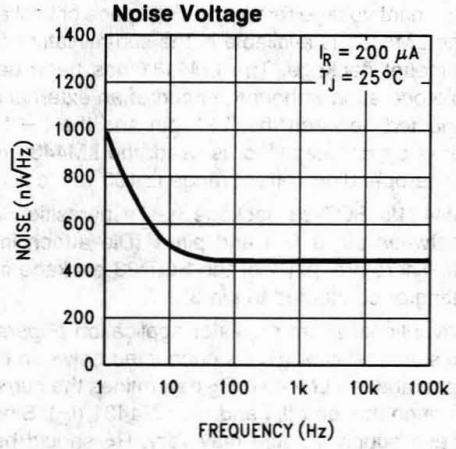
TL/H/11374–3

Reverse Characteristics and Minimum Operating Current



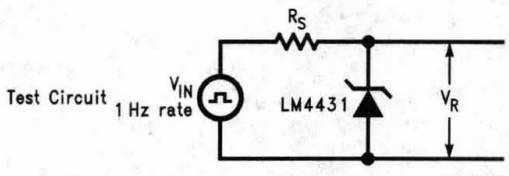
TL/H/11374–4

Noise Voltage



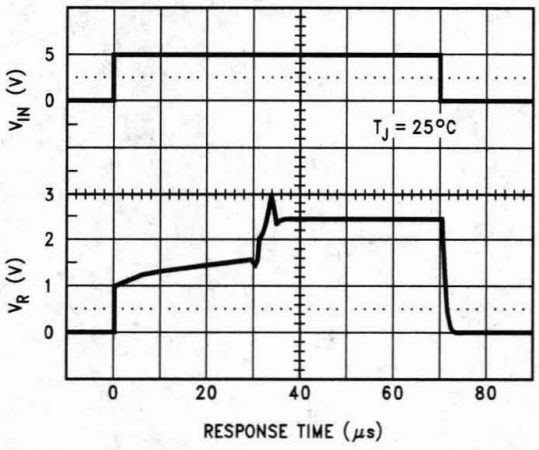
TL/H/11374–5

Start-Up Characteristics



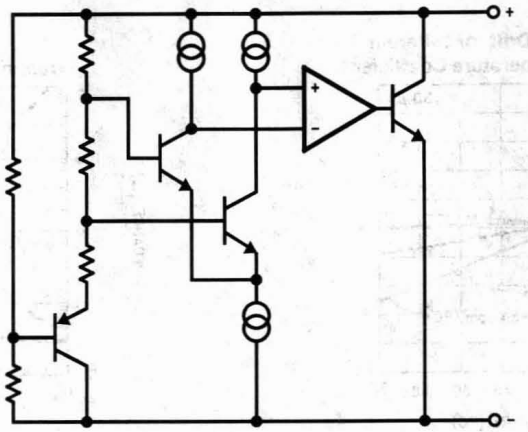
TL/H/11374–6

LM4431-2.5 R_S = 30k



TL/H/11374–7

Functional Block Diagram



TL/H/11374–8

Applications Information

The LM4431 is a micro-power curvature-corrected 2.5V bandgap shunt voltage reference. For space critical applications, the LM4431 is available in the sub-miniature SOT-23 surface-mount package. The LM4431 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4431 remains stable. The operating current range is 100 μA to 15 mA.

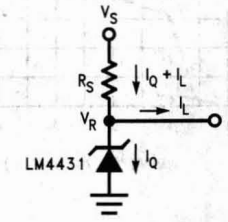
The LM4431's SOT-23 package has a parasitic Schottky diode between pin 3 (−) and pin 1 (Die attach interface contact). Therefore, pin 1 of the SOT-23 package must be left floating or connected to pin 3.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4431. R_S determines the current that flows through the load (I_L) and the LM4431 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4431 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4431 is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4431's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

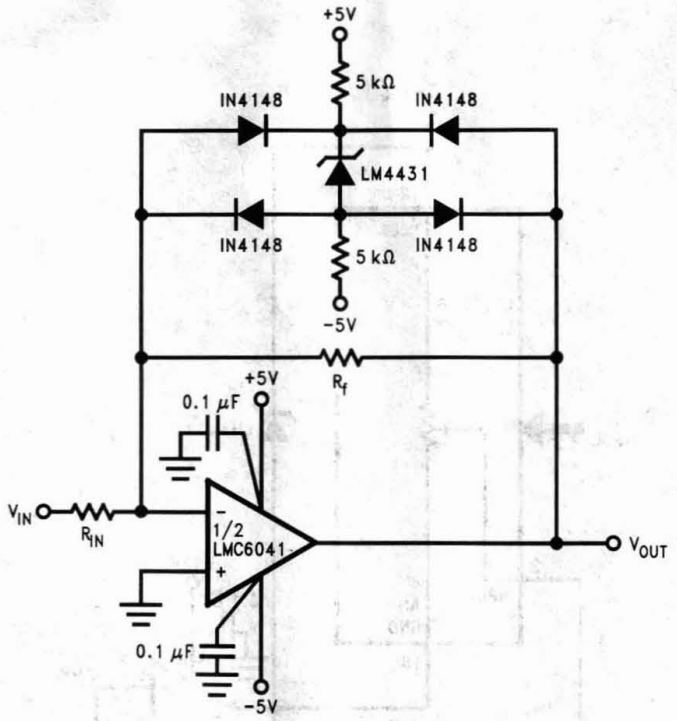
Typical Applications



TL/H/11374–9

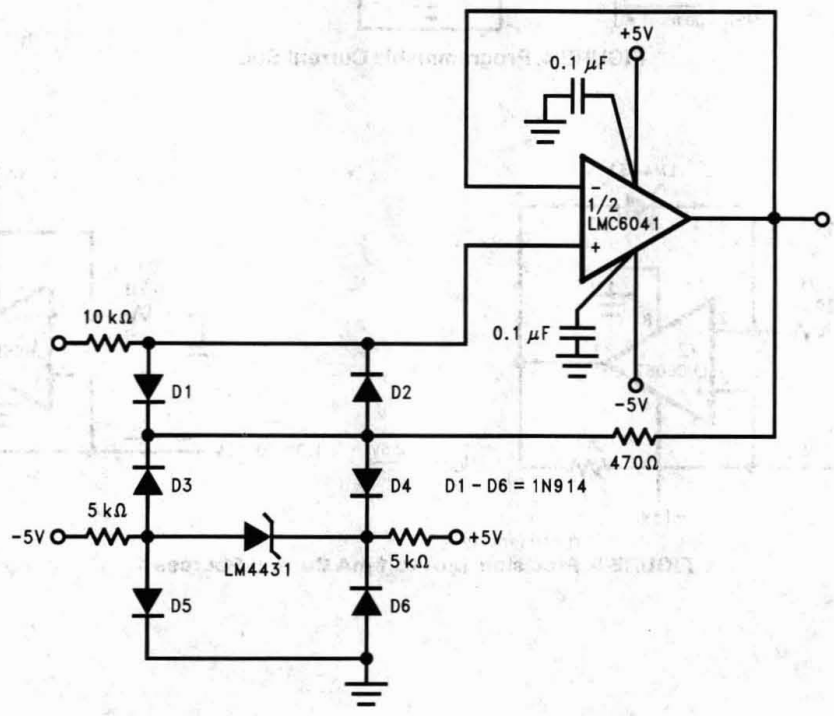
FIGURE 1. Shunt Regulator

Typical Applications (Continued)



TL/H/11374–10

FIGURE 2. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is ±3.9V (LM4431's reverse breakdown voltage + 2 diode V_F).



TL/H/11374–11

FIGURE 3. Protecting Op Amp input. The bounding voltage is ±4V with the LM4431 (LM4431's reverse breakdown voltage + 3 diode V_F).

Typical Applications (Continued)

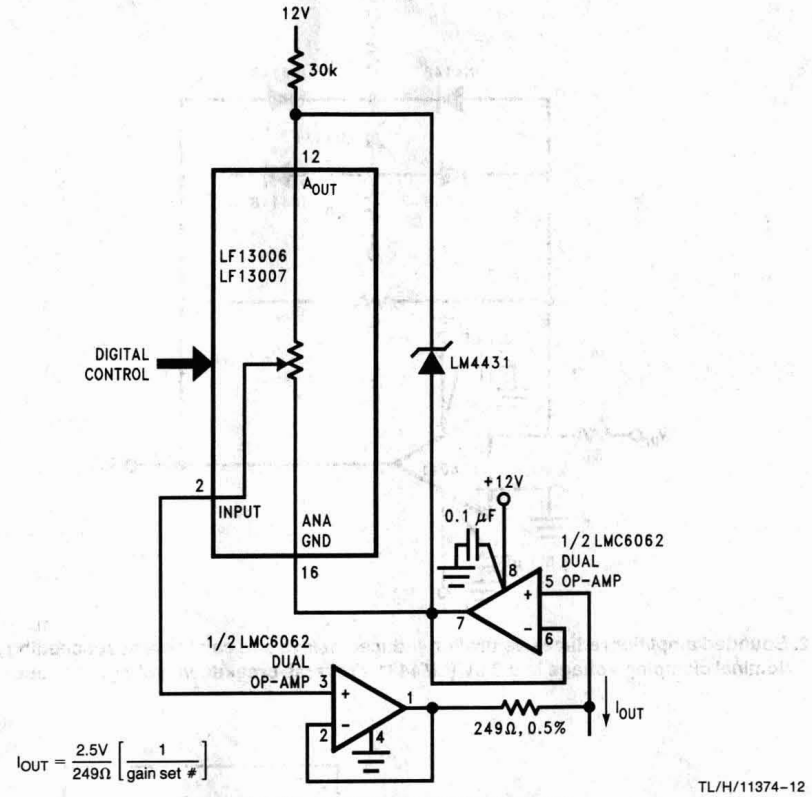


FIGURE 4. Programmable Current Source

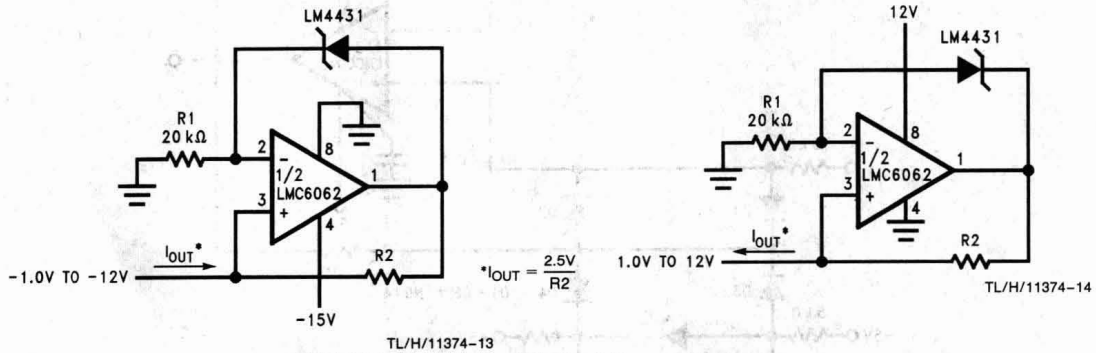


FIGURE 5. Precision 1 μA to 1 mA Current Sources

National Semiconductor

LM9140
Precision Micropower Shunt Voltage Reference

General Description

The LM9140's reverse breakdown voltage temperature coefficients of ±25 ppm/°C are ideal for precision applications. The LM9140's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM9140 easy to use. Further reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, and 10.000V. The minimum operating current increases from 60 μA for the LM9140-2.5 to 100 μA for the LM9140-10.0. All versions have a maximum operating current of 15 mA.

The LM9140 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.5% (B grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features

- Guaranteed temperature coefficient of ±25 ppm/°C
- Reverse breakdown voltage tolerance of ±0.5%
- Small package: TO-92
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 2.500V, 4.096V, 5.000V, and 10.000V

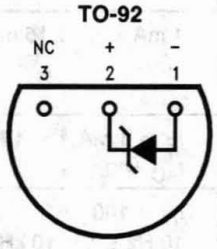
Key Specifications (LM9140-2.5)

- Temperature coefficient ±25 ppm/°C (max)
- Output voltage tolerance ±0.5% (max)
- Low output noise (10 Hz to 10 kHz) 35 μV_{rms} (typ)
- Wide operating current range 60 μA to 15 mA
- Industrial temperature range −40°C to +85°C

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams



TL/H/11393–2

Bottom View

See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Z (TO-92)
0.5%, 25 ppm/°C max	LM9140BYZ-2.5, LM9140BYZ-4.1, LM9140BYZ-5.0, LM9140BYZ-10.0

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Power Dissipation (T_A = 25°C (Note 2)	
Z Package	550 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
Z Package	
Soldering (10 seconds)	+260°C
ESD Susceptibility	
Human Boddy Mode (Note 3)	2 kV
Machine Model (Note 3)	200V

Operating Ratings (Notes 1 and 2)

Temperature Range	
($T_{min} \le T_A \le T_{max}$)	$-40°C \le T_A \le +85°C$
Reverse Current	
LM9140-2.5	60 μA to 15 mA
LM9140-4.1	68 μA to 15 mA
LM9140-5.0	74 μA to 15 mA
LM9140-10.0	100 μA to 15 mA

LM9140BYZ-2.5

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500		V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±12.5 **±16.6**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient (Note 7)	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±10 ±10 ±10	 **±25**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.3	 0.8 **1.0**	mV mV (max) mV (max)
		1 mA $\le I_R \le$ 15 mA	2.5	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, I_{AC} = 0.1 I_R	0.3	 0.8	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35		μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120		ppm

LM9140BYZ-4.1

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	$I_R = 100\ \mu A$	4.096		V
	Reverse Breakdown Voltage Tolerance (Note 6)	$I_R = 100\ \mu A$		±20.5 **±27.1**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient (Note 7)	$I_R = 10$ mA $I_R = 1$ mA $I_R = 100\ \mu A$	±10 ±10 ±10	 **±25**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.5	 0.9 **1.2**	mV mV (max) mV (max)
		1 mA ≤ I_R ≤ 15 mA	3.0	 7.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	$I_R = 1$ mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.0	Ω Ω(max)
e_N	Wideband Noise	$I_R = 100\ \mu A$ 10 Hz ≤ f ≤ 10 kHz	80		μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C $I_R = 100\ \mu A$	120		ppm

4

LM9140BYZ-5.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	$I_R = 100\ \mu A$	5.000		V
	Reverse Breakdown Voltage Tolerance (Note 6)	$I_R = 100\ \mu A$		±25.0 **±33.1**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		55	 74 **80**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient (Note 7)	$I_R = 10$ mA $I_R = 1$ mA $I_R = 100\ \mu A$	±10 ±10 ±10	 **±25**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.5	 1.0 **1.4**	mV mV (max) mV (max)
		1 mA $\le I_R \le$ 15 mA	3.5	 8.0 **12.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	$I_R = 1$ mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.1	Ω Ω(max)
e_N	Wideband Noise	$I_R = 100\ \mu A$ 10 Hz ≤ f ≤ 10 kHz	80		μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C $I_R = 100\ \mu A$	120		ppm

LM9140BYZ-10.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	$I_R = 150\ \mu A$	10.00		V
	Reverse Breakdown Voltage Tolerance (Note 6)	$I_R = 100\ \mu A$		±50.0 **±66.3**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient (Note 7)	$I_R = 10$ mA $I_R = 1$ mA $I_R = 150\ \mu A$	±10 ±10 ±10	 **±25**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA	0.8	 1.6 **3.5**	mV mV (max) mV (max)
		1 mA $\le I_R \le$ 15 mA	8.0	 12.0 **23.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	$I_R = 1$ mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.7	 1.7	Ω Ω(max)
e_N	Wideband Noise	$I_R = 150\ \mu A$ 10 Hz $\le$ f $\le$ 10 kHz	180		μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C $I_R = 150\ \mu A$	120		ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{MAX} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM9140, T_{Jmax} = 125°C, and the typcial thermal resistance (θ_{JA}), when board mounted, is 170°C/W with 0.125″ lead length for the TO-92 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine mode is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at T_J = 25°C and represent most likely parametric norm.

Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

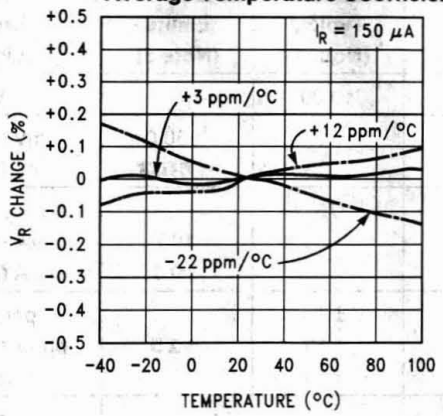
Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as a room termperature Reverse Breakdown Voltage Tolerance ± [$\Delta V_R/\Delta T$) (65°C) (V_R)]. $\Delta V_R/\Delta T$ is the V_R temperature coefficent, 65°C is the temperature range from −40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over-temperature tolerence for the different grades is shown below:
B-grade: ±0.66% = ±0.5% ±25 ppm/°C × 65°C

Therefore, as an example, the B-grade LM9140-2.5 has an over-temperature Reverse Breakdown Voltage tolerance of ±2.5V × 0.66% = ±16.6 mV.

Note 7: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX} - T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C and 125°C.

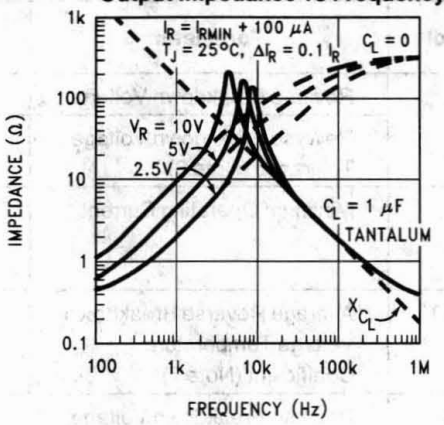
Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



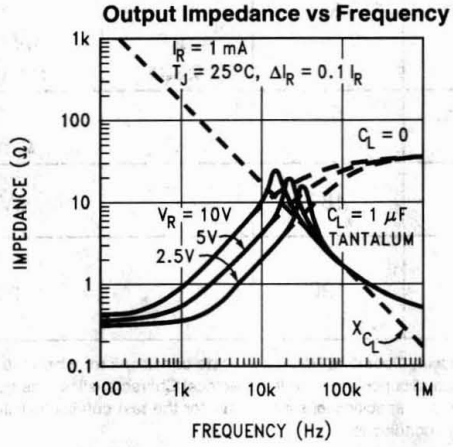
TL/H/11393–3

Output Impedance vs Frequency



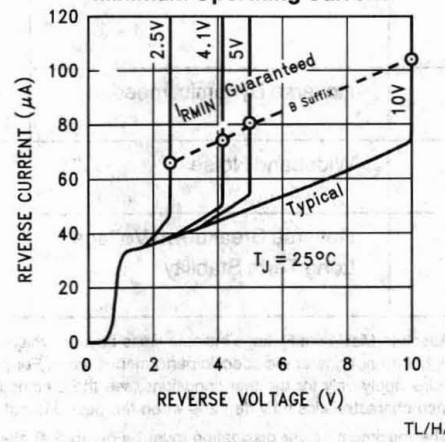
TL/H/11393–4

Output Impedance vs Frequency



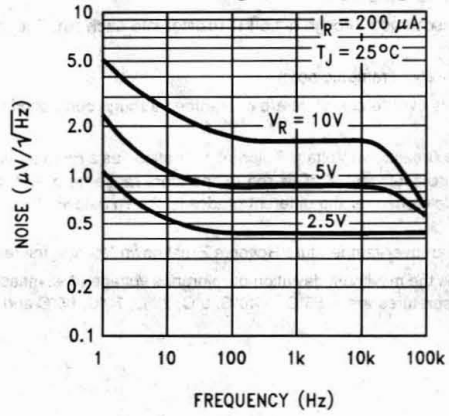
TL/H/11393–5

Reverse Characteristics and Minimum Operating Current



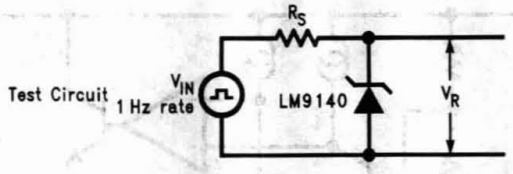
TL/H/11393–6

Noise Voltage vs Frequency

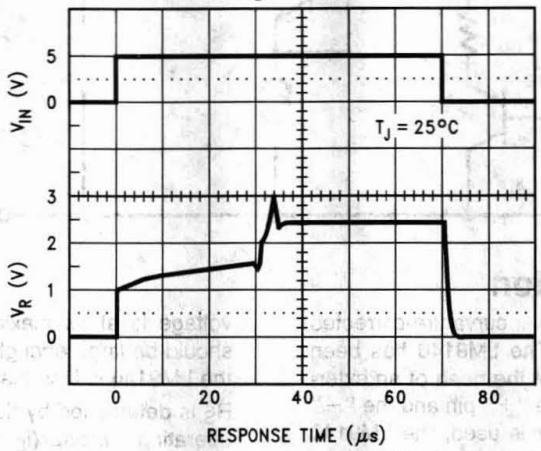


TL/H/11393–7

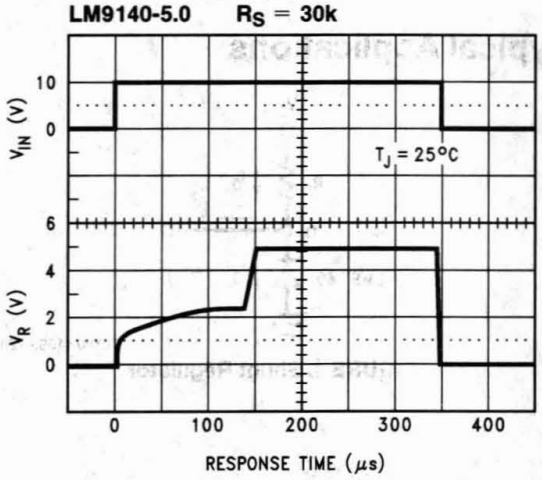
Start-Up Characteristics



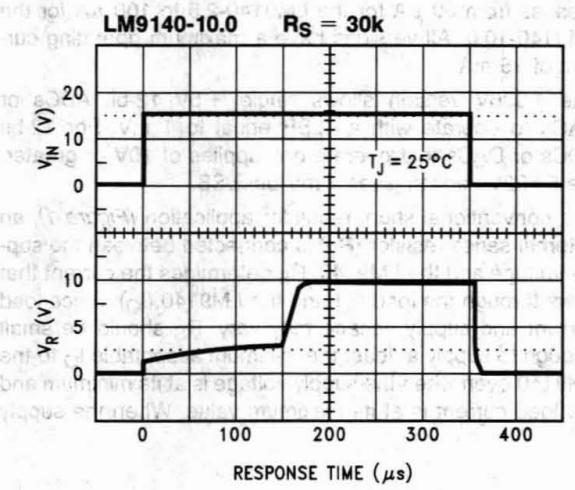
TL/H/11393-8



TL/H/11393-9



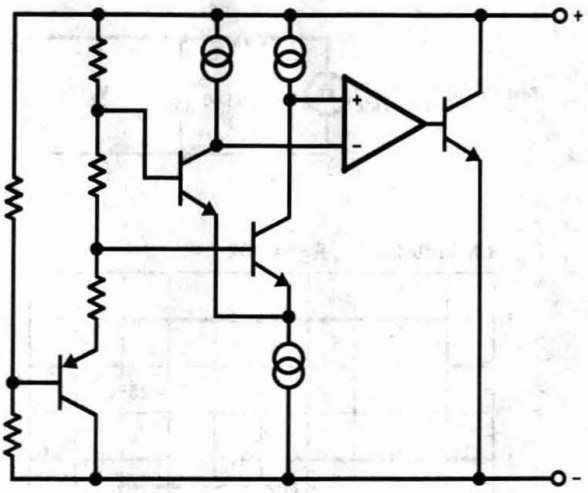
TL/H/11393-10



TL/H/11393-11

4

Functional Block Diagram



TL/H/11393–12

Applications Information

The LM9140 is a precision micro-power curvature-corrected bandgap shunt voltage reference. The LM9140 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM9140 remains stable. Reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, and 10.000V. The minimum operating current increases from 60 μA for the LM9140-2.5 to 100 μA for the LM9140-10.0. All versions have a maximum operating current of 15 mA.

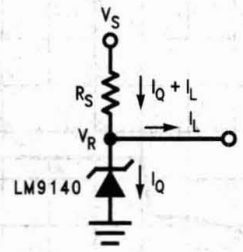
The 4.096V version allows single +5V 12-bit ADCs or DACs to operate with an LSB equal to 1 mV. For 12-bit ADCs or DACs that operate on supplies of 10V or greater, the 8.192V version gives 2 mV per LSB.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM9140. R_S determines the current that flows through the load (I_L) and the LM9140 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM9140 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM9140 is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM9140's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

Typical Applications



TL/H/11393–20

FIGURE 1. Shunt Regulator

Typical Applications (Continued)

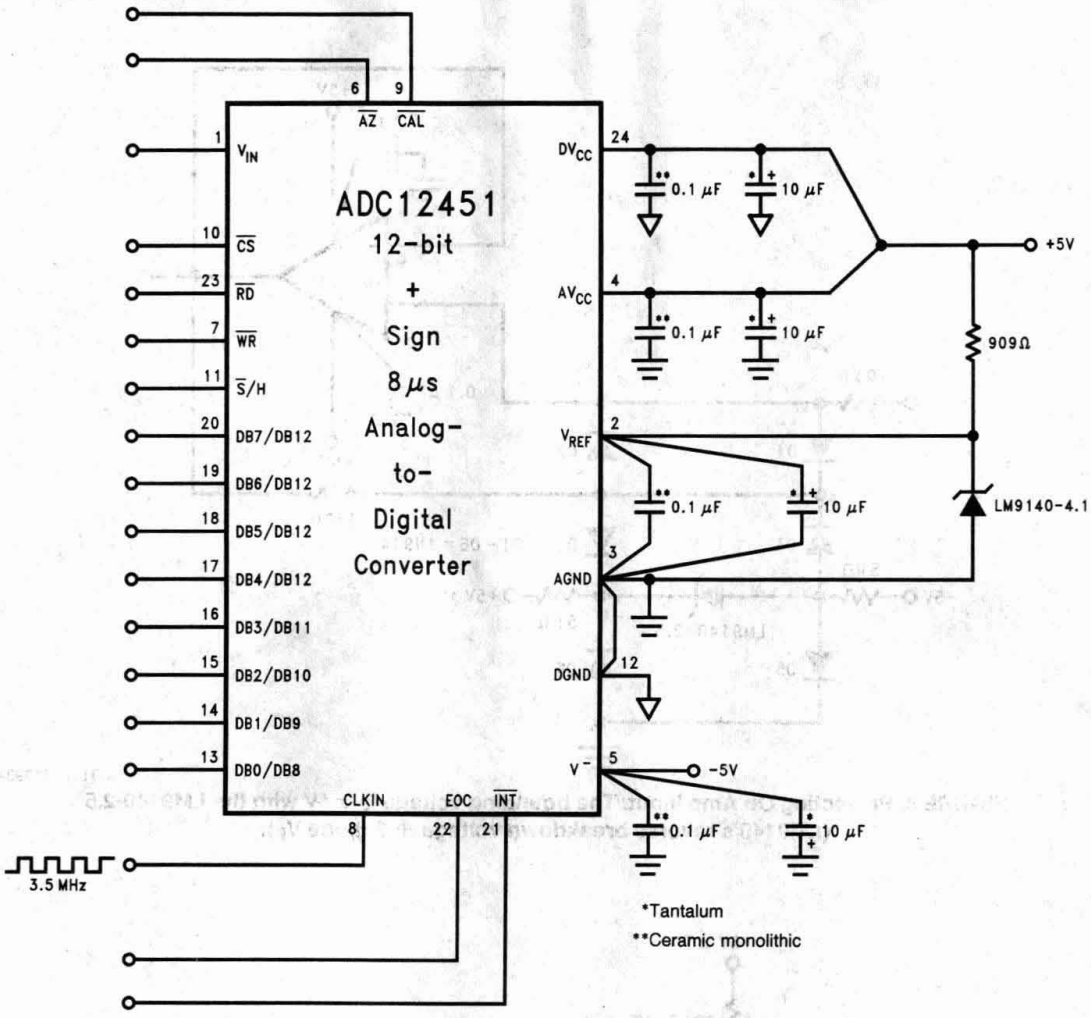
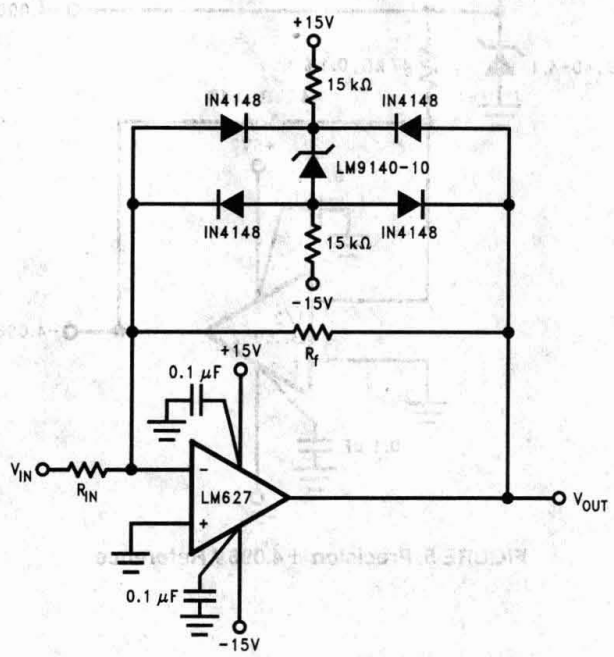


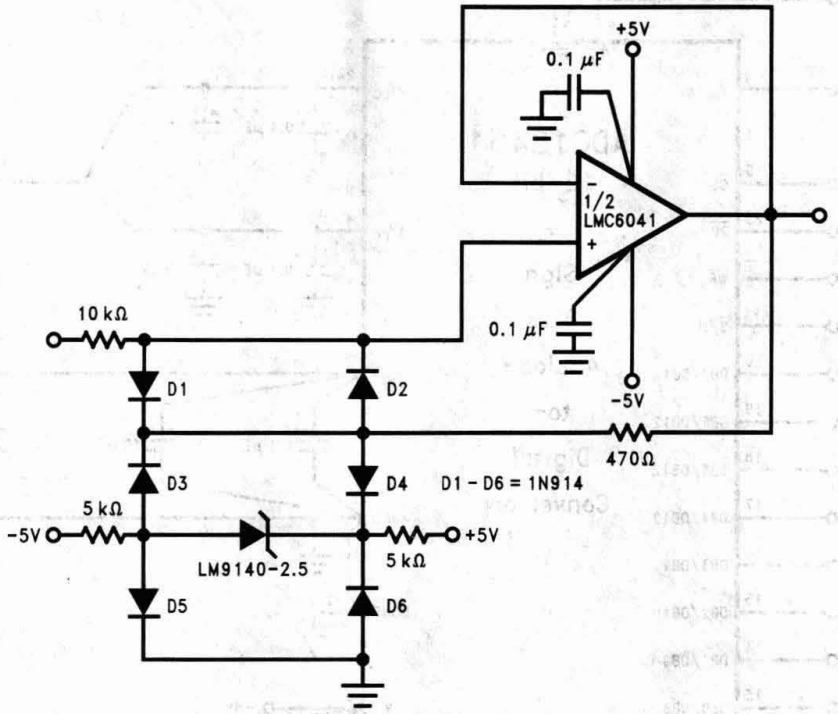
FIGURE 2. LM9140-4.1's Nominal 4.096 breakdown voltage gives ADC12451 1 mV/LSB TL/H/11393-13



TL/H/11393-14

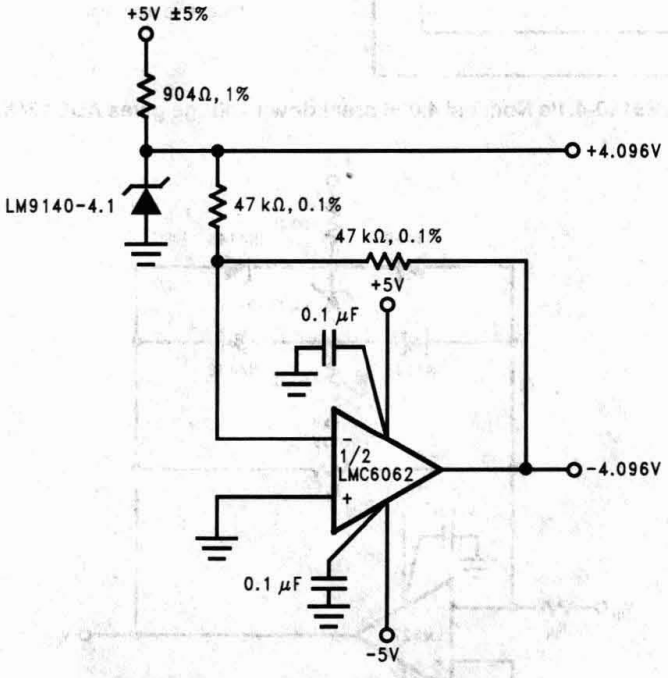
FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is ±11.5V (LM9140's reverse breakdown voltage + 2 diode V_F).

Typical Applications (Continued)



TL/H/11393–15

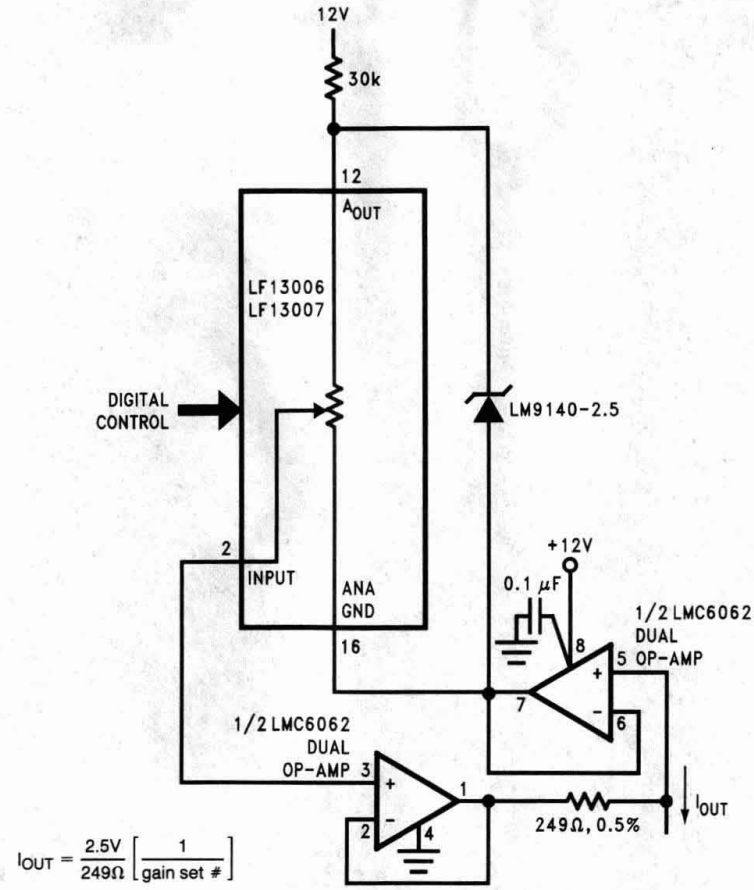
FIGURE 4. Protecting Op Amp input. The bounding voltage is ±4V with the LM9140-2.5 (LM9140's reverse breakdown voltage + 3 diode V_F).



TL/H/11393–16

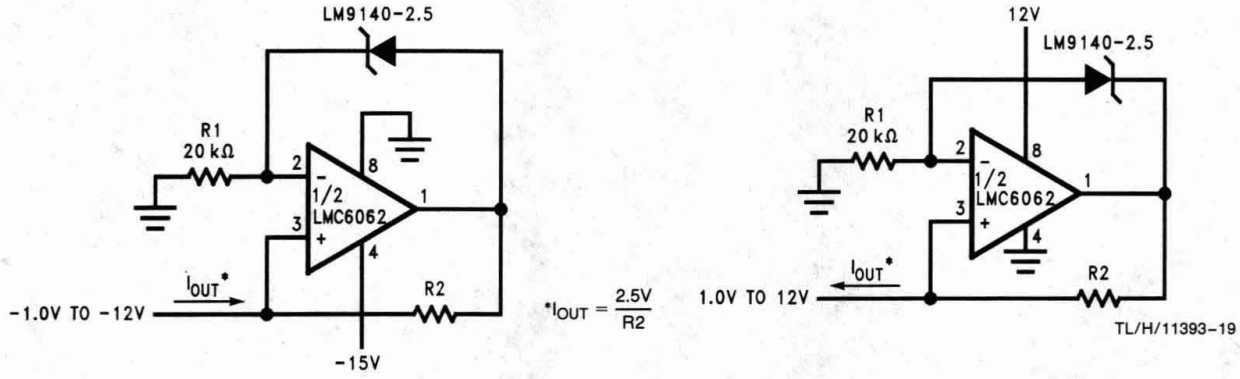
FIGURE 5. Precision ±4.096V Reference

Typical Applications (Continued)



TL/H/11393-17

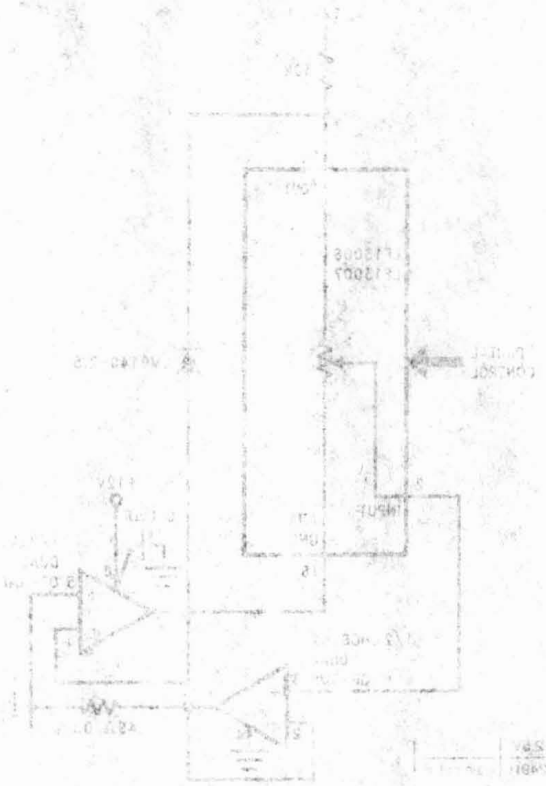
FIGURE 6. Programmable Current Source



TL/H/11393-18

TL/H/11393-19

FIGURE 7. Precision 1 μA to 1 mA Current Sources



Section 5

Temperature Sensors

Section 5 Contents

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LM34/LM34A/LM34C/LM34CA/LM34D Precision Fahrenheit Temperature Sensors 5-4
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LM135/LM235/LM335/LM135A/LM235A/LM335A Precision Temperature Sensors 5-38

National Semiconductor

Temperature Sensor Selection Guide

Part	Temp. Range	*Accuracy	Output Scale
LM34A	−50°F to +300°F	±2.0°F	10 mV/°F
LM34	−50°F to +300°F	±3.0°F	10 mV/°F
LM34CA	−40°F to +230°F	±2.0°F	10 mV/°F
LM34C	−40°F to +230°F	±3.0°F	10 mV/°F
LM34D	+32°F to +212°F	±4.0°F	10 mV/°F
LM35A	−55°C to +150°C	±1.0°C	10 mV/°C
LM35	−55°C to +150°C	±1.5°C	10 mV/°C
LM35CA	−40°C to +110°C	±1.0°C	10 mV/°C
LM35C	−40°C to +110°C	±1.5°C	10 mV/°C
LM35D	0°C to +100°C	±2.0°C	10 mV/°C
LM45B	−20°C to +100°C	±2.0°C	10 mV/°C
LM45C	−20°C to +100°C	±3.0°C	10 mV/°C
LM134-3	−55°C to +125°C	±3.0°C	$I_{SET} \propto$ °K
LM134-6	−55°C to +125°C	±6.0°C	$I_{SET} \propto$ °K
LM234-3	−25°C to +100°C	±3.0°C	$I_{SET} \propto$ °K
LM234-6	−25°C to +100°C	±6.0°C	$I_{SET} \propto$ °K
LM334	0°C to +70°C	±6.0°C	$I_{SET} \propto$ °K
LM135A	−55°C to +150°C	±1.3°C	10 mV/°K
LM135†	−55°C to +150°C	±2.0°C	10 mV/°K
LM235A	−40°C to +125°C	±1.3°C	10 mV/°K
LM235	−40°C to +125°C	±2.0°C	10 mV/°K
LM335A	−40°C to +100°C	±2.0°C	10 mV/°K
LM335	−40°C to +100°C	±4.0°C	10 mV/°K

***Note:** Accuracy is measured over T(Min) to T(Max) uncalibrated

Note: The LM134/234/334 3-Terminal Adjustable current sources Datasheet can be found in Section 4.

†**Note:** Military screening available

National Semiconductor

LM34/LM34A/LM34C/LM34CA/LM34D Precision Fahrenheit Temperature Sensors

General Description

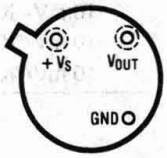
The LM34 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Fahrenheit temperature. The LM34 thus has an advantage over linear temperature sensors calibrated in degrees Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Fahrenheit scaling. The LM34 does not require any external calibration or trimming to provide typical accuracies of ±½°F at room temperature and ±1½°F over a full −50 to +300°F temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM34's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies or with plus and minus supplies. As it draws only 75 μA from its supply, it has very low self-heating, less than 0.2°F in still air. The LM34 is rated to operate over a −50° to +300°F temperature range, while the LM34C is rated for a −40° to +230°F range (0°F with improved accuracy). The LM34 series is available packaged in hermetic TO-46 transistor packages, while the LM34C, LM34CA and LM34D are also available in the plastic TO-92 transistor package. The LM34D is also available in an 8-lead surface mount small outline package. The LM34 is a complement to the LM35 (Centigrade) temperature sensor.

Features

- Calibrated directly in degrees Fahrenheit
- Linear +10.0 mV/°F scale factor
- 1.0°F accuracy guaranteed (at +77°F)
- Rated for full −50° to +300°F range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 5 to 30 volts
- Less than 90 μA current drain
- Low self-heating, 0.18°F in still air
- Nonlinearity only ±0.5°F typical
- Low-impedance output, 0.4Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*



TL/H/6685–1

*Case is connected to negative pin (GND).

Order Numbers LM34H, LM34AH, LM34CH, LM34CAH or LM34DH
See NS Package Number H03H

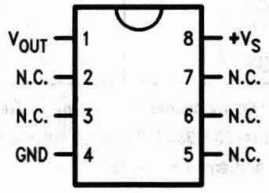
TO-92
Plastic Package

BOTTOM VIEW

TL/H/6685–2

Order Number LM34CZ, LM34CAZ or LM34DZ
See NS Package Number Z03A

SO-8
Small Outline Molded Package



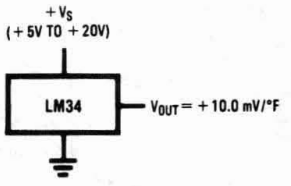
TL/H/6685–20

Top View

N.C. = No Connection

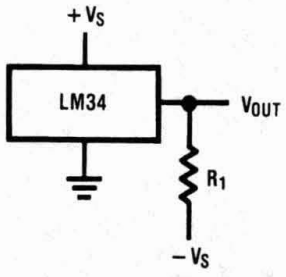
Order Number LM34DM
See NS Package Number M08A

Typical Applications



TL/H/6685–3

FIGURE 1. Basic Fahrenheit Temperature Sensor (+5° to +300°F)



CHOOSE $R_1 = (-V_S)/50\ \mu A$
$V_{OUT} = +3{,}000$ mV AT +300°F
$= +750$ mV AT +75°F
$= -500$ mV AT −50°F

TL/H/6685–4

FIGURE 2. Full-Range Fahrenheit Temperature Sensor

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
SO-8 Package	−65°C to +150°C
ESD Susceptibility (Note 11)	800V
Lead Temp.	
TO-46 Package (Soldering, 10 seconds)	+300°C
TO-92 Package (Soldering, 10 seconds)	+260°C
SO Package (Note 12):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Specified Operating Temp. Range (Note 2)

	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, Note 6)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	2.0		0.5	2.0		µA
	$5V \le V_S \le 30V$	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \le T_j \le +300°F$ for the LM34 and LM34A; $-40°F \le T_j \le +230°F$ for the LM34C and LM34CA; and $+32°F \le T_j \le +212°F$ for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \le T_j \le 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1*.

Note 2: Thermal resistance of the TO-46 package is 720°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient. Thermal resistance of the small outline molded package is 400°F/W junction to ambient. For additional thermal resistance information see table in the Typical Applications section.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

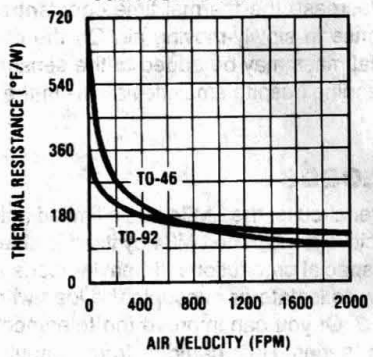
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 1, **Note 6**) (Continued)

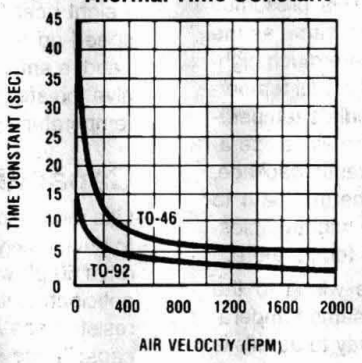
Parameter	Conditions	LM34			LM34C, LM34D			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM34, LM34C (Note 7)	T_A = +77°F	±0.8	±2.0		±0.8	±2.0		°F
	T_A = 0°F	±1.0			±1.0		±3.0	°F
	T_A = T_{MAX}	±1.6	±3.0		±1.6		±3.0	°F
	T_A = T_{MIN}	±1.6		±3.0	±1.6		±4.0	°F
Accuracy, LM34D (Note 7)	T_A = +77°F				±1.2	±3.0		°F
	T_A = T_{MAX}				±1.8		±4.0	°F
	T_A = T_{MIN}				±1.8		±4.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.6**		**±1.0**	**±0.4**		**±1.0**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±2.5		±0.4	±2.5		mV/mA
	$T_{MIN} \le T_A \le$ +150°F	**±0.5**		**±6.0**	**±0.5**		**±6.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.1		±0.01	±0.1		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	100		75	100		µA
	V_S = +5V	**131**		**176**	**116**		**154**	µA
	V_S = +30V, +77°F	76	103		76	103		µA
	V_S = +30V	**132**		**181**	**117**		**159**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	3.0		0.5	3.0		µA
	$5V \le V_S \le 30V$	**+1.0**		**5.0**	**1.0**		**5.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.7**	**+0.30**		**+0.7**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Typical Performance Characteristics

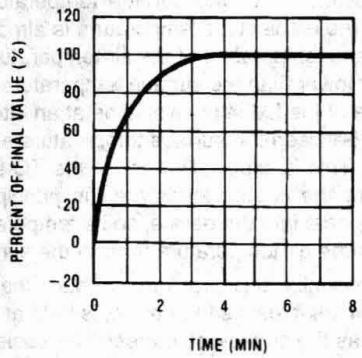
Thermal Resistance Junction to Air



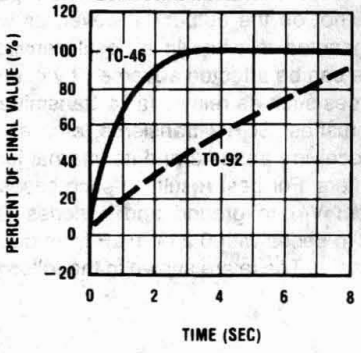
Thermal Time Constant



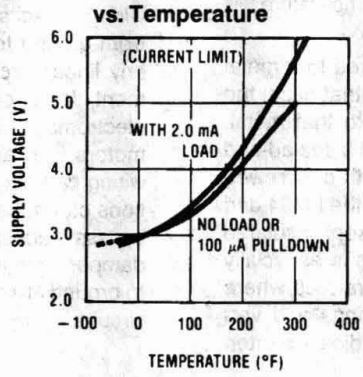
Thermal Response in Still Air



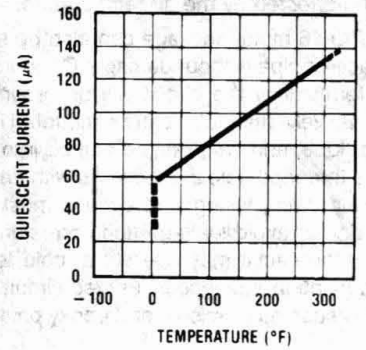
Thermal Response in Stirred Oil Bath



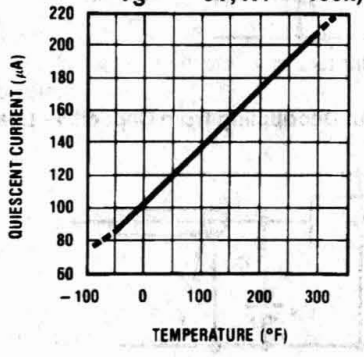
Minimum Supply Voltage vs. Temperature



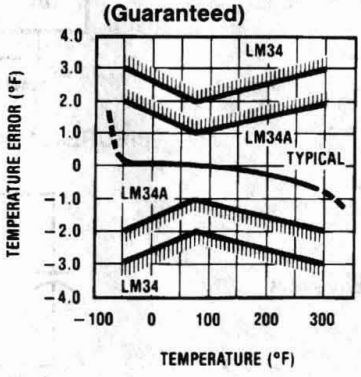
Quiescent Current vs. Temperature (In Circuit of *Figure 1*)



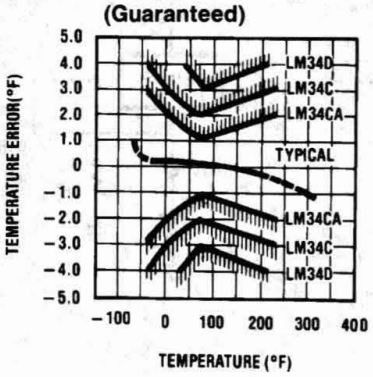
Quiescent Current vs. Temperature (In Circuit of *Figure 2*; $-V_S = -5V$, R1 = 100k)



Accuracy vs. Temperature (Guaranteed)



Accuracy vs. Temperature (Guaranteed)



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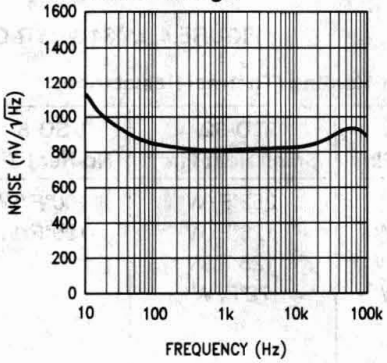
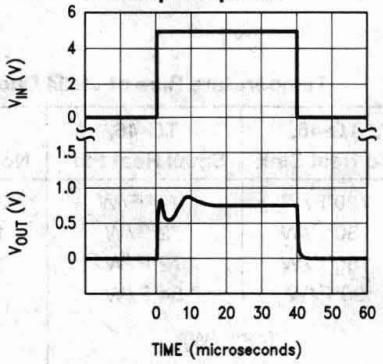
Noise Voltage



Start-Up Response



TL/H/6685-21

Typical Applications

The LM34 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.02°F of the surface temperature. This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM34 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM34, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM34 die's temperature will not be affected by the air temperature.

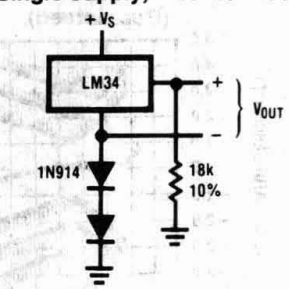
The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course in that case, the V_- terminal of the circuit will be grounded to that metal. Alternatively, the LM34 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM34 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM34 or its connections.

These devices are sometimes soldered to a small, lightweight heat fin to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor to give the steadiest reading despite small deviations in the air temperature.

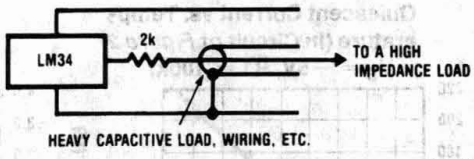
Capacitive Loads

Like most micropower circuits, the LM34 has a limited ability to drive heavy capacitive loads. The LM34 by itself is able to drive 50 pF without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*. When the LM34 is applied with a 499Ω load resistor (as shown), it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR's transients, etc., as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in the following circuits.

Temperature Sensor, Single Supply, −50° to +300°F



TL/H/6685–6



TL/H/6685–7

FIGURE 3. LM34 with Decoupling from Capacitive Load

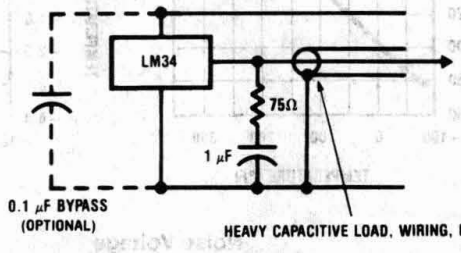


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FIGURE 4. LM34 with R-C Damper

Temperature Rise of LM34 Due to Self-Heating (Thermal Resistance)

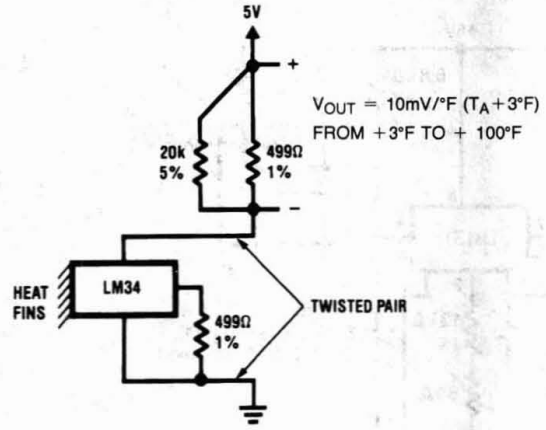
Conditions	TO-46, No Heat Sink	TO-46, Small Heat Fin*	TO-92, No Heat Sink	TO-92, Small Heat Fin**	SO-8 No Heat Sink	SO-8 Small Heat Fin**
Still air	720°F/W	180°F/W	324°F/W	252°F/W	400°F/W	200°F/W
Moving air	180°F/W	72°F/W	162°F/W	126°F/W	190°F/W	160°F/W
Still oil	180°F/W	72°F/W	162°F/W	126°F/W		
Stirred oil	90°F/W	54°F/W	81°F/W	72°F/W		
(Clamped to metal, infinite heat sink)	(43°F/W)				(95°F/W)	

*Wakefield type 201 or 1" disc of 0.020" sheet brass, soldered to case, or similar.

**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz copper foil, or similar.

Typical Applications (Continued)

Two-Wire Remote Temperature Sensor (Grounded Sensor)



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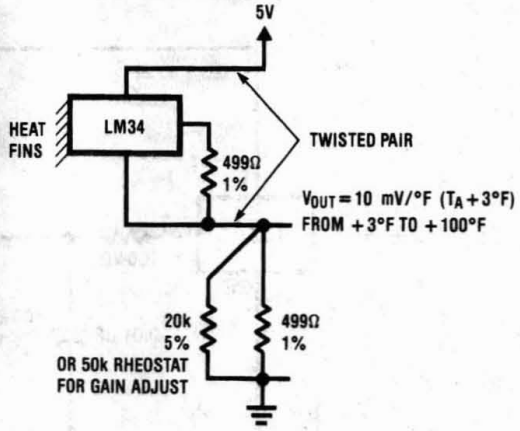
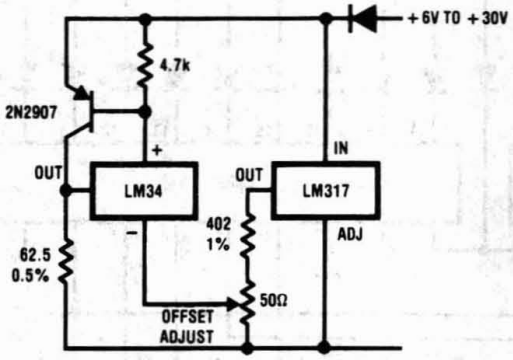
Two-Wire Remote Temperature Sensor (Output Referred to Ground)



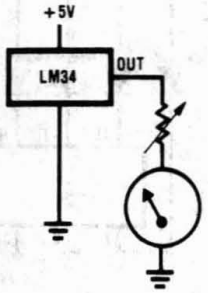
TL/H/6685–10

4-to-20 mA Current Source (0 to + 100°F)



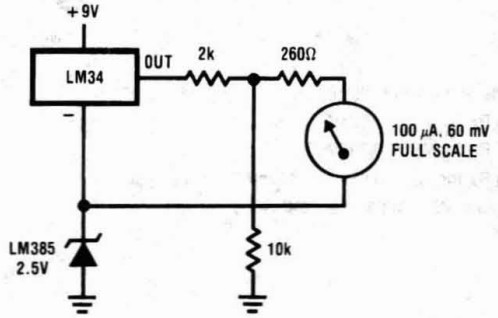
TL/H/6685–11

Fahrenheit Thermometer (Analog Meter)



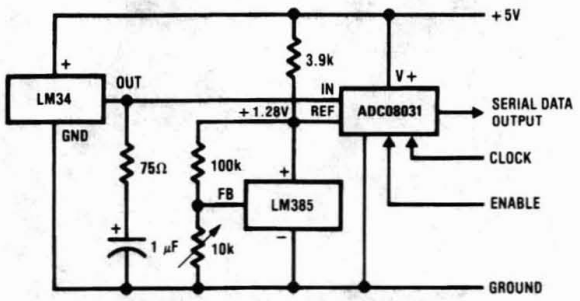
TL/H/6685–12

Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)



TL/H/6685–13

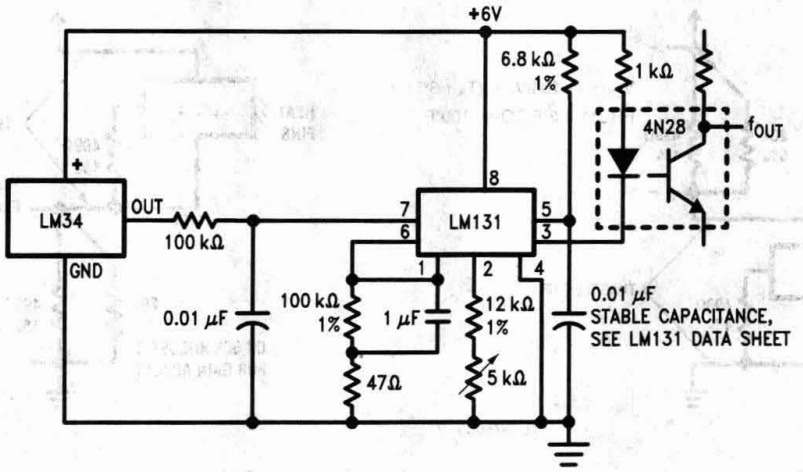
Temperature-to-Digital Converter (Serial Output, + 128°F Full Scale)



TL/H/6685–14

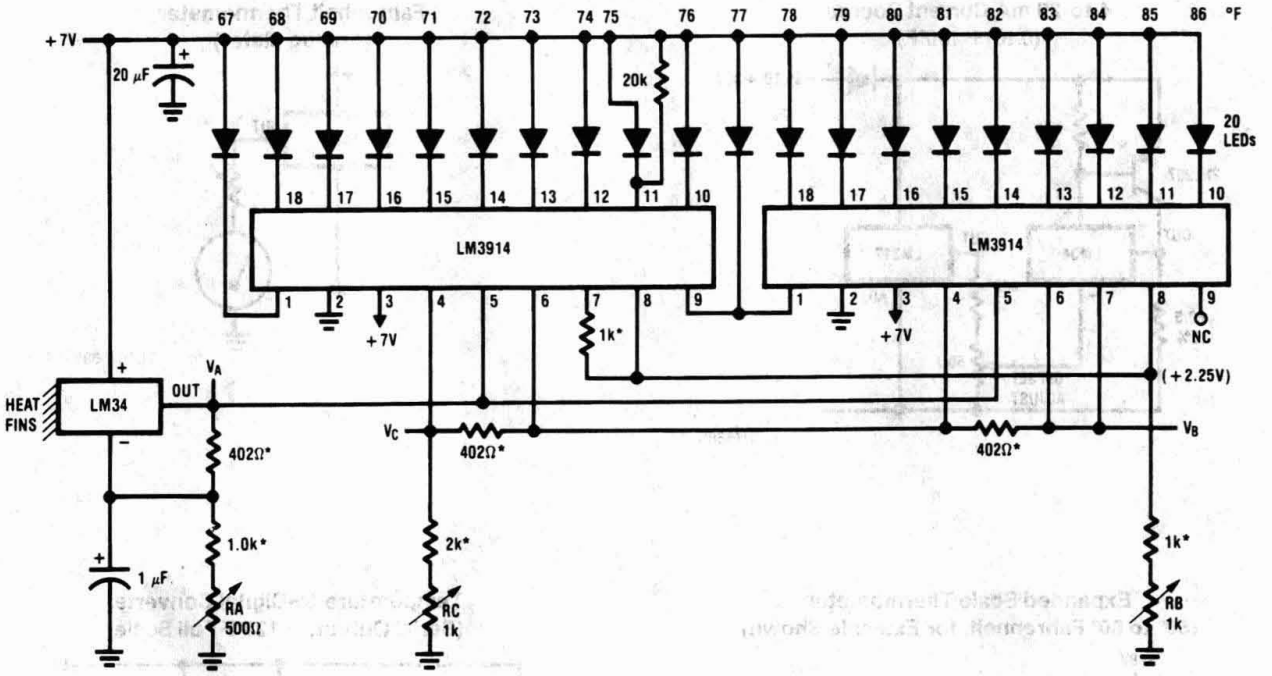
Typical Applications (Continued)

LM34 with Voltage-to-Frequency Converter and Isolated Output (3°F to + 300°F; 30 Hz to 3000 Hz)



TL/H/6685–15

Bar-Graph Temperature Display (Dot Mode)



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* = 1% or 2% film resistor

—Trim R_B for V_B = 3.525V

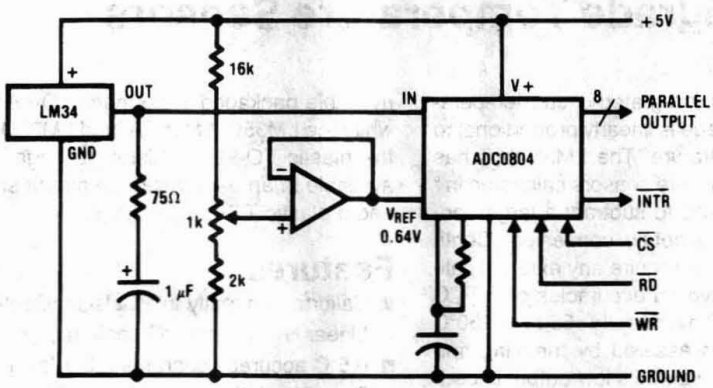
—Trim R_C for V_C = 2.725V

—Trim R_A for V_A = 0.085V + 40 mV/°F × $T_{AMBIENT}$

—Example, V_A = 3.285V at 80°F

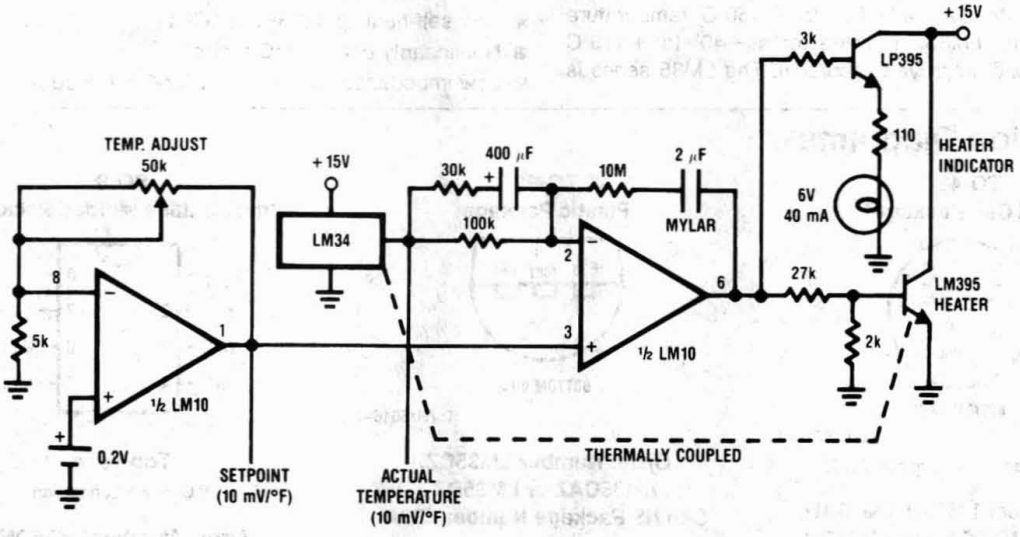
Typical Applications (Continued)

Temperature-to-Digital Converter
(Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface, 128 °F Full Scale)



TL/H/6685–17

Temperature Controller



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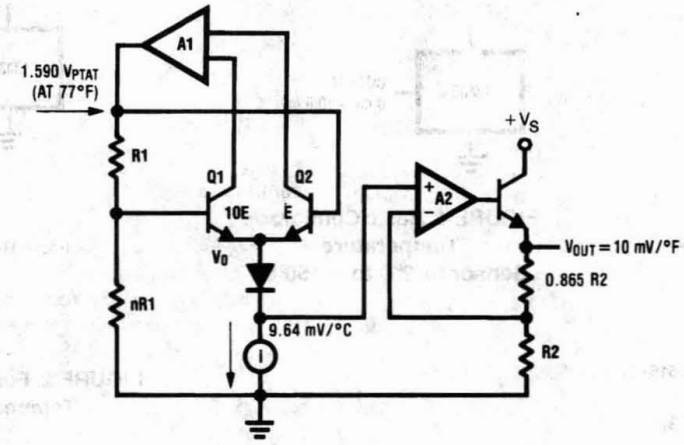
Block Diagram



TL/H/6685–19

5

National Semiconductor

LM35/LM35A/LM35C/LM35CA/LM35D Precision Centigrade Temperature Sensors

General Description

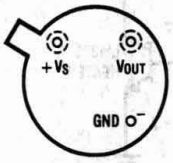
The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-202 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*



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*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

TO-92
Plastic Package

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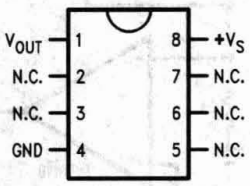
Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

SO-8
Small Outline Molded Package

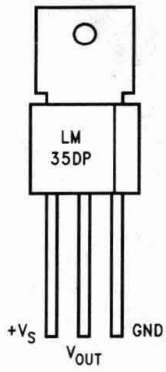


TL/H/5516–21

Top View
N.C. = No Connection

Order Number LM35DM
See NS Package Number M08A

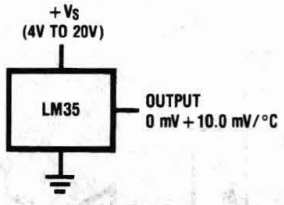
TO-202
Plastic Package



TL/H/5516–24

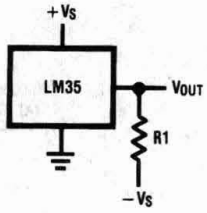
Order Number LM35DP
See NS Package Number P03A

Typical Applications



TL/H/5516–3

FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



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Choose $R_1 = -V_S/50\ \mu A$

$V_{OUT} = +1{,}500$ mV at +150°C
$= +250$ mV at +25°C
$= -550$ mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp., TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-202 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 Package, (Soldering, 10 seconds)	260°C
TO-202 Package, (Soldering, 10 seconds)	+230°C
SO Package (Note 12):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics (Note 1) (Note 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	$T_A = +25°C$	±0.2	±0.5		±0.2	±0.5		°C
	$T_A = -10°C$	±0.3			±0.3		±1.0	°C
	$T_A = T_{MAX}$	±0.4	±1.0		±0.4	±1.0		°C
	$T_A = T_{MIN}$	±0.4	±1.0		±0.4		±1.5	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	$T_A = +25°C$	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
Line Regulation (Note 3)	$T_A = +25°C$	±0.01	±0.05		±0.01	±0.05		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +25°C$	56	67		56	67		µA
	$V_S = +5V$	**105**		**131**	**91**		**114**	µA
	$V_S = +30V, +25°C$	56.2	68		56.2	68		µA
	$V_S = +30V$	**105.5**		**133**	**91.5**		**116**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V, +25°C$	0.2	1.0		0.2	1.0		µA
	$4V \le V_S \le 30V$	**0.5**		**2.0**	**0.5**		**2.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L = 0$	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J = T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40° \le T_J \le +110°C$ for the LM35C and LM35CA; and $0° \le T_J \le +100°C$ for the LM35D. $V_S = +5$Vdc and $I_{LOAD} = 50$ µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-202 package is 85°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Electrical Characteristics (Note 1) **(Note 6)** (Continued)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	$T_A = +25°C$	±0.4	±1.0		±0.4	±1.0		°C
	$T_A = -10°C$	±0.5			±0.5		±1.5	°C
	$T_A = T_{MAX}$	±0.8	±1.5		±0.8		±1.5	°C
	$T_A = T_{MIN}$	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	$T_A = +25°C$				±0.6	±1.5		°C
	$T_A = T_{MAX}$				±0.9		±2.0	°C
	$T_A = T_{MIN}$				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	$T_A = +25°C$	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	$T_A = +25°C$	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +25°C$	56	80		56	80		µA
	$V_S = +5V$	**105**		**158**	**91**		**138**	µA
	$V_S = +30V, +25°C$	56.2	82		56.2	82		µA
	$V_S = +30V$	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V, +25°C$	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L = 0$	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J = T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

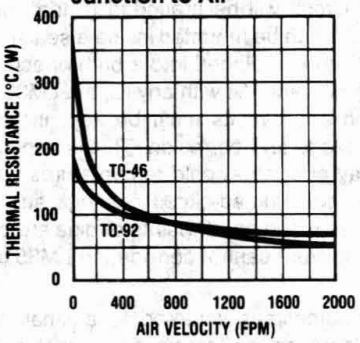
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

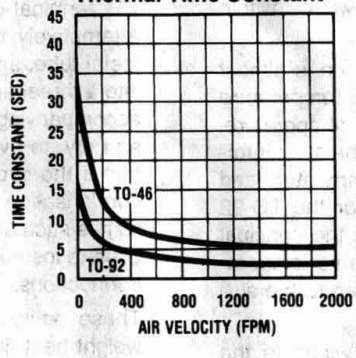
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Typical Performance Characteristics

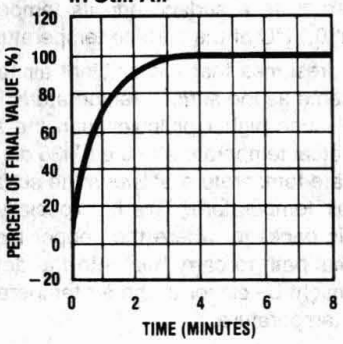
Thermal Resistance Junction to Air



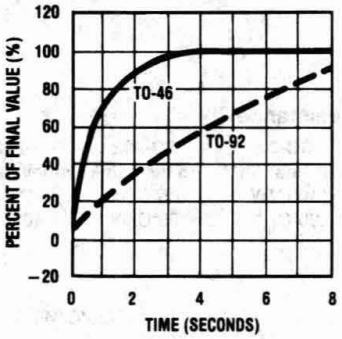
Thermal Time Constant



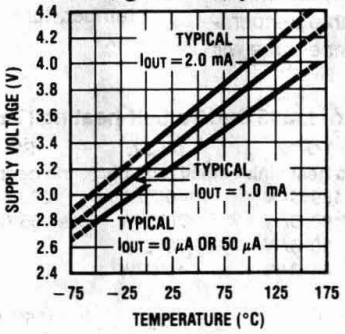
Thermal Response in Still Air



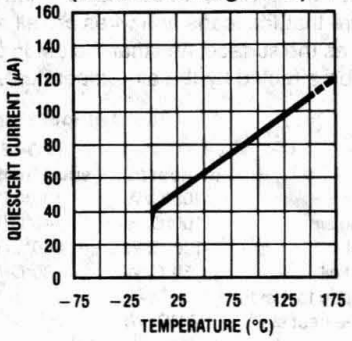
Thermal Response in Stirred Oil Bath



Minimum Supply Voltage vs. Temperature



Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)



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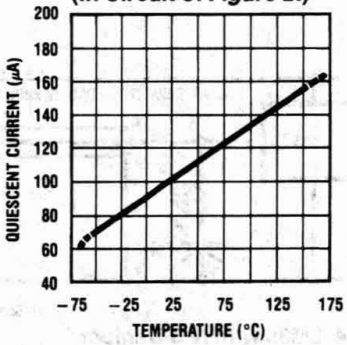
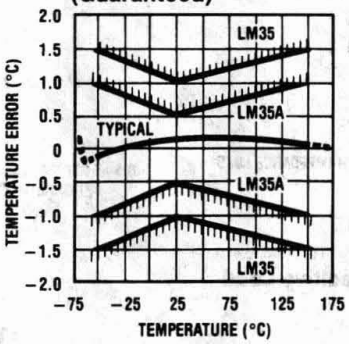
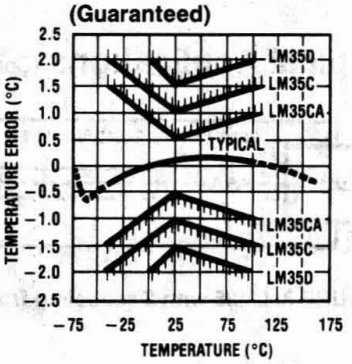
Quiescent Current vs. Temperature (In Circuit of *Figure 2*.)



Accuracy vs. Temperature (Guaranteed)



Accuracy vs. Temperature (Guaranteed)



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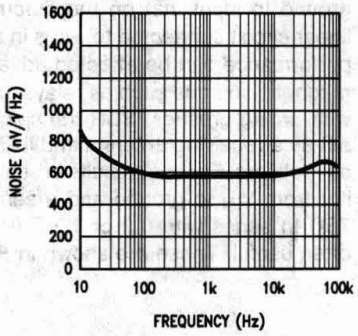
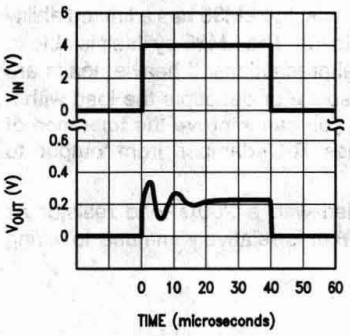
Noise Voltage



Start-Up Response



TL/H/5516–22

5

Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small lightweight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

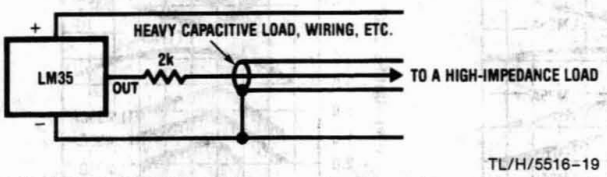
Temperature Rise of LM35 Due To Self-heating (Thermal Resistance)

	TO-46, no heat sink	TO-46, small heat fin*	TO-92, no heat sink	TO-92, small heat fin**	SO-8 no heat sink	SO-8 small heat fin**	TO-202 no heat sink	TO-202 *** small heat fin
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	85°C/W	60°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	25°C/W	40°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W				
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W				
(Clamped to metal, Infinite heat sink)	(24°C/W)				(55°C/W)		(23°C/W)	

* Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.

** TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications (Continued)



TL/H/5516–19

FIGURE 3. LM35 with Decoupling from Capacitive Load

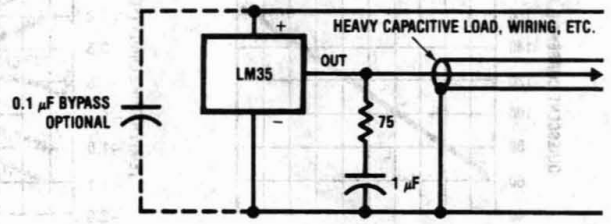


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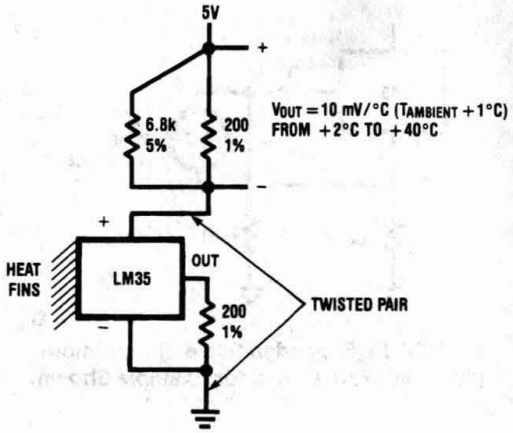
FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5, 6,* or *8,* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in *Figures 13, 14,* and *16.*

Typical Applications (Continued)



TL/H/5516–5

FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

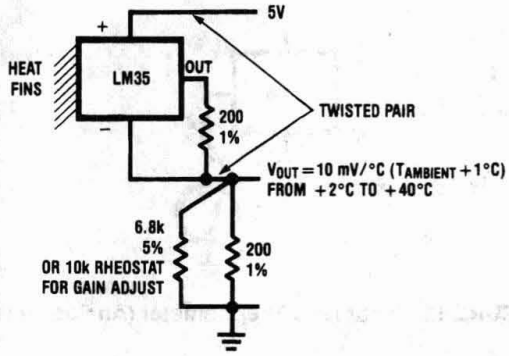


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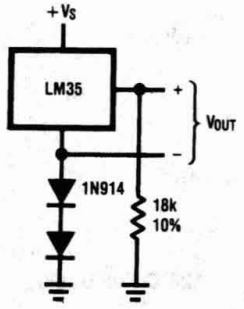
FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)



TL/H/5516–7

FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

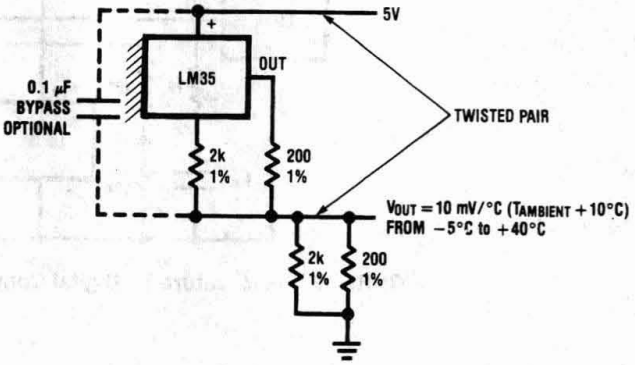


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FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

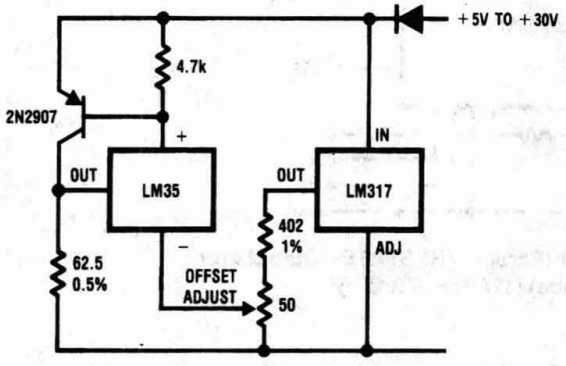

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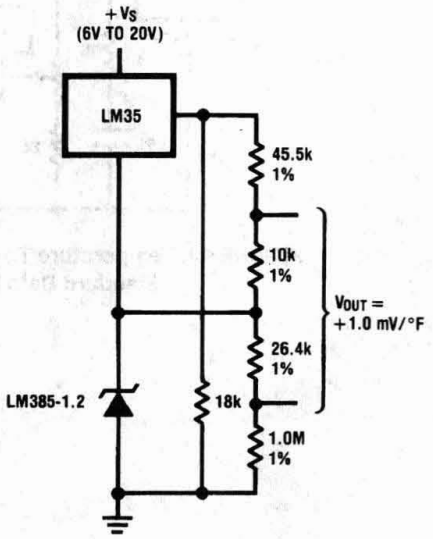
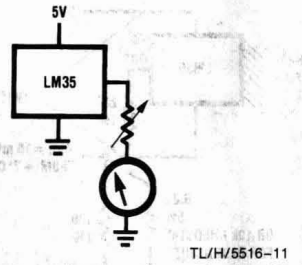
FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)



TL/H/5516–10

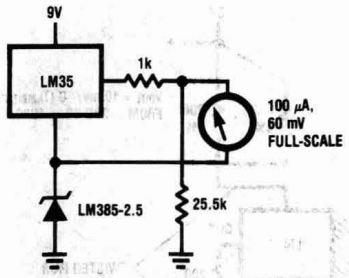
FIGURE 10. Fahrenheit Thermometer

Typical Applications (Continued)



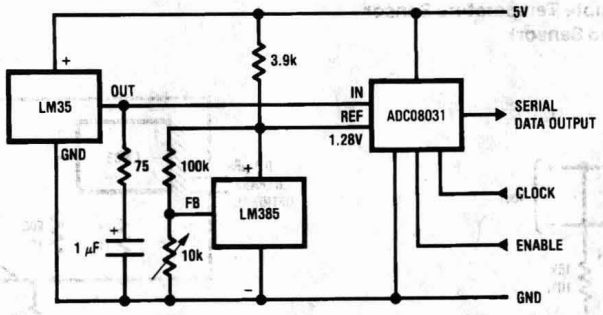
TL/H/5516–11

FIGURE 11. Centigrade Thermometer (Analog Meter)



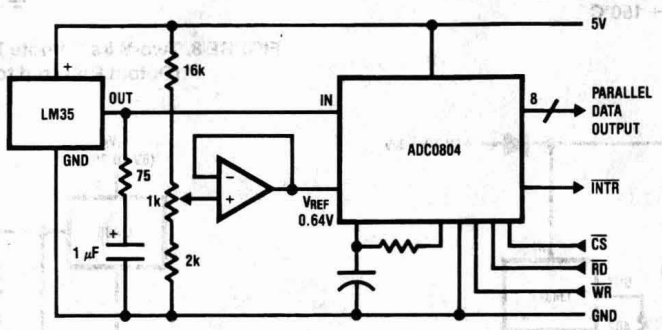
TL/H/5516–12

FIGURE 12. Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)



TL/H/5516–13

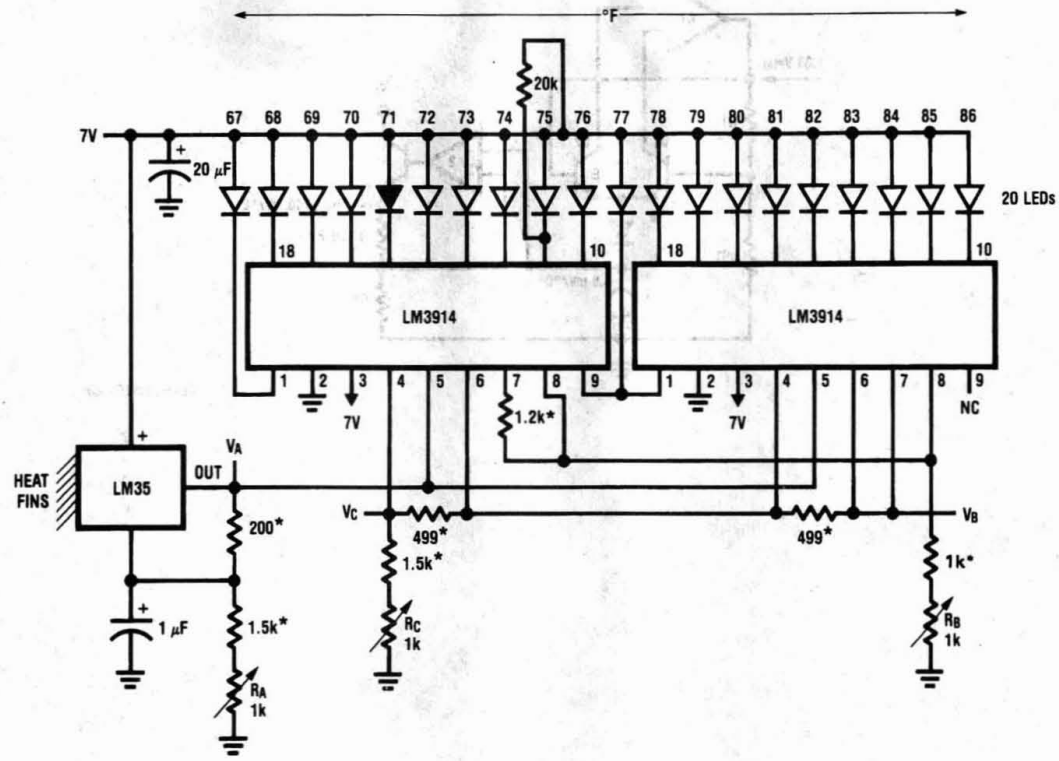
FIGURE 13. Temperature To Digital Converter (Serial Output) (+ 128°C Full Scale)



TL/H/5516–14

FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (128°C Full Scale)

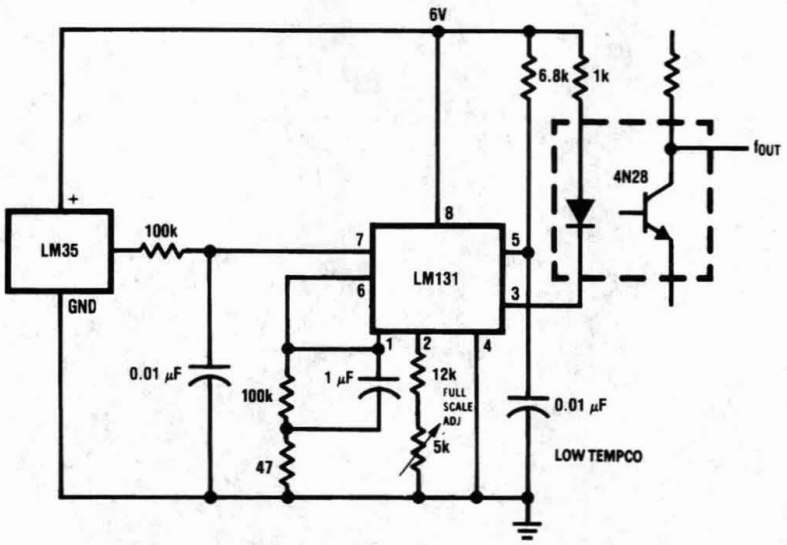
Typical Applications (Continued)



TL/H/5516–16

*=1% or 2% film resistor
-Trim R_B for V_B=3.075V
-Trim R_C for V_C=1.955V
-Trim R_A for V_A=0.075V + 100mV/°C × $T_{ambient}$
-Example, V_A=2.275V at 22°C

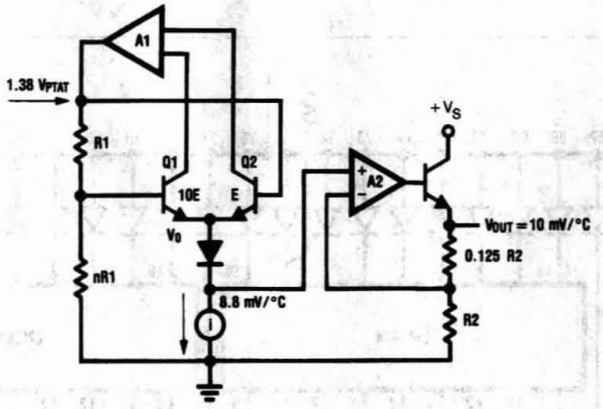
FIGURE 15. Bar-Graph Temperature Display (Dot Mode)



TL/H/5516–15

FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram



TL/H/5516–23

National Semiconductor

LM45B/LM45C
SOT-23 Precision Centigrade Temperature Sensors

General Description

The LM45 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM45 does not require any external calibration or trimming to provide accuracies of ±2°C at room temperature and ±3°C over a full −20 to +100°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM45's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with a single power supply, or with plus and minus supplies. As it draws only 120 μA from its supply, it has very low self-heating, less than 0.2°C in still air. The LM45 is rated to operate over a −20° to +100°C temperature range.

Applications

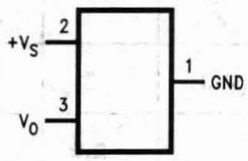
- Battery Management
- FAX Machines
- Printers
- Portable Medical Instruments
- HVAC
- Power Supply Modules
- Disk Drives
- Computers
- Automotive

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- ±3°C accuracy guaranteed
- Rated for full −20° to +100°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4.0V to 10V
- Less than 120 μA current drain
- Low self-heating, 0.20°C in still air
- Nonlinearity only ±0.8°C max over temp
- Low impedance output, 20Ω for 1 mA load

Connection Diagram

SOT-23



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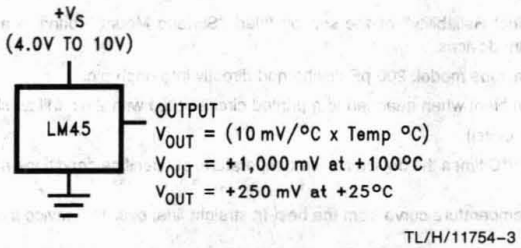
Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)

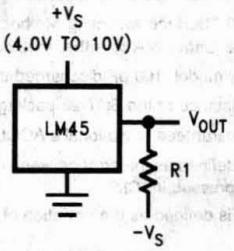
Order Number	SOT-23 Device Marking	Supplied As
LM45BIM3	T4B	250 Units on Tape and Reel
LM45BIM3X	T4B	3000 Units on Tape and Reel
LM45CIM3	T4C	250 Units on Tape and Reel
LM45CIM3X	T4C	3000 Units on Tape and Reel

Typical Applications



TL/H/11754–3

FIGURE 1. Basic Centigrade Temperature Sensor (+2.5°C to +100°C)



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Choose $R_1 = -V_S/50\ \mu A$

V_{OUT} = (10 mV/°C × Temp °C)

V_{OUT} = +1,000 mV at +100°C

= +250 mV at +25°C

= −200 mV at −20°C

FIGURE 2. Full-Range Centigrade Temperature Sensor (−20°C to +100°C)

Absolute Maximum Ratings (Note 1)

Supply Voltage	+12V to −0.2V
Output Voltage	$+V_S$ + 0.6V to −1.0V
Output Current	10 mA
Storage Temperature	−65°C to +150°C
Lead Temperature	
SOT Package (Note 2):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 3):	
Human Body Model	2000V
Machine Model	TBD

Operating Ratings (Note 1)

Specified Temperature Range (Note 4)	T_{MIN} to T_{MAX}
LM45B, LM45C	−20°C to +100°C
Operating Temperature Range	
LM45B, LM45C	−40°C to +125°C
Supply Voltage Range ($+V_S$)	+4.0V to +10V

Electrical Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = +5Vdc and I_{LOAD} = +50 μA, in the circuit of *Figure 2*. These specifications also apply from +2.5°C to T_{MAX} in the circuit of *Figure 1* for $+V_S$ = +5Vdc. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = +25°C, unless otherwise noted.

Parameter	Conditions	LM45B		LM45C		Units (Limit)
		Typical	Limit (Note 5)	Typical	Limit (Note 5)	
Accuracy (Note 6)	T_A = +25°C		±2.0		±3.0	°C (max)
	T_A = T_{MAX}		±3.0		±4.0	°C (max)
	T_A = T_{MIN}		±3.0		±4.0	°C (max)
Nonlinearity (Note 7)	$T_{MIN} \le T_A \le T_{MAX}$		**±0.8**		**±0.8**	°C (max)
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$		**+9.7**		**+9.7**	mV/°C (min)
			+10.3		**+10.3**	mV/°C (max)
Load Regulation (Note 8)	$0 \le I_L \le +1$ mA		**±35**		**±35**	mV/mA (max)
Line Regulation (Note 8)	$+4.0V \le +V_S \le +10V$		±0.80		±0.80	mV/V (max)
			±1.2		**±1.2**	mV/V (max)
Quiescent Current (Note 9)	$+4.0V \le +V_S \le +10V$, +25°C		120		120	μA (max)
	$+4.0V \le +V_S \le +10V$		**160**		**160**	μA (max)
Change of Quiescent Current (Note 8)	$4.0V \le +V_S \le 10V$		**2.0**		**2.0**	μA (max)
Temperature Coefficient of Quiescent Current		**+2.0**		**+2.0**		μA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0		+2.5		+2.5	°C (min)
Long Term Stability (Note 10)	T_J = T_{MAX}, for 1000 hours	±0.12		±0.12		°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

Note 4: Thermal resistance of the SOT-23 package is 260°C/W, junction to ambient when attached to a printed circuit board with 2 oz. foil as shown in *Figure 3*.

Note 5: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Accuracy is defined as the error between the output voltage and 10 mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 7: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 8: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

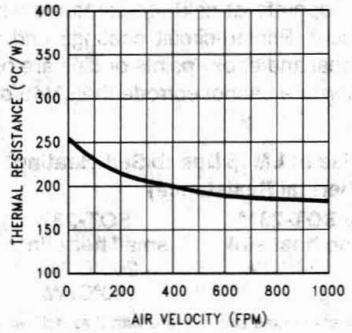
Note 9: Quiescent current is measured using the circuit of *Figure 1*.

Note 10: For best long-term stability, any precision circuit will give best results if the unit is aged at a warm temperature, and/or temperature cycled for at least 46 hours before long-term life test begins. This is especially true when a small (Surface-Mount) part is wave-soldered; allow time for stress relaxation to occur.

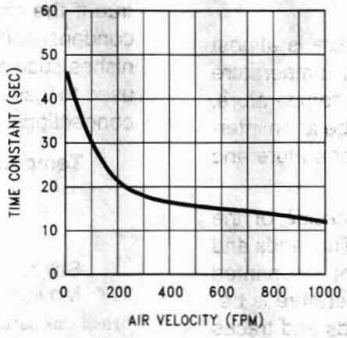
Typical Performance Characteristics

To generate these curves the LM45 was mounted to a printed circuit board as shown in *Figure 3*.

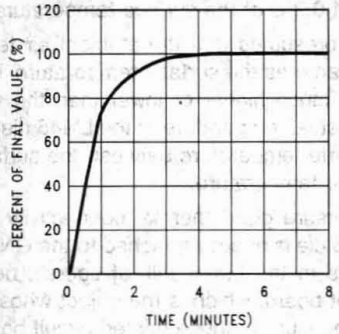
Thermal Resistance Junction to Air



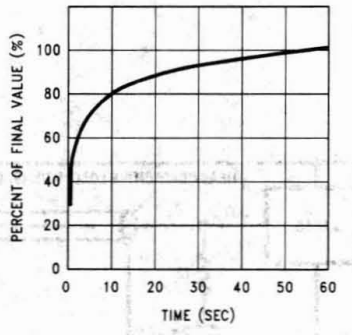
Thermal Time Constant



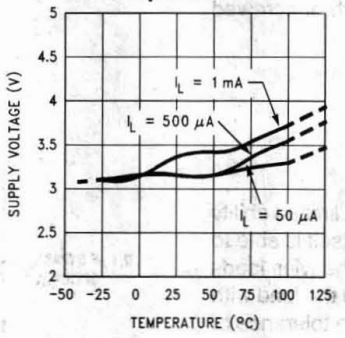
Thermal Response in Still Air with Heat Sink (*Figure 3*)



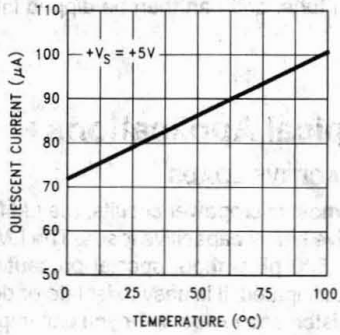
Thermal Response in Stirred Oil Bath with Heat Sink



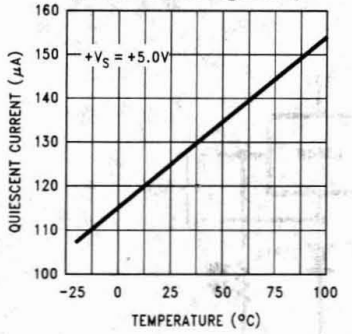
Start-Up Voltage vs Temperature



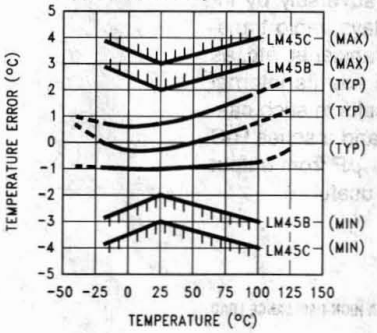
Quiescent Current vs Temperature (In Circuit of *Figure 1*)



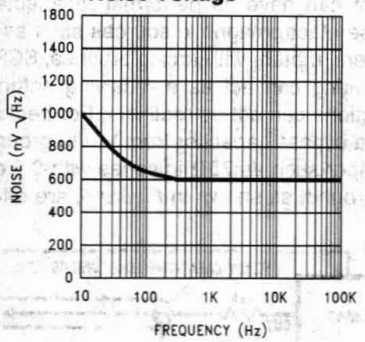
Quiescent Current vs Temperature (In Circuit of *Figure 2*)



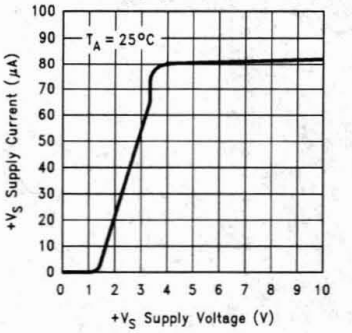
Accuracy vs Temperature (Guaranteed)



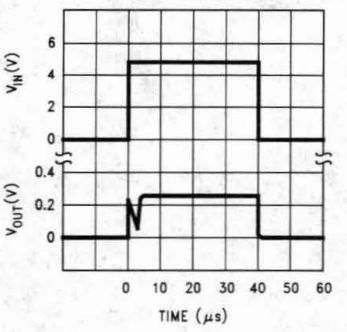
Noise Voltage



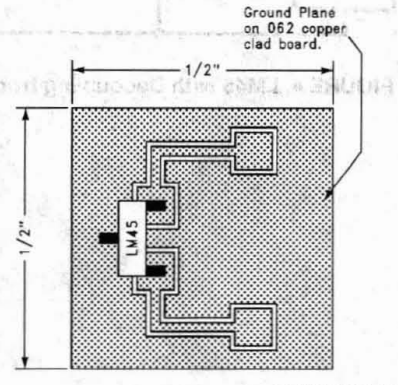
Supply Voltage vs Supply Current



Start-Up Response



TL/H/11754–5



TL/H/11754–23

FIGURE 3. Printed Circuit Board Used for Heat Sink to Generate All Curves. ½" Square Printed Circuit Board with 2 oz. Foil or Similar

Applications

The LM45 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.2°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM45 die would be at an intermediate temperature between the surface temperature and the air temperature.

To ensure good thermal conductivity the backside of the LM45 die is directly attached to the GND pin. The lands and traces to the LM45 will, of course, be part of the printed circuit board, which is the object whose temperature is being measured. These printed circuit board lands and traces will not cause the LM45s temperature to deviate from the desired temperature.

Alternatively, the LM45 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM45 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM45 or its connections.

Temperature Rise of LM45 Due to Self-Heating (Thermal Resistance)

	SOT-23** no heat sink	SOT-23 small heat fin*
Still air	450°C/W	260°C/W
Moving air		180°C/W

* Heat sink used is ½" square printed circuit board with 2 oz. foil with part attached as shown in *Figure 3*.

** Part soldered to 30 gauge wire.

Typical Applications

CAPACITIVE LOADS

Like most micropower circuits, the LM45 has a limited ability to drive heavy capacitive loads. The LM45 by itself is able to drive 500 pF without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 4*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 5*.

Any linear circuit connected to wires in a hostile environment can have its performance affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground, as shown in *Figure 5*, are often useful.

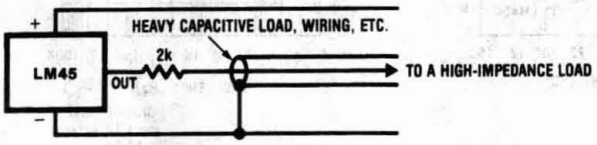


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FIGURE 4. LM45 with Decoupling from Capacitive Load

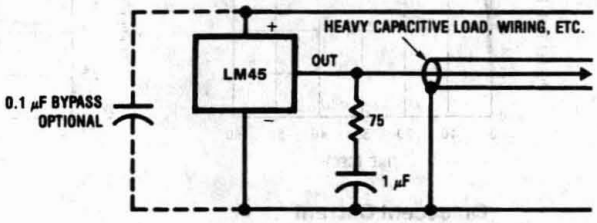

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FIGURE 5. LM45 with R-C Damper

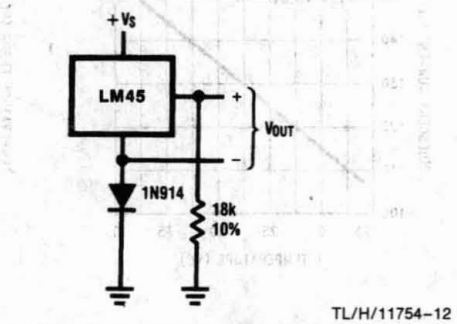

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FIGURE 6. Temperature Sensor, Single Supply, −20°C to +100°C

Typical Applications (Continued)

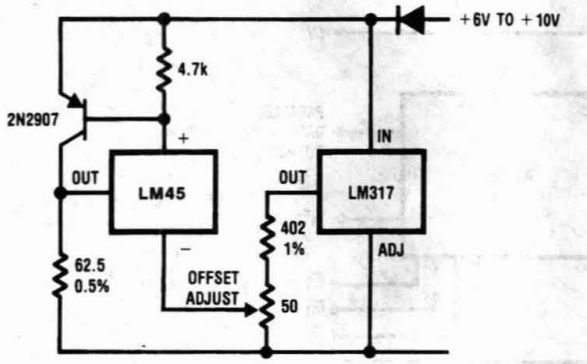

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FIGURE 7. 4-to-20 mA Current Source (0°C to +100°C)

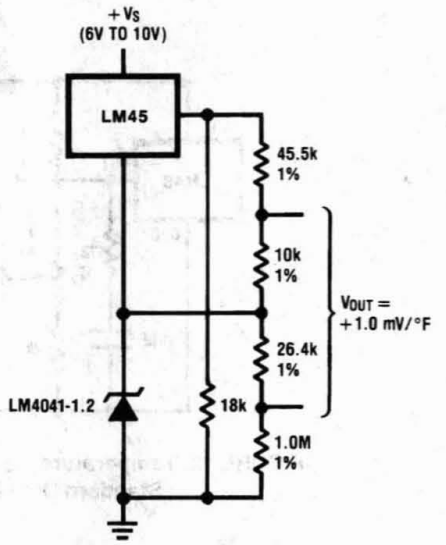

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FIGURE 8. Fahrenheit Thermometer

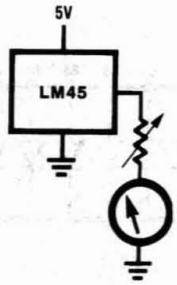

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FIGURE 9. Centigrade Thermometer (Analog Meter)

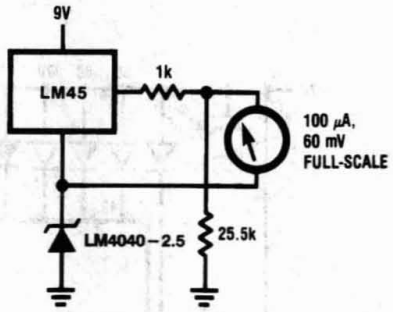

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FIGURE 10. Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)

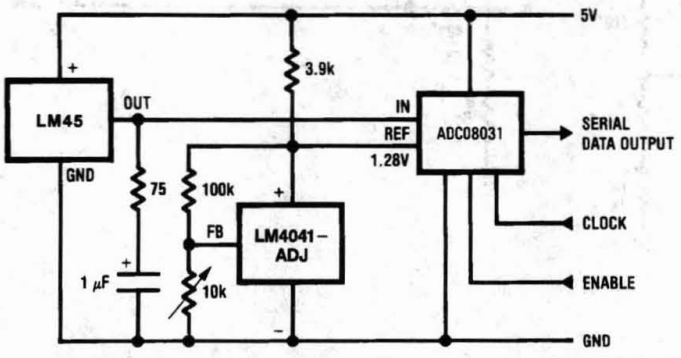

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FIGURE 11. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

Typical Applications (Continued)

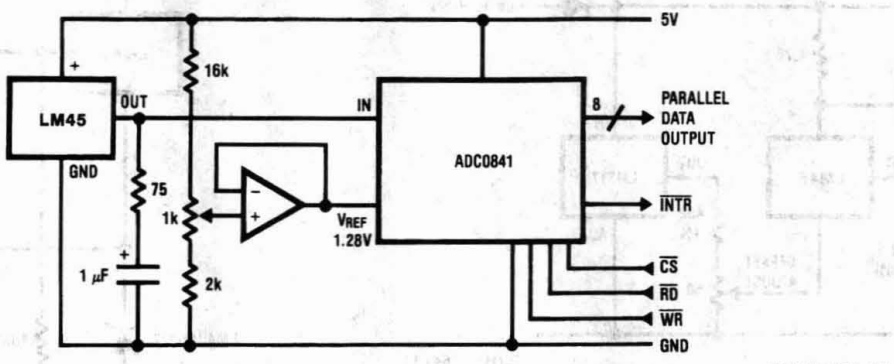

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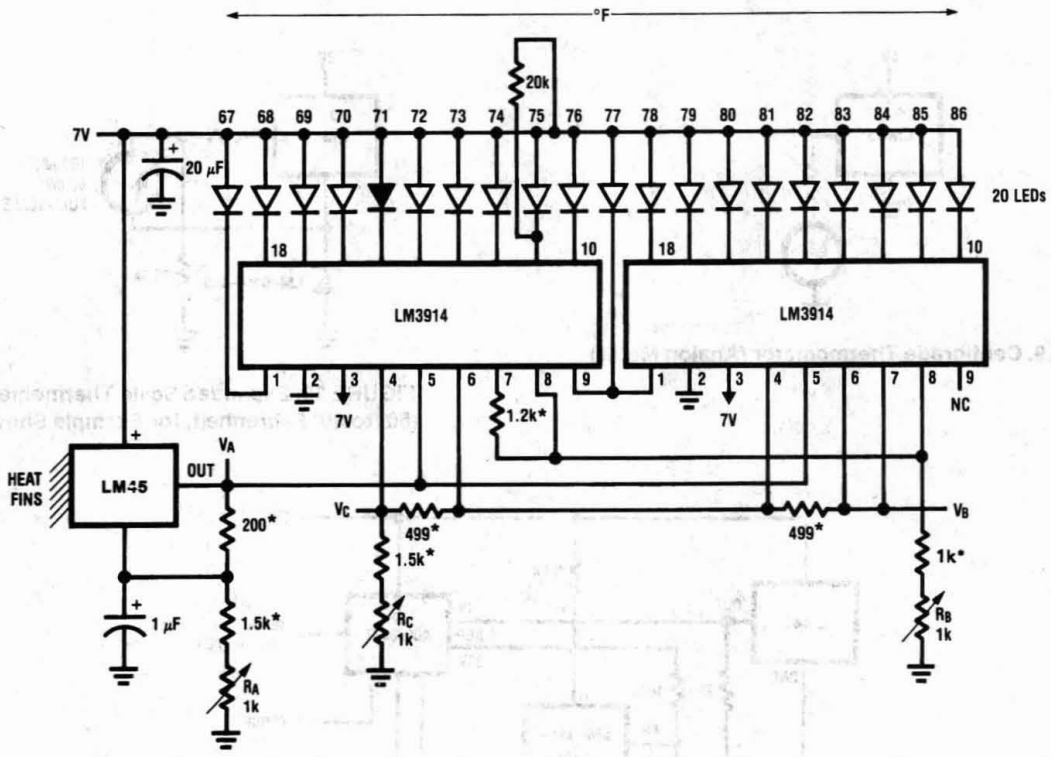
FIGURE 12. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (128°C Full Scale)



TL/H/11754–20

*=1% or 2% film resistor
-Trim R_B for $V_B = 3.075V$
-Trim R_C for $V_C = 1.955V$
-Trim R_A for $V_A = 0.075V + 100mV/°C \times T_{ambient}$
-Example, $V_A = 2.275V$ at 22°C

FIGURE 13. Bar-Graph Temperature Display (Dot Mode)

Typical Applications (Continued)

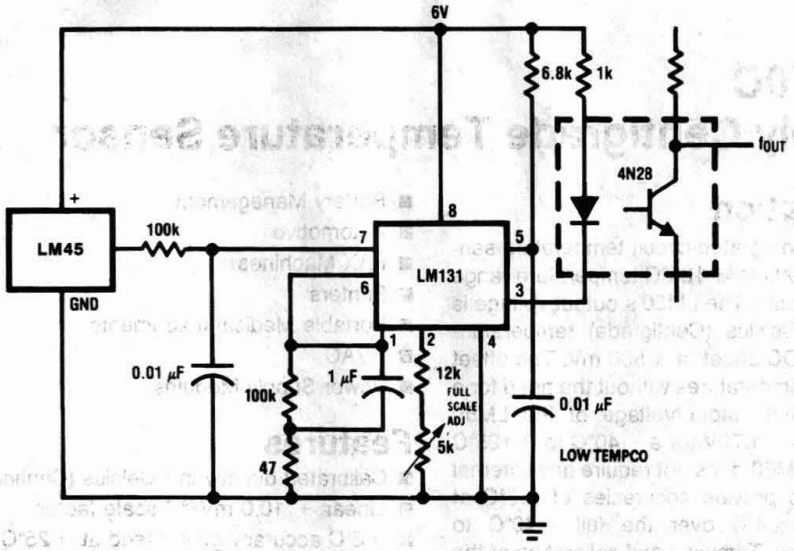


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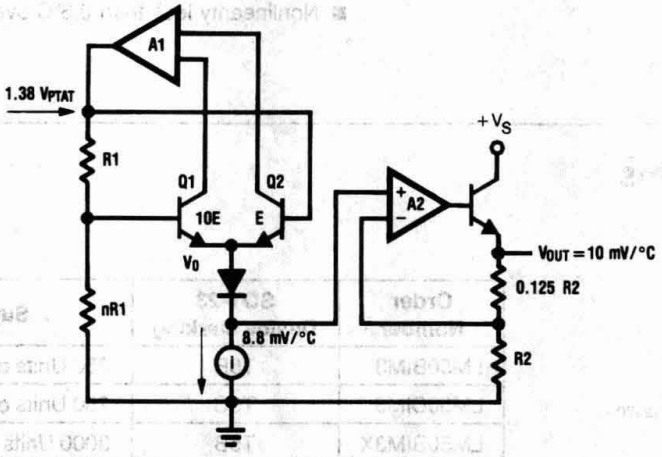
FIGURE 14. LM45 With Voltage-To-Frequency Converter And Isolated Output (2.5°C to +100°C; 25 Hz to 1000 Hz)

Block Diagram



TL/H/11754–22

National Semiconductor

ADVANCE INFORMATION

LM50B/LM50C
Single-Supply Centigrade Temperature Sensor

General Description

The LM50 is a precision integrated-circuit temperature sensor that can sense a −40°C to +125°C temperature range using a single positive supply. The LM50's output voltage is linearly proportional to Celsius (Centigrade) temperature (+10 mV/°C) and has a DC offset of +500 mV. The offset allows reading negative temperatures without the need for a negative supply. The ideal output voltage of the LM50 ranges from +100 mV to +1.75V for a −40°C to +125°C temperature range. The LM50 does not require any external calibration or trimming to provide accuracies of ±3°C at room temperature and ±4°C over the full −40°C to +125°C temperature range. Trimming and calibration of the LM50 at the wafer level assure low cost and high accuracy. The LM50's linear output, +500 mV offset, and factory calibration simplify circuitry required in a single supply environment where reading negative temperatures is required. Because the LM50's quiescent current is less than 130 μA, self-heating is limited to a very low 0.2°C in still air.

Applications

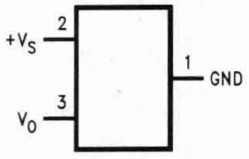
- Computers
- Disk Drives
- Battery Management
- Automotive
- FAX Machines
- Printers
- Portable Medical Instruments
- HVAC
- Power Supply Modules

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- ±2°C accuracy guaranteed at +25°C
- Specified for full −40° to +125°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4.5V to 10V
- Less than 130 μA current drain
- Low self-heating, less than 0.2°C in still air
- Nonlinearity less than 0.8°C over temp

Connection Diagrams

SOT-23



TL/H/12370–1

Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)

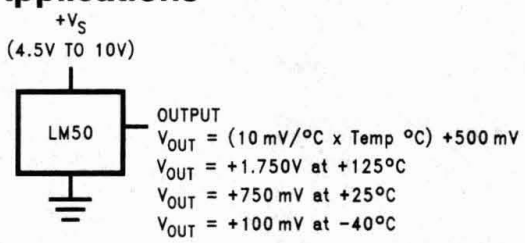
Order Number	SOT-23 Device Marking	Supplied As
LM50BIM3	T5B	250 Units on Tape and Reel
LM50CIM3	T5C	250 Units on Tape and Reel
LM50BIM3X	T5B	3000 Units on Tape and Reel
LM50CIM3X	T5C	3000 Units on Tape and Reel

TO-92
Plastic Package

TL/H/12370–2

Order Number LM50BIZ
or LM50CIZ
See NS Package Number Z03A

Typical Applications



TL/H/12370–3

FIGURE 1. Full-Range Centigrade Temperature Sensor (−40°C to +125°C)

National Semiconductor

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64 mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈ +0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM134-3/LM234-3 and LM134-6/LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

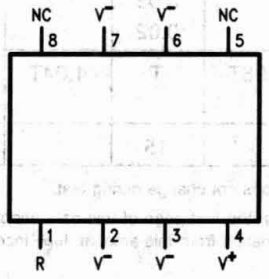
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic, TO-92 and SO-8 plastic packages.

Features

- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

Connection Diagrams

SO-8
Surface Mount Package



TL/H/5697–24

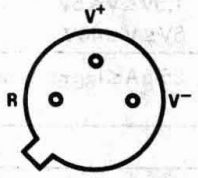
Order Number LM334M
See NS Package
Number M08A

SO-8 Alternative Pinout
Surface Mount Package

TL/H/5697–25

Order Number LM334SM
See NS Package
Number M08A

TO-46
Metal Can Package



TL/H/5697–12

Bottom View

V⁻ Pin is electrically connected to case.

Order Number LM134H,
LM134H-3, LM134H-6,
LM234H or LM334H
See NS Package
Number H03H

TO-92
Plastic Package

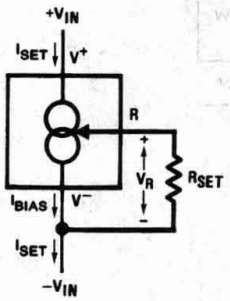
TL/H/5697–10

Bottom View

Order Number LM334Z,
LM234Z-3 or LM234Z-6
See NS Package
Number Z03A

Typical Application

Basic 2-Terminal Current Source



TL/H/5697–1

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^+ to V^- Forward Voltage	
LM134/LM234/LM334	40V
LM134-3/LM134-6/LM234-3/LM234-6	30V
V^+ to V^- Reverse Voltage	20V
R Pin to V^- Voltage	5V
Set Current	10 mA
Power Dissipation	400 mW
ESD Susceptibility (Note 5)	2000V

Operating Temperature Range (Note 4)	
LM134/LM134-3/LM134-6	−55°C to +125°C
LM234/LM234-3/LM234-6	−25°C to +100°C
LM334	0°C to +70°C
Soldering Information	
TO-92 Package (10 sec.)	260°C
TO-46 Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions	LM134/LM234			LM334			Units
		Min	Typ	Max	Min	Typ	Max	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$10\ \mu A \le I_{SET} \le 1$ mA			3			6	%
	1 mA $< I_{SET} \le 5$ mA			5			8	%
	$2\ \mu A \le I_{SET} < 10\ \mu A$			8			12	%
Ratio of Set Current to Bias Current	$100\ \mu A \le I_{SET} \le 1$ mA	14	18	23	14	18	26	
	1 mA $\le I_{SET} \le 5$ mA		14			14		
	$2\ \mu A \le I_{SET} \le 100\ \mu A$		18	23		18	26	
Minimum Operating Voltage	$2\ \mu A \le I_{SET} \le 100\ \mu A$		0.8			0.8		V
	$100\ \mu A < I_{SET} \le 1$ mA		0.9			0.9		V
	1 mA $< I_{SET} \le 5$ mA		1.0			1.0		V
Average Change in Set Current with Input Voltage	$2\ \mu A \le I_{SET} \le 1$ mA							
	$1.5V \le V^+ \le 5V$		0.02	0.05		0.02	0.1	%/V
	$5V \le V^+ \le 40V$		0.01	0.03		0.01	0.05	%/V
	1 mA $< I_{SET} \le 5$ mA							
	$1.5V \le V \le 5V$		0.03			0.03		%/V
	$5V \le V \le 40V$		0.02			0.02		%/V
Temperature Dependence of Set Current (Note 3)	$25\ \mu A \le I_{SET} \le 1$ mA	0.96T	T	1.04T	0.96T	T	1.04T	
Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25°C$ with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V^+ pin. For the Basic 2-Terminal Current Source circuit shown on the first page of this data sheet. I_{SET} is determined by the following formula: $I_{SET} = 67.7\ mV/R_{SET}$ (@ 25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ $T_j = 25°C$ (227 μV/°C).

Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: $I_{SET} = I_o\ (T/T_o)$ where I_o is I_{SET} measured at T_o (°K).

Note 4: For elevated temperature operation, T_j max is:

LM134	150°C
LM234	125°C
LM334	100°C

Thermal Resistance	TO-92	TO-46	SO-8
θ_{ja} (Junction to Ambient)	180°C/W (0.4" leads) 160°C/W (0.125" leads)	440°C/W	165°C/W
θ_{jc} (Junction to Case)	N/A	32°C/W	80°C/W

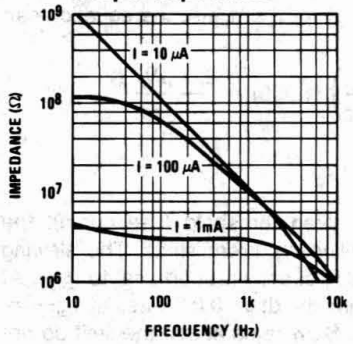
Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Electrical Characteristics (Note 1) (Continued)

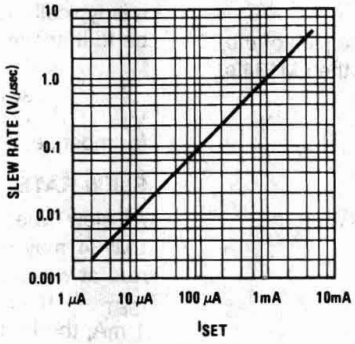
Parameter	Conditions	LM134-3, LM234-3			LM134-6, LM234-6			Units
		Min	Typ	Max	Min	Typ	Max	
Set Current Error, $V^+ = 2.5V$, (Note 2)	$100\ \mu A \le I_{SET} \le 1\ mA$, $T_j = 25°$			±1			±2	%
Equivalent Temperature Error				±3			±6	°C
Ratio of Set Current to Bias Current	$100\ \mu A \le I_{SET} \le 1\ mA$	14	18	26	14	18	26	
Minimum Operating Voltage	$100\ \mu A\ I_{SET} \le 1\ mA$		0.9			0.9		V
Average Change in Set Current with Input Voltage	$100\ \mu A \le I_{SET} \le 1\ mA$ $1.5 \le V^+ \le 5V$ $5V \le V^+ \le 30V$		 0.02 0.01	 0.05 0.03		 0.02 0.01	 0.01 0.05	 %/V %/V
Temperature Dependence of Set Current (Note 3) and	$100\ \mu A \le I_{SET} \le 1\ mA$	0.98T	T	1.02T	0.97T	T	1.03T	
Equivalent Slope Error				±2			±3	%
Effective Shunt Capacitance			15			15		pF

Typical Performance Characteristics

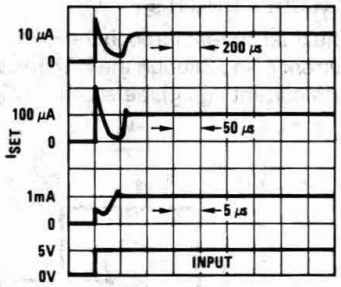
Output Impedance



Maximum Slew Rate for Linear Operation

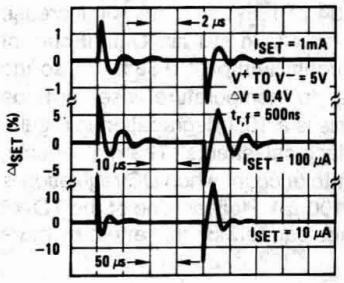


Start-Up



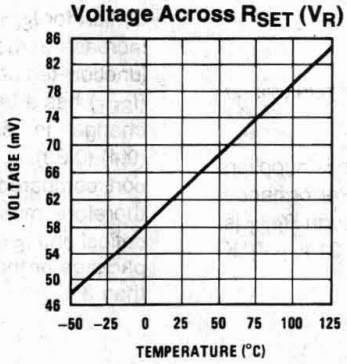
TIME (Note scale changes at each current level)

Transient Response

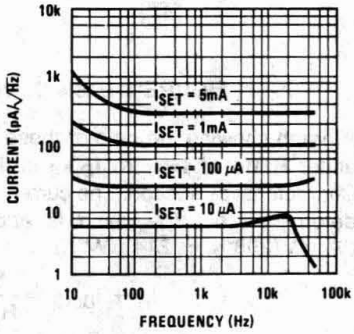


TIME (Note scale changes for each current)

Voltage Across R_{SET} (V_R)



Current Noise



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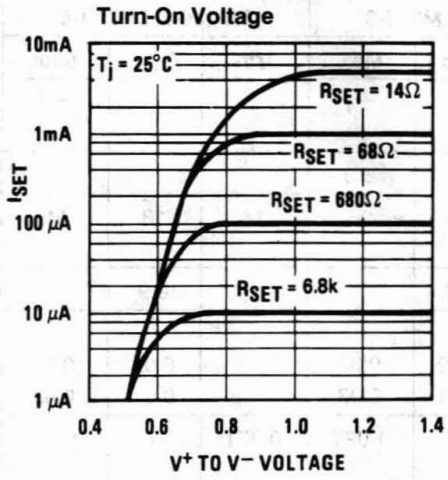
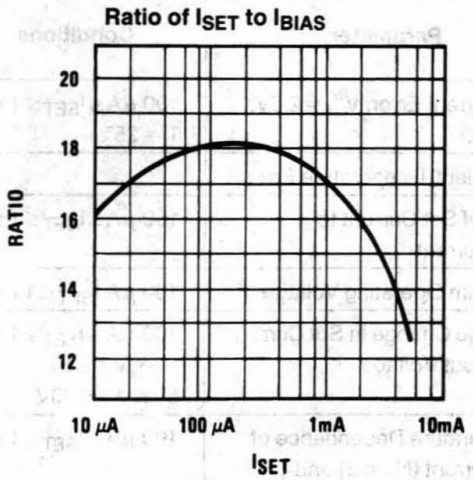
Typical Performance Characteristics (Continued)



TL/H/5697–29



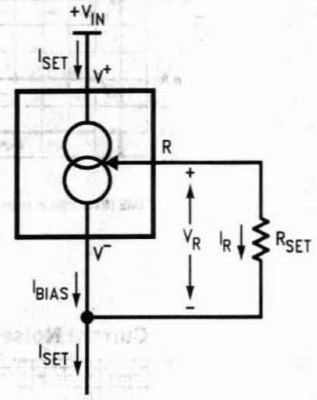
TL/H/5697–3

Application Hints

The LM134 has been designed for ease of application, but a general discussion of design features is presented here to familiarize the designer with device characteristics which may not be immediately obvious. These include the effects of slewing, power dissipation, capacitance, noise, and contact resistance.

CALCULATING R_{SET}

The total current through the LM134 (I_{SET}) is the sum of the current going through the SET resistor (I_R) and the LM134's bias current (I_{BIAS}), as shown in *Figure 1.*



TL/H/5697–27

FIGURE 1. Basic Current Source

A graph showing the ratio of these two currents is supplied under **Ratio of I_{SET} to I_{BIAS}** in the Typical Performance Characteristics section. The current flowing through R_{SET} is determined by V_R, which is approximately 214 μV/°K (64 mV/298°K ~ 214 μV/°K).

$$I_{SET} = I_R + I_{BIAS} = \frac{V_R}{R_{SET}} + I_{BIAS}$$

Since (for a given set current) I_{BIAS} is simply a percentage of I_{SET}, the equation can be rewritten

$$I_{SET} = \left(\frac{V_R}{R_{SET}}\right)\left(\frac{n}{n-1}\right)$$

where n is the ratio of I_{SET} to I_{BIAS} as specified in the Electrical Characteristics Section and shown in the graph. Since n is typically 18 for 2 μA ≤ I_{SET} ≤ 1 mA, the equation can be further simplified to

$$I_{SET} = \left(\frac{V_R}{R_{SET}}\right)(1.059) = \frac{227\ \mu V/°K}{R_{SET}}$$

for most set currents.

SLEW RATE

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET}. At I_{SET} = 10 μA, maximum dV/dt is 0.01V/μs; at I_{SET} = 1 mA, the limit is 1V/μs. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

THERMAL EFFECTS

Internal heating can have a significant effect on current regulation for I_{SET} greater than 100 μA. For example, each 1V increase across the LM134 at I_{SET} = 1 mA will increase junction temperature by ≈0.4°C in still air. Output current (I_{SET}) has a temperature coefficient of ≈0.33%/°C, so the change in current due to temperature rise will be (0.4) (0.33) = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds 100 μA. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

Application Hints (Continued)

SHUNT CAPACITANCE

In certain applications, the 15 pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET as shown in the applications. This can reduce capacitance to less than 3 pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage), are not affected.

NOISE

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12 dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

LEAD RESISTANCE

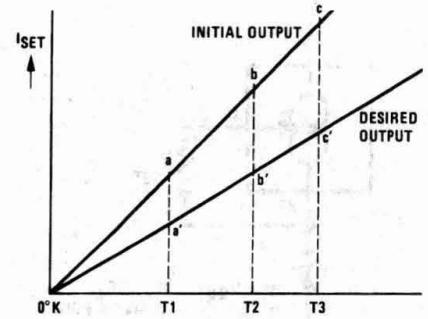
The sense voltage which determines operating current of the LM134 is less than 100 mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7Ω contact resistance to reduce output current by 1% at the 1 mA level.

SENSING TEMPERATURE

The LM134 makes an ideal remote temperature sensor because its current mode operation does not lose accuracy over long wire runs. Output current is directly proportional to absolute temperature in degrees Kelvin, according to the following formula:

$$I_{SET} = \frac{(227\ \mu V/°K)\ (T)}{R_{SET}}$$

Calibration of the LM134 is greatly simplified because of the fact that most of the initial inaccuracy is due to a gain term (slope error) and not an offset. This means that a calibration consisting of a gain adjustment only will trim both slope and zero at the same time. In addition, gain adjustment is a one point trim because the output of the LM134 extrapolates to zero at 0°K, independent of R_{SET} or any initial inaccuracy.



TL/H/5697–4

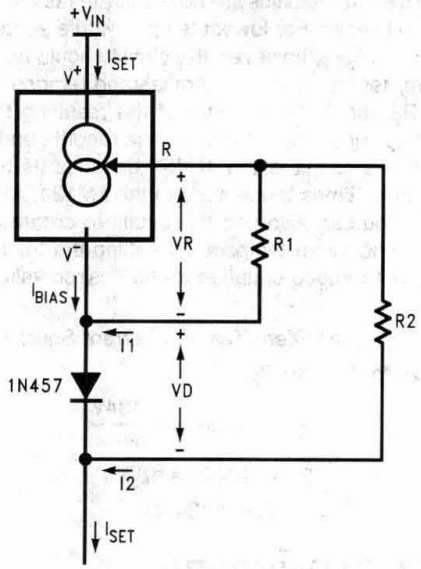
FIGURE 2. Gain Adjustment

This property of the LM134 is illustrated in the accompanying graph. Line abc is the sensor current before trimming. Line a'b'c' is the desired output. A gain trim done at T2 will move the output from b to b' and will simultaneously correct the slope so that the output at T1 and T3 will be correct. This gain trim can be done on R_{SET} or on the load resistor used to terminate the LM134. Slope error after trim will normally be less than ±1%. To maintain this accuracy, however, a low temperature coefficient resistor must be used for R_{SET}.

A 33 ppm/°C drift of R_{SET} will give a 1% slope error because the resistor will normally see about the same temperature variations as the LM134. Separating R_{SET} from the LM134 requires 3 wires and has lead resistance problems, so is not normally recommended. Metal film resistors with less than 20 ppm/°C drift are readily available. Wire wound resistors may also be used where best stability is required.

APPLICATION AS A ZERO TEMPERATURE COEFFICENT CURRENT SOURCE

Adding a diode and a resistor to the standard LM134 configuration can cancel the temperature-dependent characteristic of the LM134. The circuit shown in *Figure 3* balances the positive tempco of the LM134 (about +0.23 mV/°C) with the negative tempco of a forward-biased silicon diode (about −2.5 mV/°C).



TL/H/5697–28

FIGURE 3. Zero Tempco Current Source

The set current (I_{SET}) is the sum of I_1 and I_2, each contributing approximately 50% of the set current, and I_{BIAS}. I_{BIAS} is usually included in the I_1 term by increasing the V_R value used for calculations by 5.9%. (See **CALCULATING R_{SET}**.)

$$I_{SET} = I_1 + I_2 + I_{BIAS}, \text{ where}$$

$$I_1 = \frac{V_R}{R_1} \quad \text{and} \quad I_2 = \frac{V_R + V_D}{R_2}$$

The first step is to minimize the tempco of the circuit, using the following equations. An example is given using a value of +227 μV/°C as the tempco of the LM134 (which includes the I_{BIAS} component), and −2.5 mV/°C as the tempco of the diode (for best results, this value should be directly measured or obtained from the manufacturer of the diode).

$$I_{SET} = I_1 + I_2$$

$$\frac{dI_{SET}}{dT} = \frac{dI_1}{dT} + \frac{dI_2}{dT}$$

$$\approx \frac{227\ \mu V/°C}{R_1} + \frac{227\ \mu V/°C - 2.5\ mV/°C}{R_2}$$

$$= 0 \text{ (solve for tempco} = 0)$$

5

Application Hints (Continued)

$$\frac{R_2}{R_1} \approx \frac{2.5\ mV/°C - 227\ \mu V/°C}{227\ \mu V/°C} \approx 10.0$$

With the R_1 to R_2 ratio determined, values for R_1 and R_2 should be determined to give the desired set current. The formula for calculating the set current at T = 25°C is shown below, followed by an example that assumes the forward voltage drop across the diode (V_D) is 0.6V, the voltage across R_1 is 67.7 mV (64 mV + 5.9% to account for I_{BIAS}), and $R_2/R_1 = 10$ (from the previous calculations).

$$I_{SET} = I_1 + I_2 + I_{BIAS}$$
$$= \frac{V_R}{R_1} + \frac{V_R + V_D}{R_2}$$
$$\approx \frac{67.7\ mV}{R_1} + \frac{67.7\ mV + 0.6V}{10.0\ R_1}$$
$$I_{SET} \approx \frac{0.134V}{R_1}$$

This circuit will eliminate most of the LM134's temperature coefficient, and it does a good job even if the estimates of the diode's characteristics are not accurate (as the following example will show). For lowest tempco with a specific diode at the desired I_{SET}, however, the circuit should be built and tested over temperature. If the measured tempco of I_{SET} is positive, R_2 should be reduced. If the resulting tempco is negative, R_2 should be increased. The recommended diode for use in this circuit is the 1N457 because its tempco is centered at 11 times the tempco of the LM134, allowing $R_2 = 10\ R_1$. You can also use this circuit to create a current source with non-zero tempcos by setting the tempco component of the tempco equation to the desired value instead of 0.

EXAMPLE: A 1 mA, Zero-Tempco Current Source

First, solve for R_1 and R_2:

$$I_{SET} \approx 1\ mA = \frac{0.134V}{R_1}$$
$$R_1 = 134\Omega = 10\ R_2$$
$$R_2 = 1340\Omega$$

The values of R_1 and R_2 can be changed to standard 1% resistor values ($R_1 = 133\Omega$ and $R_2 = 1.33\ k\Omega$) with less than a 0.75% error.

If the forward voltage drop of the diode was 0.65V instead of the estimate of 0.6V (an error of 8%), the actual set current will be

$$I_{SET} = \frac{67.7\ mV}{R_1} + \frac{67.7\ mV + 0.65V}{R_2}$$
$$= \frac{67.7\ mV}{133} + \frac{67.7\ mV + 0.65V}{1330}$$
$$= 1.049\ mA$$

an error of less than 5%.

If the estimate for the tempco of the diode's forward voltage drop was off, the tempco cancellation is still reasonably effective. Assume the tempco of the diode is 2.6 mV/°C instead of 2.5 mV/°C (an error of 4%). The tempco of the circuit is now:

$$\frac{dI_{SET}}{dT} = \frac{dI_1}{dT} + \frac{dI_2}{dT}$$
$$= \frac{227\ \mu V/°C}{133\Omega} + \frac{227\ \mu V/°C - 2.6\ mV/°C}{1330\Omega}$$
$$= -77\ nA/°C$$

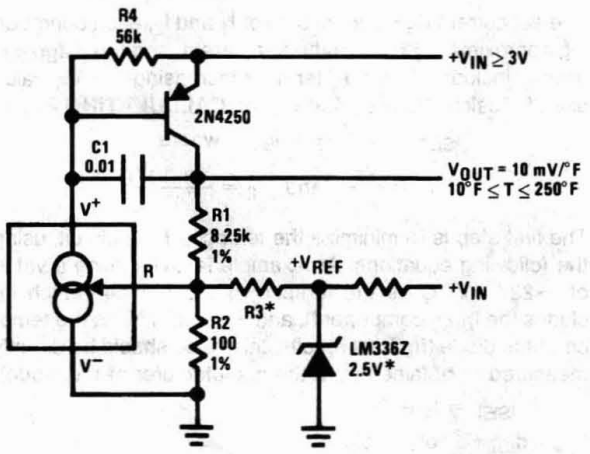
A 1 mA LM134 current source with no temperature compensation would have a set resistor of 68Ω and a resulting tempco of

$$\frac{227\ \mu V/°C}{68\Omega} = 3.3\ \mu A/°C$$

So even if the diode's tempco varies as much as ±4% from its estimated value, the circuit still eliminates 98% of the LM134's inherent tempco.

Typical Applications

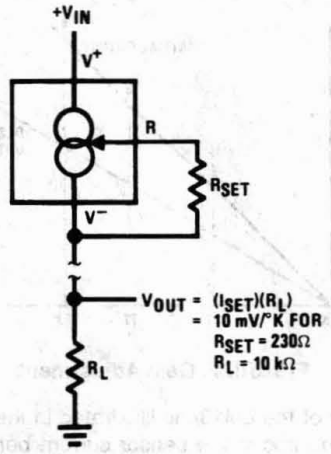
Ground Referred Fahrenheit Thermometer



TL/H/5697–15

*Select R3 = $V_{REF}/583\ \mu A$. V_{REF} may be any stable positive voltage ≥ 2V
Trim R3 to calibrate

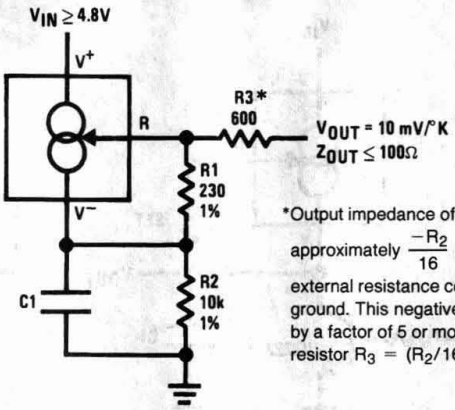
Terminating Remote Sensor for Voltage Output



TL/H/5697–14

Typical Applications (Continued)

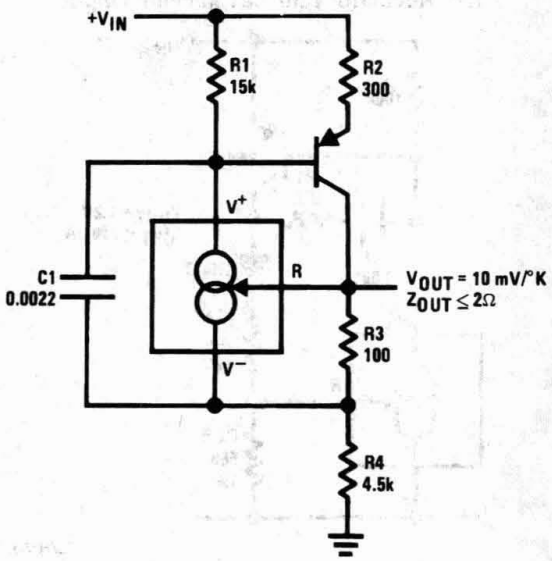
Low Output Impedance Thermometer



*Output impedance of the LM134 at the "R" pin is approximately $\frac{-R_2}{16}$ where R_2 is the equivalent external resistance connected from the V⁻ pin to ground. This negative resistance can be reduced by a factor of 5 or more by inserting an equivalent resistor $R_3 = (R_2/16)$ in series with the output.

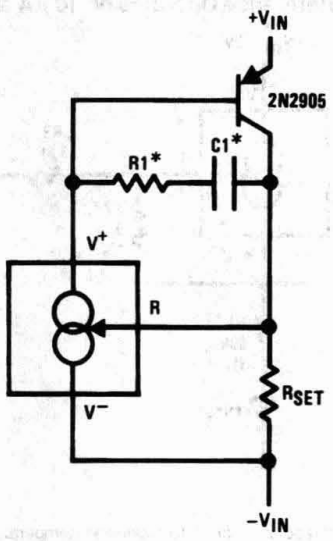
TL/H/5697–6

Low Output Impedance Thermometer



TL/H/5697–16

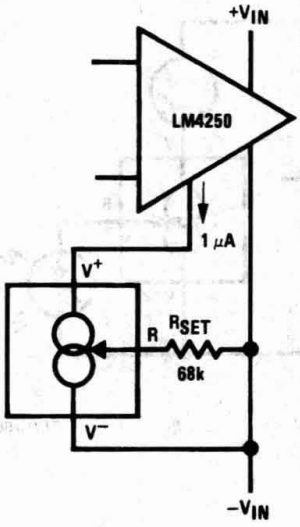
Higher Output Current



TL/H/5697–5

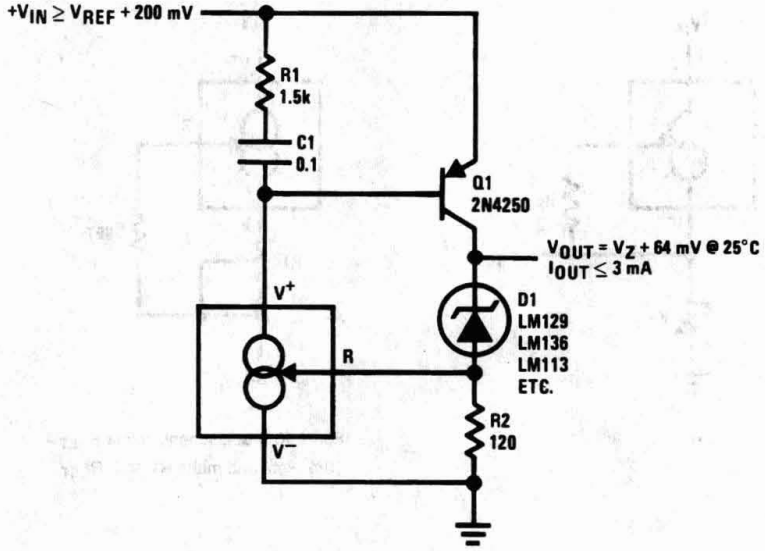
*Select R1 and C1 for optimum stability

Micropower Bias



TL/H/5697–17

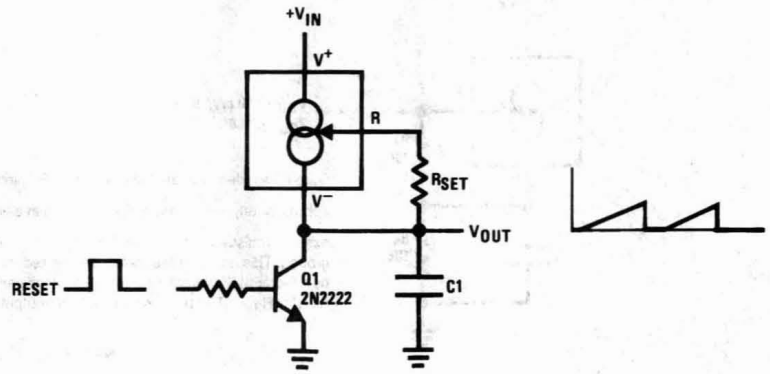
Low Input Voltage Reference Driver



TL/H/5697–18

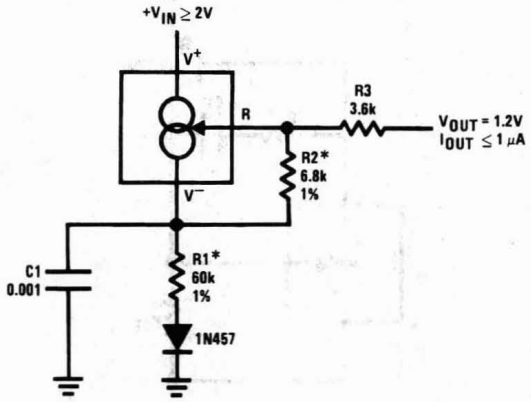
Typical Applications (Continued)

Ramp Generator



TL/H/5697–19

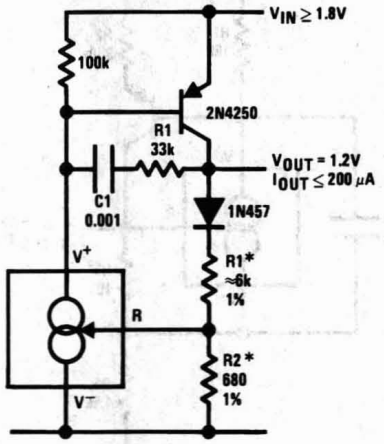
1.2V Reference Operates on 10 μA and 2V



TL/H/5697–20

*Select ratio of R1 to R2 to obtain zero temperature drift

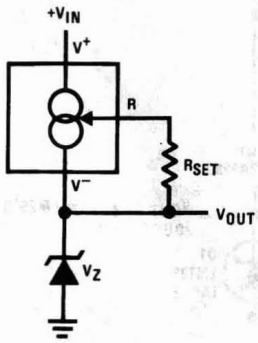
1.2V Regulator with 1.8V Minimum Input



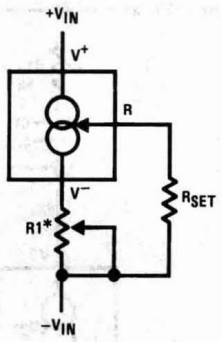
TL/H/5697–7

*Select ratio of R1 to R2 for zero temperature drift

Zener Biasing

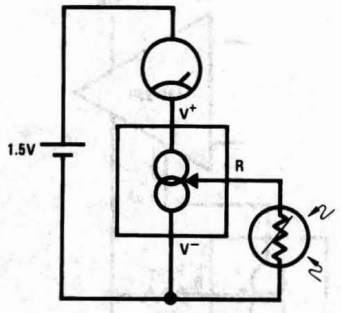


Alternate Trimming Technique



*For ±10% adjustment, select R_{SET} 10% high, and make R1 ≈ 3 R_{SET}

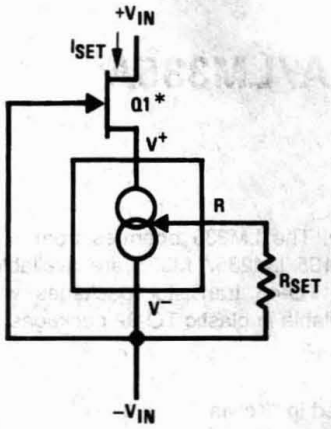
Buffer for Photoconductive Cell



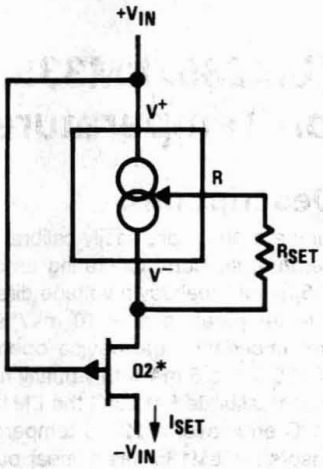
TL/H/5697–8

Typical Applications (Continued)

FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



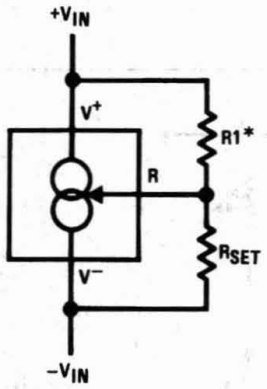
TL/H/5697–21



TL/H/5697–22

*Select Q1 or Q2 to ensure at least 1V across the LM134. $V_p\ (1 - I_{SET}/I_{DSS}) \geq 1.2V$.

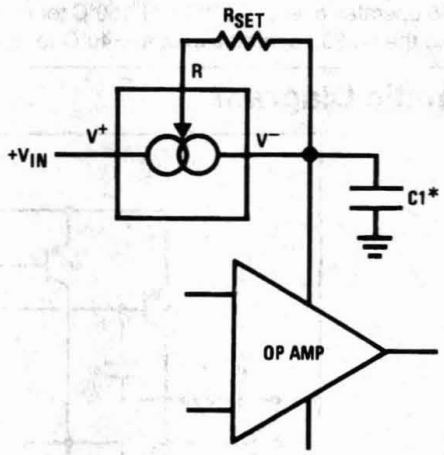
Generating Negative Output Impedance



TL/H/5697–23

*$Z_{OUT} \approx -16 \bullet$ R1 (R1/V_{IN} must not exceed I_{SET})

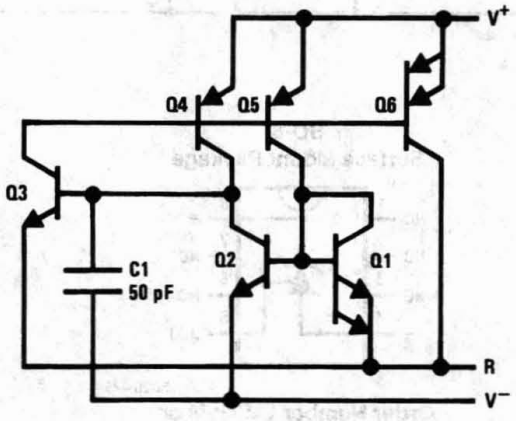
In-Line Current Limiter



TL/H/5697–9

*Use minimum value required to ensure stability of protected device. This minimizes inrush current to a direct short.

Schematic Diagram



TL/H/5697–11

National Semiconductor

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

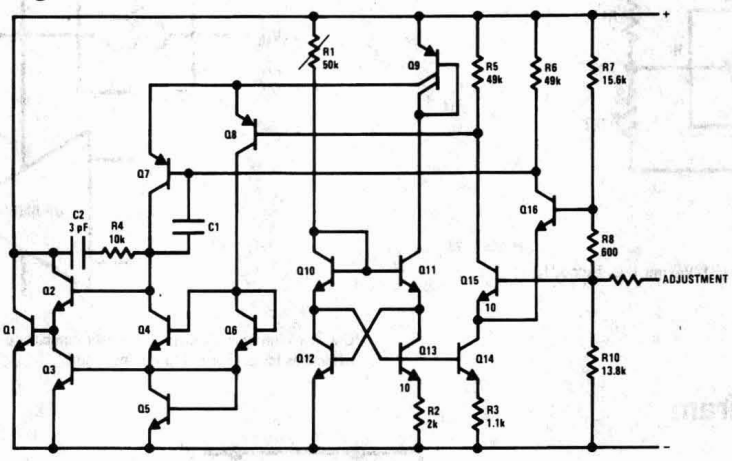
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

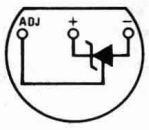
Schematic Diagram



TL/H/5698–1

Connection Diagrams

TO-92
Plastic Package

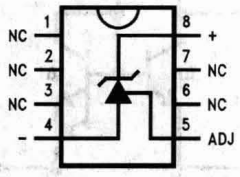


TL/H/5698–8

Bottom View

Order Number LM335Z or LM335AZ
See NS Package Number Z03A

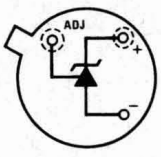
SO-8
Surface Mount Package



TL/H/5698–25

Order Number LM335M or LM335AM
See NS Package Number M08A

TO-46
Metal Can Package*



TL/H/5698–26

Bottom View

*Case is connected to negative pin

Order Number LM135H, LM135H-MIL, LM235H, LM335H, LM135AH, LM235AH or LM335AH
See NS Package Number H03H

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Reverse Current	15 mA
Forward Current	10 mA
Storage Temperature	
TO-46 Package	−60°C to +180°C
TO-92 Package	−60°C to +150°C
SO-8 Package	−65°C to +150°C

Specified Operating Temp. Range

	Continuous	Intermittent (Note 2)
LM135, LM135A	−55°C to +150°C	150°C to 200°C
LM235, LM235A	−40°C to +125°C	125°C to 150°C
LM335, LM335A	−40°C to +100°C	100°C to 125°C

Lead Temp. (Soldering, 10 seconds)	
TO-92 Package:	260°C
TO-46 Package:	300°C
SO-8 Package:	300°C
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Temperature Accuracy LM135/LM235, LM135A/LM235A (Note 1)

Parameter	Conditions	LM135A/LM235A			LM135/LM235			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Output Voltage	T_C = 25°C, I_R = 1 mA	2.97	2.98	2.99	2.95	2.98	3.01	V
Uncalibrated Temperature Error	T_C = 25°C, I_R = 1 mA		0.5	1		1	3	°C
Uncalibrated Temperature Error	$T_{MIN} \le T_C \le T_{MAX}$, I_R = 1 mA		1.3	2.7		2	5	°C
Temperature Error with 25°C Calibration	$T_{MIN} \le T_C \le T_{MAX}$, I_R = 1 mA		0.3	1		0.5	1.5	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	I_R = 1 mA		0.3	0.5		0.3	1	°C

Temperature Accuracy LM335, LM335A (Note 1)

Parameter	Conditions	LM335A			LM335			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Output Voltage	T_C = 25°C, I_R = 1 mA	2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error	T_C = 25°C, I_R = 1 mA		1	3		2	6	°C
Uncalibrated Temperature Error	$T_{MIN} \le T_C \le T_{MAX}$, I_R = 1 mA		2	5		4	9	°C
Temperature Error with 25°C Calibration	$T_{MIN} \le T_C \le T_{MAX}$, I_R = 1 mA		0.5	1		1	2	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	I_R = 1 mA		0.3	1.5		0.3	1.5	°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM135/LM235 LM135A/LM235A			LM335 LM335A			Units
		Min	Typ	Max	Min	Typ	Max	
Operating Output Voltage Change with Current	400 μA ≤ I_R ≤ 5 mA At Constant Temperature		2.5	10		3	14	mV
Dynamic Impedance	I_R = 1 mA		0.5			0.6		Ω
Output Voltage Temperature Coefficient			+10			+10		mV/°C
Time Constant	Still Air 100 ft/Min Air Stirred Oil		80 10 1			80 10 1		sec sec sec
Time Stability	T_C = 125°C		0.2			0.2		°C/khr

Note 1: Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

Note 2: Continuous operation at these temperatures for 10,000 hours for H package and 5,000 hours for Z package may decrease life expectancy of the device.

Note 3: Thermal Resistance

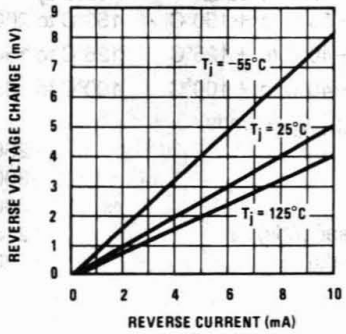
	TO-92	TO-46	SO-8
θ_{JA} (junction to ambient)	202°C/W	400°C/W	165°C/W
θ_{JC} (junction to case)	170°C/W	N/A	N/A

Note 4: Refer to RETS135H for military specifications.

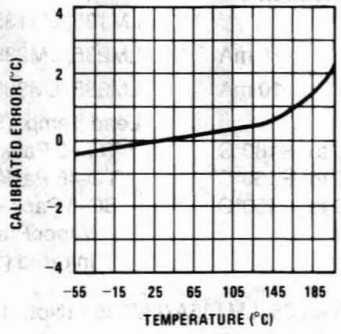
5

Typical Performance Characteristics

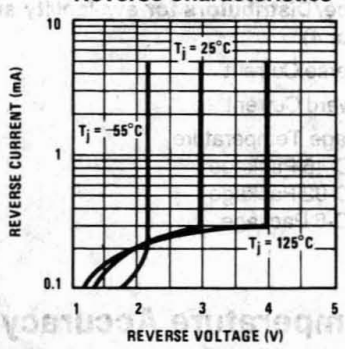
Reverse Voltage Change



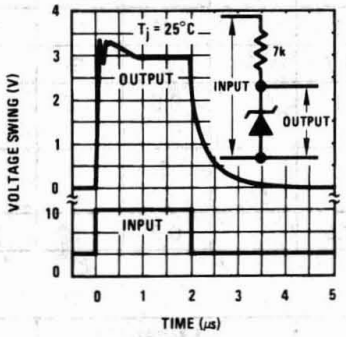
Calibrated Error



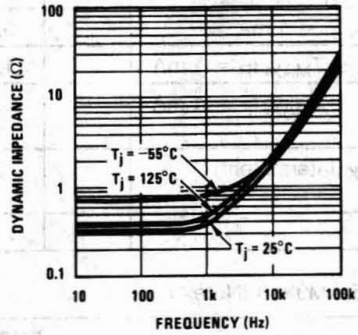
Reverse Characteristics



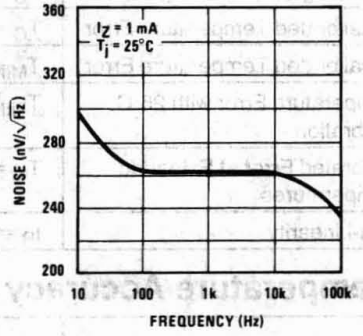
Response Time



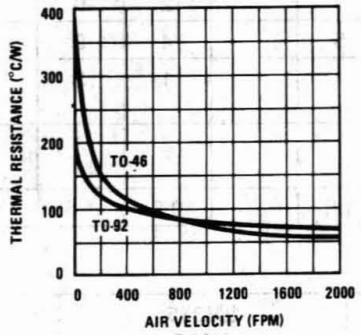
Dynamic Impedance



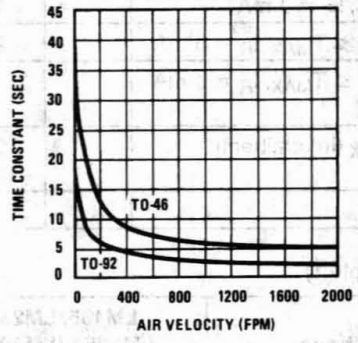
Noise Voltage



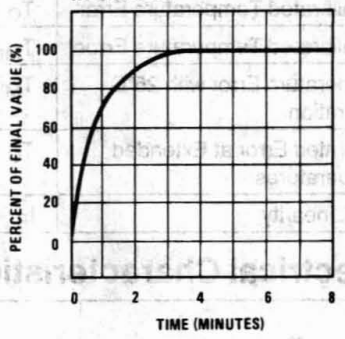
Thermal Resistance Junction to Air



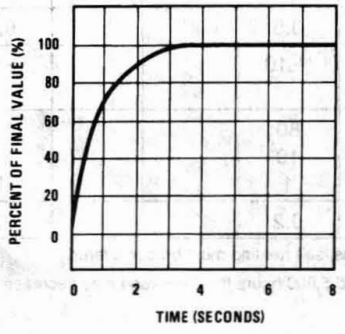
Thermal Time Constant



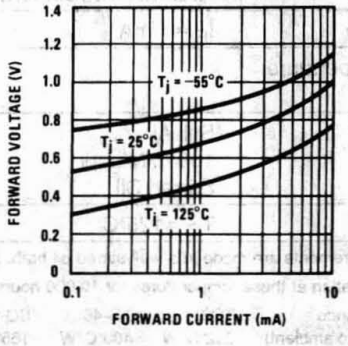
Thermal Response in Still Air



Thermal Response in Stirred Oil Bath



Forward Characteristics



TL/H/5698–3

Application Hints

CALIBRATING THE LM135

Included on the LM135 chip is an easy method of calibrating the device for higher accuracies. A pot connected across the LM135 with the arm tied to the adjustment terminal allows a 1-point calibration of the sensor that corrects for inaccuracy over the full temperature range.

This single point calibration works because the output of the LM135 is proportional to absolute temperature with the extrapolated output of sensor going to 0V output at 0°K (−273. 15°C). Errors in output voltage versus temperature are only slope (or scale factor) errors so a slope calibration at one temperature corrects at all temperatures.

The output of the device (calibrated or uncalibrated) can be expressed as:

$$V_{OUT_T} = V_{OUT_{T_o}} \times \frac{T}{T_o}$$

where T is the unknown temperature and T_o is a reference temperature, both expressed in degrees Kelvin. By calibrating the output to read correctly at one temperature the output at all temperatures is correct. Nominally the output is calibrated at 10 mV/°K.

To insure good sensing accuracy several precautions must be taken. Like any temperature sensing device, self heating can reduce accuracy. The LM135 should be operated at the lowest current suitable for the application. Sufficient current, of course, must be available to drive both the sensor and the calibration pot at the maximum operating temperature as well as any external loads.

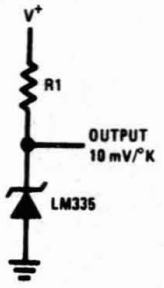
If the sensor is used in an ambient where the thermal resistance is constant, self heating errors can be calibrated out. This is possible if the device is run with a temperature stable current. Heating will then be proportional to zener voltage and therefore temperature. This makes the self heating error proportional to absolute temperature the same as scale factor errors.

WATERPROOFING SENSORS

Meltable inner core heat shrinkable tubing such as manufactured by Raychem can be used to make low-cost waterproof sensors. The LM335 is inserted into the tubing about ½" from the end and the tubing heated above the melting point of the core. The unfilled ½" end melts and provides a seal over the device.

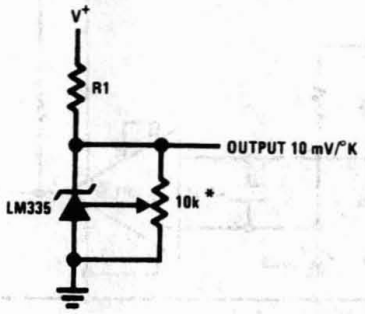
Typical Applications

Basic Temperature Sensor



TL/H/5698–2

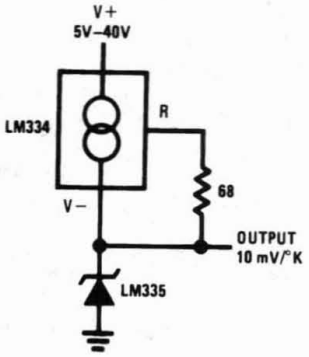
Calibrated Sensor



TL/H/5698–9

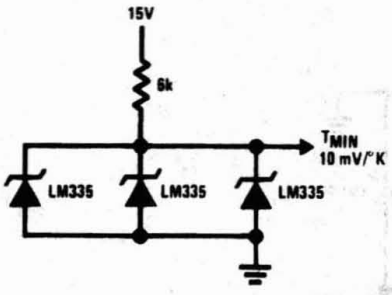
*Calibrate for 2.982V at 25°C

Wide Operating Supply



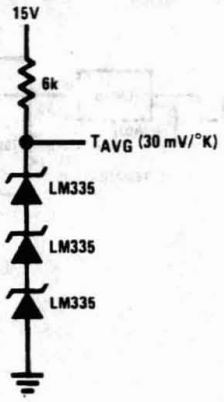
TL/H/5698–10

Minimum Temperature Sensing



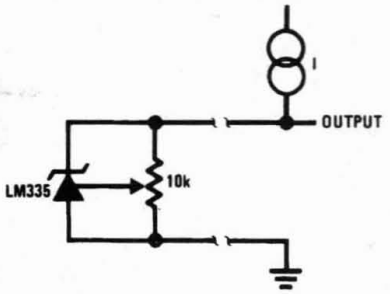
TL/H/5698–4

Average Temperature Sensing



TL/H/5698–18

Remote Temperature Sensing



TL/H/5698–19

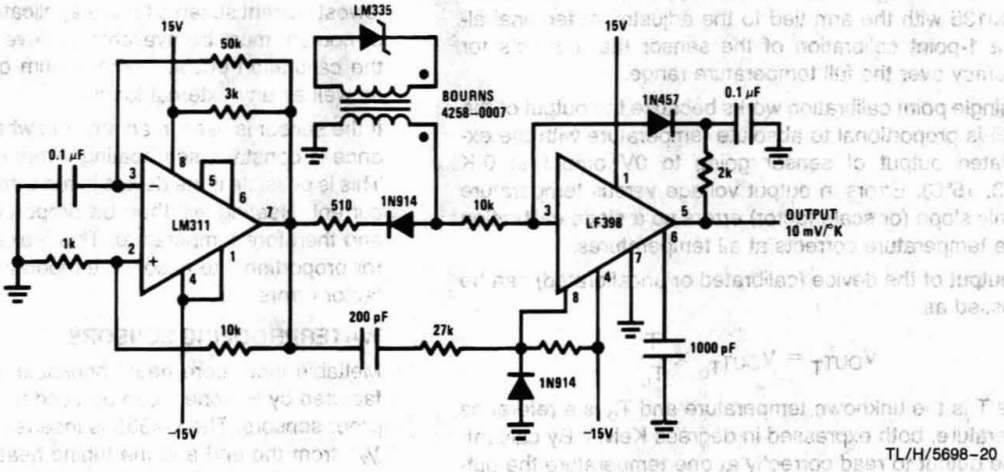
Wire length for 1°C error due to wire drop

AWG	I_R = 1 mA FEET	I_R = 0.5 mA* FEET
14	4000	8000
16	2500	5000
18	1600	3200
20	1000	2000
22	625	1250
24	400	800

*For I_R = 0.5 mA, the trim pot must be deleted.

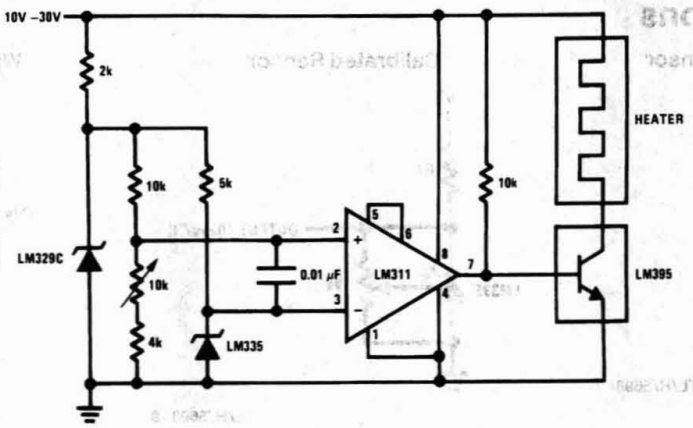
Typical Applications (Continued)

Isolated Temperature Sensor



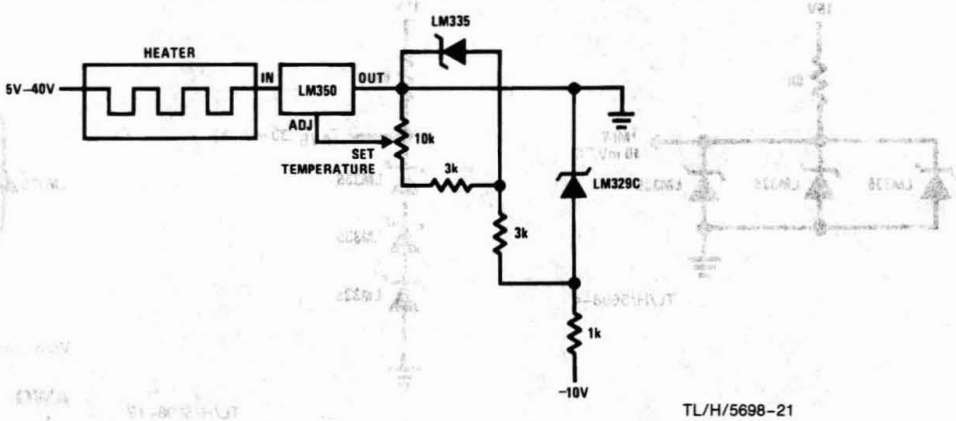
TL/H/5698-20

Simple Temperature Controller



TL/H/5698-5

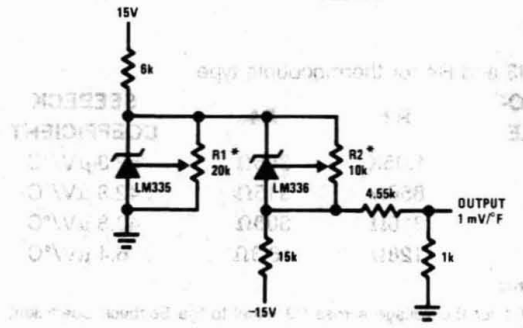
Simple Temperature Control



TL/H/5698-21

Typical Applications (Continued)

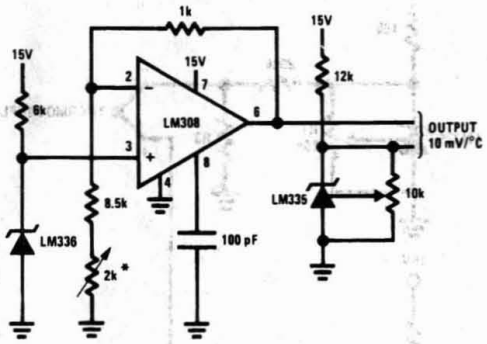
Ground Referred Fahrenheit Thermometer



TL/H/5698–22

*Adjust R2 for 2.554V across LM336.
Adjust R1 for correct output.

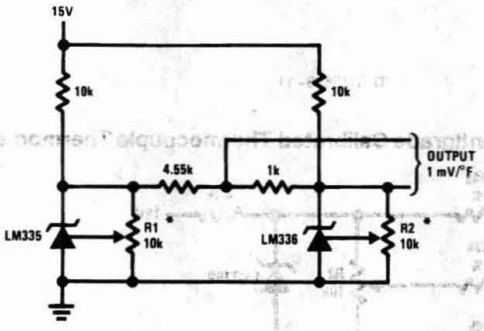
Centigrade Thermometer



TL/H/5698–23

*Adjust for 2.7315V at output of LM308

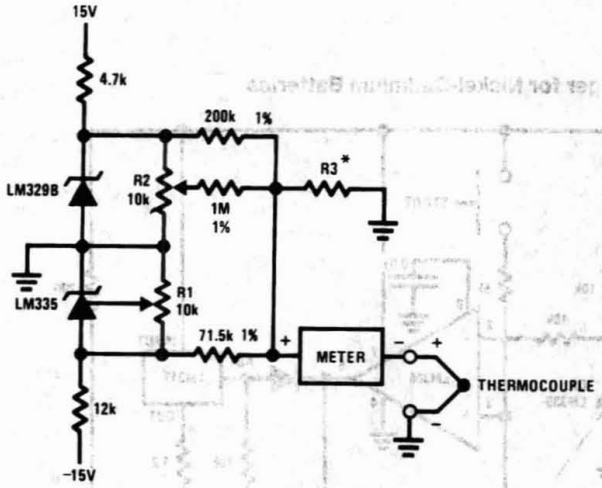
Fahrenheit Thermometer



TL/H/5698–24

*To calibrate adjust R2 for 2.554V across LM336.
Adjust R1 for correct output.

THERMOCOUPLE COLD JUNCTION COMPENSATION
Compensation for Grounded Thermocouple



TL/H/5698–6

*Select R3 for proper thermocouple type

THERMOCOUPLE	R3 (±1%)	SEEBECK COEFFICIENT
J	377Ω	52.3 μV/°C
T	308Ω	42.8 μV/°C
K	293Ω	40.8 μV/°C
S	45.8Ω	6.4 μV/°C

Adjustments: Compensates for both sensor and resistor tolerances

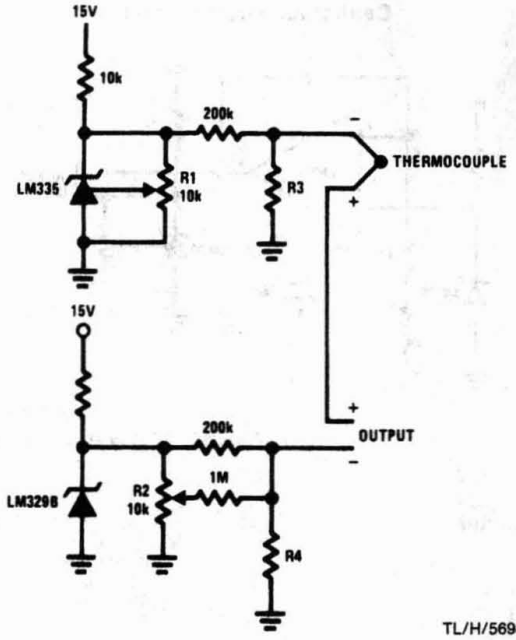
1. Short LM329B
2. Adjust R1 for Seebeck Coefficient times ambient temperature (in degrees K) across R3.
3. Short LM335 and adjust R2 for voltage across R3 corresponding to thermocouple type

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

5

Typical Applications (Continued)

Single Power Supply Cold Junction Compensation



TL/H/5698–11

*Select R3 and R4 for thermocouple type

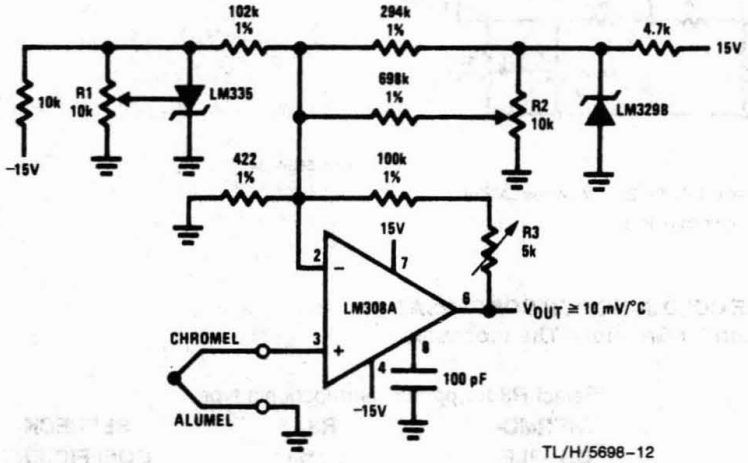
THERMOCOUPLE	R3	R4	SEEBECK COEFFICIENT
J	1.05K	385Ω	52.3 μV/°C
T	856Ω	315Ω	42.8 μV/°C
K	816Ω	300Ω	40.8 μV/°C
S	128Ω	46.3Ω	6.4 μV/°C

Adjustments:

1. Adjust R1 for the voltage across R3 equal to the Seebeck Coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 corresponding to thermocouple

J	14.32 mV
T	11.79 mV
K	11.17 mV
S	1.768 mV

Centigrade Calibrated Thermocouple Thermometer



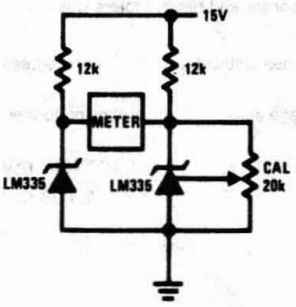
TL/H/5698–12

Terminate thermocouple reference junction in close proximity to LM335.

Adjustments:

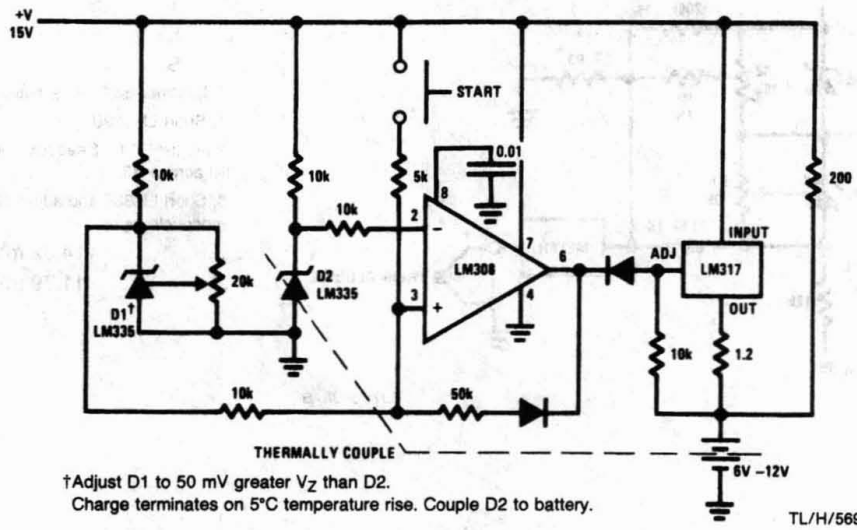
1. Apply signal in place of thermocouple and adjust R3 for a gain of 245.7.
2. Short non-inverting input of LM308A and output of LM329B to ground.
3. Adjust R1 so that V_{OUT} = 2.982V @ 25°C.
4. Remove short across LM329B and adjust R2 so that V_{OUT} = 246 mV @ 25°C.
5. Remove short across thermocouple.

Differential Temperature Sensor



TL/H/5698–7

Fast Charger for Nickel-Cadmium Batteries

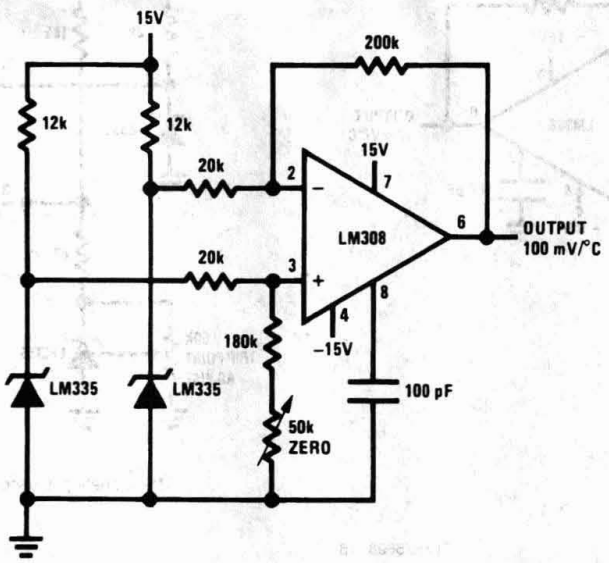


†Adjust D1 to 50 mV greater V_Z than D2.
Charge terminates on 5°C temperature rise. Couple D2 to battery.

TL/H/5698–13

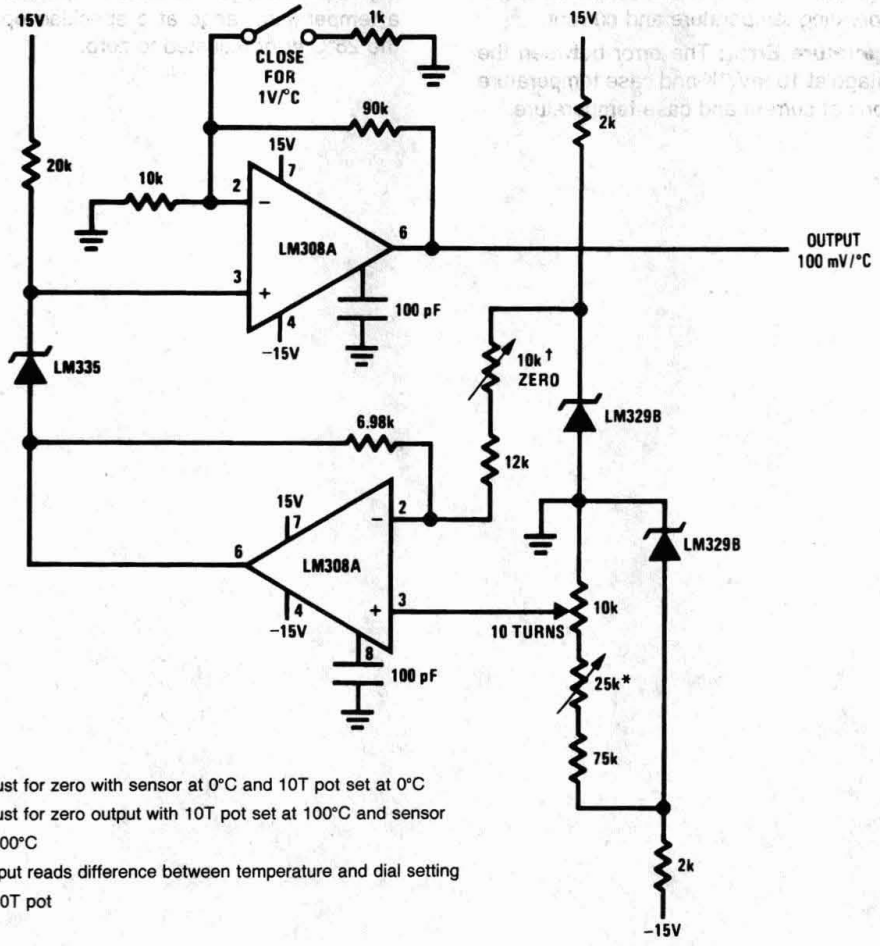
Typical Applications (Continued)

Differential Temperature Sensor



TL/H/5698–14

Variable Offset Thermometer‡



†Adjust for zero with sensor at 0°C and 10T pot set at 0°C

*Adjust for zero output with 10T pot set at 100°C and sensor at 100°C

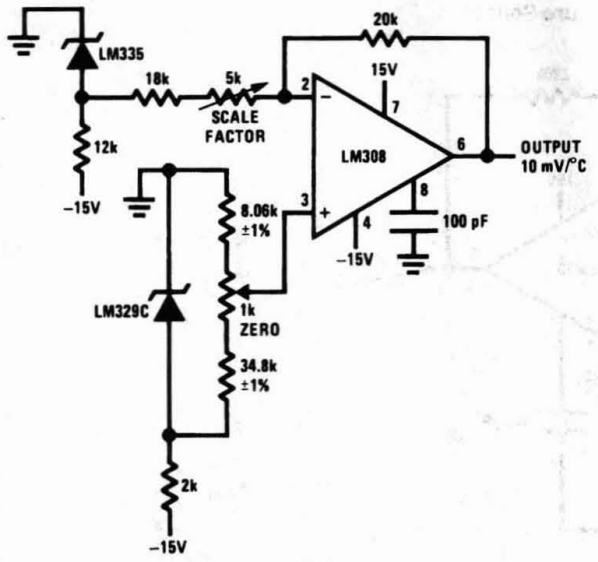
‡Output reads difference between temperature and dial setting of 10T pot

TL/H/5698–15

5

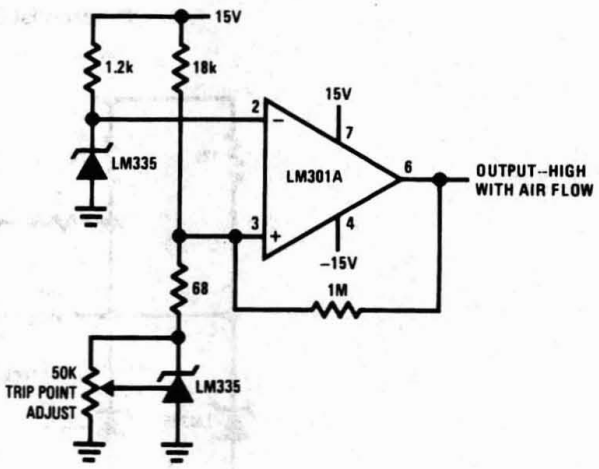
Typical Applications (Continued)

Ground Referred Centigrade Thermometer



TL/H/5698–16

Air Flow Detector*



TL/H/5698–17

*Self heating is used to detect air flow

Definition of Terms

Operating Output Voltage: The voltage appearing across the positive and negative terminals of the device at specified conditions of operating temperature and current.

Uncalibrated Temperature Error: The error between the operating output voltage at 10 mV/°K and case temperature at specified conditions of current and case temperature.

Calibrated Temperature Error: The error between operating output voltage and case temperature at 10 mV/°K over a temperature range at a specified operating current with the 25°C error adjusted to zero.

Section 6

Sample and Hold

Section 6 Contents

Sample and Hold Definition of Terms 6-3
Sample and Hold Selection Guide 6-4
LF198/LF298/LF398/LF198A/LF398A Monolithic Sample and Hold Circuits 6-5
LF13006/LF13007 Digital Gain Set 6-15

Sample and Hold Definition of Terms

Acquisition Time: The time required to acquire a new analog input voltage once a sample command has been given. A signal is "acquired" when it has settled within a specified error band around its final value of output voltage. The maximum value of the acquisition time occurs when the hold capacitor must change to a full-scale voltage change. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Jetter: The uncertainty in the aperture time. Aperture jitter results from noise which is superimposed on the hold command which affects its timing.

Aperture Time (Aperture Delay): The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

Droop Rate: The rate at which the output voltage is changing in hold mode as a result of leakage from the hold capacitor.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Feedthrough Attenuation Ratio: The fraction of the input signal that appears at the output while the S/H is in hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Capacitor Leakage Current: The current which flows into or out of the hold capacitor while the S/H is in hold mode.

Hold Settling Time: The time required for the output to settle within a specified error band after the "hold" logic command has been given.

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage.

Sample-to-Hold Transient: The transient that appears at the output due to a sample-to-hold transition.

National Semiconductor

Sample and Hold Selection Guide

	LF198A	LF398A	LF198	LF398	LF298	Units
Accuracy Gain/Offset Error	0.01	0.01	0.02	0.02	0.02	% Max
Offset Voltage	2	3	5	10	5	mV Max
Droop Rate (25°C)						
C_S = 1000 pF	30	30	30	30	30	mV/sec
C_S = 10000 pF	3	3	3	3	3	
Acquisition Time (25°C)						
C_S = 1000 pF	4	4	4	4	4	μs
C_S = 10000 pF	20	20	20	20	20	
Aperture Time (25°C)	250	250	250	250	250	ns
Temperature Range	−55 to +125	0 to +70	−55 to +125	0 to +70	−25 to +85	°C
Comment	Low Drift	Low Drift	General Purpose	General Purpose	Low Drift	

National Semiconductor

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

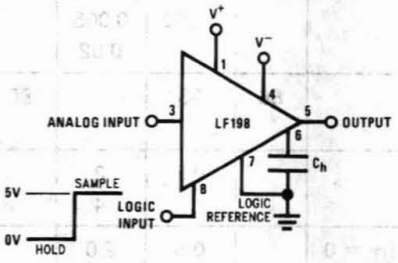
Features

- Operates from $\pm$5V to $\pm$18V supplies
- Less than 10 μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified

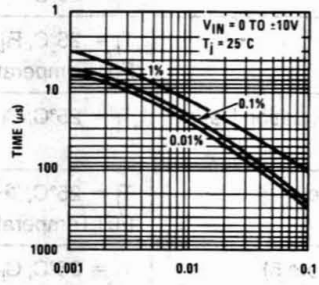
Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from $\pm$5V to $\pm$18V supplies.

An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve



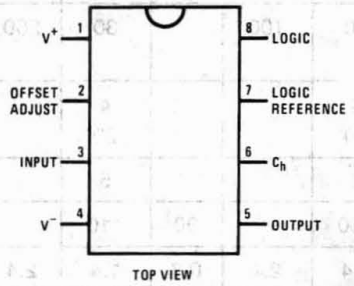
Acquisition Time



TL/H/5692–2

Connection Diagrams

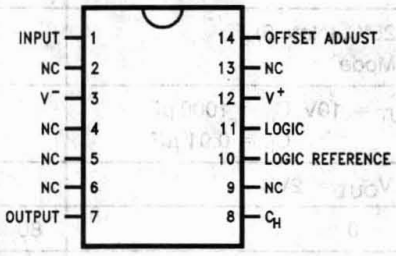
Dual-In-Line Package



TL/H/5692–11

Order Number LF398N or LF398AN
See NS Package Number N08E

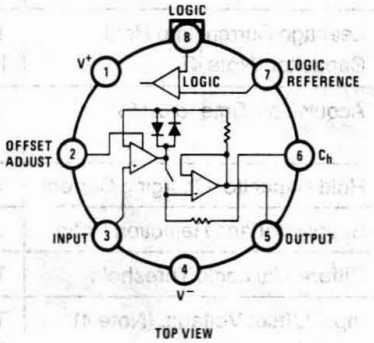
Small-Outline Package



TL/H/5692–15

Order Number LF298M or LF398M
See NS Package Number M14A

Metal Can Package



TL/H/5692–14

Order Number LF198H,
LF198H/883, LF298H,
LF398H, LF198AH or LF398AH
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 1)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec

Lead Temperature (Note 3)	
H package (Soldering, 10 sec.)	260°C
N package (Soldering, 10 sec.)	260°C
M package:	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Thermal Resistance (θ_{JA}) (typicals)	
H package	215°C/W (Board mount in still air)
	85°C/W (Board mount in 400LF/min air flow)
N package	115°C/W
M package	106°C/W
θ_{JC} (H package, typical)	20°C/W

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 4)	$T_j = 25°C$ Full Temperature Range		1	3 5		2	7 10	mV mV
Input Bias Current, (Note 4)	$T_j = 25°C$ Full Temperature Range		5	25 75		10	50 100	nA nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$ Full Temperature Range		0.002	0.005 0.02		0.004	0.01 0.02	% %
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode Full Temperature Range		0.5	2 4		0.5	4 6	Ω Ω
"HOLD" Step, (Note 5)	$T_j = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 4)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 4)	$T_j = 25°C$, (Note 6) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000\ pF$ $C_h = 0.01\ \mu F$		4 20			4 20		μs μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V
Input Offset Voltage, (Note 4)	$T_j = 25°C$ Full Temperature Range		1	1 2		2	2 3	mV mV
Input Bias Current, (Note 4)	$T_j = 25°C$ Full Temperature Range		5	25 75		10	25 50	nA nA

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$, $^+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified. (Continued)

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$ Full Temperature Range		0.002	0.005 0.01		0.004	0.005 0.01	% %
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode Full Temperature Range		0.5	1 4		0.5	1 6	Ω Ω
"HOLD" Step, (Note 5)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 4)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 4)	$T_j = 25°C$, (Note 6) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF $C_h = 0.01\ \mu F$		4 20	6 25		4 20	6 25	μs μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, T_{JMAX}, for the LF198/LF198A is 150°C; for the LF298, 115°C; and for the LF398/LF398A, 100°C.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: See AN-450 "Surface Mounting Methods and their effects on Product Reliability" for other methods of soldering surface mount devices.

Note 4: These parameters guaranteed over a supply voltage range of ±5 to ±18V, and an input range of $-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V$.

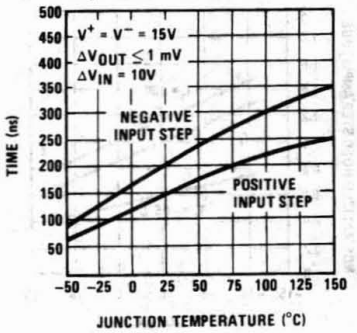
Note 5: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 6: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 7: A military RETS electrical test specification is available on request. The LF198 may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

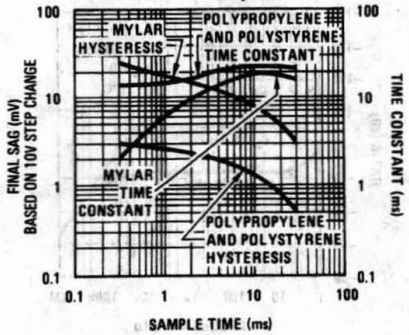
Typical Performance Characteristics

Aperture Time*

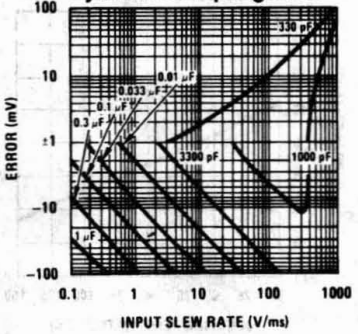


*See Definition of Terms

Dielectric Absorption Error in Hold Capacitor



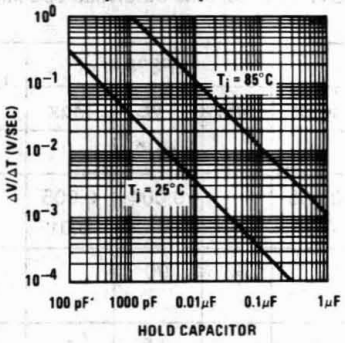
Dynamic Sampling Error



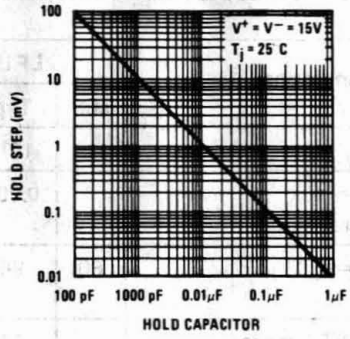
TL/H/5692–3

Typical Performance Characteristics (Continued)

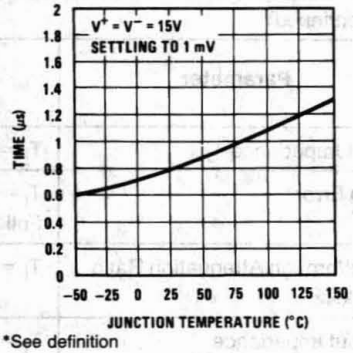
Output Droop Rate



Hold Step

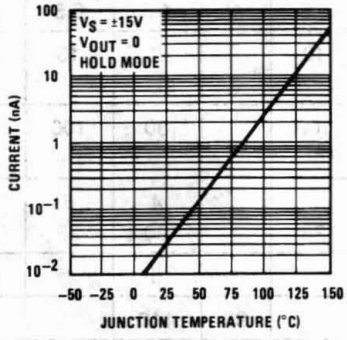


"Hold" Settling Time*

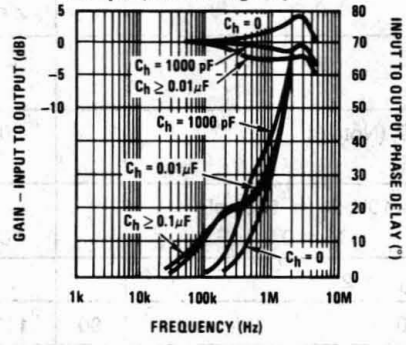


*See definition

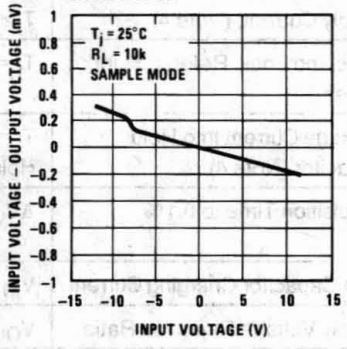
Leakage Current into Hold Capacitor



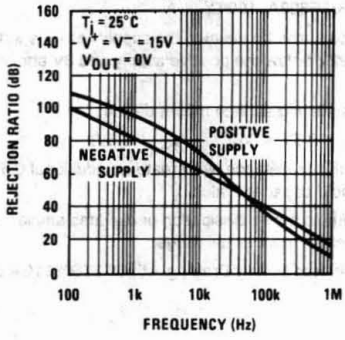
Phase and Gain (Input to Output, Small Signal)



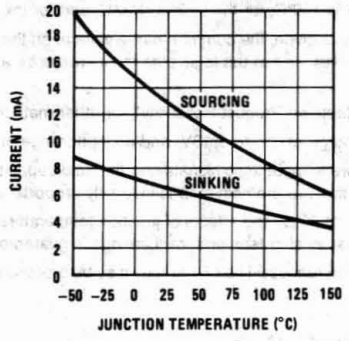
Gain Error



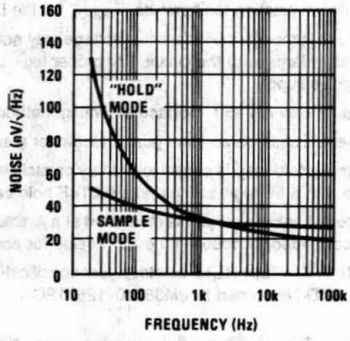
Power Supply Rejection



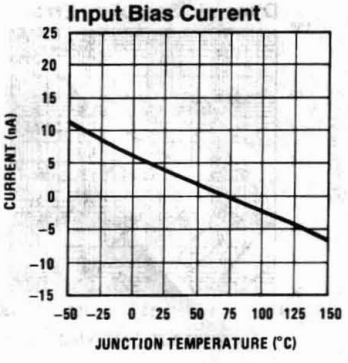
Output Short Circuit Current



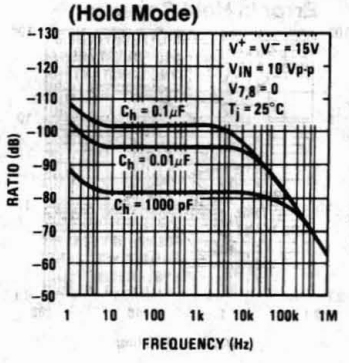
Output Noise



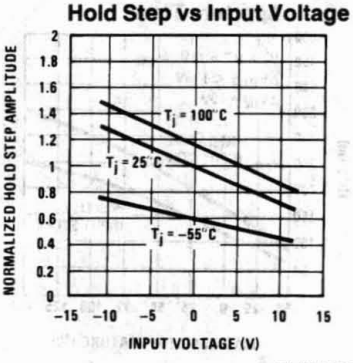
Input Bias Current



Feedthrough Rejection Ratio (Hold Mode)



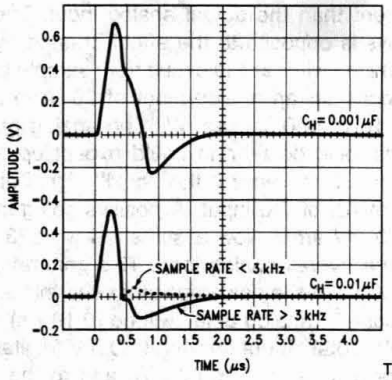
Hold Step vs Input Voltage



TL/H/5692–4

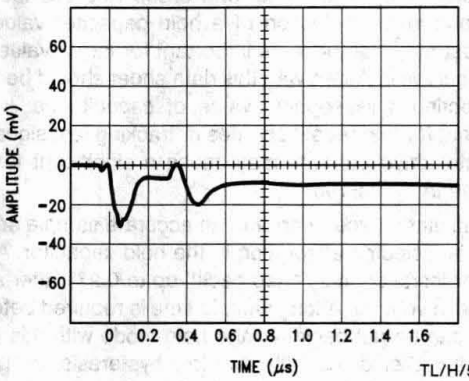
Typical Performance Characteristics (Continued)

Output Transient at Start of Sample Mode



TL/H/5692-12

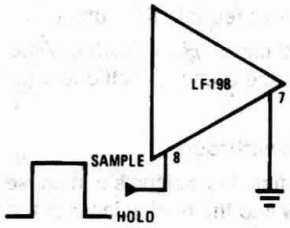
Output Transient at Start of Hold Mode



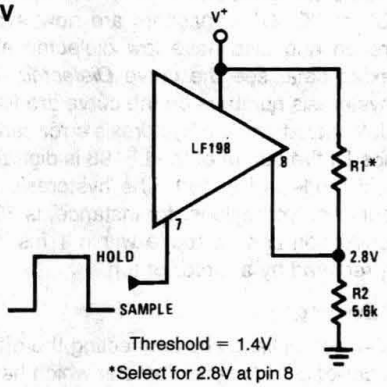
TL/H/5692-13

Logic Input Configurations

TTL & CMOS
3V ≤ V_{LOGIC} (Hi State) ≤ 7V

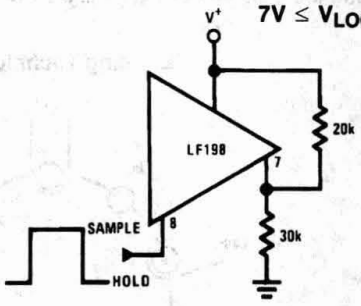


Threshold = 1.4V

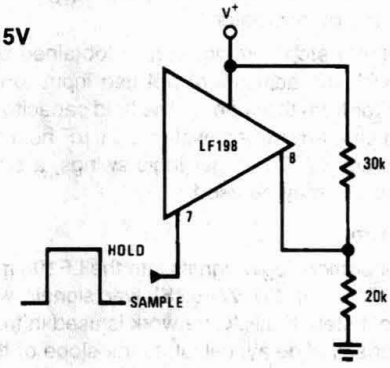


Threshold = 1.4V
*Select for 2.8V at pin 8

CMOS
7V ≤ V_{LOGIC} (Hi State) ≤ 15V

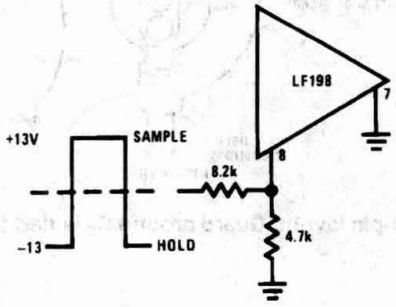


Threshold = 0.6 (V^+) + 1.4V

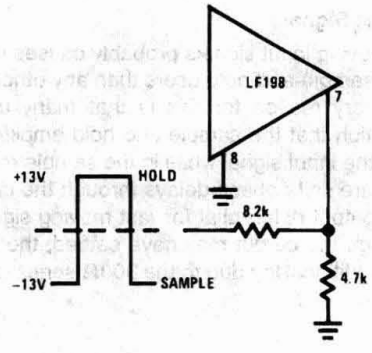


Threshold = 0.6 (V^+) − 1.4V

Op Amp Drive



Threshold ≈ +4V



Threshold = −4V

TL/H/5692-6

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Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error.* The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

Sampling Dynamic Signals

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 μs) (0.6V/μs) = 60 mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μs) (0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

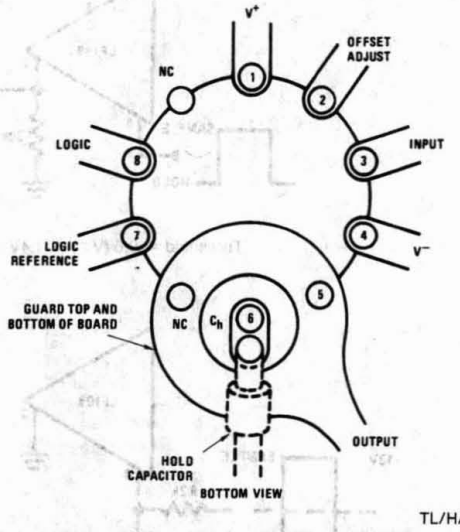
A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the C_h pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

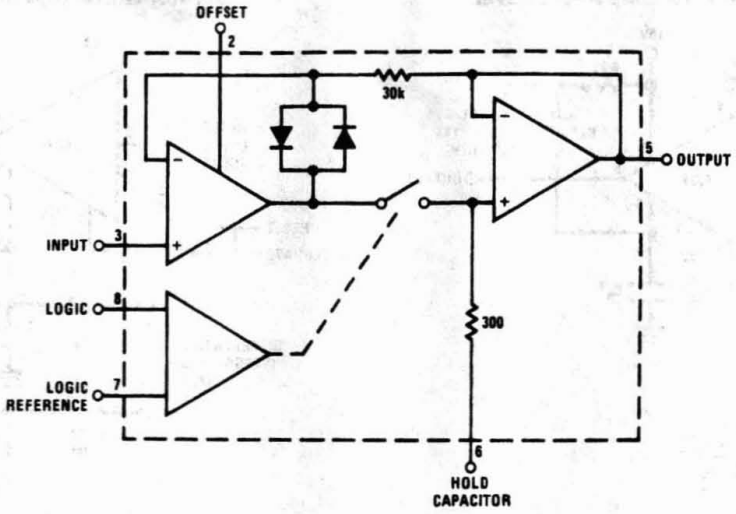
Guarding Technique



TL/H/5692–5

Use 10-pin layout. Guard around C_h is tied to output.

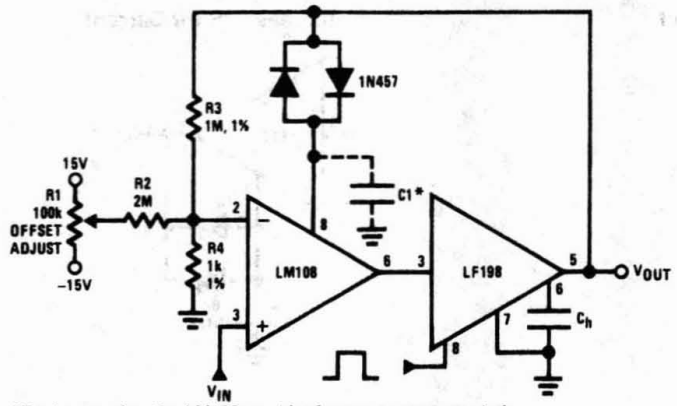
Functional Diagram



TL/H/5692–1

Typical Applications (Continued)

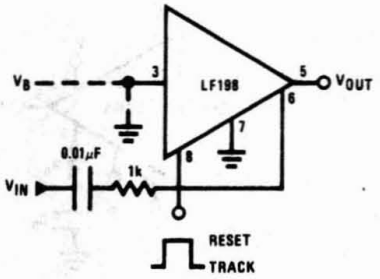
X1000 Sample & Hold



*For lower gains, the LM108 must be frequency compensated

Use $\approx \frac{100}{A_V}$ pF from comp 2 to ground

Sample and Difference Circuit
(Output Follows Input in *Hold* Mode)



$V_{OUT} = V_B + \Delta V_{IN}$(HOLD MODE)

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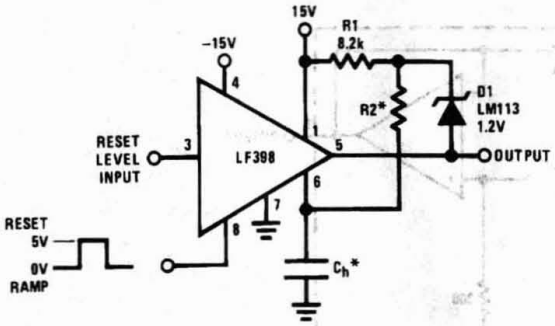
6

Typical Applications (Continued)

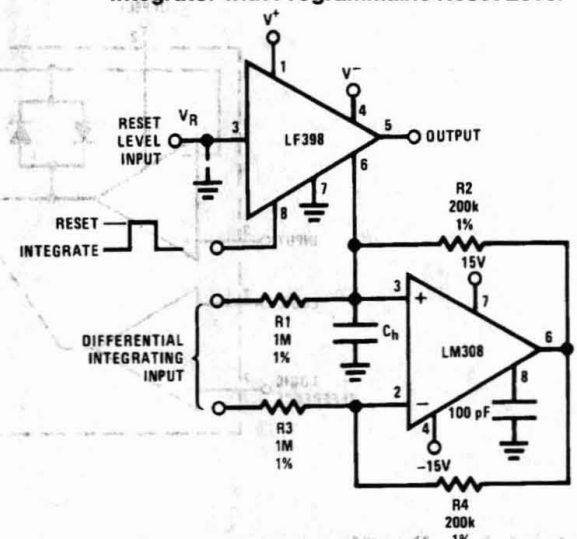
Ramp Generator with Variable Reset Level



*Select for ramp rate R2 ≥ 10k

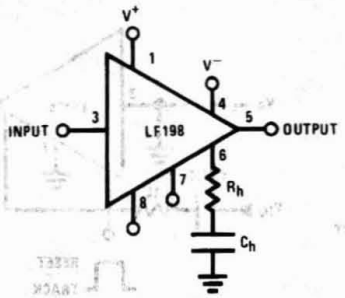
$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)\,(C_h)}$$

Integrator with Programmable Reset Level



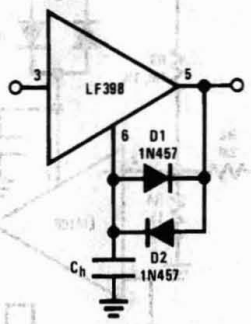
$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)\,(C_h)}\int_0^t V_{IN}\,dt\right] + \left[V_R\right]$$

Output Holds at Average of Sampled Input

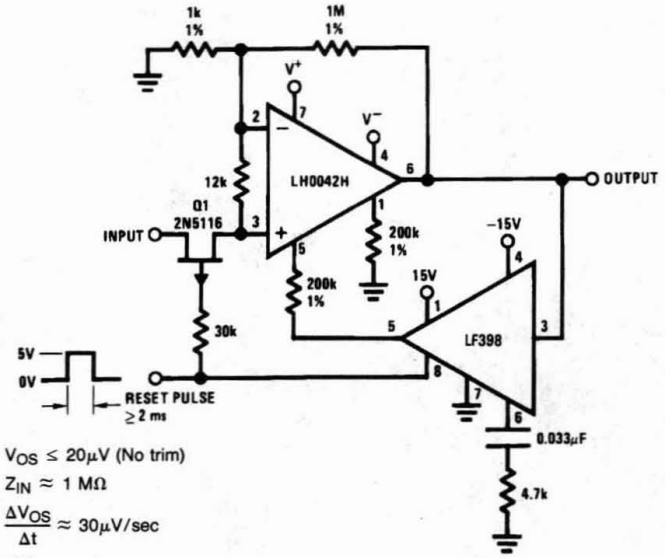


$$\text{Select } (R_h)\,(C_h) \geq \frac{1}{2\pi f_{IN}\,(\text{Min})}$$

Increased Slew Current



Reset Stabilized Amplifier (Gain of 1000)



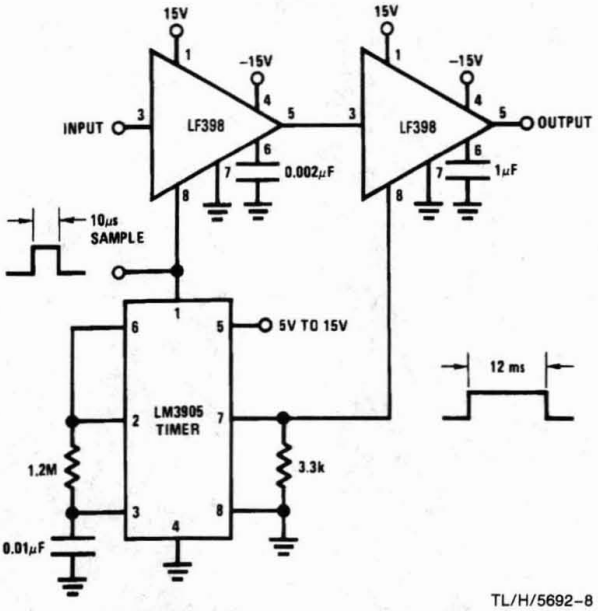
$V_{OS} \leq 20\mu V$ (No trim)

$Z_{IN} \approx 1\ M\Omega$

$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V/\text{sec}$

$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/°C$

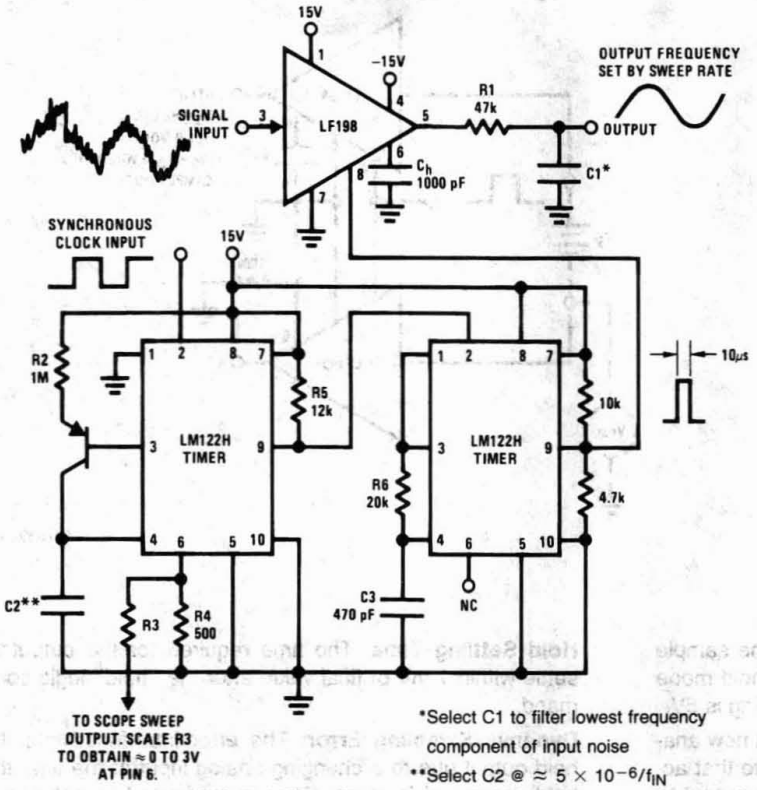
Fast Acquisition, Low Droop Sample & Hold



TL/H/5692–8

Typical Applications (Continued)

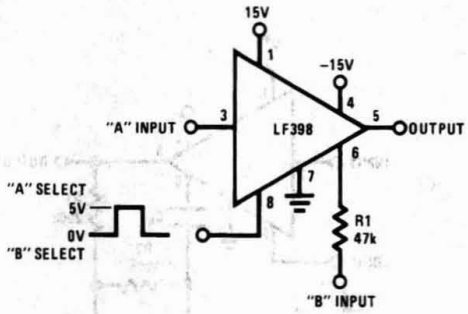
Synchronous Correlator for Recovering Signals Below Noise Level



*Select C1 to filter lowest frequency component of input noise

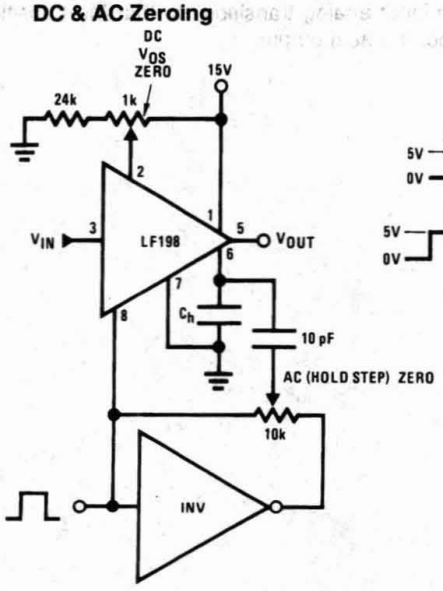
**Select C2 @ $\approx 5 \times 10^{-6}/f_{IN}$

2-Channel Switch

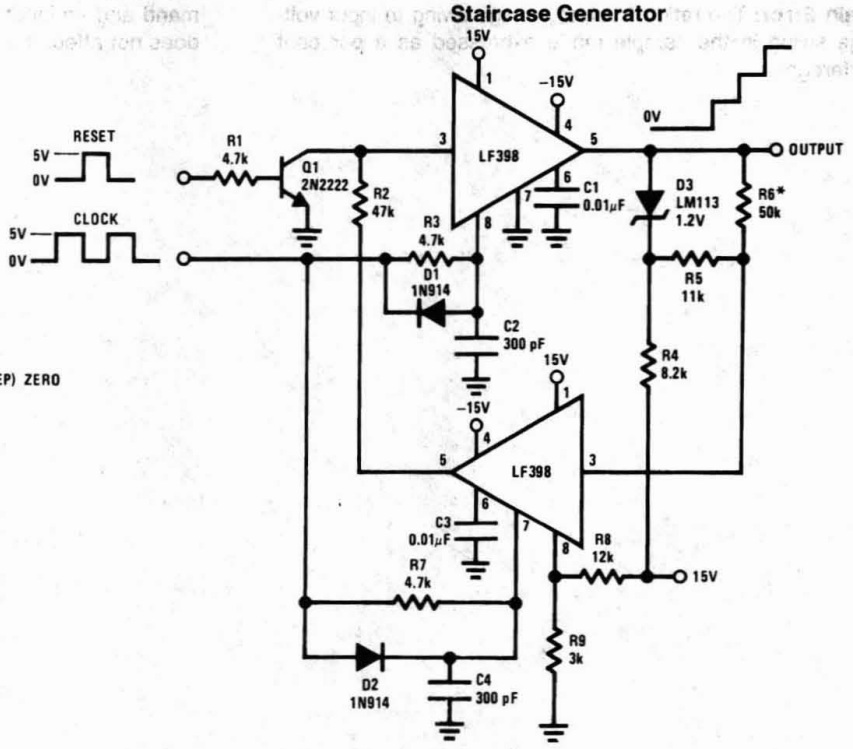


	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47 kΩ
BW	≅ 1 MHz	≅ 400 kHz
Crosstalk @ 1 kHz	−90 dB	−90 dB
Offset	≤ 6 mV	≤ 75 mV

DC & AC Zeroing



Staircase Generator

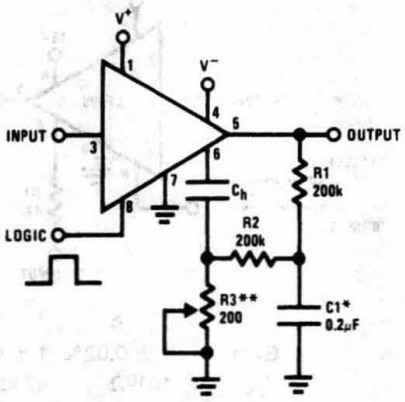


TL/H/5692–9

*Select for step height
50k → ≅ 1V Step

Typical Applications (Continued)

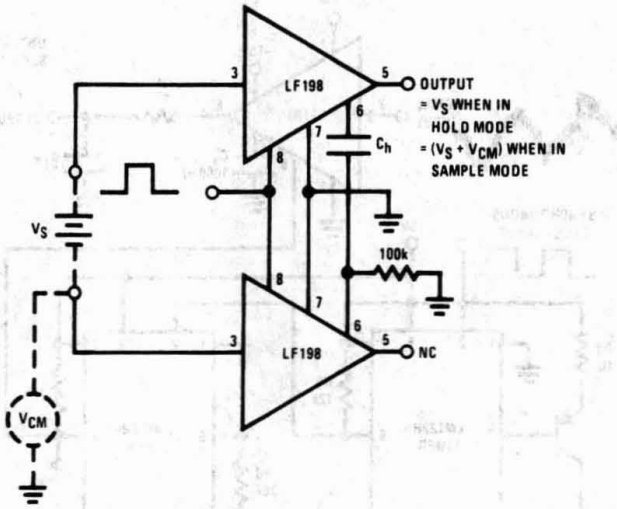
Capacitor Hysteresis Compensation



*Select for time constant C1 = $\frac{\tau}{100k}$

**Adjust for amplitude

Differential Hold



TL/H/5692–10

Definition of Terms

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

National Semiconductor

LF13006/LF13007 Digital Gain Set

General Description

The LF13006 and LF13007 are precision digital gain sets used for accurately setting non-inverting op amp gains. Gains are set with a 3-bit digital word which can be latched in with $\overline{WR}$ and $\overline{CS}$ pins. All digital inputs are TTL and CMOS compatible.

The LF13006 shown below will set binary scaled gains of 1, 2, 4, 8, 16, 32, 64, and 128. The LF13007 will set gains of 1, 2, 5, 10, 20, 50, and 100 (a common attenuator sequence). In addition, both versions have several taps and two uncommitted matching resistors that allow customization of the gain.

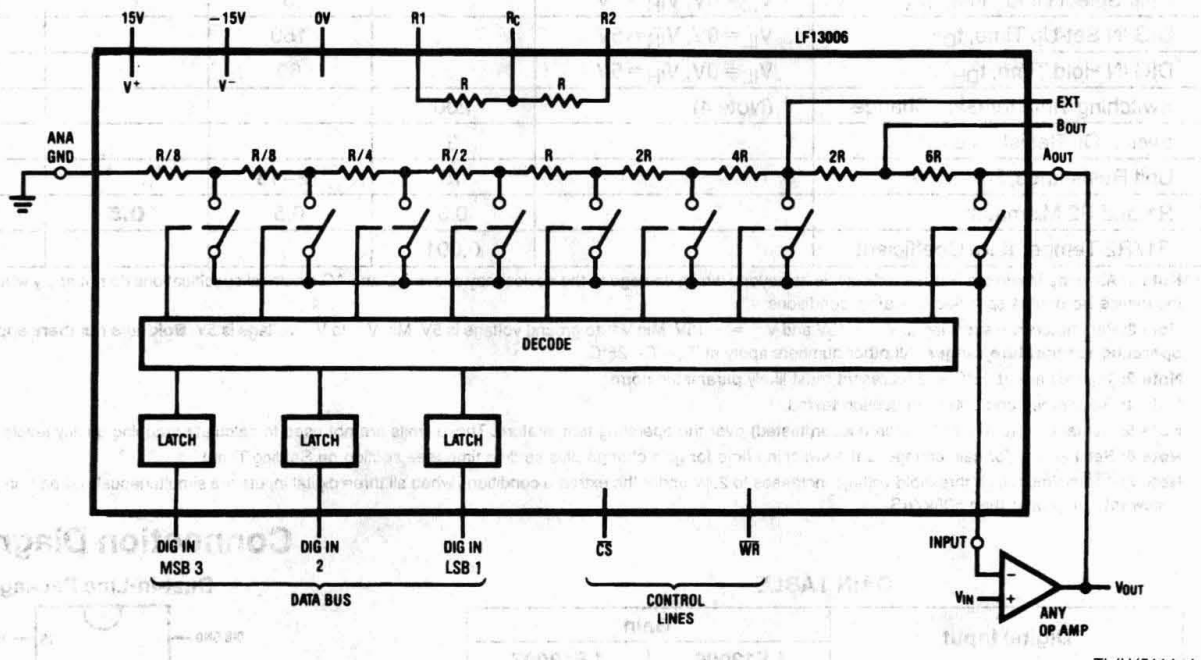
The gains are set with precision thin film resistors. The low temperature coefficient of the thin film resistors and their excellent tracking result in gain ratios which are virtually independent of temperature.

The LF13006, LF13007 used in conjunction with an amplifier not only satisfies the need for a digitally programmable amplifier in microprocessor based systems, but is also useful for discrete applications, eliminating the need to find 0.5% resistors in the ratio of 100 to 1 which track each other over temperature.

Features

- TTL and CMOS compatible logic levels
- Microprocessor compatible
- Gain error 0.5% max
- Binary or scope knob gains
- Wide supply range + 5V to ± 18V
- Packaged in 16-pin DIP

Block Diagram and Typical Application (LF13006)



TL/H/5114–1

Note: R ≅ 15 kΩ

Order Number LF13006N or LF13007N
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V^+ to V^-	36V
Supply Voltage, V^+ to GND	25V
Voltage at Any Digital Input	V^+ to GND
Analog Voltage	V^+ to (V^- + 2V)

Operating Ratings (Note 1)

Operating Temperature Range	−40°C to +85°C
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics (Note 2)

Parameter	Conditions	Typ (Note 3)	Tested Limit (Note 4)	Design Limit (Note 5)	Units
Gain Error	$A_{OUT} = \pm 10V$ ANA GND = 0V $I_{INPUT} < 10$ nA	0.3	0.5	**0.5**	%(max)
Gain Temperature Coefficient	$A_{OUT} = \pm 10V$ ANA GND = 0V	0.001			%/°C
Digital Input Voltage Low High		 1.4 1.6	 0.8 2.0	 **0.8** **2.0**	 V(max) V(min)
Digital Input Current Low High	 $V_{IL} = 0V$ $V_{IH} = 5V$	 −38 0.0001	 −100 1	 **−100** **1**	 μA(max) μA(max)
Positive Power Supply Current	All Logic Inputs Low	2	5	**5**	mA(max)
Negative Power Supply Current	All Logic Inputs Low	−1.7	−5	**−5**	mA(max)
$\overline{\text{Write}}$ Pulse Width, t_W	$V_{IL} = 0V$, $V_{IH} = 5V$		150		ns(min)
$\overline{\text{Chip Select}}$ Set-Up Time, t_{CS}	$V_{IL} = 0V$, $V_{IH} = 5V$		250		ns(min)
$\overline{\text{Chip Select}}$ Hold Time, t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$		0		ns(min)
DIG IN Set-Up Time, t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$		150		ns(min)
DIG IN Hold Time, t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$		60		ns(min)
Switching Time for Gain Change	(Note 4)	200			ns(max)
Switch On Resistance		3			kΩ
Unit Resistance, R		15	12–18		kΩ
R1 and R2 Mismatch		0.3	0.5	**0.5**	%(max)
R1/R2 Temperature Coefficient		0.001			%/°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Parameters are specified at $V^+ = 15V$ and $V^- = -15V$. Min V^+ to ground voltage is 5V. Min V^+ to V^- voltage is 5V. **Boldface numbers apply over full operating temperature ranges.** All other numbers apply at $T_A = T_j = 25°C$.

Note 3: Typicals are at 25°C and represent most likely parametric norm.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the operating temperature. These limits are not used to calculate outgoing quality levels.

Note 6: Settling time for gain change is the switching time for gain change plus settling time (see section on Settling Time).

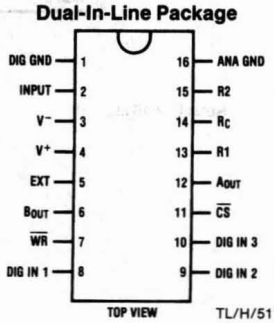
Note 7: $\overline{WR}$ minimum high threshold voltage increases to 2.4V under the extreme conditions when all three digital inputs are simultaneously taken from 0V to 5V at a slew rate of greater than 500V/μS.

GAIN TABLE

Digital Input			Gain			
			LF13006		LF13007	
DIG in 3	DIG in 2	DIG in 1	A_{OUT}	B_{OUT}	A_{OUT}	B_{OUT}
0	0	0	1	1	1	1
0	0	1	2	1.25	1.25	1
0	1	0	4	2.5	2	1.6
0	1	1	8	5	5	4
1	0	0	16	10	10	8
1	0	1	32	20	20	16
1	1	0	64	40	50	40
1	1	1	128	80	100	80

Connection Diagram

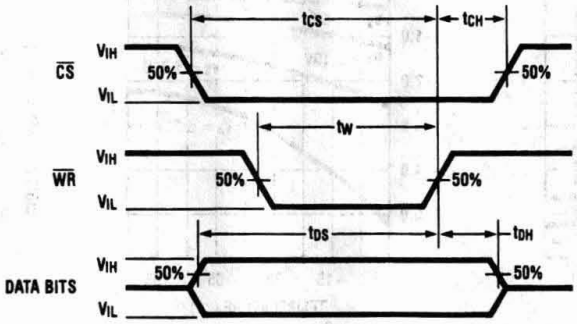
Dual-In-Line Package



TOP VIEW

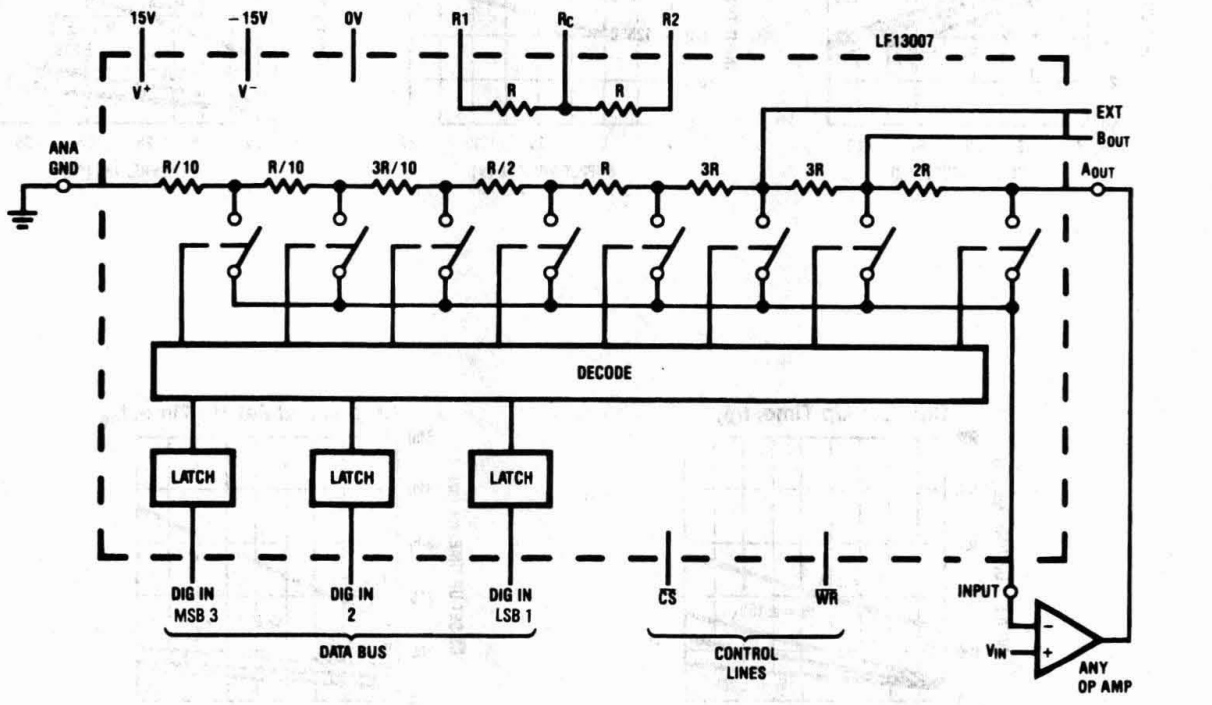
TL/H/5114–2

Switching Waveforms



TL/H/5114-3

Block Diagram and Typical Application (Continued) (LF13007)

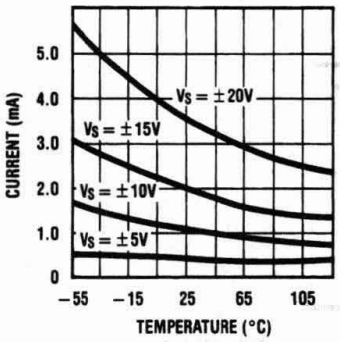


TL/H/5114-4

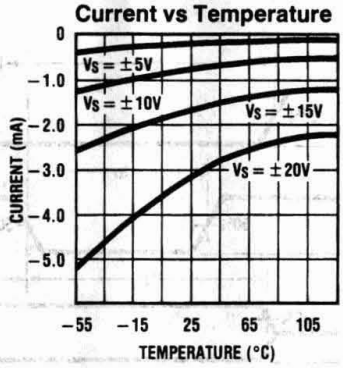
Note: R ≅ 15 kΩ

Typical Performance Characteristics

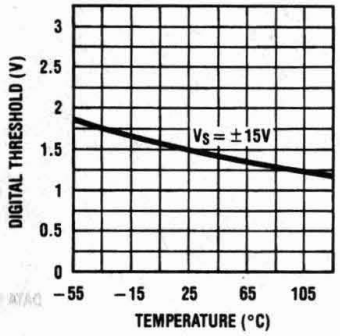
Positive Power Supply Current vs Temperature



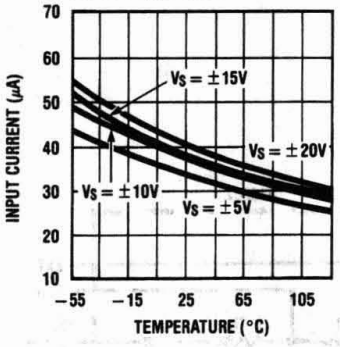
Negative Power Supply Current vs Temperature



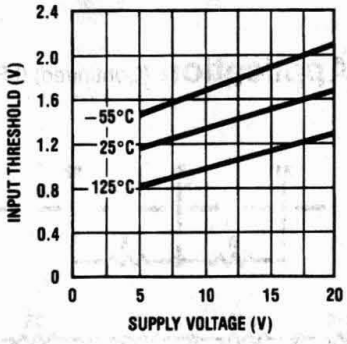
Digital Input Threshold vs Temperature



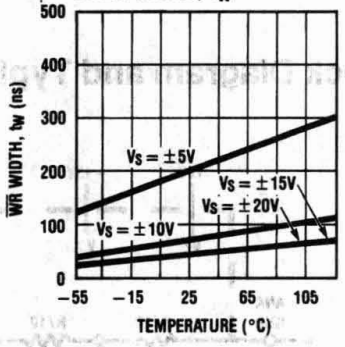
Logical 0 Input Bias Current vs Temperature



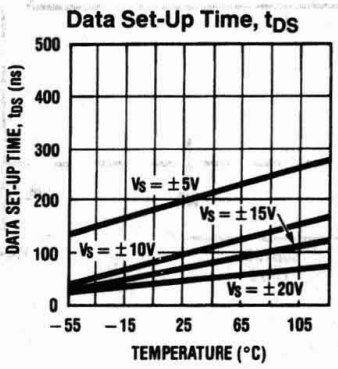
Digital Input Threshold vs Supply Voltage



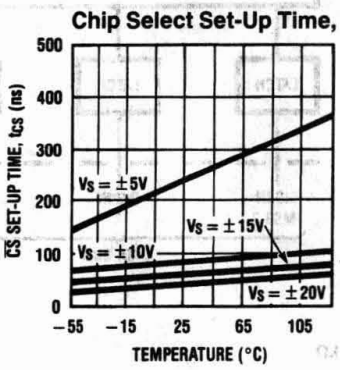
Write Width, t_w



Data Set-Up Time, t_{DS}



Chip Select Set-Up Time, t_{cs}



TL/H/5114–5

Application Information

FLOW-THROUGH OPERATION

THE LF13006, LF13007 can be operated with control lines $\overline{CS}$ and $\overline{WR}$ grounded. In this mode new data on the digital inputs will immediately set the new gain value. Input data cannot be latched in this mode.

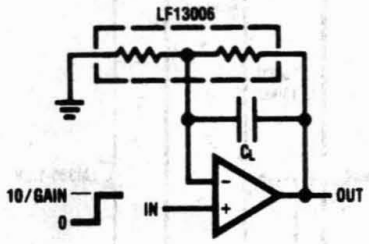
INPUT CURRENT

Current flowing through the input (pin 2) due to bias current of the op amp will result in a gain error due to switch impedance. Normally this error is very small. For example, 10 nA of bias current flowing through 3 kΩ of switch resistance will result in an error of 30 μV at the summing node. However, applications that have significant current flowing through the input must take this effect into account.

SETTLING TIME

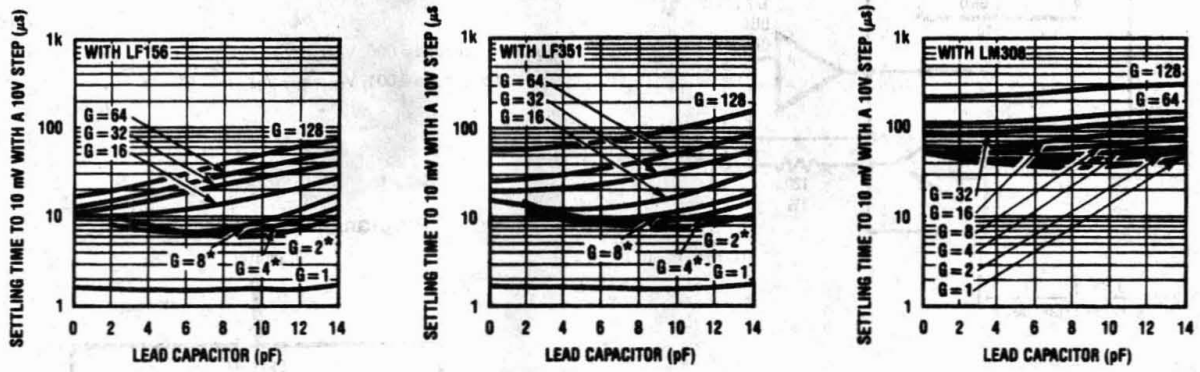
Settling time is a function of the particular op amp used with the LF13006/7 and the gain that is selected. It can be optimized and stability problems can be prevented through the use of a lead capacitor from the inverting input to the output of the amplifier. A lead capacitor is effective whenever the feedback around an amplifier is resistive, whether with discrete resistors or with the LF13006/7. It compensates for the feedback pole created by the parallel resistance and capacitance from the inverting input of the op amp to AC ground.

Settling Time Test Circuit



TL/H/5114–6

Typical Settling Time Curves



TL/H/5114–7

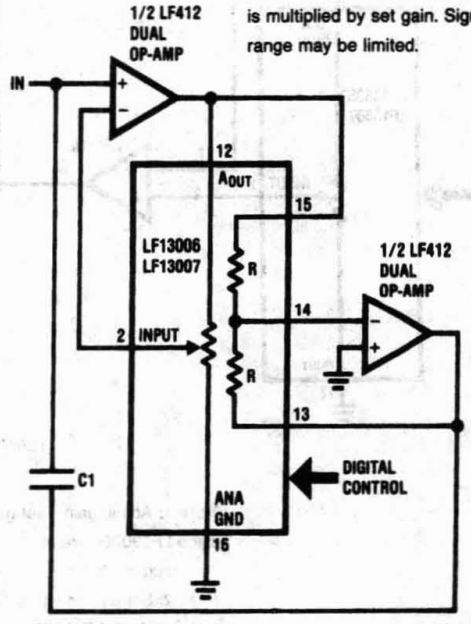
* Unstable at C_L less than 2 pF

Typical Applications

Variable Capacitance Multiplier

$C_{effective}$ = C1(gain set #)

Note: Output swing at input op amp is multiplied by set gain. Signal range may be limited.



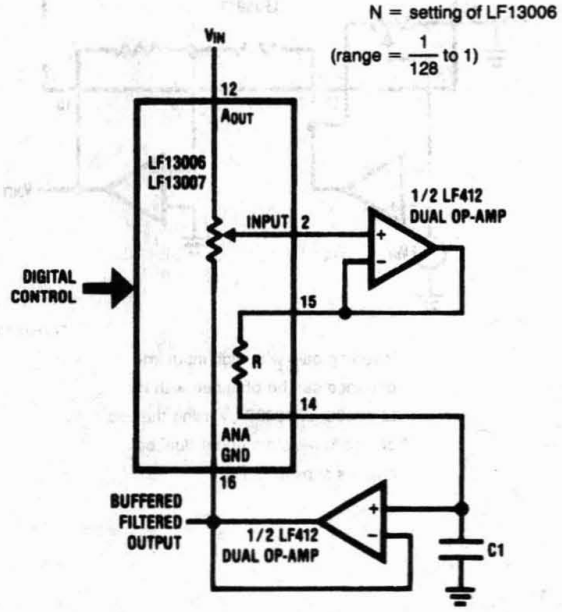
TL/H/5114–8

Variable Time Constant Filter

Time constant = $\frac{R}{N}$C1

N = setting of LF13006

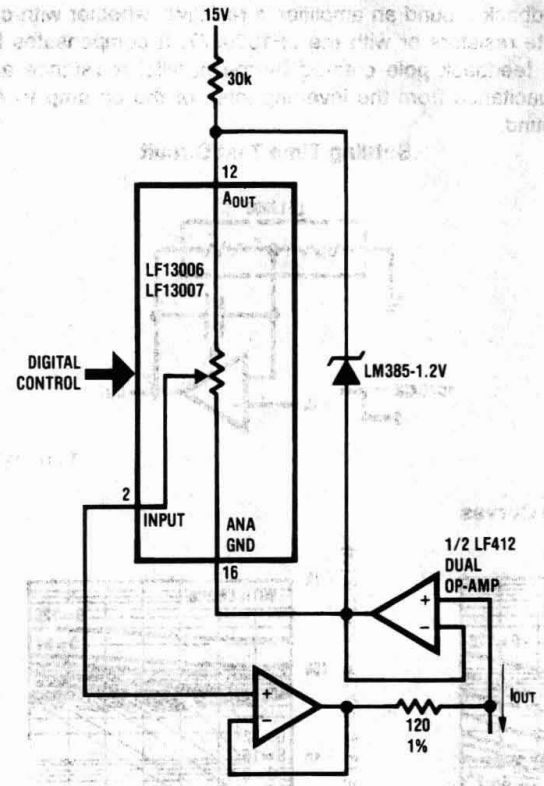
(range = $\frac{1}{128}$ to 1)



TL/H/5114–9

Typical Applications (Continued)

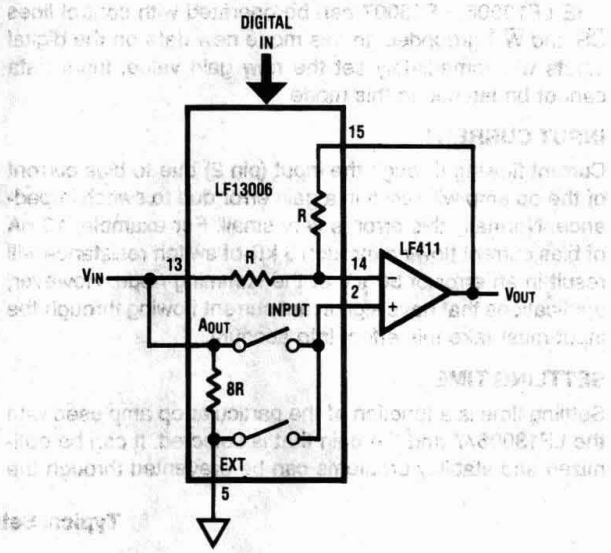
Programmable Current Source



TL/H/5114–10

$$I_{OUT} = \frac{1.2V}{120\Omega}\left[\frac{1}{\text{gain set \#}}\right]$$

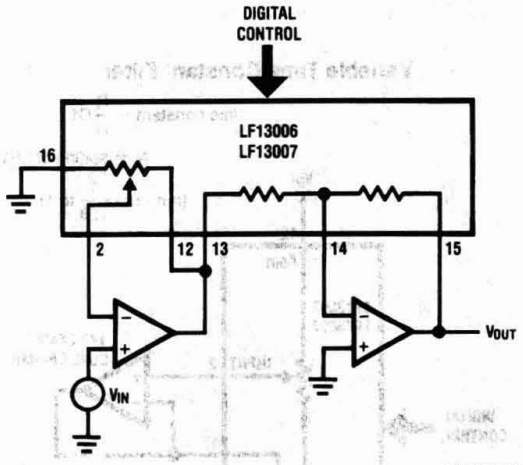
Switchable Gain of ±1



TL/H/5114–11

Note: Digital code = 000, $V_{OUT} = V_{IN}$;
Digital code = 001, $V_{OUT} = -V_{IN}$

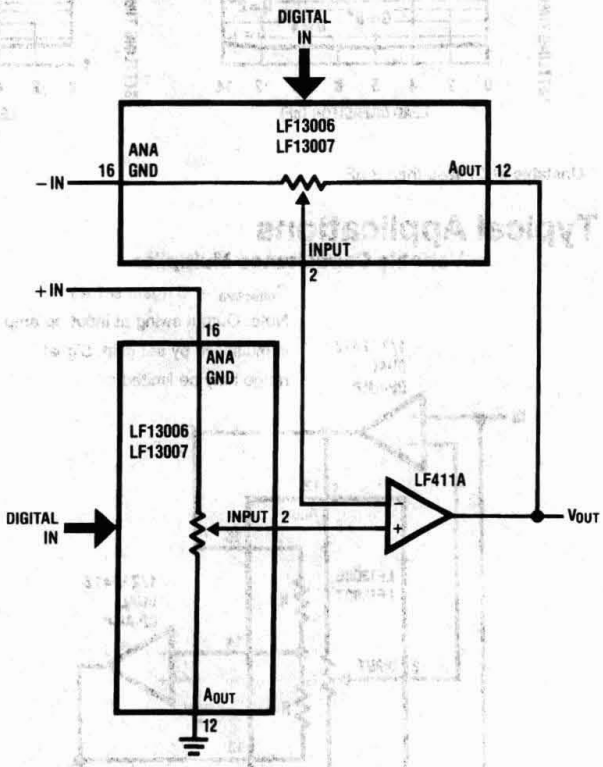
Inverting Gains



TL/H/5114–12

Inverting gain with high input impedance can be obtained with the LF13006, LF13007 by using the two on-board resistors and a dual op amp as shown.

Programmable Differential Amp



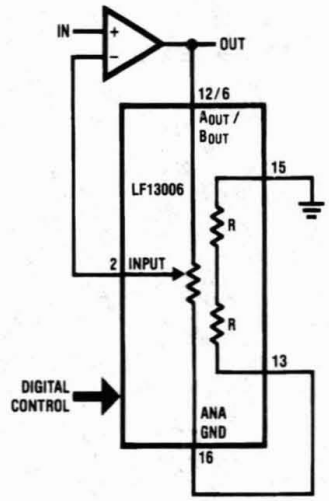
TL/H/5114–13

Note 1: Actual gain = set gain − 1 since LF13006s are in "inverting mode".

Note 2: Set gain must be same on both LF13006s.

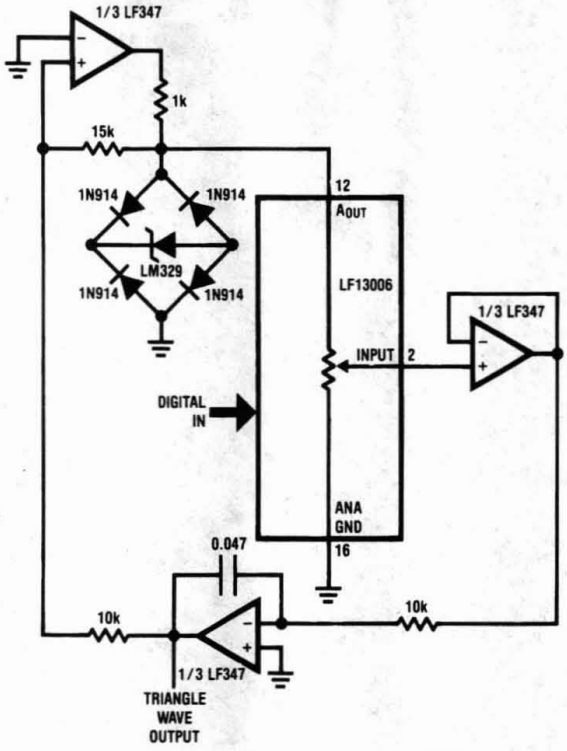
Typical Applications (Continued)

Altered Gain Range



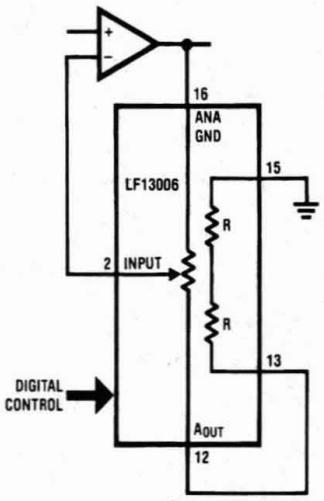
TL/H/5114-14

One Octave per Bit Function Generator



TL/H/5114-15

Variable Gains of Almost 1



TL/H/5114-16

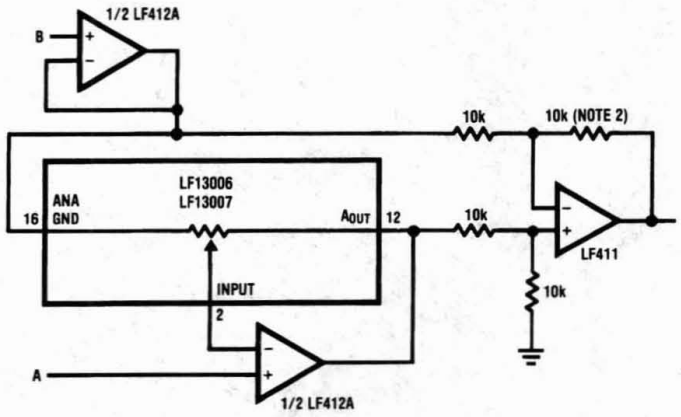
GAINS

A_{OUT}	B_{OUT}
1	1
1.8	1.2
3	2
4.5	3
6	4
7.2	4.8
8	5.33
8.47	5.65

GAINS

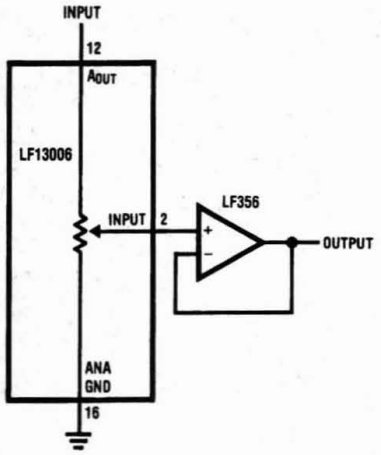
9
1.8
1.29
1.125
1.059
1.029
1.014
1.007

Programmable Instrumentation Amp



TL/H/5114-17

Attenuator (0 dB to −42 dB in 6 dB steps)



TL/H/5114-18

Note 1: $V_{OUT} = N\,(A - B)$, N = set gain.

Note 2: All 10k resistors 0.1% matched.

Section 7
Active Filters

Section 7 Contents

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Active Filters Selection Guide 7-4
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LMF60 High Performance 6th-Order Switched Capacitor Butterworth Low-Pass Filter 7-19
LMF90 4th-Order Elliptic Notch Filter 7-37
LMF100 High Performance Dual Switched Capacitor Filter 7-57
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MF4 4th Order Switched Capacitor Butterworth Lowpass Filter 7-89
MF5 Universal Monolithic Switched Capacitor Filter 7-102
MF6 6th Order Switched Capacitor Butterworth Lowpass Filter 7-117
MF8 4th Order Switched Capacitor Bandpass Filter 7-135
MF10 Universal Monolithic Dual Switched Capacitor Filter 7-157

Active Filters
Definition of Terms

f_{CLK}: the switched capacitor filter external clock frequency.

f_o: center of frequency of the second order function complex pole pair. f_o is measured at the bandpass output of each ½ MF10, and it is the frequency of the bandpass peak occurrence.

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each ½ MF10 and it is the ratio of f_o over the −3 dB bandwidth of the 2nd order bandpass filter. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain in (V/V) of the lowpass output of each ½ MF10 at $f \rightarrow 0$ Hz.

H_{OHP}: the gain in (V/V) of the highpass output of each ½ MF10 as $f \rightarrow f_{CLK}/2$.

Q_Z: the quality factor of the 2nd order function complex zero pair, if any. (Q_Z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

f_Z: the center frequency of the 2nd order function complex zero pair, if any. If f_Z is different from f_o, and if the Q_Z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF10.

H_{ON_1}: the notch output gain as $f \rightarrow 0$ Hz.

H_{ON_2}: the notch output gain as $f \rightarrow f_{CLK}/2$.

National Semiconductor

Active Filter Selection Guide

Device #	Type	Function	Max Order	Max Freq Accuracy	Freq Range	Typ. Q Accuracy	Max F* x Q
MF10 (S, T)	Universal	Universal	4th	±0.6%	0.1–30 kHz	±2%	200 kHz
MF8 (T)	Bandpass	Chebyshev Butterworth	4th	±1.0%	0.1–20 kHz	±2%	5 MHz*
MF6 (S, T)	Lowpass	Butterworth	6th	±1.0%	0.1–20 kHz	N/A	N/A
MF5 (S)	Universal	Universal	2nd	±1.0%	0.1–30 kHz	±6%	200 kHz
MF4 (S)	Lowpass	Butterworth	4th	±0.6%	0.1–20 kHz	N/A	N/A
LMF40 (S, T)	Lowpass	Butterworth	4th	±1.0%	0.1–40 kHz	N/A	N/A
LMF60 (S, T)	Lowpass	Butterworth	6th	±1.0%	0.1–30 kHz	N/A	N/A
LMF100 (S, T)	Universal	Universal	4th	±0.6%	0.1–40 kHz	±2%	1.8 MHz
LMF90 (S, T)	Notch	Elliptic	4th	±1%	0.1–30 kHz	N/A	N/A
LMF380	Triple One-Third Octave	Triple Bandpass	12th	±0.5% (typ)	0.1–25 kHz	N/A	N/A

S Surface Mount Available

T Extended Temperature Available

*For the MF8 use clock frequency for the parameter F. For all other parts use the center or cut off frequency.

National Semiconductor

LMF40 High Performance 4th-Order Switched-Capacitor Butterworth Low-Pass Filter

General Description

The LMF40 is a versatile, easy to use, precision 4th-order Butterworth low-pass filter fabricated using National's high performance LMCMOS process. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50-to-1 (LMF40-50) or 100-to-1 (LMF40-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, an external TTL or CMOS logic compatible clock can be applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading LMF40 sections together for higher-order filtering.

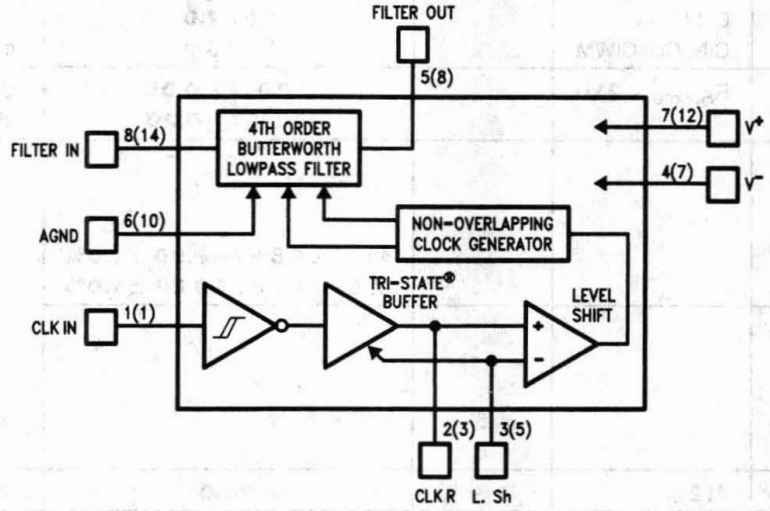
Features

- Cutoff frequency range of 0.1 Hz to 40 kHz
- Cutoff frequency accuracy of ±1.0%, maximum
- Low offset voltage, ±100 mV, maximum, ±5V supply
- Low clock feedthrough of 5 mV_{P-P}, typical
- Dynamic range of 88 dB, typical
- No external components required
- 8-pin mini-DIP or 14-pin wide-body small-outline packages
- 4V to 14V single/dual supply operation
- Cutoff frequency set by external or internal clock
- Pin-compatible with MF4

Applications

- Communication systems
- Instrumentation
- Automated control systems

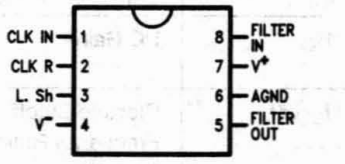
Block and Connection Diagrams



TL/H/10557–1

*Pin numbers in parentheses are for the 14-pin package

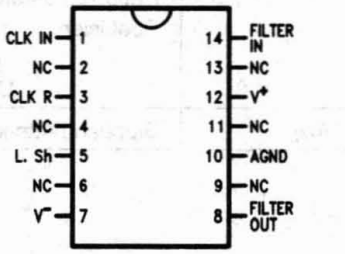
Dual-In-Line Package



TL/H/10557–2

Top View

Small-Outline-Wide-Body Package



TL/H/10557–3

Top View

Ordering Information

Industrial ($-40°C \le T_A \le +85°C$)	Package
LMF40CIN-50, LMF40CIN-100	N08E
LMF40CIWM-50	M14B
LMF40CIWM-100	M14B
Military ($-55°C \le T_A \le +125°C$)	
LMF40CMJ-50, LMF40CMJ-100	J08A

7

Absolute Maximum Ratings

(Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	15V
Voltage at Any Pin	$V^- - 0.2V$ to $V^+ + 0.2V$
Input Current at Any Pin (Note 13)	5 mA
Package Input Current (Note 13)	20 mA
Power Dissipation (Note 14)	500 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package, Soldering (10 sec.)	+260°C
J Package, Soldering (10 sec.)	+300°C
WM Package, Vapor Phase (60 sec.) (Note 16)	+215°C
WM Package, Infrared (15 sec.)	+220°C
ESD Susceptibility (Note 12)	2000V
Pin 1 CLK IN	1700V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF40CIN-50, LMF40CIN-100 LMF40CIWM-50, LMF40CIWM-100	$-40°C \le T_A \le +85°C$
LMF40CMJ-50, LMF40CMJ-100	$-55°C \le T_A \le +125°C$
Supply Voltage Range ($V^+ - V^-$)	4V to 14V

Filter Electrical Characteristics

The following specifications apply for f_{CLK} = 500 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
$V^+ = +5V, V^- = -5V$					
f_{CLK}	Clock Frequency Range (Note 17)		5	**2**	Hz (min) MHz (max)
I_S	Supply Current	CMJ CIN, CIJ, CIWM		3.5 / **7.0** 3.5 / **5.0**	mA (max) mA (max)
H_O	DC Gain	$R_{Source} \le 2\ k\Omega$		+0.05 / +**0.05** −0.15 / −**0.20**	dB (max) dB (min)
f_{CLK}/f_c	Clock to Cutoff Frequency Ratio (Note 3) LMF40-50 LMF40-100			 49.80 ± 0.8% / **49.80 ± 1.0%** 99.00 ± 0.8% / **99.00 ± 1.0%**	 (max) (max)
$\Delta f_{CLK}/f_c/\Delta T$	Clock to Cutoff Frequency Ratio Temperature Coefficient LMF40-50 LMF40-100		 5 5		 ppm/°C ppm/°C
A_{MIN}	Stopband Attenuation	At 2 f_c		**24.0**	dB (min)

Filter Electrical Characteristics (Continued)

The following specifications apply for f_{CLK} = 500 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
V^+ = +5V, V^- = −5V (Continued)					
V_{OS}	Unadjusted DC Offset Voltage				
	LMF40-50			±80 / ±**100**	mV (max)
	LMF40-100			±80 / ±**100**	mV (max)
V_O	Output Swing	R_L = 5 kΩ		+3.9 / +**3.7**	V (min)
				−4.2 / −**4.0**	V (max)
I_{SC}	Output Short Circuit Current (Note 8)	Source	90		mA
		Sink	2.2		mA
	Dynamic Range (Note 4)		88		dB
	Additional Magnitude Response Test Points (Note 6)				
	LMF40-50	f_{IN} = 12 kHz		−7.50 ±0.26 / −**7.50 ±0.30**	dB (max)
		f_{IN} = 9 kHz		−1.46 ±0.12 / −**1.46 ±0.16**	dB (max)
	LMF40-100	f_{IN} = 6 kHz		−7.15 ±0.26 / −**7.15 ±0.30**	dB (max)
		f_{IN} = 4.5 kHz		−1.42 ±0.12 / −**1.42 ±0.16**	dB (max)
	Clock Feedthrough	Filter Output V_{IN} = 0V	5		mV_{P-P}

Filter Electrical Characteristics

The following specifications apply for f_{CLK} = 250 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
V^+ = +2.5V, V^- = −2.5V					
f_{CLK}	Clock Frequency Range (Note 17)		5		Hz (min)
				1.0	MHz (max)
I_S	Supply Current	CMJ		2.1 / **4.0**	mA (max)
		CIN, CIJ, CIWM		2.1 / **3.0**	mA (max)
H_O	DC Gain	$R_S \leq 2$ kΩ f_{CLK} = 250 kHz		+0.05 / +**0.05**	dB (max)
				−0.15 / −**0.20**	dB (min)
		f_{CLK} = 500 kHz	−0.1		dB
f_{CLK}/f_c	Clock to Cutoff Frequency Ratio				
	LMF40-50	f_{CLK} = 250 kHz		**49.80 ±0.8%**	(max)
		f_{CLK} = 500 kHz	49.80 ±0.6%		
	LMF40-100 (Note 3)	f_{CLK} = 250 kHz		99.00 ±1.0% / **99.00 ±1.2%**	(max)
		f_{CLK} = 500 kHz	99.00 ±1.2%		

Filter Electrical Characteristics (Continued)

The following specifications apply for f_{CLK} = 250 kHz. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** All other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
V^+ = +2.5V, V^- = −2.5V (Continued)					
$\Delta f_{CLK}/f_c/\Delta T$	Clock to Cutoff Frequency Ratio Temperature Coefficient				
	LMF40-50		5		ppm/°C
	LMF40-100		5		ppm/°C
A_{MIN}	Stopband Attenuation	At 2 f_c		**−24.0**	dB (min)
V_{OS}	Unadjusted DC Offset Voltage				
	LMF40-50			±80 / ±**100**	mV (max)
	LMF40-100			±80 / ±**100**	mV (max)
V_O	Output Swing	R_L = 5 kΩ		+1.4 / +**1.2**	V (min)
				−2.0 / −**1.8**	V (max)
I_{SC}	Output Short Circuit Current (Note 8)	Source	42		mA
		Sink	0.9		mA
	Dynamic Range (Note 4)		81		dB
	Additional Magnitude Response Test Points (Note 6)				
	LMF40-50	f_{IN} = 6 kHz		−7.50 ±0.26 / −**7.50 ±0.30**	dB (max)
		f_{IN} = 4.5 kHz		−1.46 ±0.12 / −**1.46 ±0.16**	dB (max)
	LMF40-100	f_{IN} = 3 kHz		−7.15 ±0.26 / −**7.15 ±0.30**	dB (max)
		f_{IN} = 2.25 kHz		−1.42 ±0.12 / −**1.42 ±0.16**	dB (max)
	Clock Feedthrough	Filter Output V_{IN} = 0V	5		mV_{P-P}

Logic Input-Output Characteristics

The following specifications apply for V^- = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
TTL CLOCK INPUT, CLK R PIN (Note 9)					
	TTL CLK R Pin Input Voltage	V^+ = +5V, V^- = −5V			
	Logic "1"			2.0 / **2.1**	V (min)
	Logic "0"			0.8 / **0.8**	V (max)
	CLK R Input Voltage	V^+ = +2.5V, V^- = −2.5V			
	Logic "1"			2.0 / **2.0**	V (min)
	Logic "0"			0.6 / **0.4**	V (max)
	Maximum Leakage Current at CLK R Pin		2.0		μA
SCHMITT TRIGGER					
V_T+	Positive Going Input Threshold Voltage CLK IN Pin	V^+ = +10V		6.1 / **6.0**	V (min)
				8.8 / **8.9**	V (max)
		V^+ = +5V		3.0 / **2.9**	V (min)
				4.3 / **4.4**	V (max)

Logic Input-Output Characteristics (Continued) The following specifications apply for V^- = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limit)
SCHMITT TRIGGER (Continued)					
V_T-	Negative Going Input Threshold Voltage CLK IN Pin	$V^+ = +10V$		1.4 / **1.3** 3.8 / **3.9**	V (min) V (max)
		$V^+ = +5V$		0.7 / **0.6** 1.9 / **2.0**	V (min) V (max)
$V_T+ - V_T-$	Hysteresis CLK IN Pin	$V^+ = +10V$		2.3 / **2.1** 7.4 / **7.6**	V (min) V (max)
		$V^+ = +5V$		1.1 / **0.9** 3.6 / **3.8**	V (min) V (max)
	Logical "1" Output Voltage CLK R Pin	$I_O = -10\ \mu A$ $V^+ = +10V$ $V^+ = +5V$		 9.1 / **9.0** 4.6 / **4.5**	 V (min) V (min)
	Logical "0" Output Voltage CLK R Pin	$I_O = -10\ \mu A$ $V^+ = +10V$ $V^+ = +5V$		 0.9 / **1.0** 0.4 / **0.5**	 V (max) V (max)
	Output Source Current CLK R Pin	CLK R to V^- $V^+ = +10V$ $V^+ = +5V$		 4.9 / **3.7** 1.6 / **1.2**	 mA (min) mA (min)
	Output Sink Current CLK R Pin	CLK R to V^+ $V^+ = +10V$ $V^+ = +5V$		 4.9 / **3.7** 1.6 / **1.2**	 mA (min) mA (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating range.

Note 2: All voltages are specified with respect to ground.

Note 3: The filter's cutoff frequency is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 4: For ±5V supplies the dynamic range is referenced to 2.62 V_{rms} (3.7V peak) where the wideband noise over a 20 kHz bandwidth is typically 100 μV_{rms} for the LMF40. For ±2.5V supplies the dynamic range is referenced to 0.849 V_{rms} (1.2V peak) where the wideband noise over a 20 kHz bandwidth is typically 75 μV_{rms} for the LMF40.

Note 5: The specifications for the LMF40 have been given for a clock frequency (f_{CLK}) of 500 kHz at ±5V and 250 kHz at ±2.5V. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.8% over the temperature range, but the filter still maintains its magnitude characteristics. See Application Information, Section 1.4.

Note 6: The filter's magnitude response is tested at the cutoff frequency, f_c, $f_S = 2\ f_c$, and at these other two additional frequencies.

Note 7: For simplicity all logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 8: The short circuit source current is measured by forcing the output that is being tested to its maximum positive swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 9: The LMF40 is operated with symmetrical supplies and L. Sh. is tied to ground.

Note 10: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

Note 11: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 13: When the input voltage (V_{IN}) at any pin exceeds the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply voltages with 5 mA current limit to four.

Note 14: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $PD = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LMF40, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance, when board mounted, is 67°C/W for the LMF40CIN, 62°C/W for the LMF40CIJ and LMF40CMJ, and 78°C/W for the LMC40CIWM.

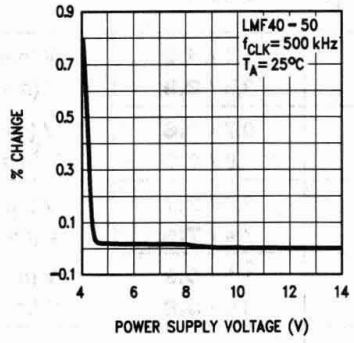
Note 15: In popular usage the term cutoff frequency defines that frequency at which a filter's gain drops 3.01 dB below its DC value. Equations (2) and (3) and design example 2.1, however, use the term cutoff frequency (f_b) to define that frequency at which a filter's gain drops by a variable amount as determined from the given design specifications.

Note 16: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices or see the section titled "Surface Mount" in the *Linear Data Book*.

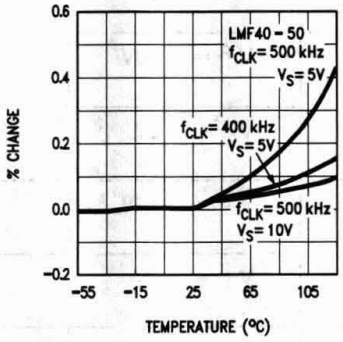
Note 17: The nominal ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50-to-1 (LMF40-50) or 100-to-1 (LMF40-100).

Typical Performance Characteristics

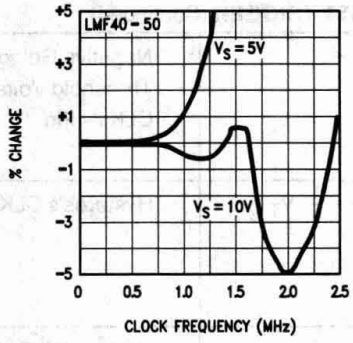
f_{CLK}/f_c Deviation vs Power Supply Voltage



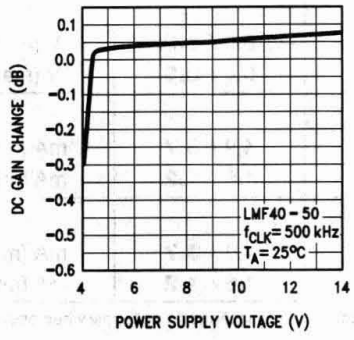
f_{CLK}/f_c Deviation vs Temperature



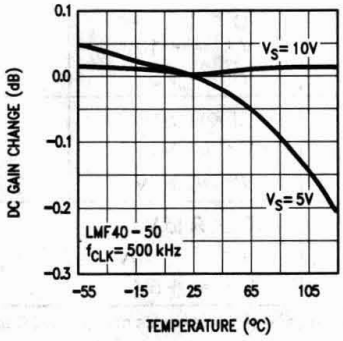
f_{CLK}/f_c Deviation vs Clock Frequency



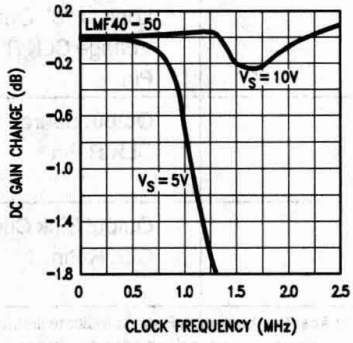
DC Gain Deviation vs Power Supply Voltage



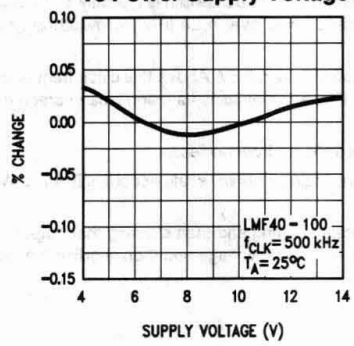
DC Gain Deviation vs Temperature



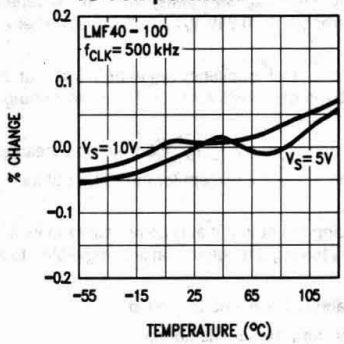
DC Gain Deviation vs Clock Frequency



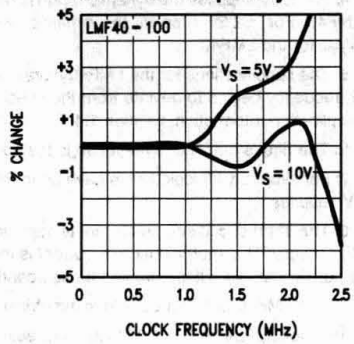
f_{CLK}/f_c Deviation vs Power Supply Voltage



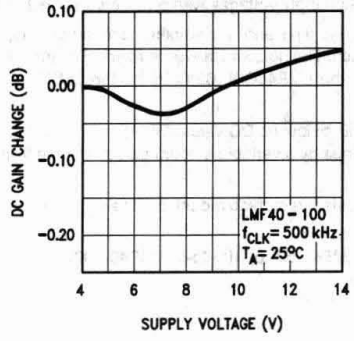
f_{CLK}/f_c Deviation vs Temperature



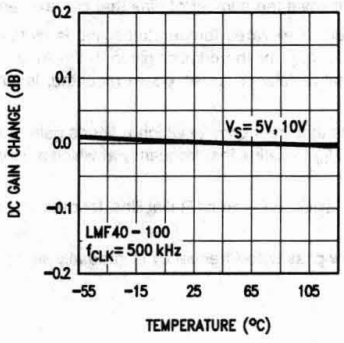
f_{CLK}/f_c Deviation vs Clock Frequency



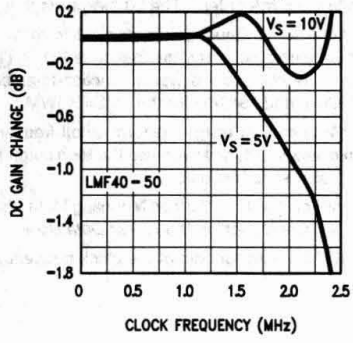
DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



DC Gain Deviation vs Clock Frequency



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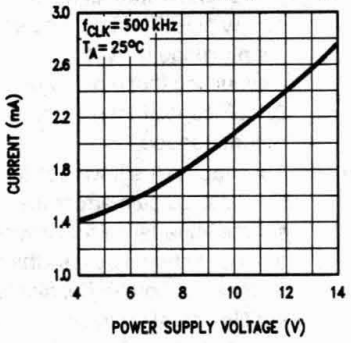
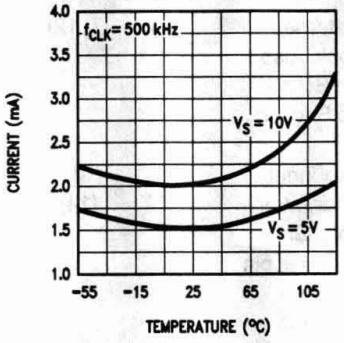
Typical Performance Characteristics (Continued)

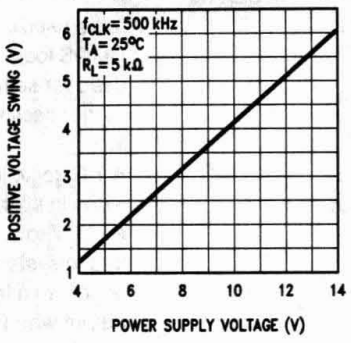
Power Supply Current vs Power Supply Voltage



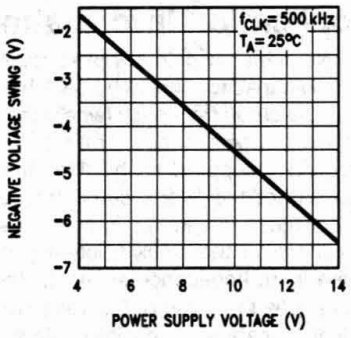
Power Supply Current vs Temperature



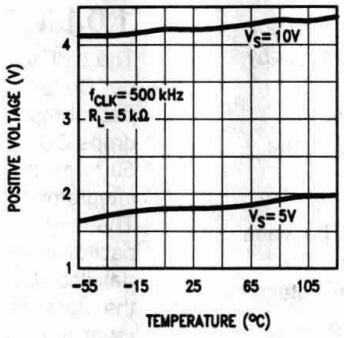
Positive Voltage Swing vs Power Supply Voltage



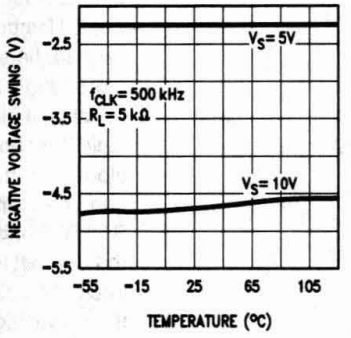
Negative Voltage Swing vs Power Supply Voltage



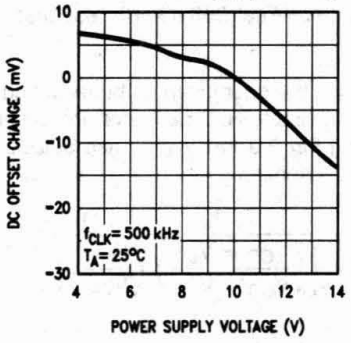
Positive Voltage Swing vs Temperature



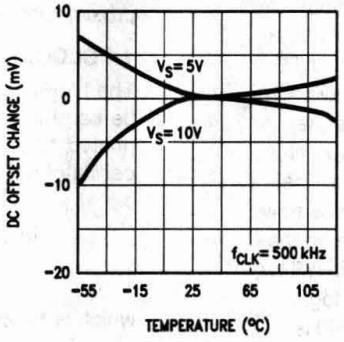
Negative Voltage Swing vs Temperature



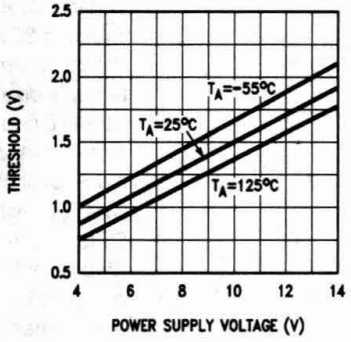
DC Offset Voltage Deviation vs Power Supply Voltage



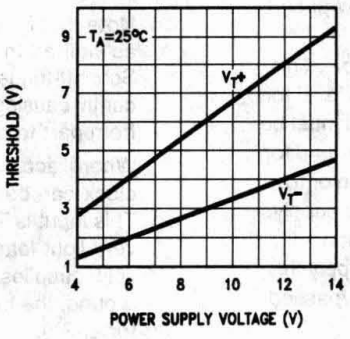
DC Offset Voltage Deviation vs Temperature



CLK R Trigger Threshold vs Power Supply Voltage



Schmitt Trigger Threshold vs Power Supply Voltage



TL/H/10557–6

Pin Descriptions

(Numbers in ( ) are for 14-pin package).

Pin #	Pin Name	Function
1 (1)	CLK IN	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self clocking Schmitt-trigger oscillator (see Section 1.1).
2 (3)	CLK R	A TTL logic level clock input when in split supply operation (±2.0V to ±7V) with L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see Section 1.1). The TTL input signal must not exceed the supply voltages by more than 0.2V.
3 (5)	L. Sh	Level shift pin; selects the logic threshold levels for the clock. When tied to V^- it enables an internal TRI-STATE® buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds 25% $(V^+ - V^-) + V^-$ the internal TRI-STATE buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level-shift stage. The CLK R threshold level is now 2V above the voltage on the L. Sh pin. The CLK R pin will be compatible with TTL logic levels when the LMF40 is operated on split supplies with the L. Sh pin connected to system ground.
5 (8)	FILTER OUT	The output of the low-pass filter.
6 (10)	AGND	The analog ground pin. This pin sets the DC bias level for the filter section and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see Section 1.2). When tied to mid-supply this pin should be well bypassed.
7, 4 (7, 12)	V^+, V^-	The positive and negative supply pins. The total power supply range is 4V, to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
8 (14)	FILTER IN	The input to the low-pass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (see Section 3). For single supply operation the input signal must be biased to mid-supply or AC coupled through a capacitor.

1.0 LMF40 Application Information

The LMF40 is a non-inverting unity gain low-pass fourth-order Butterworth switched-capacitor filter. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock-to-cutoff-frequency ratio (f_{CLK}/f_C) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock-to-cutoff-frequency ratio the closer this approximation is to the theoretical Butterworth response.

1.1 CLOCK INPUTS

The LMF40 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. Pin 3 is connected to V^-, making Pin 2 a low impedance output. The oscillator's frequency is nominally

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_t-}{V_{CC} - V_t+}\right)\left(\frac{V_t+}{V_t-}\right)\right]} \quad (1)$$

which is typically

$$f_{CLK} \cong \frac{1}{1.37\ RC} \quad (1a)$$

for $V_{CC} = 10V$.

Note that f_{CLK} is dependent on the buffer's threshold levels as well as the resistor/capacitor tolerance (see *Figure 1*). Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accurate cutoff frequency is required, an external clock can be used to drive the CLK R input of the LMF40. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 μA). With split supplies and the level shift (L. Sh) tied to system ground, the logic level is about 2V. (See the Pin Description for L. Sh).

1.0 LMF40 Application Information (Continued)

1.2 POWER SUPPLY

The LMF40 can be powered from a single supply or split supplies. The split supply mode shown in *Figure 2* is the most flexible and easiest to implement. Supply voltages of ±5V to ±7V enable the use of TTL or CMOS clock logic levels. *Figure 3* shows AGND resistor-biased to $V^+/2$ for single supply operation. In this mode only CMOS clock logic levels can be used, and input signals should be capacitor-coupled or biased near mid-supply.

1.3 INPUT IMPEDANCE

The LMF40 low-pass filter input (FILTER IN) is not a high impedance buffer input. This input is a switched-capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the filter's input can be seen in *Figure 4*. The input capacitor charges to V_{IN} during the first half of the clock period; during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{IN} V_{IN}$, and since current is defined as the flow of charge per unit time, the average input current becomes

$$I_{IN} = Q/T$$

(where T equals one clock period) or

$$I_{IN\,AVE} = \frac{C_{IN} V_{IN}}{T} = C_{IN} V_{IN} f_{CLK}$$

The equivalent input resistor (R_{IN}) then can be expressed as

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{C_{IN} f_{CLK}}$$

The input capacitor is 2 pF for the LMF40-50 and 1 pF for the LMF40-100, so for the LMF40-100

$$R_{IN} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{IN} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the LMF40-50. The above equation shows that for a given cutoff frequency (f_c), the input resistance of the LMF40-50 is the same as that of the LMF40-100. The higher the clock-to-cutoff-frequency ratio, the greater equivalent input resistance for a given clock frequency.

This input resistance will form a voltage divider with the source impedance (R_{Source}). Since R_{IN} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to attenuate the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity, the overall gain is given by:

$$A_V = \frac{R_{IN}}{R_{IN} + R_{Source}}$$

If the LMF40-50 or the LMF40-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{IN} = \frac{1 \times 10^{10}}{10\ kHz} = 1\ M\Omega$$

As an example, with a source impedance of 10 kΩ the overall gain would be:

$$A_V = \frac{1\ M\Omega}{10\ k\Omega + 1\ M\Omega} = 0.99009 \text{ or } -0.086\ dB$$

Since the maximum overall gain error for the LMF40 is +0.05, −0.15 dB @ 25°C with $R_S \leq 2\ k\Omega$ the actual gain error for this case would be −0.04 dB to −0.24 dB.

1.4 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit due to leakage currents through the internal switches draining the charge stored on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error. For example:

$$f_{CLK} = 100\ Hz,\ I_{Leakage} = 1\ pA,\ C = 1\ pF$$

$$V = \frac{1\ pA}{1\ pF\ (100\ Hz)} = 10\ mV$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors limit the filter's accuracy at high clock frequencies. The amplitude characteristic on ±5V supplies will typically stay flat until f_{CLK} exceeds 1.5 MHz and then peak at about 0.1 dB at the corner frequency with a 2 MHz clock. As supply voltage drops to ±2.5V, a shift in the f_{CLK}/f_c ratio occurs which will become noticeable when the clock frequency exceeds 500 kHz. The response of the LMF40 is still a good approximation of the ideal Butterworth low-pass characteristic shown in *Figure 5*.

2.0 Designing with the LMF40

Given any low-pass filter specification, two equations will come in handy in trying to determine whether the LMF40 will do the job. The first equation determines the order of the low-pass filter required to meet a given response specification:

$$n = \frac{\log\left[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)\right]}{2 \log (f_s/f_b)} \qquad (2)$$

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at cutoff frequency f_b (Note 15). If the result of this equation is greater than 4, more than one LMF40 will be required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10 \log\left[1 + (10^{0.1A_{max}} - 1)(f/f_b)^{2n}\right] dB \qquad (3)$$

where n = 4 for the LMF40.

2.1 A LOW-PASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 6* is given. Can the LMF40 be used? The order of the Butterworth approximation will have to be determined using (1):

$$A_{min} = 18\ dB,\ A_{max} = 1.0\ dB,\ f_s = 2\ kHz, \text{ and } f_b = 1\ kHz$$

$$n = \frac{\log[(10^{1.8} - 1)/(10^{0.1} - 1)]}{2 \log(2)} = 3.95$$

Since n can only take on integer values, n = 4. Therefore the LMF40 can be used. In general, if n is 4 or less a single LMF40 can be utilized.

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2.0 Designing with the LMF40 (Continued)

Likewise, the attenuation at f_s can be found using (3) with the above values and n = 4:

$$\text{Attn (2 kHz)} = 10 \log[1 + 10^{0.1} - 1)\,(2\text{ kHz}/1\text{ kHz})^8] = 18.28\text{ dB}$$

This result also meets the design specification given in *Figure 6* again verifying that a single LMF40 section will be adequate.

Since the LMF40's cutoff frequency (f_c), which corresponds to a gain attenuation of −3.01 dB, was not specified in this example, it needs to be calculated. Solving equation (3) where $f = f_c$ as follows:

$$f_c = f_b\left[\frac{10^{0.1(3.01\text{ dB})} - 1}{(10^{0.1A_{max}} - 1)}\right]^{1/(2n)}$$

$$= 1\text{ kHz}\left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/8}$$

$$= 1.184\text{ kHz}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$. To implement this example for the LMF40-50 the clock frequency will have to be set to $f_{CLK} = 50(1.184\text{ kHz}) = 59.2\text{ kHz}$, or for the LMF40-100, $f_{CLK} = 100\ (1.184\text{ kHz}) = 118.4\text{ kHz}$.

2.2 CASCADING LMF40s

When a steeper stopband attenuation rate is required, two LMF40s can be cascaded *(Figure 7)* yielding an 8th order slope of 48 dB per octave. Because the LMF40 is a Butterworth filter and therefore has no ripple in its passband, when LMF40s are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 8a*.

In determining whether the cascaded LMF40s will yield a filter that will meet a particular amplitude response specification, as above, equations (4) and (5) can be used, shown below.

$$n = \frac{\log[(10,^{0.05A_{min}} - 1)/(10^{0.05A_{max}} - 1)]}{2\log(f_s/f_b)} \quad (4)$$

$$\text{Attn}(f) = 10\log[1 + (10^{0.05A_{max}} - 1)\,(f/f_b)^2]\text{dB} \quad (5)$$

where n = 4 (the order of each filter).

Equation (4) will determine whether the order of the filter is adequate ($n \le 4$) while equation (5) can determine the actual stopband attenuation and cutoff frequency (f_c) necessary to obtain the desired frequency response. The design procedure would be identical to the one shown in Section 2.0.

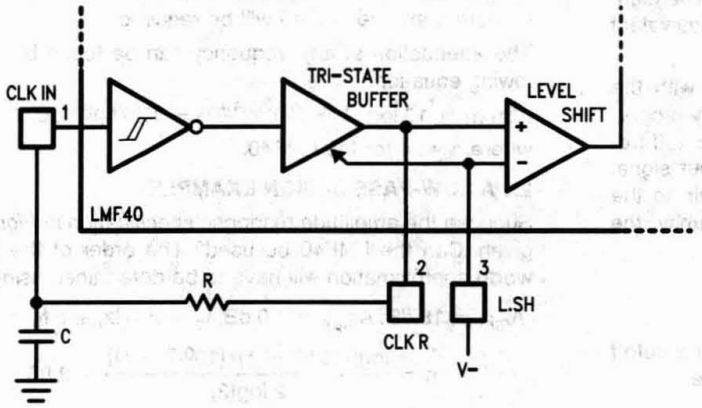
2.3 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The LMF40 responds well to an instantaneous change in clock frequency. If the control signal in *Figure 9* is low the LMF40-50 has a 100 kHz clock making f_c = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding f_c = 1 kHz. As *Figure 9* illustrates, the output signal changes quickly and smoothly in response to a sudden change in clock frequency.

The step response of the LMF40 in *Figure 10* is dependent on f_c. The LMF40 responds as a classical fourth-order Butterworth low-pass filter.

2.4 ALIASING CONSIDERATIONS

Aliasing effects have to be considered when input signal frequencies exceed half the sampling rate. For the LMF40 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency $f_{CLK}/2$, as in *Figure 11a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range below $f_{CLK}/2$, as in *Figure 11b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore, if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the LMF40 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level.



$$f = \frac{1}{RC\ln\left[\left(\frac{V_{CC} - V_{t-}}{V_{CC} - V_{t+}}\right)\left(\frac{V_{t+}}{V_{t-}}\right)\right]}$$

$$f \cong \frac{1}{1.37\,RC}$$

$(V_{CC} = 10V)$

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FIGURE 1. Schmitt Trigger R/C Oscillator

2.0 Designing with the LMF40 (Continued)

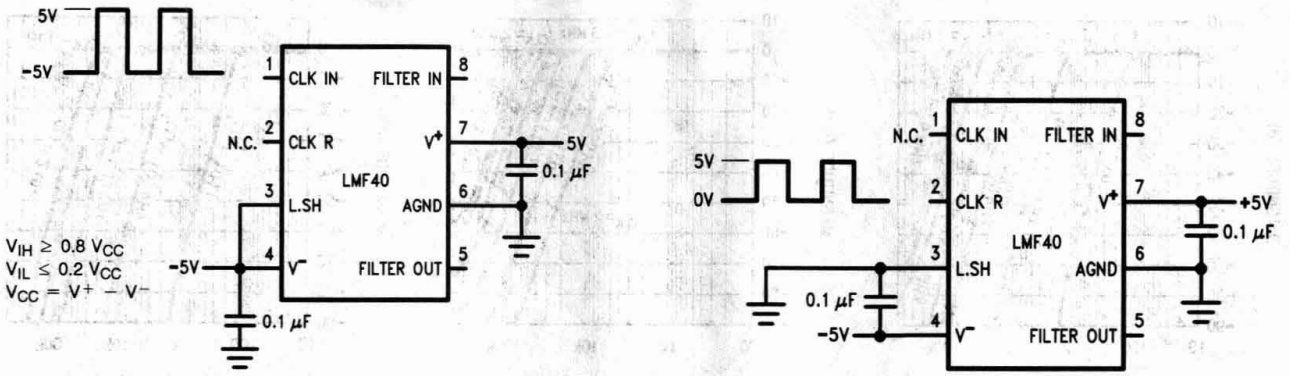


FIGURE 2. Split Supply Operation with CMOS Level Clock (a), and TTL Level Clock (b)

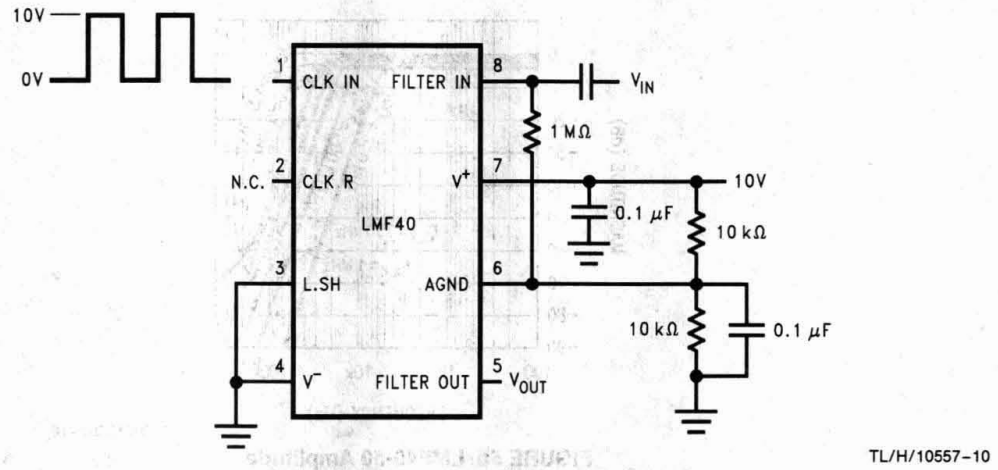
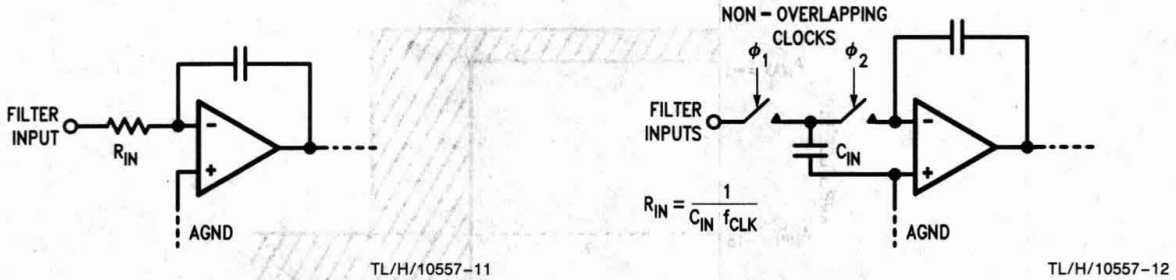


FIGURE 3. Single Supply Operation. AGND Resistor Biased to $V^+/2$



a) Equivalent Circuit for LMF40 Filter Input

b) Actual Circuit for LMF40 Filter Input

FIGURE 4. LMF40 Filter Input

2.0 Designing with the LMF40 (Continued)

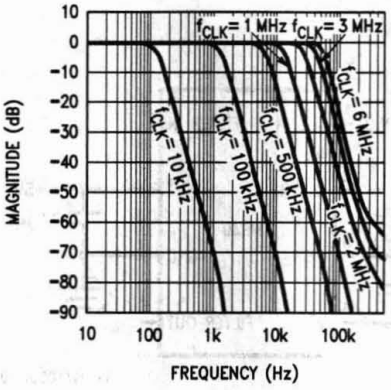


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FIGURE 5a. LMF40-100 Amplitude Response with ±5V Supplies

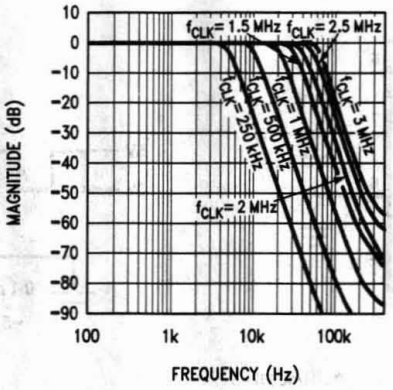

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FIGURE 5b. LMF40-50 Amplitude Response with ±5V Supplies

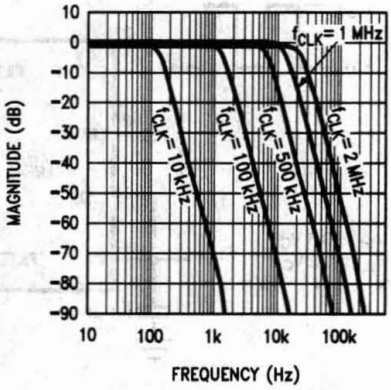

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FIGURE 5c. LMF40-100 Amplitude Response with ±2.5V Supplies

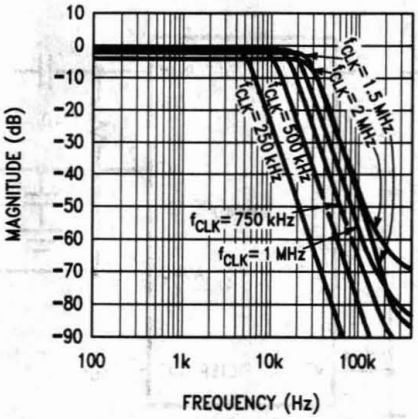

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FIGURE 5d. LMF40-50 Amplitude Response with ±2.5V Supplies

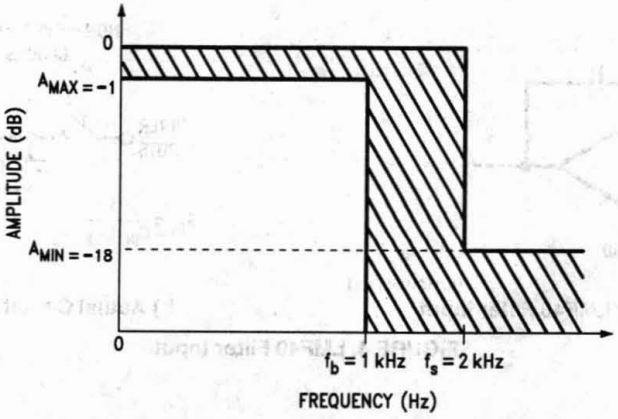

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FIGURE 6. Design Example Magnitude Response Specification. The response of the filter design must fall within the shaded area of the specification.

2.0 Designing with the LMF40 (Continued)

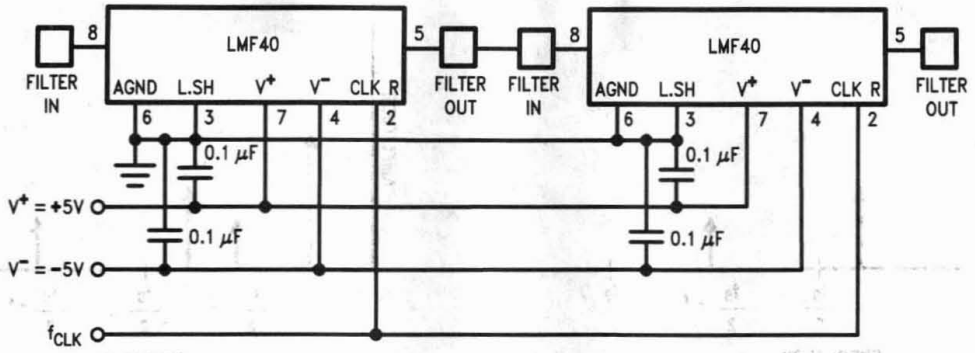

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FIGURE 7. Cascading Two LMF40s

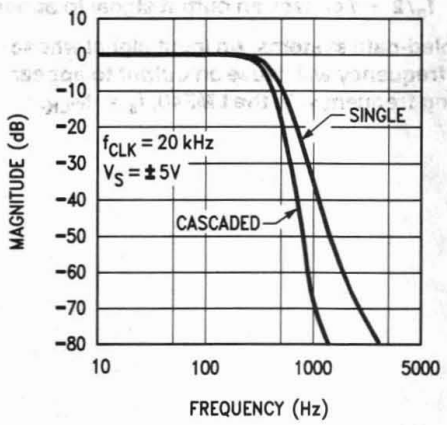

FIGURE 8a. One LMF40-50 vs Two LMF40-50s Cascaded

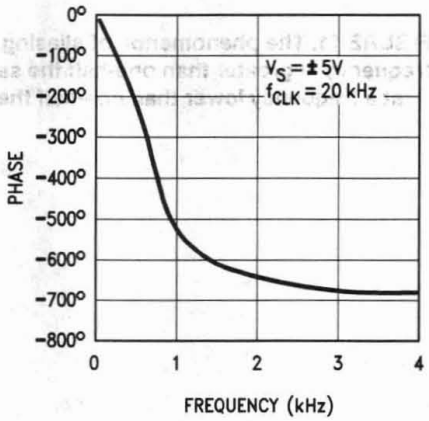

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FIGURE 8b. Phase Response of Two Cascaded LMF40-50s

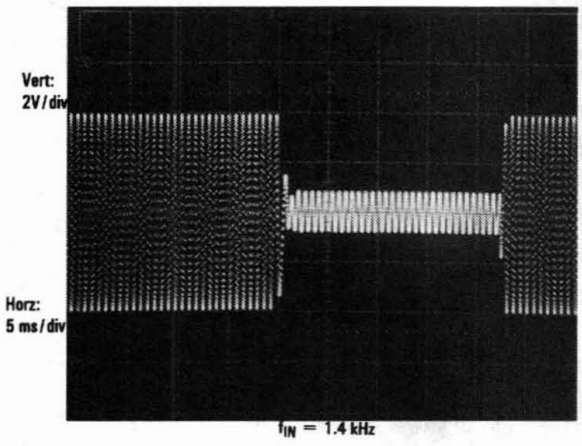

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FIGURE 9. LMF40-50 Abrupt Clock Frequency Change

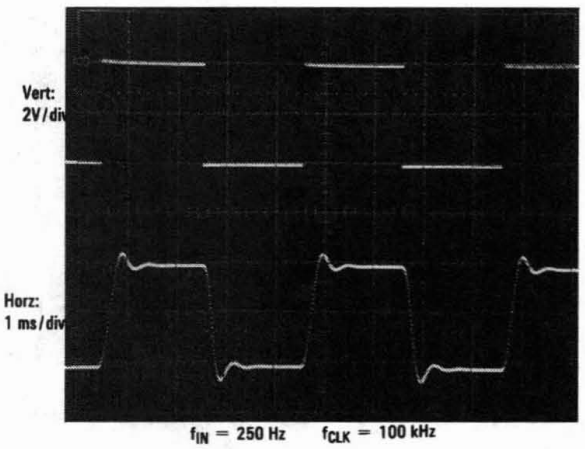

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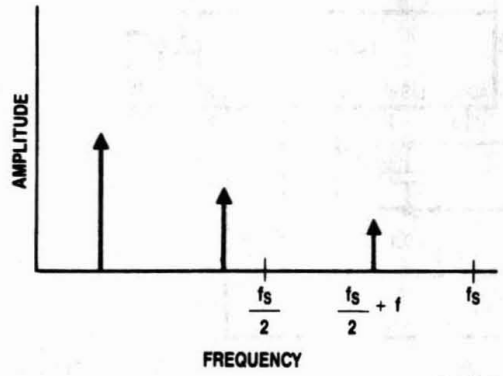
FIGURE 10. LMF40-50 Input Step Response

2.0 Designing with the LMF40 (Continued)



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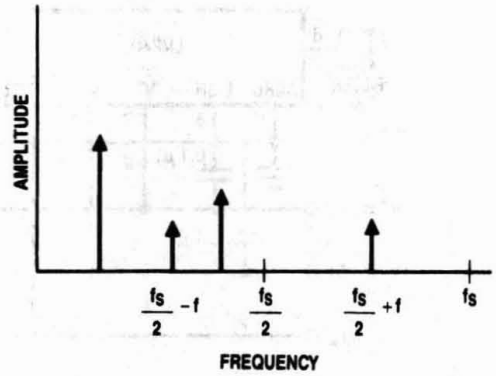
(a) Input Signal Spectrum



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(b)Output Signal Spectrum. Note that the input signal at $f_S/2 + f$ causes an output signal to appear at $f_S/2 - f$.

FIGURE 11. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the LMF40, $f_S = f_{CLK}$.

National Semiconductor

LMF60 High Performance 6th-Order Switched Capacitor Butterworth Lowpass Filter

General Description

The LMF60 is a high performance, precision, 6th-order Butterworth lowpass active filter. It is fabricated using National's LMCMOS process, an improved silicon-gate CMOS process specifically designed for analog products. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50:1 (LMF60-50) or 100:1 (LMF60-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1V/V allows cascading LMF60 sections for higher-order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications. The LMF60 is pin- and functionally-compatible with the MF6, but provides improved performance.

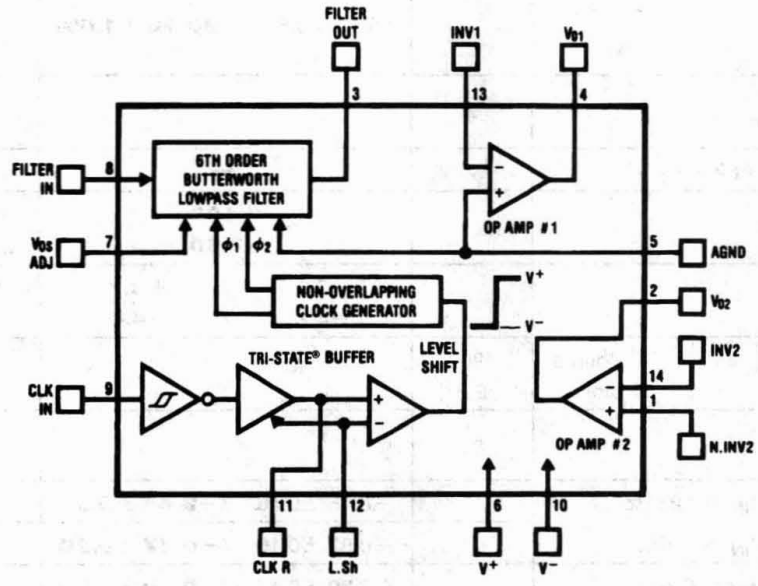
Features

- Cutoff frequency range of 0.1 Hz to 30 kHz
- Cutoff frequency accuracy of ±1.0%, maximum
- Low offset voltage ±100 mV, maximum, ±5V supply
- Low clock feedthrough of 10 mV_{p-p}, typical
- Dynamic range of 88 dB, typical
- Two uncommitted op amps available
- No external components required
- 14-pin DIP or 14-pin wide-body S.O. package
- Single/Dual Supply Operation: +4V to +14V (±2V to ±7V)
- Cutoff frequency set by external or internal clock
- Pin-compatible with the MF6

Applications

- Communication systems
- Audio filtering
- Anti-alias filtering
- Data acquisition noise filtering
- Instrumentation
- High-order tracking filters

Block and Connection Diagrams



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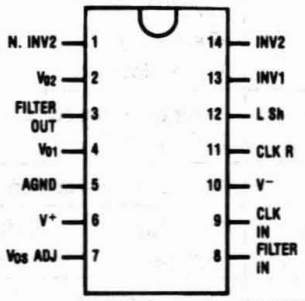
All Packages



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Top View

Order Number LMF60CMJ-50, (5962-9096 701MCA or LMF60CMJ50/883), LMF60CMJ-100, or (5962-9096 702MCA or LMF60CMJ100/883)
See NS Package Number J14A

Order Number LMF60CIWM-50 or LMF60CIWM-100
See NS Package Number M14B

Order Number LMF60CIN-50 or LMF60CIN-100
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) (Note 2)	15V
Voltage at Any Pin	$V^+ + 0.2V$ $V^- - 0.2V$
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 5)	2000V
CLK IN Pin	1700V

Soldering Information:

• N Package: 10 sec.	260°C
• J Package: 10 sec.	300°C
• SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 6)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{Min} \le T_A \le T_{Max}$
LMF60CIN-50, LMF60CIN-100 LMF60CIJ-50, LMF60CIJ-100, LMF60CIWM-50, LMF60CIWM-100	$-40°C \le T_A \le +85°C$
LMF60CMJ-50, LMF60CMJ-100, LMF60CMJ50/883, LMF60CMJ100/883	$-55°C \le T_A \le +125°C$
Supply Voltage ($V^+ - V^-$)	4V to 14V

Filter Electrical Characteristics

The following specifications apply for f_{CLK} = 500 kHz (Note 7) unless otherwise specified. **Boldface limits apply for $T_A = T_J$ = T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
$V^+ = +5V, V^- = -5V$					
f_{CLK}	Clock Frequency Range (Note 16)		5	**1.5**	Hz (Min) MHz (Max)
I_S	Total Supply Current			7.0 / **12.0**	mA (Max)
	Clock Feedthrough	V_{IN} = 0V Filter Opamp	10 5		mVp-p mVp-p
H_o	DC Gain	$R_{Source} \le 2\ k\Omega$		0.10 / **0.10** −0.26 / **−0.30**	dB (Max) dB (Min)
f_{CLK}/f_C	Clock to Cutoff Frequency Ratio (Note 10) LMF60-50			49.00 ±0.8% / **49.00 ±1.0%**	(Max)
	LMF60-100			98.10 ±0.8% / **98.10 ±1.0%**	(Max)
	Temperature Coefficient of f_{CLK}/f_C		4		ppm/°C
A_{MIN}	Stopband Attenuation	At 2 × f_C		**36**	dB (Min)
V_{OS}	DC Offset Voltage LMF60-50			**±100**	mV (Max)
	LMF60-100			**±150**	mV (Max)
V_{OUT}	Output Voltage Swing (Note 2)			+3.9 / **+3.7** −4.2 / **−4.0**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 11)	Source Sink	90 2.2		mA mA
	Dynamic Range (Note 12)		88		dB
	Additional Magnitude Response Test Points (Note 13) LMF60-50	f_{IN} = 12 kHz		−9.45 ±0.46 / **−9.45 ±0.50**	dB
		f_{IN} = 9 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB
	LMF60-100	f_{IN} = 6 kHz		−9.30 ±0.46 / **−9.30 ±0.50**	dB
		f_{IN} = 4.5 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB

Filter Electrical Characteristics (Continued)

The following specifications apply for f_{CLK} = 250 kHz (Note 7) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
$V^+ = +2.5V, V^- = -2.5V$					
f_{CLK}	Clock Frequency Range (Note 16)		5	**750**	Hz (Min) kHz (Max)
I_S	Total Supply Current			5.0 / **6.5**	mA (Max)
	Clock Feedthrough (Peak to Peak)	V_{IN} = 0V Filter Opamp	6 3		mV mV
H_o	DC Gain (with $R_{Source} \leq 2\ k\Omega$)	f_{CLK} = 250 kHz		0.10 / **0.10** −0.26 / **−0.30**	dB (Max) dB (Min)
		f_{CLK} = 500 kHz	−0.08		dB
f_{CLK}/f_C	Clock to Cutoff Frequency Ratio (Note 10) LMF60-50	f_{CLK} = 250 kHz		49.00 ±0.8% / **49.00 ± 1.0%**	(Max)
		f_{CLK} = 500 kHz	49.00 ±0.6%		
	LMF60-100	f_{CLK} = 250 kHz		98.10 ±0.8% / **98.10 ± 1.0%**	(Max)
		f_{CLK} = 500 kHz	98.10 ±0.6%		
	Temperature Coefficient of f_{CLK}/f_C		4		ppm/°C
A_{MIN}	Stopband Attenuation	At 2 × f_C		**36**	dB (Min)
V_{OS}	DC Offset Voltage LMF60-50			**±60**	mV (Max)
	LMF60-100			**±90**	mV (Max)
V_{OUT}	Output Voltage Swing (Note 2)	R_L = 5 kΩ		+1.4 / **+1.2** −2.0 / **−1.8**	V (Max) V (Min)
I_{SC}	Output Short Circuit Current (Note 11)	Source Sink	42 0.9		mA mA
	Dynamic Range (Note 12)		81		dB
	Additional Magnitude Response Test Points (Note 13) LMF60-50	f_{IN} = 6 kHz		−9.45 ±0.46 / **−9.45 ±0.50**	dB
		f_{IN} = 4.5 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB
	LMF60-100	f_{IN} = 3 kHz		−9.30 ±0.46 / **−9.30 ±0.50**	dB
		f_{IN} = 2.25 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB

Op Amp Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
$V^+ = +5V, V^- = -5V$					
V_{OS}	Input Offset Voltage			**±20**	mV (Max)
I_B	Input Bias Current		10		pA
CMRR	Common Mode Rejection Ratio (Op Amp #2 Only)	Test Input Range = −2.2V to +1.8V		**55**	dB
V_O	Output Voltage Swing	$R_L = 5\ k\Omega$		3.8 / **3.6** −4.2 / **−4.0**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 13)	Source Sink	90 2.1		mA mA
SR	Slew Rate		4		V/μs
A_{VOL}	DC Open Loop Gain		80		dB (Min)
GBW	Gain Bandwidth Product		2.0		MHz
$V^+ = +2.5V, V^- = -2.5V$					
V_{OS}	Input Offset Voltage			**±20**	mV (Max)
I_B	Input Bias Current		10		pA
CMRR	Common Mode Rejection Ratio (Op Amp #2 Only)	Test Input Range = −0.9V to +0.5V		**55**	dB
V_O	Output Voltage Swing	$R_L = 5\ k\Omega$		1.3 / **1.1** −1.8 / **−1.6**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 13)	Source Sink	42 0.9		mA mA
SR	Slew Rate		3		V/μs
A_{VOL}	DC Open Loop Gain		74		dB (Min)
GBW	Gain Bandwidth Product		2.0		MHz

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (Note 15), L.Sh = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
TTL CLOCK INPUT, CLK R PIN (NOTE 14)						
V_{IH} V_{IL}	TTL Input Voltage	Logical "1" Logical "0"	$V^+ = +5V, V^- = -5V$		**2.0** **0.8**	V (Min) V (Max)
V_{IH} V_{IL}	CLK R Input Voltage	Logical "1" Logical "0"	$V^+ = +2.5V, V^- = -2.5V$		**2.0** 0.6 / **0.4**	V (Min) V (Max)
	Maximum Leakage Current at CLK R			2.0		μA

Logic Input-Output Characteristics (Continued)

The following specifications apply for V^- = 0V (Note 15), L.Sh = 0V unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
SCHMITT TRIGGER					
V_{T+}	Positive Going Input Threshold Voltage	V^+ = 10V		6.1 / **6.0** 8.8 / **8.9**	V (Min) V (Max)
		V^+ = 5V		3.0 / **2.9** 4.3 / **4.4**	V (Min) V (Max)
V_{T-}	Negative Going Input Threshold Voltage	V^+ = 10V		1.4 / **1.3** 3.8 / **3.9**	V (Min) V (Max)
		V^+ = 5V		0.7 / **0.6** 1.9 / **2.0**	V (Min) V (Max)
$V_{T+} - V_{T-}$	Hysteresis	V^+ = 10V		2.3 / **2.1** 7.4 / **7.6**	V (Min) V (Max)
		V^+ = 5V		1.1 / **0.9** 3.6 / **3.8**	V (Min) V (Max)
V_{OH}	Logical "1" Voltage I_O = −10 μA, Pin 11	V^+ = +10V V^+ = +5V		9.1 / **9.0** 4.6 / **4.5**	V (Min) V (Min)
V_{OL}	Logical "0" Voltage I_O = −10 μA, Pin 11	V^+ = +10V V^+ = +5V		0.9 / **1.0** 0.4 / **0.5**	V (Max) V (Max)
I_{SOURCE}	Output Source Current, Pin 11	CLK R to V^- V^+ = +10V V^+ = +5V		 4.9 / **3.7** 1.6 / **1.2**	 mA (Min) mA (Min)
I_{SINK}	Output Sink Current, Pin 11	CLK R to V^+ V^+ = +10V V^+ = +5V		 4.9 / **3.7** 1.6 / **1.2**	 mA (Min) mA (Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. Specified Electrical Characteristics do not apply when operating the device outside its specified conditions.

Note 2: All voltages are measured with respect to AGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with 5 mA to four.

Note 4: The Maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J\,Max}$, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is PD = $(T_{J\,Max} - T_A)/\theta_{JA}$ or the number given in the absolute ratings, whichever is lower. For this device, $T_{J\,Max}$ = 125°C, and the typical junction-to-ambient thermal resistance of the LMF60CCN when board mounted is 67°C/W. For the LMF60CIJ this number decreases to 62°C/W. For the LMF60CIWM, θ_{JA} = 78°C/W.

Note 5: Human body model: 100 pF discharged through a 1.5 kΩ resistor.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any current Linear Databook for other methods of soldering surface mount devices.

Note 7: The specifications given are for a clock frequency (f_{CLK}) of 500 kHz at +5V and 250 kHz at ±2.5V. Above this frequency, the cutoff frequency begins to deviate from the specified error band over the temperature range but the filter still maintains its amplitude characteristics. See application hints.

Note 8: Typicals are at 25°C and represent the most likely parametric norm.

Note 9: Guaranteed to National's Average Outgoing Quality Level (AOQL).

Note 10: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 11: The short circuit source current is measured by forcing the output to its maximum positive swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 12: For ±5V supplies the dynamic range is referenced to 2.62 V_{rms} (3.7V peak), where the wideband noise over a 20 kHz bandwidth is typically 100 μV. For ±2.5V supplies the dynamic range is referenced to 0.849 V_{rms} (1.2V peak), where the wideband noise over a 20 kHz bandwidth is typically 75 μV_{rms}.

Note 13: The filter's magnitude response is tested at the cutoff frequency, f_C, at f_{IN} = 2 f_C, and at these two additional frequencies.

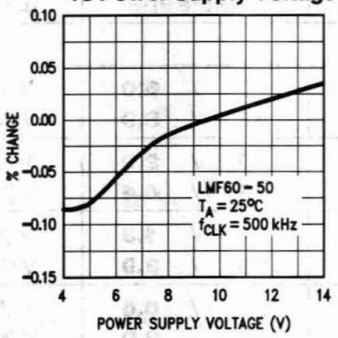
Note 14: The LMF60 is operated with symmetrical supplies and L.Sh is tied to GND.

Note 15: For simplicity all the logic levels (except for the TTL input logic levels) have been referenced to V^- = 0V. The logic levels will scale accordingly for ±5V and ±2.5V supplies.

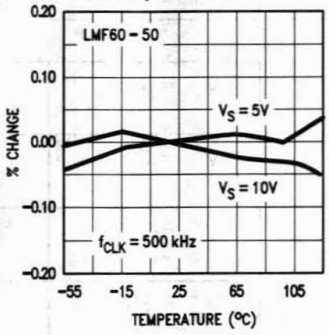
Note 16: The nominal ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50-to-1 (LMF60-50) or 100-to-1 (LMF60-100).

Typical Performance Characteristics

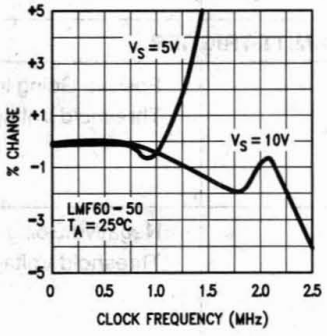
f_{CLK}/f_C Deviation vs Power Supply Voltage



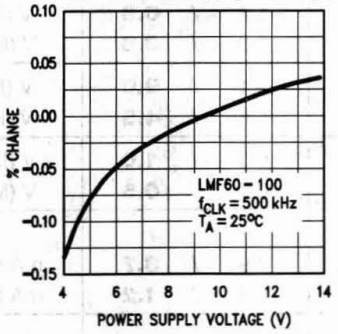
f_{CLK}/f_C Deviation vs Temperature



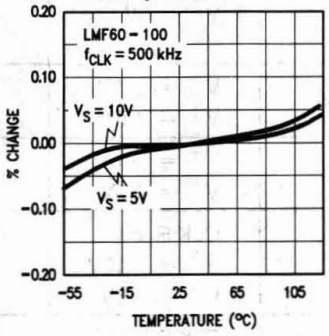
f_{CLK}/f_C Deviation vs Clock Frequency



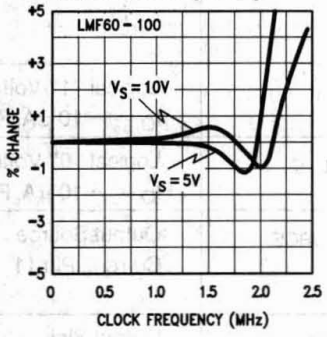
f_{CLK}/f_C Deviation vs Power Supply Voltage



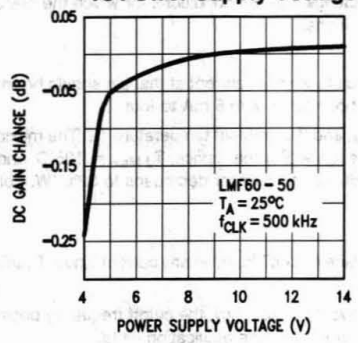
f_{CLK}/f_C Deviation vs Temperature



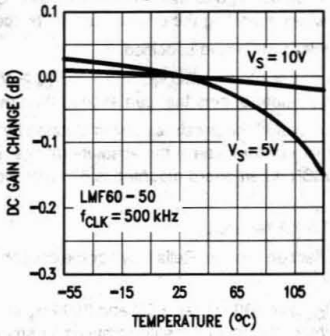
f_{CLK}/f_C Deviation vs Clock Frequency



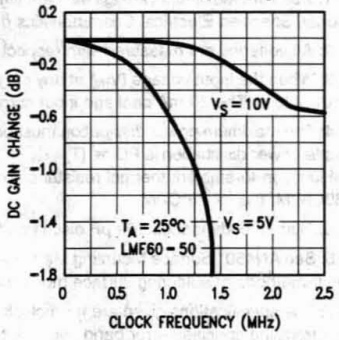
DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



DC Gain Deviation vs Clock Frequency



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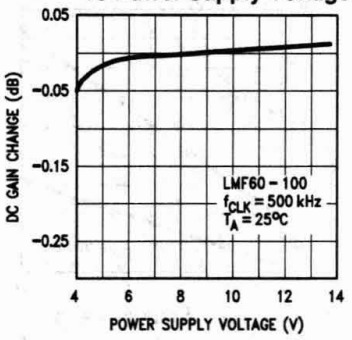
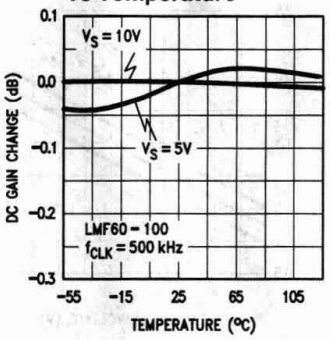
Typical Performance Characteristics (Continued)

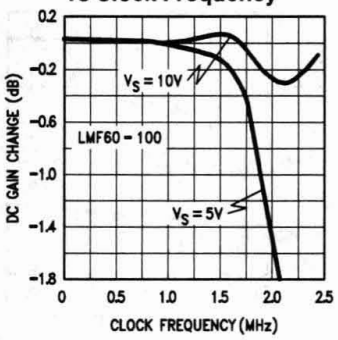
DC Gain Deviation vs Power Supply Voltage



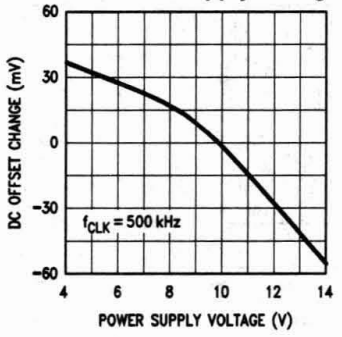
DC Gain Deviation vs Temperature



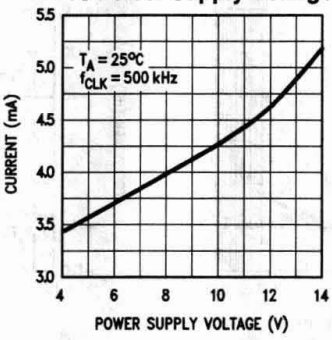
DC Gain Deviation vs Clock Frequency



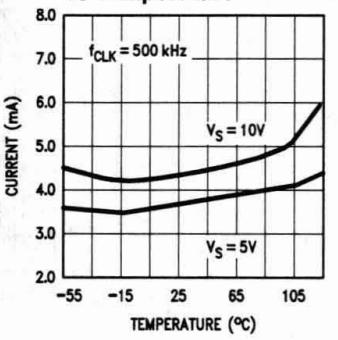
DC Offset Voltage Deviation vs Power Supply Voltage



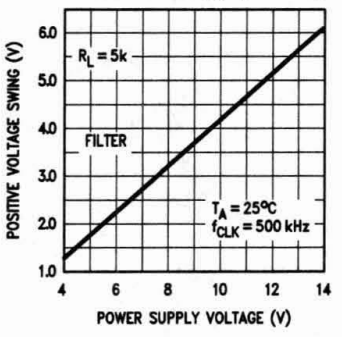
Power Supply Current vs Power Supply Voltage



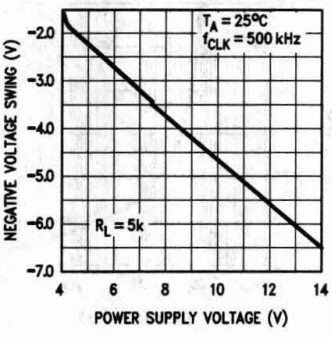
Power Supply Current vs Temperature



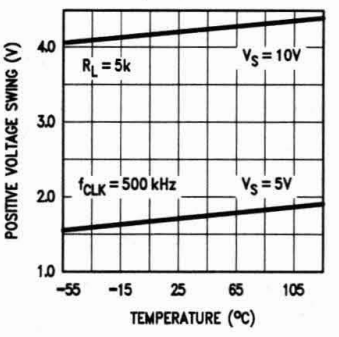
Positive Voltage Swing vs Power Supply Voltage



Negative Voltage Swing vs Power Supply Voltage



Positive Voltage Swing vs Temperature



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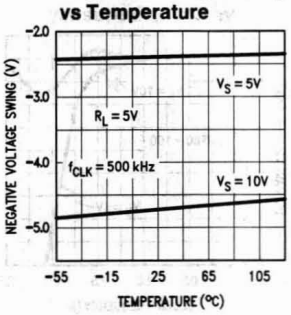
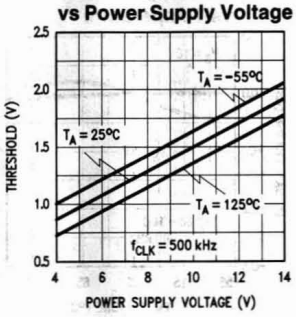
Typical Performance Characteristics (Continued)

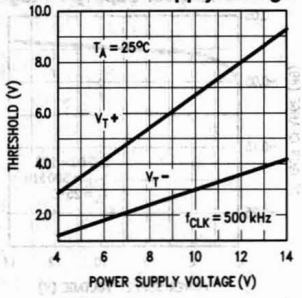
Negative Voltage Swing vs Temperature



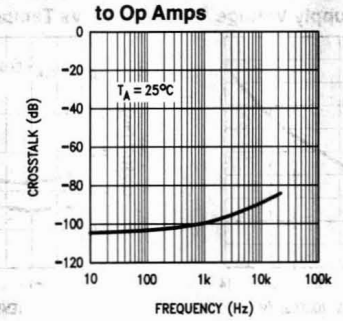
CLK R Trigger Threshold vs Power Supply Voltage



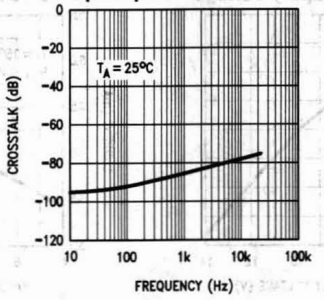
Schmitt Trigger Threshold vs Power Supply Voltage



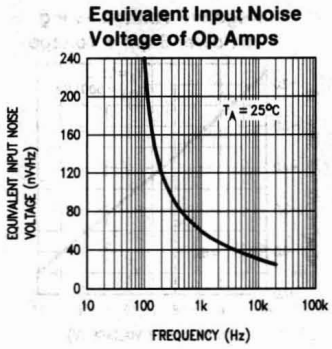
Crosstalk from Filter to Op Amps



Crosstalk from Either Op Amp to Filter



Equivalent Input Noise Voltage of Op Amps



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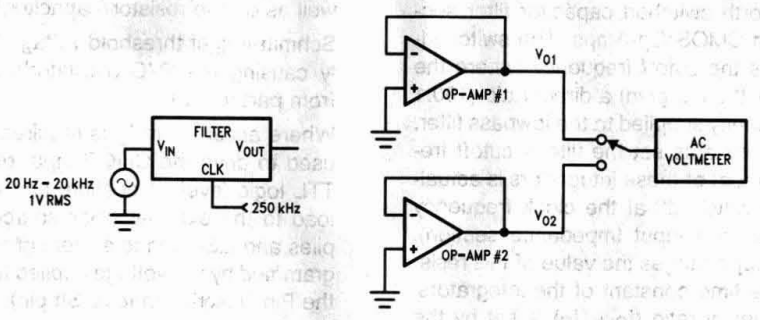
Crosstalk Test Circuits

From Filter to Op-Amps



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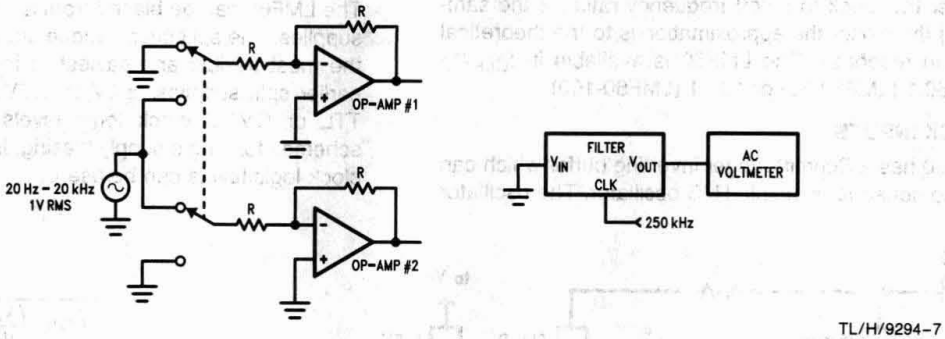
From Either Op-Amp to Filter Output



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Pin Description (Pin Numbers)

Pin	Description
FILTER OUT (3)	The output of the lowpass filter will typically swing to within 1V of each supply rail.
FILTER IN (8)	The input to the lowpass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (See Section 1.4). For single supply operation the input signal must be biased to mid-supply or AC coupled.
V_{OS}ADJ (7)	This pin is used to adjust the DC offset of the filter output; if not used it must be tied to the AGND potential. (See Section 1.3)
AGND (5)	The analog ground pin. This pin sets the DC bias level for the filter section and the noninverting input of Op-Amp #1 and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (See Section 1.2). When tied to mid-supply this pin should be well bypassed.
V_{O1}(4), INV1 (13)	V_{O1} is the output and INV1 is the inverting input of Op-Amp #1. The non-inverting input of this Op-Amp is internally connected to the AGND pin.
V_{O2}(2), INV2 (14), NINV2 (1)	V_{O2} is the output, INV2 is the inverting input, and NINV2 is the non-inverting input of Op-Amp #2.
V^+ (6), V^- (10)	The positive and negative supply pins. The total power supply range is 4V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
CLK IN (9)	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self-clocking Schmitt-trigger oscillator (See Section 1.1).
CLK R (11)	A TTL logic level clock input when in split supply operation ($\pm$2V to $\pm$7V) and L. Sh tied to system ground. This pin becomes a low impedance output when L.Sh is tied to V^-. Also used in conjunction with the CLK IN pin for self clocking Schmitt-trigger oscillator (See Section 1.1).
L.Sh (12)	Level shift pin, selects the logic threshold levels for the desired clock. When tied to V^- it enables an internal TRI-STATE® buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds [25% ($V^+ - V^-$) + V^-] the internal TRI-STATE® buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level shift stage. The CLK R threshold level is now 2V above the voltage applied to the L.Sh pin. Driving the CLK R pin with TTL logic levels can be accomplished through the use of split supplies and by tying the L.Sh pin to system ground.

1.0 LMF60 Application Hints

The LMF60 is comprised of a non-inverting unity gain lowpass sixth-order Butterworth switched capacitor filter section and two undedicated CMOS Op-Amps. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the lowpass filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock to cutoff frequency ratio (f_{CLK}/f_C) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock to cutoff frequency ratio (or the sampling rate) the closer the approximation is to the theoretical Butterworth response. The LMF60 is available in f_{CLK}/f_C ratios of 50:1 (LMF60-50) or 100:1 (LMF60-100).

1.1 CLOCK INPUTS

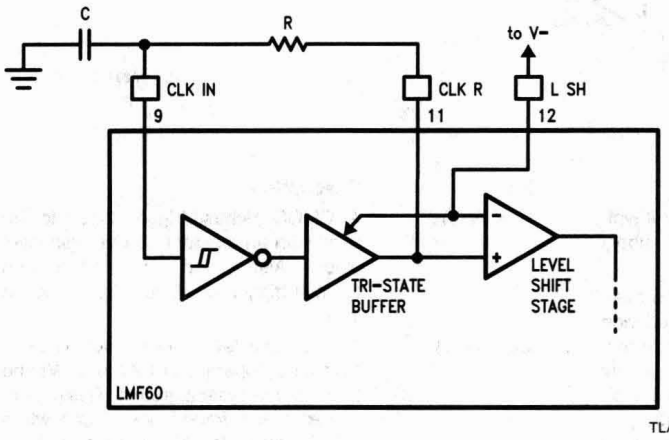
The LMF60 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. The oscillator frequency is dependent on the buffer's threshold levels as well as on the resistor/capacitor tolerance (See *Figure 1*).

Schmitt-trigger threshold voltage levels can vary significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accuracy in f_C is required an external clock can be used to drive the CLK R input of the LMF60. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 μA) with split supplies and L.Sh tied to system ground. The logic level is programmed by the voltage applied to level shift (L.Sh) pin (See the Pin Description for L.Sh pin).

1.2 POWER SUPPLY BIASING

The LMF60 can be biased from a single supply or dual split supplies. The split supply mode shown in *Figures 2* and *3* is the most flexible and easiest to implement. As discussed earlier split supplies, ±2V to ±7V, will enable the use of TTL or CMOS clock logic levels. *Figure 4* shows two schemes for single supply biasing. In this mode only CMOS clock logic levels can be used.



TL/H/9294–8

FIGURE 1. Schmitt Trigger R/C Oscillator

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\frac{V_{T+}}{V_{T-}}\right]}$$

Typically for $V_{CC} = V^+ - V^- = 10V$:

$$f_{CLK} = \frac{1}{1.37\,RC}$$

1.0 LMF60 Application Hints (Continued)

If the LMF60-50 or the LMF60-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{IN} = \frac{1 \times 10^{10}}{10\ kHz} = 1\ M\Omega$$

In this example with a source impedance of 10k the overall gain, if the LMF60 had an ideal gain of 1 (0 dB) would be:

$$A_V = \frac{1\ M\Omega}{10\ k\Omega + 1\ M\Omega} = 0.99009\ (-86.4\ mdB)$$

Since the maximum overall gain error for the LMF60 is +0.1 dB, −0.3 dB with a $R_S \leq 2\ k\Omega$ the actual gain error for this case would be +0.21 dB to −0.39 dB.

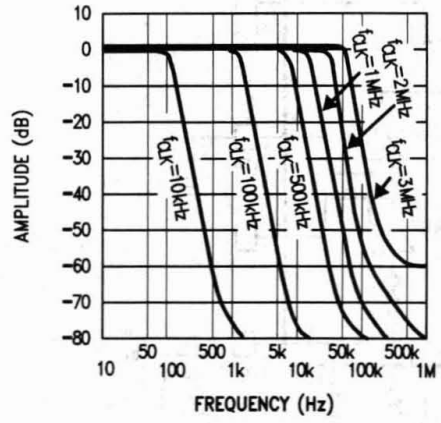
1.5 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_C) has a lower limit caused by leakage currents through the internal switches discharging the stored charge on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ Hz,\ I_{LEAKAGE} = 1\ pA,\ C = 1\ pF$$

$$V = \frac{1\ pA}{1\ pF\ (100\ Hz)} = 10\ mV$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors increases as the LMF60 power supply voltage decreases. This causes a shift in the f_{CLK}/f_C ratio which will become noticeable when the clock frequency exceeds 500 kHz. The amplitude characteristic will stay within tolerance until f_{CLK} exceeds 750 kHz and will peak at about 0.4 dB at the cutoff frequency with a 2 MHz clock. The response of the LMF60 is still a reasonable approximation of the ideal Butterworth lowpass characteristic as can be seen in *Figure 7*.



TL/H/9294–17

FIGURE 7a. LMF60-100 ±5V Supplies Amplitude Response

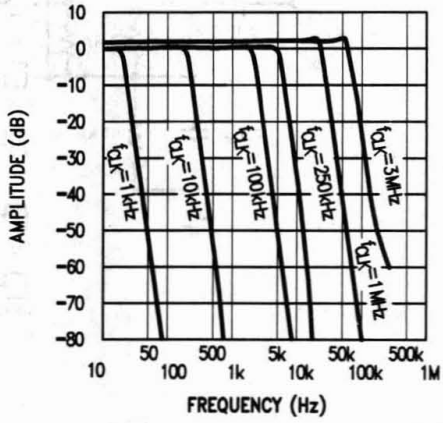


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FIGURE 7b. LMF60-50 ±5V Supplies Amplitude Response

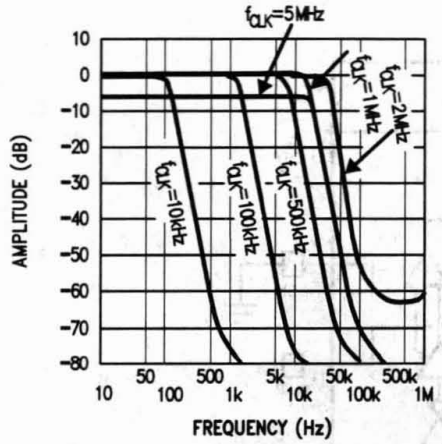

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FIGURE 7c. LMF60-100 ±2.5V Supplies Amplitude Response

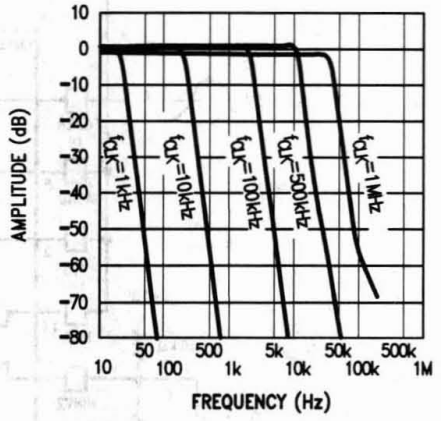

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FIGURE 7d. LMF60-50 ±2.5V Supplies Amplitude Response

1.0 LMF60 Application Hints (Continued)

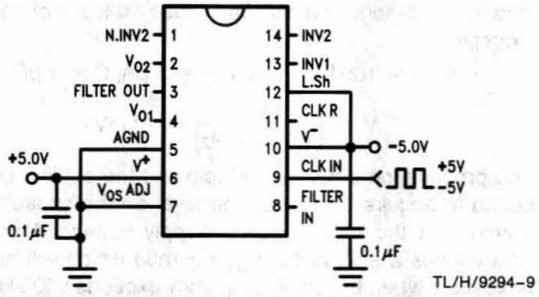


FIGURE 2. Dual Supply Operation LMF60 Driven with CMOS Logic Level Clock ($V_{IH} \geq V^+ - 0.3\ V_S$ and $V_{IL} \leq V^- + 0.3\ V_S$ where $V_S = V^+ - V^-$)

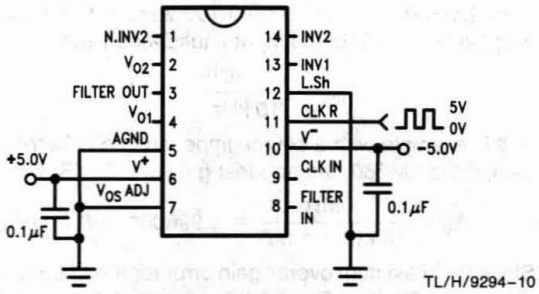
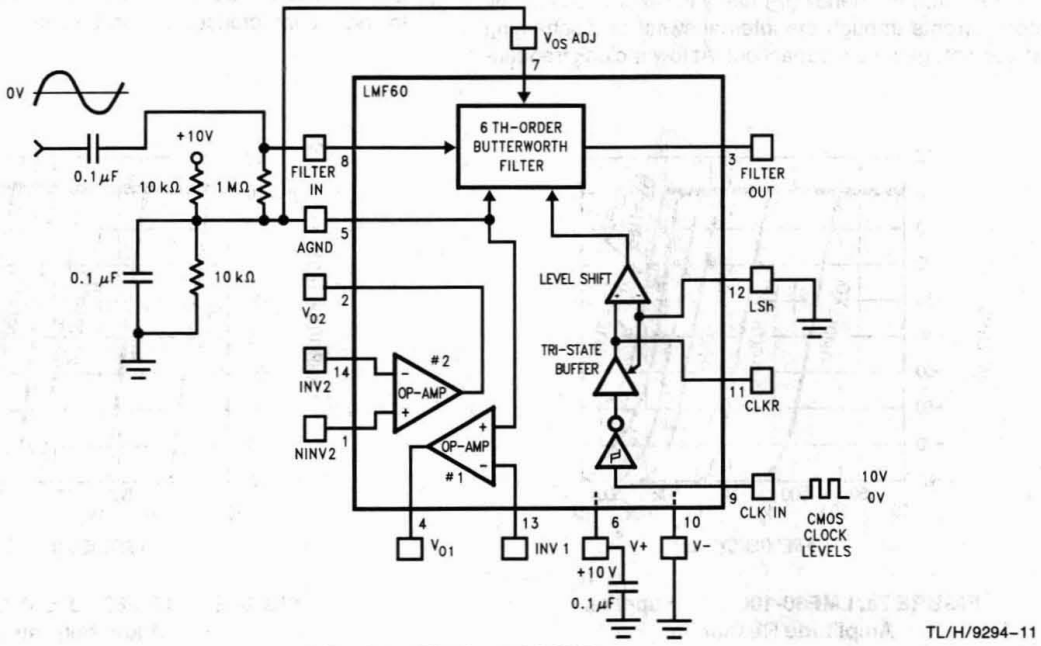
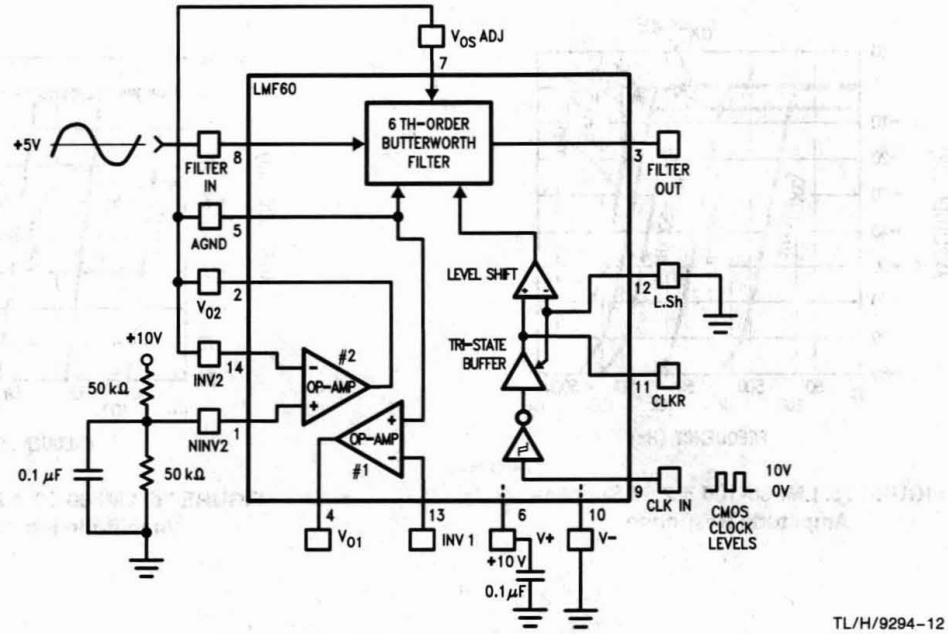


FIGURE 3. Dual Supply Operation LMF60 Driven with TTL Logic Level Clock



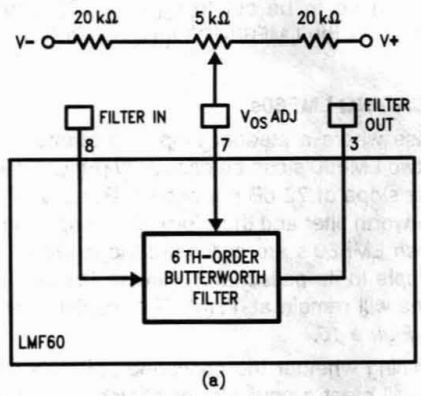
a) Resistor Biasing of AGND



b) Using Op-Amp 2 to Buffer AGND

FIGURE 4. Single Supply Operation

1.0 LMF60 Application Hints (Continued)



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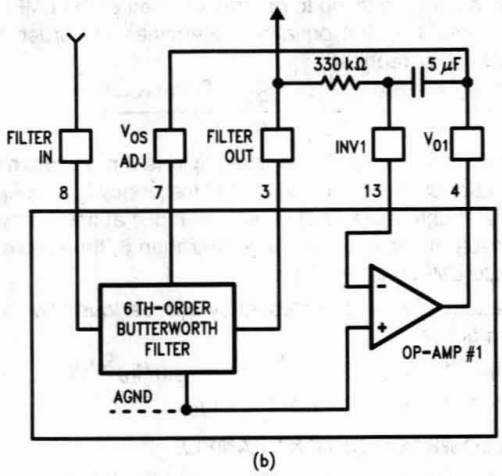

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FIGURE 5. V_{OS} Adjust Schemes

1.3 OFFSET ADJUST

The V_{OS}ADJ pin is used in adjusting the output offset level of the filter section. If this pin is not used it must be tied to the analog ground (AGND) level, either mid-supply for single ended supply operation or ground for split supply operation. This pin sets the zero reference for the output of the filter. The implementation of this pin can be seen in *Figure 5*. In *5(a)* DC offset is adjusted using a potentiometer; in *5(b)* the Op-Amp integrator circuit keeps the average DC output level at AGND. The circuit in *5(b)* is therefore appropriate only for AC-coupled signals and signals biased at AGND.

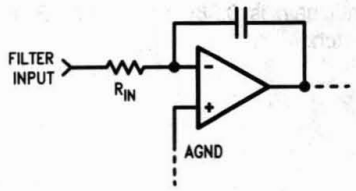
1.4 INPUT IMPEDANCE

The LMF60 lowpass filter input (FILTER IN pin) is not a high impedance buffer input. This input is a switched capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the input to the filter can be seen in *Figure 6*. The input capacitor charges to the input voltage (V_{IN}) during one half of the clock period, during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{IN}V_{IN}$, and since current is defined as the flow of charge per unit time the average input current becomes

$$I_{IN} = Q/T$$

(where T equals one clock period) or

$$I_{IN} = \frac{C_{IN}V_{IN}}{T} = C_{IN}V_{IN}f_{CLK}$$



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a) Equivalent Circuit for LMF60 Filter Input

The equivalent input resistor (R_{IN}) then can be defined as

$$R_{IN} = V_{IN}/I_{IN} = \frac{1}{C_{IN}f_{CLK}}$$

The input capacitor is 2 pF for the LMF60-50 and 1 pF for the LMF60-100, so for the LMF60-100

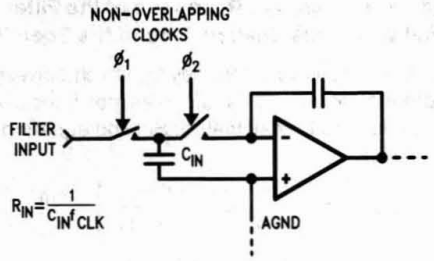
$$R_{IN} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_C \times 100} = \frac{1 \times 10^{10}}{f_C}$$

and

$$R_{IN} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_C \times 50} = \frac{1 \times 10^{10}}{f_C}$$

for the LMF60-50. As shown in the above equations, for a given cutoff frequency (f_C) the input impedance remains the same for the LMF60-50 and the LMF60-100. The higher the clock to cutoff frequency ratio, the greater equivalent input resistance for a given clock frequency. As the cutoff frequency increases the equivalent input impedance decreases. This input resistance will form a voltage divider with the source impedance (R_{SOURCE}). Since R_{IN} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain at the output of the filter. Since the filter's ideal gain is unity, its overall gain is given by:

$$A_V = \frac{R_{IN}}{R_{IN} + R_{SOURCE}}$$



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b) Actual Circuit for LMF60 Filter Input

FIGURE 6. LMF60 Filter Input

2.0 Designing with the LMF60

Given any lowpass filter specification, two equations will come in handy in trying to determine whether the LMF60 will do the job. The first equation determines the order of the lowpass filter required:

$$n = \frac{\log(10^{0.1A_{Min}} - 1) - \log(10^{0.1A_{Max}} - 1)}{2\log(f_s/f_b)} \quad (1)$$

where n is the order of the filter, A_{Min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{Max} is the passband ripple or attenuation (in dB) at frequency f_b. If the result of this equation is greater than 6, then more than a single LMF60 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10\log[1 + (10^{0.1A_{Max}} - 1)(f/f_b)^{2n}]\text{dB} \quad (2)$$

where n = 6 (the order of the filter).

2.1 A LOWPASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 8* is given. Can the LMF60 be used? The order of the Butterworth approximation will have to be determined using eq. 1:

A_{Min} = 30 dB, A_{Max} = 1.0 dB, f_s = 2 kHz, and f_b = 1 kHz

$$n = \frac{\log(10^3 - 1) - \log(10^{0.1} - 1)}{2\log(2)} = 5.96$$

Since n can only take on integer values, n = 6. Therefore the LMF60 can be used. In general, if n is 6 or less a single LMF60 stage can be utilized.

Likewise, the attenuation at f_s can be found using equation 2 with the above values and n = 6 giving:

$$\text{Atten (2 kHz)} = 10\log[1 + (10^{0.1} - 1)(2/1)^{12}]$$
$$= 30.26\text{ dB}$$

This result also meets the design specification given in *Figure 8* again verifying that a single LMF60 section will be adequate.

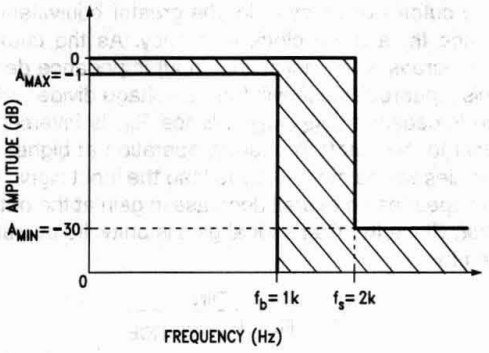

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FIGURE 8. Design Example Magnitude Response Specification Where the Response of the Filter Design Must Fall Within the Shaded Area of the Specification

Since the LMF60's cutoff freqency f_C, which corresponds to a gain attenuation of −3.01 dB, was not specified in this example it needs to be calculated. Solving equation 2 where $f = f_C$ as follows:

$$f_c = f_b\left[\frac{10^{0.1(3.01\text{ dB})} - 1)}{(10^{0.1A_{Max}} - 1)}\right]^{1/(2n)}$$
$$= 1\left(\frac{10^{0.301} - 1}{10^{0.1} - 1}\right)^{1/12}$$
$$= 1.119\text{ kHz}$$

where $f_C = f_{CLK}/50$ or $f_{CLK}/100$.

To implement this example for the LMF60-50 the clock frequency will have to be set to f_{CLK} = 50(1.119 kHz) = 55.95 kHz or for the LMF60-100 f_{CLK} = 100(1.119 kHz) = 111.9 kHz

2.2 CASCADING LMF60s

In the case where a steeper stopband attenuation rate is required two LMF60's can be cascaded *(Figure 9)* yielding a 12th order slope of 72 dB per octave. Because the LMF60 is a Butterworth filter and therefore has no ripple in its passband, when LMF60's are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 10*.

In determining whether the cascaded LMF60's will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log(10^{0.05\,A_{min}} - 1) - \log(10^{0.05\,A_{Max}} - 1)}{2\log(f_s/f_b)} \quad (3)$$

$$\text{Attn}(f) = 10\log[1 + (10^{0.05\,A_{Max}} - 1)(f/f_b)^{2n}]\text{ dB} \quad (4)$$

where n = 6 (the order of each filter).

Equation 3 will determine whether the order of the filter is adequate ($n \leq 6$) while equation 4 can determine if the required stopband attenuation is met and what actual cutoff frequency (f_C) is required to obtain the particular frequency response desired. The design procedure would be identical to the one shown in Section 2.1.

2.3 IMPLEMENTING A "NOTCH" FILTER WITH THE LMF60

A "notch" filter with 60 dB of attenuation can be obtained by using one of the Op-Amps available in the LMF60 and three external resistors. The circuit and amplitude response are shown in *Figure 11*.

The frequency where the "notch" will occur is equal to the frequency at which the output signal of the LMF60 will have the same magnitude but be 180 degrees out of phase with its input signal. For a sixth order Butterworth filter 180° phase shift occurs where $f = f_n = 0.742\,f_C$. The attenuation at this frequency is 0.12 dB which must be compensated for by making $R_1 = 1.014 \times R_2$.

Since R_1 does not equal R_2 there will be a gain inequality above and below the notch frequency. At frequencies below the notch frequency ($f \ll f_n$), the signal through the filter has a gain of one and is non-inverting. Summing this with the input signal through the Op-Amp yields an overall gain of two or +6 dB. For $f \gg f_n$, the signal at the output of the filter is greatly attenuated thus only the input signal will appear at the output of the Op-Amp. With $R_3 = R_1 = 1.014\,R_2$ the overall gain is 0.986 or −0.12 dB at frequencies above the notch.

2.0 Designing with the LMF60 (Continued)

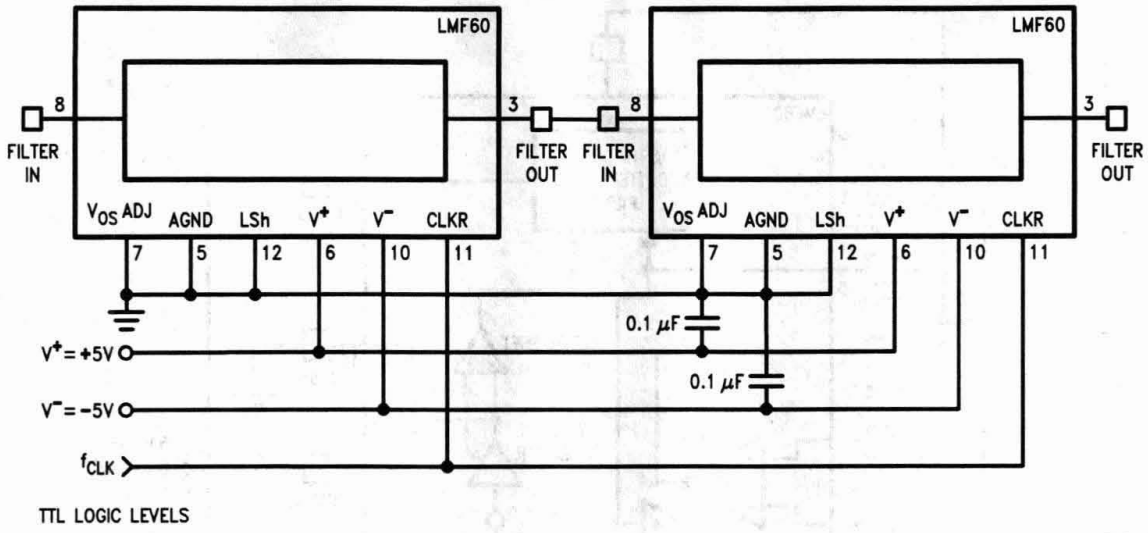

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FIGURE 9. Cascading Two LMF60s

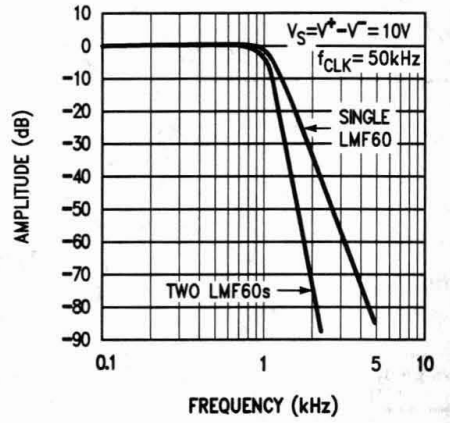

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FIGURE 10a. One LMF60-50 vs. Two LMF60-50s Cascaded

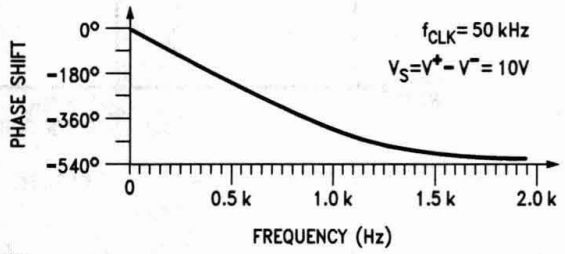

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FIGURE 10b. Phase Response of Two Cascaded LMF60-50s

2.0 Designing with the LMF60 (Continued)

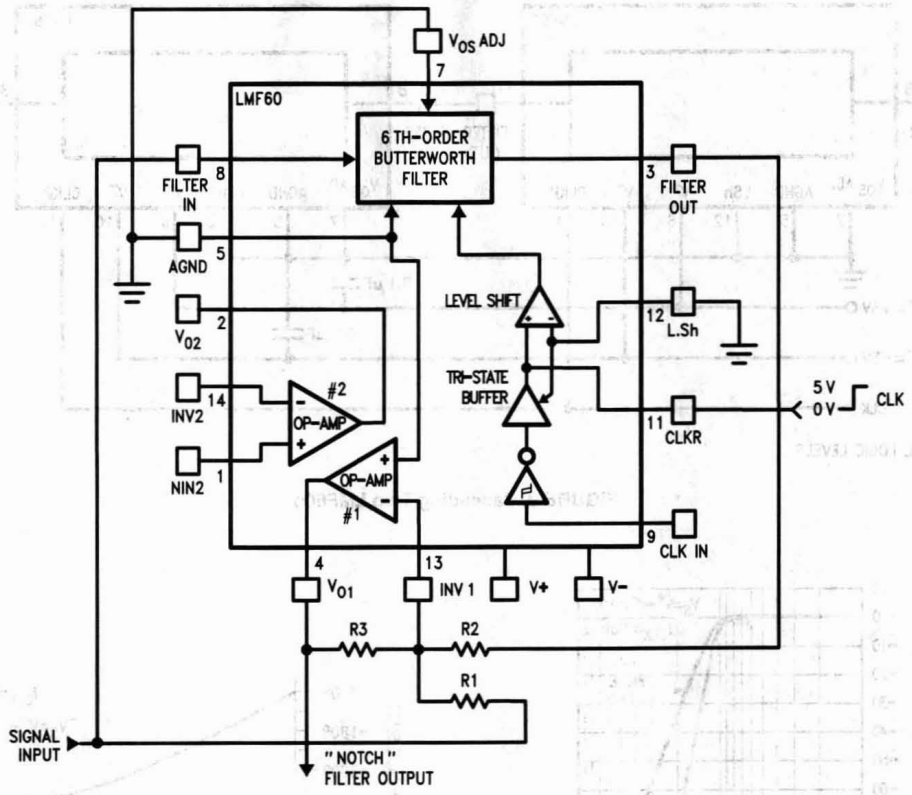

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FIGURE 11a. "Notch" Filter

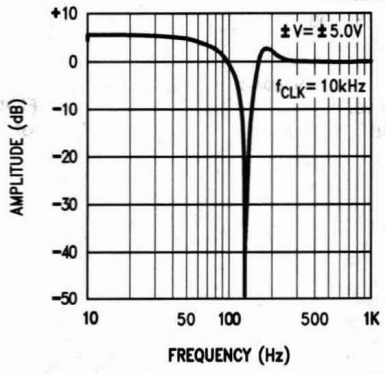

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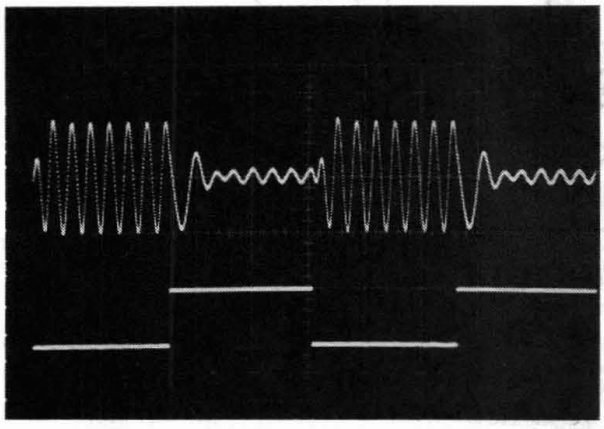
FIGURE 11b. LMF60-50 "Notch" Filter Amplitude Response

2.0 Designing with the LMF60 (Continued)

2.4 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The LMF60 will respond well to a sudden change in clock frequency. Distortion in the output signal occurs at the transition of the clock frequency and lasts approximately three cutoff frequency (f_C) cycles. As shown in *Figure 12*, if the control signal is low the LMF60-50 has a 100 kHz clock making f_C = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding 1 kHz f_C.

The transient response of the LMF60 seen in *Figure 13* is also dependent on the f_c and thus the f_{CLK} applied to the filter. The LMF60 responds as a classical sixth order Butterworth lowpass filter.



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f_{IN} = 1.5 kHz (Scope Time Base = 2 ms/Div)

FIGURE 12. LMF60-50 Abrupt Clock Frequency Change

2.5 ALIASING CONSIDERATIONS

Aliasing effects have to be taken into consideration when input signal frequencies exceed half the sampling rate. For the LMF60 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency, as in *Figure 14a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range *below* $f_{CLK}/2$ as in *Figure 14b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the LMF60 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level. An example circuit is shown in *Figure 15* using one of the uncommitted Op-Amps available in the LMF60.

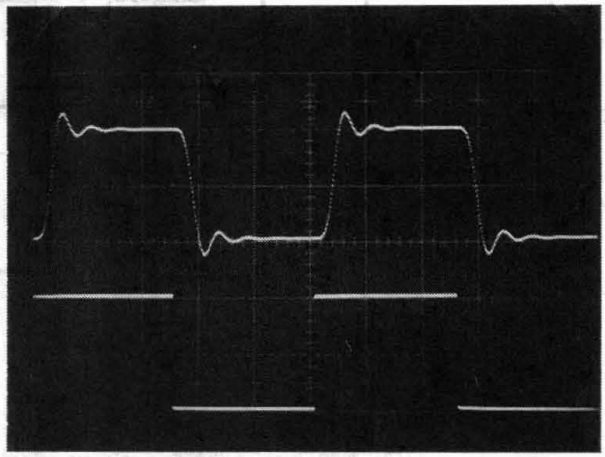

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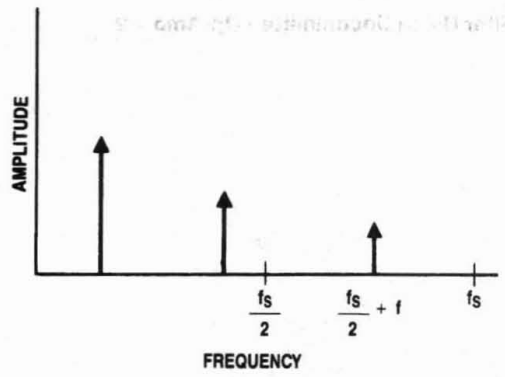
FIGURE 13. LMF60-50 Step Input Response, Vertical = 2V/Div., Horizontal = 1 ms/Div., f_{CLK} = 100 kHz



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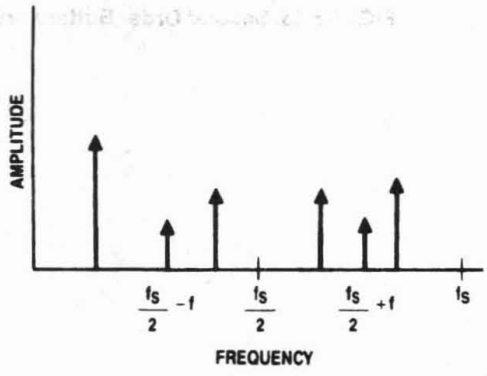
(a) Input Signal Spectrum



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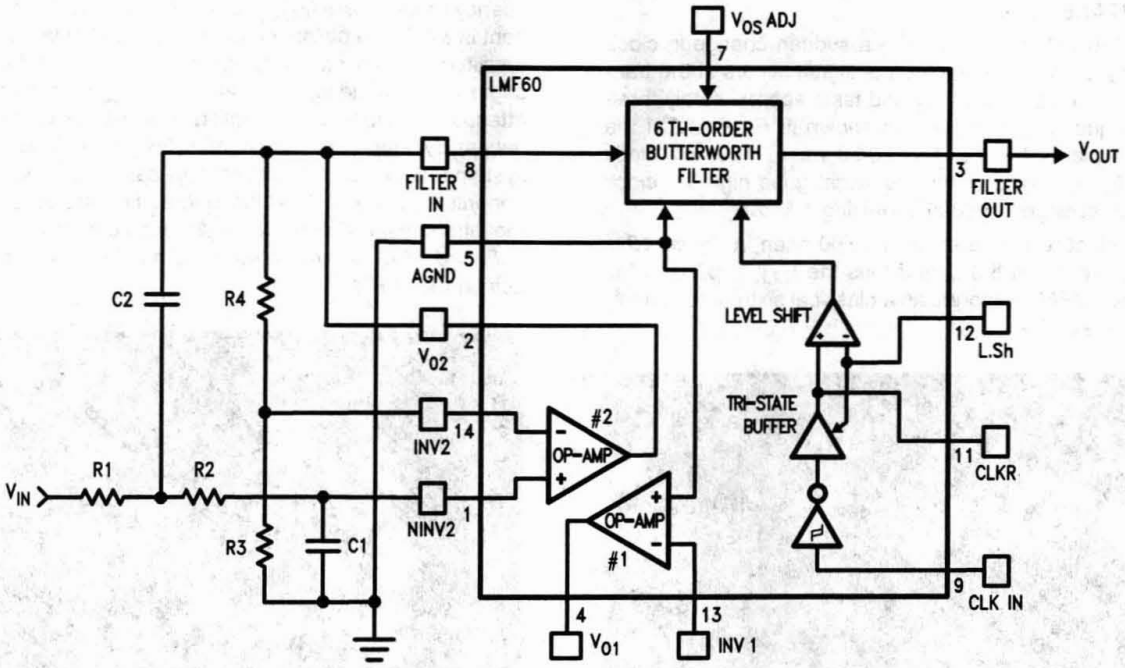
(b) Output Signal Spectrum. Note that the input signal at $f_s/2 + f$ causes an output signal to appear at $f_s/2 - f$.

FIGURE 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the LMF60, $f_s = f_{CLK}$.

2.0 Designing with the LMF60 (Continued)



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$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

$H_0 = R_4/R_3$ ($H_0 = 1$ when R_3 and R_4 are omitted and V_{O2} is directly tied to INV2).

Design Procedure:
pick C_1

$$R_2 = \frac{1}{2QC_1\omega_0}$$

for a 2nd Order Butterworth $Q = 0.707$

$$R_2 = \frac{0.113}{C_1f_0}$$

make $R_1 = R_2$
and

$$C_2 = \frac{1}{(2\pi f_0R_1)^2C_1}$$

Note: The parallel combination of R_4 (if used), R_1 and R_2 should be $\geq$ 10 kΩ in order not to load Op-Amp #2.

FIGURE 15. Second Order Butterworth Anti-Aliasing Filter Using Uncommitted Op-Amp #2

National Semiconductor

LMF90
4th-Order Elliptic Notch Filter

General Description

The LMF90 is a fourth-order elliptic notch (band-reject) filter based on switched-capacitor techniques. No external components are needed to define the response function. The depth of the notch is set using a two-level logic input, and the width is programmed using a three-level logic input. Two different notch depths and three different ratios of notch width to center frequency may be programmed by connecting these pins to V^+, ground, or V^-. Another three-level logic pin sets the ratio of clock frequency to notch frequency.

An internal crystal oscillator is provided. Used in conjunction with a low-cost color TV crystal and the internal clock frequency divider, a notch filter can be built with center frequency at 50 Hz, 60 Hz, 100 Hz, 120 Hz, 150 Hz, or 180 Hz for rejection of power line interference. Several LMF90s can be operated from a single crystal. An additional input is provided for an externally-generated clock signal.

Features

- Center frequency set by external clock or on-board clock oscillator
- No external components needed to set response characteristics
- Notch width, attenuation, and clock-to-center-frequency ratio independently programmable
- 14 pin 0.3″ wide package

Key Specifications

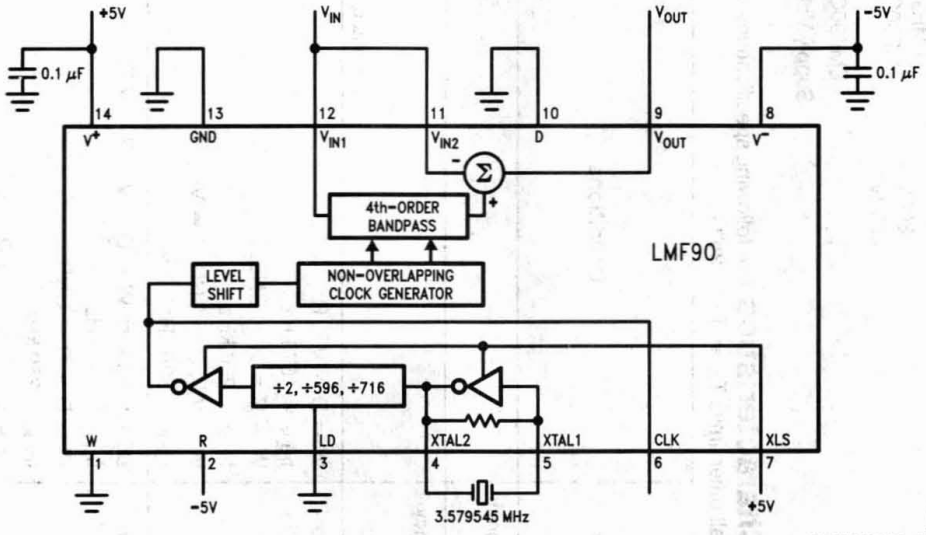
- f_0 Range 0.1 Hz to 30 kHz
- f_0 accuracy over full temperature range (max) 1.5%
- Supply voltage range ±2V to ±7.5V or 4V to 15V
- Passband Ripple (typ) 0.25 dB
- Attenuation at f_0 (typ) 39 dB or 48 dB (selectable)
- f_{CLK}: f_0 100:1, 50:1, or 33.3:1
- Notch Bandwidth (typ) 0.127 f_0, 0.26 f_0, or 0.55 f_0
- Output offset voltage (max) 120 mV

Applications

- Automatic test equipment
- Communications
- Power line interference rejection

Typical Connection

60 Hz Notch Filter



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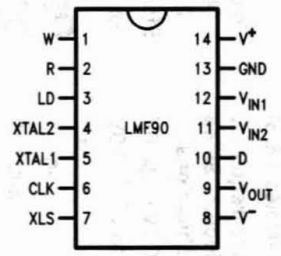
Connection Diagram

Dual-In-Line and Small Outline Packages



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Top View

Order Number LMF90CCN, LMF90CIWM, LMF90CCWM, LMF90CIJ, LMF90CCJ, LMF90CIN, LMF90CMJ or LMF90CMJ/883
See NS Package Number J14A, M14B or N14A

Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_S = V^+ - V^-$)	−0.3V to +16V
Voltage at any Input or Output	V^- −0.3V to V^+ +0.3V
Input Current at any Pin (Note 10)	5 mA
Package Input Current (Note 10)	20 mA
Power Dissipation (Note 5)	500 mW
ESD Susceptability (Note 6)	
Pin 9	1800V
All Other Pins	2000V
Soldering Information (Note 4)	
N Package (Soldering, 10 sec.)	260°C
J Package (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF90CCN, LMF90CCWM, LMF90CCJ	$0°C \le T_A \le +70°C$
LMF90CIJ, LMF90CIWM, LMF90CIN	$-40°C \le T_A \le +85°C$
LMF90CMJ, LMF90CMJ/883	$-55°C \le T_A \le +125°C$
Supply Voltage Range	4.0V to 15.0V

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
			Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
f_O	Center Frequency Range		0.1			0.1			Hz (Min)
				30	**30**		**30**		kHz (Max)
f_{CLK}	Clock Frequency Range	Pin 6	10			10			Hz (Min)
		Pin 6		1.5	**1.5**		**1.5**		MHz (Max)
		Pins 4 and 5		4.0	**4.0**		**4.0**		MHz (Max)
f_{CLK}/f_{O1}	Clock-to-Center-Frequency Ratio	W = D = V^-, R = V^+, f_{CLK} = 167 kHz		33.5 ±1%	**33.5 ±1.5%**		**33.5 ±1.5%**		(Max)
f_{CLK}/f_{O2}		W = D = R = GND, f_{CLK} = 250 kHz		50.25 ±1%	**50.25 ±1.5%**		**50.25 ±1.5%**		(Max)
f_{CLK}/f_{O3}		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz		100.5 ±1%	**100.5 ±1.5%**		**100.5 ±1.5%**		(Max)
H_{ON}	Passband Gain	DC and 20 kHz, W = D = V^-, R = V^+, f_{CLK} = 167 kHz	0	±0.2	**±0.2**	0	**±0.2**		dB (Max)
		W = D = R = GND, f_{CLK} = 250 kHz	0	±0.2	**±0.2**	0	**±0.2**		dB (Max)
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz	0	±0.2	**±0.2**	0	**±0.2**		dB (Max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
			Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
PBW	Ratio of Passband Width to Center Frequency	W = D = V^-, R = V^+, f_{CLK} = 167 kHz		0.1275 ±0.0175	**0.1275 ±0.0175**		**0.1275 ±0.0175**		(Max)
		W = D = R = GND, f_{CLK} = 250 kHz		0.265 ±0.025	**0.265 ±0.025**		**0.265 ±0.025**		(Max)
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz		0.550 ±0.05	**0.550 ±0.05**		**0.550 ±0.05**		(Max)
$A_{Min1}@f_{O1}$	Gain at Center Frequency	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	−39	−30	**−30**	−39	**−30**		dB (Max)
$A_{Min2}@f_{O2}$		W = D = R = GND, f_{CLK} = 250 kHz	−48	−36.5	**−36.5**	−48	**−36.5**		dB (Max)
$A_{Min3}@f_{O3}$		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz	−48	−36.5	**−36.5**	−48	**−36.5**		dB (Max)
	Additional Center Frequency Gain Tests at f_{O1}	W = GND, D = V^-, R = V^+, f_{CLK} = 167 kHz	−36	−30	**−30**	−36	**−30**		dB (Max)
		W = V^+, D = V^-, R = V^+, f_{CLK} = 167 kHz	−36	−30	**−30**	−36	**−30**		dB (Max)
		W = V^-, D = GND, R = V^+, f_{CLK} = 167 kHz	−42	−30	**−30**	−42	**−30**		dB (Max)
		W = D = GND, R = V^+, f_{CLK} = 167 kHz	−48	−35	**−35**	−48	**−35**		dB (Max)
		W = V^+, D = GND,R = V^+, f_{CLK} = 167 kHz	−48	−35	**−35**	−48	**−35**		dB (Max)

AC Electrical Characteristics The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions		LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
				Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
	Additional Center Frequency Gain Tests at f_{O2}	$W = V^-, D = V^-, R = GND, f_{CLK} = 250$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = GND, D = V^-, R = GND, f_{CLK} = 250$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^+, D = V^-, R = GND, f_{CLK} = 250$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^-, D = R = GND, f_{CLK} = 250$ kHz		−42	−30	**−30**	−42	**−30**		dB (Max)
		$W = V^+, D = R = GND, f_{CLK} = 250$ kHz		−48	−35	**−35**	−48	**−35**		dB (Max)
	Additional Center Frequency Gain Tests at f_{O3}	$W = D = R = V^-, f_{CLK} = 500$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = GND, D = V^-, R = V^-, f_{CLK} = 500$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^+, D = V^-, R = V^-, f_{CLK} = 500$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^-, D = GND, R = V^-, f_{CLK} = 500$ kHz		−42	−30	**−30**	−42	**−30**		dB (Max)
		$W = D = GND, R = V^-, f_{CLK} = 500$ kHz		−48	−35	**−35**	−48	**−35**		dB (Max)
A_{3a}	Gain at $f_3 = 0.995\ f_{O1}$	$W = D = V^-, R = V^+, f_{CLK} = 167$ kHz		−41	−30	**−30**	−41	**−30**		dB (Max)
A_{4a}	Gain at $f_4 = 1.005\ f_{O1}$			−41	−30	**−30**	−41	**−30**		dB (Max)
A_{3b}	Gain at $f_3 = 0.992\ f_{O2}$	$W = D = R = GND, f_{CLK} = 250$ kHz		−40	−35	**−35**	−40	**−35**		dB (Max)
A_{4b}	Gain at $f_4 = 1.008\ f_{O2}$			−40	−35	**−35**	−40	**−35**		dB (Max)
A_{3c}	Gain at $f_3 = 0.982\ f_{O3}$	$W = V^+, D = GND, R = V^-, f_{CLK} = 500$ kHz		−41	−35	**−35**	−41	**−35**		dB (Max)
A_{4c}	Gain at $f_4 = 1.018\ f_{O3}$			−41	−35	**−35**	−41	**−35**		dB (Max)
A_{max1}	Passband Ripple	$W = D = V^-, R = V^+, f_{CLK} = 167$ kHz	$f_5 = 0.914\ f_{O1}$	0.25	0.9	**0.9**	0.25	**0.9**		dB (Max)
				0.25	0	**0**	0.25	**0**		dB (Min)
			$f_6 = 1.094\ f_{O1}$	0.25	0.9	**0.9**	0.25	**0.9**		dB (Max)
				0.25	0	**0**	0.25	**0**		dB (Min)

AC Electrical Characteristics The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions		LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
				Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
A_{Max2}	Passband Ripple	W = D = R = GND, f_{CLK} = 250 kHz	$f_5 = 0.830\ f_{O2}$	0.25 0.25	0.9 0	**0.9** **0**	0.26 0.25	**0.9** **0**		dB (Max) dB (Min)
			$f_6 = 1.205\ f_{O2}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
A_{Max3}	Passband Ripple	W = V^+, D = GND, R = V^- f_{CLK} = 500 kHz	$f_5 = 0.700\ f_{O3}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
			$f_6 = 1.428\ f_{O3}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
E_n	Output Noise	20 kHz Bandwidth W = D = V^-, R = V^+, f_{CLK} = 167 kHz W = D = R = GND, f_{CLK} = 250 kHz W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz		670 370 250			670 370 250			μVrms μVrms μVrms
	Clock Feedthrough			50			50			mVp–p
GBW	Output Buffer Gain Bandwidth			1			1			MHz
SR	Output Buffer Slew Rate			3			3			V/μs
C_L	Maximum Capacitive Load			200			200			pF

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface Limits Apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
			Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
I_S	Power Supply Current	f_{CLK} = 500 kHz, $V_{IN1} = V_{IN2}$ = GND	2.35	5.0	**5.0**	2.35	**5.0**		mA (Max)
V_{OS}	Output Offset Voltage	W = D = V^-, R = V^+, f_{CLK} = 167 kHz W = D = R = GND, f_{CLK} = 250 kHz W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz	±50 ±60 ±80	±120 ±140 ±170	**±120** **±140** **±170**	±50 ±60 ±80	**±120** **±140** **±170**		mV (Max) mV (Max) mV (Max)
V_{OUT}	Output Voltage Swing	R_L = 5 kΩ	+4.2, −4.7	±4.0	**±4.0**	+4.2, −4.7	**±4.0**		V (Min)
V_{I1}	Logical "Low" Input Voltage	Pins 1, 2, 3, 7, and 10		−4.0	**−4.0**		**−4.0**		V (Max)
V_{I2}	Logical "GND" Input Voltage	Pins 1, 2, 3, 7, and 10		+1.0 −1.0	**+1.0** **−1.0**		**+1.0** **−1.0**		V (Max) V (Min)
V_{I3}	Logical "High" Input Voltage	Pins 1, 2, 3, and 7		+4.0	**+4.0**		**+4.0**		V (Min)
I_{IN}	Input Current	Pins 1, 2, 3, 7, and 10		±10	**±10**		**±10**		μA (Max)
V_{IL}	Logical "0" Input Voltage, Pins 5 and 6	Pin 5, XLS = V^+ or Pin 6, XLS = GND		−4.0	**−4.0**		**−4.0**		V (Max)
V_{IH}	Logical "1" Input Voltage, Pins 5 and 6			+4.0	**+4.0**		**+4.0**		V(Min)
V_{IL}	Logical "0" Input Voltage, Pin 6	$V^+ - V^-$ = 10V, XLS = V^- or V^+ = +5V, V^- = 0V, XLS = +2.5V		+0.8	**+0.8**		**+0.8**		V (Max)
V_{IH}	Logical "1" Input Voltage, Pin 6			+2.0	**+2.0**		**+2.0**		V (Min)
V_{OL}	Logical "0" Output Voltage, Pin 6	XLS = V^+, $\|I_{OUT}\|$ = 4 mA		−4.0	**−4.0**		**−4.0**		V (Max)
V_{OH}	Logical "1" Output Voltage, Pin 6			+4.0	**+4.0**		**+4.0**		V (Min)

DC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND unless otherwise specified.

Note 4: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any current Linear Data Book for other methods of soldering surface mount devices.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 150°C$, and the typical thermal resistance (Θ_{JA}) when board mounted is 61°C/W for the LMF90CCN and CIN, 134°C/W for the LMF90CCWM and CWIM and 59°C/W for the LMF90CCJ, CIJ and CMJ.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

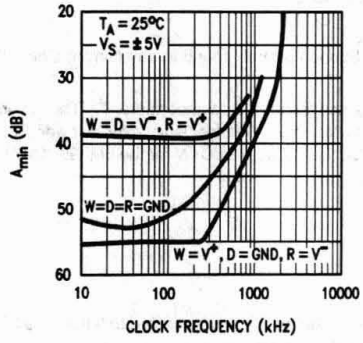
Note 8: Tested Limits are guaranteed and 100% tested.

Note 9: Design Limits are guaranteed, but not 100% tested.

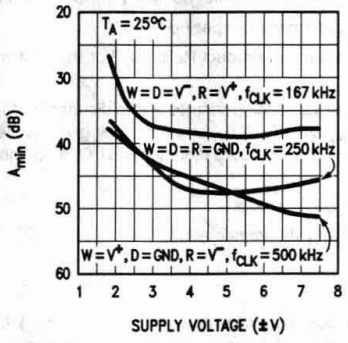
Note 10: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > V^+$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Typical Performance Characteristics

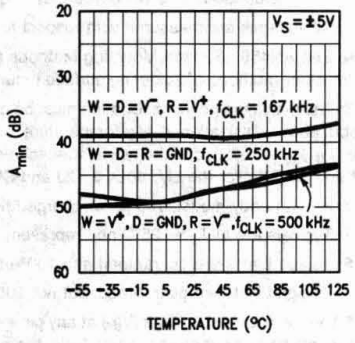
Notch Depth vs Clock Frequency



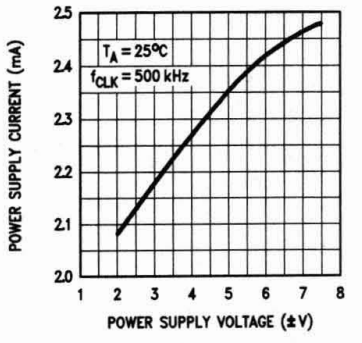
Notch Depth vs Supply Voltage



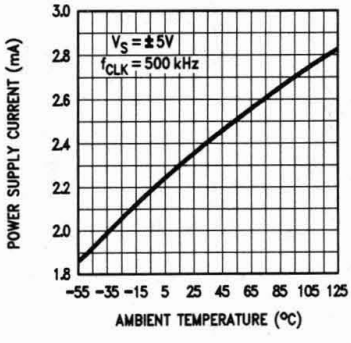
Notch Depth vs Temperature



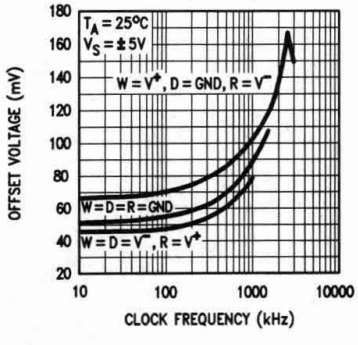
Power Supply Current vs Power Supply Voltage



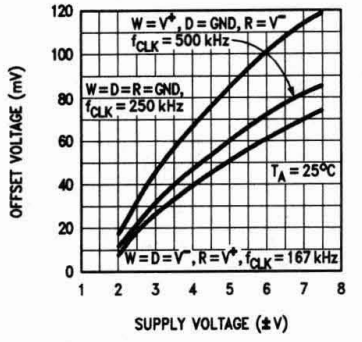
Power Supply Current vs Temperature



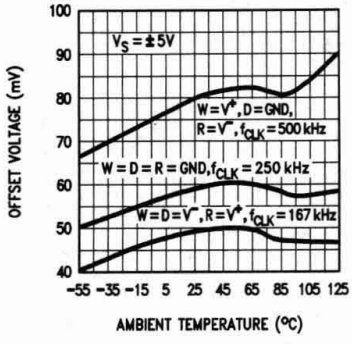
Offset Voltage vs Clock Frequency



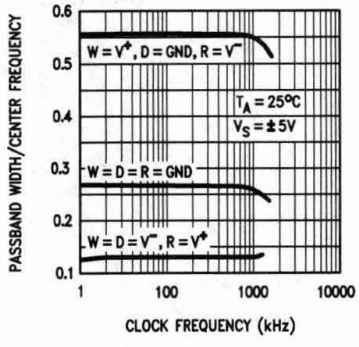
Offset Voltage vs Supply Voltage



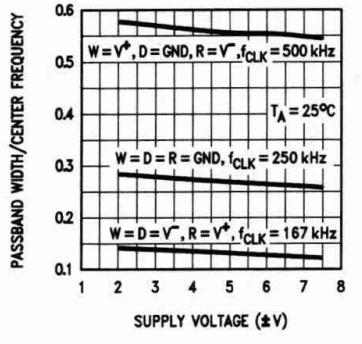
Offset Voltage vs Temperature



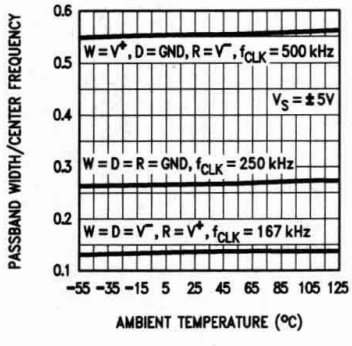
Passband Width vs Clock Frequency



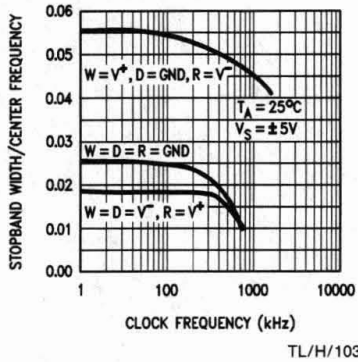
Passband Width vs Supply Voltage



Passband Width vs Temperature


$W = V^+, D = GND, R = V^-, f_{CLK} = 500$ kHz
$V_S = \pm 5V$
$W = D = R = GND, f_{CLK} = 250$ kHz
$W = D = V^-, R = V^+, f_{CLK} = 167$ kHz
PASSBAND WIDTH/CENTER FREQUENCY
AMBIENT TEMPERATURE (°C)

Stopband Width vs Clock Frequency



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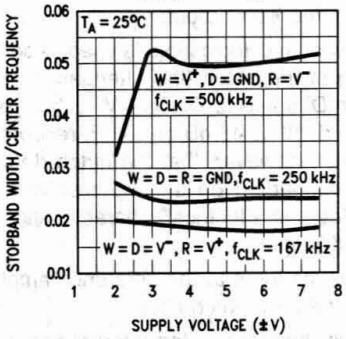
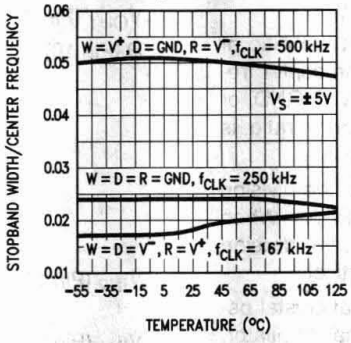
Typical Performance Characteristics (Continued)

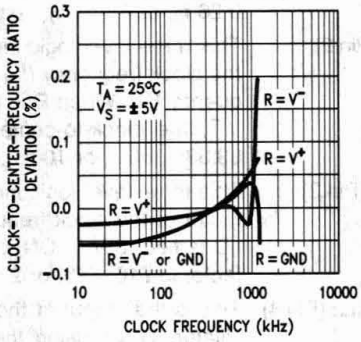
Stopband Width vs Supply Voltage



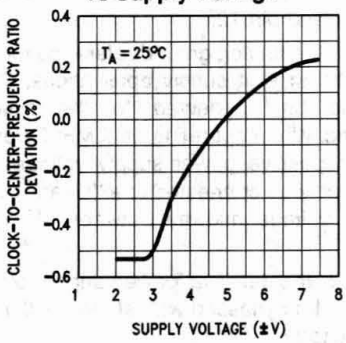
Stopband Width vs Temperature



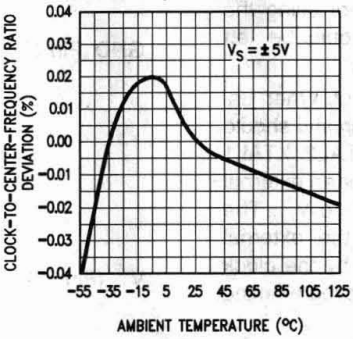
Clock-to-Center-Frequency Ratio Deviation vs Clock Frequency



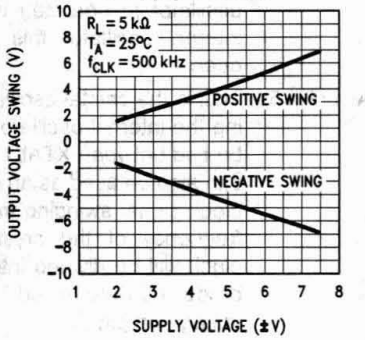
Clock-to-Center-Frequency Ratio Deviation vs Supply Voltage



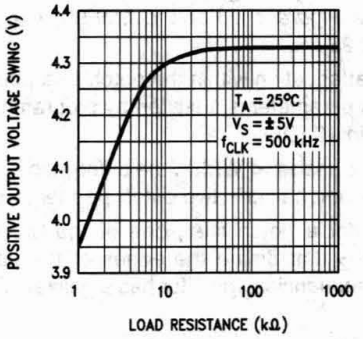
Clock-to-Center-Frequency Ratio Deviation vs Temperature



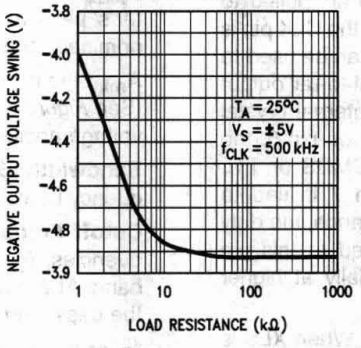
Output Swing vs Supply Voltage



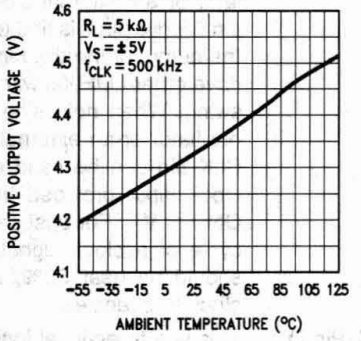
Positive Output Voltage Swing vs Load Resistance



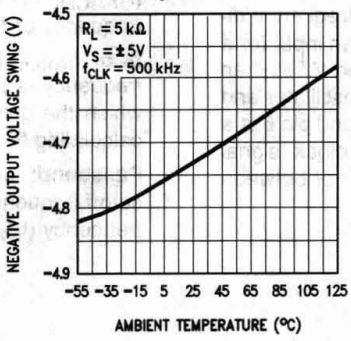
Negative Output Voltage Swing vs Load Resistance



Positive Output Swing vs Temperature



Negative Output Swing vs Temperature



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Pin Descriptions

W (Pin 1) This three-level logic input sets the width of the notch. Notch width is $f_{c2}-f_{c1}$ (see *Figure 1*). When W is tied to V^+ (pin 14), GND (pin 13), or V^- (pin 8), the notch width is 0.55 f_0, 0.26 f_0, or 0.127 f_0, respectively.

R (Pin 2) This three-level logic input sets the ratio of the clock frequency (f_{CLK}) to the center frequency (f_0). When R is tied to V^+, GND, or V^-, the clock-to-center-frequency ratio is 33.33:1, 50:1, or 100:1, respectively.

LD (Pin 3) This three-level logic input sets the division factor of the clock frequency divider. When LD is tied to V^+, GND, or V^-, the division factor is 716, 596, or 2, respectively.

XTAL2 (Pin 4) This is the output of the internal crystal oscillator. When using the internal oscillator, the crystal should be tied between XTAL2 and XTAL1. (The capacitors are internal—no external capacitors are needed for the oscillator to operate.) When not using the internal oscillator this pin should be left open.

XTAL1 (Pin 5) This is the crystal oscillator input. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2. XTAL1 can also be used as an input for an external clock signal swinging from V^+ to V^-. The frequency of the crystal or the external clock will be divided internally by the clock divider as determined by the programming voltage on pin 3.

CLK (Pin 6) This is the filter clock pin. The clock signal appearing on this pin is the filter clock (f_{CLK}). When using the internal crystal oscillator or an external clock signal applied to pin 5 while pin 7 is tied to V^+, the CLK pin is the output of the divider and can be used to drive other LMF90s with its rail-to-rail output swing. When not using the internal crystal oscillator or an external clock on pin 5, the CLK pin can be used as a CMOS or TTL clock input provided that pin 7 is tied to GND or V^-. For best performance, the duty cycle of a clock signal applied to this pin should be near 50%, especially at higher clock frequencies.

XLS (Pin 7) This is a three-level logic pin. When XLS is tied to V^+, the crystal oscillator and frequency divider are enabled and CLK (pin 6) is an output. When XLS is tied to GND (pin 13), the crystal oscillator and frequency divider are disabled and pin 6 is an input for a clock swinging between V^- and V^+. When XLS is tied to V^-, the crystal oscillator and frequency divider are disabled and pin 6 is a TTL level clock input for a clock signal swinging between GND and V^+ or between V^- and GND.

V^- (Pin 8) This is the negative power supply pin. It should be bypassed with at least a 0.1 μF capacitor. For single-supply operation, connect this pin to system ground.

V_{OUT} (Pin 9) This is the filter output.

D (Pin 10) This two-level logic input is used to set the depth of the notch (the attenuation at f_0). When D is tied to GND or V^-, the typical notch depth is 48 dB or 39 dB, respectively. Note, however, that the notch depth is also dependent on the width setting (pin 1). See the Electrical Characteristics for tested limits.

V_{IN2} (Pin 11) This is the input to the difference amplifier section of the notch filter.

V_{IN1} (Pin 12) This is the input to the internal bandpass filter. This pin is normally connected to pin 11. For wide bandwidth applications, an anti-aliasing filter can be inserted between pin 11 and pin 12.

GND (Pin 13) This is the analog ground reference for the LMF90. In split supply applications, GND should be connected to the system ground. When operating the LMF90 from a single positive power supply voltage, pin 13 should be connected to a "clean" reference voltage midway between V^+ and V^-.

V^+ (Pin 14) This is the positive power supply pin. It should be bypassed with at least a 0.1 μF capacitor.

1.0 Definition of Terms

A_{max}: the maximum amount of gain variation within the filter's passband (See *Figure 1*). For the LMF90, A_{Max} is nominally equal to 0.25 dB.

A_{min}: the minimum attenuation within the notch's stopband. (See *Figure 1*). This parameter is adjusted by programming voltage applied to pin 10 (D).

Bandwidth (BW) or Passband Width: the difference in frequency between the notch filter's two cutoff frequencies.

Cutoff Frequency: for a notch filter, one of the two frequencies, f_{C1} and f_{C2} that define the edges of the passband. At these two frequencies, the filter has a gain equal to the passband gain.

f_{CLK}: the frequency of the clock signal that appears at the CLK pin. This frequency determines the filter's center frequency. Depending on the programming voltage on pin 2 (R), f_{CLK} will be either 33.33, 50, or 100 times the center frequency of the notch.

f_0 or f_{Notch}: the center frequency of the notch filter. This frequency is measured by finding the two frequencies for which the gain −3 dB relative to the passband gain, and calculating their geometrical mean.

Passband: for a notch filter, frequencies above the upper cutoff frequency (f_{C2} in *Figure 1*) and below the lower cutoff frequency (f_{C1} in *Figure 1*).

1.0 Definition of Terms (Continued)

Passband Gain: the notch filter's gain for signal frequencies near dc or $f_{CLK}/2$. The passband gain of a notch filter is also called "H_{ON}". For the LMF90, the passband gain is nominally 0 dB.

Passband Ripple: the variation in gain within the filter's passband.

Stopband: for a notch filter, the range of frequencies for which the attenuation is at least A_{min} (f_{S1} to f_{S2}) in *Figure 1*).

Stop Frequency: one of the two frequencies (f_{S1} and f_{S2}) at the edges of the notch's stopband.

Stopband Width (SBW): the difference in frequency between the two stopband edges ($f_{S2}-f_{S1}$).

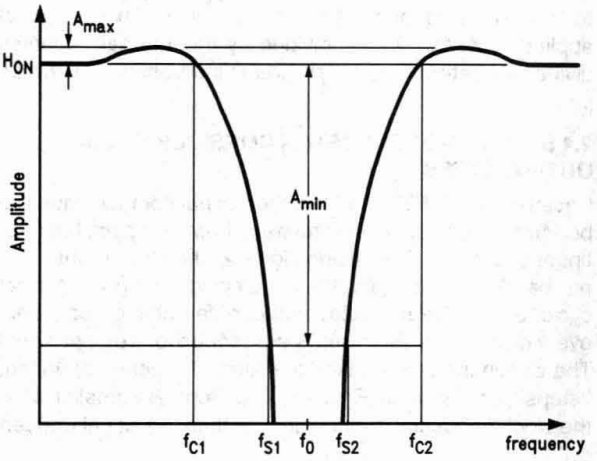

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FIGURE 1. General Form of Notch Response

2.0 Applications Information

2.1 FUNCTIONAL DESCRIPTION

The LMF90 uses switched-capacitor techniques to realize a fourth-order elliptic notch transfer function with 0.25 dB passband ripple. No external components other than supply bypass capacitors and a clock (or crystal) are required.

As is evident from the block diagram, the analog signal path consists of a fourth-order bandpass filter and a summing amplifier. The analog input signal is applied to the input of the bandpass filter, and to one of the summing amplifier inputs. The bandpass filter's output drives the other summing amplifier input. The output of the summing amplifier is the difference between the input signal and the bandpass output, and has a notch filter characteristic. Notch width and depth are controlled by the dc programming voltages applied to two pins (1 and 10), and the center frequency is proportional to the clock frequency, which may be generated externally or internally with the aid of an external crystal. The clock-to-center-frequency ratio can be one of three different values, and is selected by the voltage on a three-level logic input (pin 2).

The clock signal passes through a digital frequency divider circuit that can divide the clock frequency by any of three different factors before it reaches the filters. This divider can also be disabled, if desired. Pin 7 enables and disables the frequency divider and also configures the clock inputs for operation with an external CMOS or TTL clock or with the internal oscillator circuit.

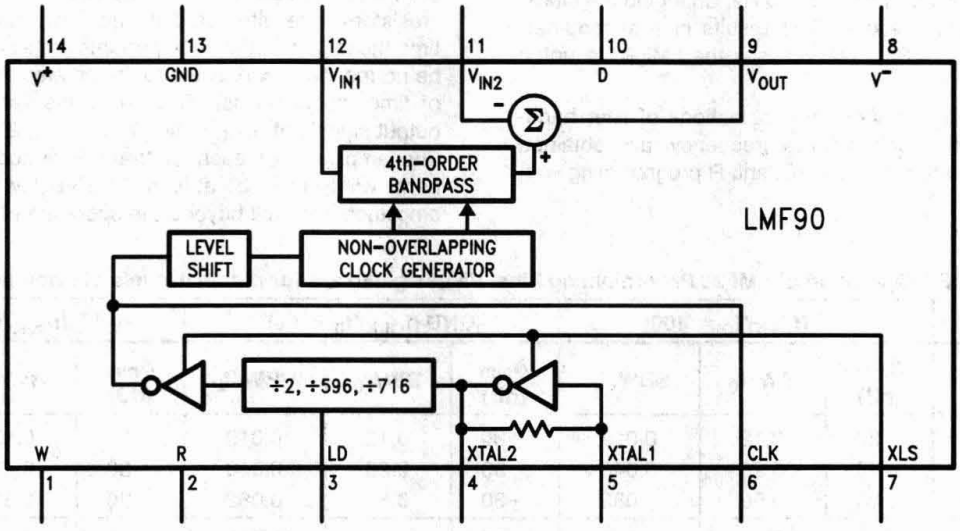

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FIGURE 2. LMF90 Block Diagram

2.0 Applications Information (Continued)

2.2 PROGRAMMING PINS

The LMF90 has five control pins that are used to program the filter's characteristics via a three-level logic scheme. In dual-supply applications, these inputs are tied to either V^+, V^-, or GND in order to select a particular set of characteristics. For example, the W input (pin 1) sets the filter's passband width to 0.55 f_0, 0.26 f_0 or 0.127 f_0 when the W input is connected to V^+, GND, or V^-, respectively. Applying V^- and GND to the D input (pin 10) will set the notch depth to 40 dB or 30 dB, respectively.

The R input (pin 2) is another three-level logic input, and it sets the clock-to-center-frequency ratio to 33.33:1, 50:1, or 100:1 for input voltages equal to V^+, GND, or V^-, respectively. Note that the clock frequency referred to here is the frequency at the CLK pin and at the frequency divider output (if used). This is different from the frequency at the divider's input. LD (pin 3) sets the frequency divider's division factor to either 716, 596, or 2 for input voltages equal to V^+, GND, or V^-, respectively. XLS (pin 7) enables and disables the crystal oscillator and clock divider. When XLS is connected to the positive supply, the oscillator and divider are enabled, and CLK is the output of the divider and can drive the clock inputs of other LMF90s. When XLS is connected to GND, the oscillator and divider are disabled, and the CLK pin becomes a clock input for CMOS-level signals. Connecting XLS to the negative supply disables the oscillator and divider and causes CLK to operate as a TTL-level clock input.

Using an external 3.579545 MHz color television crystal with the internal oscillator and divider, it is possible to build a power line frequency notch for 50 Hz or 60 Hz line frequencies or their second and third harmonics using the LMF90. A 60 Hz notch is shown in the Typical Application circuit on the first page of this data sheet. Connecting LD to V^+ changes the notch frequency to 50 Hz. Changing the clock-to-center-frequency ratio to 50:1 results in a second-harmonic notch, and a 33:1 ratio causes the LMF90 to notch the third harmonic.

Table I illustrates 18 different combinations of filter bandwidth, depth, and clock-to-center-frequency ratio obtained by choosing the appropriate W, D, and R programming voltages.

2.3 DIGITAL INPUTS AND OUTPUTS

As mentioned above, the CLK pin can serve as either an input or an output, depending on the programming voltage on XLS. When CLK is operating as a TTL input, it will operate properly in both dual-supply and single-supply applications, because it has two logic thresholds—one referred to V^-, and one referred to GND. When operating as an output, CLK swings rail-to-rail (CMOS logic levels).

XTAL1 and XTAL2 are the input and output pins for the internal crystal oscillator. When using the internal oscillator (XLS connected to V^+), the crystal is connected between these two pins. When the internal oscillator is not used, XTAL2 should be left open. XTAL1 can be used as an input for an external CMOS-level clock signal swinging from V^- to V^+. The frequency of the crystal or the external clock applied to XTAL1 will be divided by the internal frequency divider as determined by programming voltage on the LD pin.

2.4 SAMPLED-DATA SYSTEM CONSIDERATIONS OUTPUT STEPS

Because the LMF90 uses switched-capacitor techniques, its performance differs in several ways from non-sampled (continuous) circuits. The analog signal at the input to the internal bandpass filter (pin 12) is sampled during each clock cycle, and, since the output voltage can change only once every clock cycle, the result is a discontinuous output signal. The bandpass output takes the form of a series of voltage "steps", as shown in *Figure 3*. The steps are smaller when the clock frequency is much greater than the signal frequency.

Switched-capacitor techniques are used to set the summing amplifier's gain. Its input and feedback "resistors" are actually made from switches and capacitors. Two sets of these "resistors" are alternated during each clock cycle. Each time these gain-setting components are switched, there will be no feedback connected to the op amp for a short period of time (about 50 ns). This generates very low-amplitude output signals at $f_{CLK} + f_{IN}$, $f_{CLK} - f_{IN}$, $2\,f_{CLK} + f_{IN}$, etc. The amplitude of each of these intermodulation components will typically be at least 70 dB below the input signal amplitude and well beyond the spectrum of interest.

TABLE I. Operation of LMF90 Programming Pins. Values given are for nominal levels of attenuation.

R		V^- (f_{CLK}/f_0 = 100)			GND (f_{CLK}/f_0 = 50)			V^+ (f_{CLK}/f_0 = 33.33)		
D	W	A_{min} (dB)	BW/f_0	SBW/f_0	A_{min} (dB)	BW/f_0	SBW/f_0	A_{min} (dB)	BW/f_0	SBW/f_0
V^-	V^-	−30	0.12	0.019	−30	0.12	0.019	−30	0.12	0.019
	GND	−30	0.26	0.040	−30	0.26	0.040	−30	0.26	0.040
	V^+	−30	0.55	0.082	−30	0.55	0.082	−30	0.55	0.082
GND	V^-	−35	0.12	0.010	−35	0.12	0.010	−35	0.12	0.010
	GND	−40	0.26	0.024	−40	0.26	0.024	−40	0.26	0.024
	V^+	−40	0.55	0.050	−40	0.55	0.050	−40	0.55	0.050

2.0 Applications Information (Continued)

ALIASING

Another important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The LMF90's sampling frequency is the same as the filter's clock frequency. This is the frequency at the CLK pin). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_S/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_S/2 - 10$ Hz. This phenomenon is known as "aliasing". Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_S/2$.

In some cases, it may be necessary to use a bandwidth limiting filter (often a simple passive RC low-pass) ahead of the bandpass input. Although the summing amplifier uses switched-capacitor techniques, it does not exhibit aliasing behavior, and the anti-aliasing filter need not be in its input signal path. The filter can be placed ahead of pin 12 as shown in *Figure 4*, with the non-band limited input signal applied to pin 11. The output spectrum will therefore be wideband, although limited by the bandwidth of the summing amplifier's output buffer amplifier (typically 1 MHz), even if f_{CLK} is less than 1 MHz. Phase shift in the anti-aliasing filter will affect the accuracy of the notch transfer function, however, so it is best to use the highest available clock-to-center-frequency ratio (100:1) and set the RC filter cutoff frequency to about 15 to 20 times the notch frequency. This will provide reasonable attenuation of high-frequency input signals, while avoiding degradation of the overall notch response. If the anti-aliasing filter's cutoff frequency is too low, it will introduce phase shift and gain errors large enough to shift the frequency of the notch and reduce its depth. A cutoff frequency that is too high may not provide sufficient attenuation of unwanted high-frequency signals.

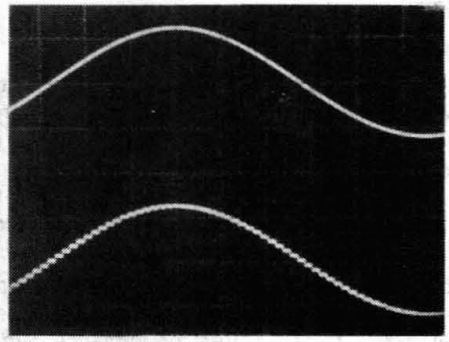

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FIGURE 3. Output waveform of a switched-capacitor filter. Note the voltage steps caused by sampling at the clock frequency.

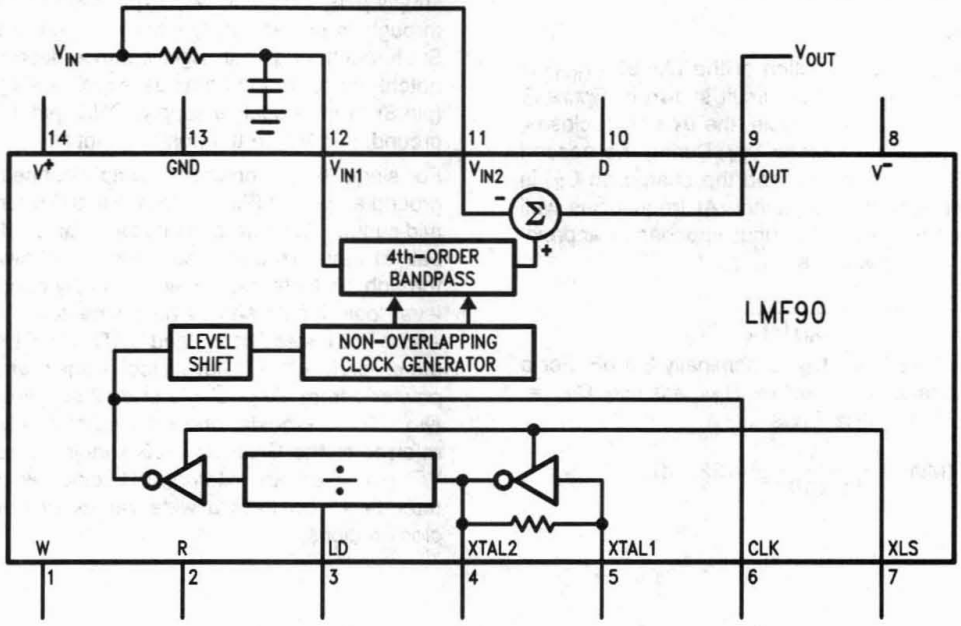

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FIGURE 4. Using a simple passive low-pass filter to prevent aliasing in the presence of high-frequency input signals.

2.0 Applications Information (Continued)

NOISE

Switched-capacitor filters have two kinds of noise at their outputs. There is a random, "thermal" noise component whose level is typically on the order of hundreds of microvolts. The other kind of noise is digital clock feedthrough. This will have an amplitude in the vicinity of 50 mV peak-to-peak. In some applications, the clock noise frequency is so high compared to the signal frequency that it is unimportant. In other cases, clock noise may have to be removed from the output signal with, for example, a passive low-pass filter at the LMF90's output pin.

CLOCK FREQUENCY LIMITATIONS

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the time between clock cycles is relatively long, and small parasitic leakage currents cause the internal capacitors to discharge sufficiently to affect the filter's offset voltage and gain. This effect becomes more pronounced at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal operational amplifiers to settle. Best performance with high clock frequencies will be obtained when the filter clock's duty cycle is 50%. The clock frequency divider, when used, provides a 50% duty cycle clock to the filter, but when an external clock is applied to CLK, it should have a duty cycle close to 50% for best performance.

Input Impedance

The input to the bandpass section of the LMF90 (V_{IN1}) is similar to the switched-capacitor circuit shown in *Figure 5*. During the first half of a clock cycle, the θ_1 switch closes, charging C_{IN} to the input voltage V_{IN}. During the second half-cycle, the θ_2 switch closes, and the charge on C_{IN} is transferred to the feedback capacitor. At frequencies well below the clock frequency, the input impedance approximates a resistor whose value is

$$R_{IN} = \frac{1}{C_{IN}\, f_{CLK}}.$$

At the bandpass filter input, C_{IN} is nominally 3.0 pF. For a worst-case calculation of effective R_{IN}, assume C_{IN} = 3.0 pF and f_{CLK} = 1.5 MHz. Thus,

$$R_{IN}\,(\text{Min}) = \frac{1}{4.5 \times 10^{-6}} = 222\ \text{k}\Omega.$$

At the maximum clock frequency of 1.5 MHz, the lowest typical value for the effective R_{IN} at the V_{IN1} input is therefore 222 kΩ. Note that R_{IN} increases as f_{CLK} decreases, so the input impedance will be greater than or equal to this value. Source impedance should be low enough that this input impedance doesn't significantly affect gain.

The summing amplifier input impedance at V_{IN2} is calculated in a similar manner, except that C_{IN} = 5.0 pF. This yields a minimum input impedance of 133 kΩ at V_{IN2}. When both inputs are connected together, the combined input impedance will be 83.3 kΩ with a 1.5 MHz filter clock.

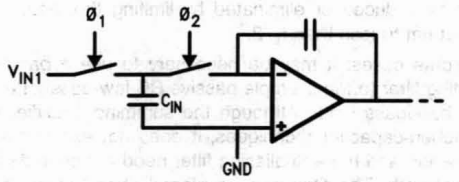

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FIGURE 5. Simplified LMF90 bandpass section input stage. At frequencies well below the center frequency, the input impedance appears to be resistive.

2.5 POWER SUPPLY AND CLOCK OPTIONS

The LMF90 is designed to operate from either single or dual power supply voltages from 5V to 15V. In either case, the supply pins should be well-bypassed to minimize any feedthrough of power supply noise into the filter's signal path. Such feedthrough can significantly reduce the depth of the notch. For operation from dual supply voltages, connect V^- (pin 8) to the negative supply, GND (pin 13) to the system ground, and V^+ to the positive supply.

For single supply operation, simply connect V^- to system ground and GND (Pin 13) to a "clean" reference voltage at mid-supply. This reference voltage can be developed with a pair of resistors and a capacitor as shown in *Figures 10* through *16*. Note that for single supply operation, the three-level logic inputs should be connected to system ground and $V^+/2$ instead of V^- and GND. The CLK input will operate properly with TTL-level clock signals when the LMF90 is powered from either single or dual supplies because it has two TTL thresholds, one referred to the V^- pin and one referred to the GND pin. XLS should be connected to the V^- pin when an external TTL clock is used. *Figures 6* through *16* illustrate a wide variety of power supply and clock options.

2.0 Applications Information (Continued)

DUAL-SUPPLY CLOCK OPTIONS

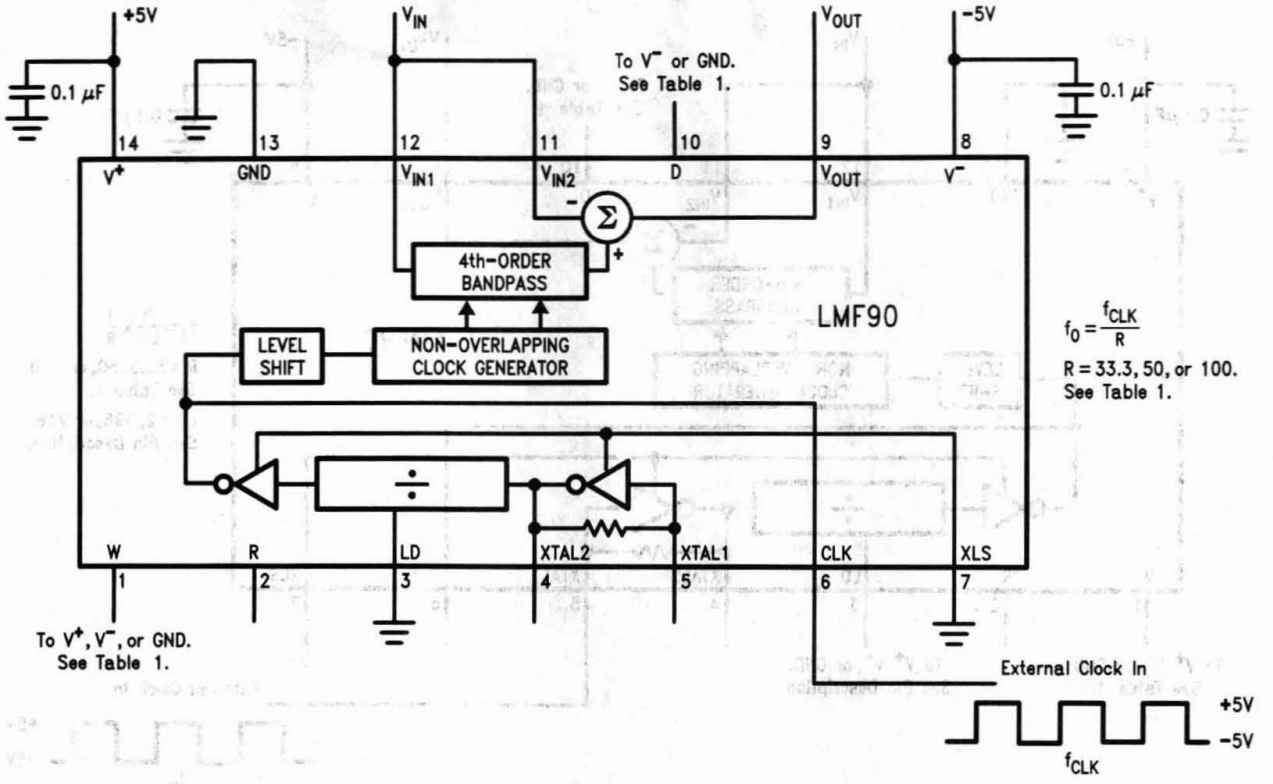

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FIGURE 6. Dual supply; external CMOS-level clock. Internal frequency divider disabled.

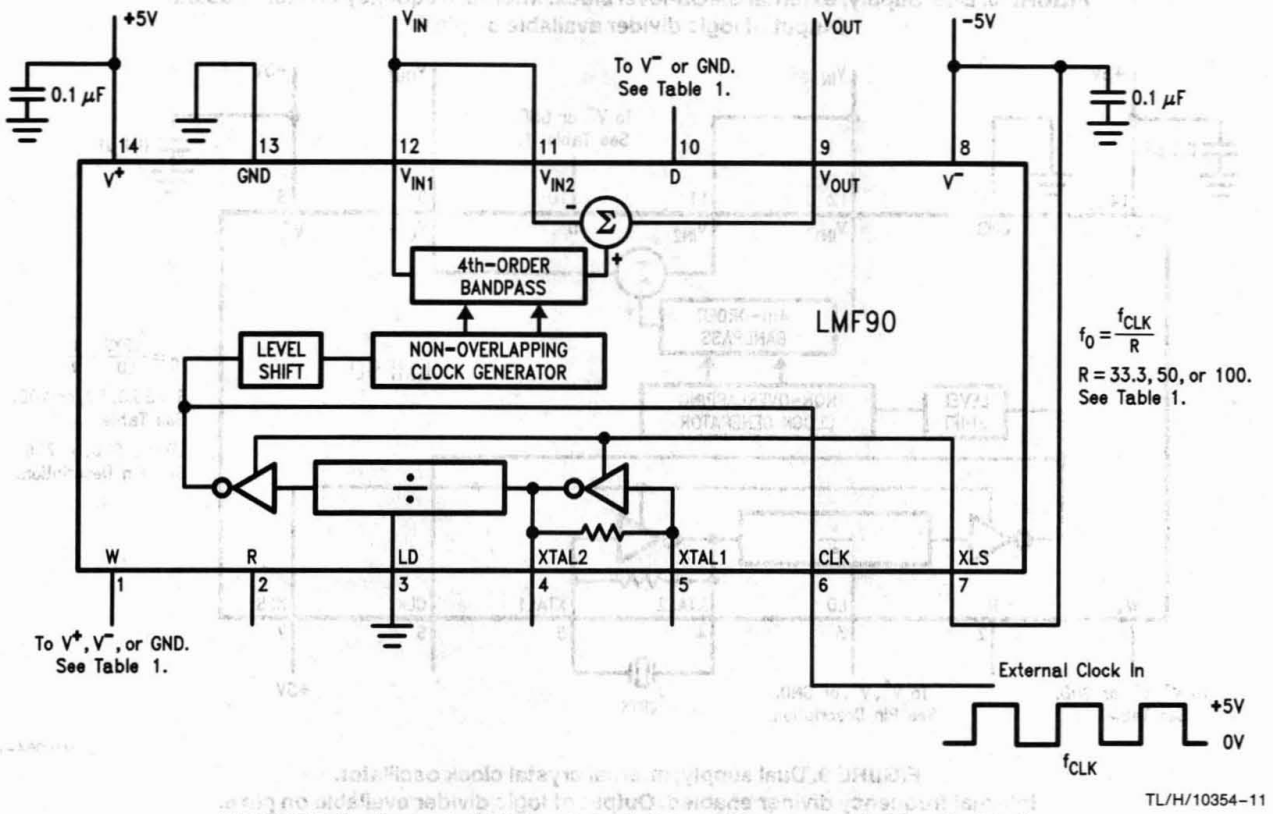

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FIGURE 7. Dual supply; TTL-level clock. Internal frequency divider disabled.

2.0 Applications Information (Continued)

DUAL-SUPPLY CLOCK OPTIONS

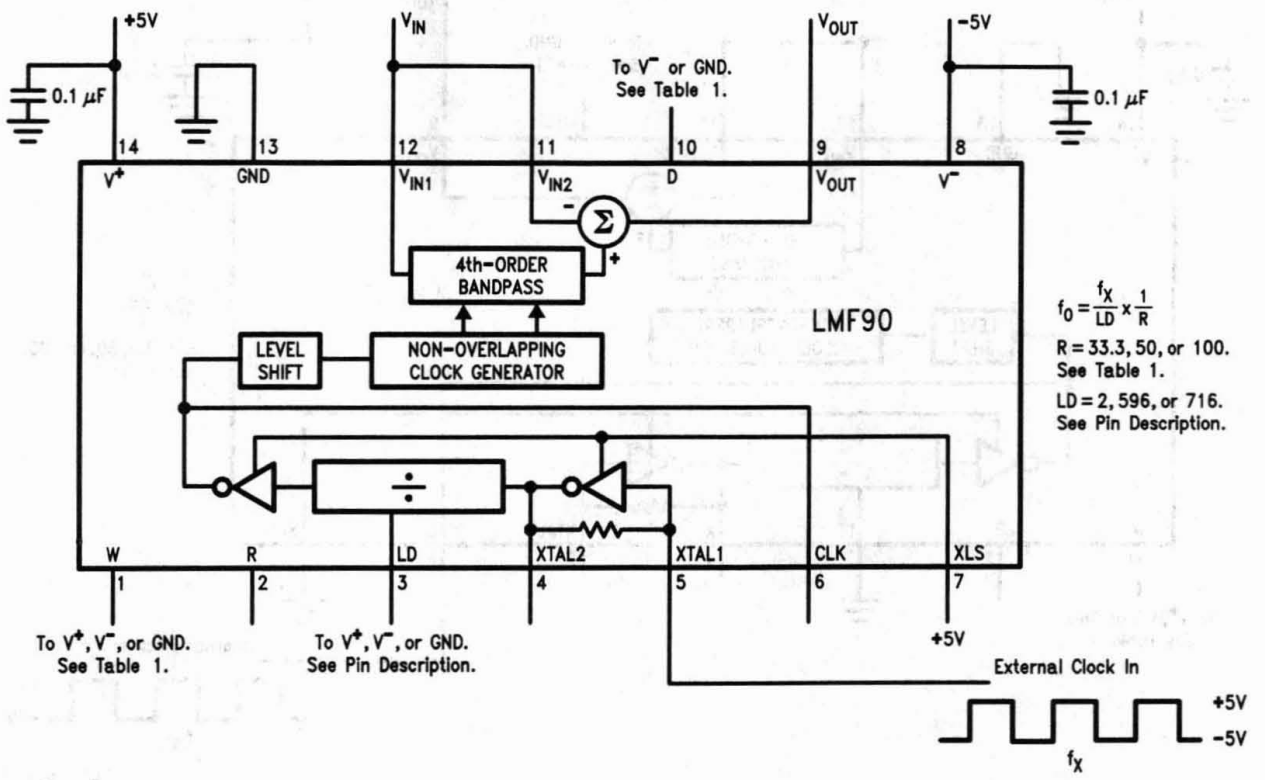

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FIGURE 8. Dual Supply; external CMOS-level clock. Internal frequency divider enabled. Output of logic divider available on pin 6.

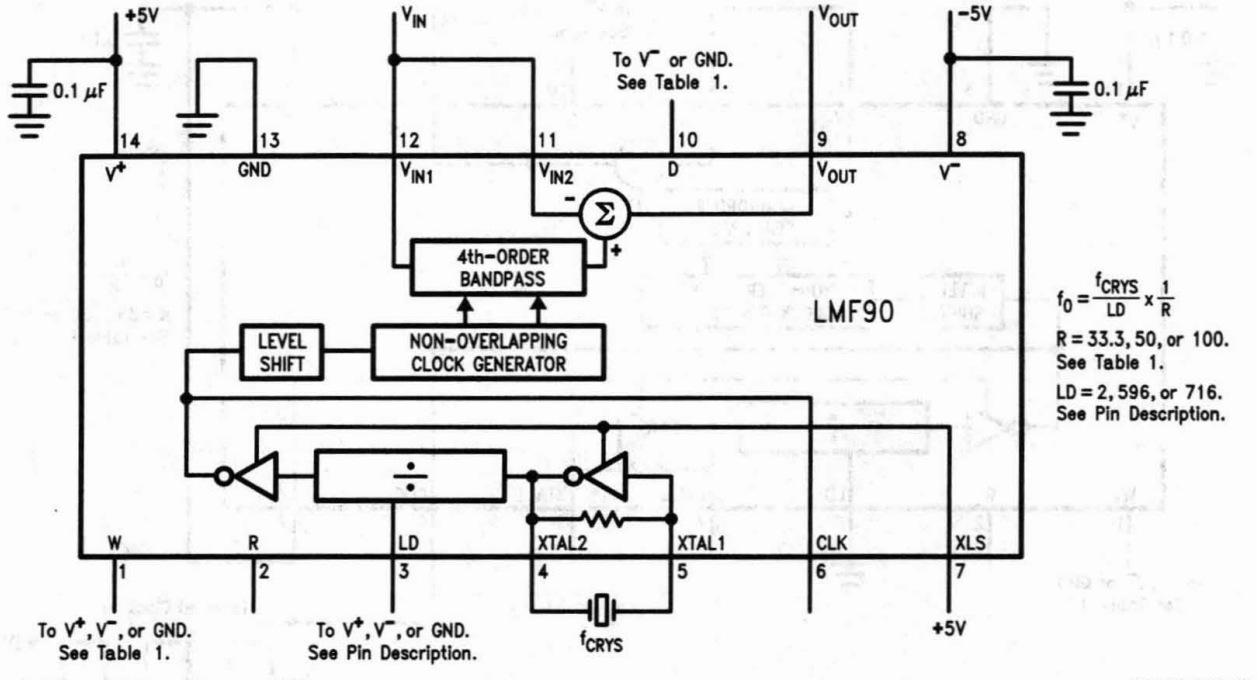

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FIGURE 9. Dual supply; internal crystal clock oscillator. Internal frequency divider enabled. Output of logic divider available on pin 6.

2.0 Applications Information (Continued)

SINGLE-SUPPLY CLOCK OPTIONS

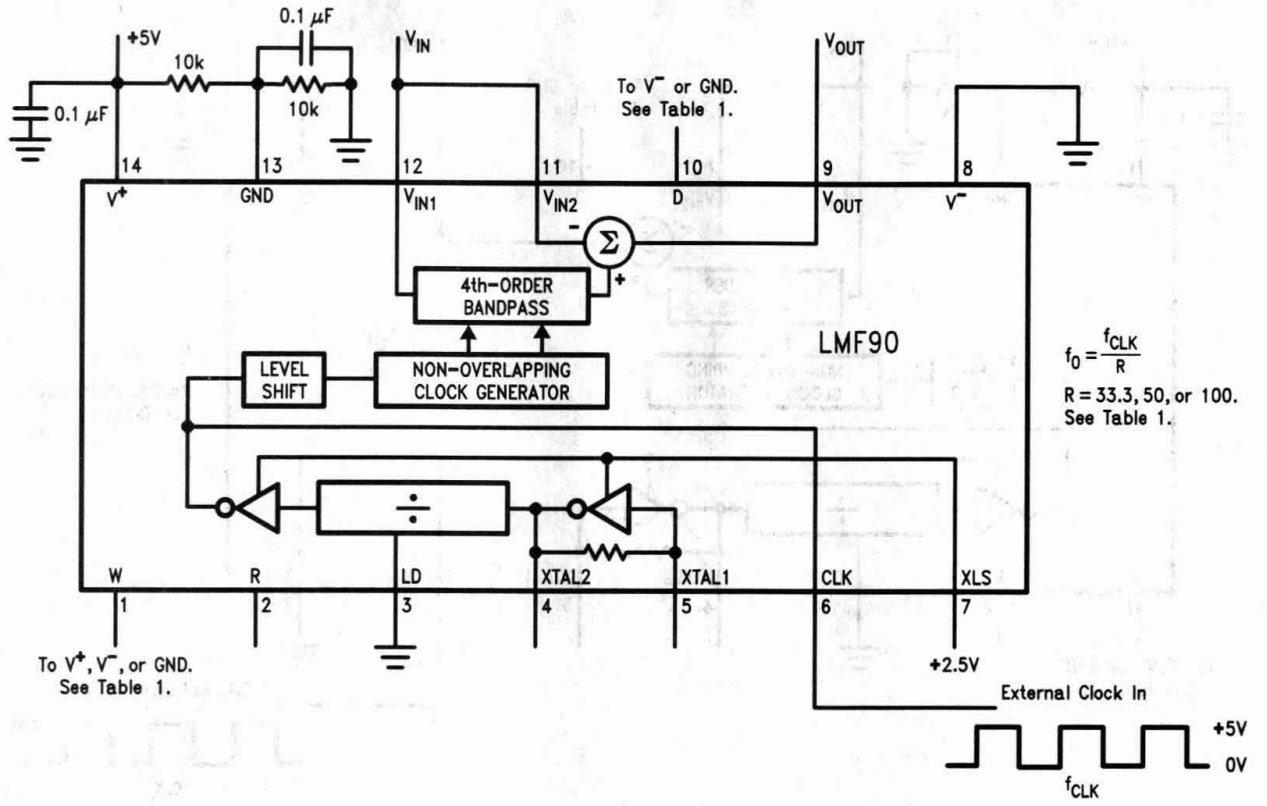

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FIGURE 10. Single +5V supply; external TTL-level clock. Internal frequency divider disabled.

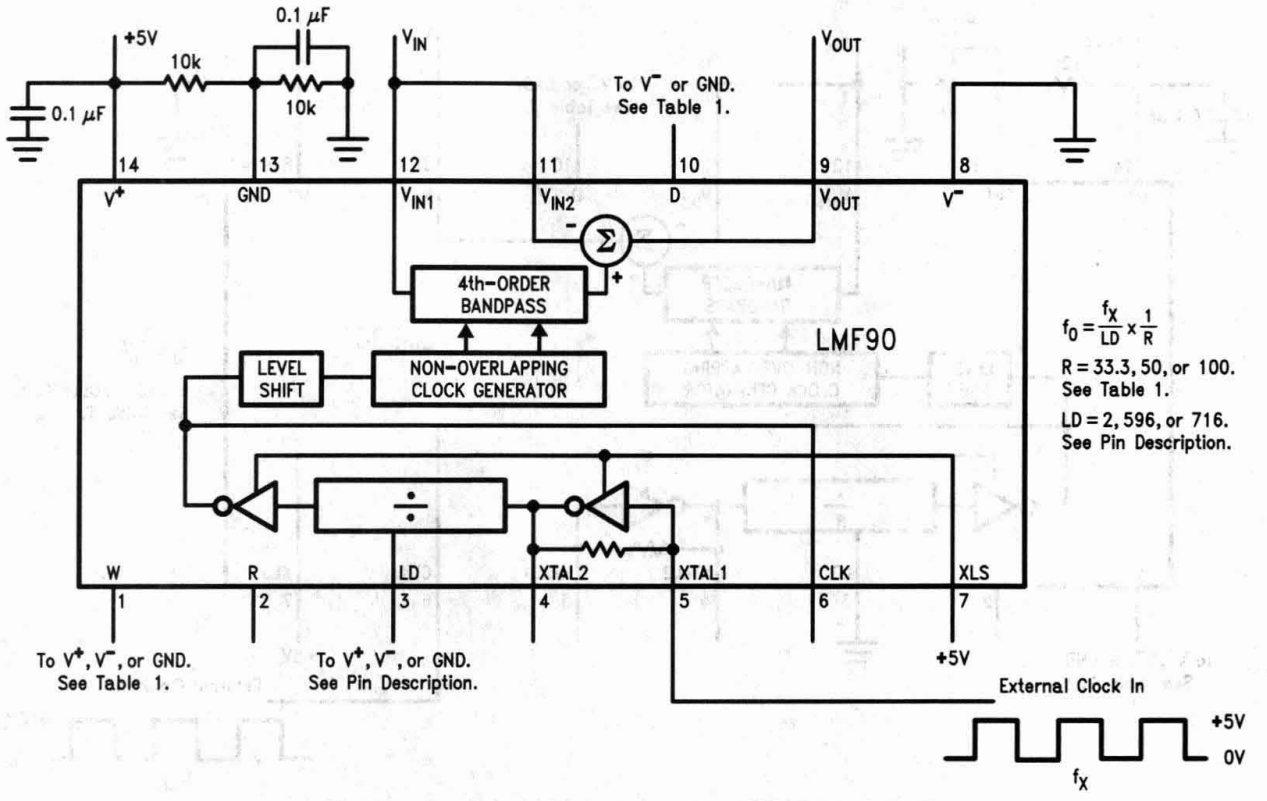

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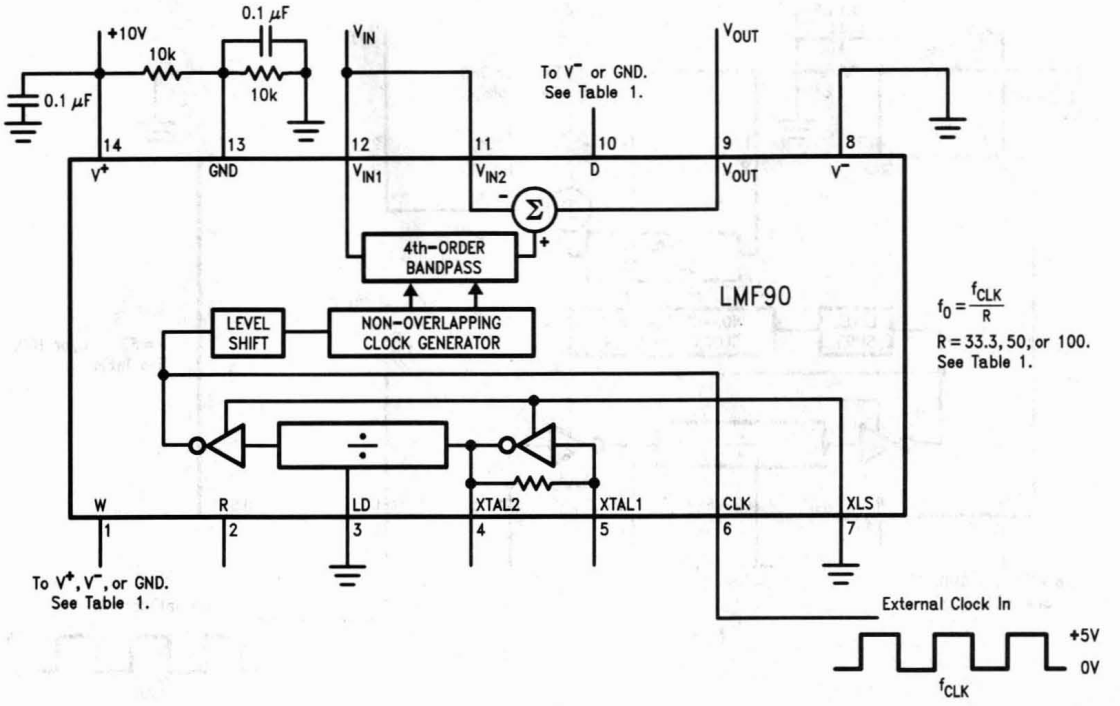
FIGURE 11. Single +5V supply; external CMOS-level clock. Internal frequency divider enabled. Output of logic divider available on pin 6.

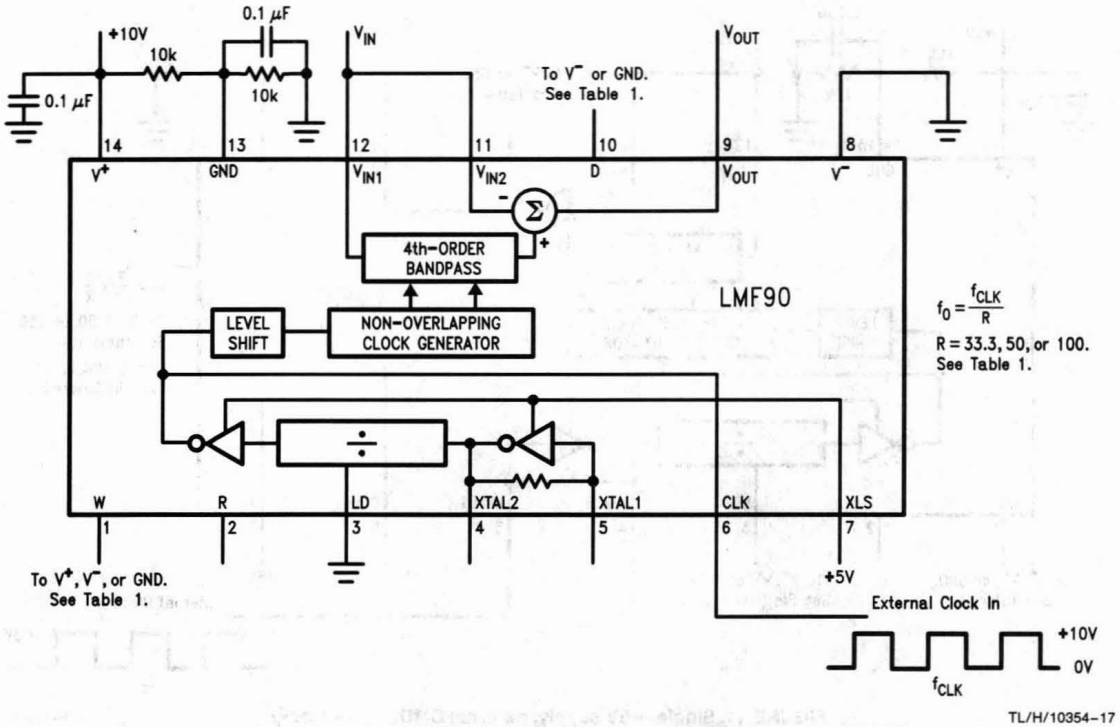
2.0 Applications Information (Continued)

SINGLE-SUPPLY CLOCK OPTIONS



TL/H/10354–16

FIGURE 12. Single + 10V supply; external TTL-level clock. Internal frequency divider disabled.

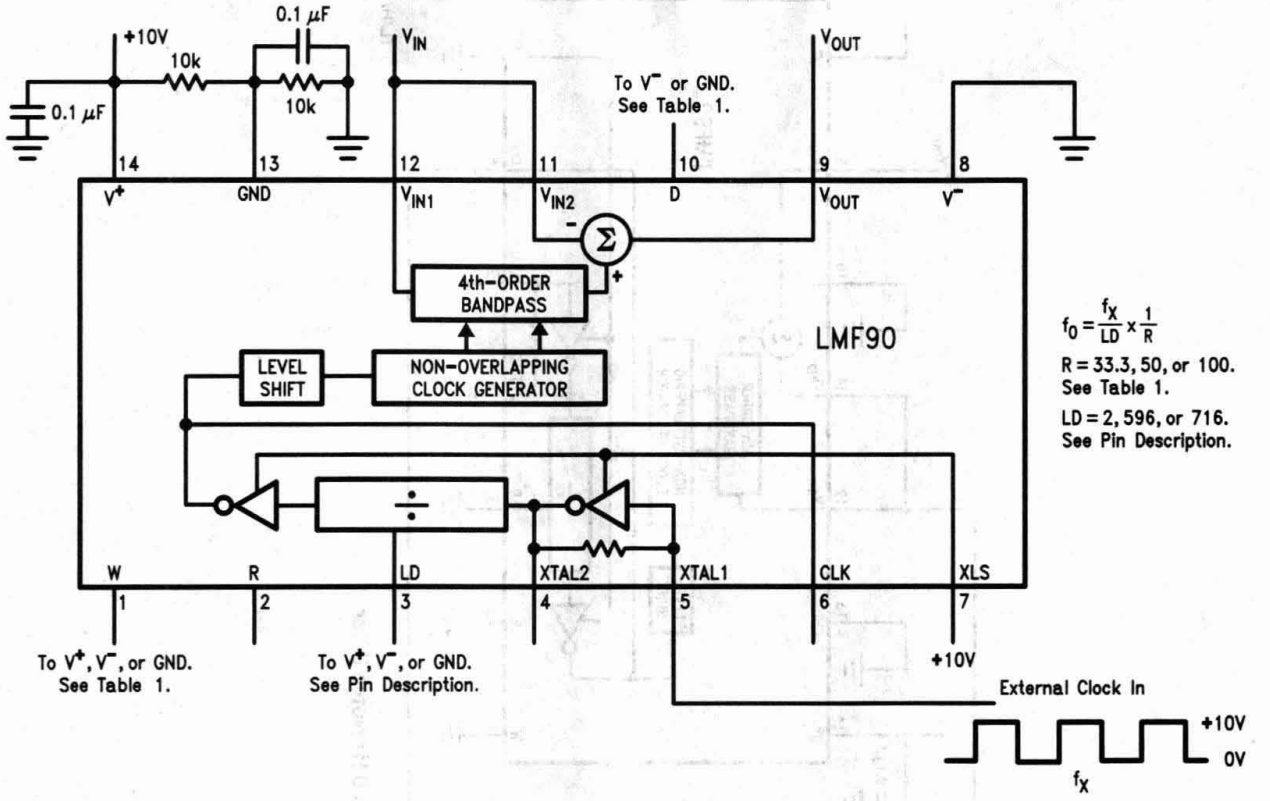


TL/H/10354–17

FIGURE 13. Single + 10V supply; external CMOS-level clock. Internal frequency divider disabled.

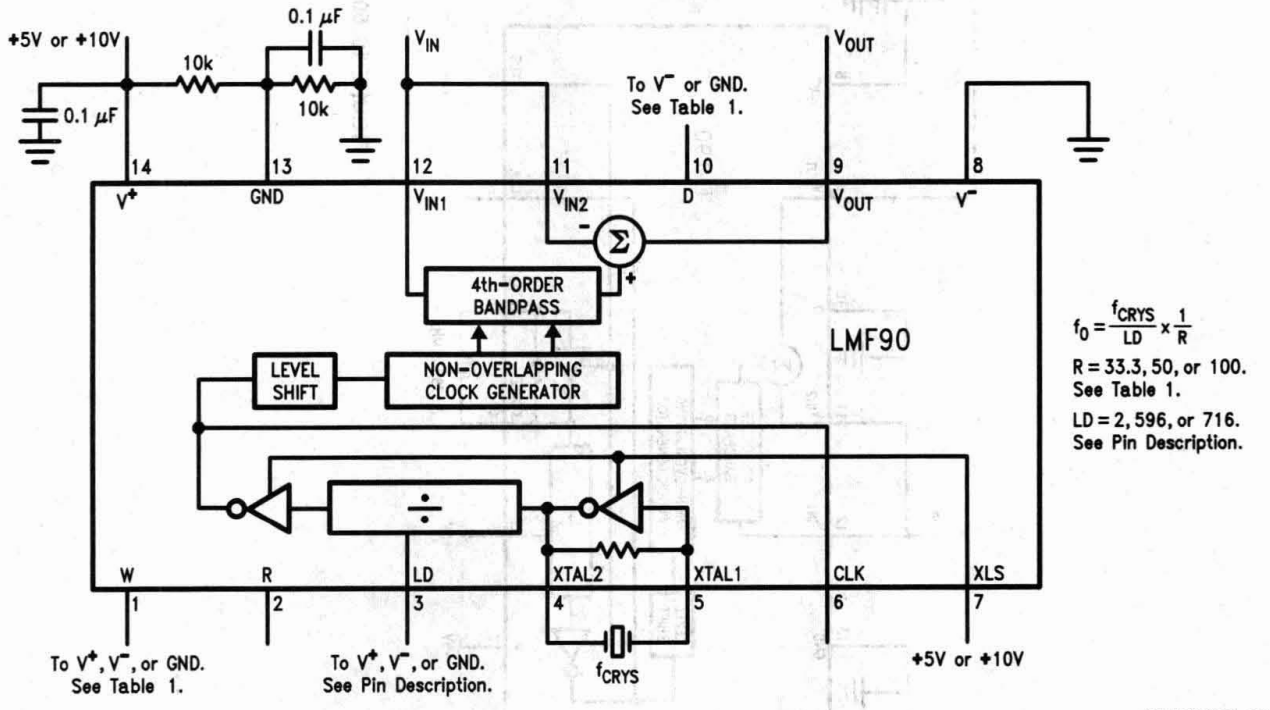
2.0 Applications Information (Continued)

SINGLE-SUPPLY CLOCK OPTIONS



TL/H/10354–18

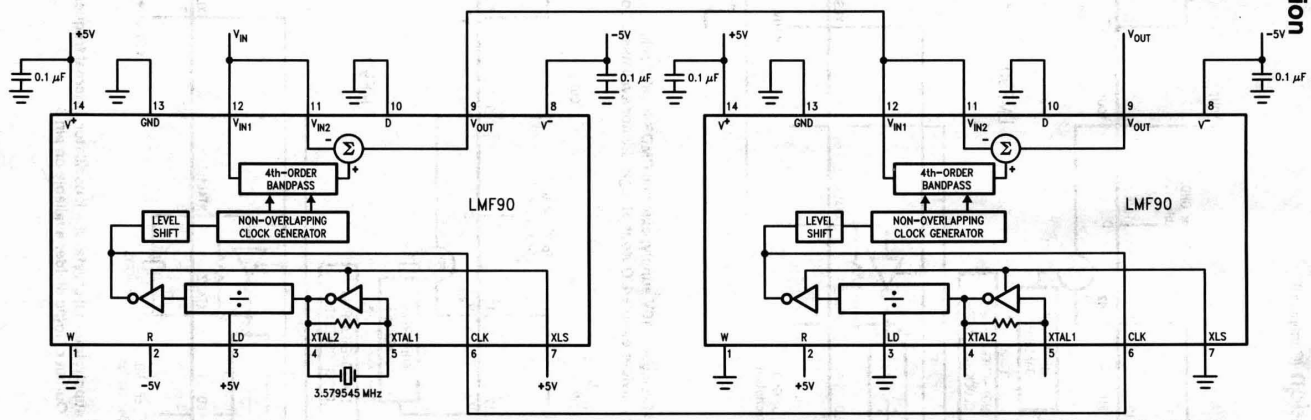
FIGURE 14. Single +10V supply; external CMOS-level clock. Internal frequency divider enabled. Output of logic divider available on pin 6.



TL/H/10354–19

FIGURE 15. Single +5V or +10V supply; internal crystal clock oscillator. Internal frequency divider enabled. Output of logic divider available on pin 6.

Typical Application



TL/H/10354–20

FIGURE 16. 50 Hz and 150 Hz Notch Filter

National Semiconductor

LMF100 High Performance Dual Switched Capacitor Filter

General Description

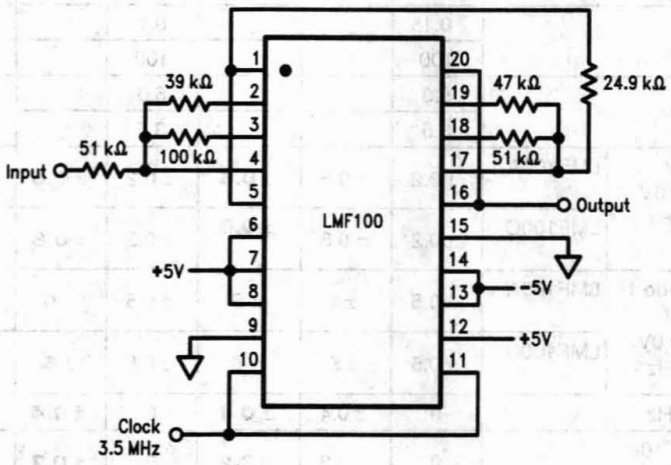
The LMF100 consists of two independent general purpose high performance switched capacitor filters. With an external clock and 2 to 4 resistors, various second-order and first-order filtering functions can be realized by each filter block. Each block has 3 outputs. One output can be configured to perform either an allpass, highpass, or notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter stage is tuned by using an external clock or a combination of a clock and resistor ratio. Up to a 4th-order biquadratic function can be realized with a single LMF100. Higher order filters are implemented by simply cascading additional packages, and all the classical filters (such as Butterworth, Bessel, Elliptic, and Chebyshev) can be realized.

The LMF100 is fabricated on National Semiconductor's high performance analog silicon gate CMOS process, LMCMOS™. This allows for the production of a very low offset, high frequency filter building block. The LMF100 is pin-compatible with the industry standard MF10, but provides greatly improved performance.

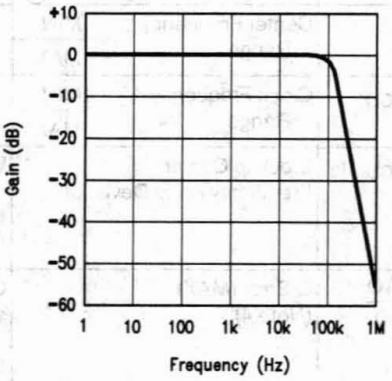
Features

- Wide 4V to 15V power supply range
- Operation up to 100 kHz
- Low offset voltage (50:1 or 100:1 mode) — typically
  Vos1 = ±5 mV
  Vos2 = ±15 mV
  Vos3 = ±15 mV
- Low crosstalk −60 dB
- Clock to center frequency ratio accuracy ±0.2% typical
- $f_0 \times Q$ range up to 1.8 MHz
- Pin-compatible with MF10

4th Order 100 kHz Butterworth Lowpass Filter



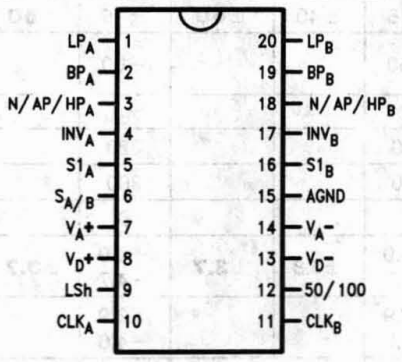
TL/H/5645-2



TL/H/5645-3

Connection Diagram

Surface Mount and Dual-In-Line Package



TL/H/5645-18

Top View

Order Number LMF100AE/883 or 5962-9153301M2A, LMF100AJ, LMF100AJ/883 or 5962-9153301MRA, LMF100CIJ, LMF100ACN, LMF100CCN, LMF100CIN or LMF100CIWM

See NS Package Number J20A, N20A or M20B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 14)

Supply Voltage ($V^+ - V^-$)	16V
Voltage at Any Pin	$V^+ + 0.3V$
	$V^- - 0.3V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150°C
ESD Susceptability (Note 11)	2000V

Soldering Information

N Package: 10 sec.	260°C
J Package: 10 sec.	300°C
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF100ACN, LMF100CCN	$0°C \le T_A \le +70°C$
LMF100CIJ, LMF100CIN, LMF100CIWM	$-40°C \le T_A \le +85°C$
LMF100AJ, MF100AJ/883, LMF100AE/883	$-55°C \le T_A \le +125°C$
Supply Voltage	$4V \le V^+ - V^- \le 15V$

Electrical Characteristics

The following specifications apply for Mode 1, Q = 10 ($R_1 = R_3 = 100k$, $R_2 = 10k$), $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		LMF100ACN, LMF100CCN			LMF100AJ, LMF100CIN, LMF100CIWM, LMF100CIJ			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
I_s	Maximum Supply Current		f_{CLK} = 250 kHz No Input Signal		9	13	**13**	9	**13**		mA
f_0	Center Frequency Range	MIN			0.1			0.1			Hz
		MAX			100			100			kHz
f_{CLK}	Clock Frequency Range	MIN			5.0			5.0			Hz
		MAX			3.5			3.5			MHz
f_{CLK}/f_0	Clock to Center Frequency Ratio Deviation		V_{Pin12} = 5V or 0V, f_{CLK} = 1 MHz	LMF100A	±0.2	±0.6	**±0.6**	±0.2	**±0.6**		%
				LMF100C	±0.2	±0.8	**±0.8**	±0.2	**±0.8**		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		Q = 10, Mode 1, V_{Pin12} = 5V or 0V, f_{CLK} = 1 MHz	LMF100A	±0.5	±4	**±5**	±0.5	**±5**		%
				LMF100C	±0.5	±5	**±6**	±0.5	**±6**		%
H_{OBP}	Bandpass Gain at f_0		f_{CLK} = 1 MHz		0	±0.4	**±0.4**	0	**±0.4**		dB
H_{OLP}	DC Lowpass Gain		$R_1 = R_2$ = 10k, f_{CLK} = 250 kHz		0	±0.2	**±0.2**	0	**±0.2**		dB
V_{OS1}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±5.0	±15	**±15**	±5.0	**±15**		mV
V_{OS2}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz	$S_{A/B} = V^+$	±30	±80	**±80**	±30	**±80**		mV
				$S_{A/B} = V^-$	±15	±70	**±70**	±15	**±70**		mV
V_{OS3}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±15	±40	**±60**	±15	**±60**		mV
	Crosstalk (Note 6)		A Side to B Side or B Side to A Side		−60			−60			dB
	Output Noise (Note 12)		f_{CLK} = 250 kHz, 20 kHz Bandwidth, 100:1 Mode	N	40			40			μV
				BP	320			320			
				LP	300			300			
	Clock Feedthrough (Note 13)		f_{CLK} = 250 kHz 100:1 Mode		6			6			mV
V_{OUT}	Minimum Output Voltage Swing		R_L = 5k (All Outputs)		+4.0 −4.7	±3.8	**±3.7**	+4.0 −4.7	**±3.7**		V
			R_L = 3.5k (All Outputs)		+3.9 −4.6			+3.9 −4.6			V
GBW	Op Amp Gain BW Product				5			5			MHz
SR	Op Amp Slew Rate				20			20			V/μs

Electrical Characteristics

The following specifications apply for Mode 1, Q = 10 ($R_1 = R_3 = 100k$, $R_2 = 10k$), $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter		Conditions	LMF100ACN, LMF100CCN			LMF100AJ, LMF100CIN, LMF100CIWM, LMF100CIJ			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
I_{sc}	Maximum Output Short Circuit Current (Note 7)	Source	(All Outputs)	12			12			mA
		Sink		45			45			mA
I_{IN}	Input Current on Pins: 4, 5, 6, 9, 10, 11, 12, 16, 17				10			**10**		μA

Electrical Characteristics

The following specifications apply for Mode 1, Q = 10 ($R_1 = R_3 = 100k$, $R_2 = 10k$), $V^+ = +2.50V$ and $V^- = -2.50V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		LMF100ACN, LMF100CCN			LMF100AJ, LMF100CIN, LMF100CIWM, LMF100CIJ			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
I_s	Maximum Supply Current		f_{CLK} = 250 kHz No Input Signal		8	12	**12**	8	**12**		mA
f_0	Center Frequency Range	MIN			0.1			0.1			Hz
		MAX			50			50			kHz
f_{CLK}	Clock Frequency Range	MIN			5.0			5.0			Hz
		MAX			1.5			1.5			MHz
f_{CLK}/f_0	Clock to Center Frequency Ratio Deviation		V_{Pin12} = 2.5V or 0V, f_{CLK} = 1 MHz	LMF100A	±0.2	±0.6	**±0.8**	±0.2	**±0.8**		%
				LMF100C	±0.2	±1	**±1**	±0.2	**±1**		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		Q = 10, Mode 1, V_{Pin12} = 5V or 0V, f_{CLK} = 1 MHz	LMF100A	±0.5	±4	**±6**	±0.5	**±6**		%
				LMF100C	±0.5	±5	**±8**	±0.5	**±8**		%
H_{OBP}	Bandpass Gain at f_0		f_{CLK} = 1 MHz		0	±0.4	**±0.5**	0	**±0.5**		dB
H_{OLP}	DC Lowpass Gain		$R_1 = R_2 = 10k$, f_{CLK} = 250 kHz		0	±0.2	**±0.2**	0	**±0.2**		dB
V_{OS1}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±5.0	±15	**±15**	±5.0	**±15**		mV
V_{OS2}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz	$S_{A/B} = V^+$	±20	±60	**±60**	±20	**±60**		mV
				$S_{A/B} = V^-$	±10	±50	**±60**	±10	**±60**		mV
V_{OS3}	DC Offset Voltage (Note 5)		f_{CLK} = 250 kHz		±10	±25	**±30**	±10	**±30**		mV
	Crosstalk (Note 6)		A Side to B Side or B Side to A Side		−65			−65			dB
	Output Noise (Note 12)		f_{CLK} = 250 kHz, 20 kHz Bandwidth, 100:1 Mode	N	25			25			μV
				BP	250			250			
				LP	220			220			
	Clock Feedthrough (Note 13)		f_{CLK} = 250 kHz 100:1 Mode		2			2			mV
V_{OUT}	Minimum Output Voltage Swing		R_L = 5k (All Outputs)		+1.6 −2.2	±1.5	**±1.4**	+1.6 −2.2	**±1.4**		V
			R_L = 3.5k (All outputs)		+1.5 −2.1			+1.5 −2.1			V
GBW	Op Amp Gain BW Product				5			5			MHz
SR	Op Amp Slew Rate				18			18			V/μs
I_{sc}	Maximum Output Short Circuit Current (Note 7)	Source	(All Outputs)		10			10			mA
		Sink			20			20			mA

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Logic Input Characteristics **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions	LMF100ACN, LMF100CCN			LMF100AJ, LMF100CIN, LMF100CIWM, LMF100CIJ			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +5V, V^- = -5V,$ $V_{LSh} = 0V$		+3.0	**+3.0**		**+3.0**		V
	MAX Logical "0"			−3.0	**−3.0**		**−3.0**		V
	MIN Logical "1"	$V^+ = +10V, V^- = 0V,$ $V_{LSh} = +5V$		+8.0	**+8.0**		**+8.0**		V
	MAX Logical "0"			+2.0	**+2.0**		**+2.0**		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5V, V^- = -5V,$ $V_{LSh} = 0V$		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"			+0.8	**+0.8**		**+0.8**		V
	MIN Logical "1"	$V^+ = +10V, V^- = 0V,$ $V_{LSh} = 0V$		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"			+0.8	**+0.8**		**+0.8**		V
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +2.5V, V^- = -2.5V,$ $V_{LSh} = 0V$		+1.5	**+1.5**		**+1.5**		V
	MAX Logical "0"			−1.5	**−1.5**		**−1.5**		V
	MIN Logical "1"	$V^+ = +5V, V^- = 0V,$ $V_{LSh} = +2.5V$		+4.0	**+4.0**		**+4.0**		V
	MAX Logical "0"			+1.0	**+1.0**		**+1.0**		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5V, V^- = 0V,$ $V_{LSh} = 0V, V_D{}^+ = 0V$		+2.0	**+2.0**		**+2.0**		V
	MAX Logical "0"			+0.8	**+0.8**		**+0.8**		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the LMF100ACN/CCN/CIN when board mounted is 55°C/W. For the LMF100AJ/CIJ, this number increases to 95°C/W and for the LMF100CIWM this number is 66°C/W.

Note 4: The accuracy of the Q value is a function of the center frequency (f_0). This is illustrated in the curves under the heading "Typical Peformance Characteristics".

Note 5: V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in the Applications Information section 3.4.

Note 6: Crosstalk between the internal filter sections is measured by applying a 1 V_{RMS} 10 kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the 1 V_{RMS} input signal of the other section.

Note 7: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Design limits are guaranteed to National's AOQL (Average Outgoing Quality Level) but are not 100% tested.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

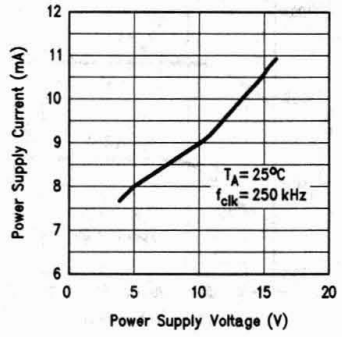
Note 12: In 50:1 mode the output noise is 3 dB higher.

Note 13: In 50:1 mode the clock feedthrough is 6 dB higher.

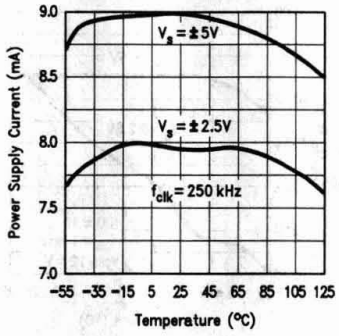
Note 14: A military RETS specification is available upon request.

Typical Performance Characteristics

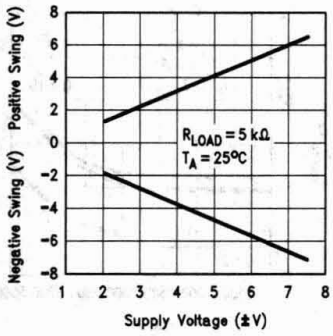
Power Supply Current vs Power Supply Voltage



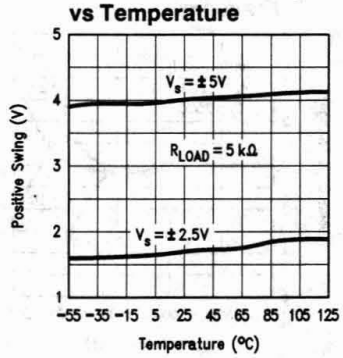
Power Supply Current vs Temperature



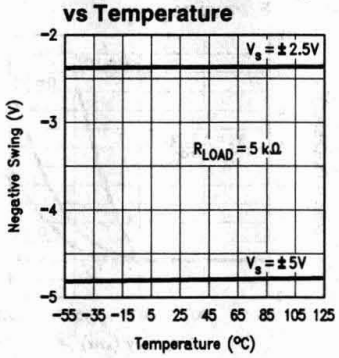
Output Swing vs Supply Voltage



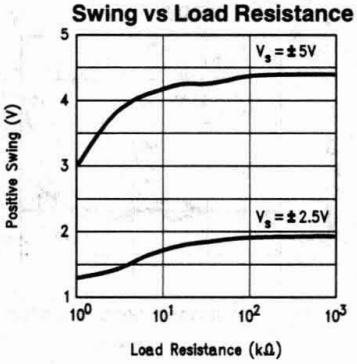
Positive Output Swing vs Temperature



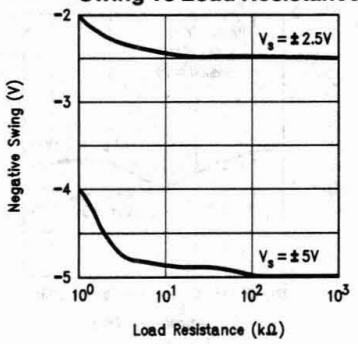
Negative Output Swing vs Temperature



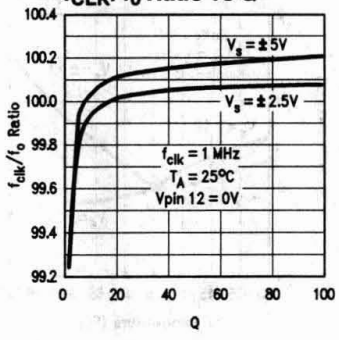
Positive Output Voltage Swing vs Load Resistance



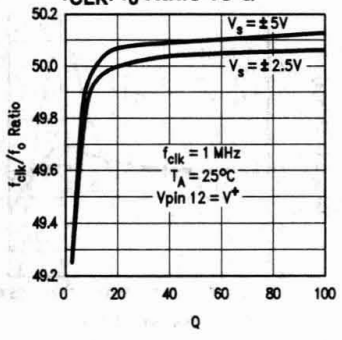
Negative Output Voltage Swing vs Load Resistance



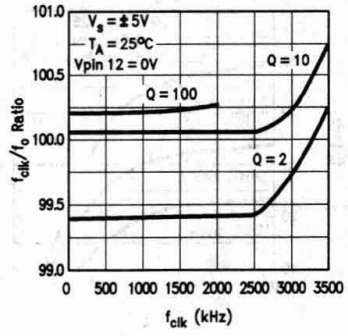
f_{CLK}/f_0 Ratio vs Q



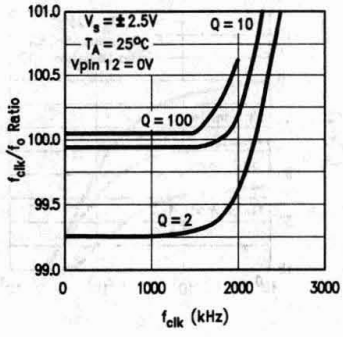
f_{CLK}/f_0 Ratio vs Q



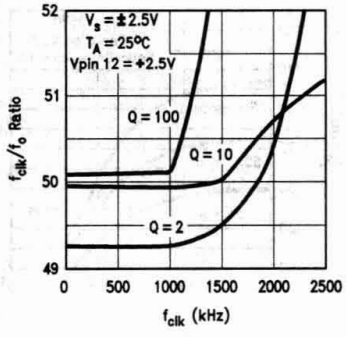
f_{CLK}/f_0 Ratio vs f_{CLK}



f_{CLK}/f_0 Ratio vs f_{CLK}



f_{CLK}/f_0 Ratio vs f_{CLK}

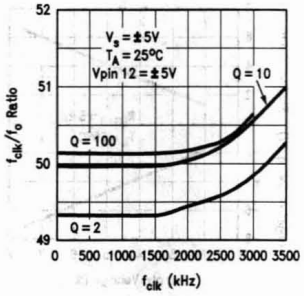


TL/H/5645–8

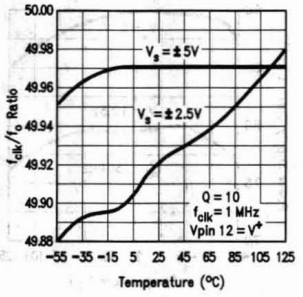
7

Typical Performance Characteristics (Continued)

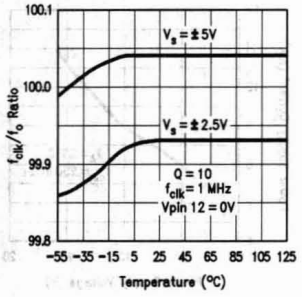
f_{CLK}/f_0 Ratio vs f_{CLK}



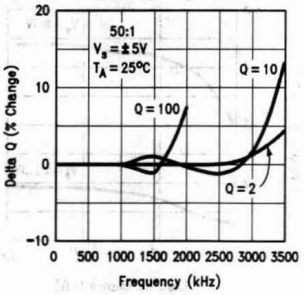
f_{CLK}/f_0 Ratio vs Temperature



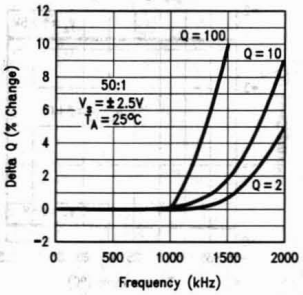
f_{CLK}/f_0 Ratio vs Temperature



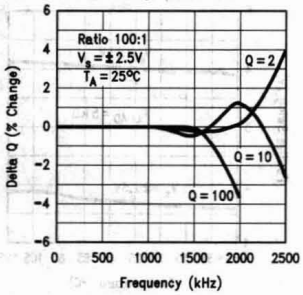
Q Deviation vs Clock Frequency



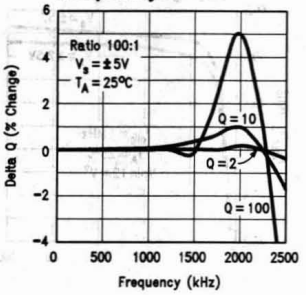
Q Deviation vs Clock Frequency



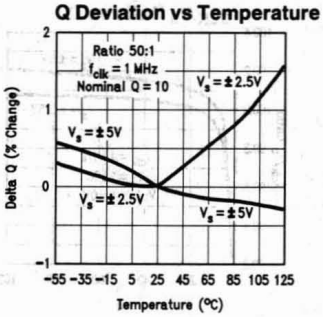
Q Deviation vs Clock Frequency



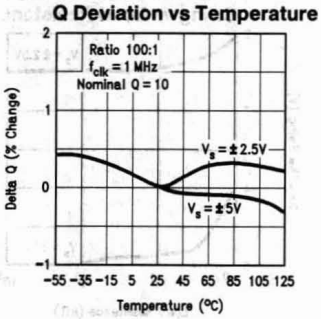
Q Deviation vs Clock Frequency



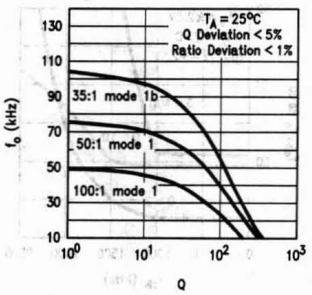
Q Deviation vs Temperature



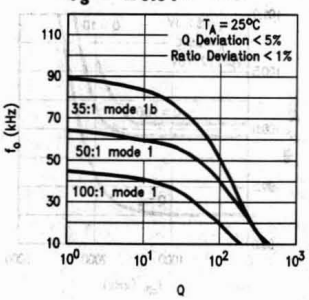
Q Deviation vs Temperature



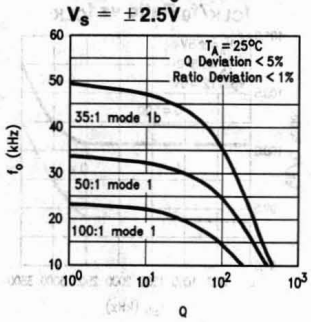
Maximum f_0 vs Q at $V_s = \pm 7.5V$



Maximum f_0 vs Q at $V_s = \pm 5.0V$

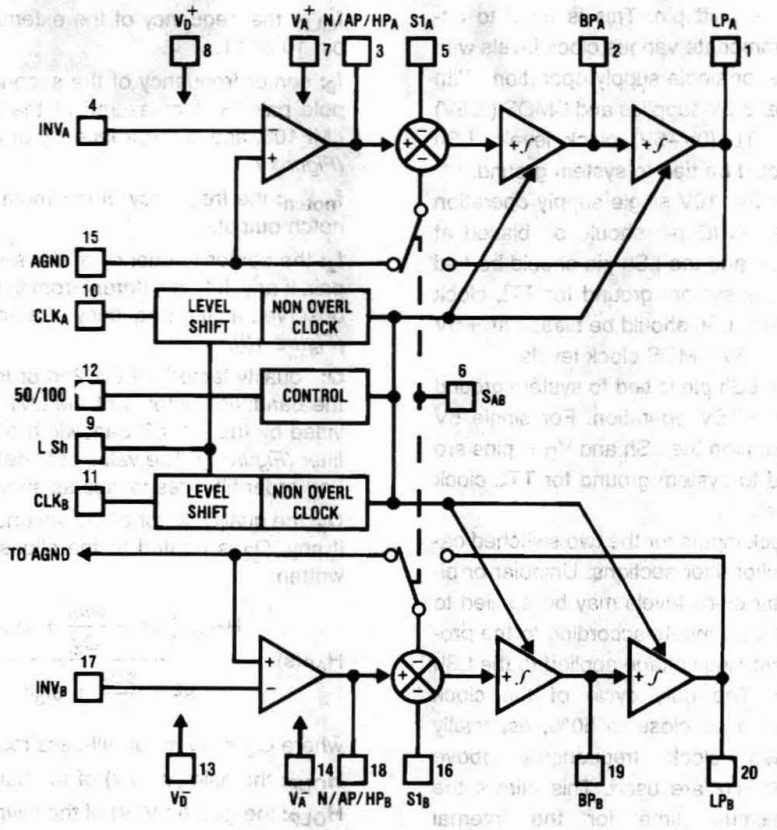


Maximum f_0 vs Q at $V_s = \pm 2.5V$



TL/H/5645–9

LMF100 System Block Diagram



TL/H/5645–1

Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18) The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically swing to within 1V of each supply when driving a 5 kΩ load. For optimum performance, capacitive loading on these outputs should be minimized. For signal frequencies above 15 kHz the capacitance loading should be kept below 30 pF.

INV(4,17) The inverting input of the summing opamp of each filter. These are high impedance inputs. The non-inverting input is internally tied to AGND so the opamp can be used only as an inverting amplifier.

S1(5,16) S1 is a signal input pin used in modes 1b, 4, and 5. The input impedance is $1/f_{CLK} \times 1$ pF. The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

$S_{A/B}$(6) This pin activates a switch that connects one of the inputs of each filter's second summer either to AGND ($S_{A/B}$ tied to V^-) or to the lowpass (LP) output ($S_{A/B}$ tied to V^+). This offers the flexibility needed for configuring the filter in its various modes of operation.

V_A^+(7)* This is both the analog and digital positive supply.

V_D^+(8)* This pin needs to be tied to V^+ except when the device is to operate on a single 5V supply and a TTL level clock is applied. For 5V, TTL operation, V_D^+ should be tied to ground (0V).

V_A^-(14), V_D^-(13) Analog and digital negative supplies. V_A^- and V_D^- should be derived from the same source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can also be tied together externally and bypassed with a single capacitor.

Pin Descriptions (Continued)

LSh(9) — Level shift pin. This is used to accommodate various clock levels with dual or single supply operation. With dual ±5V supplies and CMOS (±5V) or TTL (0V–5V) clock levels, LSh should be tied to system ground.

For 0V–10V single supply operation the AGND pin should be biased at +5V and the LSh pin should be tied to the system ground for TTL clock levels. LSh should be biased at +5V for ±5V CMOS clock levels.

The LSh pin is tied to system ground for ±2.5V operation. For single 5V operation the LSh and V_D+ pins are tied to system ground for TTL clock levels.

CLK(10,11) — Clock inputs for the two switched capacitor filter sections. Unipolar or bipolar clock levels may be applied to the CLK inputs according to the programming voltage applied to the LSh pin. The duty cycle of the clock should be close to 50%, especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal opamps to settle, which yields optimum filter performance.

50/100(12)* — By tying this pin to V^+ a 50:1 clock to filter center frequency ratio is obtained. Tying this pin at mid-supply (i.e., system ground with dual supplies) or to V^- allows the filter to operate at a 100:1 clock to center frequency ratio.

AGND(15) — This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

*This device is pin-for-pin compatible with the MF10 except for the following changes:

1. Unlike the MF10, the LMF100 has a single positive supply pin (V_A+).
2. On the LMF100 V_D+ is a control pin and is not the digital positive supply as on the MF10.
3. Unlike the MF10, the LMF100 does not support the current limiting mode. When the 50/100 pin is tied to V^- the LMF100 will remain in the 100:1 mode.

1.0 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_0: center frequency of the second order function complex pole pair. f_0 is measured at the bandpass outputs of the LMF100, and is the frequency of maximum bandpass gain. *(Figure 1)*.

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_0 and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. *(Figure 13)*.

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the LMF100 and is equal to f_0 divided by the −3 dB bandwidth of the 2nd order bandpass filter *(Figure 1)*. The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q_z} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

where $Q_Z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_0$.

H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz *(Figure 2)*.

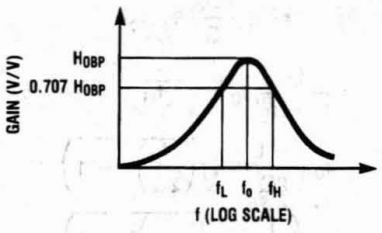
H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{CLK}/2$ *(Figure 3)*.

H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency *(Figure 4)*. When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a *(Figures 10 and 12)*, the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

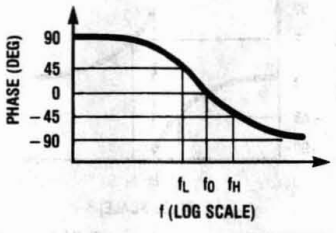
H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{CLK}/2$.

1.0 Definitions of Terms (Continued)



TL/H/5645–19

(a)



TL/H/5645–20

(b)

$$H_{BP}(s) = \frac{\frac{\omega_O}{Q} s}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

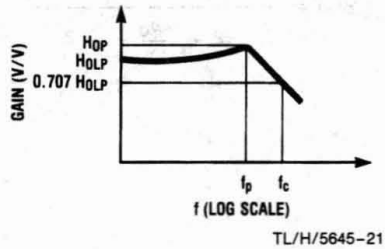
$$Q = \frac{f_0}{f_H - f_L}; \; f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0 \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_0 \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

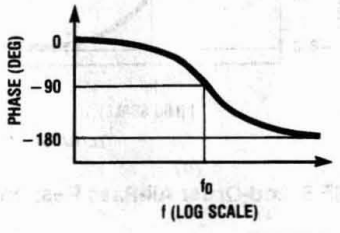
$$\omega_o = 2\pi f_0$$

FIGURE 1. 2nd-Order Bandpass Response



TL/H/5645–21

(a)



TL/H/5645–22

(b)

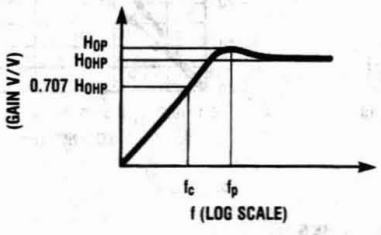
$$H_{LP}(s) = \frac{H_{OLP}\omega_O^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$f_c = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_0 \sqrt{1 - \frac{1}{2Q^2}}$$

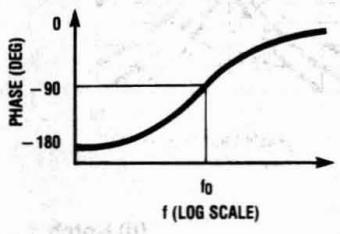
$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



TL/H/5645–23

(a)



TL/H/5645–24

(b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$f_c = f_0 \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

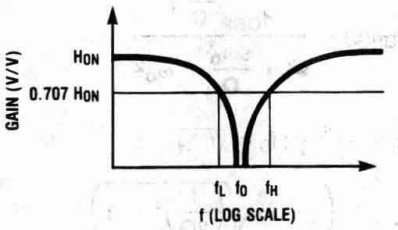
$$f_p = f_0 \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3. 2nd-Order High-Pass Response

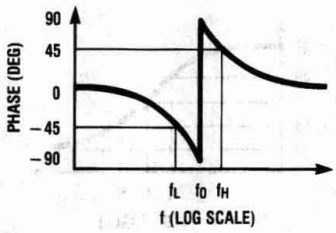
7

1.0 Definitions of Terms (Continued)



TL/H/5645–25

(a)



TL/H/5645–26

(b)

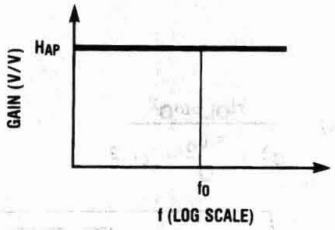
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_0}{f_H - f_L};\ f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

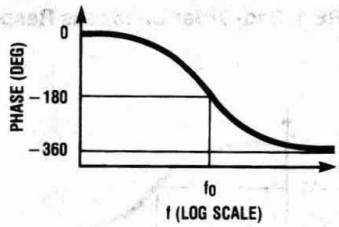
$$f_H = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



TL/H/5645–27

(a)

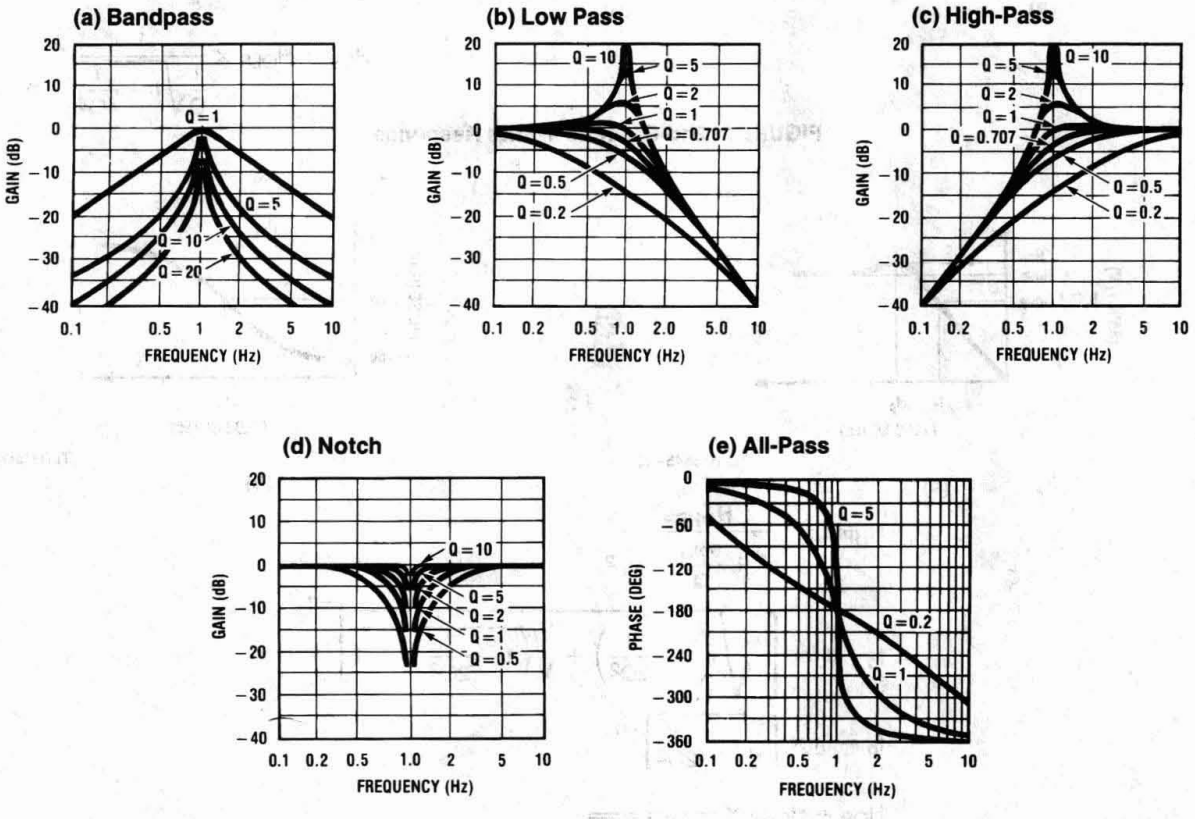


TL/H/5645–28

(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

FIGURE 5. 2nd-Order All-Pass Response



TL/H/5645–29

FIGURE 6. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The LMF100 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain analysis is appropriate. Since this is cumbersome, and since the LMF100 closely approximates continuous filters, the following discussion is based on the well-known frequency domain. Each LMF100 can produce two full 2nd order functions. See Table I for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_0$ **(See *Figure 7*)**

f_0 = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair = f_0.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $f \rightarrow 0$, $f \rightarrow f_{CLK}/2$ $= \frac{-R_2}{R_1}$

$Q = \frac{f_0}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{Q}$ or $H_{OBP} = H_{OLP} \times Q$

$= H_{ON} \times Q$.

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$f_0 = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

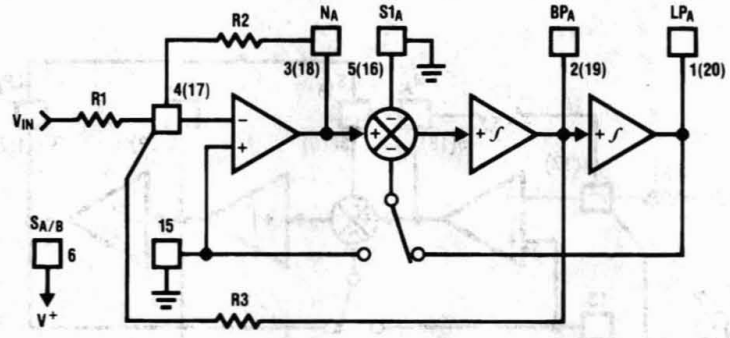
$H_{OLP} = -1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

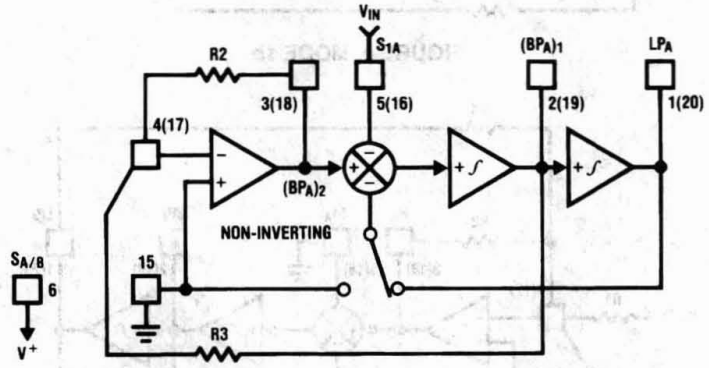
Circuit dynamics: $H_{OBP_1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ) source.



TL/H/5645–11

FIGURE 7. MODE 1



TL/H/5645–4

FIGURE 8. MODE 1a

2.0 Modes of Operation (Continued)

MODE 1b: Notch 1, Bandpass, Lowpass Outputs: $f_{notch} = f_0$ (See *Figure 9*)

f_0 = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100} \times \sqrt{2}$ or $\frac{f_{CLK}}{50} \times \sqrt{2}$

f_{notch} = center frequency of the imaginary zero pair = f_0.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{2R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{array}{l} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{array}\right\} = \frac{-R_2}{R_1}$

$Q = \frac{f_0}{BW} = \frac{R3}{R2} \times \sqrt{2}$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{\sqrt{2}\,Q}$ or $H_{OBP} = H_{OLP} \times Q \times \sqrt{2}$

$H_{OBP} = \frac{H_{ON} \times Q}{\sqrt{2}}$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_0$ (See *Figure 10*)

f_0 = center frequency

$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4} + 1}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4} + 1}$

$f_{notch} = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

Q = quality factor of the complex pole pair

$= \frac{\sqrt{R2/R4 + 1}}{R2/R3}$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)

$= -\frac{R2/R1}{R2/R4 + 1}$

H_{OBP} = Bandpass output gain (at $f = f_0$) $= -R3/R1$

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)

$= -\frac{R2/R1}{R2/R4 + 1}$

H_{ON_2} = Notch output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = \sqrt{H_{ON_1}\,H_{ON_2}}$

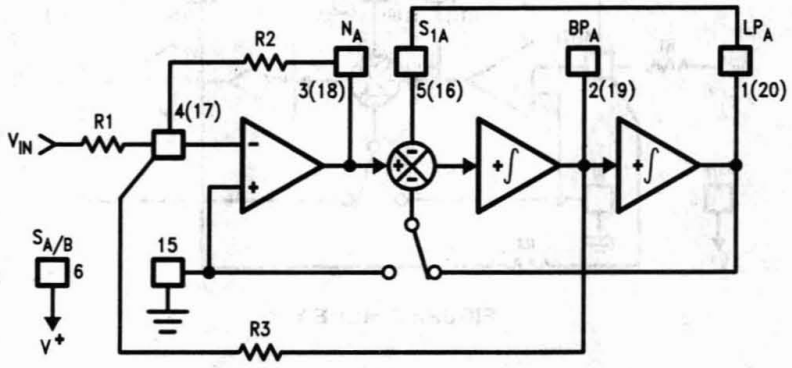


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FIGURE 9. MODE 1b

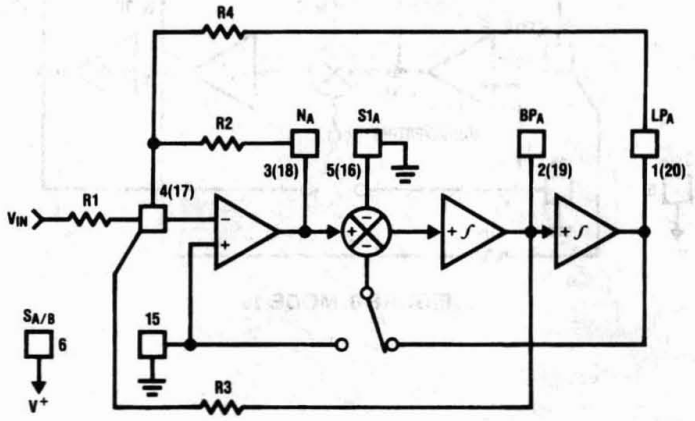

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FIGURE 10. MODE 2

2.0 Modes of Operation (Continued)

MODE 3: Highpass, Bandpass, Lowpass Outputs
(See *Figure 11*)

$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

Q = quality factor of the complex pole pair

$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$

H_{OHP} = Highpass gain $\left(\text{at } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) $= -\frac{R3}{R1}$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R4}{R1}$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)

MODE 3a: HP, BP, LP and Notch with External Op Amp
(See *Figure 12*)

$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$

$H_{OHP} = -\frac{R2}{R1}$

$H_{OBP} = -\frac{R3}{R1}$

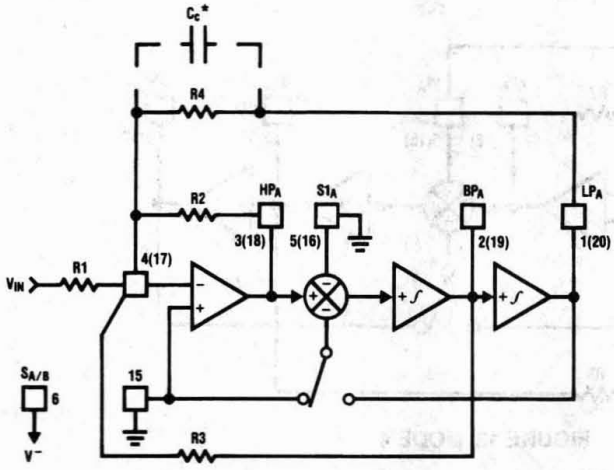
$H_{OLP} = -\frac{R4}{R1}$

f_n = notch frequency $= \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_I}}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_I}}$

H_{ON} = gain of notch at $f = f_0 = \left\| Q\left(\frac{R_g}{R_I} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right) \right\|$

H_{n1} = gain of notch (as $f \rightarrow 0$) $= \frac{R_g}{R_I} \times H_{OLP}$

H_{n2} = gain of notch $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

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FIGURE 11. MODE 3

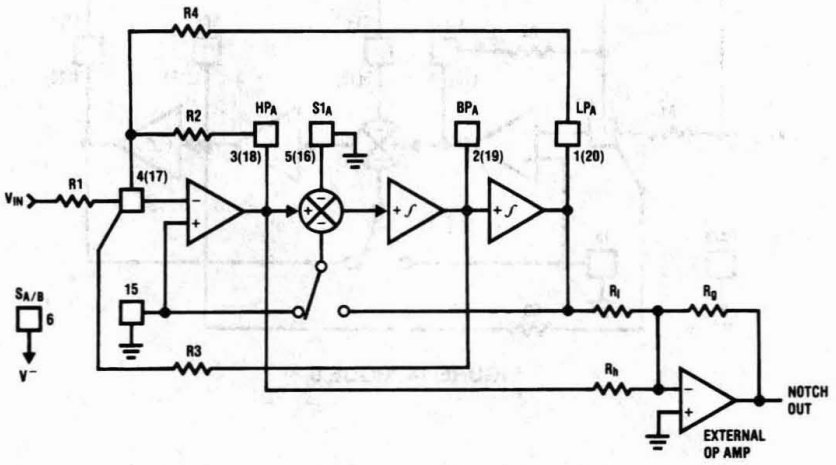

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FIGURE 12. MODE 3a

7

2.0 Modes of Operation (Continued)

MODE 4: Allpass, Bandpass, Lowpass Outputs

(See *Figure 13*)

f_0 = center frequency

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$;

f_z* = center frequency of the complex zero $\approx f_0$

$Q = \frac{f_0}{BW} = \frac{R3}{R2}$;

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

H_{OAP}* = Allpass gain $\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$)

$= -\left(\frac{R2}{R1} + 1\right) = -2$

H_{OBP} = Bandpass gain (at $f = f_0$)

$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_0 occurs causing a 0.4 dB peaking around f_0 of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

MODE 5: Numerator Complex Zeros, BP, LP

(See *Figure 14*)

$f_0 = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100}$ or $\sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$

$f_z = \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{100}$ or $\sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$

$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$

$Q_Z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$

$H_{0_{Z1}}$ = gain at C.Z. output (as $f \rightarrow 0$ Hz)

$\frac{-R2(R4 - R1)}{R1(R2 + R4)}$

$H_{0_{Z2}}$ = gain at C.Z. output $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$

$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$

$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$

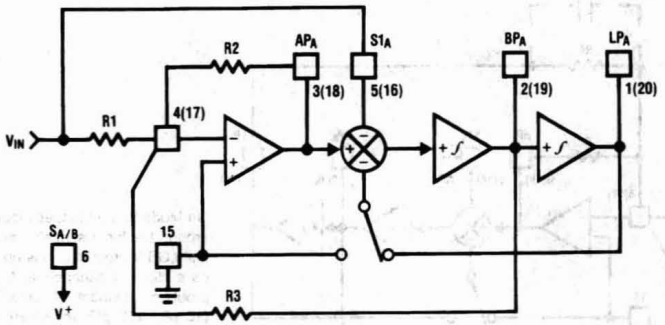

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FIGURE 13. MODE 4

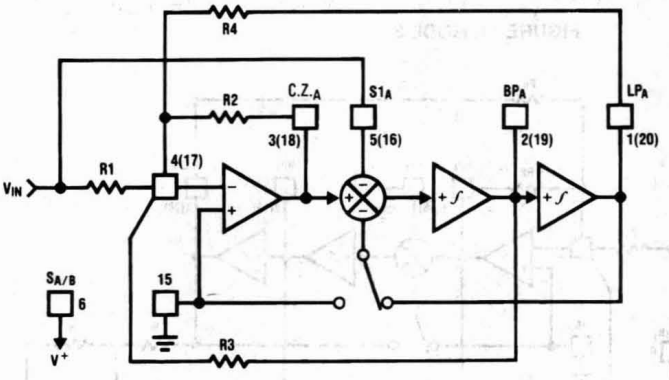

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FIGURE 14. MODE 5

2.0 Modes of Operation (Continued)

MODE 6a: Single Pole, HP, LP Filter (See *Figure 15*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 16*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP_1} = 1 \text{ (non-inverting)}$$

$$H_{OLP_2} = -\frac{R3}{R2}$$

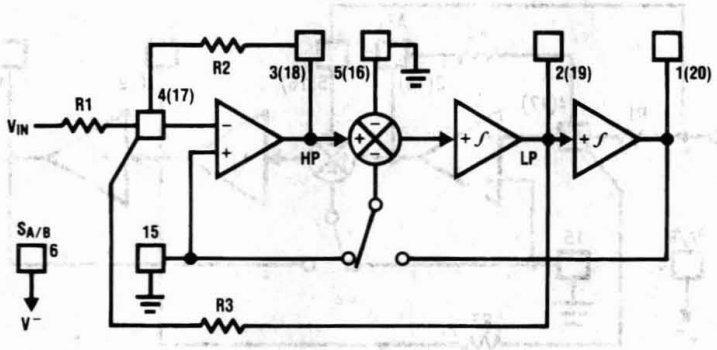

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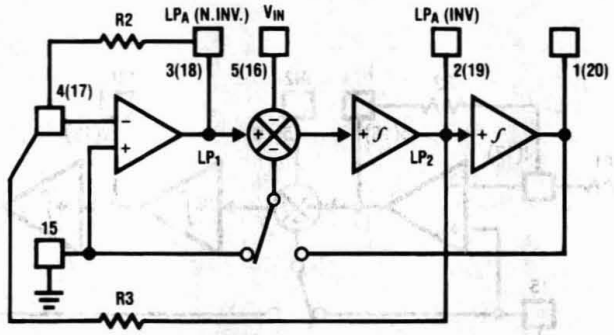
FIGURE 15. MODE 6a



TL/H/5645–7

FIGURE 16. MODE 6b

2.0 Modes of Operation (Continued)

MODE 6c: Single Pole, AP, LP Filter (See *Figure 17*)

$f_c = \frac{f_{CLK}}{50}$ or $\frac{f_{CLK}}{100}$

$H_{OAP} = 1$ (as $f \rightarrow 0$)

$H_{OAP} = -1$ (as $f \rightarrow f_{CLK}/2$)

$H_{OLP} = -2$

$R_1 = R_2 = R_3$

MODE 7: Summing Integrator (See *Figure 18*)

τ = integrator time constant

$= \frac{16}{f_{CLK}}$ or $\frac{8}{f_{CLK}}$

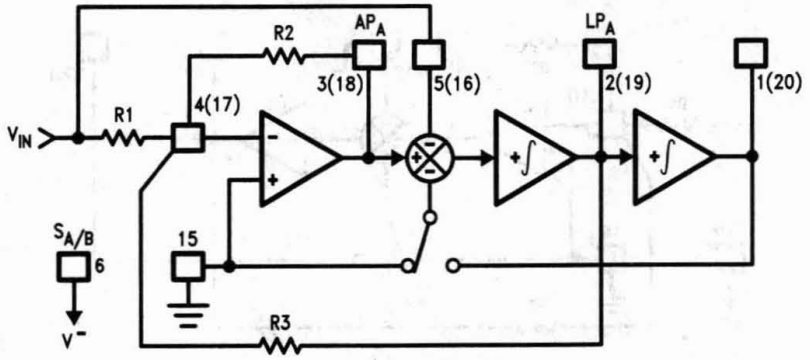


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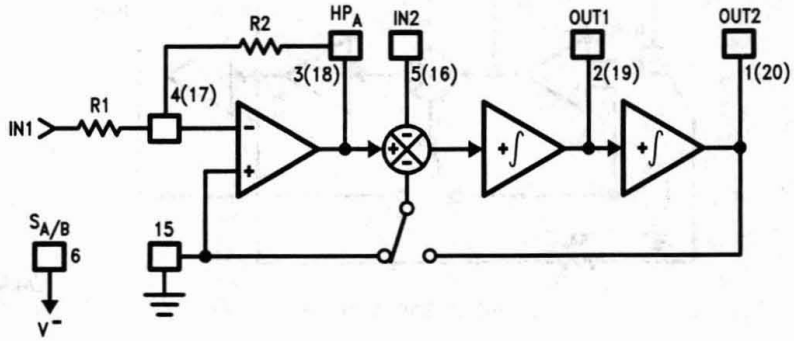
FIGURE 17. MODE 6c



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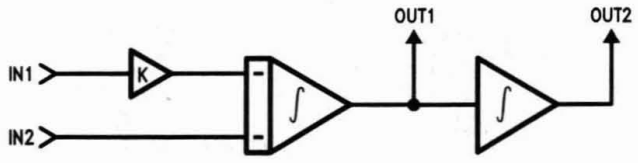
Equivalent Circuit



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$K = \frac{R_2}{R_1}$

$OUT1 = -\frac{k}{\tau}\int IN1\ dt - \frac{1}{\tau}\int IN2\ dt$

$OUT2 = \frac{1}{\tau}\int OUT1\ dt$

FIGURE 18. MODE 7

2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of Resistors	Adjustable f_{CLK}/f_0	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = +1$				2	No	May need input buffer. Poor dynamics for high Q.
1b	*	*		*		3	No	Useful for high frequency applications.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4	Yes	Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3	Yes	Single pole.
6b		(2) $H_{OLP1} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2	Yes	Single pole.
6c		*			*	3	No	Single pole.
7						2	Yes	Summing integrator with adjustable time constant.

3.0 Applications Information

The LMF100 is a general purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). The various clocking options are summarized in the following table.

Clocking Options

Power Supply	Clock Levels	LSh	V_D^+
−5V and +5V	TTL (0V to +5V)	0V	+5V
−5V and +5V	CMOS (−5V to +5V)	0V	+5V
0V and 10V	TTL (0V to 5V)	0V	+10V
0V and 10V	CMOS (0V to +10V)	+5V	+10V
−2.5V and +2.5V	CMOS (−2.5V to +2.5V)	0V	+2.5V
0V and 5V	TTL (0V to +5V)	0V	0V
0V and 5V	CMOS (0V to +5V)	+2.5V	+5V

By connecting pin 12 to the appropriate dc voltage, the filter center frequency, f_0, can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_0 can be very accurately set (within ±0.6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_0 ratio can be altered by external resistors as in *Figures 10, 11, 12, 13, 14, 15* and *16*. This is useful when high-order filters (greater than two) are to be realized by cascading the second-order sections. This allows each stage to be stagger tuned while using only one clock. The filter Q and gain are set by external resistor ratios.

All of the five second-order filter types can be built using either section of the LMF100. These are illustrated in *Figures 1* through *5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves.

3.0 Applications Information (Continued)

3.1 DESIGN EXAMPLE

In order to design a filter using the LMF100, we must define the necessary values of three parameters for each second-order section: f_0, the filter section's center frequency; H_0, the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at dc, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an LMF100. Many filter design texts (and National's Switched Capacitor Filter Handbook) include tables that list the characteristics (f_0 and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

$f_{0A} = 529$ Hz $\quad Q_A = 0.785$

$f_{0B} = 993$ Hz $\quad Q_B = 3.559$

For unity gain at dc, we also specify:

$H_{0A} = 1$

$H_{0B} = 1$

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust $\frac{f_{CLK}}{f_0}$ externally. From Table I, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: $R_{1A} = 20$k. The absolute value of the passband gain H_{OLPA} is made equal to 1 by choosing R_{4A} such that: $R_{4A} = -H_{OLPA}R_{1A} = R_{1A} = 20$k. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R_{2A} by:

$$R_{2A} = R_{4A}\frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6\text{k and}$$

$$R_{3A} = Q_A\sqrt{R_{2A}R_{4A}} = 0.785\sqrt{5.6 \times 10^3 \times 2 \times 10^4} = 8.3\text{k}$$

The resistors for the second section are found in a similar fashion:

$R_{1B} = 20$k

$R_{4B} = R_{1B} = 20$k

$$R_{2B} = R_{4B}\frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20\text{k}\frac{(993)^2}{(1000)^2} = 19.7\text{k}$$

$$R_{3B} = Q_B\sqrt{R_{2B}R_{4B}} = 3.559\sqrt{1.97 \times 10^4 \times 2 \times 10^4} = 70.6\text{k}$$

The complete circuit is shown in *Figure 19* for split ±5V power supplies. Supply bypass capacitors are highly recommended.

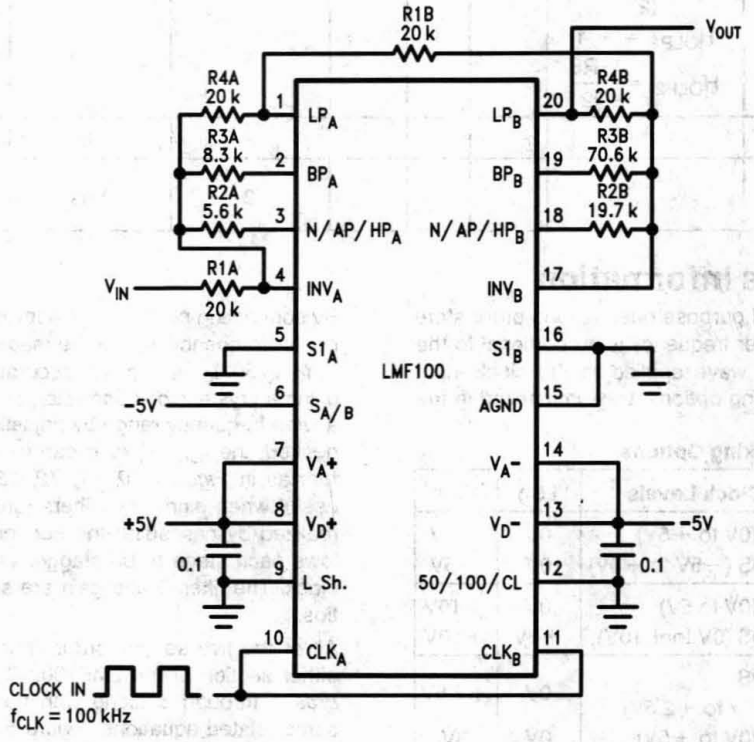

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FIGURE 19. Fourth-order Chebyshev low-pass filter from example in 3.1. ±5V power supply. 0V–5V TTL or ±5V CMOS logic levels.

3.0 Applications Information (Continued)

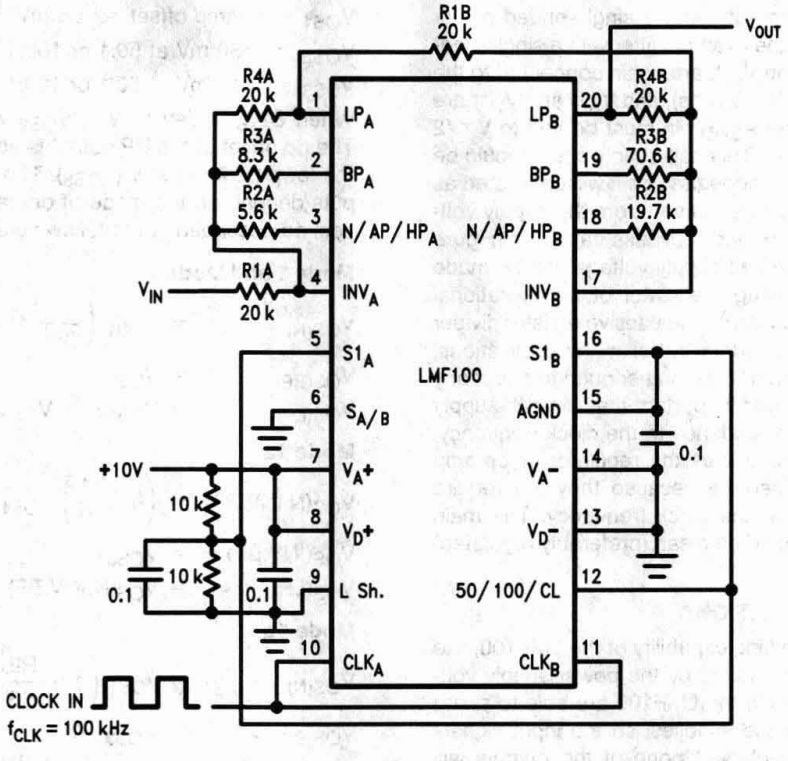
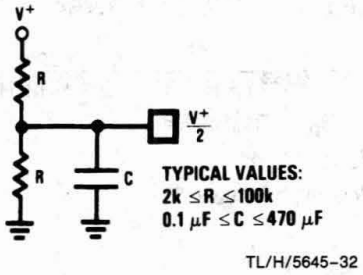
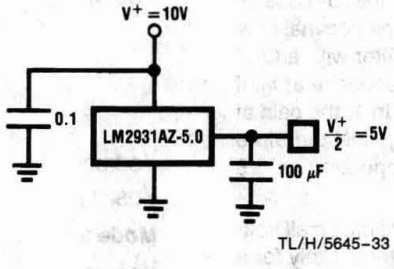


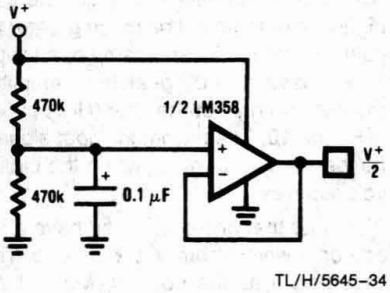
FIGURE 20. Fourth-order Chebyshev low-pass filter from example in 3.1. Single + 10V power supply. 0V–5V TTL logic levels. Input signals should be referred to half-supply or applied through a coupling capacitor.



(a) Resistive Divider with Decoupling Capacitor



(b) Voltage Regulator



(c) Operational Amplifier with Divider

FIGURE 21. Three Ways of Generating $\frac{V^+}{2}$ for Single-Supply Operation

3.0 Applications Information (Continued)

3.2 SINGLE SUPPLY OPERATION

The LMF100 can also operate with a single-ended power supply. *Figure 20* shows the example filter with a single-ended power supply. V_A^+ and V_D^+ are again connected to the positive power supply (4 to 15 volts), and V_A^- and V_D^- are connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor *(Figure 21a)*, or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier *(Figures 21b* and *21c)*. The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 μF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the LMF100, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the LMF100 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the LMF100 is operating on ± 5 volts, for example, the outputs will clip at about $8V_{p\text{-}p}$. The maximum input voltage multiplied by the filter gain should therefore be less than $8V_{p\text{-}p}$.

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain *(Figure 6)*. As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_0. If the nominal gain of the filter (H_{OLP}) is equal to 1, the gain at f_0 will be 10. The maximum input signal at f_0 must therefore be less than 800 $mV_{p\text{-}p}$ when the circuit is operated on ± 5 volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 *(Figure 7)*. The notch output will be very small at f_0, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_0 and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *17* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The LMF100's switched capacitor integrators have a slightly higher input offset voltage than found in a typical continuous time active filter integrator. Because of National's new LMCMOS process and new design techniques the internal offsets have been minimized, compared to the industry standard MF10. *Figure 22* shows an equivalent circuit of the LMF100 from which the output dc offsets can be calculated.

Typical values for these offsets with $S_{A/B}$ tied to V^+ are:

V_{OS1} = opamp offset = ± 5 mV

V_{OS2} = ± 30 mV at 50:1 or 100:1

V_{OS3} = ± 15 mV at 50:1 or 100:1

When $S_{A/B}$ is tied to V^-, V_{OS2} will approximately halve. The dc offset at the BP output is equal to the input offset of the lowpass integrator (V_{OS3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

Mode 1b

$$V_{OS(N)} = V_{OS1}\left(1 + \frac{R2}{R3} + \frac{R2}{R1}\right) - \frac{R2}{R3}V_{OS3}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = \frac{V_{OS(N)}}{2} - \frac{V_{OS2}}{2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{Rp} + 1\right)V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1+R4/R2} - \frac{V_{OS3}}{Q\sqrt{1+R2/R4}}$$

$$R_p = R1\|R3\|R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS1}\left[1 + \frac{R4}{R_p}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$$

$$R_p = R1\|R2\|R3$$

Mode 6a and 6c

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(LP)} = V_{OS1}\left(1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right) - \frac{R_3}{R_2}V_{OS2}$$

Mode 6b

$$V_{OS(LP\ (N.INV))} = V_{OS2}$$

$$V_{OS(LP\ (INV))} = V_{OS1}\left(1 + \frac{R_3}{R_2}\right) - \frac{R_3}{R_2}V_{OS2}$$

3.0 Applications Information (Continued)

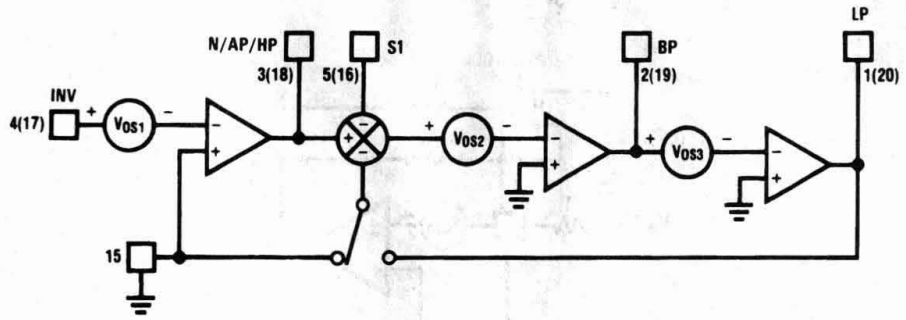


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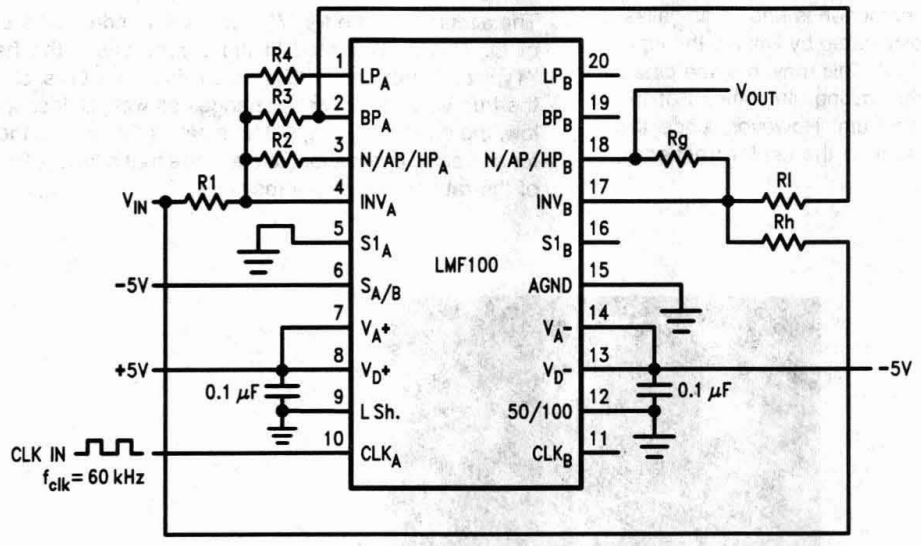
FIGURE 22. Offset Voltage Sources

In many applications, the outputs are ac coupled and dc offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_0 and Q. When operating in Mode 3, offsets can become excessively large if R_2 and R_4 are used to make f_{CLK}/f_0 significantly higher than the nominal value, especially if Q is also high.

For example, *Figure 23* shows a second-order 60 Hz notch filter. This circuit yields a notch with about 40 dB of attenuation at 60 Hz. A notch is formed by subtracting the bandpass output of a mode 3 configuration from the input using the unused side B opamp. The Q is 10 and the gain is 1 V/V in the passband. However, f_{CLK}/f_0 = 1000 to allow for a wide input spectrum. This means that for pin 12 tied to ground (100:1 mode), R4/R2 = 100. The offset voltage at the lowpass output (LP) will be about 3V. However, this is an extreme case and the resistor ratio is usually much smaller. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 24*. This allows adjustment of V_{OS1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{OS(BP)}$ in modes 1a and 3, for example).



R1 = 100 kΩ
R2 = 1 kΩ
R3 = 100 kΩ
R4 = 100 kΩ
Rg = 10 kΩ
RI = 10 kΩ
Rh = 10 kΩ

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FIGURE 23. Second-Order Notch Filter

3.0 Applications Information (Continued)

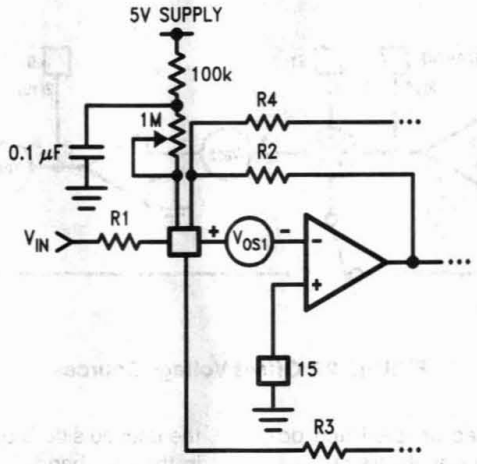

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FIGURE 24. Method for Trimming V_{OS}

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The LMF100 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The LMF100's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 100$ Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the LMF100 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate *(Figure 25)*. If necessary, these can be "smoothed" with a simple R-C low-pass filter at the LMF100 output.

The ratio of f_{CLK} to f_c (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise-sensitive applications, a ratio of 100:1 will result in 3 dB lower output noise for the same filter configuration.

The accuracy of the f_{CLK}/f_0 ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_0 will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

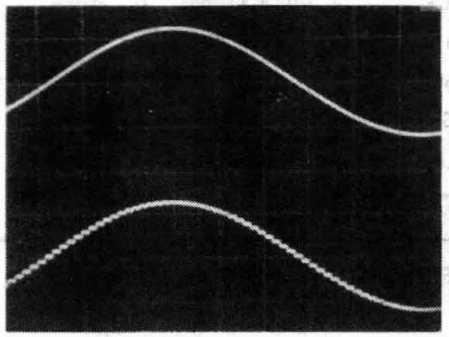

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FIGURE 25. The Sampled-Data Output Waveform

National Semiconductor

LMF380 Triple One-Third Octave Switched-Capacitor Active Filter

General Description

The LMF380 is a triple, one-third octave filter set designed for use in audio, audiological, and acoustical test and measurement applications. Built using advanced switched-capacitor techniques, the LMF380 contains three filters, each having a bandwidth equal to one-third of an octave in frequency. By combining several LMF380s, each covering a frequency range of one octave, a filter set can be implemented that encompasses the entire audio frequency range while using only a small fraction of the number of components and circuit board area that would be required if a conventional active filter approach were used. The center frequency range is not limited to the audio band, however. Center frequencies as low as 0.125 Hz or as high as 25 kHz are attainable with the LMF380.

The center frequency of each filter is determined by the clock frequency. The clock signal can be supplied by an external source, or it can be generated by the internal oscillator, using an external crystal and two capacitors. Since the LMF380 has an internal clock frequency divider ($\div 2$) and an output pin for the half-frequency clock signal, a single clock oscillator for the top-octave LMF380 becomes the master clock for the entire array of filters in a multiple LMF380 application.

Accuracy is enhanced by close matching of the internal components: the ratio of the clock frequency to the center frequency is typically accurate to $\pm 0.5\%$, and passband gain and stopband attenuation are guaranteed over the full temperature range.

Features

- Three bandpass filters with one-third octave center frequency spacing
- Choice of internal or external clock
- No external components other than clock or crystal and two capacitors

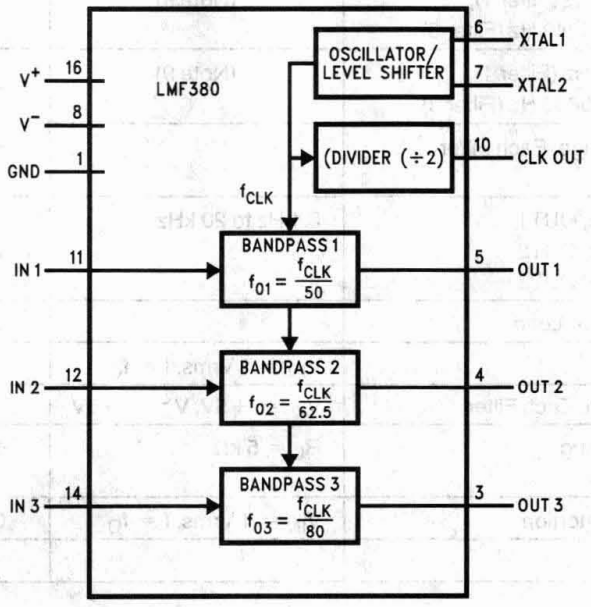
Key Specifications

- Passband gain accuracy: Better than 0.7 dB over temperature
- Supply voltage range: ± 2V to ± 7.5V or $+4$V to $+14$V

Applications

- Real-Time Audio Analyzers (ANSI Type E, Class II)
- Acoustical Instrumentation
- Noise Testing

Simplified Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	−0.3V to +16V
Voltage at Any Pin	V^- − 0.3V to V^+ + 0.3V
Input Current per Pin (Note 3)	±5 mA
Total Input Current (Note 3)	±20 mA
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	300°C
Surface Mount Package (Note 4)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Power Dissipation (Note 5)	500 mW
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 6)	2000V

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF380CIN, LMF380CIV, LMF380CIJ	$-40°C \le T_A \le +85°C$
LMF380CMJ	$-55°C \le T_A \le +125°C$
Supply Voltage ($V^+ - V^-$)	4.0V to 14V
Clock Input Frequency	10 Hz to 1.25 MHz

Filter Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$, and f_{CLK} = 320 kHz unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
$f_{CLK:f01}$	Clock-to-Center-Frequency Ratio, Filter 1		50:1		
$f_{CLK:f02}$	Clock-to-Center-Frequency Ratio, Filter 2		62.5:1		
$f_{CLK:f03}$	Clock-to-Center-Frequency Ratio, Filter 3		80:1		
A_1	Gain at f_1 = 3720 Hz (Filter 1), 2960 Hz (Filter 2), 2340 Hz (Filter 3)	(Note 9)	−32	**−30**	dB (max)
A_2	Gain at f_2 = 6080 Hz (Filter 1), 4820 Hz (Filter 2), 3820 Hz (Filter 3)	(Note 9)	+0.1	**0.1 ± 0.7**	dB (max)
A_3	Gain at f_3 = 6200 Hz (Filter 1), 4960 Hz (Filter 2), 3940 Hz (Filter 3)	(Note 9	0.0	**−0.0 ± 0.7**	dB (max)
A_4	Gain at f_4 = 6400 Hz (Filter 1), 5080 Hz (Filter 2), 4040 Hz (Filter 3)	(Note 9)	−0.2	**−0.2 ± 0.7**	dB (max)
A_5	Gain at f_5 = 6540 Hz (Filter 1), 5180 Hz (Filter 2), 4120 Hz (Filter 3)	(Note 9)	−0.1	**−0.1 ± 0.7**	dB (max)
A_6	Gain at f_6 = 6720 Hz (Filter 1), 5340 Hz (Filter 2), 4240 Hz (Filter 3)	(Note 9)	+0.15	**−0.15 ± 0.7**	dB (max)
A_7	Gain at f_7 = 8900 Hz (Filter 1), 7060 Hz (Filter 2), 5600 Hz (Filter 3)	(Note 9)	−22	**−20**	dB (max)
V_{OS}	Output Offset Voltage, Each Filter		+50	**+120** **−30**	mV (max) mV (min)
En	Total Output Noise, OUT1 Total Output Noise, OUT2 Total Output Noise, OUT3	0.1 Hz to 20 kHz	240 210 190		μVrms
C_L	Maximum Capacitive Load		200		pF
	Crosstalk	V_{IN} = 1 Vrms, f = f_O	−67		dB
	Clock Feedthrough, Each Filter	$V^+ = +5V$, $V^- = -5V$	10		mV_{p-p}
V_{OUT}	Output Voltage Swing	R_L = 5 kΩ	+4.2 −4.6	**+3.8** **−4.2**	V (min) V (max)
THD	Total Harmonic Distortion	V_{IN} = 1 Vrms, f = f_O	0.05		%
I_S	Supply Current		6.0	**9.0**	mA (max)

Logic Input and Output Electrical Characteristics

The following specifications for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits apply for $T_A = T_J = +25°C$.

Symbol	Parameter		Conditions	Typical (Note 7)	Tested Limit (Note 8)	Units (Limit)
V_{IH} V_{IL}	XTAL1 CMOS Clock Input Voltage	Logical "1" Logical "0"	$V^+ = 5V, V^- = -5V$		$+3.0$ -3.0	V (min) V (max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 10V, V^- = 0V$		$+8.0$ $+2.0$	V (min) V (max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 2.5V, V^- = -2.5V$		$+1.5$ -1.5	V (min) V (max)
V_{IH} V_{IL}		Logical "1" Logical "0"	$V^+ = 5V, V^- = 0V$		$+4.0$ $+1.0$	V (min) V (max)
V_{OH} V_{OL}	Clock Output Logical "1" Clock Output Logical "0"		$I_{OUT} = -1$ mA $I_{OUT} = +1$ mA		$V^+ - 1.0$ $V^- + 1.0$	V (min) V (max)
I_{IN}	Input Current XTAL1				± 20	μA (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > V^+$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 4: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any volume of the Linear Data Book Rev. 1 for other methods of soldering surface mount devices.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is a function of T_{Jmax}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation, $T_{Jmax} = 125°C$. The typical thermal resistance (θ_{JA}) of the LMF380N when board-mounted is 51°C.W. θ_{JA} is typically 52°C/W for the LMF380J, and 86°C/W for the LMF380V.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

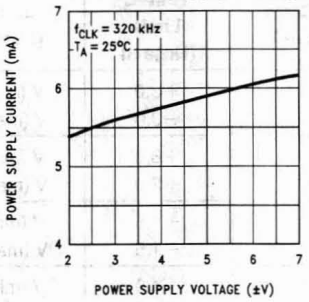
Note 7: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

Note 8: Limits are guaranteed to National's Averge Outgoing Quality Level (AOQL).

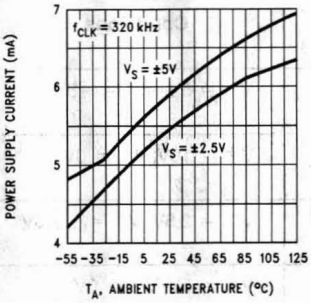
Note 9: The nominal test frequencies are: $f_1 = 0.58\ f_O$, $f_2 = 0.95\ f_O$, $f_3 = 0.98\ f_O$, $f_4 = f_O$, $f_5 = 1.02\ f_O$, $f_6 = 1.05\ f_O$, and $f_7 = 1.39\ f_O$. The actual test frequencies listed in the table may differ slightly from the nominal values.

Typical Performance Characteristics

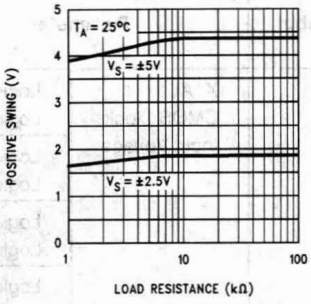
Power Supply Current vs Power Supply Voltage



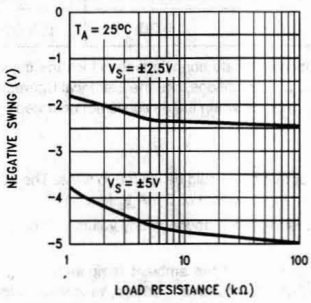
Power Supply Current vs Temperature



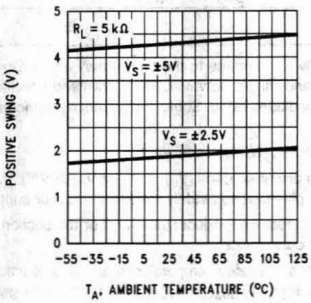
Positive Output Swing vs Load Resistance



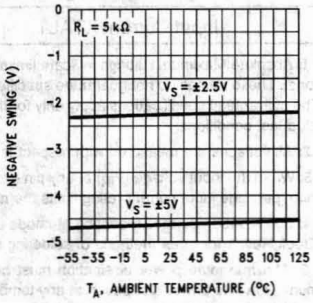
Negative Output Swing vs Load Resistance



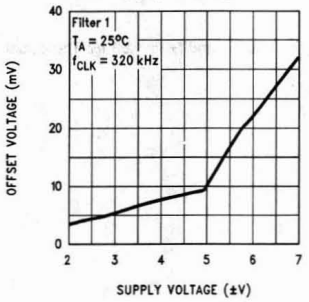
Positive Output Swing vs Temperature



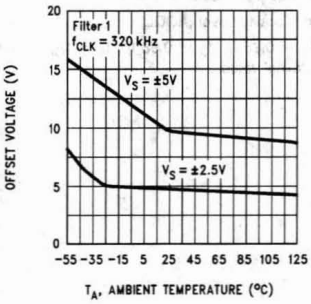
Negative Output Swing vs Temperature



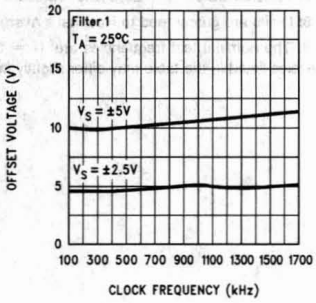
Offset Voltage vs Supply Voltage



Offset Voltage vs Temperature



Offset Voltage vs Clock Frequency



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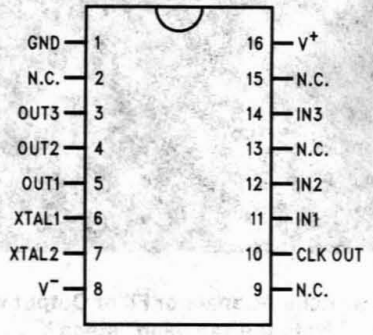
Connection Diagrams

Dual-In-Line Package

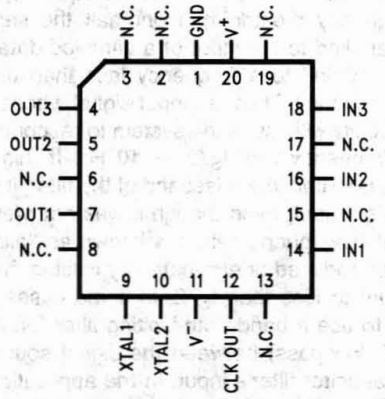


TL/H/11123-2

Top View

Order Number LMF380CIJ, LMF380CMJ or LMF380CIN
See NS Package Number J16A or N16E

Plastic Chip Carrier Package



TL/H/11123-3

Top View

Order Number LMF380CIV
See NS Package Number V20A

Pin Description

GND — This is the analog ground reference for the LMF380. In split supply applications, GND should be connected to the system ground. When operating the LMF380 from a single positive power supply voltage, pin 1 should be connected to a "clean" reference voltage midway between V^+ and V^-.

N.C. — These pins are not connected to the internal circuitry.

OUT1, OUT2, OUT3 — These are the outputs of the filters.

XTAL1 — This is the crystal oscillator input pin. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2. XTAL1 also serves as the input for an external CMOS-level clock.

XTAL2 — This is the output of the internal crystal oscillator. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2.

V^- — This is the negative power supply pin. It should be bypassed with at least a 0.1 μF ceramic capacitor. For best results, a 1.0 μF to 10.0 μF tantalum capacitor should also be used. For single-supply operation, connect this pin to system ground.

CLOCK OUT — This is the clock output pin. It can drive the clock inputs (XTAL1) of additional LMF380s or other components. The clock output frequency is one-half the clock frequency at XTAL1.

INPUT1, INPUT2, INPUT3 — These are the signal inputs to the filters.

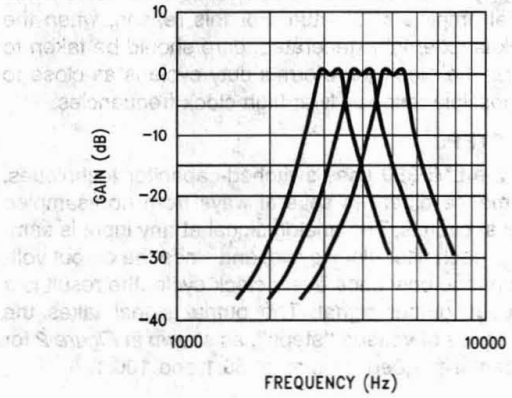
V^+ — This is the positive power supply pin. It should be bypassed with at least a 0.1 μF ceramic capacitor. For best results, a 1.0 μF to 10.0 μF tantalum capacitor should also be used.

Functional Description

The LMF380 contains three fourth-order Chebyshev bandpass filters whose center frequencies are spaced one-third of an octave apart, making it ideal for use in "real time" audio spectrum analysis applications. As with other switched-capacitor filters, the center frequencies are proportional to the clock frequency applied to the IC; the center frequencies of the LMF380's three filters are located at $f_{CLK}/50$, $f_{CLK}/62.5$, and $f_{CLK}/80$.

The three filters in an LMF380 cover a full octave in frequency, so that by using several LMF380s with clock frequencies separated by a factor of 2n, a complex audio program can be analyzed for frequency content over a range of several octaves. To facilitate this, the CLK OUT pin of the LMF380 supplies an output clock signal whose frequency is one-half that of the incoming clock frequency. Therefore, a single clock source can provide the clock reference for all of the 30 filters (10LMF380s) in a real time analyzer that covers the entire 10-octave audio frequency range. The LMF380 contains an internal clock oscillator that requires an external crystal and two capacitors to operate. Since the clock divider is on-board, only a single crystal is needed for the top-octave filter chip; the remaining devices can derive their clock signals from the master. If desired, an external oscillator can be used instead.

Figure 1 shows the magnitude versus frequency curves for the three filters in the LMF380. Separate input and output pins are provided for the three internal filters. The input pins will normally be connected to a common signal source, but can also be connected to separate input signals when necessary.



TL/H/11123-6

FIGURE 1. Response curves for the three filters in the LMF380. The clock frequency is 250 kHz.

7

Applications Information

POWER SUPPLIES

The LMF380 can operate from a total supply voltage ($V^+ - V^-$) ranging from 4.0V up to 14V, but the choice of supply voltage can affect circuit performance. The IC depends on MOS switches for its operation. All such switches have inherent "ON" resistances, which can cause small delays in charging internal capacitances. Increasing the supply voltage reduces this "ON" resistance, which improves the accuracy of the filter in high-frequency applications. The maximum practical center frequency improves by roughly 10% to 20% when the supply voltage increases from 5V to 10V.

Dynamic range is also affected by supply voltage. The maximum signal voltage swing capability increases as supply voltage increases, so the dynamic range is greater with higher power supply voltages. It is therefore recommended that the supply voltage be kept near the maximum operating voltage when dynamic range and/or high-frequency performance are important.

As with all switched-capacitor filters, each of the LMF380's power supply pins should be bypassed with a minimum of 0.1 μF located close to the chip. An additional 1 μF to 10 μF tantalum capacitor on each supply pin is recommended for best results.

Sampled-Data System Considerations

CLOCK CIRCUITRY

The LMF380's clock input circuitry accepts an external CMOS-level clock signal at XTAL1, or can serve as a self-contained oscillator with the addition of an external 1 MHz crystal and two 30 pF capacitors (see *Figure 3*).

The Clock Output pin provides a clock signal whose frequency is one-half that of the clock signal at XTAL1. This allows multiple LMF380s to operate from a single internal or external clock oscillator.

CLOCK FREQUENCY LIMITATIONS

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the time between clock cycles is relatively long, and small parasitic leakage currents cause the internal capacitors to discharge sufficiently to affect the filter's offset voltage and gain. This effect becomes more pronounced at elevated operating temperatures.

At higher clock frequencies, performance deviations are due primarily to the reduced time available for the internal operational amplifiers to settle. For this reason, when the filter clock is externally generated, care should be taken to ensure that the clock waveform's duty cycle is as close to 50% as possible, especially at high clock frequencies.

OUTPUT STEPS

Because the LMF380 uses switched-capacitor techniques, its performance differs in several ways from non-sampled (continuous) circuits. The analog signal at any input is sampled during each filter clock cycle, and since the output voltage can change only once every clock cycle, the result is a discontinuous output signal. The output signal takes the form of a series of voltage "steps", as shown in *Figure 2* for clock-to-center-frequency ratios of 50:1 and 100:1.

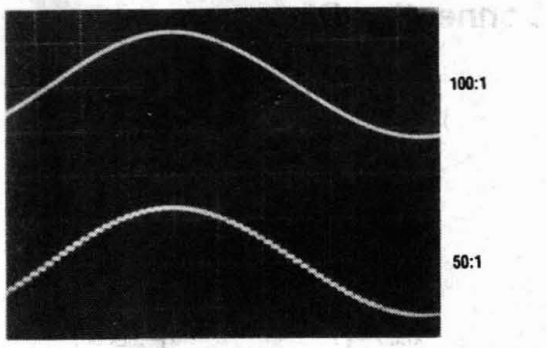


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FIGURE 2. Switched-Capacitor Filter Output Waveform. Note the sampling "steps".

ALIASING

Another important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency, f_S. (The LMF380's sampling frequency is the same as the filter clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_S/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_S/2 - 10$ Hz. If this frequency happens to be within the passband of the filter, it will appear at the filter's output, even though it was not present in the input signal. This phenomenon is known as "aliasing". Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_S/2$. In some cases, it may be necessary to use a bandwidth-limiting filter (often a simple passive RC low-pass) between the signal source and the switched-capacitor filter's input. In the application example shown in *Figure 3,* two LMF60 6th-order low-pass filters provide anti-aliasing filtering.

OFFSET VOLTAGE

Switched-capacitor filters often have higher offset voltages than non-sampling filters with similar topologies. This is due to charge injection from the MOS switches into the sampling and integrating capacitors. The LMF380's offset voltage ranges from a minimum of -30 mV to a maximum of $+120$ mV.

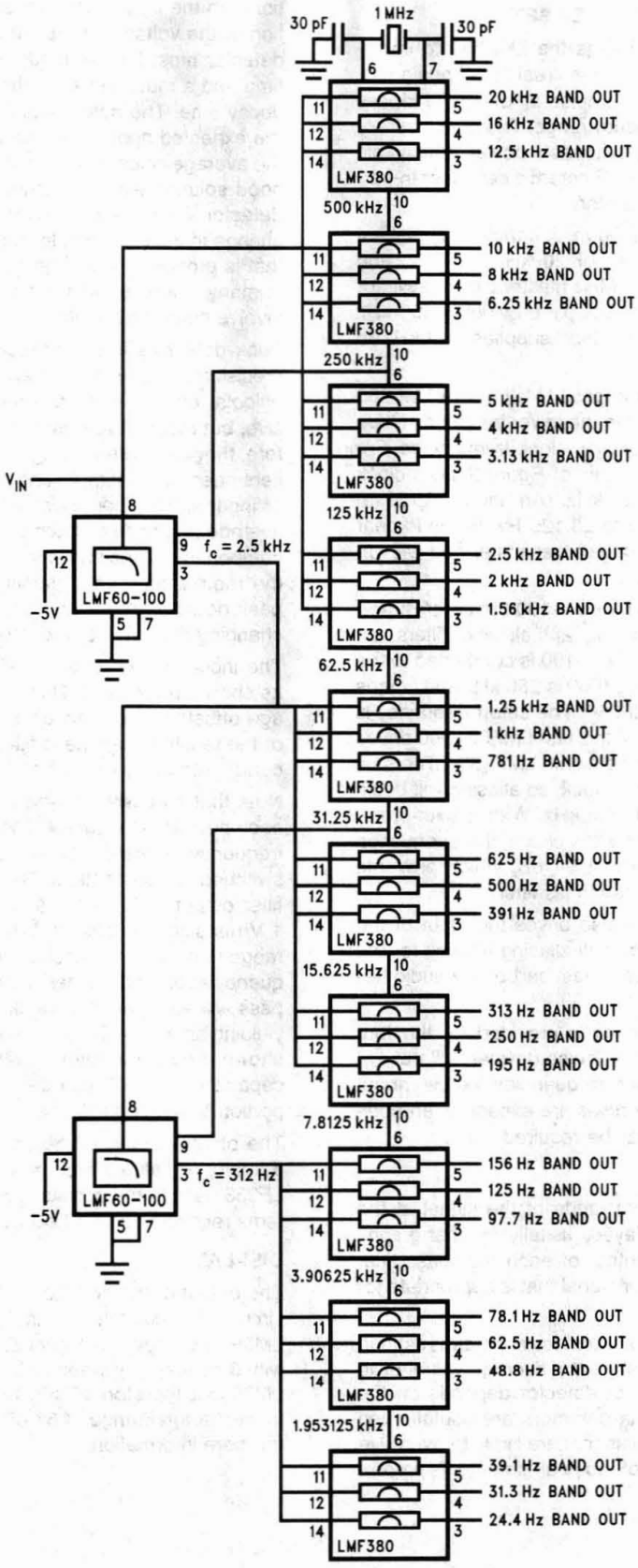
NOISE

Switched-capacitor filters have two kinds of noise at their outputs. There is a random, "thermal" noise component whose amplitude is typically on the order of 210 μV. The other kind of noise is digital clock feedthrough. This will have an amplitude in the vicinity of 10 mV peak-to-peak. In some applications, the clock noise frequency is so high compared to the signal frequency that it is unimportant. In other cases, clock noise may have to be removed from the output signal with, for example, a passive low-pass filter at the LMF380's output (see *Figure 4*).

INPUT IMPEDANCE

The LMF380's input pins are connected directly to the internal biquad filter sections. The input impedance is purely capacitive and is approximately 6.2 pF at each input pin, including package parasitics.

Typical Applications



TL/H/11123–7

FIGURE 3. Complete, one-third octave filter set for the entire audio frequency range. Ten LMF380s provide the thirty bandpass filters required for this function. Power supply connections and bypass capacitors are not shown. Pin numbers are for the dual-in-line package.

Typical Applications (Continued)

THIRD-OCTAVE ANALYZER FILTER SET

The circuit shown in *Figure 3* uses the LMF380 to implement a 1/3-octave filter set for use in "real time" audio program analyzers. Ten LMF380s provide all of the bandpass filtering for the full audio frequency range. The power supply connections are not shown, but each power supply pin should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 1 μF tantalum capacitor.

The first LMF380, at the top of *Figure 3,* handles the highest octave, with center frequencies of 20 kHz, 16 kHz, and 12.6 kHz. It also contains the 1 MHz master clock oscillator for the entire system. Its Clock Out pin provides a 500 kHz clock for the second LMF380, which supplies 250 kHz to the third LMF380, and so on.

If the audio input signal were applied to all of the LMF380 input pins, aliasing might occur in the lower frequency filters due to audio components near their clock frequencies. For example, the LMF380 at the bottom of *Figure 3* has a clock frequency equal to 1.953125 kHz. An input signal at 1.93 kHz will be aliased down to 23.125 Hz, which is near the band center of the 24.4 Hz bandpass filter and will appear at the output of that filter.

This problem is solved by two LMF60–100 6th order Butterworth low-pass filters serving as anti-aliasing filters, as shown in *Figure 3.* The first LMF60–100 is connected to the input signal. The clock for this LMF60 is 250 kHz and comes from pin 10 of the second LMF380. The cutoff frequency is therefore 2.5 kHz. The output of this first LMF60–100 drives the inputs of the fifth, sixth, and seventh LMF380s. The seventh LMF380 has a 15.625 kHz clock, so aliasing will begin to become a problem around 15.2 kHz. With a sixth-order, 2.5 kHz low-pass filter preceding this circuit, the attenuation at 15.2 kHz is theoretically about 94 dB, which prevents aliasing from occuring at this bandpass filter.

The output of the first LMF60 also drives the input of the second LMF60, which provides anti-aliasing filtering for the three LMF380s that handle the lowest part of the audio frequency spectrum.

Note that no anti-aliasing filtering is provided for the four LMF380s at the top of *Figure 3.* These devices will not encounter aliasing problems for frequencies below about 120 kHz; if higher input frequencies are expected, an additional low-pass filter at V_{IN} may be required.

DETECTORS

In a real-time analyzer, the amplitude of the signal at the output of each filter is displayed, usually in "bar-graph" form. The AC signal at the output of each bandpass filter must be converted to a unipolar signal that is appropriate for driving the display circuit.

The detector can take any of several forms. It can respond to the peaks of the input signal, to the average value, or to the rms value. The best type of detector depends on the application. For example, peak detectors are useful when monitoring audio program signals that are likely to overdrive an amplifier. Since the output of the peak detector is proportional to the peak signal voltage, it provides a good indication of the voltage swing. Generally, the output of the peak detector must have a moderately fast (about 1 ms) attack time and a much slower (tens or hundreds of milliseconds) decay time. The actual attack and decay times depend on the expected application. An average detector responds to the average value of the rectified input signal and provides a good solution when measuring random noise. An average detector will normally respond relatively slowly to a rapid change in input amplitude. An rms detector gives an output that is proportional to signal power, and is therefore useful in many instrumentation applications, especially those that involve complex signals.

Peak detectors and average-responding detectors require precision rectifiers to convert the bipolar input signal into a unipolar output. Half-wave rectifiers are relatively inexpensive, but respond to only one polarity of input signal; therefore, they can potentially ignore information. Full-wave rectifiers need more components, but respond to both polarities of input signal. Examples of half- and full-wave peak- and average-responding detectors are shown in *Figure 4.* The component values shown may need to be adjusted to meet the requirements of a particular application. For example, peak detector attack and decay times may be changed by changing the value of the "hold" capacitor.

The input to each detector should be capacitively-coupled as shown in *Figure 4.* This prevents any errors due to voltage offsets in the preceding circuitry. The cutoff frequency of the resulting high-pass filter should be less than half the center frequency of the band of interest.

Note that a passive low-pass filter is shown at the input to each detector in *Figure 4.* These filters attenuate any clock-frequency signals at the outputs of the third-octave switched-capacitor filters. The typical clock feedthrough at a filter output is 10 mV rms, or 40 dB down from a nominal 1 Vrms signal amplitude. When more than 40 dB dynamic range is needed, a passive low-pass filter with a cutoff frequency about three times the center frequency of the bandpass will attenuate the clock feedthrough by about 24 dB, yielding about 64 dB dynamic range. The component values shown produce a cutoff frequency of 1 kHz; changing the capacitor value will alter the cutoff frequency in inverse proportion to the capacitance.

The offset voltage of the operational amplifier used in the detector will also affect the detector's dynamic range. The LF353 used in the circuits in *Figure 3* is appropriate for systems requiring up to 40 dB dynamic range.

DISPLAYS

The output of the detector will drive the input of the display circuit. An example of an LED display driver using the LM3915 is shown in *Figure 5.* The LM3915 drives 10 LEDs with 3 dB steps between LEDs; the total display range for an LM3915 is therefore 27 dB. Two LM3915s can be cascaded to yield a total range of 57 dB. See the LM3915 data sheet for more information.

Typical Applications (Continued)

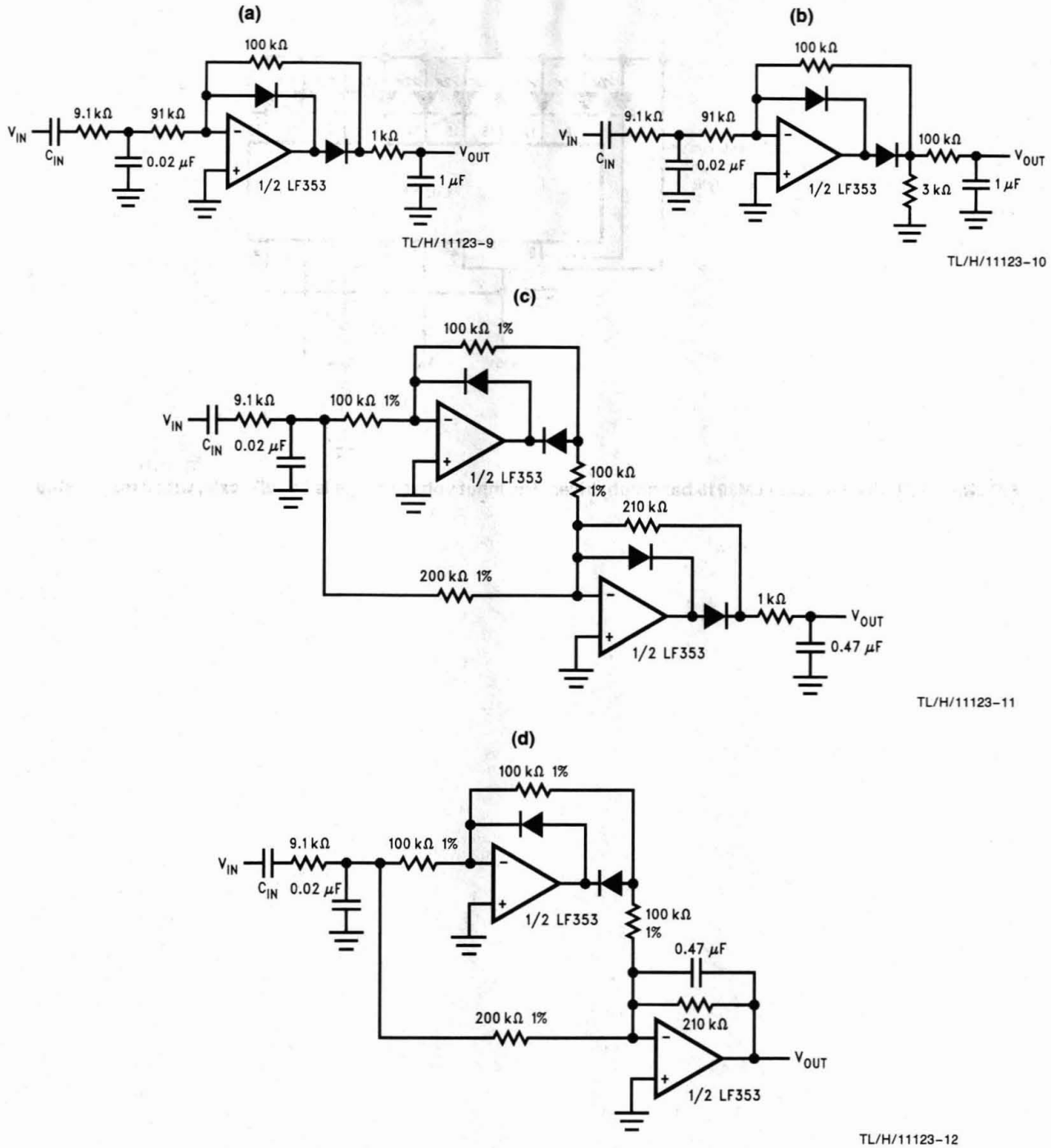


FIGURE 4. Examples of detectors for audio signals. (a) Half-wave peak detector. (b) Half-wave average detector. (c) Full-wave peak detector. (d) Full-wave average detector. All diodes are 1N914 or 1N4148. Input RC low-pass filters attenuate clock noise from switched-capacitor filters; values shown are for 1 kHz cutoff frequency. C_{IN} should be at least 0.27 μF for frequency bands below 50 Hz and 0.1 μF for higher frequencies. Power supplies (not shown) should be bypassed with at least 0.1 μF close to the amplifiers.

Typical Applications (Continued)

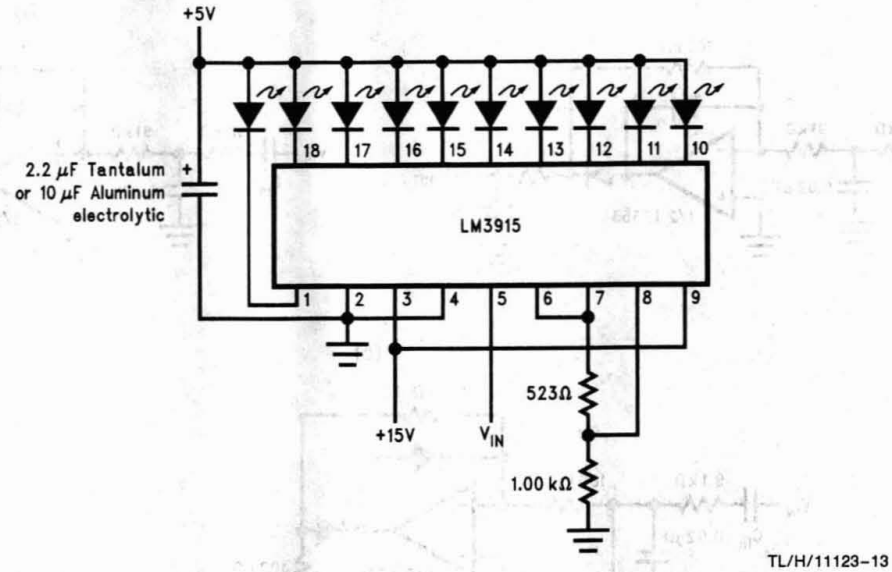


FIGURE 5. LED display using LM3915 bar graph driver. The input voltage range is 2V full-scale, with 3 dB per step.

National Semiconductor

MF4 4th Order Switched Capacitor Butterworth Lowpass Filter

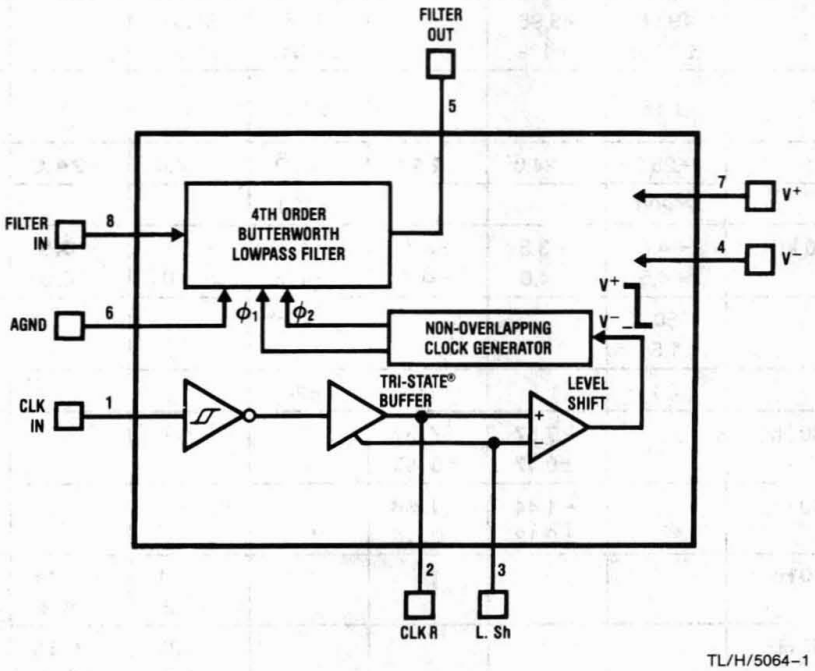
General Description

The MF4 is a versatile, easy to use, precision 4th order Butterworth low-pass filter. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50 to 1 (MF4-50) or 100 to 1 (MF4-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control an external TTL or CMOS logic compatible clock can be applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF4 sections together for higher order filtering.

Features

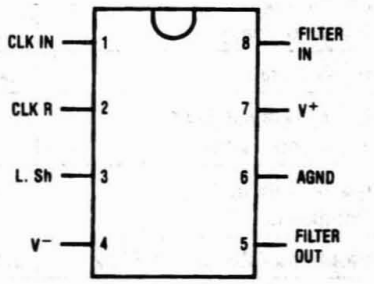
- Low Cost
- Easy to use
- 8-pin mini-DIP or 14-pin wide-body S.O.
- No external components
- 5V to 14V supply voltage
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Cutoff frequency accuracy of ± 0.3% typical
- Cutoff frequency set by external clock
- Separate TTL and CMOS/Schmitt-trigger clock inputs

Block and Connection Diagrams



TL/H/5064–1

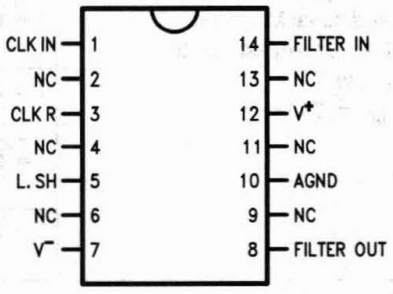
Dual-In-Line Package



TL/H/5064–2

Order Number MF4CN-50
or MF4CN-100
See NS Package Number N08E

Small-Outline
Wide-Body Package



TL/H/5064–25

Top View
Order Number MF4CWM-50
or MF4CWM-100
See NS Package Number M14B

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Voltage At Any Pin	$V^+ + 0.2V$ $V^- - 0.2V$
Input Current at Any Pin (Note 14)	5 mA
Package Input Current (Note 14)	20 mA
Power Dissipation (Note 15)	500 mW
Storage Temperature	150°C
ESD Susceptibility (Note 13)	800 V

Soldering Information:

- N Package: 10 sec. 260°C
- SO Package: Vapor Phase (60 sec.) 215°C
  Infrared (15 sec.) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Note 2)

Temperature Range	$T_{min} \le T_A \le T_{max}$
MF4CN-50, MF4CN-100	$0°C \le T_A \le 70°C$
MF4CWM-50, MF4CWM-100	$0°C \le T_A \le 70°C$
Supply Voltage ($V^+ - V^-$)	5V to 14V

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \le 250$ kHz (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF4-50 Typical (Note 10)	MF4-50 Tested Limit (Note 11)	MF4-50 Design Limit (Note 12)	MF4-100 Typical (Note 10)	MF4-100 Tested Limit (Note 11)	MF4-100 Design Limit (Note 12)	Unit
$V^+ = +5V, V^- = -5V$								
f_c, Cutoff Frequency Range (Note 3) Min				0.1			0.1	Hz
f_c, Cutoff Frequency Range (Note 3) Max				20k			10k	Hz
Supply Current	$f_{clk} = 250$ kHz	2.5	3.5	**3.5**	2.5	3.5	**3.5**	mA
Maximum Clock Feedthrough (Peak-to-Peak) Filter Output	$V_{in} = 0V$	25			25			mV
H_O, DC Gain	$R_{source} \le 2$ kΩ	0.0	±0.15	**±0.15**	0.0	±0.15	**±0.15**	dB
f_{clk}/f_c, Clock to Cutoff Frequency Ratio		49.96 ±0.3%	49.96 ±1%		99.09 ±0.3%	99.09 ±1.0%		
f_{clk}/f_c Temperature Coefficient		±15			±30			ppm/°C
Stopband Attenuation (Min)	at 2 f_c	−25.0	−24.0	**−24.0**	−25.0	−24.0	**−24.0**	dB
DC Offset Voltage		−200			−400			mV
Minimum Output Swing	$R_L = 10$ kΩ	+4.0 −4.5	+3.5 −4.0	**+3.5** **−4.0**	+4.0 −4.5	+3.5 −4.0	**+3.5** **−4.0**	V V
Output Short Circuit Current (Note 8) Source		50			50			mA
Output Short Circuit Current (Note 8) Sink		1.5			1.5			mA
Dynamic Range (Note 4)		80			82			dB
Additional Magnitude Response Test Points (Note 6) $f_{clk} = 250$ kHz	f = 6000 Hz		−7.57 ±0.47	**−7.57** **±0.47**				dB
	f = 4500 Hz		−1.44 ±0.12	**−1.44** **±0.12**				dB
	f = 3000 Hz					−7.21 ±0.2	**−7.21** **±0.2**	dB
	f = 2250 Hz					−1.39 ±0.1	**−1.39** **±0.1**	dB

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \leq 250$ kHz (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Parameter		Conditions	MF4-50			MF4-100			Unit
			Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	
$V^+ = +2.5V, V^- = -2.5V$									
f_c Cutoff Frequency Range (Note 3)	min max				0.1 10k			0.1 5k	Hz
Supply Current		$f_{clk} = 250$ kHz	1.5	2.25	**2.25**	1.5	2.25	**2.25**	mA
Maximum Clock Feedthrough (Peak-to-Peak)	Filter Output	$V_{in} = 0V$	15			15			mV
H_o, DC Gain		$R_{source} \leq 2$ kΩ	0.0	±0.15	**±0.15**	0.0	±0.15	**±0.15**	dB
f_{clk}/f_c, Clock to Cutoff Frequency Ratio			50.07 ±0.3%	50.07 ±1.0%		99.16 ±0.3%	99.16 ±1.0%		
f_{CLK}/f_C Temperature Coefficient			±25			±60			ppm/°C
Stopband Attenuation (Min)		at 2 f_c	−25.0	−24.0	**−24.0**	−25.0	−24.0	**−24.0**	dB
DC Offset Voltage			−150			−300			mV
Minimum Output Swing		$R_L = 10$ kΩ	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.7**	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.7**	V V
Output Short Circuit Current (Note 8)	Source Sink		28 0.5			28 0.5			mA mA
Dynamic Range (Note 4)			78			78			dB
Additional Magnitude Response Test Points (Note 6) (f_c = 5 kHz) Magnitude at		$f_{clk} = 250$ kHz f = 6000 Hz		−7.57 ±0.47	**−7.57** **±0.47**				dB
		f = 4500 Hz		−1.46 ±0.12	**−1.46** **±0.12**				dB
(f_c = 2.5 kHz) Magnitude		f = 3000 Hz					−7.21 ±0.2	**−7.21** **±0.2**	dB
		f = 2250 Hz					−1.39 ±0.1	**−1.39** **±0.1**	

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (see Note 7) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions	Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
SCHMITT TRIGGER						
V_{T+}, Positive Going Threshold Voltage	Min Max	$V^+ = 10V$	7.0	6.1	**6.1** **8.9**	V
	Min Max	$V^+ = 5V$	3.5	3.1 4.4	**3.1** **4.4**	V

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (see Note 7) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = t_J = 25°C$. (Continued)

Parameter		Conditions		Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
SCHMITT TRIGGER (Continued)							
V_{T-}, Negative Going Threshold Voltage	Min	$V^+ = 10V$		3.0	1.3	**1.3**	V
	Max				3.8	**3.8**	
	Min	$V^+ = 5V$		1.5	0.6	**0.6**	V
	Max				1.9	**1.9**	
Hysteresis ($V_{T+} - V_{T-}$)	Min	$V^+ = 10V$		4.0	2.3	**2.3**	V
	Max				7.6	**7.6**	
	Min	$V^+ = 5V$		2.0	1.2	**1.2**	V
	Max				3.8	**3.8**	
Minimum Logical "1" Output Voltage (pin 2)		$I_0 = -10\ \mu A$	$V^+ = 10V$		9.0	**9.0**	V
			$V^+ = 5V$		4.5	**4.5**	V
Maximum Logical "0" Output Voltage (pin 2)		$I_0 = 10\ \mu A$	$V^+ = 10V$		1.0	**1.0**	V
			$V^+ = 5V$		0.5	**0.5**	V
Minimum Output Source Current (pin 2)		CLK R Shorted to Ground	$V^+ = 10V$	6.0	3.0	**3.0**	mA
			$V^+ = 5V$	1.5	0.75	**0.75**	mA
Maximum Output Sink Current (pin 2)		CLK R Shorted to V^+	$V^+ = 10V$	5.0	2.5	**2.5**	mA
			$V^+ = 5V$	1.3	0.65	**0.65**	mA
TTL CLOCK INPUT, CLK R PIN (Note 9)							
Maximum V_{IL}, Logical "0" Input Voltage				0.8			V
Minimum V_{IH}, Logical "1" Input Voltage				2.0			V
Maximum Leakage Current at CLK R Pin		L. Sh Pin at Mid-Supply		2.0			μA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. AC and DC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to GND.

Note 3: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 4: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 280 μVrms for the MF4-50 and 230 μVrms for the MF4-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically 130 μVrms for both the MF4-50 and the MF4-100.

Note 5: The specifications for the MF4 have been given for a clock frequency (f_{CLK}) of 250 kHz or less. Above ths clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 6: Besides checking the cutoff frequency (f_c) and the stopband attenuation at 2 f_c, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

Note 7: For simplicity all the logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 8: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 9: The MF4 is operating with symmetrical split supplies and L. Sh is tied to ground.

Note 10: Typicals are at 25°C and represent most likely parametric norm.

Note 11: Guaranteed to National's Average Outgoing Quality Level (AOOL).

Note 12: Guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Note 13: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 14: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

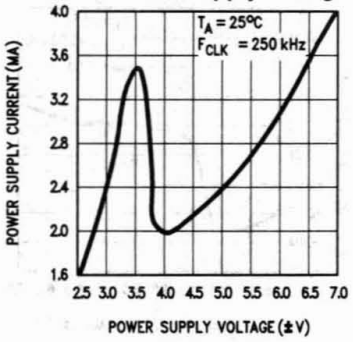
Note 15: Thermal Resistance

θ_{JA} (Junction to Ambient) N Package . . . . . 105°C/W.

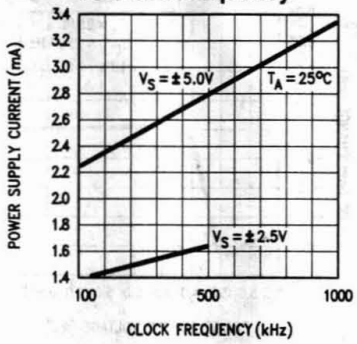
θ_{JA} M Package . . . . . 95°C/W.

Typical Performance Characteristics

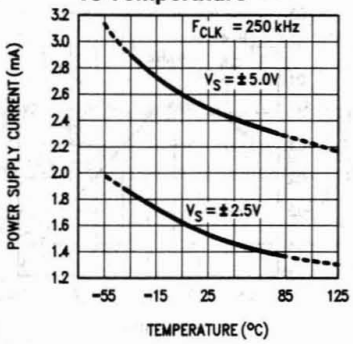
Power Supply Current vs Power Supply Voltage



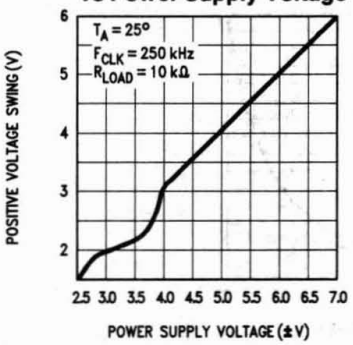
Power Supply Current vs Clock Frequency



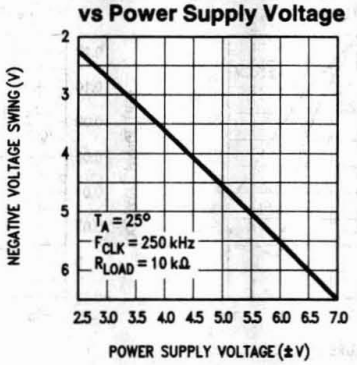
Power Supply Current vs Temperature



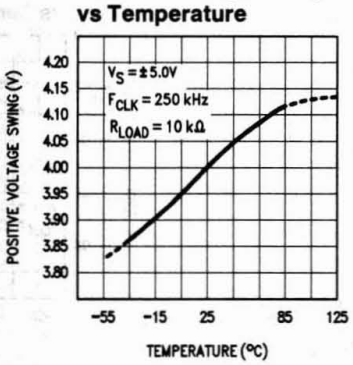
Positive Voltage Swing vs Power Supply Voltage



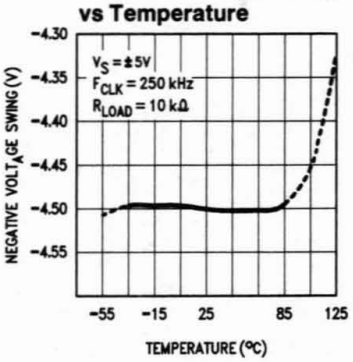
Negative Voltage Swing vs Power Supply Voltage



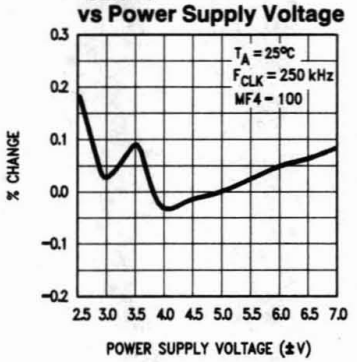
Positive Voltage Swing vs Temperature



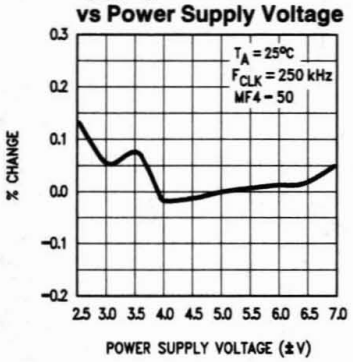
Negative Voltage Swing vs Temperature



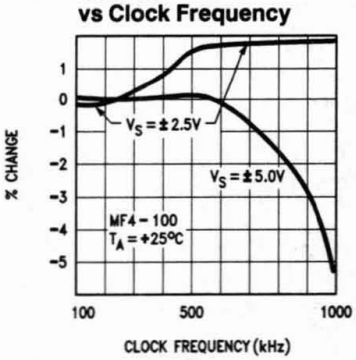
f_{CLK}/f_c Deviation vs Power Supply Voltage



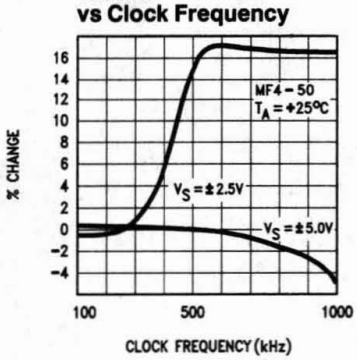
f_{CLK}/f_c Deviation vs Power Supply Voltage



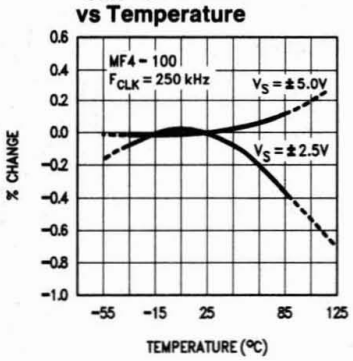
f_{CLK}/f_c Deviation vs Clock Frequency



f_{CLK}/f_c Deviation vs Clock Frequency



f_{CLK}/f_c Deviation vs Temperature



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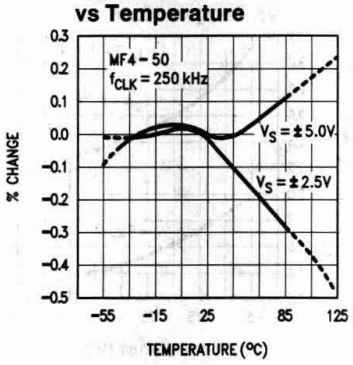
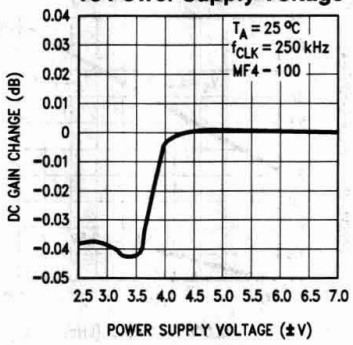
Typical Performance Characteristics (Continued)

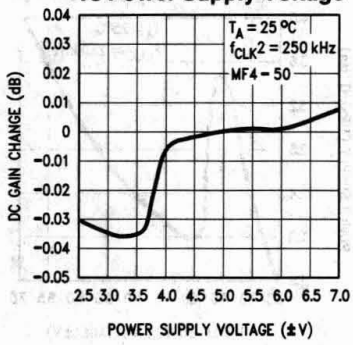
f_{CLK}/f_c Deviation vs Temperature



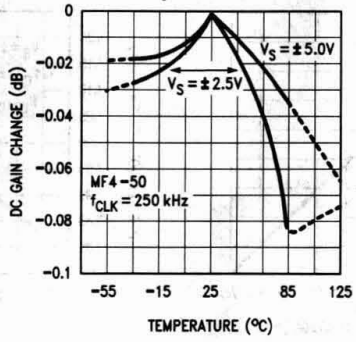
DC Gain Deviation vs Power Supply Voltage



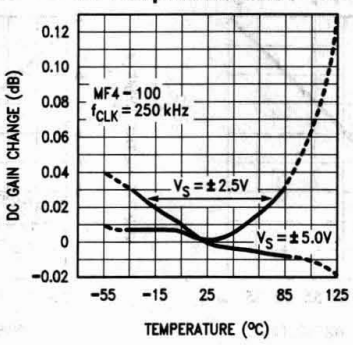
DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



DC Gain Deviation vs Temperature



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Pin Descriptions

(Numbers in ( ) are for 14-pin package.)

Pin #	Pin Name	Function
1 (1)	CLK IN	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self clocking Schmitt-trigger oscillator (see section 1.1).
2 (3)	CLK R	A TTL logic level clock input when in split supply operation (±2.5V to ±7V) with L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see section 1.1). The TTL input signal must not exceed the supply voltages by more than 0.2V.
3 (5)	L. Sh	Level shift pin; selects the logic threshold levels for the clock. When tied to V^- it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds 25% $(V^+ - V^-) + V^-$ the internal tri-state buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level-shift stage. The CLK R threshold level is now 2V above the voltage on the L. Sh pin. The CLK R pin will be compatible with TTL logic levels when the MF4 is operated on split supplies with the L. Sh pin connected to system ground.
5 (8)	FILTER OUT	The output of the low-pass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.
6 (10)	AGND	The analog ground pin. This pin sets the DC bias level for the filter section and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.
7, 4 (7, 12)	V^+, V^-	The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
8 (14)	FILTER IN	The input to the low-pass filter. To minimize gain errors the source impedance that drives this input should be less than 2K (see section 1.3 of the Application Hints). For single supply operation the input signal must be biased to mid-supply or AC coupled through a capacitor.

1.0 MF4 Application Hints

The MF4 is a non-inverting unity gain low-pass fourth-order Butterworth switched-capacitor filter. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock-to-cutoff-frequency ratio ($f_{CLK}f_c$) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock-to-cutoff-frequency ratio the closer this approximation is to the theoretical Butterworth response. The MF4 is available in f_{CLK}/f_c ratios of 50:1 (MF4-50) or 100:1 (MF4-100).

1.1 CLOCK INPUTS

The MF4 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. Pin 3 is connected to V^- which makes Pin 2 a low impedance output. The oscillator's frequency is nominally

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]} \quad (1)$$

which, is typically

$$f_{CLK} \cong \frac{1}{1.69\,RC} \quad (1a)$$

for $V_{CC} = 10V$.

Note that f_{CLK} is dependent on the buffer's threshold levels as well as the resistor/capacitor tolerance (see *Figure 1*). Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accurate cutoff frequency is required, an external clock can be used to drive the CLK R input of the MF4. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 μA). With split supplies and the level shift (L. Sh) tied to system ground, the logic level is about 2V. (See the Pin Description for L. Sh).

1.2 POWER SUPPLY

The MF4 can be powered from a single supply or split supplies. The split supply mode shown in *Figure 2* is the most flexible and easiest to implement. Supply voltages of ±5V to ±7V enable the use of TTL or CMOS clock logic levels. *Figure 3* shows AGND resistor-biased to $V^+/2$ for single supply operation. In this mode only CMOS clock logic levels can be used, and input signals should be capacitor-coupled or biased near mid-supply.

1.3 INPUT IMPEDANCE

The MF4 low-pass filter input (FILTER IN) is not a high impedance buffer input. This input is a switched-capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the filter's input can be seen in *Figure 4*. The input capacitor charges to V_{in} during the first half of the clock period; during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{in}V_{in}$, and since current is defined as the flow of charge per unit time, the average input current becomes

$$I_{in} = Q/T$$

1.0 MF4 Application Hints (Continued)

(where T equals one clock period) or

$$I_{in} = \frac{C_{in}V_{in}}{T} = C_{in}V_{in}f_{CLK}$$

The equivalent input resistor (R_{in}) then can be expressed as

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{C_{in}f_{CLK}}$$

The input capacitor is 2 pF for the MF4-50 and 1 pF for the MF4-100, so for the MF4-100

$$R_{in} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{in} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the MF4-50. The above equation shows that for a given cutoff frequency (f_c), the input resistance of the MF4-50 is the same as that of the MF4-100. The higher the clock-to-cutoff-frequency ratio, the greater equivalent input resistance for a given clock frequency.

This input resistance will form a voltage divider with the source impedance (R_{source}). Since R_{in} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity, the overall gain is given by:

$$A_v = \frac{R_{in}}{R_{in} + R_{source}}$$

If the MF4-50 or the MF-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{in} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

In this example with a source impedance of 10K the overall gain, if the MF4 had an ideal gain of 1 or 0 dB, would be:

$$A_v = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009 \text{ or } -0.086\ \text{dB}$$

Since the maximum overall gain error for the MF4 is ±0.15 dB with $R_s \leq 2\ \text{k}\Omega$ the actual gain error for this case would be +0.06 dB to −0.24 dB.

1.4 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit due to leakage currents through the internal switches draining the charge stored on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ \text{Hz}, I_{leakage} = 1\ \text{pA}, C = 1\ \text{pF}$$

$$V = \frac{1\ \text{pA}}{1\ \text{pF (100 Hz)}} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors limit the filter's accuracy at high clock frequencies. The amplitude characteristic on ±5V supplies will typically stay flat until f_{CLK} exceeds 750 kHz and then peak at about 0.5 dB at the corner frequency with a 1 MHz clock. As supply voltage drops to ± 2.5V, a shift in the f_{CLK}/f_c ratio occurs which will become noticeable when the clock frequency exceeds 250 kHz. The response of the MF4 is still a good approximation of the ideal Butterworth low-pass characteristic shown in *Figure 5*.

2.0 Designing With The MF4

Given any low-pass filter specification, two equations will come in handy in trying to determine whether the MF4 will do the job. The first equation determines the order of the low-pass filter required to meet a given response specification:

$$n = \frac{\log\left[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)\right]}{2\log(f_s/f_b)} \quad (2)$$

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at cutoff frequency f_b. If the result of this equation is greater than 4, more than a single MF4 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10\log\left[1 + (10^{0.1A_{max}} - 1)(f/f_b)^{2n}\right]\ \text{dB} \quad (3)$$

where n = 4 for the MF4.

2.1 A LOW-PASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 6* is given. Can the MF4 be used? The order of the Butterworth approximation will have to be determined using (1):

A_{min} = 18 dB, A_{max} = 1.0 dB, f_s = 2 kHz, and f_b = 1 kHz

$$n = \frac{\log\left[(10^{1.8} - 1)/(10^{0.1} - 1)\right]}{2\log(2)} = 3.95$$

Since n can only take on integer values, n = 4. Therefore the MF4 can be used. In general, if n is 4 or less a single MF4 stage can be utilized.

Likewise, the attenuation at f_s can be found using (3) with the above values and n = 4:

$\text{Attn (2 kHz)} = 10\log\left[1 + 10^{0.1} - 1)(2\ \text{kHz}/1\ \text{kHz})^8\right] =$ 18.28 dB

This result also meets the design specification given in *Figure 6* again verifying that a single MF4 section will be adequate.

Since the MF4's cutoff frequency (f_c), which corresponds to a gain attenuation of −3.01 dB, was not specified in this example, it needs to be calculated. Solving equation 3 where $f = f_c$ as follows:

$$f_c = f_b\left[\frac{(10^{0.1(3.01\ \text{dB})} - 1}{(10^{0.1A_{max}} - 1)}\right]^{1/(2n)}$$

$$= 1\ \text{kHz}\left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/8}$$

$$= 1.184\ \text{kHz}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$. To implement this example for the MF4-50 the clock frequency will have to be set to f_{CLK} = 50(1.184 kHz) = 59.2 kHz, or for the MF4-100, f_{CLK} = 100 (1.184 kHz) = 118.4 kHz.

2.2 CASCADING MF4s

When a steeper stopband attenuation rate is required, two MF4s can be cascaded (*Figure 7*) yielding an 8th order

2.0 Designing With The MF4 (Continued)

slope of 48 dB per octave. Because the MF4 is a Butterworth filter and therefore has no ripple in its passband when MF4s are cascaded, the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 9*.

In determining whether the cascaded MF4s will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log[(10^{0.05A_{min}} - 1)/(10.^{0.05A_{max}} - 1)]}{2 \log (f_s/f_c)} \quad (2)$$

$$\text{Attn}(f) = 10 \log [1 + (10^{0.05A_{max}} - 1)(f/f_c)^2] \text{ dB} \quad (3)$$

where $n = 4$ (the order of each filter).

Equation 2 will determine whether the order of the filter is adequate ($n \leq 4$) while equation 3 can determine the actual stopband attenuation and cutoff frequency (f_c) necessary to obtain the desired frequency response. The design procedure would be identical to the one shown in section 2.0.

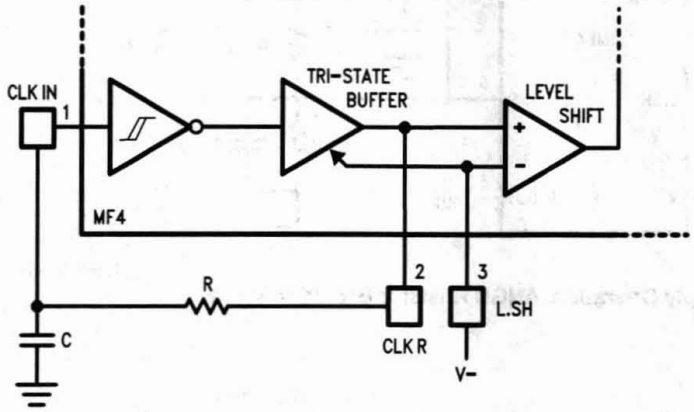
2.3 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF4 will respond favorably to an instantaneous change in clock frequency. If the control signal in *Figure 9* is low the MF4-50 has a 100 kHz clock making $f_c = 2$ kHz; when this signal goes high the clock frequency changes to 50 kHz yielding $f_c = 1$ kHz. As the Figure illustrates, the output signal changes quickly and smoothly in response to a sudden change in clock frequency.

The step response of the MF4 in *Figure 10* is dependent on f_c. The MF4 responds as a classical fourth-order Butterworth low-pass filter.

2.4 ALIASING CONSIDERATIONS

Aliasing effects have to be considered when input signal frequencies exceed half the sampling rate. For the MF4 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency $f_{CLK}/2$, as in *Figure 11a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range below $f_{CLK}/2$, as in *Figure 11b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore, if frequency components in the input signal exceed $f_{CLK}2$ they must be attenuated before being applied to the MF4 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level.



$$f = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

$$f \cong \frac{1}{1.69\,RC}$$

$(V_{CC} = 10V)$

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FIGURE 1. Schmitt Trigger R/C Oscillator

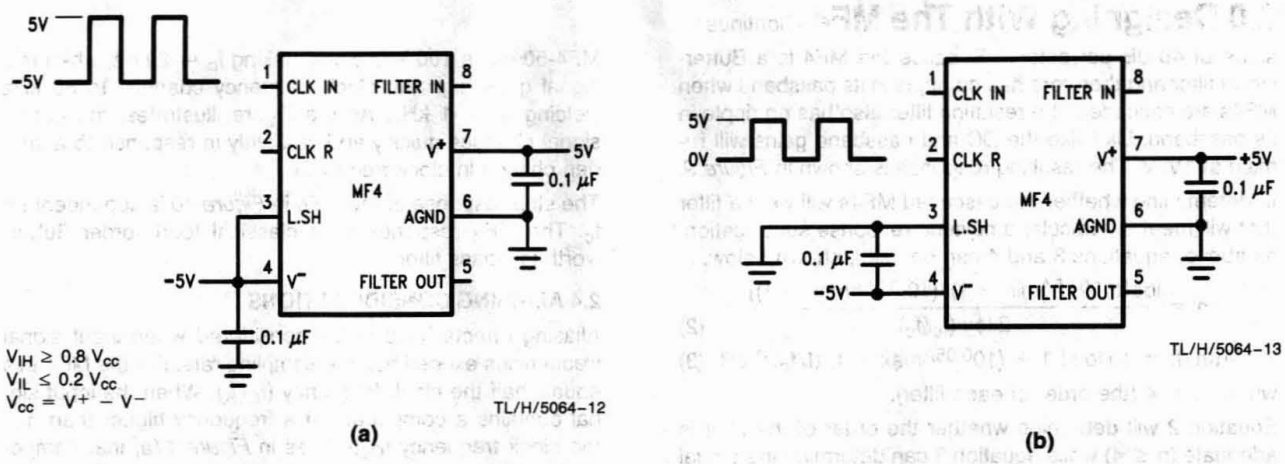


FIGURE 2. Split Supply Operation with CMOS Level Clock (a) and TTL Level Clock (b)

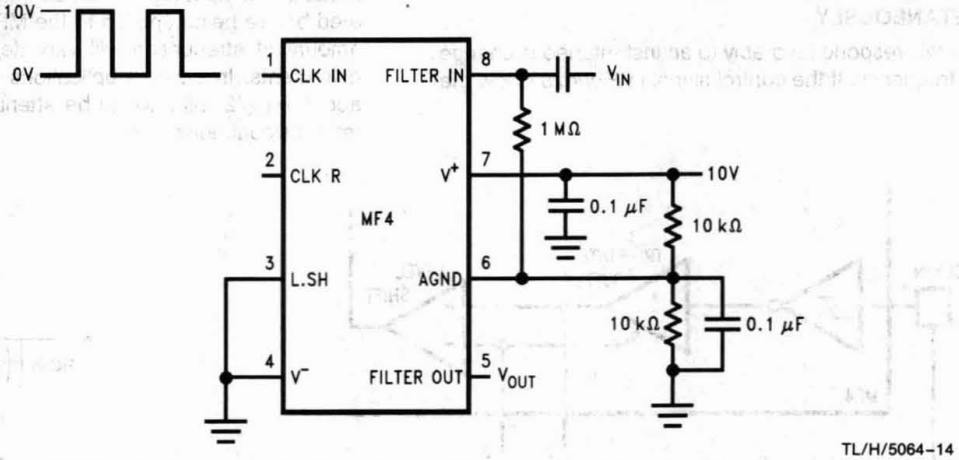
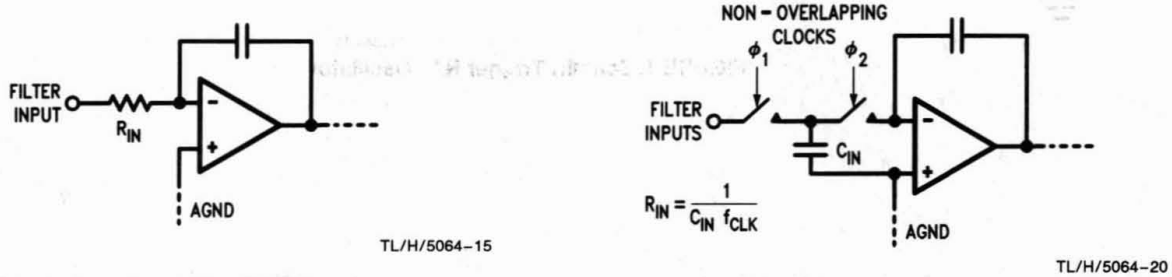


FIGURE 3. Single Supply Operation. ANGD Resistor Biased to V+/2



a) Equivalent Circuit for MF4 Filter Input **b) Actual Circuit for MF4 Filter Input**

FIGURE 4. MF4 Filter Input

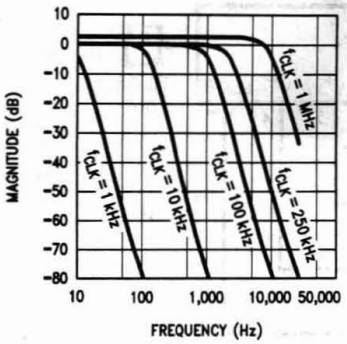


FIGURE 5a. MF4-100 Amplitude Response with ±5V Supplies

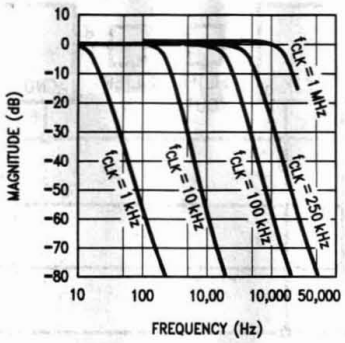


FIGURE 5b. MF4-50 Amplitude Response with ±5V Supplies

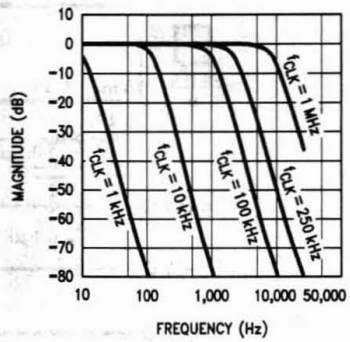


FIGURE 5c. MF4-100 Amplitude Response with ±2.5V Supplies

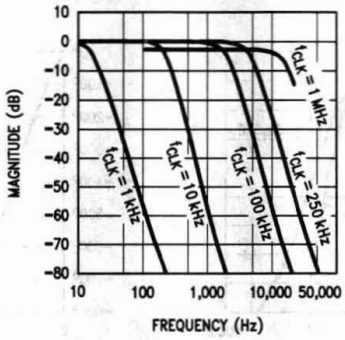


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FIGURE 5d. MF4-50 Amplitude Response with ±2.5V Supplies

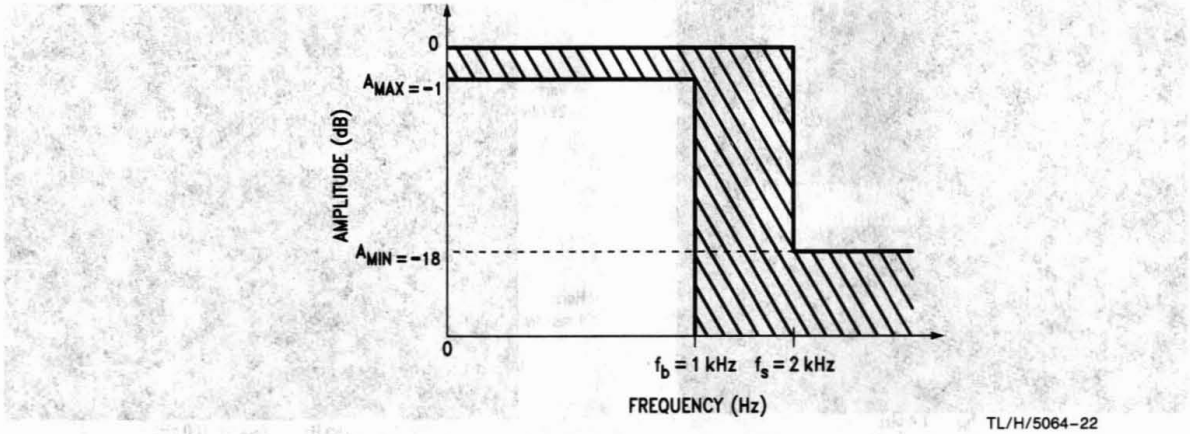

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FIGURE 6. Design Example Magnitude Response Specification where the Response of the Filter Design must fall within the shaded area of the specification

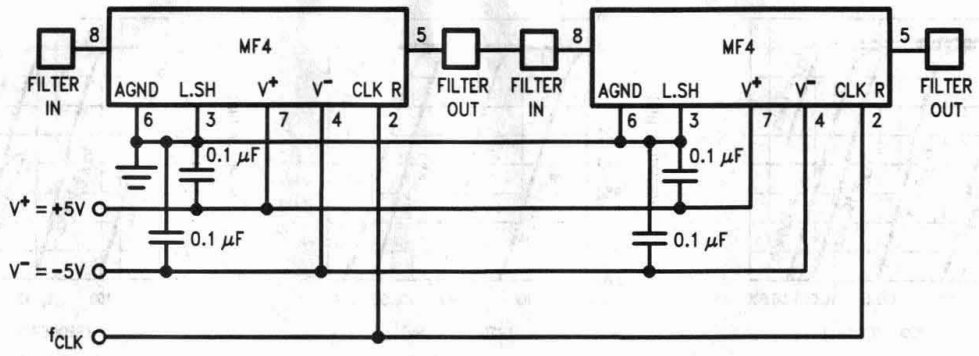

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FIGURE 7. Cascading Two MF4s

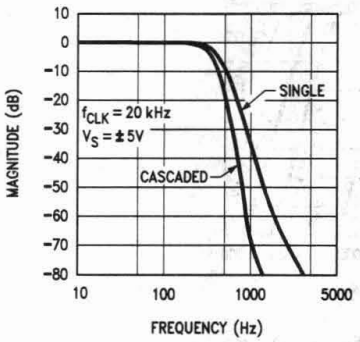

FIGURE 8a. One MF4-50 vs Two MF4-50s Cascaded

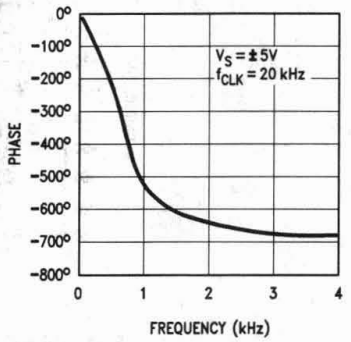

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FIGURE 8b. Phase Response of Two Cascaded MF4-50s

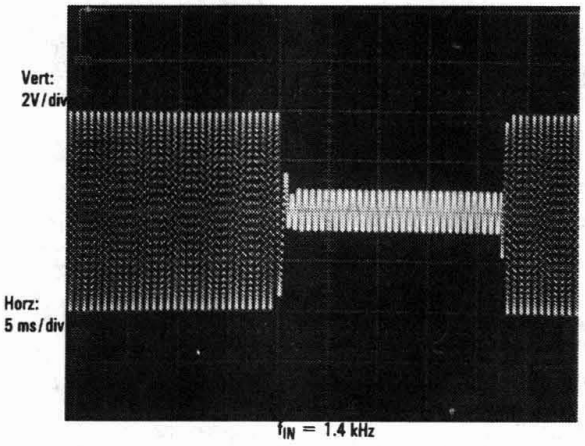

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FIGURE 9. MF4-50 Abrupt Clock Frequency Change

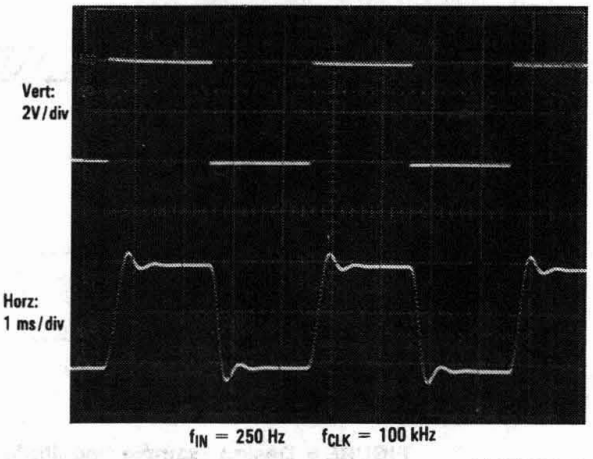

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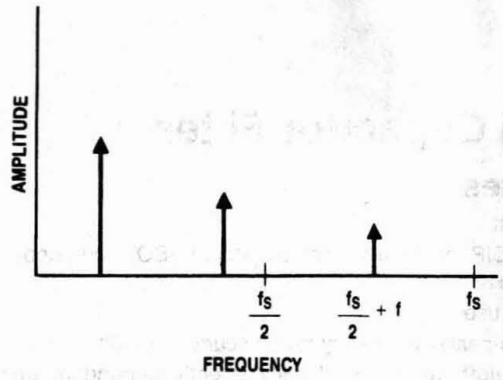
FIGURE 10. MF4-50 Input Step Response



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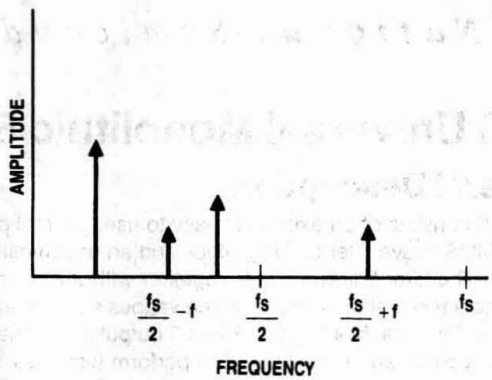
(a) input signal spectrum



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(b) Output signal spectrum. Note that the input signal at $f_C/2 + f$ causes an output signal to appear at $f_C/2 - f$.

FIGURE 11. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF4, $f_S = f_{CLK}$.

National Semiconductor

MF5 Universal Monolithic Switched Capacitor Filter

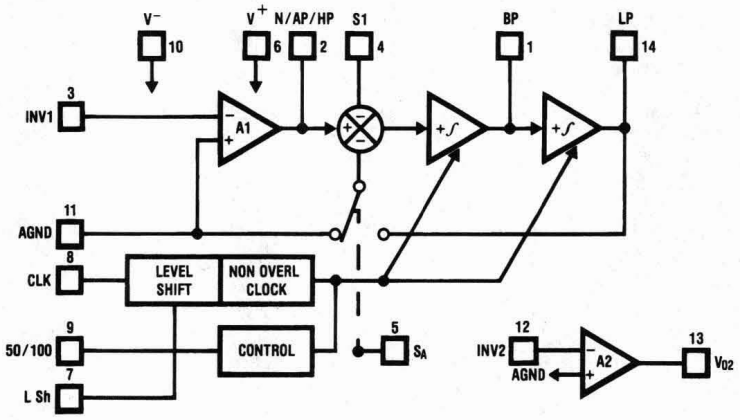
General Description

The MF5 consists of an extremely easy to use, general purpose CMOS active filter building block and an uncommitted op amp. The filter building block, together with an external clock and a few resistors, can produce various second order functions. The filter building block has 3 output pins. One of the output pins can be configured to perform highpass, allpass or notch functions and the remaining 2 output pins perform bandpass and lowpass functions. The center frequency of the filter can be directly dependent on the clock frequency or it can depend on both clock frequency and external resistor ratios. The uncommitted op amp can be used for cascading purposes, for obtaining additional allpass and notch functions, or for various other applications. Higher order filter functions can be obtained by cascading several MF5s or by using the MF5 in conjuction with the MF10 (dual switched capacitor filter building block). The MF5 is functionally compatible with the MF10. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 14-pin DIP or 14-pin Surface Mount (SO) wide-body package
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variations
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_0 \times Q$ range up to 200 kHz
- Operation up to 30 kHz (typical)
- Additional uncommitted op-amp

Block and Connection Diagrams



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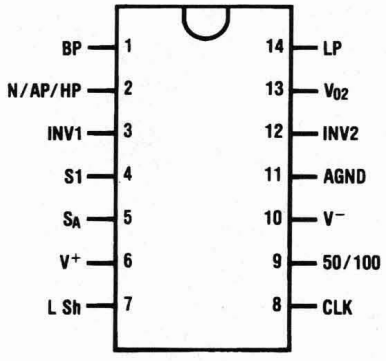
All Packages



Top View

TL/H/5066–2

Order Number MF5CN
See NS Package Number N14A

Order Number MF5CWM
See NS Package Number M14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Power Dissipation $T_A = 25°C$ (note 1)	500 mW
Storage Temp.	150°C
Soldering Information:	
N Package: 10 sec.	260°C
SO Package: Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Input Voltage (any pin)	$V^- \le V_{in} \le V^+$
Operating Temp. Range	$T_{MIN} \le T_A \le T_{MAX}$
MF5CN, MF5CWM	$0°C \le T_A \le 70°C$

Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Supply Voltage ($V^+ - V^-$)	Min				**8**	V
	Max				**14**	V
Maximum Supply Current		Clock applied to Pin 8 No Input Signal	4.5	6.0		mA
Clock Feedthrough	Filter Output		10			mV
	Op-amp Output		10			mV

Filter Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions		Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Center Frequency Range (f_o)	Max			30		**20**	kHz
	Min			0.1		**0.2**	Hz
Clock Frequency Range (f_{CLK})	Max			1.5		**1.0**	MHz
	Min			5.0		**10**	Hz
Clock to Center Frequency Ratio (f_{CLK}/f_o)		Ideal Q = 10 Mode 1	$V_{pin9} = +5V$ $F_{CLK} = 250$ kHz	50.11 ± 0.2%	50.11 ± 1.5%		
			$V_{pin9} = -5V$ $F_{CLK} = 500$ kHz	100.04 ± 0.2%	100.04 ± 1.5%		
f_{CLK}/f_o Temp. Coefficient		$V_{pin9} = +5V$ (50:1 CLK ratio)		±10			ppm/°C
		$V_{pin9} = -5V$ (100:1 CLK ratio)		±20			ppm/°C
Q Accuracy (Max) (Note 2)		Ideal Q = 10 Mode 1	$V_{pin9} = +5V$ $F_{CLK} = 250$ kHz		±10		%
			$V_{pin9} = -5V$ $F_{CLK} = 500$ kHz		±10		%
Q Temperature Coefficient		$V_{pin9} = +5V$ (50:1 CLK ratio)		−200			ppm/°C
		$V_{pin9} = -5V$ (100:1 CLK ratio)		−70			ppm/°C
DC Lowpass Gain Accuracy (Max)		Mode 1 R1 = R2 = 10 kΩ			±0.2		dB
DC Offset Voltage (Max) (Note 3)	V_{os1}			±5.0			mV
	V_{os2}	$V_{pin9} = +5V$ (50:1 CLK ratio)		−185			mV
	V_{os3}			+115			mV
	V_{os2}	$V_{pin9} = -5V$ (100:1 CLK ratio)		−310			mV
	V_{os3}			+240			mV

Filter Electrical Characteristics

$V^+ = 5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$. (Continued)

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Output Swing (Min)	BP, LP pins	RL = 5 kΩ	±4.0	±3.8		V
	N/AP/HP pin	RL = 3.5 kΩ	±4.2	±3.8		V
Dynamic Range (Note 4)		$V_{pin9} = +5V$ (50:1 CLK ratio)	83			dB
		$V_{pin9} = -5V$ (100:1 CLK ratio)	80			dB
Maximum Output Short Circuit Current (Note 5)	Source		20			mA
	Sink		3.0			mA

OP-AMP Electrical Characteristics

$V^+ = +5V \pm 0.5\%$, $V^- = -5V \pm 0.5\%$ unless other noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
Gain Bandwidth Product			2.5			MHz
Output Voltage Swing (Min)		RL = 3.5 kΩ	±4.2	±3.8		V
Slew Rate			7.0			V/μs
DC Open-Loop Gain			80			db
Input Offset Voltage (Max)			±5.0	±20		mV
Input Bias Current			10			pA
Maximum Output Short Circuit Current (Note 5)	Source		20			mA
	Sink		3.0			mA

Logic Input Characteristics

Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$. All other limits $T_A = 25°C$.

Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CMOS Clock Input	Min Logical "1" Input Voltage	$V^+ = +5V$, $V^- = -5V$, $V_{L.Sh.} = 0V$		3.0		V
	Max Logical "0" Input Voltage			−3.0		V
	Min Logical "1" Input Voltage	$V^+ = +10V$, $V^- = 0V$, $V_{L.Sh.} = +5V$		8.0		V
	Max Logical "0" Input Voltage			2.0		V
TTL Clock Input	Min Logical "1" Input Voltage	$V^+ = +5V$, $V^- = -5V$, $V_{L.Sh.} = 0V$		2.0		V
	Max Logical "0" Input Voltage			0.8		V

Note 1: The typical junction-to-ambient thermal resistance (θ_{JA}) of the 14 pin N package is 160°C/W, and 82°C/W for the M package.

Note 2: The accuracy of the Q value is a function of the center frequency (f_o). This is illustrated in the curves under the heading "Typical Performance Characteristics".

Note 3: V_{os1}, V_{os2}, and V_{os3} refer to the internal offsets as discussed in the Application Information section 3.4.

Note 4: For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μV rms for the MF5 with a 50:1 CLK ratio and 280 μV rms for the MF5 with a 100:1 CLK ratio.

Note 5: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% tested.

Note 8: Guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

Pin Description

LP(14), BP(1), N/AP/HP(2): The second order lowpass, bandpass, and notch/allpass/highpass outputs. The LP and BP outputs can typically sink 1 mA and source 3 mA. The N/AP/HP output can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.

INV1(3): The inverting input of the summing op amp of the filter. This is a high impedance input, but the non-inverting input is internally tied to AGND, making INV1 behave like a summing junction (low impedance current input).

S1(4): S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

SA(5): This pin activates a switch that connects one of the inputs of the filter's second summer to either AGND (SA tied to V−) or to the lowpass (LP) output (SA tied to V+). This offers the flexibility needed for configuring the filter in its various modes of operation.

50/100(9): This pin is used to set the internal clock to center frequency ratio (f_{CLK}/f_o) of the filter. By tying the pin to V+ an f_{CLK}/f_o ratio of about 50:1 (typically 50.11 ± 0.2%) is obtained. Tying the 50/100 pin to either AGND or V− will set the f_{CLK}/f_o ratio to about 100:1 (typically 100.04 ± 0.2%).

AGND(11): This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

V+(6), V−(10): These are the positive and negative supply pins. The MF5 will operate over a total supply range of 8V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.

CLK(8): This is the clock input for the filter. CMOS or TTL logic level clocks can be accomodated by setting the L. Sh pin to the levels described in the L. Sh pin description. For optimum filter performance a 50% duty cycle clock is recommended for clock frequencies greater than 200 kHz. This gives each op amp the maximum amount of time to settle to a new sampled input.

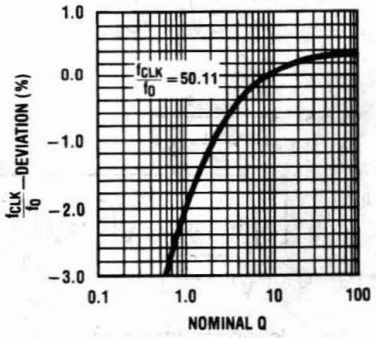
L. Sh(7): This pin allows the MF5 to accommodate either CMOS or TTL logic level clocks. For dual supply operation (i.e., ±5V), a CMOS or TTL logic level clock can be accepted if the L. Sh pin is tied to mid-supply (AGND), which should be the system ground. For single supply operation the L. Sh pin should be tied to mid-supply (AGND) for a CMOS logic level clock. The mid-supply bias should be a very low impedance node. See Applications Information for biasing techniques. For a TTL logic level clock the L. Sh pin should be tied to V− which should be the system ground.

INV2(12): This is the inverting input of the uncommitted op amp. This is a very high impedance input, but the non-inverting input is internally tied to AGND, making INV2 behave like a summing junction (low-impedance current input).

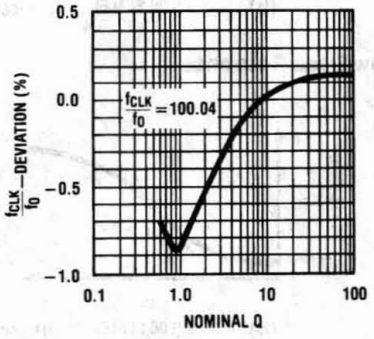
Vo2(13): This is the output of the uncommitted op amp. It will typically sink 1.5 mA and source 3.0 mA. It will typically swing to within 1V of each supply.

Typical Performance Characteristics

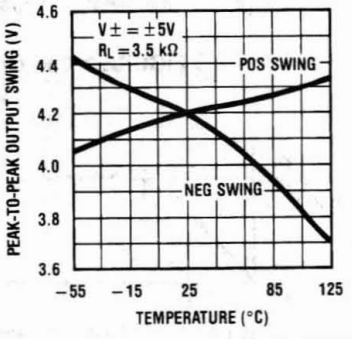
Deviation of $\frac{F_{CLK}}{F_o}$ vs Nominal Q



Deviation of $\frac{F_{CLK}}{F_o}$ vs Nominal Q



OPAMP Output Voltage Swing vs Temperature



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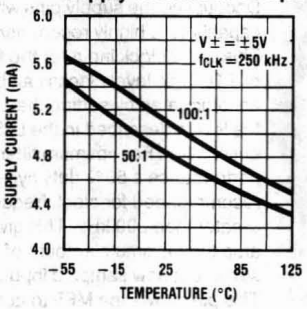
Typical Performance Characteristics (Continued)

Supply Current vs Temperature



TL/H/5066–4

1.0 Definitions of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 8.

f_o: center frequency of the second order function complex pole pair. f_o is measured at the bandpass output of the MF5, and is the frequency of maximum bandpass gain. (*Figure 1*).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch output.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_o and if Q_z is high, it can be observed as the frequency of a notch at the allpass output. (*Figure 10*).

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass output of the MF5 and is equal to f_o divided by the −3dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_z: the quality factor of the second order complex zero pair, if any. Q_z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q_z} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

where $Q_z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_o$.

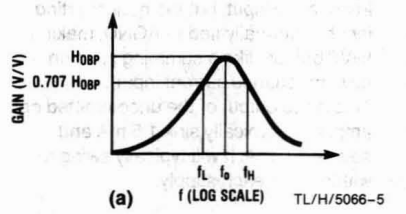
H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz (*Figure 2*).

H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{clk}/2$ (*Figure 3*).

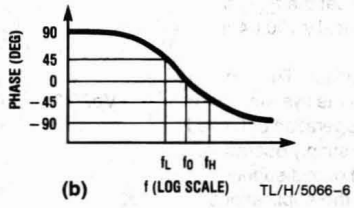
H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{clk}/2$, when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figures 11* and *8*), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{clk}/2$.



TL/H/5066–5



TL/H/5066–6

$$H_{BP}(s) = \frac{H_{OBP}\frac{\omega_o}{Q}s}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

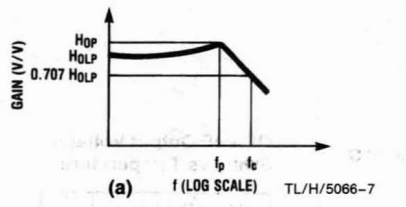
$$Q = \frac{f_o}{f_H - f_L};\quad f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

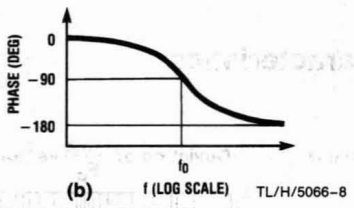
$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_o = 2\pi f_o$$

FIGURE 1. 2nd-Order Bandpass Response



TL/H/5066–7



TL/H/5066–8

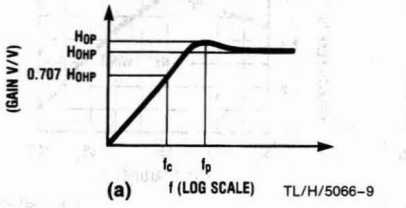
$$H_{LP}(s) = \frac{H_{OLP}\omega_o^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$f_c = f_o \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

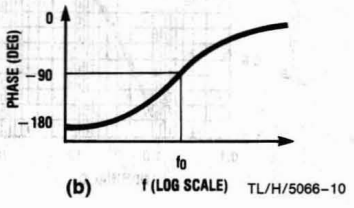
$$f_p = f_o\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



TL/H/5066–9



TL/H/5066–10

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

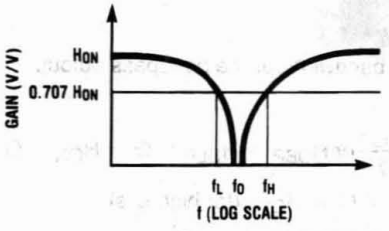
$$f_c = f_o \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

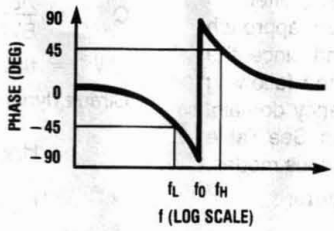
FIGURE 3. 2nd-Order High-Pass Response

1.0 Definition of Terms (Continued)



TL/H/5066–11

(a)



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(b)

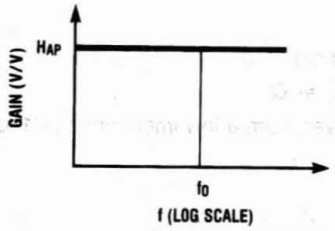
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_o}{f_H - f_L}; \quad f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

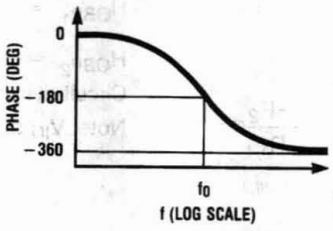
$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



TL/H/5066–13

(a)

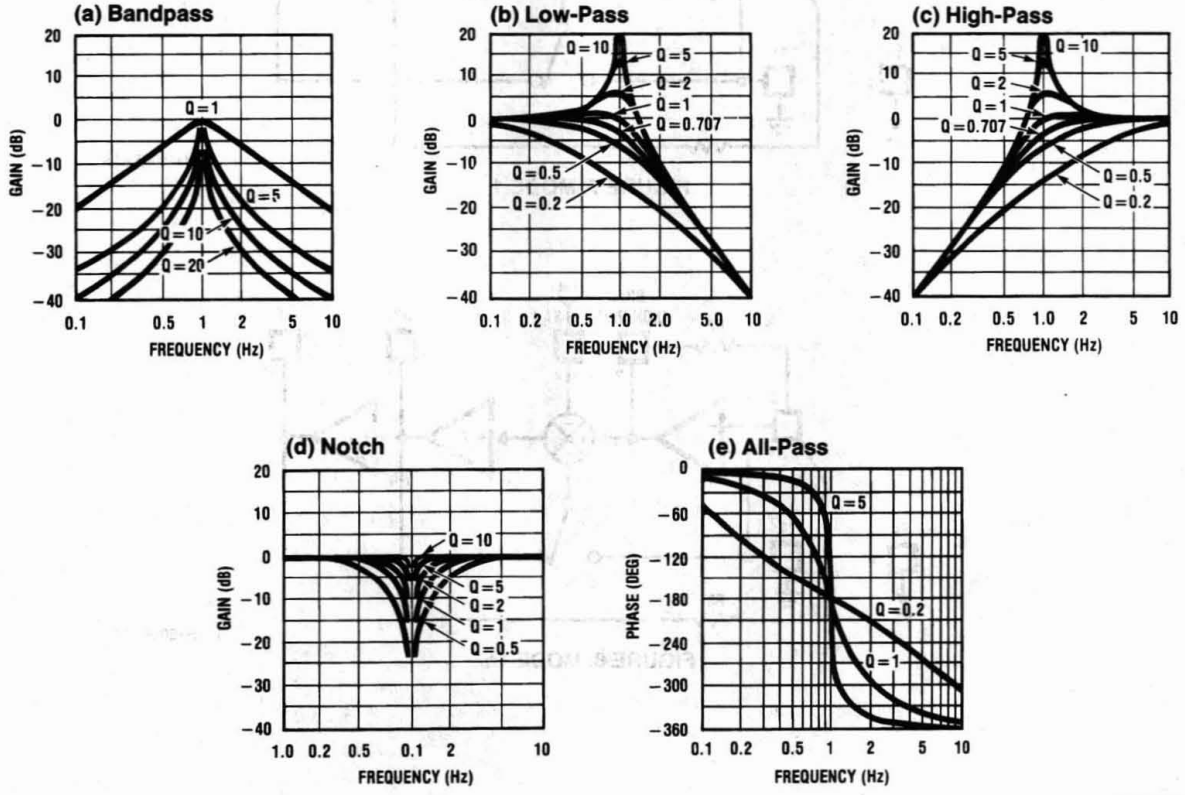


TL/H/5066–14

(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_o}{Q} + \omega_o^2\right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

FIGURE 5. 2nd-Order All-Pass Response



TL/H/5066–15

FIGURE 6. Responses of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The MF5 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF5 closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF5 can produce a full 2nd order function. See Table 1 for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$f_{notch} = f_o$ **(See *Figure 7*)**

f_o = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair = f_o.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) $= -\frac{R3}{R1}$

H_{ON} = Notch output gain as $f \rightarrow 0$, $f \rightarrow f_{CLK}/2$ $= \frac{-R_2}{R_1}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{Q}$ or $H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$.

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit dynamics: $H_{OBP_1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ)

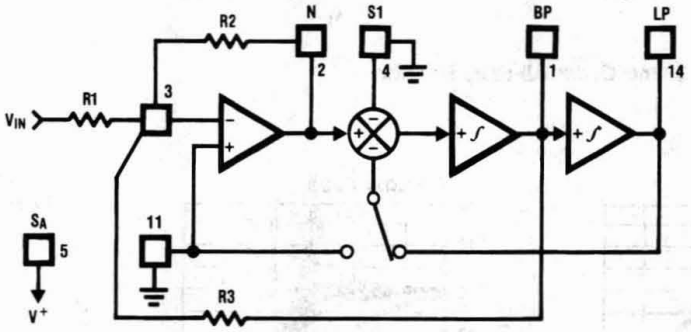


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FIGURE 7. MODE 1

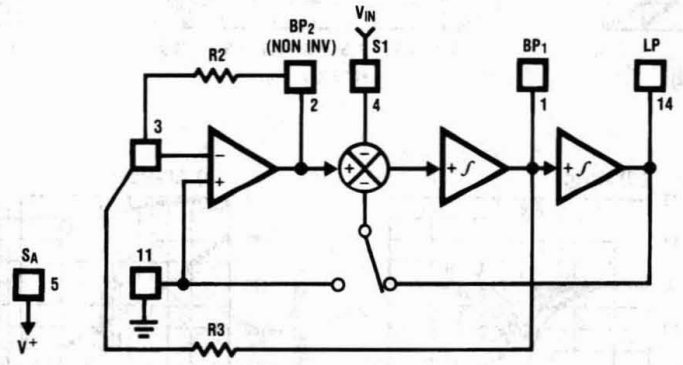

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FIGURE 8. MODE 1a

2.0 Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$ (See *Figure 9*)

f_o = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \frac{\sqrt{R2/R4+1}}{R2/R3}$$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{OBP} = Bandpass output gain (at $f = f_o$) = $-R3/R1$

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{ON_2} = Notch output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = Q\sqrt{H_{ON_1}\,H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs (See *Figure 10*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

H_{OHP} = Highpass gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) = $-\frac{R3}{R1}$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) = $-\frac{R4}{R1}$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP}} \times Q$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)

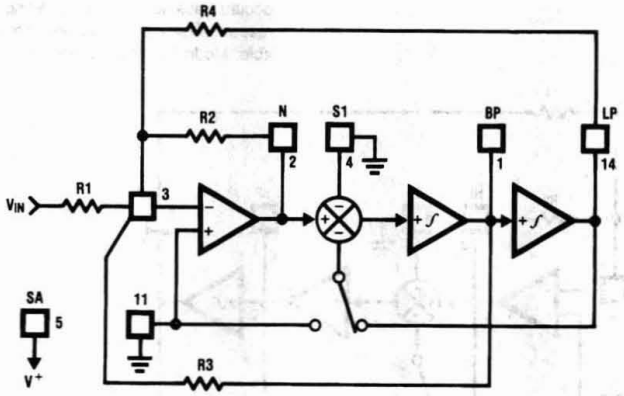

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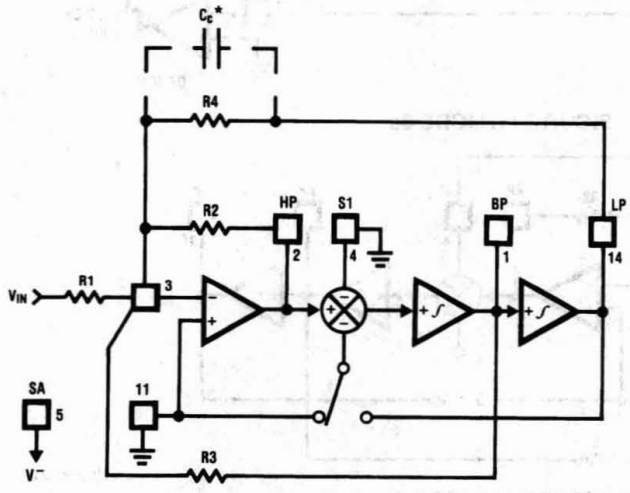
FIGURE 9. MODE 2



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*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

FIGURE 10. MODE 3

2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op amp (See *Figure 11*)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{on} = \text{gain of notch at } f = f_o = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)\right\|$$

$$H_{n1} = \text{gain of notch (as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See *Figure 12*)

f_o = center frequency

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

f_z^* = center frequency of the complex zero pair $\cong f_o$

$$Q = \frac{f_o}{BW} = \frac{R3}{R2};$$

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

$$H^*_{OAP} = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o) = -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)\, Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

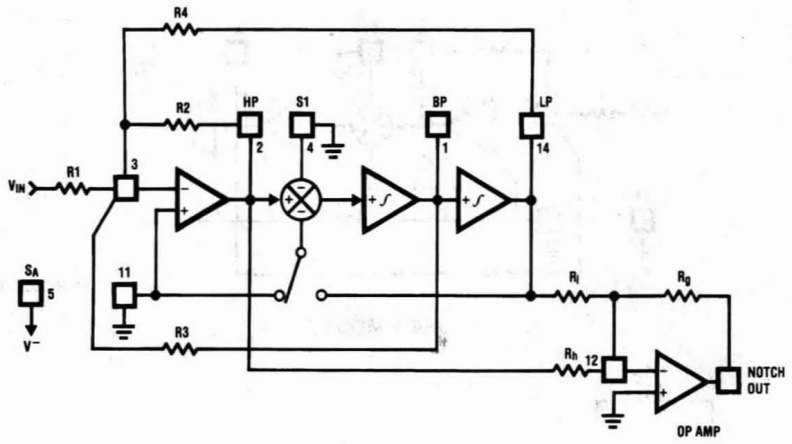

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FIGURE 11. MODE 3a

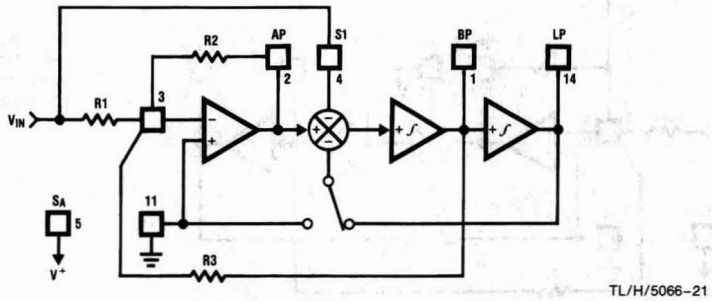

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FIGURE 12. MODE 4

2.0 Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 13*)

$$f_o = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_z = \sqrt{1-R1/R4} \times \frac{R3}{R1}$$

$$H_{0z1} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)} = \frac{-R2\,(R4-R1)}{R1\,(R4+R2)}$$

$$H_{0z2} = \text{gain at C.Z. output } \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(=\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 14*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 15*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP_1} = 1 (non-inverting)

$$H_{OLP_2} = -\frac{R3}{R2}$$

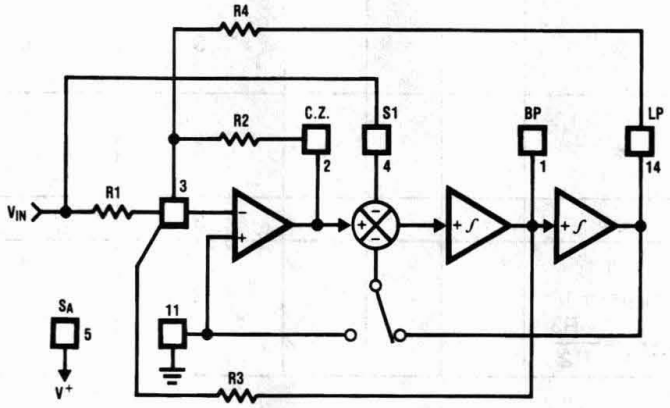

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FIGURE 13. MODE 5

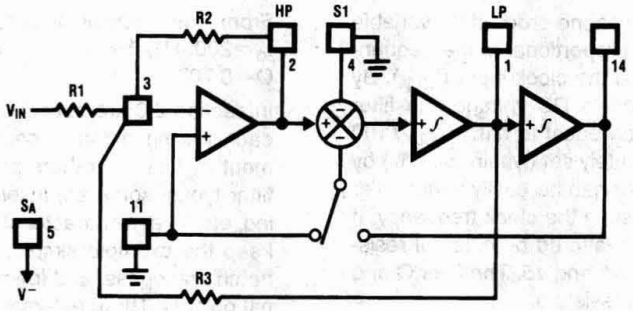

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FIGURE 14. MODE 6a

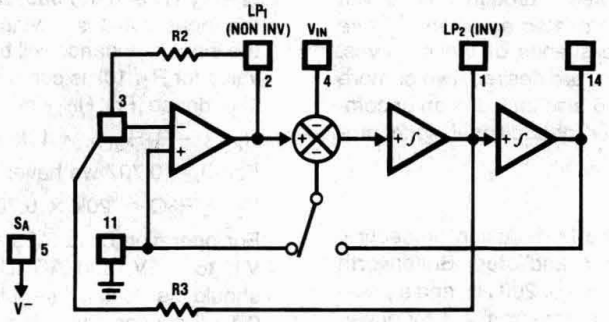

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FIGURE 15. MODE 6b

2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of resistors	Adjustable f_{CLK}/f_o	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = +1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		(2) $H_{OLP} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2		Single pole

3.0 Applications Information

The MF5 is a general-purpose second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 9 to the appropriate DC voltage, the filter center frequency f_o can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_o can be very accurately set (within ±0.6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_o ratio can be altered by external resistors as in *Figures 9, 10, 11, 13, 14*, and *15*. The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using the MF5. These are illustrated in *Figures 1* through *5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF5s can be cascaded. The MF5 also includes an uncommitted CMOS operational amplifier for additional signal processing applications.

3.1 DESIGN EXAMPLE

An example will help illustrate the MF5 design procedure. For the example, we will design a 2nd order Butterworth low-pass filter with a cutoff frequency of 200 Hz, and a passband gain of −2. The circuit will operate from a ±5V power supply, and the clock amplitude will be ±5v (CMOS) levels).

From the specifications, the filter parameters are: $f_o = 200$ Hz, $H_{OLP} = -2$, and, for Butterworth response, $Q = 0.707$.

In section 2.0 are several modes of operation for the MF5, each having different characteristics. Some allow adjustment of f_{CLK}/f_o, others produce different combinations of filter types, some are inverting while others are non-inverting, etc. These characteristics are summarized in Table I. To keep the example simple, we will use mode 1, which has notch, bandpass, and lowpass outputs, and inverts the signal polarity. Three external resistors determine the filter's Q and gain. From the equations accompanying *Figure 7*, $Q = R_3/R_2$ and the passband gain $H_{OLP} = -R_2/R_1$. Since the input signal is driving a summing junction through R_1, the input impedance will be equal to R_1. Start by choosing a value for R_1. 10k is convenient and gives a reasonable input impedance. For $H_{OLP} = -2$, we have:

$R_2 = -R_1H_{OLP} = 10k \times 2 = 20k$.

For $Q = 0.707$ we have:

$R_3 = R_2Q = 20k \times 0.707 = 14.14k$. Use 15k.

For operation on ±5V supplies, V^+ is connected to +5V, V^- to −5V, and AGND to ground. The power supplies should be "clean" (regulated supplies are preferred) and 0.1 μF bypass capacitors are recommended.

3.0 Applications Information (Continued)

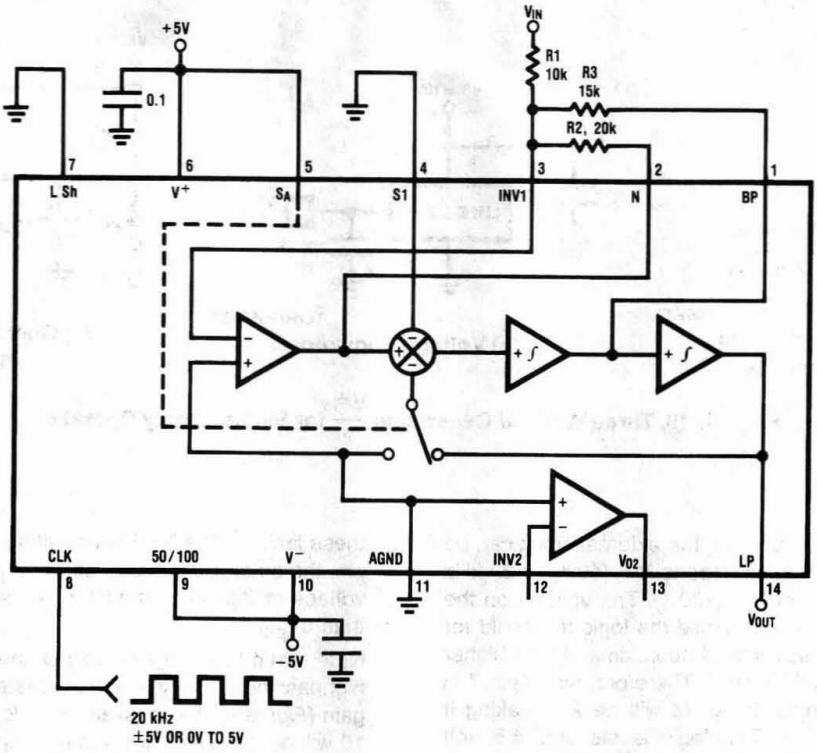

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FIGURE 16. 2nd-Order Butterworth Low-Pass Filter of Design Example. For $\frac{f_{CLK}}{f_0} = 50$, Connect Pin 9 to +5V, and Change Clock Frequency to 10 kHz.

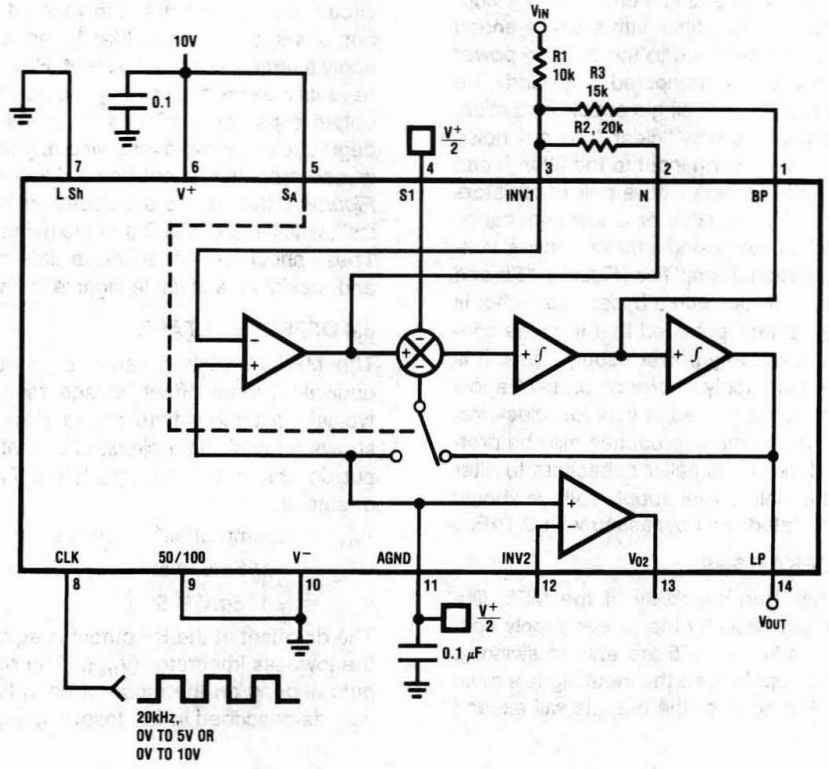

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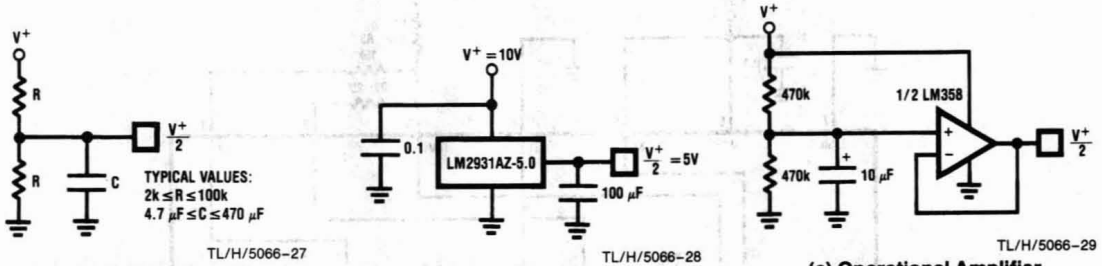
FIGURE 17. Butterworth Low-Pass Circuit of Example, but Designed for Single-Supply Operation

3.0 Applications Information (Continued)



(a) Resistive Divider with Decoupling Capaciter **(b) Voltage Regulator** **(c) Operational Amplifier with Divider**

FIGURE 18. Three Ways of Generating $\frac{V^+}{2}$ for Single-supply Operation

For a cutoff frequency of 200 Hz, the external clock can be either 10 kHz with pin 9 connected to V^+ (50:1) or 20 kHz with pin 9 tied to A_{GND} or V^- (100:1). The voltage on the Logic Level Shift pin (7) determines the logic threshold for the clock input. The threshold is approximately 2V higher than the voltage applied to pin 7. Therefore, when pin 7 is grounded, the clock logic threshold will be 2V, making it compatible with 0–5 volt TTL logic levels and ±5 volt CMOS levels. Pin 7 should be connected to a clean, low-impedance (less than 1000Ω) voltage source.

The complete circuit of the design example is shown for a 100:1 clock ratio in *Figure 16*.

3.2 SINGLE SUPPLY OPERATION

The MF5 can also operate with a single-ended power supply. *Figure 17* shows the example filter with a single-ended power supply. V^+ is again connected to the positive power supply (8 to 14 volts), and V^- is connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (*Figure 18a*), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (*Figures 18b* and *18c*). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1μF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF5, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF5 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF5 is operating on ±5 volts, for example, the outputs will clip at about $8V_{p-p}$. The maximum input voltage multiplied by the filter gain should therefore be less than $8V_{p-p}$.

Note that if the filter has high Q, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (*Figure 6*). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_o. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_o will be 10. The maximum input signal at f_o must therefore be less than 800 mV_{p-p} when the circuit is operated on ±5 volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (*Figure 7*). The notch output will be very small at f_o, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_o and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *15* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF5's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. *Figure 19* shows an equivalent circuit of the MF5 from which the output dc offsets can be calculated. Typical values for these offsets are:

V_{os1} = opamp offset = ±5mV

V_{os2} = −185mV @ 50:1 −310mV @ 100:1

V_{os3} = +115mV @ 50:1 +240mV @ 100:1

The dc offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

3.0 Applications Information (Continued)

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{Rp} + 1\right)V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1+R4/R2} - \frac{V_{OS3}}{Q\sqrt{1+R2/R4}};$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3}V_{OS3} + V_{OS2}\right) + -\frac{R4}{R2}\left(1 + \frac{R2}{R_p}\right)V_{OS1};\ R_p = R1//R3//R4$$

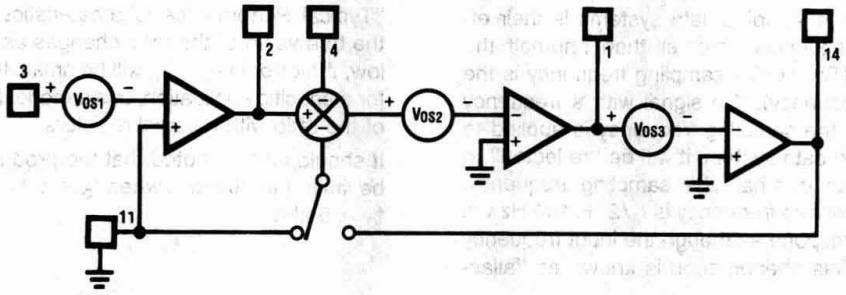


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FIGURE 19. Block Diagram Showing MF5 Offset Voltage Sources

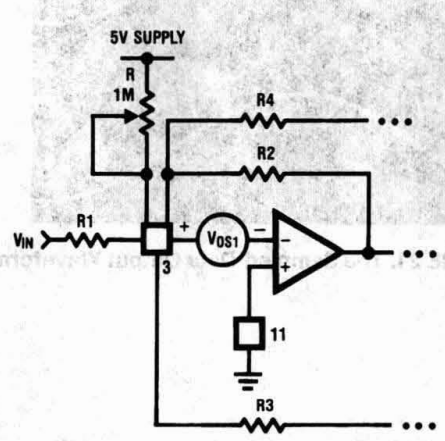

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FIGURE 20. Method for Trimming V_{OS}, See Text, Section 3.4

3.0 Applications Information (Continued)

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_o and Q. When operating in Mode 3, offsets can become excessively large if R_2 and R_4 are used to make f_{CLK}/f_o significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and $f_{CLK}/f_o = 250$ with pin 9 tied to V^- (100:1 nominal). R_4/R_2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1.9V. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 20*. This allows adjustment of V_{os1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{os(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The MF5 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF5's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 100$ Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF5 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate. (*Figure 21*) If necessary, these can be "smoothed" with a simple R-C low-pass filter at the MF5 output.

The ratio of f_{CLK} to f_c (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in 3.4.

The accuracy of the f_{CLK}/f_o ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_o will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_o should be limited to 300 kHz when $f_o < 5$ kHz, and to 200 kHz for $f_o > 5$ kHz.

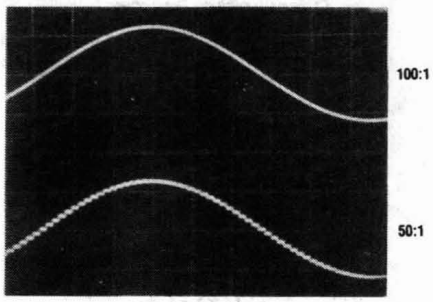

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FIGURE 21. The Sampled-Data Output Waveform

National Semiconductor

MF6 6th Order Switched Capacitor Butterworth Lowpass Filter

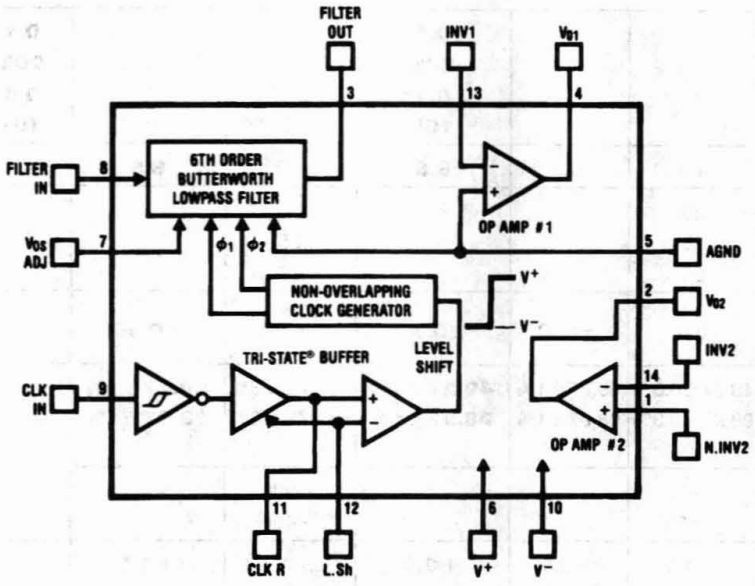
General Description

The MF6 is a versatile easy to use, precision 6th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF6-50) or 100 to 1 (MF6-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or an external TTL or CMOS logic compatible clock can be used for tighter cutoff frequency control. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF6 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

Features

- No external components
- 14-pin DIP or 14-pin wide-body S.O. package
- Cutoff frequency accuracy of ±0.3% typical
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Two uncommitted op amps available
- 5V to 14V total supply voltage
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams



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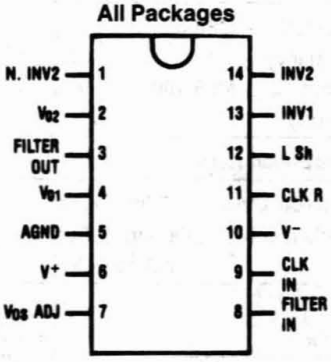

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Top View

Order Number MF6CWM-50 or MF6CWM-100
See NS Package Number M14B

Order Number MF6CN-50 or MF6CN-100
See NS Package Number N14A

Order Number MF6CJ-50 or MF6CJ-100
See NS Package Number J14A

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Voltage at Any Pin	$V^- - 0.2V$, $V^+ + 0.2V$
Input Current at Any Pin (Note 13)	5 mA
Package Input Current (Note 13)	20 mA
Power Dissipation (Note 14)	500 mW
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 12)	800V
Soldering Information	
N Package (10 sec.)	260°C
J Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 11)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF6CN-50, MF6CN-100	$0°C \le T_A \le +70°C$
MF6CWM-50, MF6CWM-100	$0°C \le T_A \le +70°C$
MF6CJ-50, MF6CJ-100	$-40°C \le T_A \le +85°C$
Supply Voltage ($V_S = V^+ - V^-$)	5V to 14V

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \le 250$ kHz (see Note 3) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CWM-50, MF6CWM-100, MF6CN-50, MF6CN-100			MF6CJ-50, MF6CJ-100			Units
		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V$, $V^- = -5V$								
f_c, Cutoff Frequency Range (Note 1) MF6-50 Min				**0.1**			**0.1**	Hz
MF6-50 Max				**20k**			**20k**	
MF6-100 Min				**0.1**			**0.1**	
MF6-100 Max				**10k**			**10k**	
Total Supply Current	$f_{CLK} = 250$ kHz	4.0	6.0	**8.5**	4.0	**8.5**		mA
Maximum Clock Feedthrough Filter Output		30			30			mV (peak-to-peak)
Op Amp 1 Out		25			25			
Op Amp 2 Out		20			20			
H_o, DC Gain	$R_{source} \le 2$ kΩ	0.0	±0.30	**±0.30**	0.0	**±0.30**		dB
f_{CLK}/f_c, Clock to Cutoff Frequency Ratio MF6-50		49.27 ± 0.3%	49.27 ± 1%	**49.27 ± 1%**	49.27 ± 0.3%	**49.27 ± 1%**		
MF6-100		98.97 ± 0.3%	98.97 ± 1%	**98.97 ± 1%**	98.97 ± 0.3%	**98.97 ± 1%**		
DC Offset Voltage MF6-50		−200			−200			mV
MF6-100		−400			−400			
Minimum Output Voltage Swing	$R_L = 10$ kΩ	+4.0	+3.5	**+3.5**	+4.0	**+3.5**		V
		−4.1	−3.8	**−3.5**	−4.1	**−3.5**		
Maximum Output Short Circuit Current (Note 6) Source		50			50			mA
Sink		1.5			1.5			
Dynamic Range (Note 2) MF6-50		83			83			dB
MF6-100		81			81			
Additional Magnitude Response Test Points (Note 4) MF6-50	$f_{CLK} = 250$ kHz							
	f = 6000 Hz	−9.47	−9.47 ± 0.6	**−9.47 ± 0.75**	−9.47	**−9.47 ± 0.75**		dB
	f = 4500 Hz	−0.92	−0.92 ± 0.6	**−0.92 ± 0.4**	−0.92	**−0.92 ± 0.4**		
MF6-100	$f_{CLK} = 250$ kHz							
	f = 3000 Hz	−9.48	−9.48 ± 0.3	**−9.48 ± 0.75**	−9.48	**−9.48 ± 0.75**		dB
	f = 2250 Hz	−0.97	−0.97 ± 0.3	**−0.97 ± 0.4**	−0.97	**−0.97 ± 0.4**		

Filter Electrical Characteristics (Continued) The following specifications apply for $f_{CLK} \leq 250$ kHz (see Note 3) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CWM-50, MF6CWM-100 MF6CN-50, MF6CN-100			MF6CJ-50, MF6CJ-100			Units
		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V, V^- = -5V$ (Continued)								
Attenuation Rate MF6-50	$f_{CLK} = 250$ kHz $f_1 = 6000$ Hz $f_2 = 8000$ Hz		−36	**−36**		**−36**		dB/ octave
MF6-100	$f_{CLK} = 250$ kHz $f_1 = 3000$ Hz $f_2 = 4000$ Hz		−36	**−36**		**−36**		dB/ octave
$V^+ = +2.5V, V^- = -2.5V$								
f_c, Cutoff Frequency Range (Note 1) MF6-50 Min				**0.1**			**0.1**	Hz
Max				**10k**			**10k**	
MF6-100 Min				**0.1**			**0.1**	
Max				**5k**			**5k**	
Total Supply Current	$f_{CLK} = 250$ kHz	2.5	4.0	**4.0**	2.5	**4.0**		mA
Maximum Clock Feedthrough Filter Output		20			20			mV (peak-to-peak)
Op Amp 1 Out		15			15			
Op Amp 2 Out		10			10			
H_o, DC Gain	$R_{source} \leq 2$ kΩ	0.0	±0.30	**±0.30**	0.0	**±0.30**		dB
f_{CLK}/f_c, Clock to Cutoff Frequency Ratio MF6-50		49.10 ± 0.3%	49.10 ± 2%	**49.10 ± 3%**	49.10 ± 0.3%	**49.10 ± 3%**		
MF6-100		98.65 ± 0.3%	98.65 ± 2%	**98.65 ± 2.25%**	98.65 ± 0.3%	**98.65 ± 2.25%**		
DC Offset Voltage MF6-50		−200			−200			mV
MF6-100		−400			−400			
Minimum Output Voltage Swing	$R_L = 10$ kΩ	+1.5 −2.2	+1.0 −1.7	**+1.0** **−1.5**	+1.5 −2.2	**+1.0** **−1.5**		V
Maximum Output Short Circuit Current (Note 6) Source		28			28			mA
Sink		0.5			0.5			
Dynamic Range (Note 2)		77			77			dB
Additional Magnitude Response Test Points (Note 4) MF6-50	$f_{CLK} = 250$ kHz							
	$f = 6000$ Hz	−9.54	−9.54 ± 0.6	**−9.54 ± 0.75**	−9.54	**−9.54 ± 0.75**		dB
	$f = 4500$ Hz	−0.96	−0.96 ± 0.3	**−0.96 ± 0.4**	−0.96	**−0.96 ± 0.4**		
MF6-100	$f_{CLK} = 250$ kHz							
	$f = 3000$ Hz	−9.67	−9.67 ± 0.6	**−9.67 ± 0.75**	−9.67	**−9.67 ± 0.75**		dB
	$f = 2250$ Hz	−1.01	−1.01 ± 0.3	**−1.01 ± 0.4**	−1.01	**−1.01 ± 0.4**		
Attenuation Rate MF6-50	$f_{CLK} = 250$ kHz $f_1 = 6000$ Hz $f_2 = 8000$ Hz		−36	**−36**		**−36**		dB/ octave
MF6-100	$f_{CLK} = 250$ kHz $f_1 = 3000$ Hz $f_2 = 4000$ Hz		−36	**−36**		**−36**		dB/ octave

Op Amp Electrical Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	MF6CN-50, MF6CN-100, MF6CWM-50, MF6CWM-100			MF6CJ-50, MF6CJ-100			Units
		Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ = +5V, V^- = -5V$								
Input Offset Voltage		±8.0	±20	**±20**	±8.0	**±20**		mV
Input Bias Current		10			10			pA
CMRR (Op Amp #2 Only)	$V_{CM1} = 1.8V$, $V_{CM2} = -2.2V$	60	55		60	55		dB
Output Voltage Swing	$R_L = 10\ k\Omega$	+4.0 −4.5	+3.8 −4.0	**+3.6** **−4.0**	+4.0 −4.5	**+3.6** **−4.0**		V
Maximum Output Short Source Circuit Current (Note 6) Sink		54 2.0	65 4.0	**80** **6.0**	54 2.0	**80** **6.0**		mA
Slew Rate		7.0			7.0			V/μs
DC Open Loop Gain		72			72			dB
Gain Bandwidth Product		1.2			1.2			MHz
$V^+ = +2.5V, V^- = -2.5V$								
Input Offset Voltage		±8.0	±20	**±20**	±8.0	**±20**		mV
Input Bias Current		10			10			pA
CMRR (Op-Amp #2 Only)	$V_{CM1} = +0.5V$, $V_{CM2} = -0.9V$	60	55		60	55		dB
Output Voltage Swing	$R_L = 10\ k\Omega$	+1.5 −2.2	+1.3 −1.7	**+1.1** **−1.7**	+1.5 −2.2	**+1.1** **−1.7**		V
Maximum Output Short Source Circuit Current (Note 6) Sink		24 1.0			24 1.0			mA
Slew Rate		6.0			6.0			V/μs
DC Open Loop Gain		67			67			dB
Gain Bandwidth Product		1.2			1.2			MHz

Logic Input-Output Electrical Characteristics

The following specifications apply for $V^- = 0V$ (see Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter		Conditions		MF6CN-50, MF6CN-100 MF6CWM-50, MF6CWM-100			MF6CJ-50, MF6CJ-100			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
TTL CLOCK INPUT, CLK R PIN (Note 7)										
Maximum V_{IL}, Logical "0" Input Voltage					0.8	**0.8**		**0.8**		V
Minimum V_{IH}, Logical "1" Input Voltage					2.0	**2.0**		**2.0**		V
Maximum Leakage Current at CLK R Pin		L Sh Pin at Mid- Supply			2.0	**2.0**		**2.0**		μA
SCHMITT TRIGGER										
V_{T+}, Positive Going Threshold Voltage	Min	$V^+ = 10V$		7.0	6.1	**6.1**	7.0	**6.1**		V
	Max				8.9	**8.9**		**8.9**		
	Min	$V^+ = 5V$		3.5	3.1	**3.1**	3.5	**3.1**		V
	Max				4.4	**4.4**		**4.4**		
V_{T-}, Negative Going Threshold Voltage	Min	$V^+ = 10V$		3.0	1.3	**1.3**	3.0	**1.3**		V
	Max				3.8	**3.8**		**3.8**		
	Min	$V^+ = 5V$		1.5	0.6	**0.6**	1.5	**0.6**		V
	Max				1.9	**1.9**		**1.9**		
Hysteresis ($V_{T+} - V_{T-}$)	Min	$V^+ = 10V$		4.0	2.3	**2.3**	4.0	**2.3**		V
	Max				7.6	**7.6**		**7.6**		
	Min	$V^+ = 5V$		2.0	1.2	**1.2**	2.0	**1.2**		V
	Max				3.8	**3.8**		**3.8**		
Minimum Logical "1" Output Voltage (Pin 11)		$I_O = -10\mu A$	$V^+ = 10V$		9.0	**9.0**		**9.0**		V
			$V^+ = 5V$		4.5	**4.5**		**4.5**		
Maximum Logical "0" Output Voltage (Pin 11)		$I_O = 10\mu A$	$V^+ = 10V$		1.0	**1.0**		**1.0**		V
			$V^+ = 5V$		0.5	**0.5**		**0.5**		
Minimum Output Source Current (Pin 11)		CLK R Tied to Ground	$V^+ = 10V$	6.0	3.0	**3.0**	6.0	**3.0**		mA
			$V^+ = 5V$	1.5	0.75	**0.75**	1.5	**0.75**		
Maximum Output Sink Current (Pin 11)		CLK R Tied to V^+	$V^+ = 10V$	5.0	2.5	**2.5**	5.0	**2.5**		mA
			$V^+ = 5V$	1.3	0.65	**0.65**	1.3	**0.65**		

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μVrms for the MF6-50 and 250 μVrms for the MF6-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically 140 μVrms for both the MF6-50 and the MF6-100.

Note 3: The specifications for the MF6 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±1.0% but the filter still maintains its magnitude characteristics. See Application Hints, Section 1.5.

Note 4: Besides checking the cutoff frequency (f_c) and the stopband attenuation at 2 f_c, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

Note 5: For simplicity all the logic levels have been referenced to $V^- = 0V$ and will scale accordingly for ±5V and ±2.5V supplies (except for the TTL input logic levels).

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: The MF6 is operating with symmetrical split supplies and L.Sh is tied to ground.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level.

Note 10: Design limits are guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 11: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified conditions.

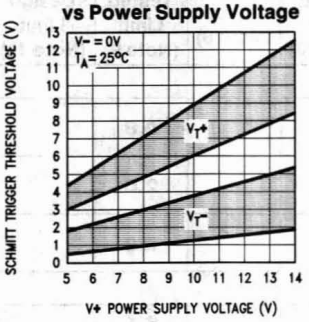
Note 12: Human body model, 100 pF discharged through a 1.5k Ω resistor.

Note 13: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

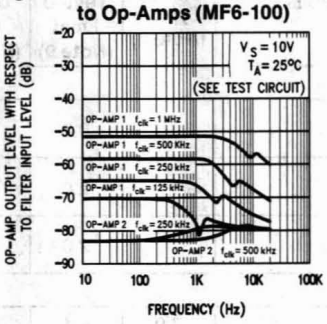
Note 14: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF6CN when board mounted is 67°C/W. For the MF6CJ this number decreases to 62°C/W. For MF6CWM, $\theta_{JA} = 78°C/W$.

Typical Performance Characteristics

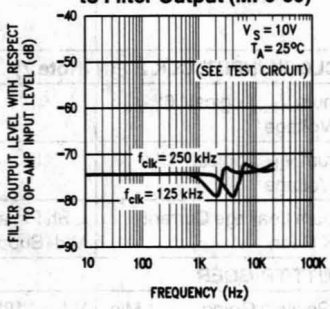
Schmitt Trigger Threshold Voltage vs Power Supply Voltage



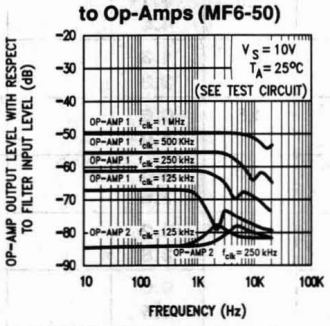
Crosstalk from Filter to Op-Amps (MF6-100)


V_S = 10V
T_A = 25°C
(SEE TEST CIRCUIT)
OP-AMP 1 f_{clk} = 1 MHz
OP-AMP 1 f_{clk} = 500 KHz
OP-AMP 1 f_{clk} = 250 kHz
OP-AMP 1 f_{clk} = 125 kHz
OP-AMP 2 f_{clk} = 250 kHz
OP-AMP 2 f_{clk} = 500 kHz
OP-AMP OUTPUT LEVEL WITH RESPECT TO FILTER INPUT LEVEL (dB)
FREQUENCY (Hz)

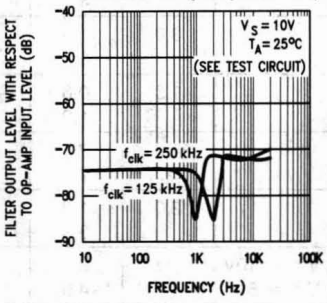
Crosstalk from Either Op-Amp to Filter Output (MF6-50)


V_S = 10V
T_A = 25°C
(SEE TEST CIRCUIT)
f_{clk} = 250 kHz
f_{clk} = 125 kHz
FILTER OUTPUT LEVEL WITH RESPECT TO OP-AMP INPUT LEVEL (dB)
FREQUENCY (Hz)

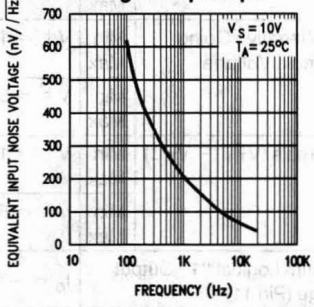
Crosstalk from Filter to Op-Amps (MF6-50)


V_S = 10V
T_A = 25°C
(SEE TEST CIRCUIT)
OP-AMP 1 f_{clk} = 1 MHz
OP-AMP 1 f_{clk} = 500 KHz
OP-AMP 1 f_{clk} = 250 kHz
OP-AMP 1 f_{clk} = 125 kHz
OP-AMP 2 f_{clk} = 125 kHz
OP-AMP 2 f_{clk} = 250 kHz
OP-AMP OUTPUT LEVEL WITH RESPECT TO FILTER INPUT LEVEL (dB)
FREQUENCY (Hz)

Crosstalk from Either Op-Amp to Filter Output (MF6-100)


V_S = 10V
T_A = 25°C
(SEE TEST CIRCUIT)
f_{clk} = 250 kHz
f_{clk} = 125 kHz
FILTER OUTPUT LEVEL WITH RESPECT TO OP-AMP INPUT LEVEL (dB)
FREQUENCY (Hz)

Equivalent Input Noise Voltage of Op-Amps



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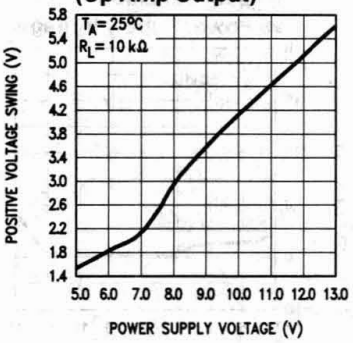
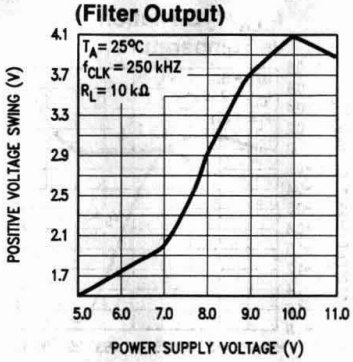
Typical Performance Characteristics (Continued)

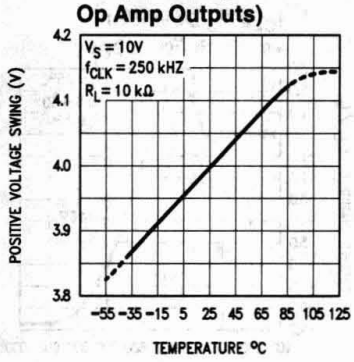
Positive Voltage Swing vs Power Supply Voltage (Op Amp Output)



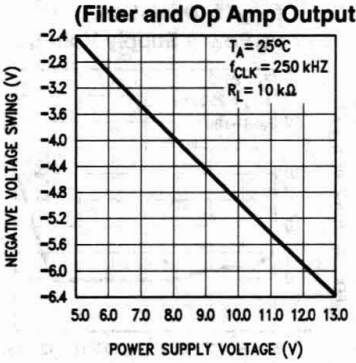
Positive Voltage Swing vs Power Supply Voltage (Filter Output)



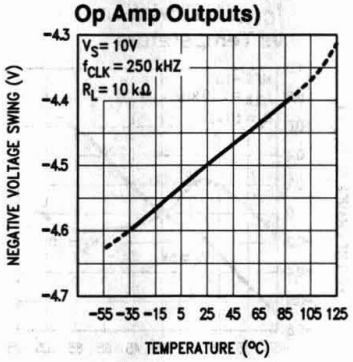
Positive Voltage Swing vs Temperature (Filter and Op Amp Outputs)



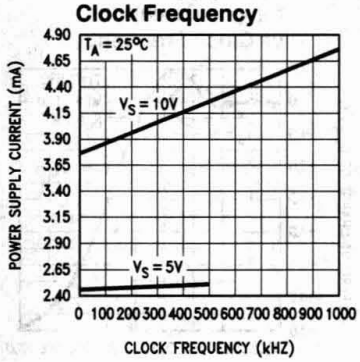
Negative Voltage Swing vs Power Supply Voltage (Filter and Op Amp Outputs)


T_A = 25°C
f_{CLK} = 250 kHZ
R_L = 10 kΩ
NEGATIVE VOLTAGE SWING (V)
−2.4 −2.8 −3.2 −3.6 −4.0 −4.4 −4.8 −5.2 −5.6 −6.0 −6.4
5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0
POWER SUPPLY VOLTAGE (V)

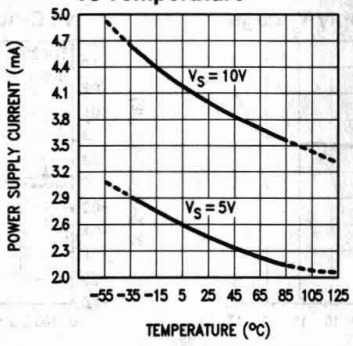
Negative Voltage Swing vs Temperature (Filter and Op Amp Outputs)



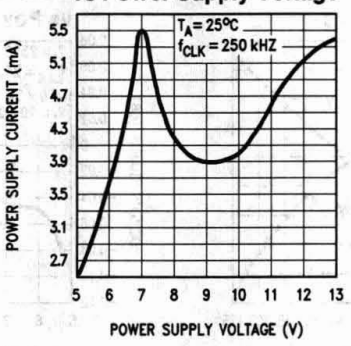
Power Supply Current vs Clock Frequency



Power Supply Current vs Temperature



Power Supply Current vs Power Supply Voltage



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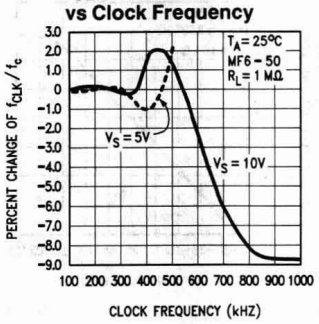
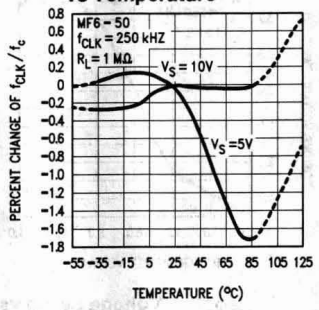
Typical Performance Characteristics (Continued)

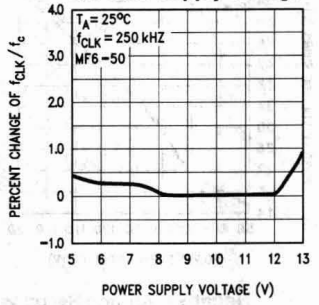
f_{CLK}/f_c Deviation vs Clock Frequency



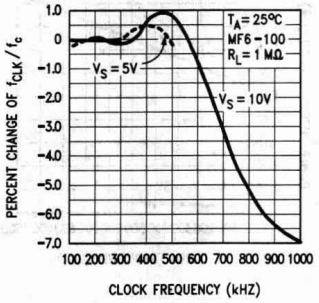
f_{CLK}/f_c Deviation vs Temperature



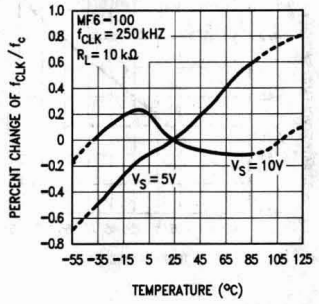
f_{CLK}/f_c Deviation vs Power Supply Voltage



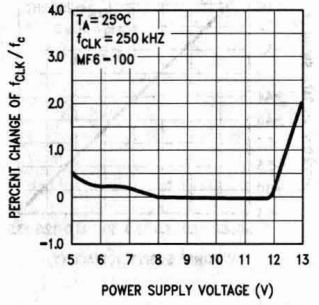
f_{CLK}/f_c Deviation vs Clock Frequency



f_{CLK}/f_c Deviation vs Temperature

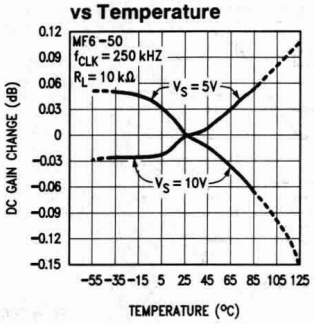


f_{CLK}/f_c Deviation vs Power Supply Voltage

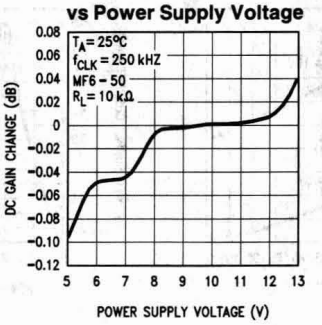


TL/H/5065–36

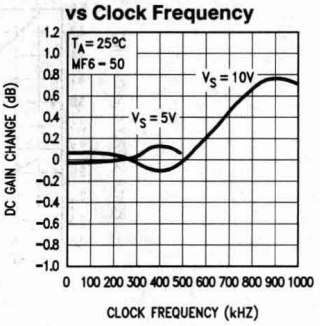
DC Gain Deviation vs Temperature



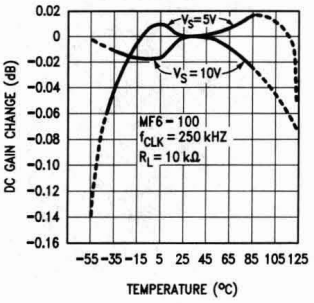
DC Gain Deviation vs Power Supply Voltage



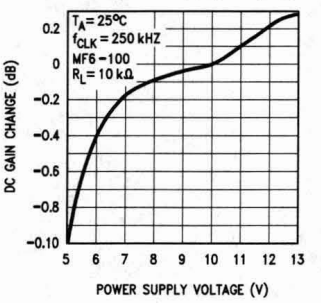
DC Gain Deviation vs Clock Frequency



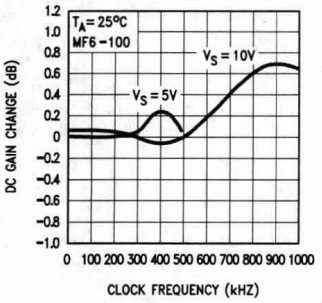
DC Gain Deviation vs Temperature



DC Gain Deviation vs Power Supply Voltage



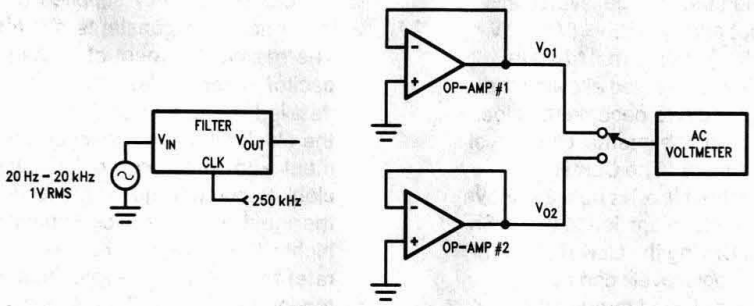
DC Gain Deviation vs Clock Frequency



TL/H/5065–39

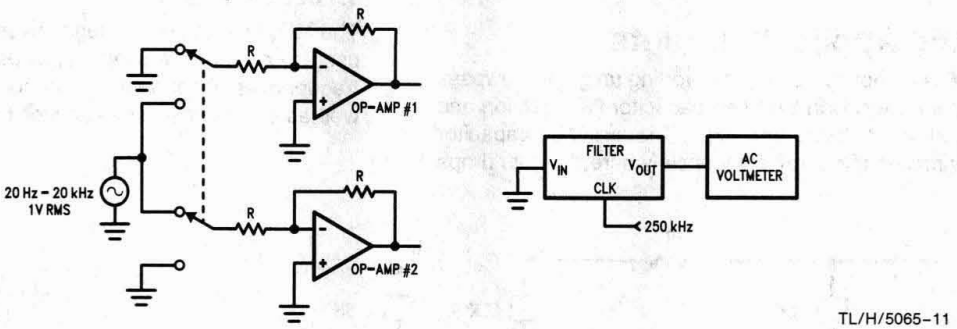
Crosstalk Test Circuits

From Filter to Opamps



TL/H/5065–10

From Either Opamp to Filter Output



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Pin Descriptions (Pin Numbers)

Pin	Description
FILTER OUT (3)	The output of the lowpass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.
FILTER IN (8)	The input to the lowpass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (see section 1.4). For single supply operation the input signal must be biased to mid-supply or AC coupled.
V_{OS}ADJ (7)	This pin is used to adjust the DC offset of the filter output; if not used it must be tied to the AGND potential. (See section 1.3)
AGND (5)	The analog ground pin. This pin sets the DC bias level for the filter section and the non-inverting input of Op-Amp #1 and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.
V_{O1} (4), INV1 (13)	V_{O1} is the output and INV1 is the inverting input of Op-Amp #1. The non-inverting input of this Op-Amp is internally connected to the AGND pin.
V_{O2} (2), INV2 (14), NINV2 (1)	V_{O2} is the output, INV2 is the inverting input, and NINV2 is the non-inverting input of Op-Amp #2.
V^+ (6), V^- (10)	The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
CLK IN (9)	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self-clocking Schmitt-trigger oscillator (see section 1.1).
CLK R (11)	A TTL logic level clock input when in split supply operation ($\pm$2.5V to $\pm$7V) and L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see section 1.1).
L. Sh (12)	Level shift pin, selects the logic threshold levels for the desired clock. When tied to V^- it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output.

Pin Descriptions (Pin Numbers) (Continued)

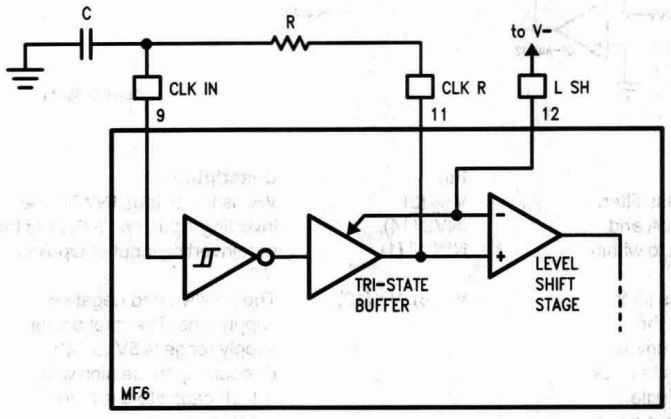
Pin	Description
L. Sh (12)	When the voltage level at this input exceeds [25%($V^+ - V^-$) + V^-] the internal tri-state buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level shift stage. The CLK R threshold level is now 2V above the voltage applied to the L. Sh pin. Driving the CLK R pin with TTL logic levels can be accomplished through the use of split supplies and by tying the L. Sh pin to system ground.

1.0 MF6 Application Hints

The MF6 is comprised of a non-inverting unity gain lowpass sixth order Butterworth switched capacitor filter section and two undedicated CMOS Op-Amps. The switched capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the lowpass filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock to cutoff frequency ratio (f_{CLK}/f_c) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock to cutoff frequency ratio (or the sampling rate) the closer this approximation is to the theoretical Butterworth response. The MF6 is available in f_{CLK}/f_c ratios of 50:1 (MF6-50) or 100:1 (MF6-100).

1.1 CLOCK INPUTS

The MF6 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. The oscillator's frequency is dependent on the buffer's threshold levels as well as on the resistor/capacitor tolerance (see *Figure 1*).



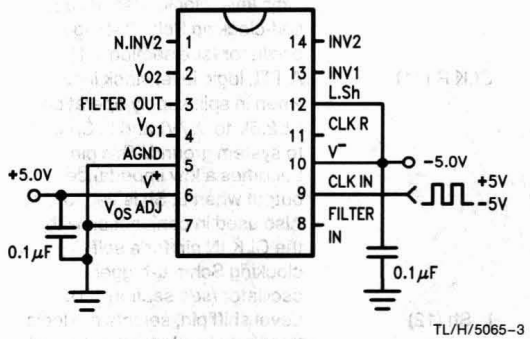
$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\frac{V_{T+}}{V_{T-}}\right]}$$

Typically for $V_{CC} = V^+ - V^- = 10V$:

$$f_{CLK} = \frac{1}{1.69\ RC}$$

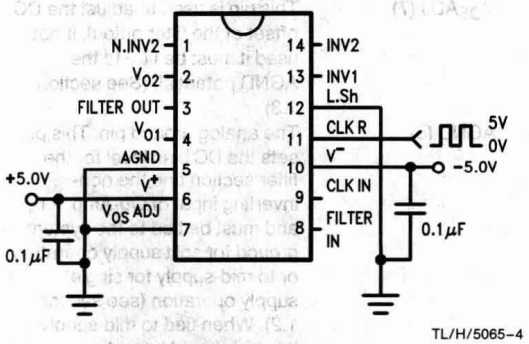
TL/H/5065–12

FIGURE 1. Schmitt Trigger R/C Oscillator



TL/H/5065–3

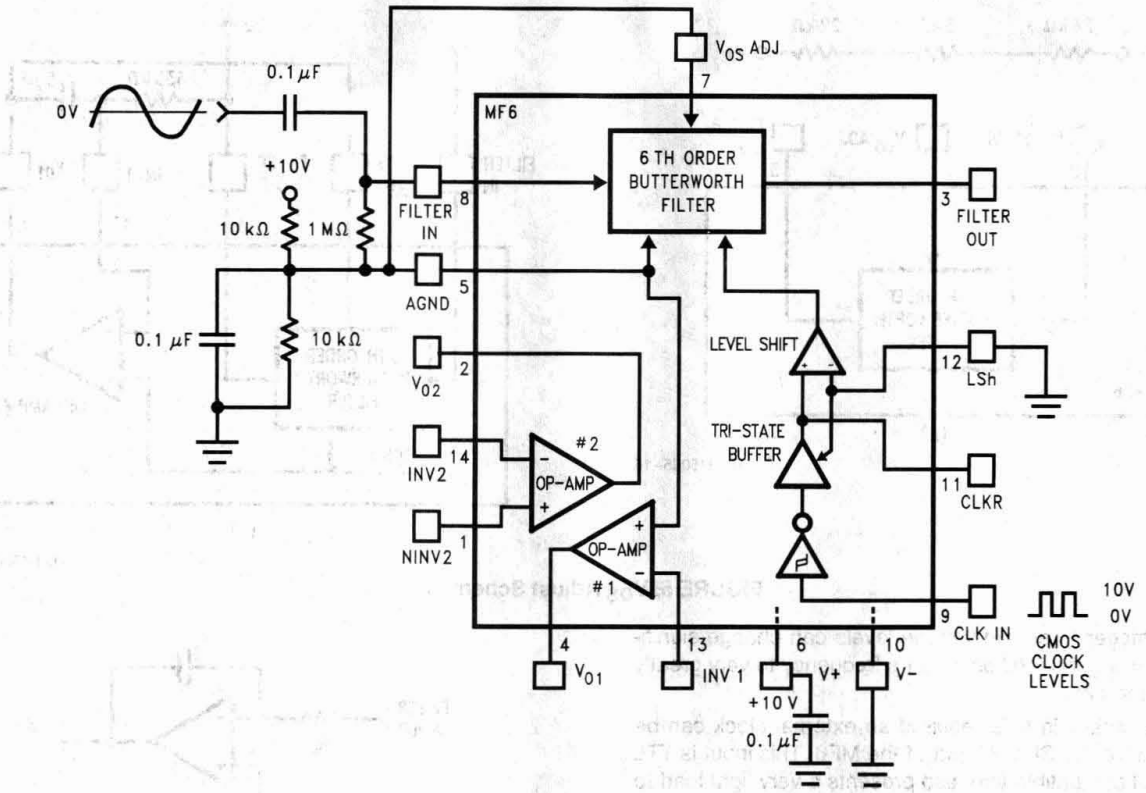
FIGURE 2. Dual Supply Operation MF6 Driven with CMOS Logic Level Clock ($V_{IH} \geq 0.8\ V_{CC}$ and $V_{IL} \leq 0.2\ V_{CC}$ where $V_{CC} = V^+ - V^-$)



TL/H/5065–4

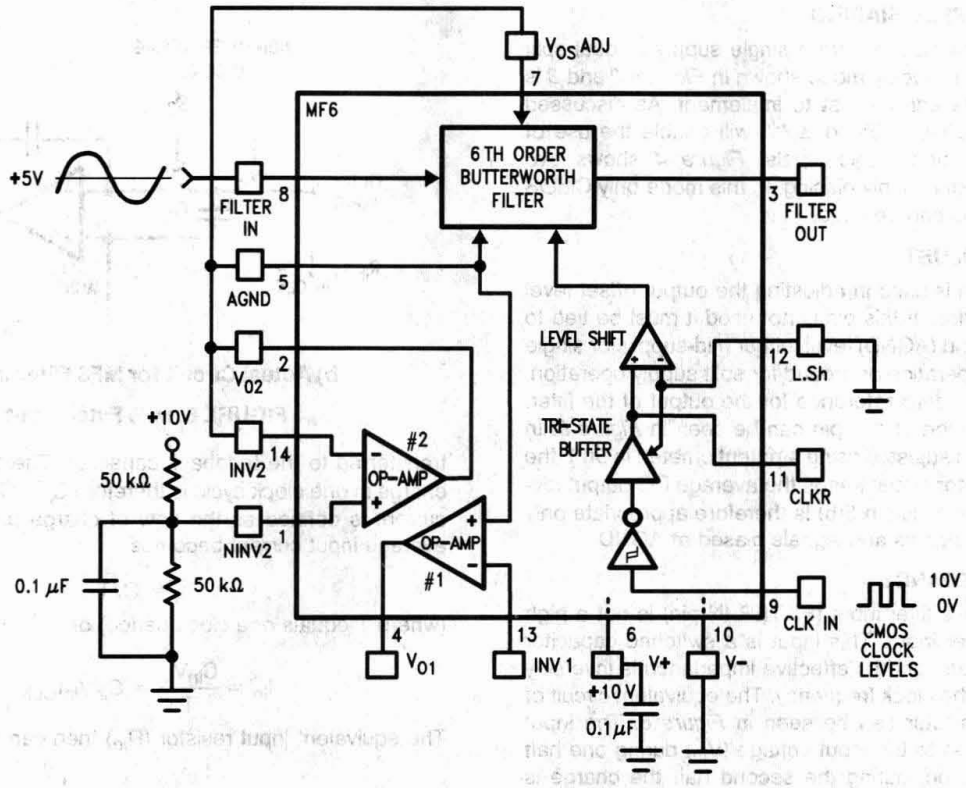
FIGURE 3. Dual Supply Operation MF6 Driven with TTL Logic Level Clock

Application Hints (Continued)



TL/H/5065–14

a) Resistor Biasing of AGND

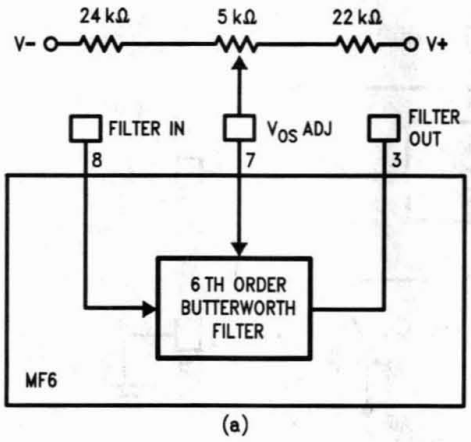


TL/H/5065–15

b) Using Op-Amp 2 to Buffer AGND

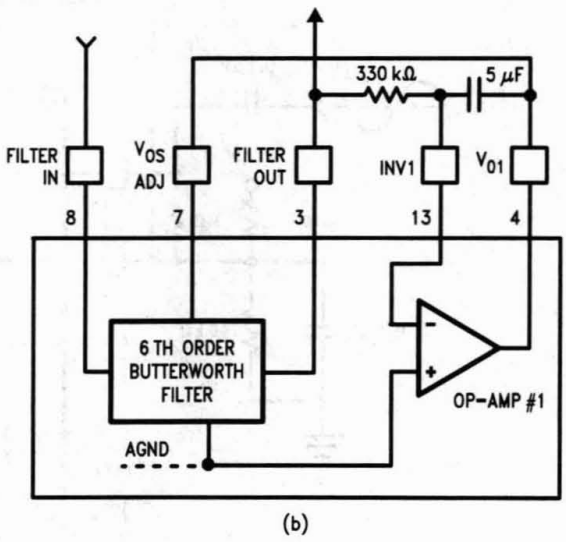
FIGURE 4. Single Supply Operation

Application Hints (Continued)



(a)

TL/H/5065–16



(b)

TL/H/5065–17

FIGURE 5. V_{OS} Adjust Schemes

Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accuracy in f_C is required an external clock can be used to drive the CLK R input of the MF6. This input is TTL logic level compatible and also presents a very light load to the external clock source ($\sim 2\ \mu A$) with split supplies and L. Sh tied to system ground. The logic level is programmed by the voltage applied to level shift (L. Sh) pin (See the Pin description for L. Sh pin).

1.2 POWER SUPPLY BIASING

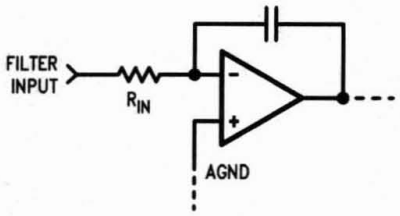
The MF6 can be biased from a single supply or dual split supplies. The split supply mode shown in *Figures 2* and *3* is the most flexible and easiest to implement. As discussed earlier split supplies, ±5V to ±7V, will enable the use of TTL or CMOS clock logic levels. *Figure 4* shows two schemes for single supply biasing. In this mode only CMOS clock logic levels can be used.

1.3 OFFSET ADJUST

The VosADJ pin is used in adjusting the output offset level of the filter section. If this pin is not used it must be tied to the analog ground (AGND) level, either mid-supply for single ended supply operation or ground for split supply operation. This pin sets the zero reference for the output of the filter. The implementation of this pin can be seen in *Figure 5*. In 5(a), DC offset is adjusted using a potentiometer; in 5(b), the Op-Amp integrator circuit keeps the average DC output level at AGND. The circuit in 5(b) is therefore appropriate only for AC-coupled signals and signals biased at AGND.

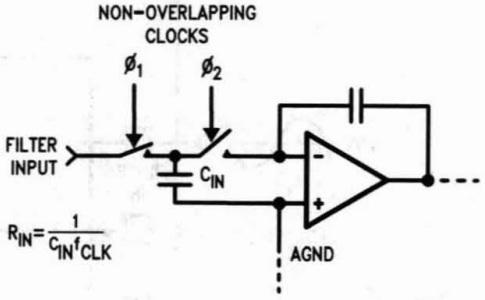
1.4 INPUT IMPEDANCE

The MF6 lowpass filter input (FILTER IN pin) is not a high impedance buffer input. This input is a switched capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the input to the filter can be seen in *Figure 6*. The input capacitor charges to the input voltage (V_{in}) during one half of the clock period, during the second half the charge is



TL/H/5065–18

a) Equivalent Circuit for MF6 Filter Input



TL/H/5065–19

b) Actual Circuit for MF6 Filter Input

FIGURE 6. MF6 Filter Input

transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{in}V_{in}$, and since current is defined as the flow of charge per unit time the average input current becomes

$$I_{in} = Q/T$$

(where T equals one clock period) or

$$I_{in} = \frac{C_{in}V_{in}}{T} = C_{in}V_{in}f_{CLK}$$

The equivalent input resistor (R_{in}) then can be defined as

$$R_{in} = V_{in}/I_{in} = \frac{1}{C_{in}f_{CLK}}$$

The input capacitor is 2 pF for the MF6-50 and 1 pF for the

Application Hints (Continued)

MF6-100, so for the MF6-100

$$R_{in} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_c \times 100} = \frac{1 \times 10^{10}}{f_c}$$

and

$$R_{in} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

for the MF6-50. As shown in the above equations for a given cutoff frequency (f_c) the input impedance remains the same for the MF6-50 and the MF6-100. The higher the clock to center frequency ratio, the greater equivalent input resistance for a given clock frequency. As the cutoff frequency increases the equivalent input impedance decreases. This input resistance will form a voltage divider with the source impedance (R_{source}). Since R_{in} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity its overall gain is given by:

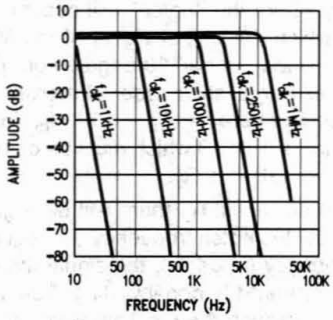
$$A_v = \frac{R_{in}}{R_{in} + R_{source}}$$

If the MF6-50 or the MF6-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{in} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

In this example with a source impedance of 10k the overall gain, if the MF6 had an ideal gain of 1 or 0 dB, would be:

$$A_v = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009 \text{ or } -86.4\ \text{mdB}$$



TL/H/5065–20

FIGURE 7a. MF6-100 ±5V Supplies Amplitude Response

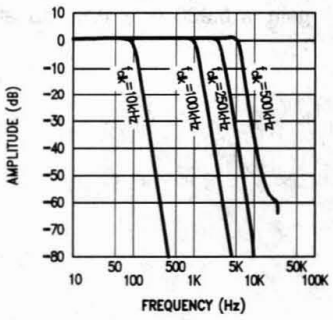


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FIGURE 7c. MF6-100 ±2.5V Supplies Amplitude Response

Since the maximum overall gain error for the MF6 is ±0.3 dB with a $R_s \leq 2\ \text{k}\Omega$ the actual gain error for this case would be +0.21 dB to −0.39 dB.

1.5 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit caused by leakage currents through the internal switches discharging the stored charge on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ \text{Hz},\ I_{leakage} = 1\ \text{pA},\ C = 1\ \text{pF}$$

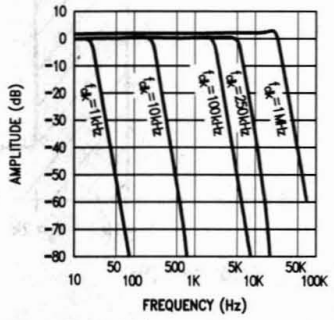
$$V = \frac{1\ \text{pA}}{1\ \text{pF}\ (100\ \text{Hz})} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors increases as the MF6 power supply voltage decreases. This causes a shift in the f_{CLK}/f_c ratio which will become noticeable when the clock frequency exceeds 250 kHz. The amplitude characteristic will stay within tolerance until f_{CLK} exceeds 500 kHz and will peak at about 0.5 dB at the corner frequency with a 1 MHz clock. The response of the MF6 is still a reasonable approximation of the ideal Butterworth lowpass characteristic as can be seen in *Figure 7*.

2.0 Designing with the MF6

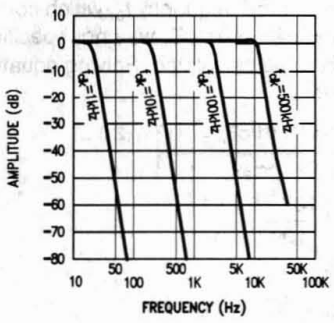
Given any lowpass filter specification two equations will come in handy in trying to determine whether the MF6 will do the job. The first equation determines the order of the lowpass filter required:

$$n = \frac{\log\left(10^{0.1\,A_{min}} - 1\right) - \log\left(10^{0.1\,A_{max}} - 1\right)}{2 \log\left(f_s/f_b\right)} \qquad (1)$$



TL/H/5065–21

FIGURE 7b. MF6-50 ±5V Supplies Amplitude Response



TL/H/5065–23

FIGURE 7d. MF6-50 ±2.5V Supplies Amplitude Response

Designing with the MF6 (Continued)

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at frequency f_b. If the result of this equation is greater than 6, then more than a single MF6 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10 \log [1 + (10^{0.1 A_{max}} - 1)\,(f/f_b)^{2n}] \text{ dB} \quad (2)$$

where n = 6 (the order of the filter).

2.1 A LOWPASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 8* is given. Can the MF6 be used? The order of the Butterworth approximation will have to be determined using eq. 1:

A_{min} = 30 dB, A_{max} = 1.0 dB, f_s = 2 kHz, and f_b = 1 kHz

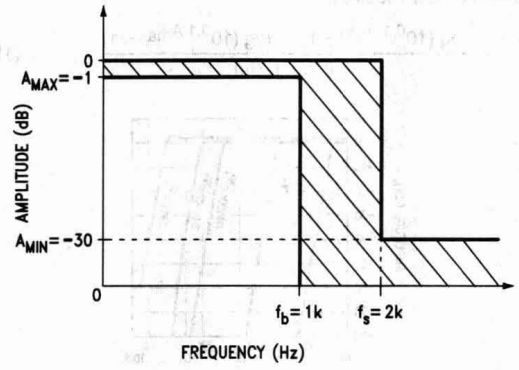
$$n = \frac{\log (10^3 - 1) - \log(10^{0.1} - 1)}{2 \log(2)} = 5.96$$

Since n can only take on integer values, n = 6. Therefore the MF6 can be used. In general, if n is 6 or less a single MF6 stage can be utilized.

Likewise, the attenuation at f_s can be found using equation 2 with the above values and n = 6 giving:

$$\text{Atten (2 kHz)} = 10 \log [1 + (10^{0.1} - 1)\,(2 \text{ kHz}/1 \text{ kHz})^{12}]$$
$$= 30.26 \text{ dB}$$

This result also meets the design specification given in *Figure 8* again verifying that a single MF6 section will be adequate.



TL/H/5065–24

FIGURE 8. Design Example Magnitude Response Specification Where the Response of the Filter Design Must Fall Within the Shaded Area of the Specification

Since the MF6's cutoff frequency f_c, which corresponds to a gain attenuation of −3.01 dB, was not specified in this example it needs to be calculated. Solving equation 2 where f = f_c as follows:

$$f_c = f_b \left[\frac{(10^{0.1(3.01 \text{ dB})} - 1)}{(10^{0.1\,A_{max}} - 1)}\right]^{1/(2n)}$$
$$= 1 \text{ kHz} \left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/12}$$
$$= 1.119 \text{ kHz}$$

where $f_c = f_{CLK}/50$ or $f_{CLK}/100$.

To implement this example for the MF6-50 the clock frequency will have to be set to f_{CLK} = 50(1.116 kHz) = 55.8 kHz or for the MF6-100 f_{CLK} = 100(1.116 kHz) = 111.6 kHz.

2.2 CASCADING MF6s

In the case where a steeper stopband attenuation rate is required two MF6's can be cascaded (*Figure 9*) yielding a 12th order slope of 72 dB per octave. Because the MF6 is a Butterworth filter and therefore has no ripple in its passband, when MF6s are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 10*.

In determining whether the cascaded MF6s will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log (10^{0.05\,A_{min}} - 1) - \log (10^{0.05\,A_{max}} - 1)}{2 \log (f_s/f_b)} \quad (3)$$

$$\text{Attn}(f) = 10 \log [1 + (10^{0.05\,A_{max}} - 1)\,(f/f_b)^{2n}] \text{ dB} \quad (4)$$

where n = 6 (the order of each filter).

Equation 3 will determine whether the order of the filter is adequate ($n \leq 6$) while equation 4 can determine if the required stopband attenuation is met and what actual cutoff frequency (f_c) is required to obtain the particular frequency response desired. The design procedure would be identical to the one shown in section 2.1.

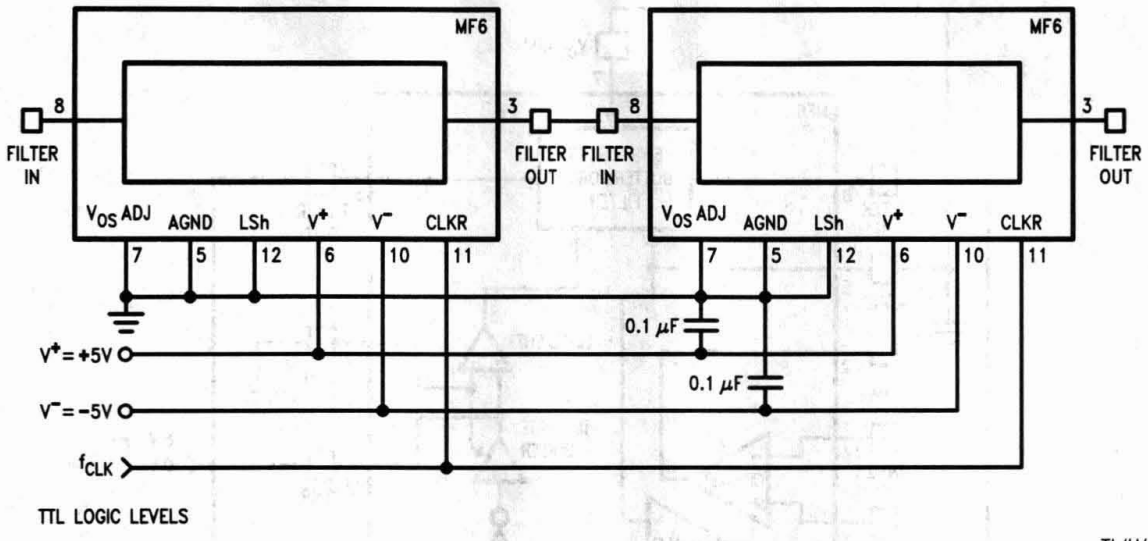
2.3 IMPLEMENTING A "NOTCH" FILTER WITH THE MF6

A "notch" filter with 60 dB of attenuation can be obtained by using one of the Op-Amps, available in the MF6, and three external resistors. The circuit and amplitude response are shown in *Figure 11*.

The frequency where the "notch" will occur is equal to the frequency at which the output signal of the MF6 will have the same magnitude but be 180 degrees out of phase with its input signal. For a sixth order Butterworth filter 180° phase shift occurs where $f = f_n = 0.742\,f_c$. The attenuation at this frequency is 0.12 dB which must be compensated for by making $R_1 = 1.014 \times R_2$.

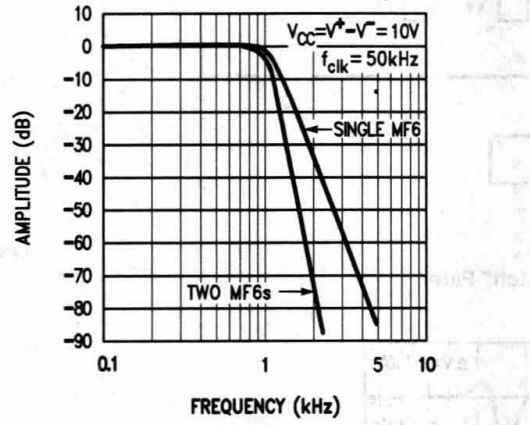
Since R_1 does not equal R_2 there will be a gain inequality above and below the notch frequency. At frequencies below the notch frequency ($f << f_n$), the signal through the filter has a gain of one and is non-inverting. Summing this with the input signal through the Op-Amp yields an overall gain of two or +6 dB. For $f >> f_n$, the signal at the output of the filter is greatly attenuated thus only the input signal will appear at the output of the Op-Amp. With $R_3 = R_1 = 1.014\,R_2$ the overall gain is 0.986 or −0.12 dB at frequencies above the notch.

Designing with the MF6 (Continued)



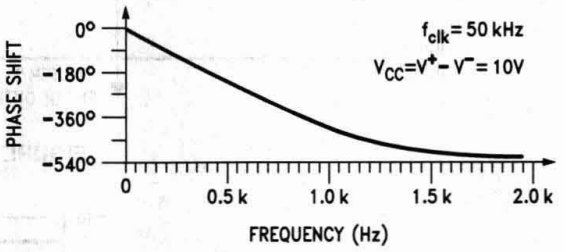
TL/H/5065–25

FIGURE 9. Cascading Two MF6s



TL/H/5065–26

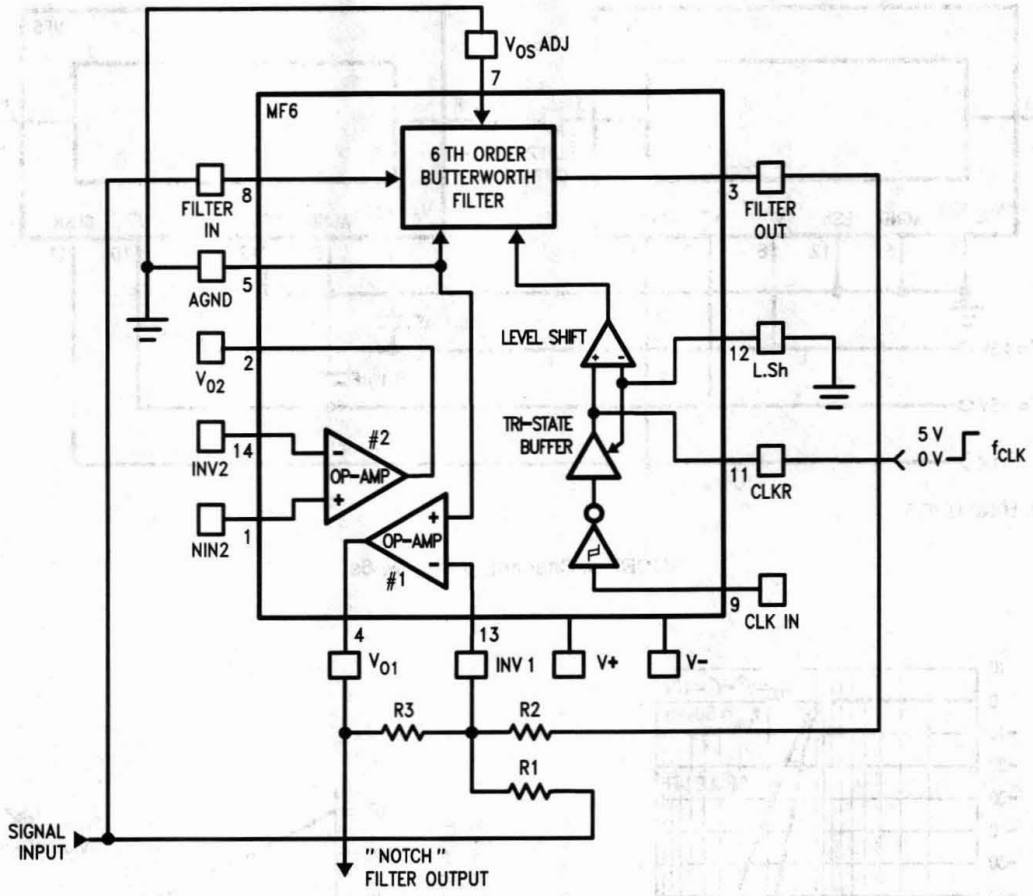
FIGURE 10a. One MF6-50 vs. Two MF6-50s Cascaded



TL/H/5065–27

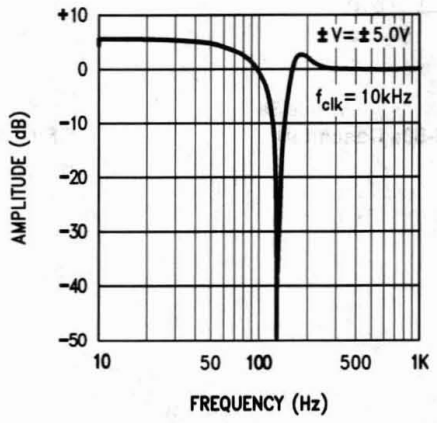
FIGURE 10b. Phase Response of Two Cascaded MF6-50s

Designing with the MF6 (Continued)



TL/H/5065–28

FIGURE 11a. "Notch" Filter



TL/H/5065–29

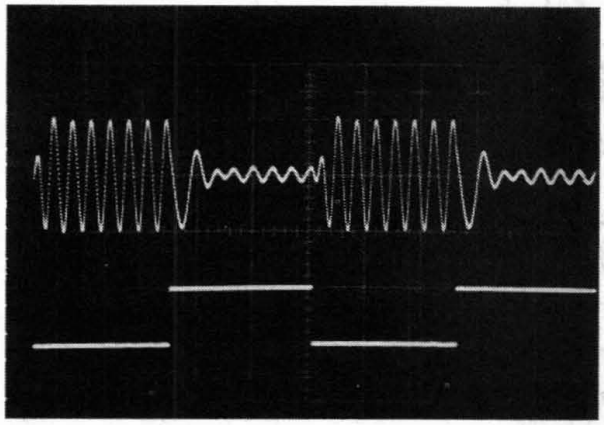
FIGURE 11b. MF6-50 "Notch" Filter Amplitude Response

Designing with the MF6 (Continued)

2.4 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF6 will respond favorably to a sudden change in clock frequency. Distortion in the output signal occurs at the transition of the clock frequency and lasts approximately three cutoff frequency (f_C) cycles. As shown in *Figure 12,* if the control signal is low the MF6-50 has a 100 kHz clock making f_C = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding 1 kHz f_C.

The transient response of the MF6 seen in *Figure 13* is also dependent on the f_C and thus the f_{CLK} applied to the filter. The MF6 responds as a classical sixth order Butterworth lowpass filter.



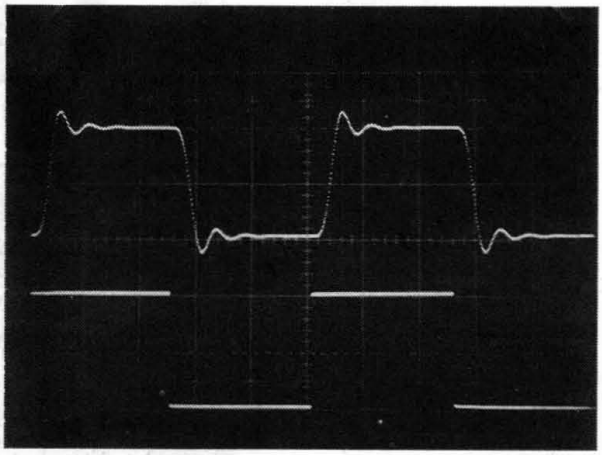
TL/H/5065–30

f_{IN} = 1.5 kHz (scope time base = 2 ms/div)

FIGURE 12. MF6-50 Abrupt Clock Frequency Change

2.5 ALIASING CONSIDERATIONS

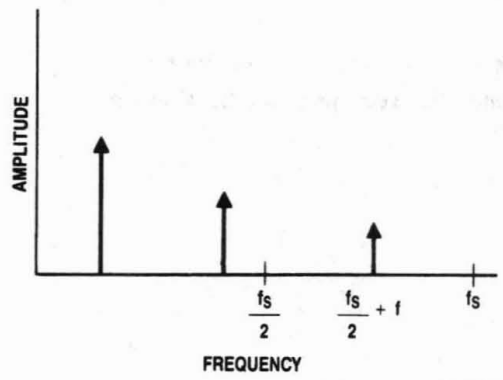
Aliasing effects have to be taken into consideration when input signal frequencies exceed half the sampling rate. For the MF6 this equals half the clock frequency (f_{CLK}). When



TL/H/5065–31

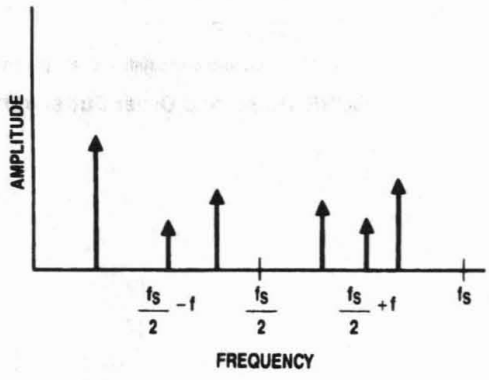
FIGURE 13. MF6-50 Step Input Response, Vertical = 2V/div., Horizontal = 1 ms/div., f_{CLK} = 100 kHz

the input signal contains a component at a frequency higher than half the clock frequency, as in *Figure 14a,* that component will be "reflected" about $f_{CLK}/2$ into the frequency range *below* $f_{CLK}/2$ as in *Figure 14b.* If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the MF6 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level. An example circuit is shown in *Figure 15* using one of the uncommitted Op-Amps available in the MF6.



TL/H/5065–37

(a) Input Signal Spectrum



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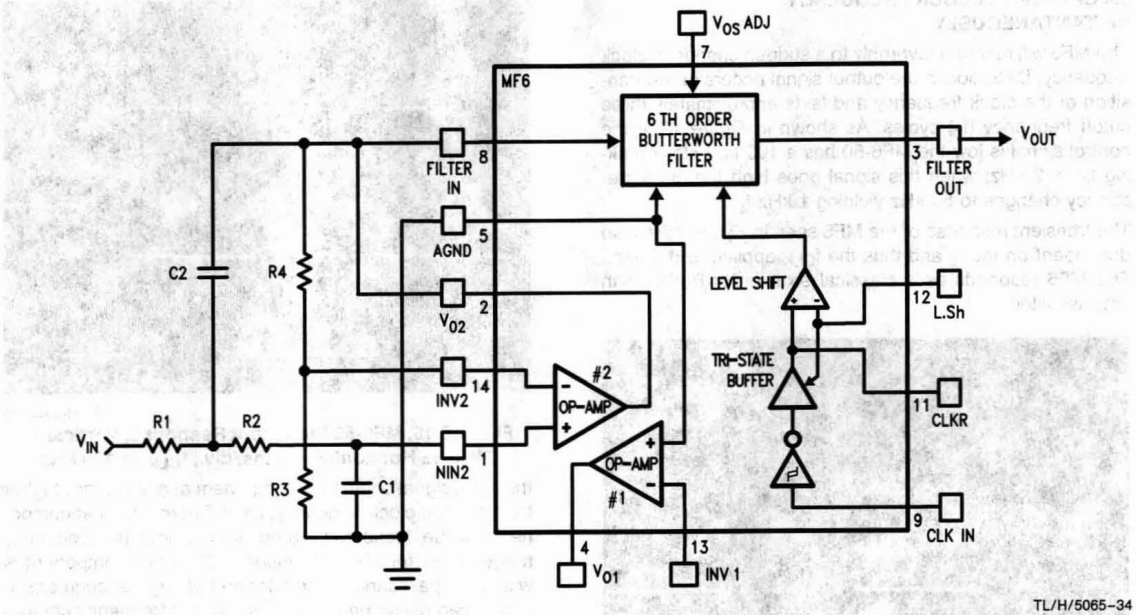
(b) Output Signal Spectrum. Note that the input signal at $f_s/2 + f$ causes an output signal to appear at $f_s/2 - f$.

Figure 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF6, $f_S = f_{CLK}$.

Designing with the MF6 (Continued)



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$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

$H_0 = R_4/R_3$ ($H_0 = 1$ when R_3 and R_4 are omitted and V_{O2} is directly tied to INV2).

Design Procedure:

pick C_1

$$R_2 = \frac{1}{2QC_1\omega_0}$$

for a 2nd Order Butterworth $Q = 0.707$

$$R_2 = \frac{0.113}{C_1f_0}$$

make $R_1 = R_2$

and

$$C_2 = \frac{1}{(2\pi f_0R_1)^2C_1}$$

Note: The parallel combination of R_4 (if used), R_1 and R_2 should be $\geq$ 10 kΩ in order not to load Op-Amp #2.

FIGURE 15. Second Order Butterworth Anti-Aliasing Filter Using Uncommitted Op-Amp #2

National Semiconductor

MF8 4th-Order Switched Capacitor Bandpass Filter

General Description

The MF8 consists of two second-order bandpass filter stages and an inverting operational amplifier. The two filter stages are identical and may be used as two tracking second-order bandpass filters, or cascaded to form a single fourth-order bandpass filter. The center frequency is controlled by an external clock for optimal accuracy, and may be set anywhere between 0.1 Hz and 20 kHz. The ratio of clock frequency to center frequency is programmable to 100:1 or 50:1. Two inputs are available for TTL or CMOS clock signals. The TTL input will accept logic levels referenced to either the negative power supply pin or the ground pin, allowing operation on single or split power supplies. The CMOS input is a Schmitt inverter which can be made to self-oscillate using an external resistor and capacitor.

By using the uncommitted amplifier and resistors for negative feedback, any all-pole (Butterworth, Chebyshev, etc.) filter can be formed. This requires only three resistors for a fourth-order bandpass filter. Q of the second-order stages may be programmed to any of 31 different values by the five "Q logic" pins. The available Q values span a range from 0.5 through 90. Overall filter bandwidth is programmed by connecting the appropriate Q logic pins to either V^+ or V^-. Filters with order higher than four can be built by cascading MF8s.

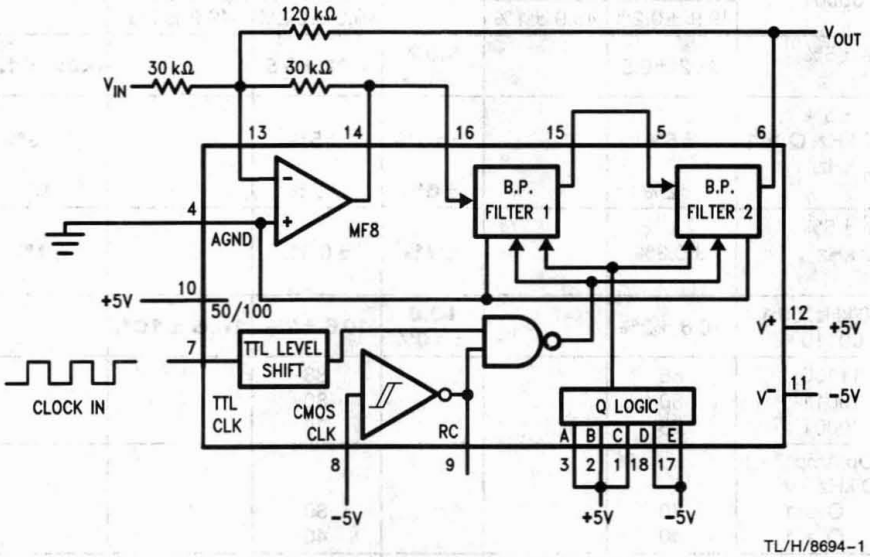
Features

- Center frequency set by external clock
- Q set by five-bit digital word
- Uncommitted inverting op amp
- 4th-order all-pole filters using only three external resistors
- Cascadable for higher-order filters
- Bandwidth, response characteristic, and center frequency independently programmable
- Separate TTL and CMOS clock inputs
- 18 pin 0.3" wide package

Key Specifications

- Center frequency range 0.1 Hz to 20 kHz
- Q range 0.5 to 90
- Supply voltage range 9V to 14V (±4.5V to ±7V)
- Center frequency accuracy 1% over full temperature range

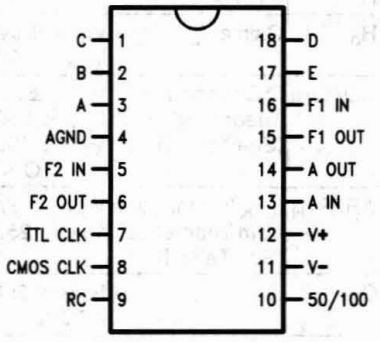
Typical Application & Connection Diagrams



TL/H/8694-1

Fourth-Order Butterworth Bandpass Filter

Dual-In-Line Package



TL/H/8694-2

Top View

Order Number MF8CCJ or MF8CCN
See NS Package Number J18A or N18A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_S = V^+ - V^-$)	−0.3V to +15V
Voltage at any Input (Note 2)	V^- −0.3V to V^+ +0.3V
Input Current at any Input Pin (Note 2)	±1 mA
Output Short-Circuit Current (Note 7)	±1 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	−65°C to +150°C
Soldering Information:	
J Package: 10 sec.	260°C
N Package: 10 sec.	300°C
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF8CCN	$0°C \le T_A \le +70°C$
MF8CCJ	$-40°C \le T_A \le +85°C$
Supply Voltage ($V_S = V^+ - V^-$)	+9V to +14V
$f_{CLK} \times Q$ Range	
for 10 Hz ≤ f_{CLK} ≤ 250 kHz	any Q
for 250 kHz ≤ f_{CLK} ≤ 1 MHz	$f_{CLK} \times Q \le 5$ MHz

Filter Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$, $C_{LOAD} = 50$ pF and $R_{LOAD} = 50$ kΩ on filter output unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter (Notes 4, 5)	Conditions	MF8CCN Typical (Note 9)	MF8CCN Tested Limit (Note 10)	MF8CCN Design Limit (Note 11)	MF8CCJ Typical (Note 9)	MF8CCJ Tested Limit (Note 10)	MF8CCJ Design Limit (Note 11)	Units
H_o	Gain at f_o	f_{CLK} = 250 kHz 100:1 ABCDE = 11100	6.02 ±.05	6.02 ±0.2		6.02 ±0.05	6.02 ±0.2		dB
Q	Q		3.92 ±2%	3.92 ±10%		3.92 ±2%	3.92 ±10%		
R	f_{CLK}/f_o		99.2 ±0.3%	99.2 ±1%		99.2 ±0.3%	99.2 ±1%		
H_o	Gain at f_o	f_{CLK} = 250 kHz 100:1 ABCDE = 10011	6.02 ±0.2	6.02 ±0.5		6.02 ±0.2	6.02 ±0.5		dB
Q	Q		15.5 ±3%	15.5 ±12%		15.5 ±3%	15.5 ±12%		
R	f_{CLK}/f_o		99.7 ±0.3%	99.7 ±1%		99.7 ±0.3%	99.7±1%		
H_o	Gain at f_o	f_{CLK} = 250 kHz 50:1 ABCDE = 00001	5.85 ±0.4	5.85 ±1		5.85 ±0.4	5.85 ±1		dB
Q	Q		55 ±5%	55 ±14%		55 ±5%	55 ±14%		
R	f_{CLK}/f_o		49.9 ±0.2%	49.9 ±1%		49.9 ±0.2%	49.9 ±1%		
H_o	Gain at f_o	V_S = ±5V ±5% $f_{CLK} \le 250$ kHz	6.02 ±0.5		**6.02 ±1.5**	6.02 ±0.5		**6.02 ±1.5**	dB
$\Delta Q/Q_{TH}$	Q Deviation from Theoretical (See Table I)	V_S = ±5V ±5% $f_{CLK} \le 250$ kHz, Q > 1 $f_{CLK} \le 100$ kHz, 1 < Q < 57	±5% ±2%		**±15%** **±6%**	±5% ±2%		**±15%** **±6%**	
$\Delta R/R_{TH}$	f_{CLK}/f_o Deviation from Theoretical (See Table I)	V_S = ±5V ±5% $f_{CLK} \le 250$ kHz	±0.3%		**±1%**	±0.3%		**±1%**	
Q	Q	f_{CLK} = 250 kHz, 50:1 ABCDE = 00110	10.6 ±2%		**10.6 ±10%**	10.6 ±2%	**10.6 ±10%**		
	Dynamic Range (Note 6)	ABCDE = 11100 ABCDE = 10011 ABCDE = 00001	86 80 75			86 80 75			dB dB dB
	Clock Feedthrough	Filter and Op Amp $f_{CLK} \le 250$ kHz Q ≤ 1 Q > 1	 80 40			 80 40			 mV mV
I_S	Maximum Supply Current	f_{CLK} = 250 kHz, no loads on outputs	9	12	**12**	9	**13**		mA
V_{OS}	Maximum Filter Output Offset Voltage	f_{CLK} = 250 kHz, Q = 4 50:1 100:1	 ±40 ±80	 ±120 ±240		 ±40 ±80	 ±120 ±240		 mV mV
V_{OUT}	Minimum Filter Output Swing	R_{LOAD} = 5 kΩ (Note 6)	±4.1	±3.8	**±3.8**	±4.1	**±3.6**		V

Op Amp Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$ and no load on the Op Amp output unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	MF8CCN			MF8CCJ			Units
			Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
V_{OS}	Maximum Input Offset Voltage		±8	±20		±8	±20		mV
I_B	Maximum Input Bias Current		10			10			pA
V_{OUT}	Minimum Output Voltage Swing	$R_{LOAD} = 5\ k\Omega$	±3.5			±3.5			V
A_{VOL}	Open Loop Gain		80			80			dB
GBW	Gain Bandwidth Product		1.8			1.8			MHz
SR	Slew Rate		10			10			V/μs

Logic Input and Output Characteristics

The following specifications apply for $V^+ = +10V$ and $V^- = 0V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	MF8CCN			MF8CCJ			Units
				Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
V_T^+	Positive Threshold Voltage on pin 8	Min	$V_S = V^+ - V^-$ referred to $V^- = 0V$ (Note 8)	$0.7V_S$	$0.58V_S$		$0.7V_S$	$0.58V_S$		V
		Max		$0.7V_S$	$0.89V_S$		$0.7V_S$	$0.89V_S$		V
V_T^-	Negative Threshold Voltage on pin 8	Min	$V_S = V^+ - V^-$ referred to $V^- = 0V$ (Note 8)	$0.35V_S$	$0.11V_S$		$0.35V_S$	$0.11V_S$		V
		Max		$0.35V_S$	$0.47V_S$		$0.35V_S$	$0.47V_S$		V
V_{OH}	Output Voltage on pin 9 (Note 12)	Min High	$I_O = -10\ \mu A$		9.0	**9.0**		**9.0**		V
V_{OL}		Max Low	$I_O = +10\ \mu A$		1.0	**1.0**		**1.0**		V
I_{OH}	Output Current on pin 9	Min Source	Pin 9 tied to V^-	6.0	3.0		6.0	3.0		mA
I_{OL}		Min Sink	Pin 9 tied to V^+	5.0	2.5		5.0	2.5		mA
V_{IH}	Input Voltage on pins: 1, 2, 3, 10, 17, & 18 (Note 12)	Min High		7.0		**9.0**	7.0	**9.0**		V
V_{IL}		Max Low		3.0		**1.0**	3.0	**1.0**		V
I_{IN}	Input Current on pins: 1, 2, 3, 7, 8, 10, 17, & 18				10	**10**		**10**		μA
V_{IH}	Input Voltage on pin 7	Min High	$V^+ = +10V$, $V^- = 0V$ or $V^+ = +5V$, $V^- = -5V$		2.0	**2.0**		**2.0**		V
V_{IL}		Max Low			0.8	**0.8**		**0.8**		V

Note 1: Absolute Maximum Rainges indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the applied voltage at any pin falls outside the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$), the absolute value of current at that pin should be limited to 1 mA or less.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, Θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF8CCN when board mounted is 50°C/W. For the MF8CCJ, this number increases to 65°C/W.

Note 4: The center frequency of each 2nd-order filter section is defined as the frequency where the phase shift through the filter is zero.

Note 5: Q is defined as the measured center frequency divided by the measured bandwidth, where the bandwidth is the difference between the two frequencies where the gain is 3 dB less than the gain measured at the center frequency.

Note 6: Dynamic range is defined as the ratio of the tested minimum output swing of 2.69 Vrms (±3.8V peak-to-peak) to the wideband noise over a 20 kHz bandwidth. For Qs of 1 or less the dynamic range and output swing will degrade because the gain at an internal node is 2/Q. Keeping the input signal level below 1.23xQ Vrms will avoid distortion in this case.

Note 7: If it is possible for a signal output (pin 6, 14, or 15) to be shorted to V^+, V^- or ground, add a series resistor to limit output current.

Note 8: If V^- is anything other than 0V then the value of V^- should be added to the values given in the table. For example for $V^+ = +5V$ and $V^- = -5V$ the typical $V_T^+ = 0.7\ (10V) + (-5V) = +2V$.

Note 9: Typicals are at 25°C and represent the most likely parametric norm.

Note 10: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Design Limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 12: These logic levels have been referenced to V^-. The logic levels will shift accordingly for split supplies.

Pin Descriptions

Q Logic Inputs A, B, C, D, E (3, 2, 1, 18, 17): These inputs program the Qs of the two 2nd-order bandpass filter stages. Logic "1" is V^+ and logic "0" is V^-.

AGND (4): This is the analog and digital ground pin and should be connected to the system ground for split supply operation or biased to mid-supply for single supply operation. For best filter performance, the ground line should be "clean".

V^+ (12), V^- (11): These are the positive and negative power supply inputs. Decoupling the power supply pins with 0.1 μF or larger capacitors is highly recommended.

F1 IN (16), F2 IN (5): These are the inputs to the bandpass filter stages. To minimize gain error the source impedance should be less than 2 kΩ. Input signals should be referenced to AGND.

F1 OUT (15), F2 OUT (6): These are the outputs of the bandpass filter stages.

A IN (13): This is the inverting input to the uncommitted operational amplifier. The non-inverting input is internally connected to AGND.

A OUT (14): This is the output of the uncommitted operational amplifier.

50/100 (10): This pin sets the ratio of the clock frequency to the bandpass center frequency. Connecting this pin to V^+ sets the ratio to 100:1. Connecting it to V^- sets the ratio to 50:1.

TTL CLK (7): This is the TTL-level clock input pin. There are two logic threshold levels, so the MF8 can be operated on either single-ended or split supplies with the logic input referred to either V^- or AGND. When this pin is not used (or when CMOS logic levels are used), it should be connected to either V^+ or V^-.

CMOS CLK (8): This pin is the input to a CMOS Schmitt inverter. Clock signals with CMOS logic levels may be applied to this input. If the TTL input is used this pin should be connected to V^-.

RC (9): This pin allows the MF8 to generate its own clock signal. To do this, connect an external resistor between the RC pin and the CMOS Clock input, and an external capacitor from the CMOS Clock input to AGND. The TTL Clock input should be connected to V^- or V^+. When the MF8 is driven from an external clock, the RC pin should be left open.

1.0 Application Information

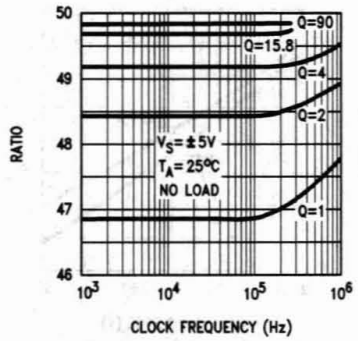
1.1 INTRODUCTION

A simplified block diagram for the MF8 is shown in *Figure 1*. The analog signal path components are two identical 2nd-order bandpass filters and an operational amplifier. Each filter has a fixed voltage gain of 2. The filters' cutoff frequency is proportional to the clock frequency, which may be applied to the chip from an external source or generated internally with the aid of an external resistor and capacitor. The proportionality constant f_{CLK}/f_0 can be set to either 50 or 100 depending on the logic level on pin 10. The "Q" of the two filters can have any of 31 values ranging from 0.5 to 90 and is set by the logic levels on pins 1, 2, 3, 17, and 18. Table I shows the available values of Q and the logic levels required to obtain them. The operational amplifier's non-inverting input is internally grounded, so it may be used only for inverting applications.

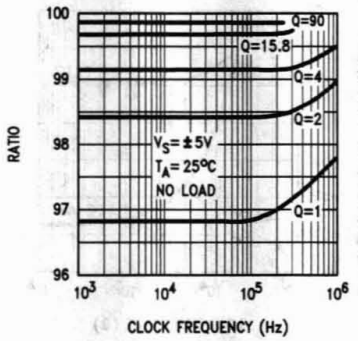
The components in the analog signal path can be interconnected in several ways, three of which are illustrated in *Figures 2a, 2b* and *2c*. The two second-order filter sections can be used as separate filters whose center frequencies track very closely as in *Figure 2a*. Each filter section has a high input impedance and low output impedance. The op amp may be used for gain scaling or other inverting functions. If sharper cutoff slopes are desired, the two filter sections may be cascaded as in *Figure 2b*. Again, the op amp is uncommitted. The circuit in *Figure 2c* uses both filter sections with the op amp and three resistors to build a "multiple feedback loop" filter. This configuration offers the greatest flexibility for fourth-order bandpass designs. Virtually any fourth-order all pole response shape (Butterworth, Chebyshev) can be obtained with a wide range of bandwidths, simply by proper choice of resistor values and Q. The three connection schemes in *Figure 2* will be discussed in more detail in Sections 1.4 and 1.5.

Typical Performance Characteristics

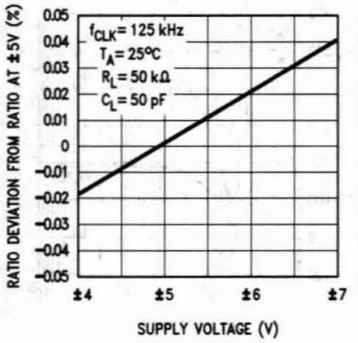
f_{CLK}/f_o Ratio vs Clock Frequency—50:1 Mode



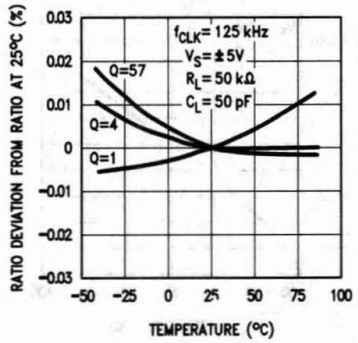
f_{CLK}/f_o Ratio vs Clock Frequency—100:1 Mode



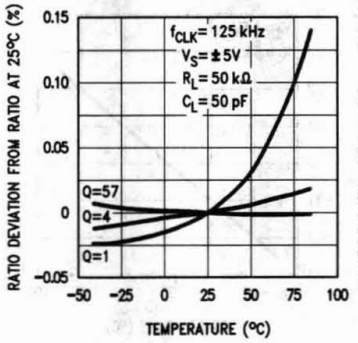
f_{CLK}/f_o Ratio vs Supply Voltage—50:1 and 100:1 Mode



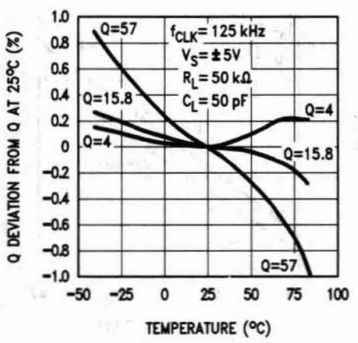
f_{CLK}/f_o Ratio vs Temperature—100:1 Mode



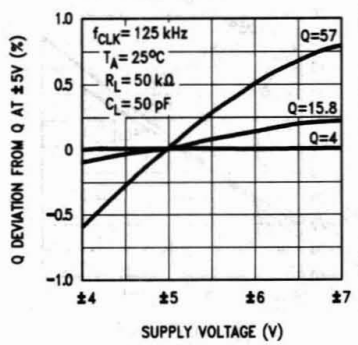
f_{CLK}/f_o Ratio vs Temperature—50:1 Mode



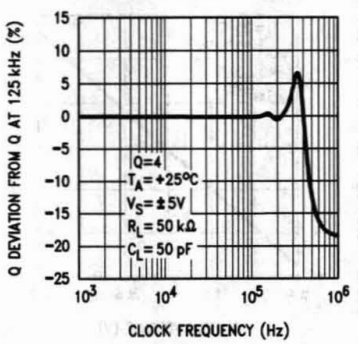
Q vs Temperature—50:1 and 100:1



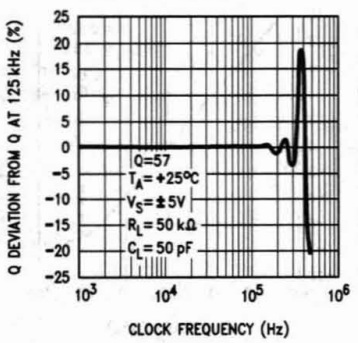
Q vs Supply Voltage—50:1 and 100:1



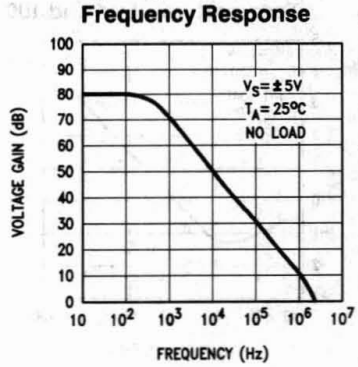
Q vs Clock Frequency—50:1 and 100:1



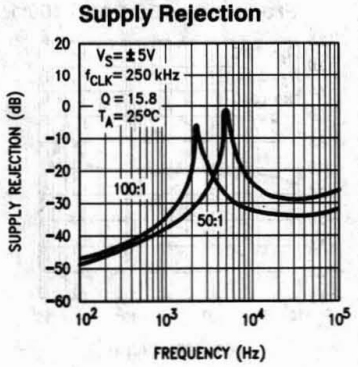
Q vs Clock Frequency—50:1 and 100:1



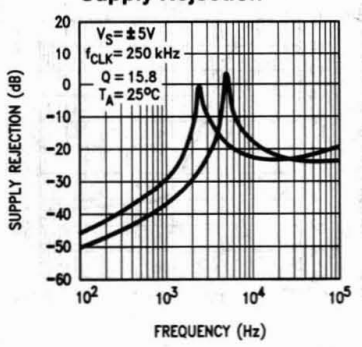
Op Amp—Open Loop Frequency Response



Positive Power Supply Rejection



Negative Power Supply Rejection



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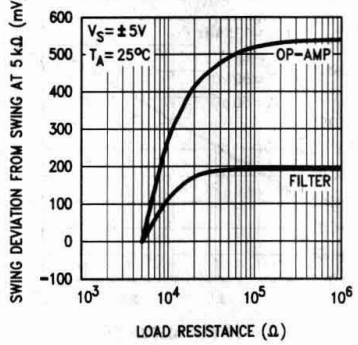
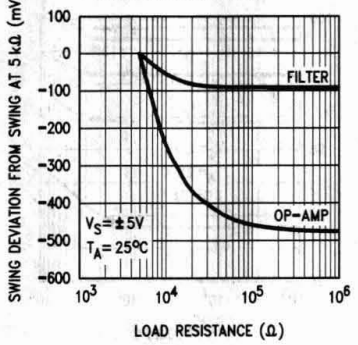
Typical Performance Characteristics (Continued)

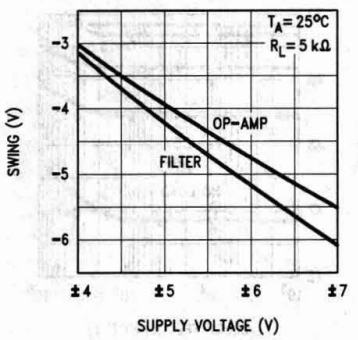
Positive Swing vs Load Resistance



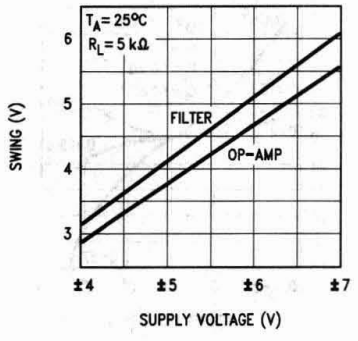
Negative Swing vs Load Resistance



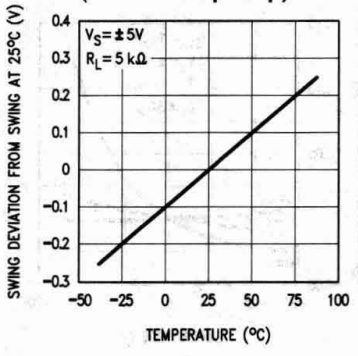
Negative Swing vs Supply Voltage



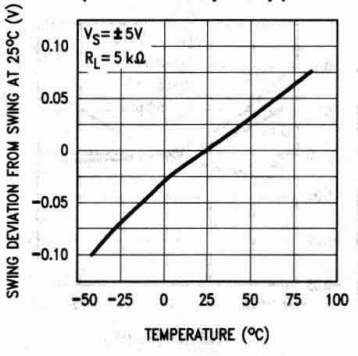
Positive Swing vs Supply Voltage



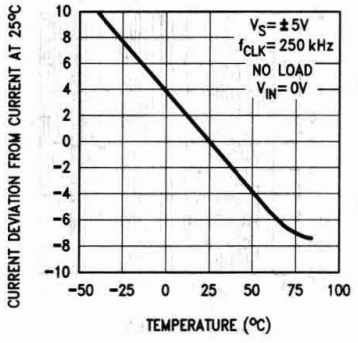
Negative Swing vs Temperature (Filter and Op Amp)



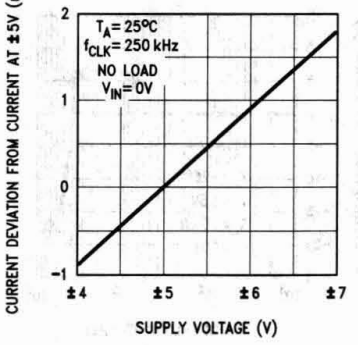
Positive Swing vs Temperature (Filter and Op Amp)



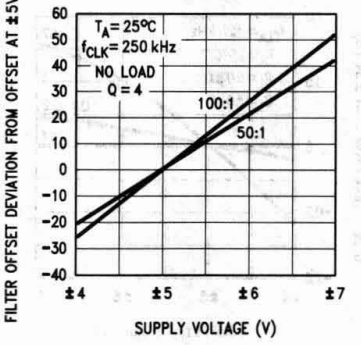
Supply Current vs Temperature



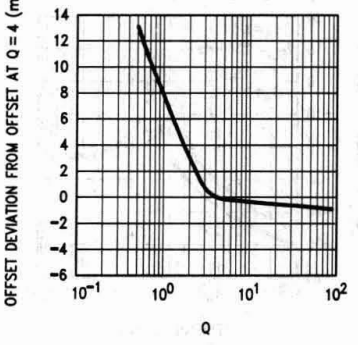
Supply Current vs Supply Voltage



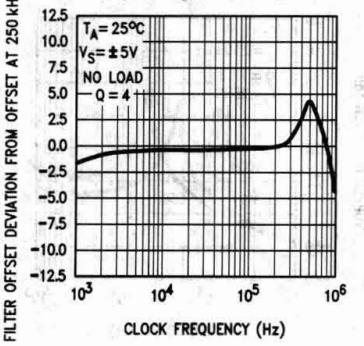
Filter Offset Voltage vs Supply Voltage



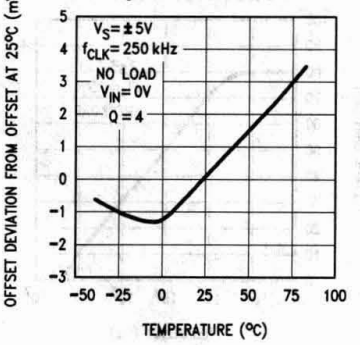
Filter Offset Voltage vs Q—50:1 and 100:1



Filter Offset Voltage vs Clock Frequency—50:1 and 100:1



Filter Offset Voltage vs Temperature—50:1 and 100:1



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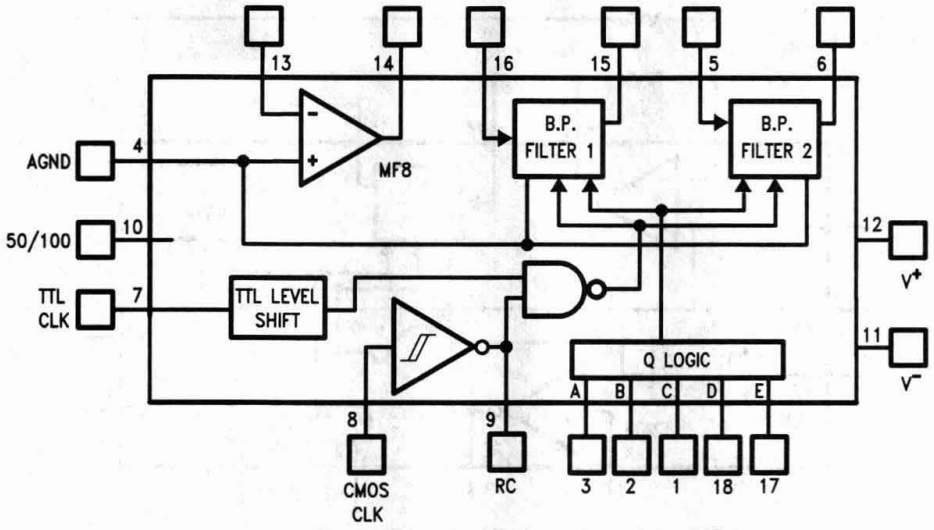
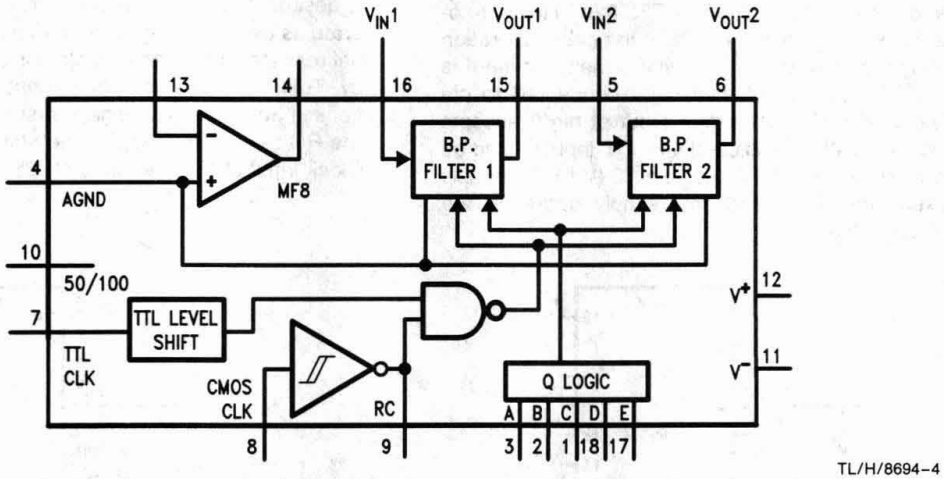
1.0 Application Information (Continued)



TL/H/8694-3

FIGURE 1. Simplified Block Diagram of the MF8



TL/H/8694-4

FIGURE 2a. Separate Second-Order "Tracking" Filters

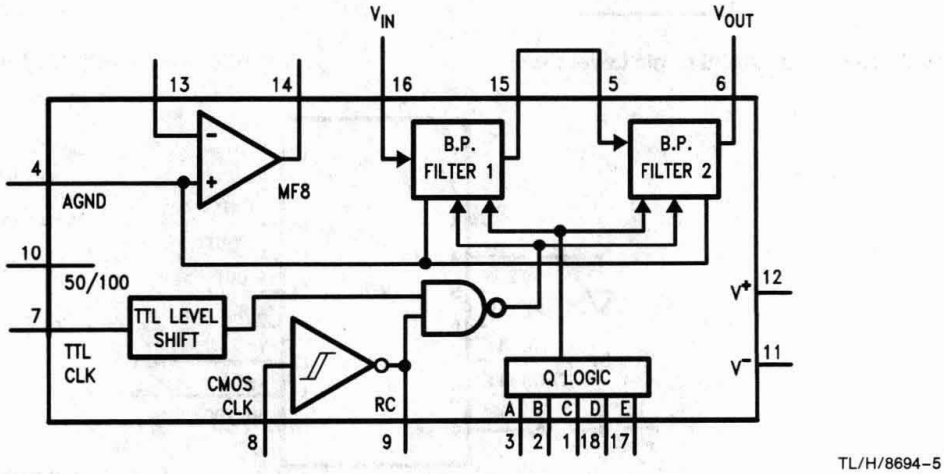


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FIGURE 2b. Fourth-Order Bandpass Made by Cascading Two Second-Order Stages

1.0 Application Information (Continued)

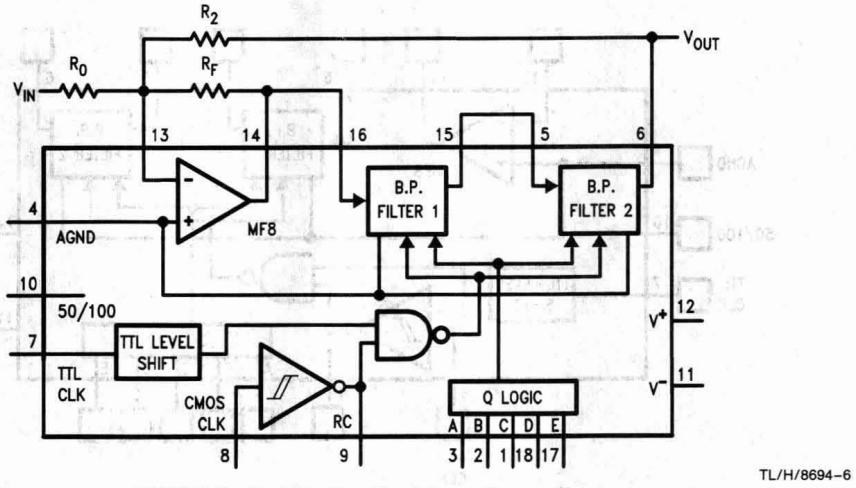

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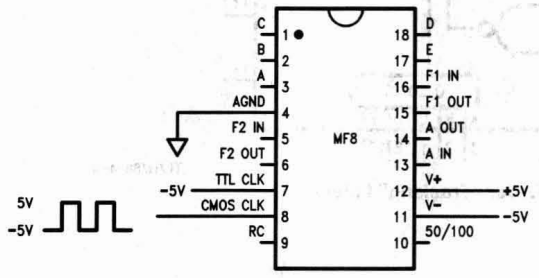
FIGURE 2c. Multiple Feedback Loop Connection

1.2 CLOCKS

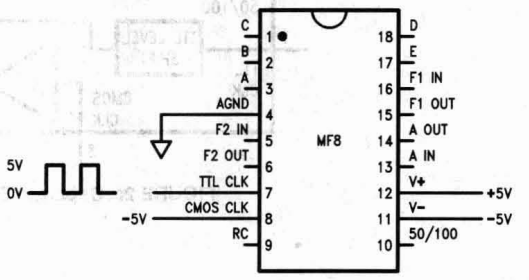
The MF8 has two clock input pins, one for CMOS logic levels and the other for TTL levels. The TTL (pin 7) input automatically adjusts its switching threshold to enable operation on either single or split power supplies. When this input is used, the CMOS logic input should be connected to pin 11(V^-). The CMOS Schmitt trigger input at pin 8 accepts CMOS logic levels. When it is used, the TTL input should be connected to either pin 11 (V^-) or pin 12 (V^+). The basic clock hookups for single and split supply operation are shown in *Figures 3* and *4*.

Clock signals derived from a crystal-controlled oscillator are recommended when maximum center frequency accuracy is desired, but in less critical applications the MF8 can generate its own clock signal as in *Figures 3c* and *4c*. An external resistor and capacitor determine the oscillation frequency. Tolerance of these components and part-to-part variations in Schmitt-trigger logic thresholds limit the accuracy of the RC clock frequency. In the self-clocked mode the TTL Clock input should be connected to either pin 11 or pin 12.



TL/H/8694–7

(a) MF8 Driven with CMOS Logic Level Clock



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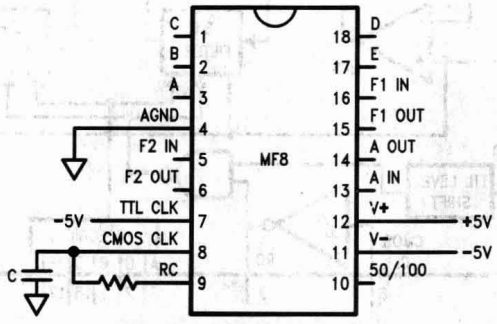
(b) MF8 Driven with TTL Logic Level Clock



$$f_{CLK} = \frac{1}{RC \ln\left|\left(\frac{V_S - V_{T-}}{V_S - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right|}$$

Typically for $V_S^* = 10V$

$$f_{CLK} = \frac{1}{1.69\,RC}$$

$^*V_S = V^+ - V^-$

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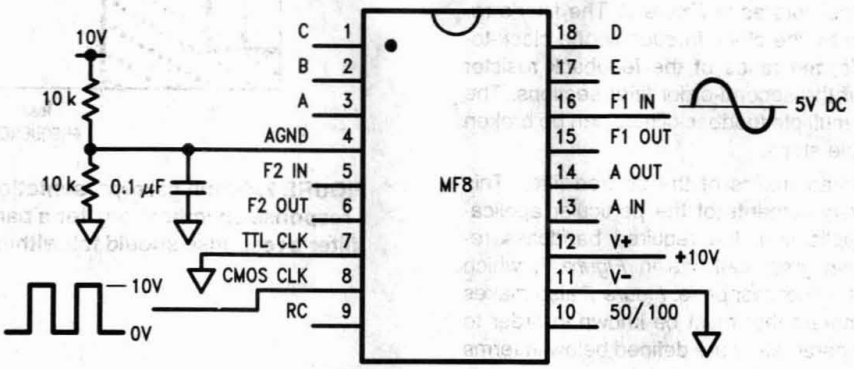
(c) MF8 Driven with Schmitt Trigger Oscillator

FIGURE 3. Dual Supply Operation

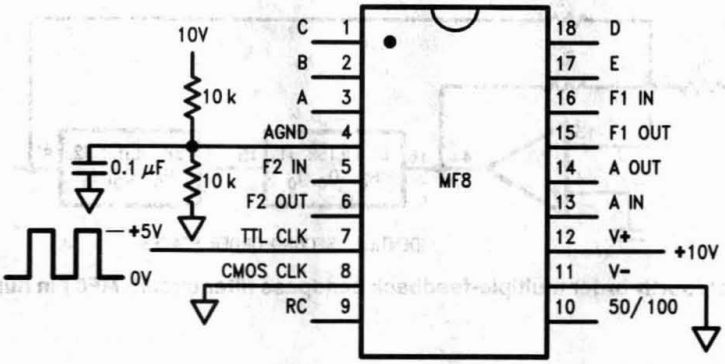
1.0 Application Information (Continued)

1.3 POWER SUPPLIES AND ANALOG GROUND

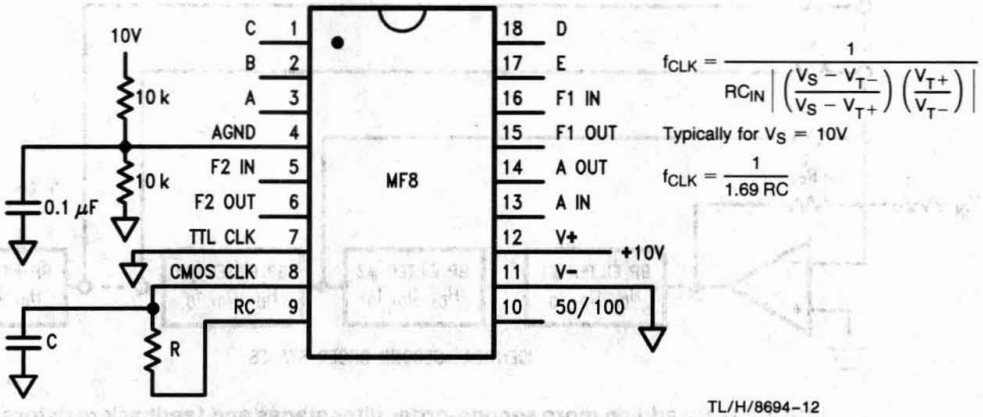
The MF8 can be operated from single or dual-polarity power supplies. For dual-supply operation, the analog ground (pin 4) should be connected to system ground. When single supplies are used, pin 4 should be biased to $V^+/2$ as in *Figures 3* and *4*. The input signal should either be capacitively coupled to the filter input or biased to $V^+/2$. It is strongly recommended that each power supply pin be bypassed to ground with at least a 0.1 μF ceramic capacitor. In single supply applications, with V^- connected to ground, V^+ and AGND should be bypassed to system ground.



(a) MF8 Driven with CMOS Logic Level Clock



(b) MF8 Driven with TTL Logic Clock



(c) MF8 Driven with the Schmitt Trigger Oscillator

FIGURE 4. Single supply operation. The AGND pin must be biased to mid-supply. The input signal should be dc biased to mid-supply or capacitor-coupled to the input pin.

1.0 Application Information (Continued)

1.4 MULTIPLE FEEDBACK LOOP CONFIGURATION

The multi-loop approach to building bandpass filters is highly flexible and stable, yet uses few external components. *Figure 5* shows the MF8's internal operational amplifier and two second-order filter stages with three external resistors in a fourth-order multiple feedback configuration. Higher-order filters may be built by adding more second-order sections and feedback resistors as in *Figure 6*. The filter's response is determined by the clock frequency, the clock-to-center-frequency ratio, the ratios of the feedback resistor values, and the Qs of the second-order filter sections. The design procedure for multiple feedback filters can be broken down into a few simple steps:

1) Determine the characteristics of the desired filter. This will depend on the requirements of the particular application. For a given application, the required bandpass response can be shown graphically as in *Figure 7*, which shows the limits for the filter response. *Figure 7* also makes use of several parameters that must be known in order to design a filter. These parameters are defined below in terms of *Figure 7*.

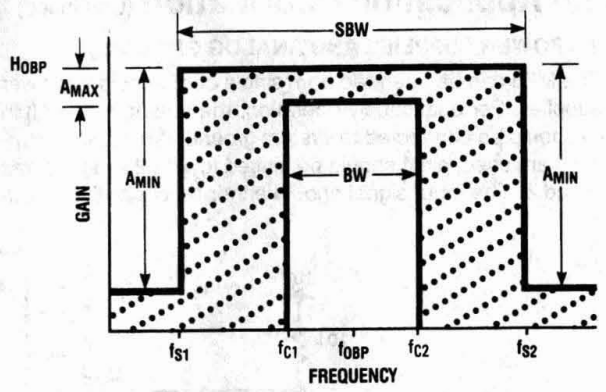


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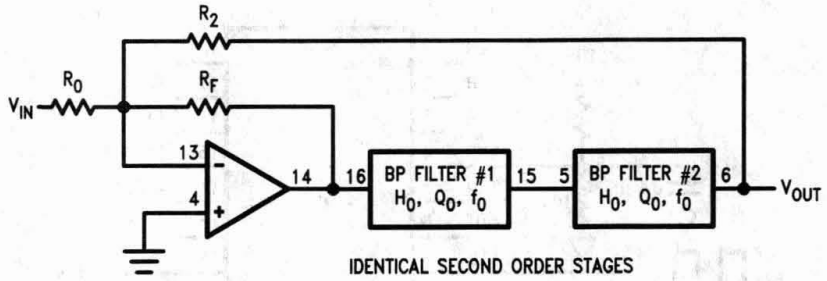
FIGURE 7. Graphical representation of the amplitude response specifications for a bandpass filter. The filter's response should fall within the shaded area.



TL/H/8694–13

FIGURE 5. General fourth-order multiple-feedback bandpass filter circuit. MF8 pin numbers are shown.

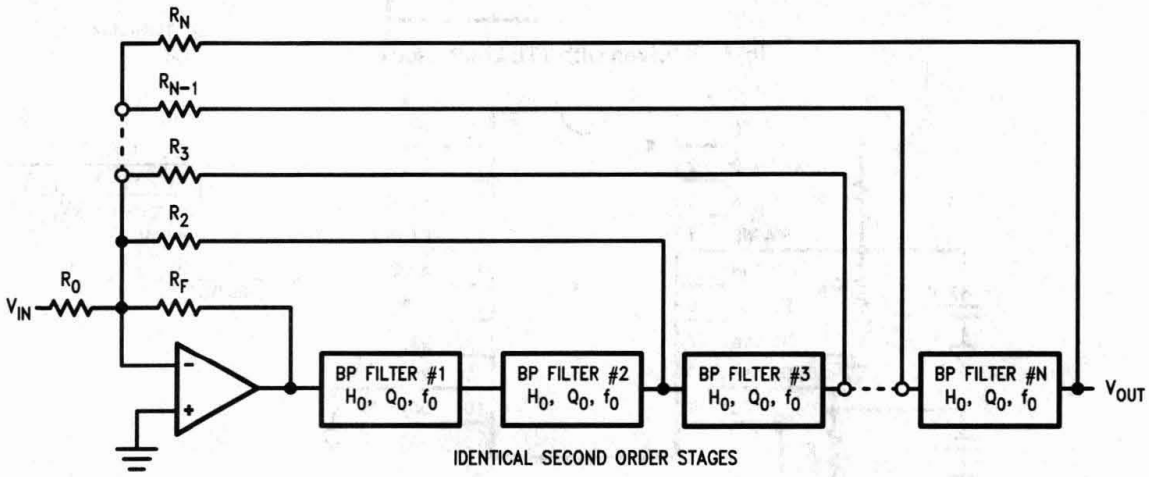


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FIGURE 6. By adding more second-order filter stages and feedback resistors, higher order multiple-feedback filters may be built.

1.0 Application Information (Continued)

f_{C1} and f_{C2}: The filter's lower and upper cutoff frequencies. These define the filter's passband.

f_{S1} and f_{S2}: The boundaries of the filter's stopband.

BW: The filter's bandwidth. BW = $f_{C2} - f_{C1}$.

SBW: The width of the filter's stopband. SBW = $f_{S2} - f_{S1}$.

f_0: The center frequency of the filter. f_0 is equal to the geometric mean of f_{C1} and f_{C2}: $f_0 = \sqrt{f_{C1}f_{C2}}$. f_0 is also equal to the geometric mean of f_{S1} and f_{S2}.

H_{0BP}: The nominal passband gain of the bandpass filter. This is normally taken to be the gain at f_0.

f_0/BW: The ratio of the center frequency to the bandwidth. For second-order filters, this quantity is also known as "Q".

SBW/BW: The ratio of stopband width to bandwidth. This quantity is also called "Omega" and may be represented by the symbol "Ω".

A_{max}: The maximum allowable gain variation within the filter passband. This will depend on the system requirements, but typically ranges from a fraction of a dB to 3 dB.

A_{min}: The minimum allowable attenuation in the stopband. Again, the required value will depend on system constraints.

2). Choose a Butterworth or Chebyshev response characteristic. Butterworth bandpass filters are monotonic on either side of the center frequency, while Chebyshev filters will have "ripple" in the passband, but generally faster attenuation outside the passband. Chebyshev filters are specified according to the amount of ripple (in dB) within the passband.

3) Determine the filter order necessary to meet the response requirements defined above. This may be done with the aid of the nomographs in *Figures 8* and *9* for Butterworth and Chebyshev filters. To use the nomographs, draw a line through the desired values on the A_{MAX}/A_{MIN} scales to the left side of the graph. Draw a horizontal line to the right of this point and mark its intersection with the vertical line corresponding to the required ratio SBW/BW. The required filter order will be equal to the number of the curve falling on or just above the intersection of the two lines. This is illustrated in *Figure 10* for a Chebyshev filter with 1 dB ripple, 30 dB minimum attenuation in the stopband, and SBW/BW = 3. From the *Figure,* the required filter order is 6.

4) The design tables in section 2.0 can now be used to find the component values that will yield the desired response for filters of order 4 through 12. The "K_n" give the ratios of resistors "R_n" to R_F, and K_Q is Q divided by f_0/BW.

As an example of the Tables' use, consider a fourth-order Chebyshev filter with 0.5 dB ripple and f_0/BW = 6. Begin by choosing a convenient value for R_F, such as 100 kΩ. From the "0.5 dB Chebyshev" filter table, $K_0 = R_0/R_F = 1.3405$. This gives $R_0 = R_F \times 1.345 = 134.05$k. In a similar manner, R_2 is found to equal 201.61k. Q is found using the column labeled K_Q. This gives $Q = K_Q \times f_0/BW = 8.4174$.

Table I shows the available Q values; the nearest value is 8.5, which is programmed by tying pins 1, 2, 3, and 18 to V^+ and pin 17 to V^-.

Note that the resistor values obtained from the tables are normalized for center frequency gain $H_{OBP} = 1$. For different gains, simply divide R_0 by the desired gain.

5) Choose the clock-to-center-frequency ratio. This will nominally be 100:1 when pin 10 is connected to pin 12(V^+) and 50:1 when pin 10 is connected to pin 11(V^-). 100:1 generally gives a response curve nearer the ideal and fewer (if any) problems with aliasing, while 50:1 allows operation over the highest octave of center frequencies (10 kHz to 20 kHz). Supply the MF8 with a clock signal of the appropriate frequency to either the TTL or CMOS input, depending on the available clock logic levels.

TABLE I. Q and Clock-to-Center-Frequency Ratio Versus Logic Levels on "Q-set" Pins

	50:1 mode		100:1 mode	
ABCDE	**F_{CLK}/F_o**	**Q**	**F_{CLK}/F_o**	**Q**
10000	43.7	0.45	94.0	0.47
11000	45.8	0.71	95.8	0.73
01000	46.8	0.96	96.8	0.98
10100	48.4	2.0	98.4	2.0
00100	48.7	2.5	98.7	2.5
01100	48.9	3.0	98.9	3.0
11100	49.2	4.0	99.2	4.0
01010	49.3	5.0	99.3	5.0
10010	49.4	5.7	99.4	5.7
10110	49.4	6.4	99.4	6.4
00010	49.5	7.6	99.5	7.6
11110	49.6	8.5	99.6	8.5
00110	49.6	10.6	99.6	10.6
11001	49.6	11.7	99.6	11.7
11010	49.7	12.5	99.7	12.5
11101	49.7	13.6	99.7	13.6
01001	49.7	14.7	99.7	14.7
10011	49.7	15.8	99.7	15.8
10101	49.7	16.5	99.7	16.5
01110	49.7	17	99.7	17
10001	49.8	19	99.8	19
10111	49.8	22	99.8	22
11011	49.8	27	99.8	27
11111	49.8	30	99.8	30
00101	49.8	33	99.8	33
01011	49.8	40	99.8	40
00111	49.8	44	99.8	44
00001	49.9	57	99.9	57
01101	49.9	68	99.9	68
00011	49.9	79	99.9	79
01111	49.9	90	99.9	90

1.0 Application Information (Continued)

Higher-order filters are designed in a similar manner. An eighth-order Chebyshev with 0.1 dB ripple, center frequency equal to 1 kHz, and 100 Hz bandwidth, for example, could be built as in *Figure 11* with the following component values:

$R_0 = 79.86k$
$R_F = 100k$
$R_2 = 57.82k$
$R_3 = 188.08k$
$R_4 = 203.42k$

Pins 1, 3, 17 and 18 high, pin 2 low. For 100:1 clock-to-center-frequency ratio, pin 10 is tied to V^+ and the clock frequency is 100 kHz. For 50:1 clock-to-center-frequency ratio, pin 10 is tied to V^- and the clock frequency is 50 kHz.

When building filters of order 4 or higher, best performance will always be realized when the filter blocks are cascaded in numerical order: Filter 1 (pins 16 and 15) should always precede Filter 2 (pins 5 and 6). If a second MF8 is used, Filter 2 of the first MF8 should precede Filter 1 of the second MF8, and so on.

Dynamic Considerations

Some filter response characteristics will result in high gain at certain internal nodes, particularly at the op amp output. This can cause clipping in intermediate stages even when no clipping is evident at the filter output. The consequences are significant distortion and degradation of the overall transfer function. The likelihood of clipping at the op amp output becomes greater as R_F/R_0 increases. As the design tables show, R_F/R_0 increases with increasing filter order and increasing ripple. It is good practice to keep out-of-band input signal levels small enough that the first stage can't overload.

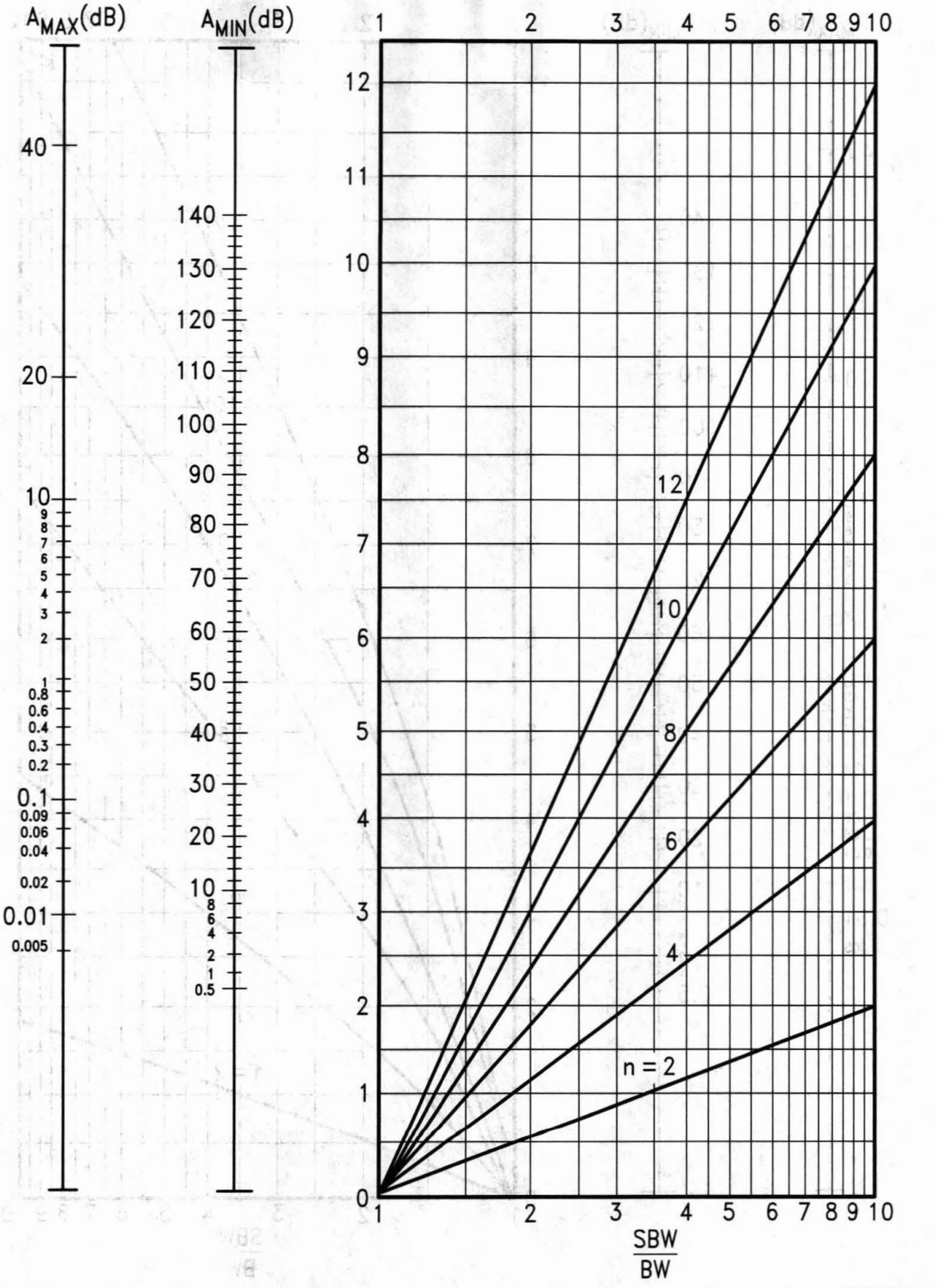

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FIGURE 8. Butterworth Bandpass Filter Design Nomograph

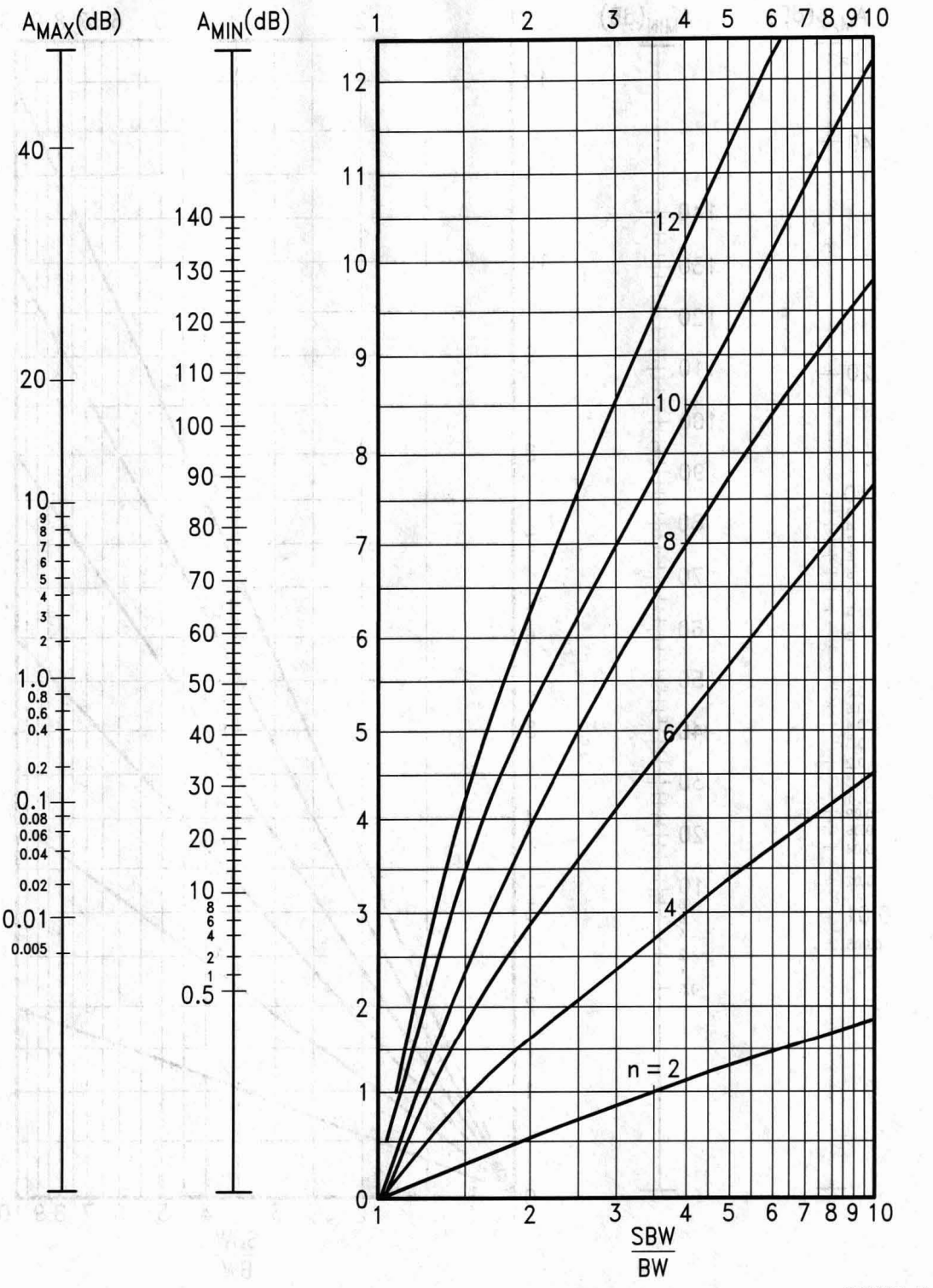

FIGURE 9. Chebyshev Bandpass Filter Design Nomograph

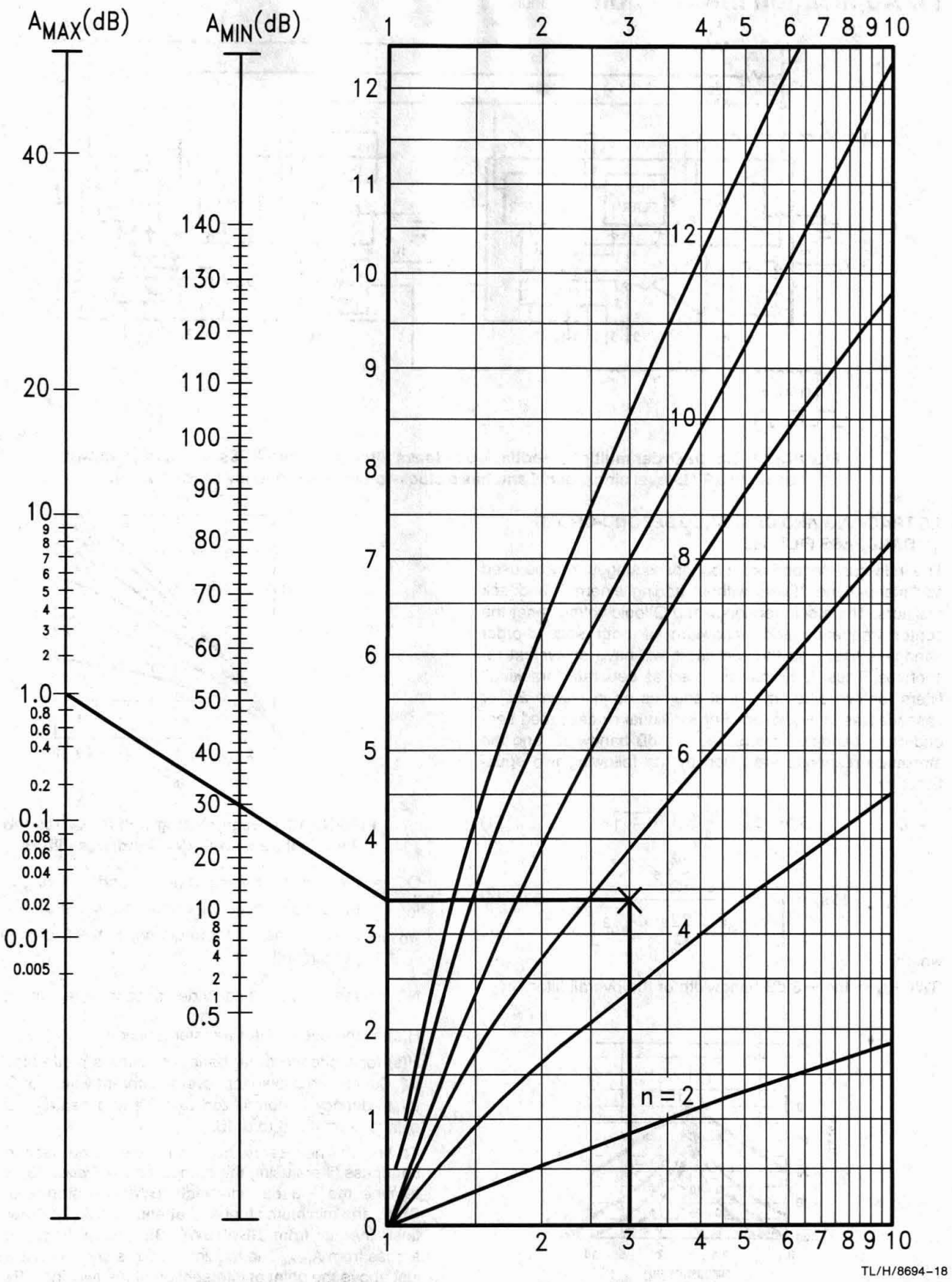

FIGURE 10. Example of Chebyshev Bandpass Nomograph Use.

A_{max} = 1 dB, A_{min} = 30 dB, and $\frac{SBW}{BW}$ = 3, resulting in n = 6.

1.0 Application Information (Continued)

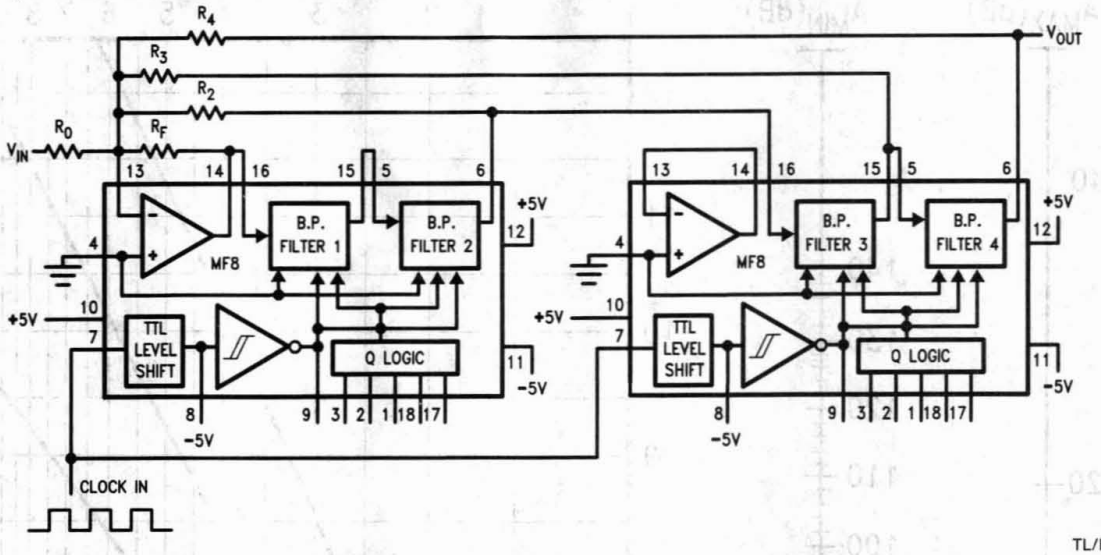

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FIGURE 11. Eighth-Order multiple-feedback bandpass filter using two MF8s. The circuit shown accepts a TTL-level clock signal and has a clock-to-center-frequency ratio of 100:1.

1.5 TRACKING AND CASCADED SECOND-ORDER BANDPASS FILTERS

The individual second-order bandpass stages may be used as "stand-alone" filters without adding external feedback resistors. The clock frequency and Q logic voltages set the center frequency and bandwidth of both second-order bandpass filters, so the two filters will have equivalent responses. Thus, they may be used as separate "tracking" filters for two different signal sources as in *Figure 2a*, or cascaded as in *Figure 2b*. For individual or cascaded second-order bandpass filters, the −3 dB bandwidth and the amplitude response are given by the following two equations:

$$BW(-3) = \frac{f_0}{Q}\sqrt{2^{(1/N)} - 1} \qquad (1)$$

$$H(s) = \left[2 \times \frac{\frac{w_0}{Q}s}{s^2 + \frac{w_0}{Q}s + w_0^2} \right]^N \qquad (2)$$

where

BW(−3) = the −3 dB bandwidth of the overall filter

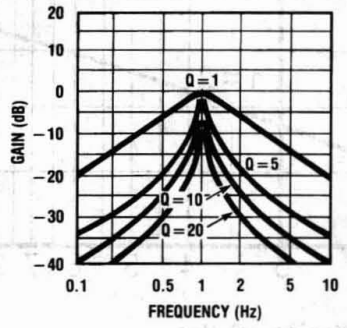

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FIGURE 12. H(s) For second-order bandpass filters with various values of Q. H_0 normalized in each case to 0 dB.

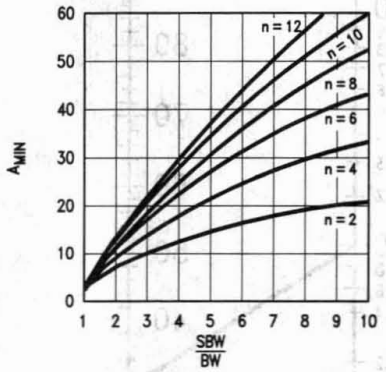

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FIGURE 13. Design Nomograph for Cascaded Identical Second-Order Bandpass Filters

Q = the Q of each second order bandpass stage

f_0 = the center frequency of the filter in Hertz

$w_0 = 2\pi f_0$ = the center frequency of the filter in radians per second

N = the number of cascaded second-order stages = $\frac{n}{2}$

H(s) = the overall filter transfer function

H(s) for a second order bandpass filter is plotted in *Figure 12*. Curves are shown for several different values of Q. Center frequency is normalized to 1 Hz and center-frequency gain is normalized to 0 dB.

To find the necessary order n for cascaded second-order bandpass filters using the nomograph in *Figure 13*, first determine the −3 dB bandwidth BW(−3), stopband width SBW, and minimum stopband attenuation A_{min}. Draw a vertical line up from SBW/BW(−3), and a horizontal line across from A_{min}. The required order is shown on the curve just above the point of intersection of the two lines. Remember that each second-order filter section will have a center frequency gain of 2, so the overall gain of a cascaded filter will be 2^N.

Cascading filters in this way may provide acceptable performance when minimum external parts count is very impor-

1.0 Application Information (Continued)

tant, but much greater flexibility and better performance will be obtained by using the feedback techniques described in 1.4.

1.6 INPUT IMPEDANCE

The input to each filter block is a switched-capacitor circuit as shown in *Figure 14*. During the first half of a clock cycle, the input capacitor charges to the input voltage V_{in}, and during the second half-cycle, its charge is transferred to a feedback capacitor. The input impedance approximates a resistor of value

$$R_{in} \cong \frac{1}{C_{in} f_{CLK}}.$$

C_{in} depends on the value of Q selected by the Q logic pins, and varies from about 1 pF to about 5 pF. For a worst-case calculation of R_{in}, assume $C_{in} = 5$ pF. Thus,

$$R_{in}(min) \cong \frac{1}{5 \times 10^{-12} f_{CLK}}$$

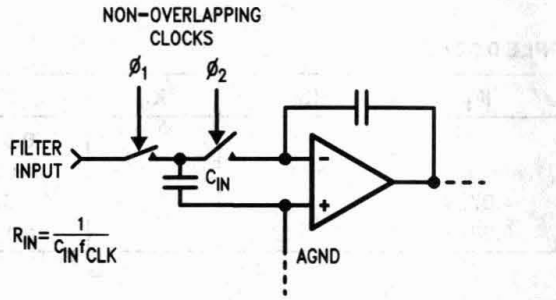

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FIGURE 14. Simplified MF8 Input Stage

At the maximum clock frequency of 1 MHz, this gives $R_{in} \cong 200$k. Note that R_{in} increases as f_{CLK} decreases, so the input impedance should never be less than this number. Source impedance should be low enough that the gain isn't significantly affected.

1.7 OUTPUT DRIVE

The filter outputs can typically drive a 5 kΩ load resistor to over ±4V peak-to-peak. Load resistors smaller than 5 kΩ should not be used. The operational amplifier can drive the minimum recommended load resistance of 5 kΩ to at least ±3.5V.

1.8 SAMPLED-DATA SYSTEM CONSIDERATIONS

Aliasing

The MF8 is a sampled-data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF8's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 10$ Hz. This phenomenon is known as "aliasing". Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter (a simple passive RC network will generally suffice) ahead of the MF8 to attenuate unwanted high-frequency signals. However, since the clock frequency is much greater than the center frequency, this will usually not be necessary.

Output Steps

Another characteristic of sampled-data circuits is that the output voltage changes only once every clock cycle, resulting in a discontinuous output signal (*Figure 15*). The "steps" are smaller when the clock-to-center-frequency ratio is 100:1 than when the ratio is 50:1.

Clock Frequency Limitations

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the internal capacitors begin to discharge slightly between clock cycles. This is due to very small parasitic leakage currents. At very low clock frequencies, the time between clock cycles is relatively long, allowing the capacitors to discharge enough to affect the filters' output offset voltage and gain. This effect becomes stronger at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal integrating op amps to settle. For this reason, the clock waveform's duty cycle should be as close as possible to 50%, especially at higher frequencies. Filter Q shows more variation from the nominal values at higher frequencies, as indicated in the typical performance curves. This is the reason for the different maximum limits on Q accuracy at $f_{CLK} = 250$ kHz and $f_{CLK} = 100$ kHz in the table of performance specifications.

Center Frequency Accuracy

Ideally, the ratio f_{CLK}/f_0 should be precisely 100 or 50, depending on the logic voltage on pin 10. However, as Table I shows, this ratio will change slightly depending on the Q selected. As the table shows, the largest errors occur at the lowest values of Q.

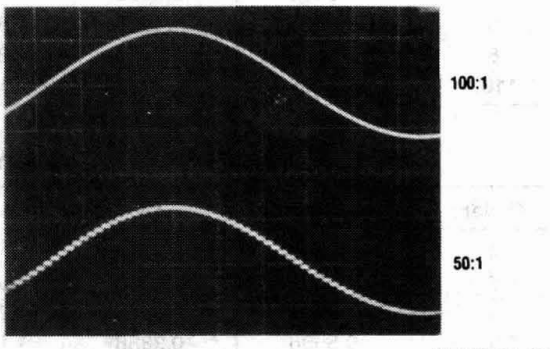

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FIGURE 15. Output Waveform of MF8 Showing Sampling Steps

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters

BUTTERWORTH RIPPLE 3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	2.0000	4.0000					1.4142
6	2.3704	2.6667	9.1429				1.5000
8	2.9142	2.0000	5.8284	14.3145			1.5307
10	3.6340	1.6000	4.4112	6.9094	27.2014		1.5451
*12	4.5635	1.3333	3.5800	4.3198	11.5043	49.0673	1.5529

CHEBYSHEV RIPPLE 0.01 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.9041	3.6339					0.4489
6	1.8277	1.8450	6.6170				0.9438
8	1.4856	0.9919	3.1209	5.0414			1.4257
*10	1.0171	0.5740	1.7484	1.2943	4.8814		1.8908

CHEBYSHEV RIPPLE 0.02 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8644	3.4922					0.5393
6	1.7024	1.6787	6.0772				1.0849
8	1.2893	0.8707	2.7661	4.0779			1.6106
*10	0.8163	0.4934	1.5155	0.9879	3.7119		2.1179

CHEBYSHEV RIPPLE 0.03 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8341	3.3871					0.6016
6	1.6183	1.5713	5.7231				1.1808
8	1.1688	0.7977	2.5491	3.5270			1.7362
*10	0.7034	0.4467	1.3786	0.8252	3.0938		2.2724

CHEBYSHEV RIPPLE 0.04 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8085	3.3009					0.6508
6	1.5535	1.4908	5.4548				1.2560
8	1.0814	0.7454	2.3919	3.1471			1.8348
*10	0.6264	0.4139	1.2818	0.7181	2.6883		2.3940

CHEBYSHEV RIPPLE 0.05 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7860	3.2268					0.6923
6	1.5002	1.4260	5.2373				1.3191
8	1.0129	0.7046	2.2685	2.8609			1.9175
*10	0.5686	0.3888	1.2072	0.6402	2.3938		2.4961

CHEBYSHEV RIPPLE 0.06 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7657	3.1612					0.7285
6	1.4548	1.3717	5.0536				1.3741
8	0.9566	0.6713	2.1670	2.6336			1.9897
*10	0.5230	0.3685	1.1467	0.5800	2.1666		2.5852

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE .07 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7471	3.1020					0.7609
6	1.4150	1.3249	4.8943				1.4232
8	0.9089	0.6431	2.0808	2.4466			2.0543
*10	0.4856	0.3516	1.0959	0.5316	1.9842		2.6649

CHEBYSHEV RIPPLE .08 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7298	3.0478					0.7905
6	1.3795	1.2837	4.7534				1.4679
8	0.8675	0.6187	2.0060	2.2887			2.1130

CHEBYSHEV RIPPLE .09 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7136	2.9978					0.8177
6	1.3475	1.2469	4.6271				1.5090
8	0.8311	0.5973	1.9400	2.1529			2.1671

CHEBYSHEV RIPPLE 0.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.6983	2.9512					0.8430
6	1.3183	1.2137	4.5125				1.5473
8	0.7986	0.5782	1.8809	2.0343			2.2176

CHEBYSHEV RIPPLE 0.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.5757	2.5998					1.0378
6	1.1128	0.9894	3.7271				1.8413
8	0.5891	0.4551	1.4954	1.3309			2.6057

CHEBYSHEV RIPPLE 0.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.4833	2.3575					1.1804
6	0.9835	0.8560	3.2501				2.0568
*8	0.4732	0.3861	1.2760	0.9885			2.8914

CHEBYSHEV RIPPLE 0.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.4067	2.1698					1.2988
6	0.8888	0.7618	2.9088				2.2363
*8	0.3956	0.3391	1.1250	0.7792			3.1299

CHEBYSHEV RIPPLE 0.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.3405	2.0161					1.4029
6	0.8143	0.6897	2.6447				2.3944
*8	0.3389	0.3040	1.0114	0.6365			3.3406

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 0.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.2816	1.8857					1.4975
6	0.7530	0.6316	2.4305				2.5385
*8	0.2952	0.2762	0.9212	0.5326			3.5329

CHEBYSHEV RIPPLE 0.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.2283	1.7727					1.5852
6	0.7012	0.5834	2.2515				2.6724
*8	0.2601	0.2535	0.8471	0.4535			3.7119

CHEBYSHEV RIPPLE 0.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.1797	1.6731					1.6678
6	0.6564	0.5424	2.0983				2.7989
*8	0.2314	0.2344	0.7846	0.3913			3.8811

CHEBYSHEV RIPPLE 0.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.1347	1.5841					1.7464
6	0.6171	0.5068	1.9650				2.9194
*8	0.2073	0.2181	0.7309	0.3413			4.0426

CHEBYSHEV RIPPLE 1.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0930	1.5039					1.8219
6	0.5822	0.4756	1.8475				3.0354
*8	0.1869	0.2038	0.6840	0.3002			4.1981

CHEBYSHEV RIPPLE 1.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0539	1.4310					1.8949
6	0.5509	0.4479	1.7428				3.1476
*8	0.1693	0.1913	0.6426	0.2660			4.3487

CHEBYSHEV RIPPLE 1.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0173	1.3643					1.9657
6	0.5226	0.4231	1.6487				3.2567
*8	0.1540	0.1801	0.6056	0.2372			4.4952

CHEBYSHEV RIPPLE 1.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9828	1.3029					2.0348
6	0.4969	0.4006	1.5634				3.3633
*8	0.1406	0.1701	0.5724	0.2125			4.6385

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 1.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9501	1.2461					2.1024
6	0.4733	0.3803	1.4857				3.4678

CHEBYSHEV RIPPLE 1.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9192	1.1934					2.1688
6	0.4515	0.3616	1.4145				3.5705

CHEBYSHEV RIPPLE 1.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8897	1.1443					2.2341
6	0.4315	0.3445	1.3490				3.6717

CHEBYSHEV RIPPLE 1.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8617	1.0983					2.2986
6	0.4128	0.3287	1.2883				3.7717

CHEBYSHEV RIPPLE 1.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8350	1.0553					2.3624
6	0.3955	0.3141	1.2321				3.8706

CHEBYSHEV RIPPLE 1.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8095	1.0148					2.4255
6	0.3793	0.3005	1.1797				3.9687

CHEBYSHEV RIPPLE 2.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7850	0.9767					2.4881
6	0.3641	0.2878	1.1308				4.0660

CHEBYSHEV RIPPLE 2.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7616	0.9407					2.5503
6	0.3498	0.2759	1.0850				4.1628

CHEBYSHEV RIPPLE 2.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7391	0.9067					2.6122
6	0.3364	0.2648	1.0420				4.2591

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 2.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7176	0.8744					2.6737
6	0.3237	0.2544	1.0016				4.3550

CHEBYSHEV RIPPLE 2.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6968	0.8438					2.7350
6	0.3118	0.2446	0.9635				4.4507

CHEBYSHEV RIPPLE 2.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6769	0.8148					2.7962
6	0.3005	0.2353	0.9275				4.5462

CHEBYSHEV RIPPLE 2.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6577	0.7871					2.8573
6	0.2897	0.2265	0.8935				4.6415

CHEBYSHEV RIPPLE 2.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6392	0.7607					2.9183
6	0.2796	0.2182	0.8612				4.7368

CHEBYSHEV RIPPLE 2.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6213	0.7356					2.9792
6	0.2699	0.2104	0.8306				4.8322

CHEBYSHEV RIPPLE 2.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6041	0.7116					3.0402
6	0.2607	0.2029	0.8016				4.9276

CHEBYSHEV RIPPLE 3.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.5875	0.6886					3.1013
6	0.2519	0.1959	0.7739				5.0231

Note: Multiple feedback loop filters of higher order than those specified in the tables will oscillate due to phase shift at the output of the summing amplifier. This phase shift is not the fault of the MF8; it is inherent in this type of multiple feedback loop topology. In addition, all filters marked with an asterisk (*) will be unstable for $Q \leq 1$, due to phase shifts caused by the MF8's switched-capacitor design approach.

National Semiconductor

MF10
Universal Monolithic Dual Switched Capacitor Filter

General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages.

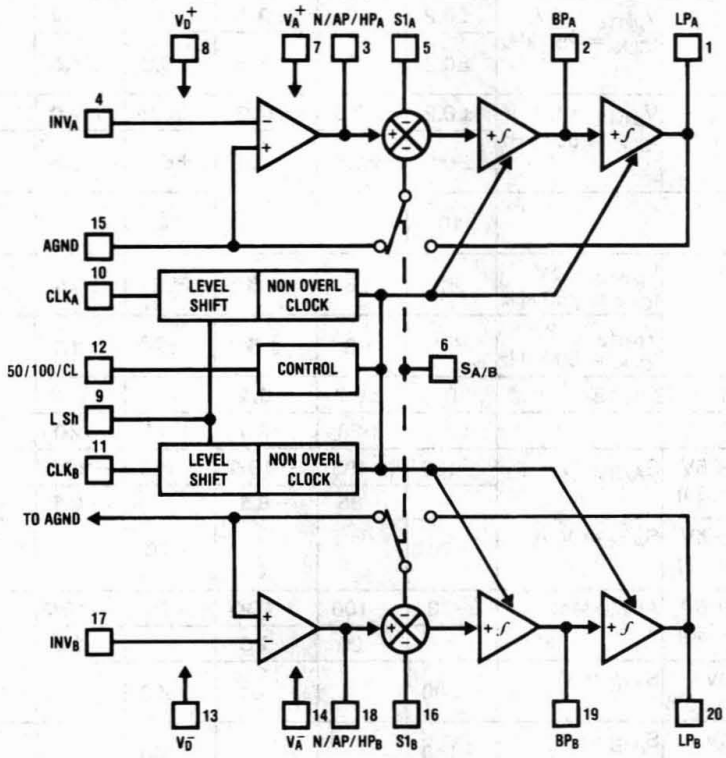
Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

For pin-compatible device with improved performance refer to LMF100 datasheet.

Features

- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_O \times Q$ range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3″ wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

System Block Diagram



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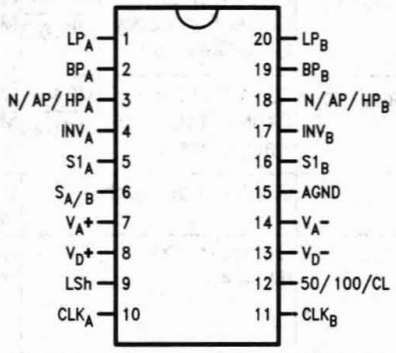
Connection Diagram

Surface Mount and Dual-In-Line Package



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Top View

Order Number MF10AJ or MF10CCJ
See NS Package Number J20A

Order Number MF10ACWM or MF10CCWM
See NS Package Number M20B

Order Number MF10ACN or MF10CCN
See NS Package Number N20A

7

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Voltage at Any Pin	$V^+ + 0.3V$ $V^- - 0.3V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150°C
ESD Susceptability (Note 11)	2000V

Soldering Information

N Package: 10 sec.	260°C
J Package: 10 sec.	300°C
SO Package: Vapor Phase (60 Sec.)	215°C
Infrared (15 Sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF10ACN, MF10CCN	$0°C \le T_A \le 70°C$
MF10CCWM, MF10ACWM	$0°C \le T_A \le 70°C$
MF10CCJ	$-40°C \le T_A \le 85°C$
MF10AJ	$-55°C \le T_A \le 125°C$

Electrical Characteristics

$V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10ACWM, MF10CCWM			MF10CCJ, MF10AJ			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ - V^-$	Supply Voltage	Min					**9**			**9**	V
		Max					**14**			**14**	V
I_S	Maximum Supply Current		Clock Applied to Pins 10 & 11 No Input Signal		8	12	**12**	8	**12**		mA
f_O	Center Frequency Range	Min	$f_O \times Q < 200$ kHz		0.1		**0.2**	0.1		**0.2**	Hz
		Max			30		**20**	30		**20**	kHz
f_{CLK}	Clock Frequency Range	Min			5.0		**10**	5.0		**10**	Hz
		Max			1.5		**1.0**	1.5		**1.0**	MHz
f_{CLK}/f_O	50:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±0.2	±0.6	±**0.6**	±0.2	±**1.0**		%
		MF10C			±0.2	±1.5	±**1.5**	±0.2	±**1.5**		%
f_{CLK}/f_O	100:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10 Mode 1	$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±0.2	±0.6	±**0.6**	±0.2	±**1.0**		%
		MF10C			±0.2	±1.5	±**1.5**	±0.2	±**1.5**		%
	Clock Feedthrough		Q = 10 Mode 1		10			10			mV
	Q Error (MAX) (Note 4)		Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±2	±6	±**6**	±2	±**10**		%
				$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±2	±6	±**6**	±2	±**10**		%
H_{OLP}	DC Lowpass Gain		Mode 1 R1 = R2 = 10k		0	±0.2	±**0.2**	0	±**0.2**		dB
V_{OS1}	DC Offset Voltage (Note 5)				±5.0	±20	±**20**	±5.0	±**20**		mV
V_{OS2}	DC Offset Voltage (Note 5)	Min	$V_{pin12} = +5V$ $(f_{CLK}/f_O = 50)$	$S_{A/B} = V^+$	−150	−185	−**185**	−150	−**185**		mV
		Max				−85	−**85**		−**85**		
		Min	$V_{pin12} = +5V$ $(f_{CLK}/f_O = 50)$	$S_{A/B} = V^-$	−70			−70			mV
		Max									
V_{OS3}	DC Offset Voltage (Note 5)	Min	$V_{pin12} = +5V$ $(f_{CLK}/f_O = 50)$	All Modes	−70	−100	−**100**	−70	−**100**		mV
		Max				−20	−**20**		−**20**		
V_{OS2}	DC Offset Voltage (Note 5)		$V_{pin12} = 0V$ $(f_{CLK}/f_O = 100)$	$S_{A/B} = V^+$	−300			−300			mV
	(Note 5)		$V_{pin12} = 0V$ $(f_{CLK}/f_O = 100)$	$S_{A/B} = V^-$	−140			−140			mV
V_{OS3}	DC Offset Voltage (Note 5)		$V_{pin12} = 0V$ $(f_{CLK}/f_O = 100)$	All Modes	−140			−140			mV

Electrical Characteristics (Continued) $V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified.

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	MF10ACN, MF10CCN, MF10ACWM, MF10CCWM			MF10CCJ, MF10AJ			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
V_{OUT}	Minimum Output Voltage Swing	BP, LP Pins	$R_L = 5k$	±4.25	±3.8	**±3.8**	±4.25	**±3.8**		V
		N/AP/HP Pin	$R_L = 3.5k$	±4.25	±3.8	**±3.8**	±4.25	**±3.6**		V
GBW	Op Amp Gain BW Product			2.5			2.5			MHz
SR	Op Amp Slew Rate			7			7			V/μs
	Dynamic Range (Note 6)		$V_{pin12} = +5V$ ($f_{CLK}/f_O = 50$)	83			83			dB
			$V_{pin12} = 0V$ ($f_{CLK}/f_O = 100$)	80			80			dB
I_{SC}	Maximum Output Short Circuit Current (Note 7)	Source		20			20			mA
		Sink		3.0			3.0			mA

Logic Input Characteristics **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$

Parameter		Conditions	MF10ACN, MF10CCN, MF10ACWM, MF10CCWM			MF10CCJ, MF10AJ			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock Input Voltage	Min Logical "1"	$V^+ = +5V, V^- = -5V,$ $V_{LSh} = 0V$		+3.0	**+3.0**		**+3.0**		V
	Max Logical "0"			−3.0	**−3.0**		**−3.0**		V
	Min Logical "1"	$V^+ = +10V, V^- = 0V,$ $V_{LSh} = +5V$		+8.0	**+8.0**		**+8.0**		V
	Max Logical "0"			+2.0	**+2.0**		**+2.0**		V
TTL Clock Input Voltage	Min Logical "1"	$V^+ = +5V, V^- = -5V,$ $V_{LSh} = 0V$		+2.0	**+2.0**		**+2.0**		V
	Max Logical "0"			+0.8	**+0.8**		**+0.8**		V
	Min Logical "1"	$V^+ = +10V, V^- = 0V,$ V_{LSh}		+2.0	**+2.0**		**+2.0**		V
	Max Logical "0"			+0.8	**+0.8**		**+0.8**		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF10ACN/CCN when board mounted is 55°C/W. For the MF10AJ/CCJ, this number increases to 95°C/W and for the MF10ACWM/CCWM this number is 66°C/W.

Note 4: The accuracy of the Q value is a function of the center frequency (f_O). This is illustrated in the curves under the heading "Typical Performance Characteristics".

Note 5: V_{OS1}, V_{OS2}, and V_{OS3} refer to the internal offsets as discussed in the Applications Information Section 3.4.

Note 6: For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μV rms for the MF10 with a 50:1 CLK ratio and 280 μV rms for the MF10 with a 100:1 CLK ratio.

Note 7: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

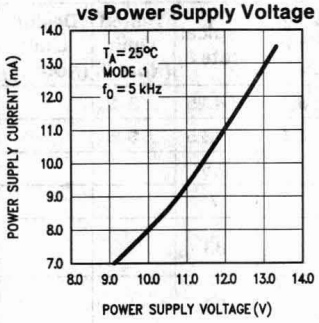
Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

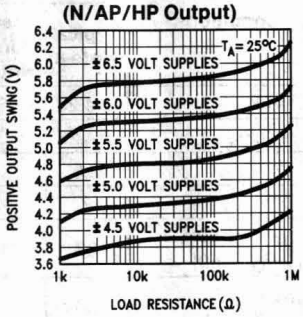
Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

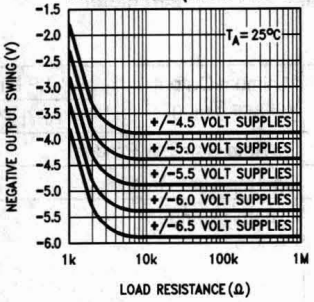
Power Supply Current vs Power Supply Voltage



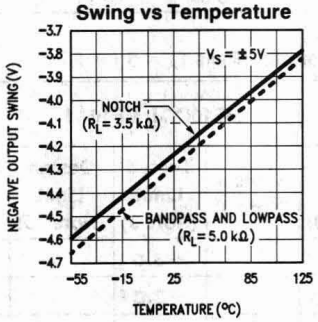
Positive Output Voltage Swing vs Load Resistance (N/AP/HP Output)



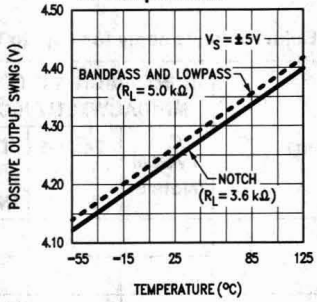
Negative Output Voltage Swing vs Load Resistance (N/AP/HP Output)



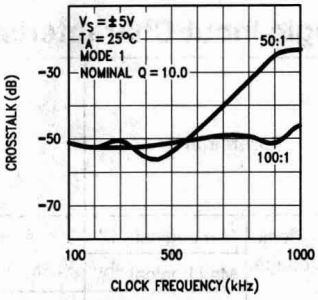
Negative Output Swing vs Temperature



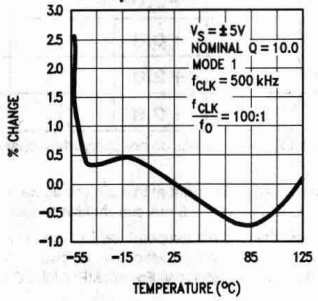
Positive Output Swing vs Temperature



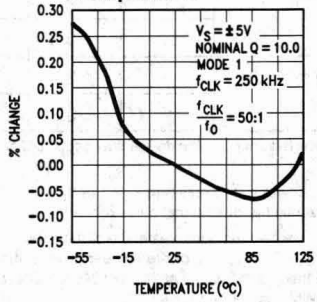
Crosstalk vs Clock Frequency



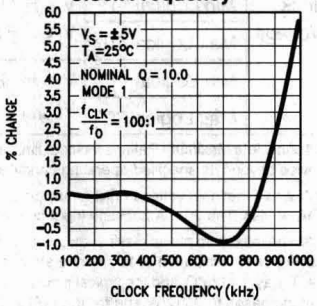
Q Deviation vs Temperature



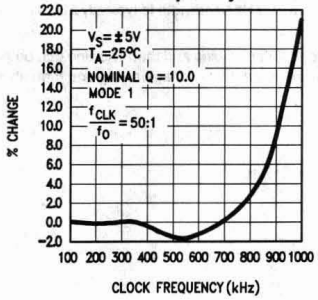
Q Deviation vs Temperature



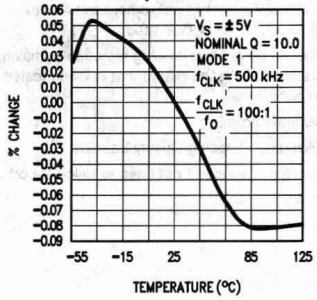
Q Deviation vs Clock Frequency



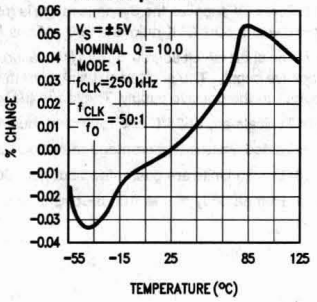
Q Deviation vs Clock Frequency



f_{CLK}/f_O Deviation vs Temperature



f_{CLK}/f_O Deviation vs Temperature



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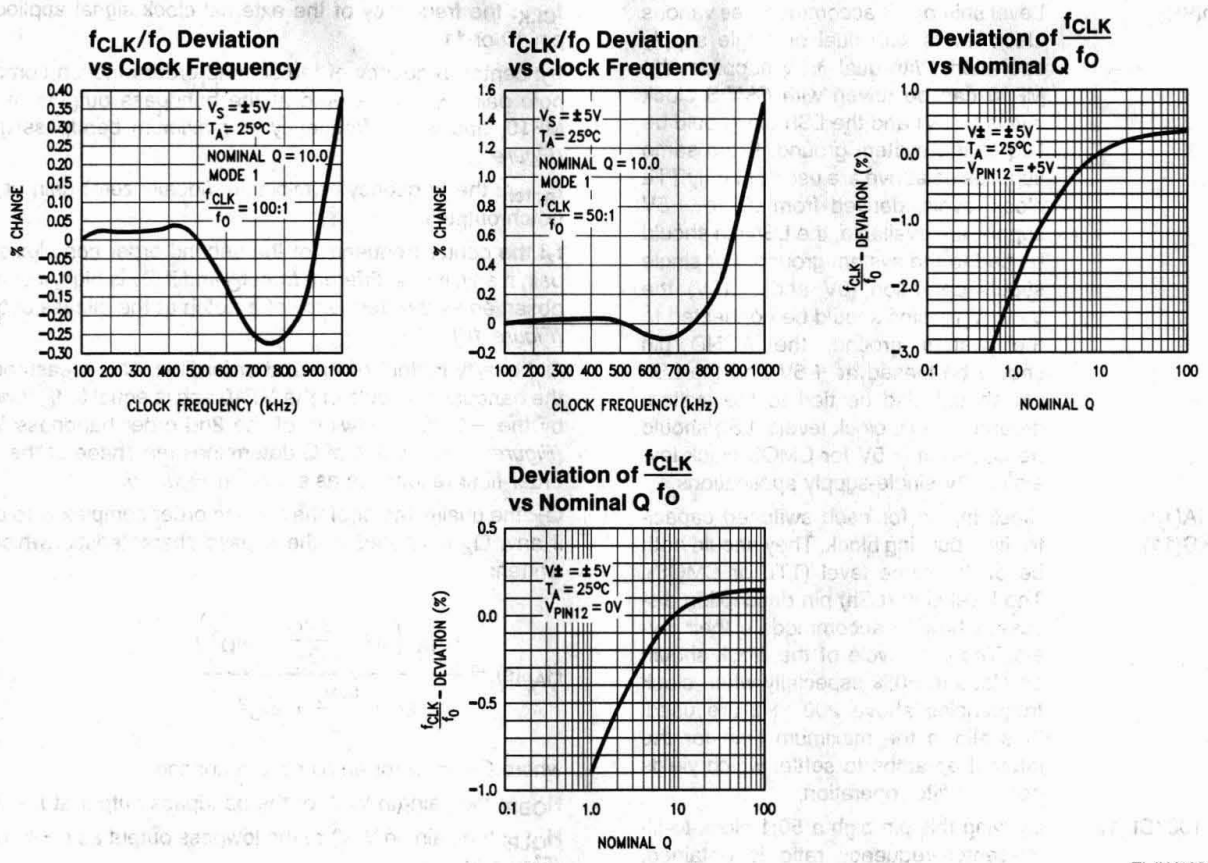
Typical Performance Characteristics (Continued)



TL/H/10399–3

Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18) — The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.

INV(4,17) — The inverting input of the summing op-amp of each filter. These are high impedance inputs, but the non-inverting input is internally tied to AGND, making INV_A and INV_B behave like summing junctions (low impedance, current inputs).

S1(5,16) — S1 is a signal input pin used in the all-pass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

$S_{A/B}$(6) — This pin activates a switch that connects one of the inputs of each filter's second summer to either AGND ($S_{A/B}$ tied to V^-) or to the lowpass (LP) output ($S_{A/B}$ tied to V^+). This offers the flexibility needed for configuring the filter in its various modes of operation.

V_A^+(7),V_D^+(8) — Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

V_A^-(14), V_D^-(13) — Analog and digital negative supplies. The same comments as for V_A^+ and V_D^+ apply here.

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Pin Descriptions (Continued)

LSh(9) — Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the LSh pin should be tied to the system ground. If the same supplies as above are used but only TTL clock levels, derived from 0V to +5V supply, are available, the LSh pin should be tied to the system ground. For single supply operation (0V and +10V) the V_A^-, V_D^- pins should be connected to the system ground, the AGND pin should be biased at +5V and the LSh pin should also be tied to the system ground for TTL clock levels. LSh should be biased at +5V for CMOS clock levels in 10V single-supply applications.

CLKA(10), CLKB(11) — Clock inputs for each switched capacitor filter building block. They should both be of the same level (TTL or CMOS). The level shift (LSh) pin description discusses how to accommodate their levels. The duty cycle of the clock should be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal op-amps to settle, which yields optimum filter operation.

50/100/CL(12) — By tying this pin high a 50:1 clock-to-filter-center-frequency ratio is obtained. Tying this pin at mid-supplies (i.e, analog ground with dual supplies) allows the filter to operate at a 100:1 clock-to-center-frequency ratio. When the pin is tied low (i.e., negative supply with dual supplies), a simple current limiting circuit is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.

AGND(15) — This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

1.0 Definition of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_O: center frequency of the second order function complex pole pair. f_O is measured at the bandpass outputs of the MF10, and is the frequency of maximum bandpass gain. *(Figure 1)*

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_O and if Q_Z is high, it can be observed as the frequency of a notch at the allpass output. *(Figure 10)*

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the MF10 and is equal to f_O divided by the −3 dB bandwidth of the 2nd order bandpass filter *(Figure 1)*. The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_Z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q_Z} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

where $Q_Z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_O$.

H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz *(Figure 2)*.

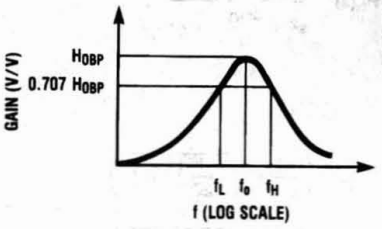
H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{CLK}/2$ *(Figure 3)*.

H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency *(Figure 4)*. When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a *(Figures 11 and 8)*, the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

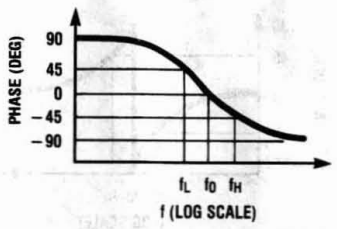
H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{CLK}/2$.

1.0 Definition of Terms (Continued)



TL/H/10399–5

(a)



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(b)

$$H_{BP}(s) = \frac{H_{OBP}\frac{\omega_O}{Q}s}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

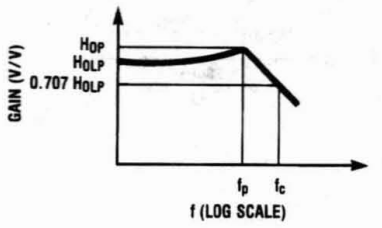
$$Q = \frac{f_O}{f_H - f_L};\ f_O = \sqrt{f_L f_H}$$

$$f_L = f_O\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_O\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

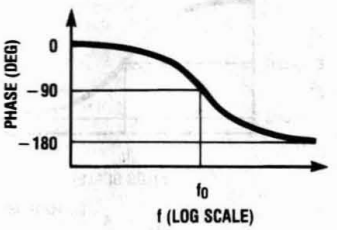
$$\omega_O = 2\pi f_O$$

FIGURE 1. 2nd-Order Bandpass Response



TL/H/10399–7

(a)



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(b)

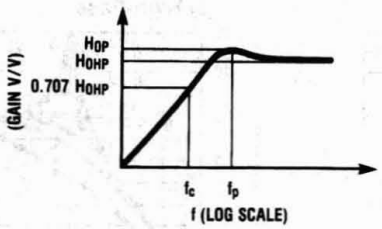
$$H_{LP}(s) = \frac{H_{OLP}\omega_O^2}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$f_C = f_O \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_O\sqrt{1 - \frac{1}{2Q^2}}$$

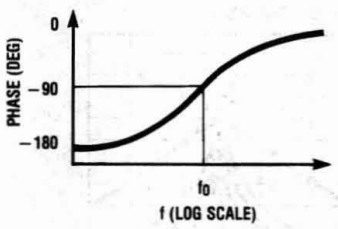
$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



TL/H/10399–9

(a)



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(b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

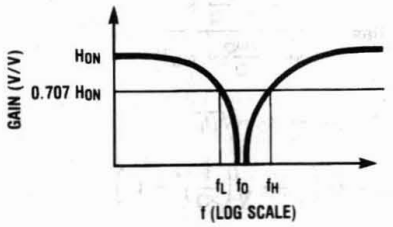
$$f_C = f_O \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_O \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3. 2nd-Order High-Pass Response

1.0 Definitions of Terms (Continued)



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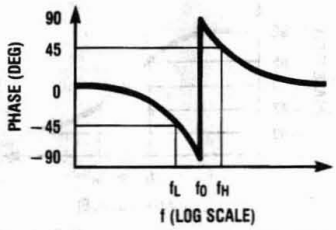
(a)



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(b)

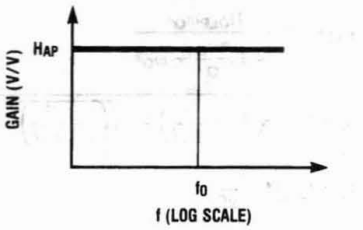
$$H_N(s) = \frac{H_{ON}(s^2 + \omega_O^2)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$Q = \frac{f_O}{f_H - f_L};\ f_O = \sqrt{f_L f_H}$$

$$f_L = f_O\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_O\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 4. 2nd-Order Notch Response



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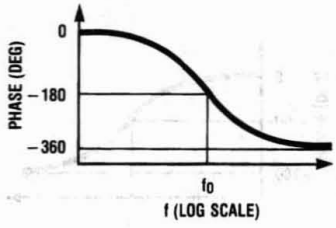
(a)



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(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

FIGURE 5. 2nd-Order All-Pass Response

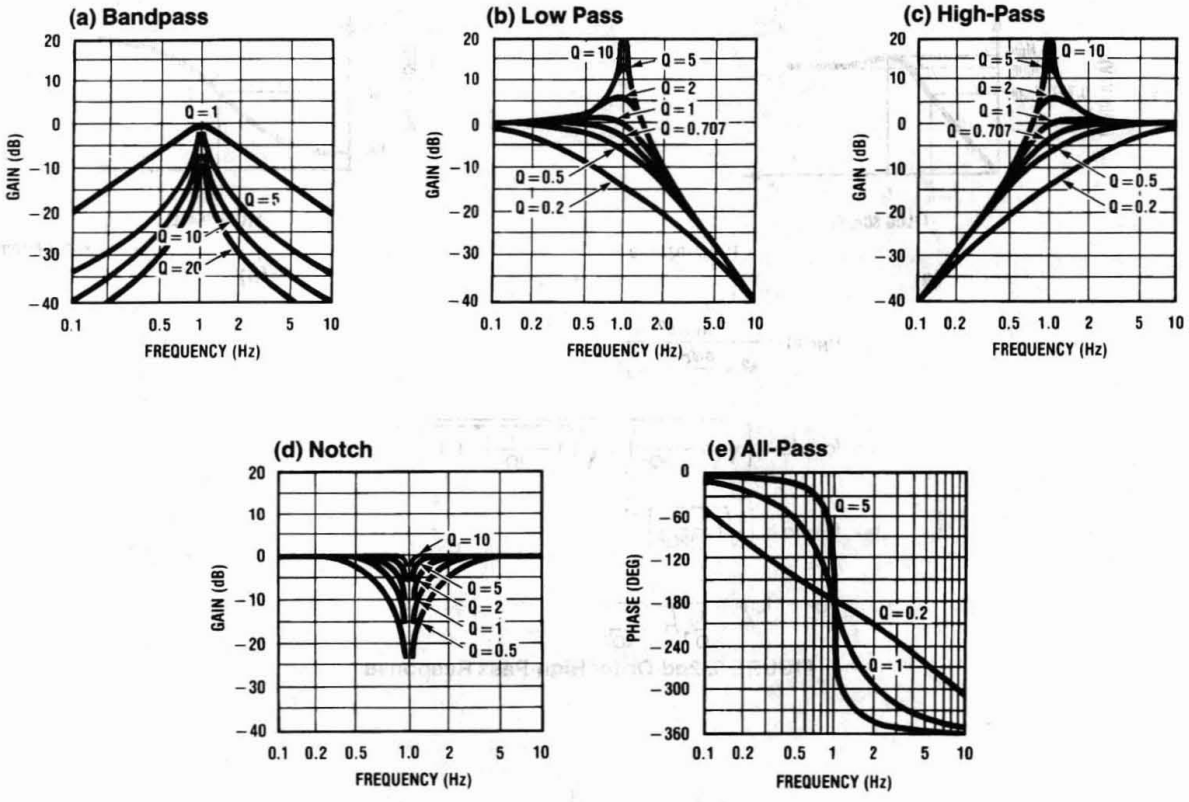

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FIGURE 6. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF10 closely approximates continuous filters, the following discussion is based on the well know frequency domain. Each MF10 can produce a full 2nd order function. See Table I for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs: $f_{notch} = f_O$ (See *Figure 7*)

f_O = center frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = center frequency of the imaginary zero pair = f_O.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) = $-\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_O$) = $-\frac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1}$

$Q = \frac{f_O}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$H_{OLP} = \frac{H_{OBP}}{Q}$ or $H_{OBP} = H_{OLP} \times Q$

$= H_{ON} \times Q.$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$f_O = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$; $H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (Non-Inverting)

Circuit Dynamics: $H_{OBP1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ) source.

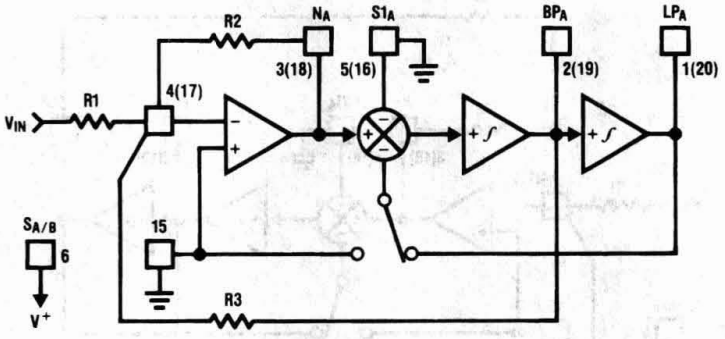

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FIGURE 7. MODE 1

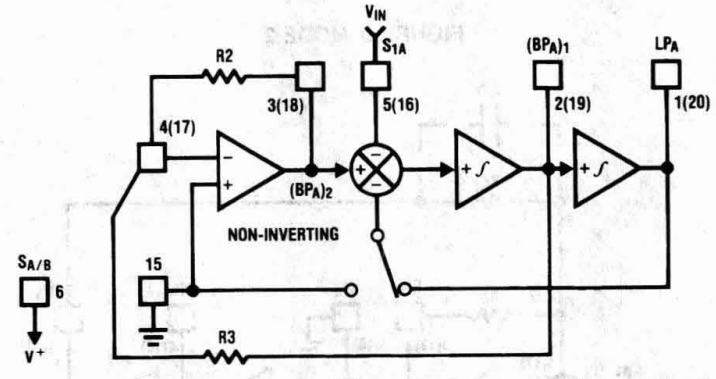

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FIGURE 8. MODE 1a

2.0 Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_O$ (See *Figure 9*)

f_O = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \frac{\sqrt{R2/R4+1}}{R2/R3}$$

H_{OLP} = Lowpass output gain (as f $\rightarrow$ 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{OBP} = Bandpass output gain (at f = f_O) = $-R3/R1$

H_{ON_1} = Notch output gain (as f $\rightarrow$ 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{ON_2} = Notch output gain $\left(\text{as f} \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = \sqrt{H_{ON1}\,H_{ON2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs (See *Figure 10*)

$$f_O = \frac{f_{CLK}}{100}\times\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\times\sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}}\times\frac{R3}{R2}$$

H_{OHP} = Highpass Gain $\left(\text{as f} \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Lowpass Gain $\left(\text{at f} = f_O\right) = -\frac{R3}{R1}$

H_{OLP} = Lowpass Gain $\left(\text{as f} \rightarrow 0\right) = -\frac{R4}{R1}$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$;

$$H_{OBP} = \sqrt{H_{OHP}\times H_{OLP}}\times Q$$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)

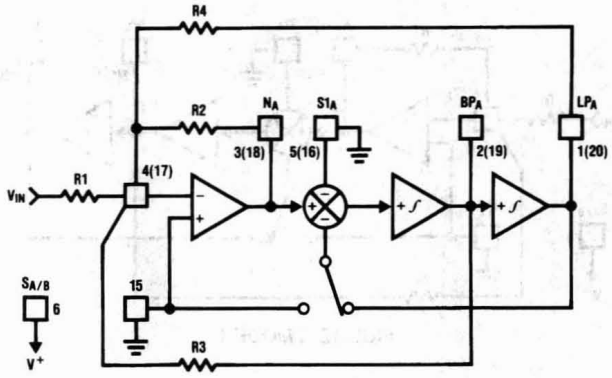

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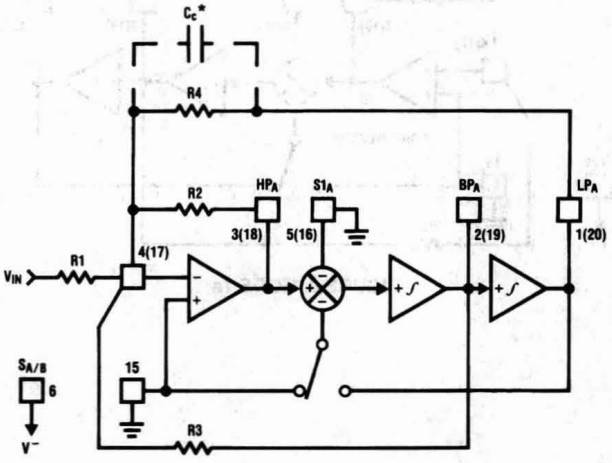
FIGURE 9. MODE 2



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*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF – 100 pF) across R4 to provide some phase lead.

FIGURE 10. MODE 3

2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op Amp (See *Figure 11*)

$$f_O = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

f_n = notch frequency $= \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_I}}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_I}}$

H_{ON} = gain of notch at

$$f = f_O = \left\| Q\left(\frac{R_g}{R_I} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)\right\|$$

H_{n1} = gain of notch (as $f \rightarrow 0$) $= \frac{R_g}{R_I} \times H_{OLP}$

H_{n2} = gain of notch $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right)$

$$= -\frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See *Figure 12*)

f_O = center frequency

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

f_z* = center frequency of the complex zero $\approx f_O$

$$Q = \frac{f_O}{BW} = \frac{R3}{R2};$$

Q_Z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

$$H_{OAP}^* = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$)

$$= -\left(\frac{R2}{R1} + 1\right) = -2$$

H_{OBP} = Bandpass gain (at $f = f_O$)

$$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

Circuit Dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_O occurs causing a 0.4 dB peaking around f_O of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

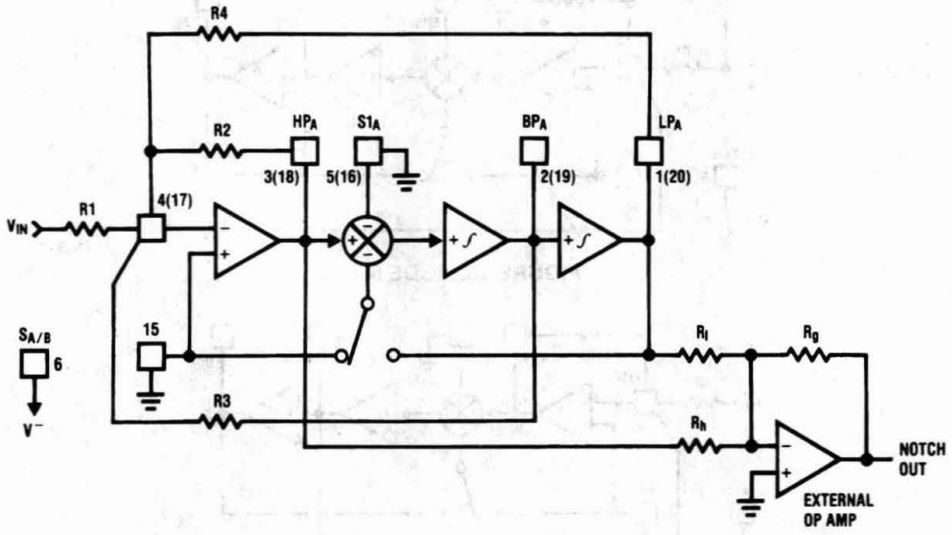

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FIGURE 11. MODE 3a

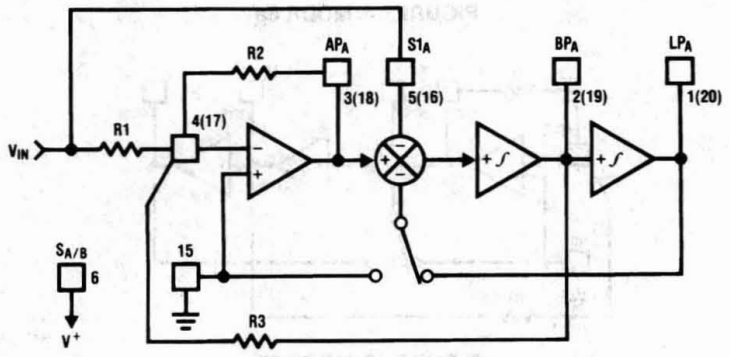

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FIGURE 12. MODE 4

2.0 Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 13*)

$$f_O = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1 - \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$$

H_{0z1} = gain at C.Z. output (as f $\rightarrow$ 0 Hz)

$$= \frac{-R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{0z2} = \text{gain at C.Z. output} \left(\text{as f} \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 14*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 15*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP1} = 1 (non-inverting)

$$H_{OLP2} = -\frac{R3}{R2}$$

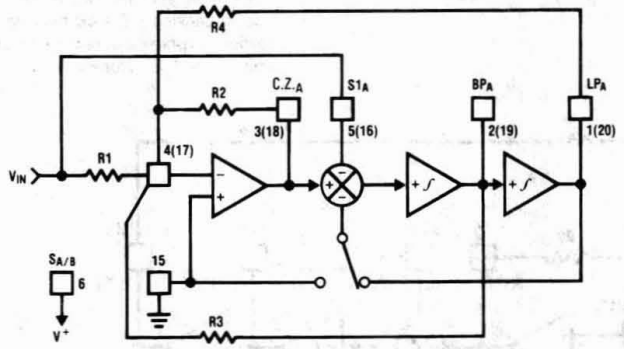

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FIGURE 13. MODE 5

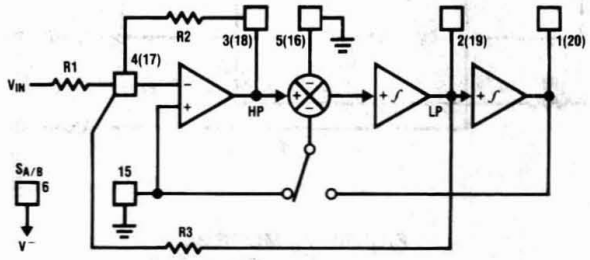

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FIGURE 14. MODE 6a

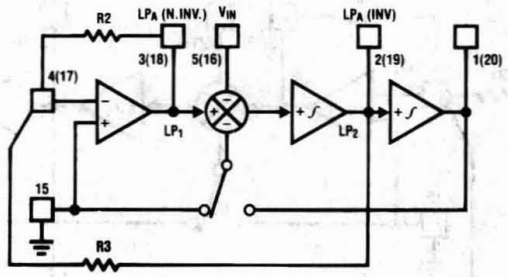

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FIGURE 15. MODE 6b

2.0 Modes of Operation (Continued)

TABLE I. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of Resistors	Adjustable f_{CLK}/f_O	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} + 1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		(2) $H_{OLP1} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2		Single Pole.

3.0 Applications Information

The MF10 is a general-purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 12 to the appropriate DC voltage, the filter center frequency f_O can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_O can be very accurately set (within ±6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_O ratio can be altered by external resistors as in *Figures 9, 10, 11, 13, 14* and *15*. The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using either section of the MF10. These are illustrated in *Figures 1* through *5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF10 sections can be cascaded.

3.1 DESIGN EXAMPLE

In order to design a second-order filter section using the MF10, we must define the necessary values of three parameters: f_0, the filter section's center frequency; H_0, the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at DC, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an MF10. Many filter design texts include tables that list the characteristics (f_O and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

$f_{0A} = 529$ Hz $\quad Q_A = 0.785$

$f_{0B} = 993$ Hz $\quad Q_B = 3.559$

For unity gain at DC, we also specify:

$H_{0A} = 1$

$H_{0B} = 1$

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust $\frac{f_{CLK}}{f_0}$ externally. From Table I, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: $R_{1A} = 20$k. The absolute value of the passband gain H_{OLPA} is made equal

3.0 Applications Information (Continued)

to 1 by choosing R_{4A} such that: $R_{4A} = -H_{OLPA}\, R_{1A} = R_{1A} = 20k$. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R_{2A} by:

$$R_{2A} = R_{4A}\frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6k \text{ and}$$

$$R_{3A} = Q_A\sqrt{R_{2A}R_{4A}} = 0.785\sqrt{5.6 \times 10^3 \times 2 \times 10^4} = 8.3k$$

The resistors for the second section are found in a similar fashion:

$R_{1B} = 20k$

$R_{4B} = R_{1B} = 20k$

$$R_{2B} = R_{4B}\frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20k\frac{(993)^2}{(1000)^2} = 19.7k$$

$$R_{3B} = Q_B\sqrt{R_{2B}R_{4B}} = 3.559\sqrt{1.97\times10^4\times2\times10^4} = 70.6k$$

The complete circuit is shown in *Figure 16* for split ±5V power supplies. Supply bypass capacitors are highly recommended.

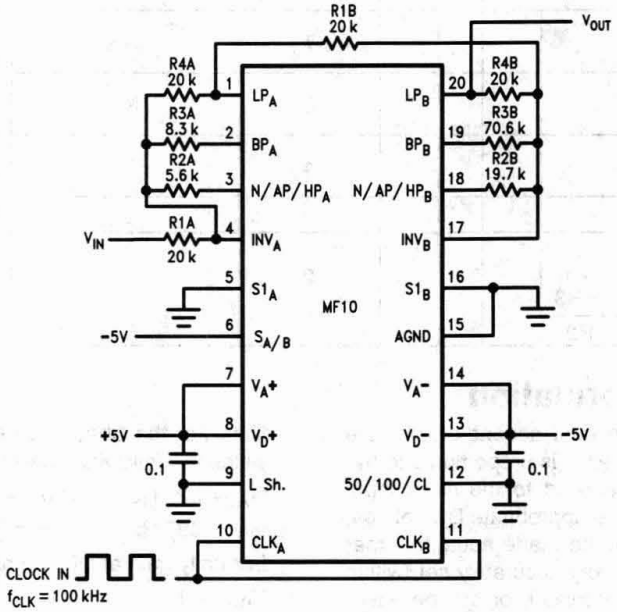

FIGURE 16. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. ±5V Power Supply. 0V–5V TTL or −5V ±5V CMOS Logic Levels.

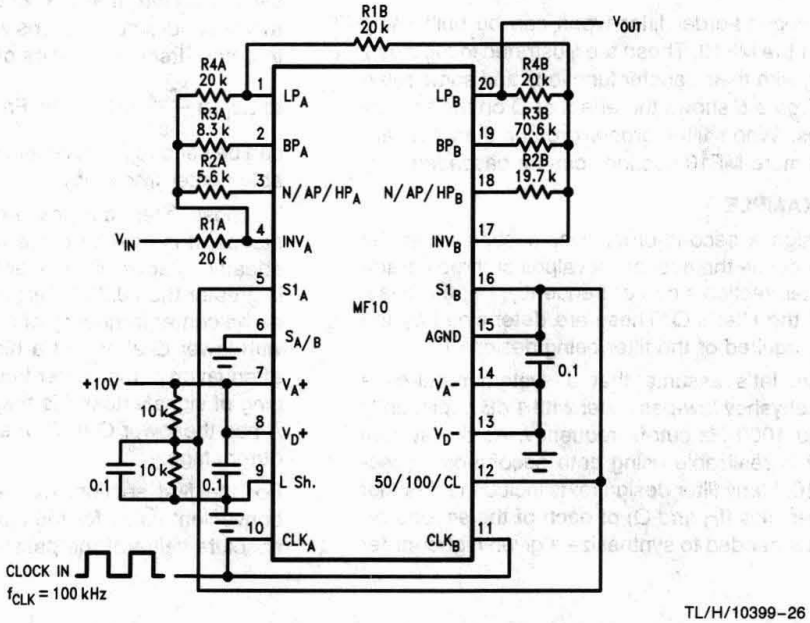

FIGURE 17. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. Single +10V Power Supply. 0V–5V TTL Logic Levels. Input Signals Should be Referred to Half-Supply or Applied through a Coupling Capacitor.

3.0 Applications Information (Continued)

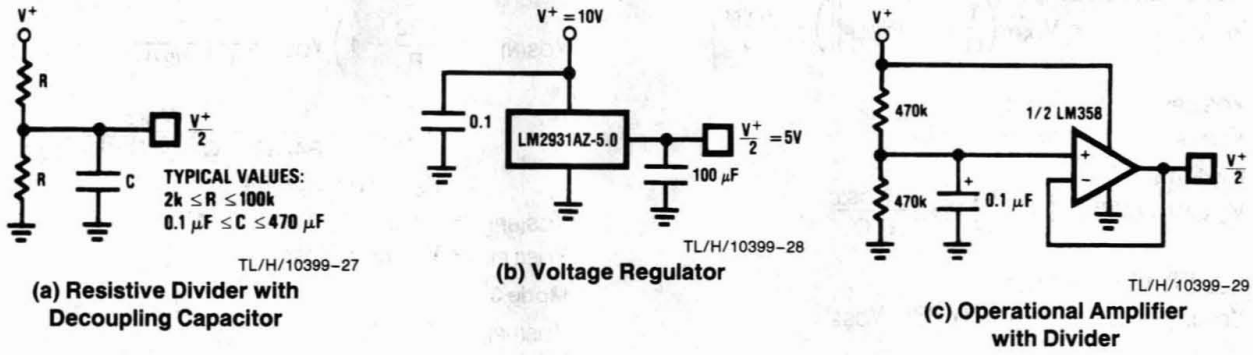

FIGURE 18. Three Ways of Generating $\frac{V^+}{2}$ for Single-Supply Operation

3.2 SINGLE SUPPLY OPERATION

The MF10 can also operate with a single-ended power supply. *Figure 17* shows the example filter with a single-ended power supply. V_A^+ and V_D^+ are again connected to the positive power supply (8V to 14V), and V_A^- and V_D^- are connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor *(Figure 18a)*, or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier *(Figures 18b* and *18c)*. The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 μF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF10, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF10 are able to swing to within about 1V of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF10 is operating on ±5V, for example, the outputs will clip at about 8 V_{p-p}. The maximum input voltage multiplied by the filter gain should therefore be less than 8 V_{p-p}.

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain *(Figure 6)*. As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_O. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_O will be 10. The maximum input signal at f_O must therefore be less than 800 mV_{p-p} when the circuit is operated on ±5V supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 *(Figure 7)*. The notch output will be very small at f_O, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_O and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figures 7* through *15* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF10's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. *Figure 19* shows an equivalent circuit of the MF10 from which the output DC offsets can be calculated. Typical values for these offsets with $S_{A/B}$ tied to V^+ are:

V_{os1} = opamp offset = ±5 mV

V_{os2} = −150 mV @ 50:1 −300 mV @ 100:1

V_{os3} = −70 mV @ 50:1 −140 mV @ 100:1

When $S_{A/B}$ is tied to V^-, V_{os2} will approximately halve. The DC offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

3.0 Applications Information (Continued)

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1\left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} + 1\right)V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$$

$$R_p = R1//R3//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS1}\left[1 + \frac{R4}{R_p}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$$

$$Rp = R1//R2//R3$$

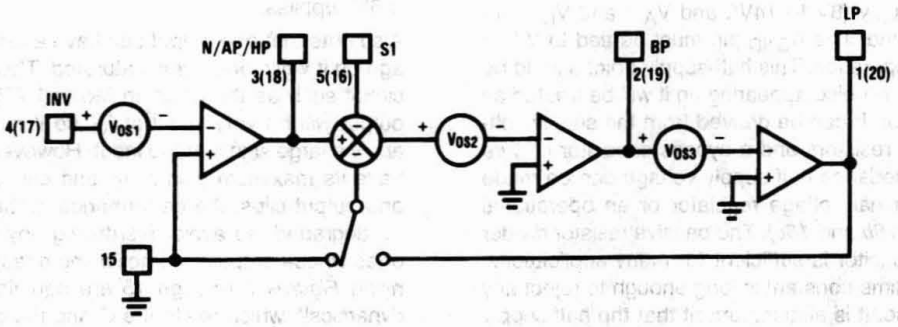

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FIGURE 19. MF10 Offset Voltage Sources

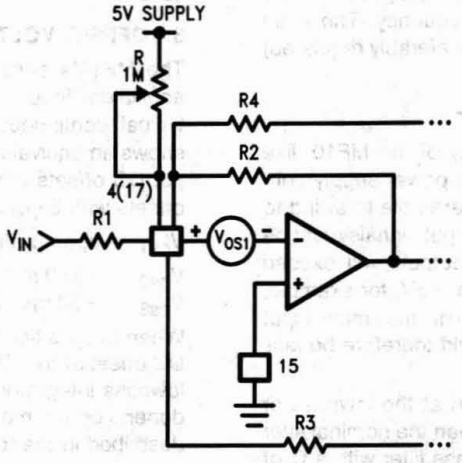

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FIGURE 20. Method for Trimming V_{OS}

3.0 Applications Information (Continued)

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower AC signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_O and Q. When operating in Mode 3, offsets can become excessively large if R2 and R4 are used to make f_{CLK}/f_O significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and $f_{CLK}/f_O = 250$ with pin 12 tied to ground (100:1 nominal). R4/R2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1V. Where necessary , the offset voltage can be adjusted by using the circuit of *Figure 20*. This allows adjustment of V_{OS1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{OS(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The MF10 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF10's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 100$ Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF10 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate *(Figure 21)*. If necessary, these can be "smoothed" with a simple R–C low-pass filter at the MF10 output.

The ratio of f_{CLK} to f_C (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in Section 3.4.

The accuracy of the f_{CLK}/f_O ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_O will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_O should be limited to 300 kHz when $f_O < 5$ kHz, and to 200 kHz for $f_O > 5$ kHz.

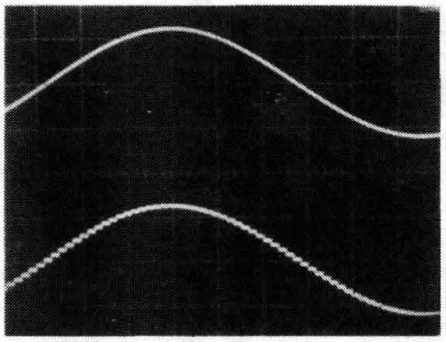

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FIGURE 21. The Sampled-Data Output Waveform

Section 8

Analog Switches/ Multiplexers

Section 8 Contents

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Analog Switches/Multiplexers Selection Guide 8-4
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AH5020C Monolithic Analog Current Switch 8-20
LF11331/LF13331/LF11332/LF13332/LF11333/LF13333, LF11201/LF13201/LF11202/LF13202 Quad SPST JFET Analog Switches 8-28
LF13508 8-Channel Analog Multiplexer 8-39
LF13509 4-Channel Differential Analog Multiplexer 8-39

Analog Switch Definition of Terms

R_{ON}: Resistance between the output and the input of an addressed channel.

C_S: Capacitance between any open terminal "S" and ground.

C_D: Capacitance between any open terminal "D" and ground.

$I_D - I_S$: Leakage current that flows from the closed switch into the body. This leakage is the difference between the current I_D going into the switch and the current I_S going out of the switch.

t_{RAN}: Delay time when switching from one address state to another.

t_{ON}: Delay time between the 50% points of an enable input and the switch ON condition.

t_{OFF}: Delay time between the 50% points of the enable input and the switch OFF condition.

National Semiconductor

Analog Switch/Multiplexer Selection Guide

Part Number	Function	Logic Input	V_S (Typ)	T_{ON}/T_{OFF} ns (Typ)	R_{ON} Ω
AH5011	QUAD SPST	TTL, CMOS	—	150/300	100
AH5012		TTL, CMOS	—	150/300	150
LF11201/LF13201	QUAD SPST	TTL	±15	90/500	200
LF11202/LF13202		TTL	±15	90/500	200
LF11331/LF13331		TTL	±15	90/500	200
LF11332/LF13332		TTL	±15	90/500	200
LF11333/LF13333		TTL	±15	90/500	200
AH5020	DUAL SPDT	TTL, CMOS	—	150/300	150
AH5010	4-CHANNEL	TTL, CMOS	—	150/300	150
LF13509	4-CHANNEL DIFFERENTIAL	TTL, CMOS	±18	1600/200	350
LF13508	8-CHANNEL	TTL, CMOS	±18	1600/200	350

National Semiconductor

AH0014/AH0014C* DPDT, AH0015/AH0015C Quad SPST, AH0019/AH0019C* Dual DPST-TTL/DTL Compatible MOS Analog Switches

General Description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in hermetic dual-in-line package.

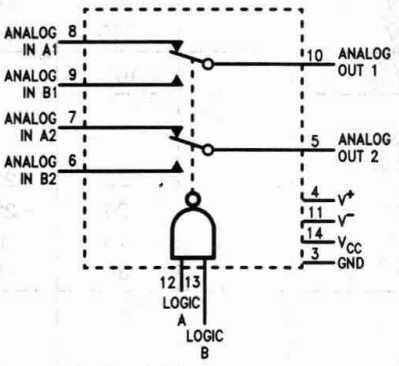
These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

Features

- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Analog signals in excess of 25 MHz
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

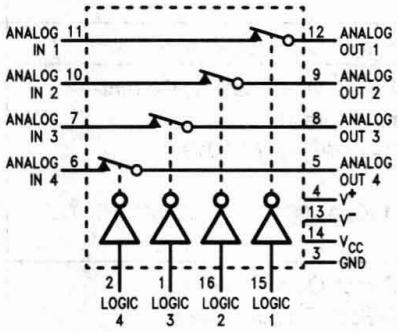
Block and Connection Diagrams



Note: All logic inputs shown at logic "1". TL/K/10125-1

Order Number AH0014D or AH0014CD
See NS Package Number D14D

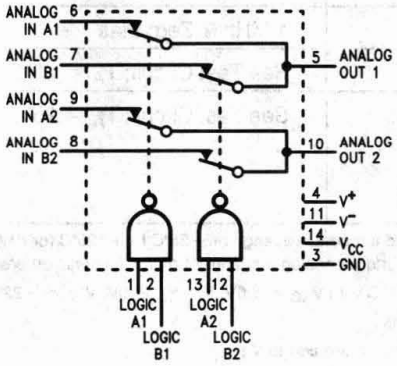
Quad SPST



Note: All logic inputs shown at logic "1". TL/K/10125-2

Order Number AH0015D or AH0015CD
See NS Package Number D16C

Dual DPST



Note: All logic inputs shown at logic "1".

TL/K/10125-3

Order Number AH0019D or AH0019CD
See NS Package Number D14D

*Previously called NH0014/NH0014C and NH0019/NH0019C

8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			1	μA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input—Each Gate (Note 3)	V_{CC} = 5.5V, V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input—Each Gate (Note 3)	V_{CC} = 5.5V, V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance—Each Gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current—Each Input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current—Each Output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time—t_{OFF}	See Test Circuit; T_A = 25°C		600	750	ns
Analog Turn-ON Time—t_{ON}	See Test Circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V. V^+ = +10V and an analog test current of 1 mA unless otherwise specified.

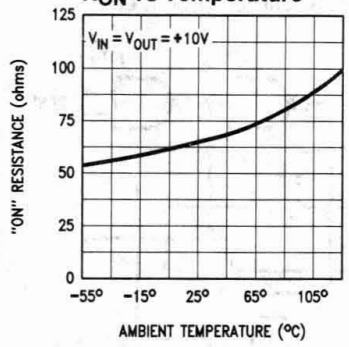
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

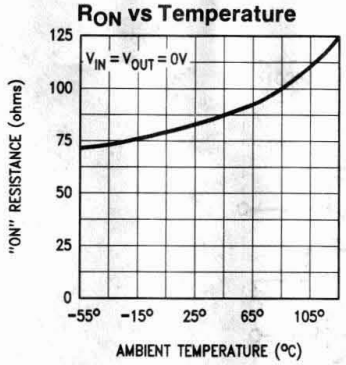
Note 4: All analog switch pins except measurement pin are tied to V^+.

Analog Switch Characteristics (Note 2)

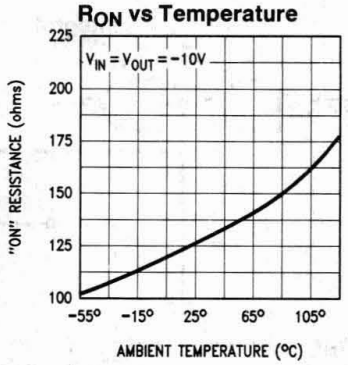
R_{ON} vs Temperature



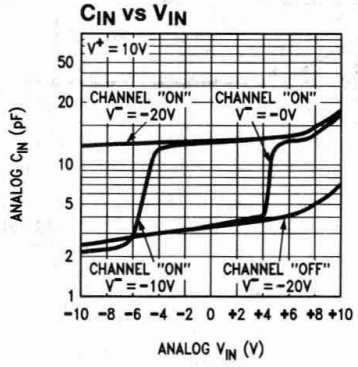
R_{ON} vs Temperature



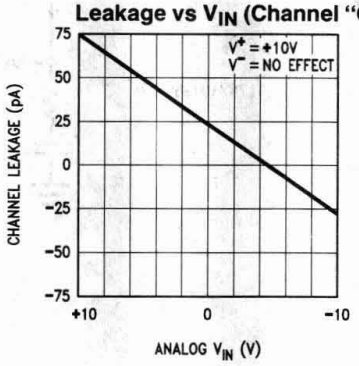
R_{ON} vs Temperature



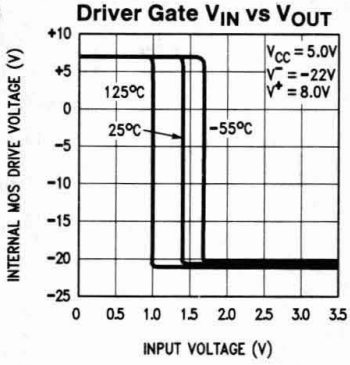
C_{IN} vs V_{IN}



Leakage vs V_{IN} (Channel "OFF")



Driver Gate V_{IN} vs V_{OUT}



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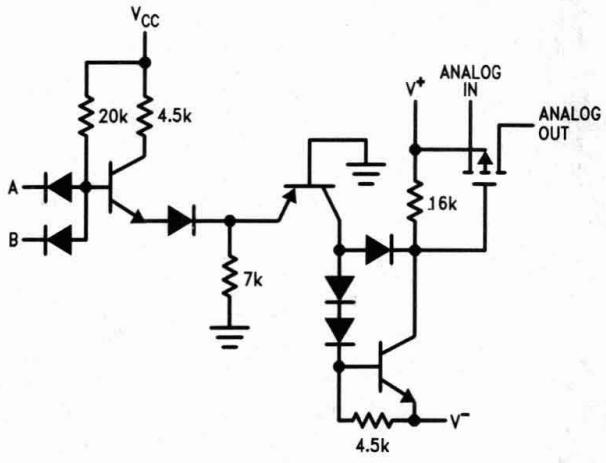
Schematic (Single Driver Gate and MOS Switch Shown)



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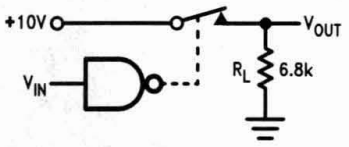
Analog Switching Time Test Circuit



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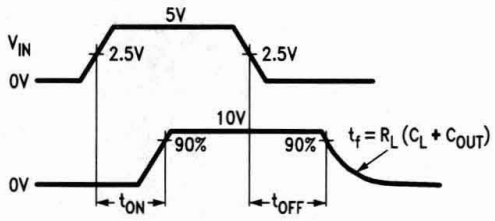

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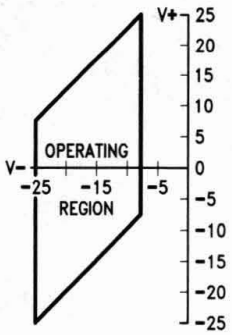
Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between $-25V$ and $-8V$. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



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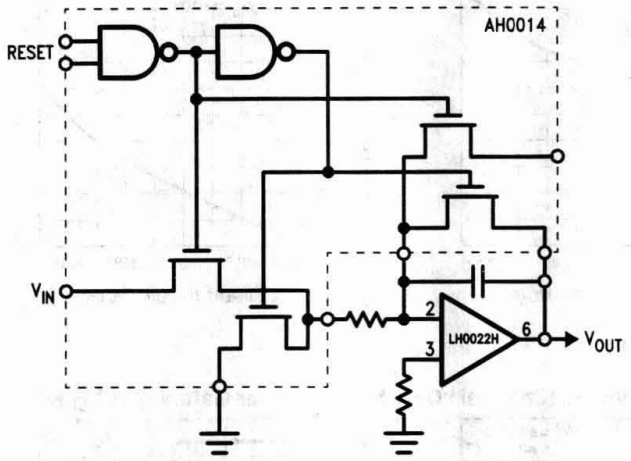
8

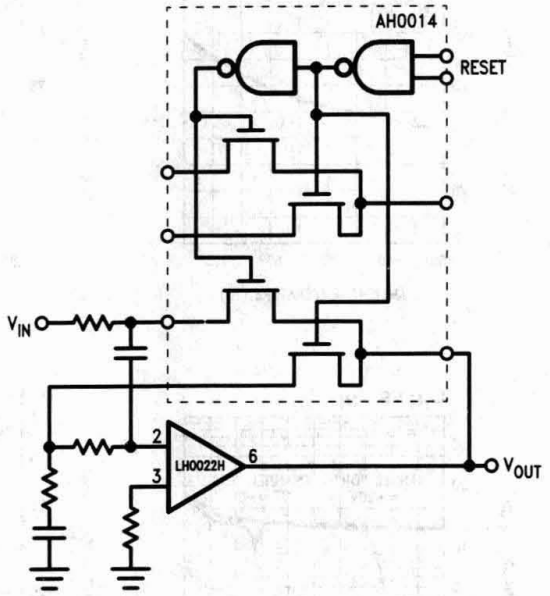
Typical Applications

Integrator



TL/K/10125–4

Reset Stabilized Amplifier



TL/K/10125–5

National Semiconductor

AH5010/AH5011/AH5012 Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches economically fulfills a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

Applications

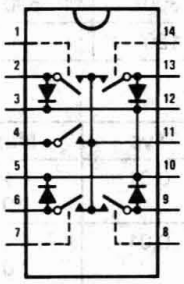
- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

■ Interfaces with standard TTL and CMOS	
■ "ON" resistance match	2Ω
■ Low "ON" resistance	100Ω
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

Connection and Schematic Diagrams (All switches shown are for logical "1" input)

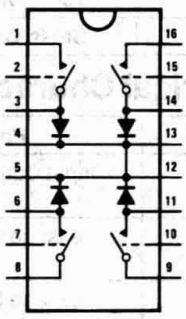
Dual-In-Line Package



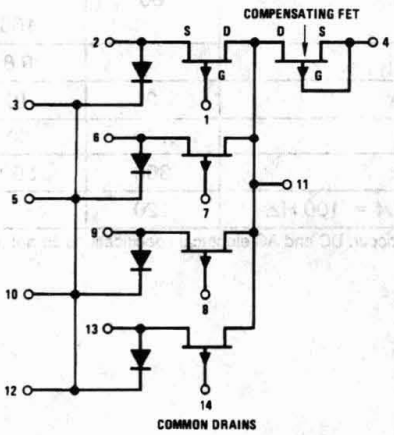
AH5010C MUX Switches
(4-Channel Version Shown)
Order Number AH5010CN
See NS Package Number M14A or N14A

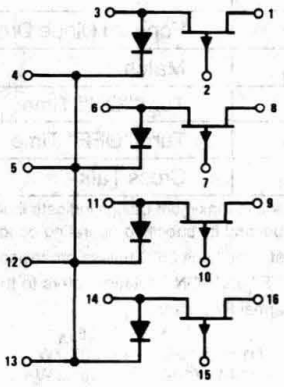
LOGIC DRIVE	4 CHANNEL MUX	4 SPST SWITCHES
5V LOGIC	AH5010C	AH5012C
15V LOGIC		AH5011C

Dual-In-Line Package



AH5011C and AH5012C SPST Switches
(Quad Version Shown)
Order Number AH5011CN,
AH5012CM or AH5012CN
See NS Package Number M16A or N16A





TL/H/5659–1

Note: All diode cathodes are internally connected to the substrate.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
AH5010/AH5011/AH5012	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Soldering Information:	
N Package 10 sec	300°C
SO Package Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics AH5010 and AH5012 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$4.5V \le V_{GD} \le 11V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 3.8V$ $T_A = 85°C$	0.02	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.08	1 200	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$	0.13	5 10	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$	0.1	10 20	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 0.35V$, $I_S = 2$ mA $T_A = +85°C$	90	150 240	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0V$, $I_D = 1$ mA	4	20	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit	120		dB

Electrical Characteristics AH5011 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$11V \le V_{GD} \le 15V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 10.3V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.04	0.5 100	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$		2 1	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$		5 2	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 1.5V$, $I_S = 2$ mA $T_A = 85°C$	60	100 160	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0V$, $I_D = 1$ mA	2	10	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	50	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit. f = 100 Hz.	120		dB

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Test conditions 25°C unless otherwise noted.

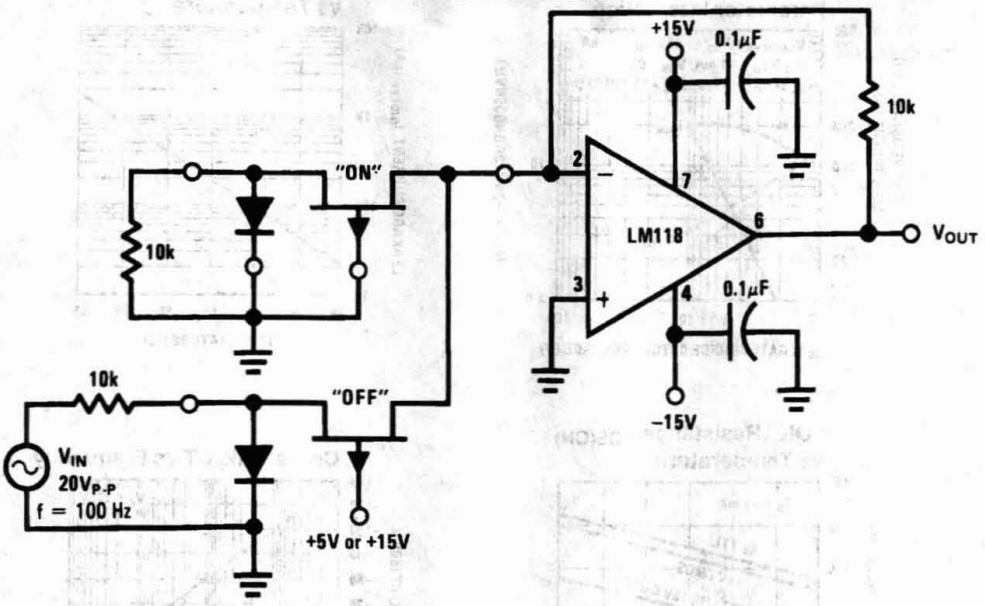
Note 3: "OFF" and "ON" notation refers to the conduction state of the FET switch.

Note 4: Thermal Resistance:

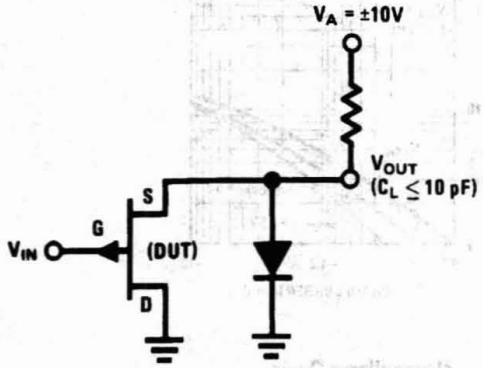
	θ_{JA}
N14A, N16A	92°C/W
M14A, M16A	115°C/W

Test Circuits and Switching Time Waveforms

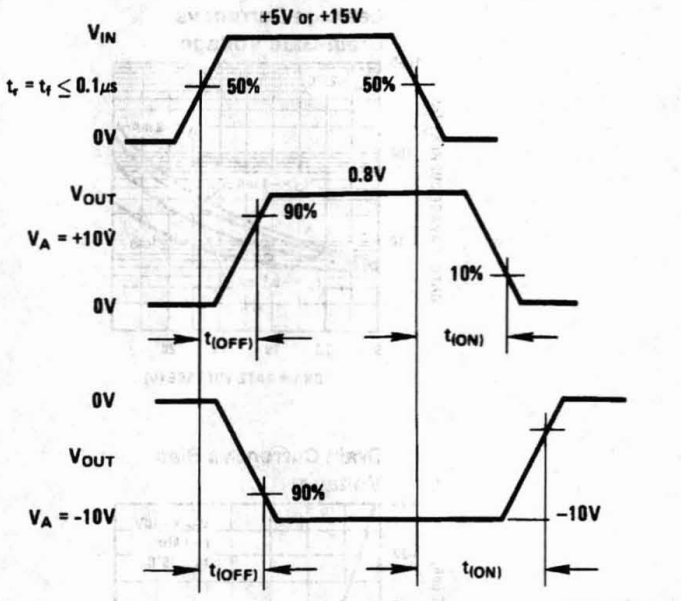
Cross Talk Test Circuit



AC Test Circuit



Time Waveforms



TL/H/5659–2

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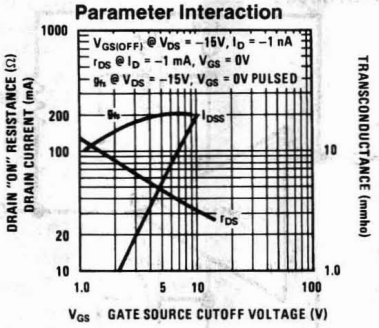
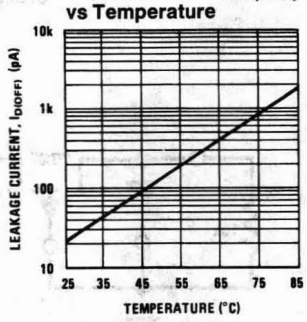
Typical Performance Characteristics

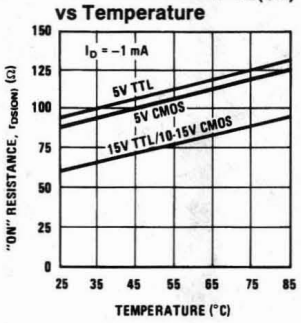
Parameter Interaction



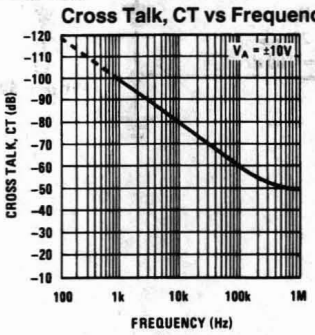
Leakage Current, $I_{D(OFF)}$ vs Temperature



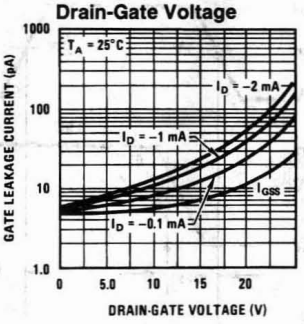
"ON" Resistance, $r_{DS(ON)}$ vs Temperature



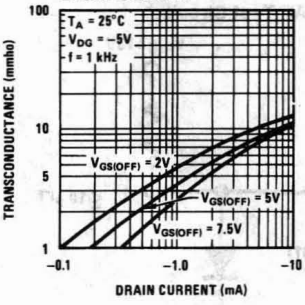
Cross Talk, CT vs Frequency



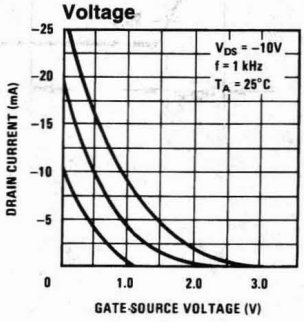
Leakage Current vs Drain-Gate Voltage



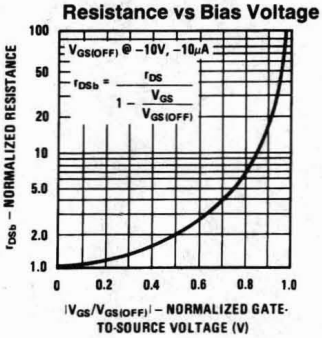
Transconductance vs Drain Current



Drain Current vs Bias Voltage



Normalized Drain Resistance vs Bias Voltage



TL/H/5659–3

Applications Information

Theory of Operation

The AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL, 5V-10V CMOS, open collector 15V TTL/CMOS.

Two basic switch configurations are available: 4 independent switches (SPST) and 4 pole switches used for multiplexing (4 PST-MUX). The MUX versions such as the AH5010 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V input will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AH series of analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{min} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \quad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \quad (2b)$$

whichever is larger.

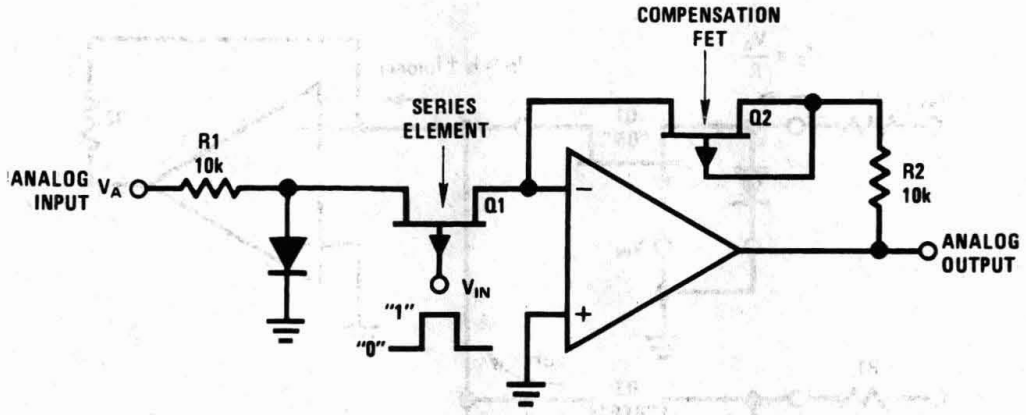
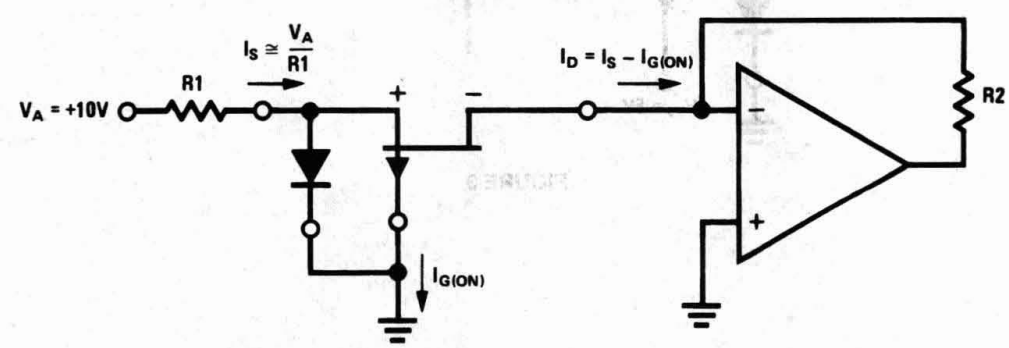


FIGURE 1. Use of Compensation FET



TL/H/5659–4

FIGURE 2. On Leakage Current, $I_{G(ON)}$

8

Applications Information (Continued)

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal
A_D = Desired accuracy
$I_{G(ON)}$ = Leakage at a given I_S
I_{DSS} = Saturation current of the FET switch
≅ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{(10V)}{\left(\frac{20\ mA}{10}\right)} = 5\ k\Omega$$

For R1 = 5k, I_S ≅ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\ \mu A$ at 85°C for the AH5010. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value of the analog input signal
A_D = Desired accuracy
N = Number of channels
$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq 10$ nA at 85°C for the AH5010. $R1_{(MAX)}$ is:

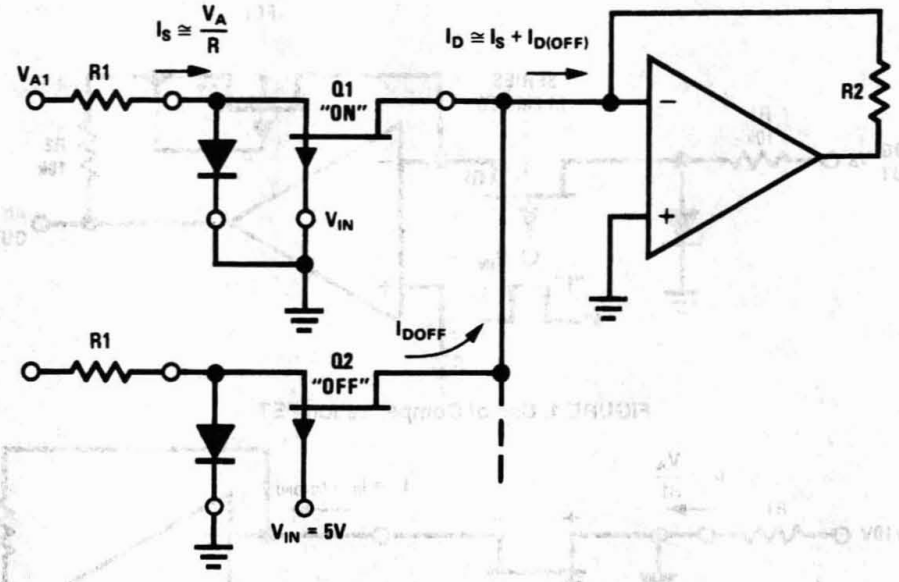
$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

TTL Compatibility

The AH series can be driven with two different logic voltage swings: the even numbered part types are specified to be driven from standard 5V TTL logic and the odd numbered types from 15V open collector TTL.



TL/H/5659–5

FIGURE 3

Applications Information (Continued)

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5*. In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} at the expense of power dissipation in the low state.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6*.

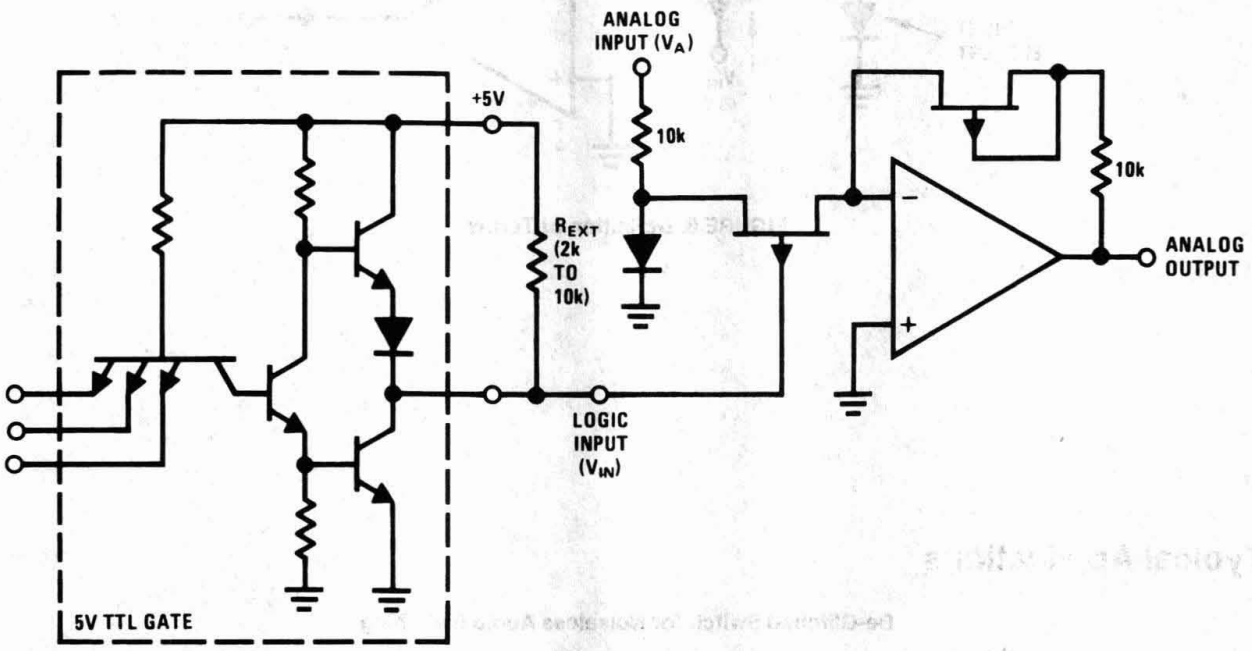
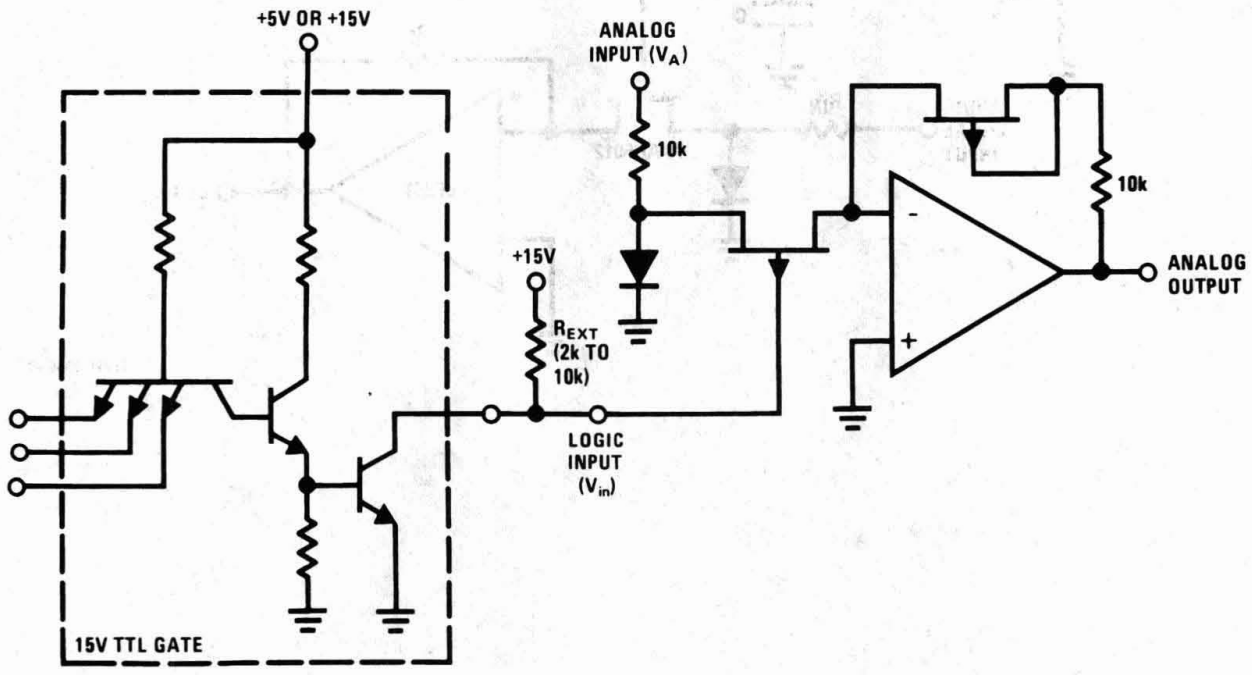


FIGURE 4. Interfacing with +5V TTL



TL/H/5659–6

FIGURE 5. Interfacing with +15V Open Collector TTL

8

Applications Information (Continued)

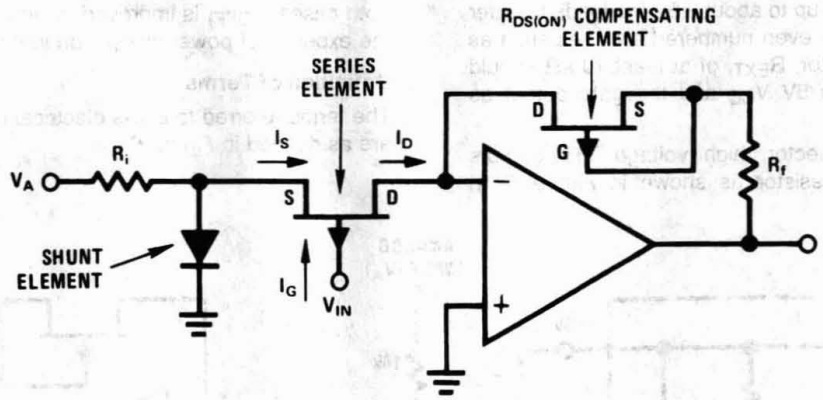
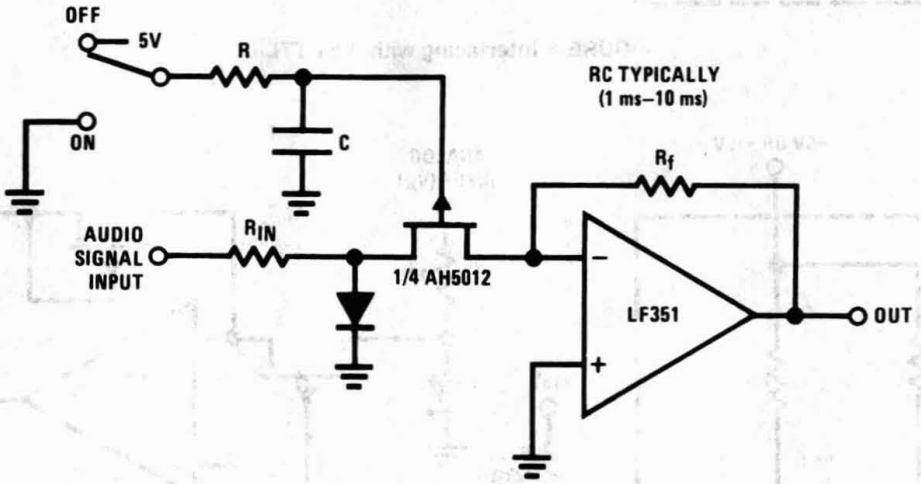


FIGURE 6. Definition of Terms

Typical Applications

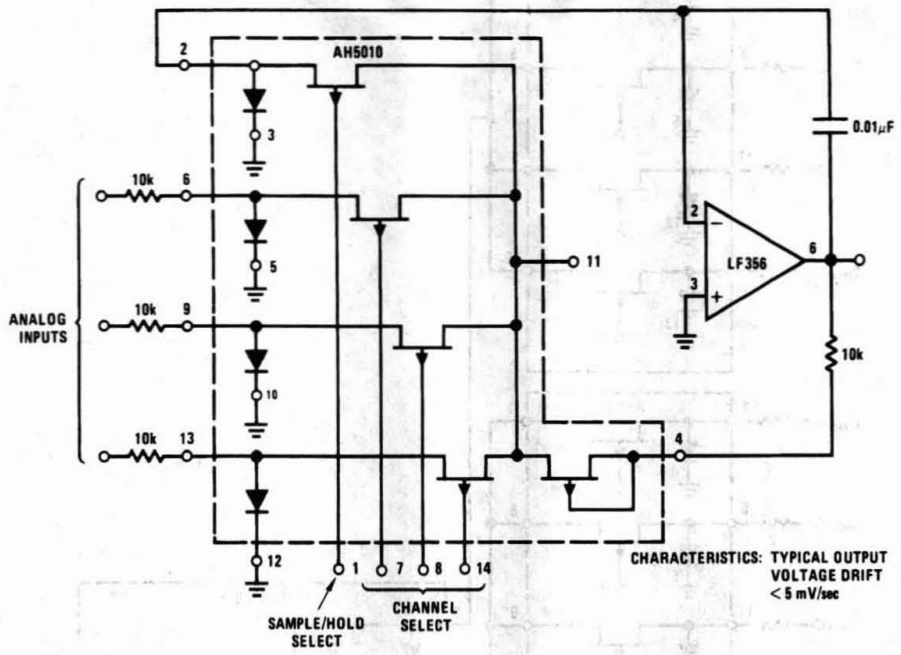
De-Glitched Switch for Noiseless Audio Switching



TL/H/5659–7

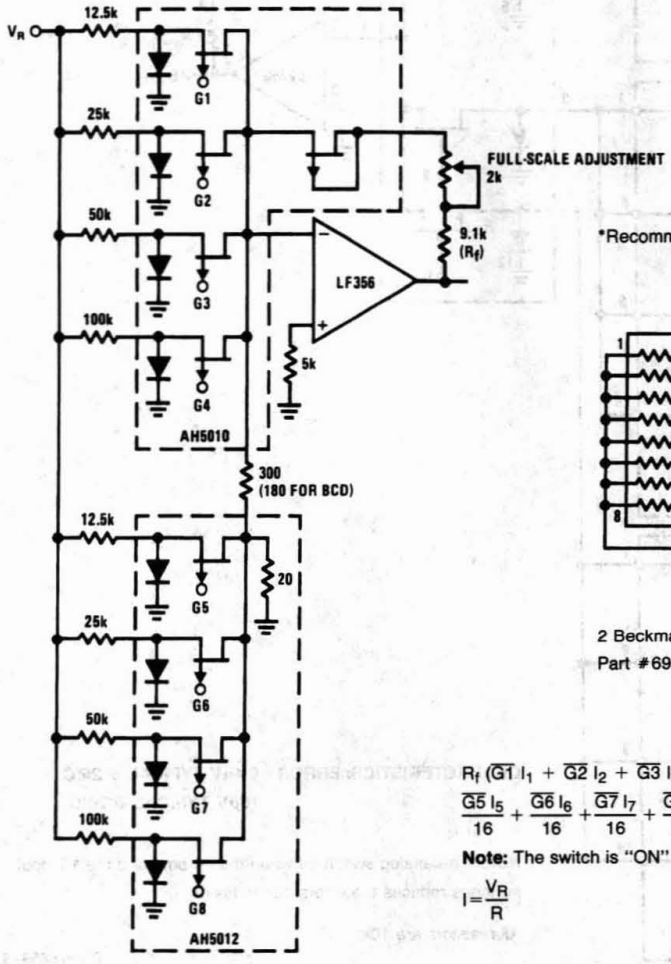
Typical Applications (Continued)

3-Channel Multiplexer with Sample and Hold

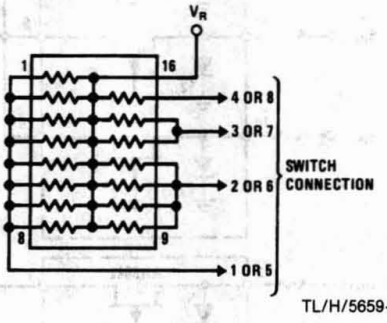


TL/H/5659–8

8-Bit Binary (BCD) Multiplying D/A Converter*



*Recommended resistor array connection for D/A application



TL/H/5659–12

2 Beckman resistor arrays
Part #698-1-R 100k B recommended

$$R_f \left(\overline{G1}\, I_1 + \overline{G2}\, I_2 + \overline{G3}\, I_3 + \overline{G4}\, I_4 + \frac{\overline{G5}\, I_5}{16} + \frac{\overline{G6}\, I_6}{16} + \frac{\overline{G7}\, I_7}{16} + \frac{\overline{G8}\, I_8}{16}\right)$$

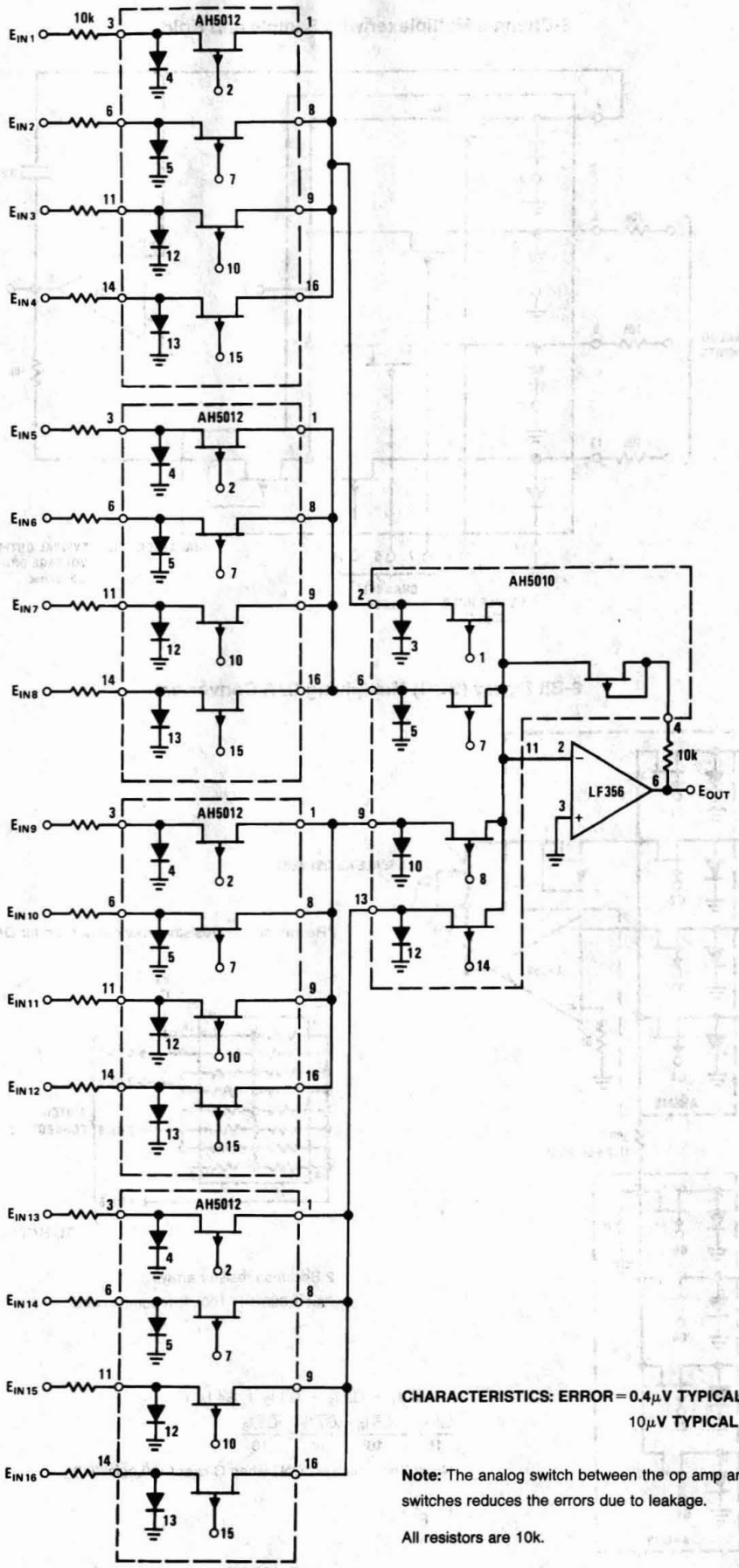
Note: The switch is "ON" when G is at 0V (Logic "0")

$$I = \frac{V_R}{R}$$

TL/H/5659–11

Typical Applications (Continued)

16-Channel Multiplexer



CHARACTERISTICS: ERROR = 0.4μV TYPICAL @ 25°C
10μV TYPICAL @ 70°C

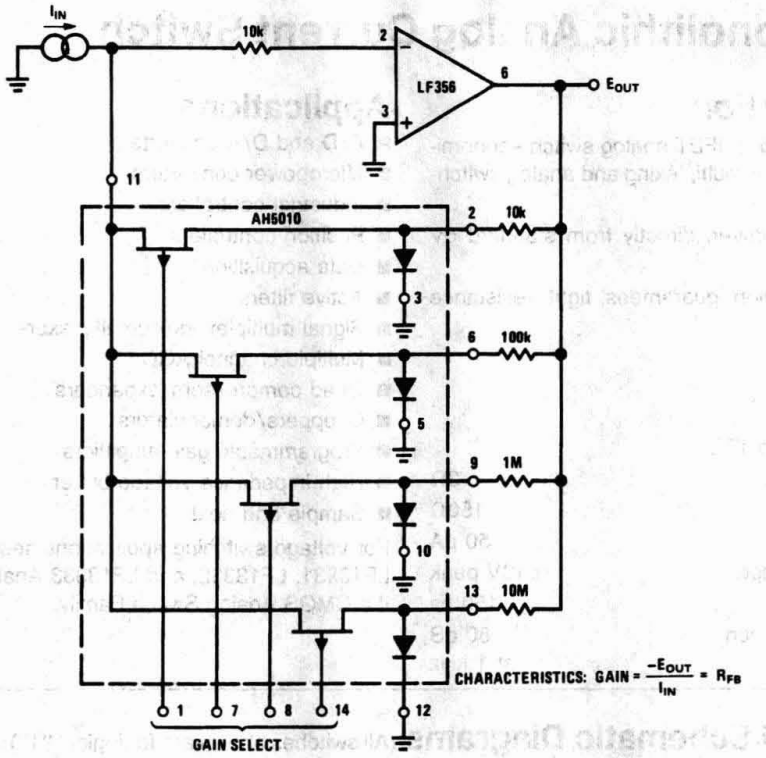
Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k.

TL/H/5659–9

Typical Applications (Continued)

Gain Programmable Amplifier



TL/H/5659–10

National Semiconductor

AH5020C Monolithic Analog Current Switch

General Description

This versatile dual monolithic JFET analog switch economically fulfills a wide variety of multiplexing and analog switching applications.

These switches may be driven directly from standard 5V logic.

The monolithic construction guarantees tight resistance match and track.

Features

■ Interfaces with standard TTL	
■ "ON" resistance match	2Ω
■ Low "ON" resistance	150Ω
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

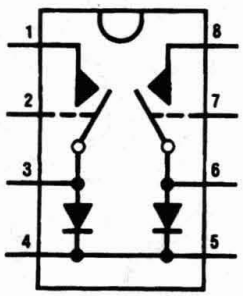
Applications

- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

For voltage switching applications see LF13201, LF13202, LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

Connection and Schematic Diagrams (All switches shown are for logical "1")

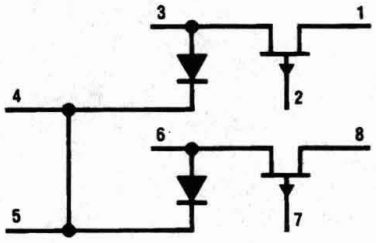
Dual-In-Line Package



TL/H/5166–1

Top View

Order Number AH5020CJ
See NS Package Number J08A



TL/H/5166–2

Note: All diode cathodes are internally connected to the substrate.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA
Drain Current	30 mA
Power Dissipation	500 mW
Operating Temp. Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Notes 2 and 3)

Symbols	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	V_{GD} = 4.5V, V_{SD} = 0.7V	0.01	0.1	nA
		V_{GD} = 11V, V_{SD} = 0.7V	0.01	0.2	nA
		T_A = 85°C, V_{GD} = 11V, V_{SD} = 0.7V		10	nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 3.8V	0.01	0.2	nA
		T_A = 85°C		10	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA	0.08	1	nA
		T_A = 85°C		200	nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA	0.13	5	nA
		T_A = 85°C		10	μA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA	0.1	10	nA
		T_A = 85°C		20	μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0.5V, I_S = 2 mA	90	150	Ω
		T_A = +85°C		240	Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	2	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Test conditions 25°C unless otherwise noted.

Note 3: "OFF" and "ON" notation refers to the conduction state of the FET switch.

Note 4: Thermal Resistance:

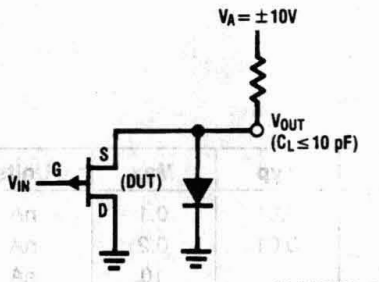
θ_{JA} (Junction to Ambient) ..... N/A

θ_{JC} (Junction to Case) ..... N/A

8

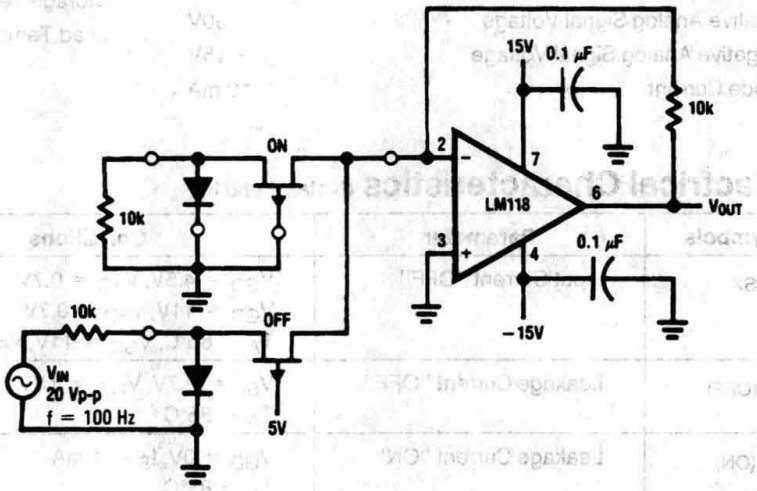
Test Circuits

AC Test Circuit



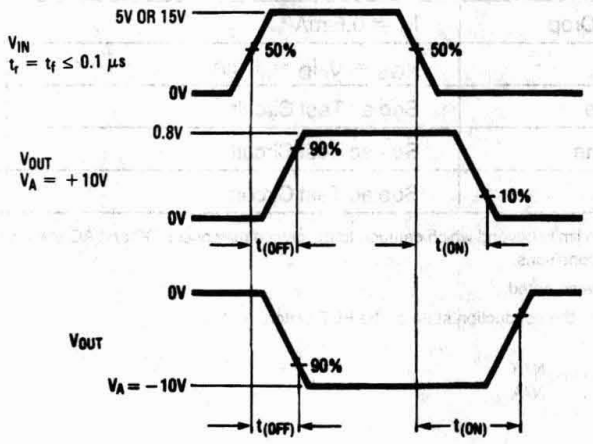
TL/H/5166–4

Cross Talk Test Circuit



TL/H/5166–3

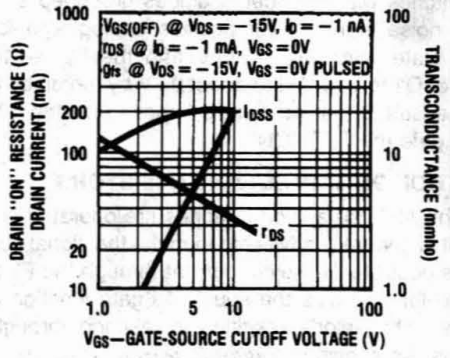
Switching Time Waveforms



TL/H/5166–5

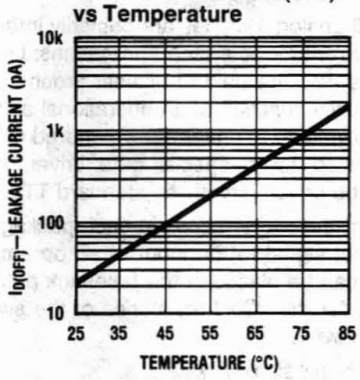
Typical Performance Characteristics

Parameter Interaction



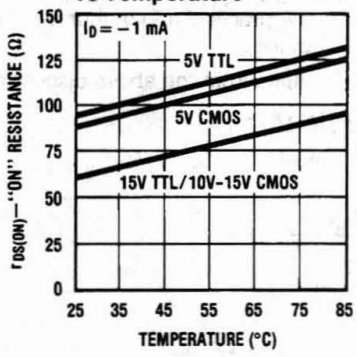
TL/H/5166–6

Leakage Current, $I_{D(OFF)}$ vs Temperature



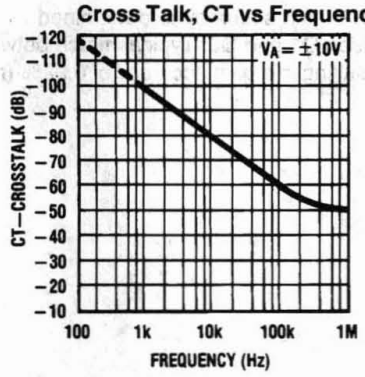
TL/H/5166–7

"ON" Resistance, $r_{DS(ON)}$ vs Temperature



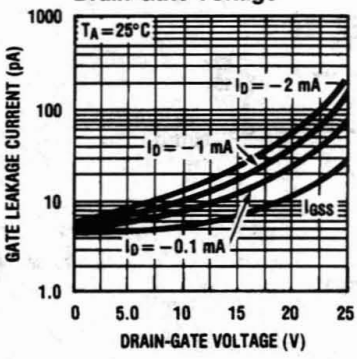
TL/H/5166–8

Cross Talk, CT vs Frequency



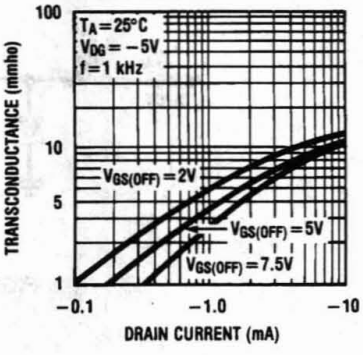
TL/H/5166–9

Leakage Current vs Drain-Gate Voltage



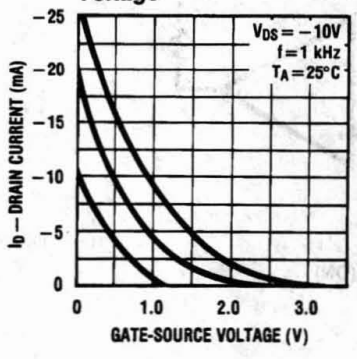
TL/H/5166–10

Transconductance vs Drain Current



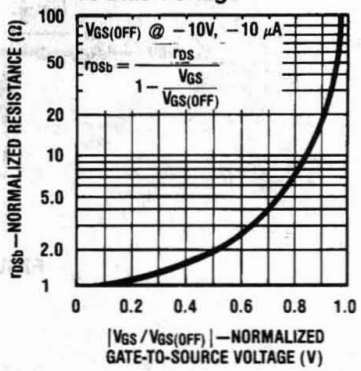
TL/H/5166–11

Drain Current vs Bias Voltage



TL/H/5166–12

Normalized Drain Resistance vs Bias Voltage



TL/H/5166–13

8

Applications Information

THEORY OF OPERATION

The AH5020 analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL.

If only one of the two switches in each package is used to apply an input signal to the input of an op amp, the other switch FET can be placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = -\frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 2Ω resulting in a gain accuracy of 0.02% (for R1 = R2 = 10 kΩ).

NOISE IMMUNITY

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V input will not gate the FET "ON".

SELECTION OF GAIN SETTING RESISTORS

Since the AH5020 analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

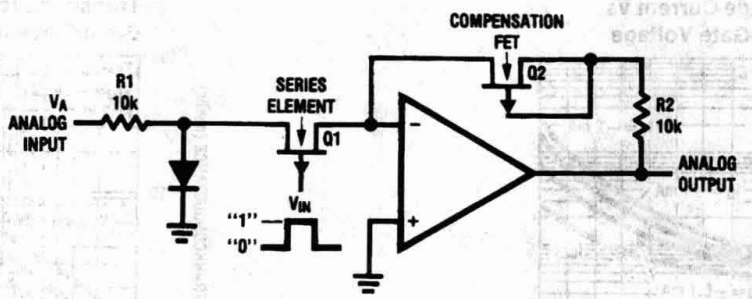
Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \quad (2a)$$

or:

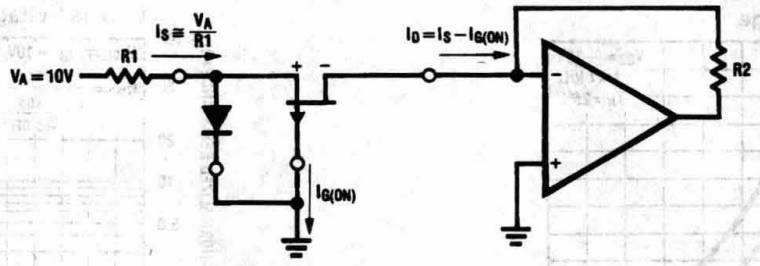
$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \quad (2b)$$

whichever is larger.



TL/H/5166–14

FIGURE 1. Use of Compensation FET



TL/H/5166–15

FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

Where $V_{A(MAX)}$ = Peak amplitude of the analog input signal
A_D = Desired accuracy
$I_{G(ON)}$ = Leakage at a given I_S
I_{DSS} = Saturation current of the FET switch = 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AH5020. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

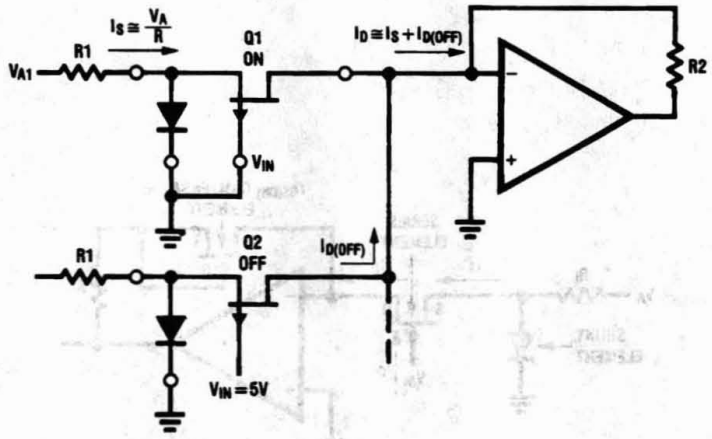
Where $V_{A(MIN)}$ = Minimum value for the analog input signal
A_D = Desired accuracy
N = Number of channels
$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AH5020. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp — all of which should be considered in setting the overall gain accuracy of the circuit.



TL/H/5166–16

FIGURE 3. Off Leakage Current, $I_{D(OFF)}$

8

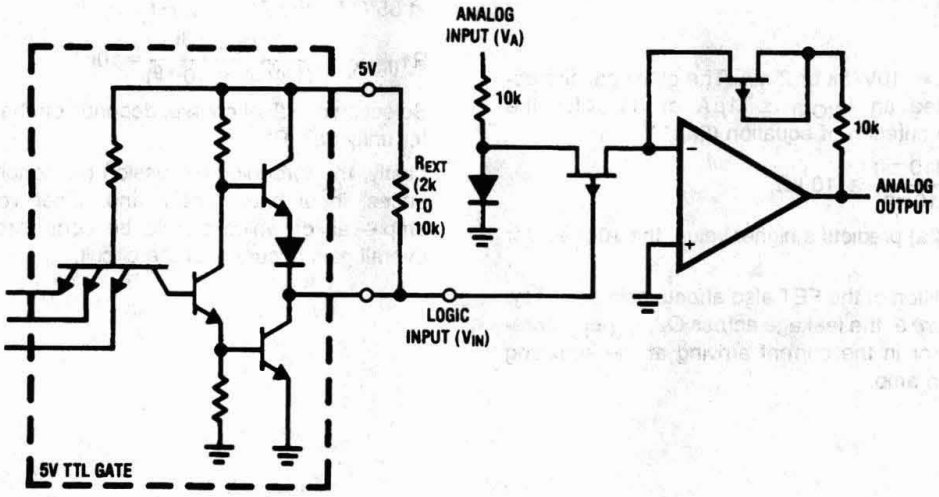
Applications Information (Continued)

TTL COMPATIBILITY

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the AH5020, a pull-up resistor, R_{EXT} of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

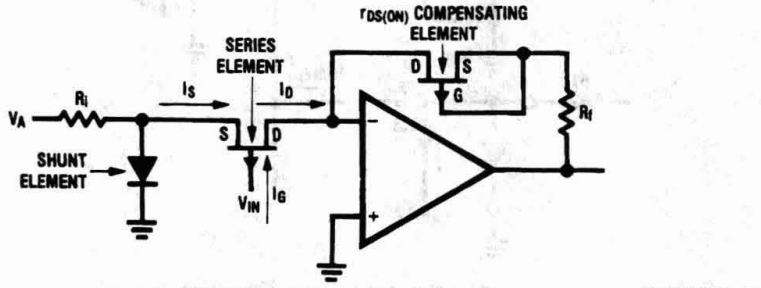
DEFINITION OF TERMS

The terms referred to in the electrical characteristics tables are as defined in *Figure 5*.



TL/H/5166–17

FIGURE 4. Interfacing with +5V TTL

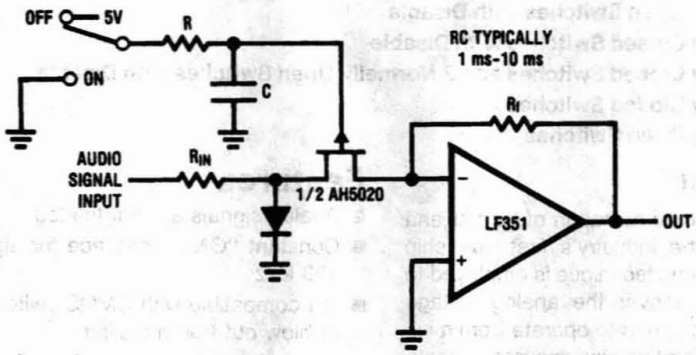


TL/H/5166–18

FIGURE 5. Definition of Terms

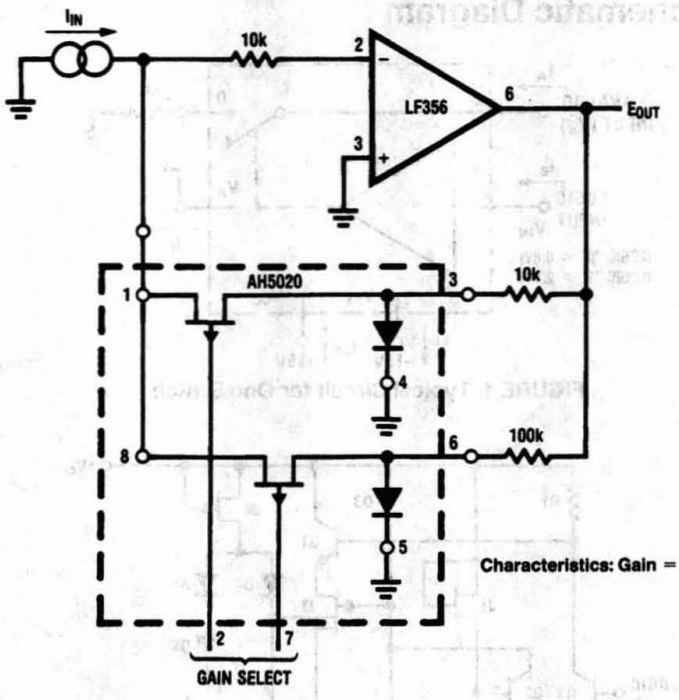
Typical Applications

Deglitched Switch for Noiseless Audio Switching



TL/H/5166–19

Gain Programmable Amplifier



Characteristics: Gain $= \frac{-E_{OUT}}{I_{IN}} = R_{FS}$

TL/H/5166–20

8

National Semiconductor

Quad SPST JFET Analog Switches

LF11331, LF13331 4 Normally Open Switches with Disable
LF11332, LF13332 4 Normally Closed Switches with Disable
LF11333, LF13333 2 Normally Closed Switches and 2 Normally Open Switches with Disable
LF11201, LF13201 4 Normally Closed Switches
LF11202, LF13202 4 Normally Open Switches

General Description

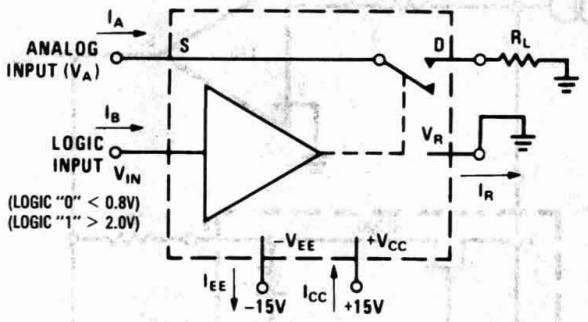
These devices are a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad JFET switch. A unique circuit technique is employed to maintain a constant resistance over the analog voltage range of ±10V. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break-before-make action.

These devices operate from ±15V supplies and swing a ±10V analog signal. The JFET switches are designed for applications where a dc to medium frequency analog signal needs to be controlled.

Features

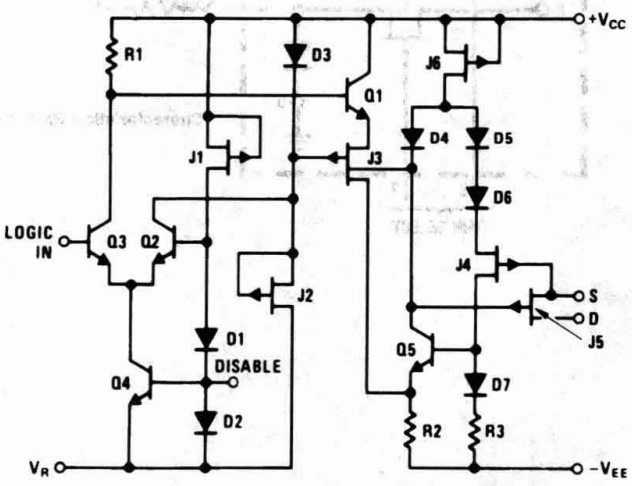
- Analog signals are not loaded
- Constant "ON" resistance for signals up to ±10V and 100 kHz
- Pin compatible with CMOS switches with the advantage of blow out free handling
- Small signal analog signals to 50 MHz
- Break-before-make action $t_{OFF} < t_{ON}$
- High open switch isolation at 1.0 MHz −50 dB
- Low leakage in "OFF" state <1.0 nA
- TTL, DTL, RTL compatibility
- Single disable pin opens all switches in package on LF11331, LF11332, LF11333
- LF11201 is pin compatible with DG201

Test Circuit and Schematic Diagram



TL/H/5667–2

FIGURE 1. Typical Circuit for One Switch



TL/H/5667–12

FIGURE 2. Schematic Diagram (Normally Open)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 1)

Supply Voltage ($V_{CC}-V_{EE}$)	36V
Reference Voltage	$V_{EE} \le V_R \le V_{CC}$
Logic Input Voltage	$V_R-4.0V \le V_{IN} \le V_R+6.0V$
Analog Voltage	$V_{EE} \le V_A \le V_{CC}+6V$; $V_A \le V_{EE}+36V$
Analog Current	$\|I_A\| < 20$ mA

Power Dissipation (Note 2)	
Molded DIP (N Suffix)	500 mW
Cavity DIP (D Suffix)	900 mW
Operating Temperature Range	
LF11201, 2 and LF11331, 2, 3	−55°C to +125°C
LF13201, 2 and LF13331, 2, 3	0°C to +70°C
Storage Temperature	−65°C to +150°C
Soldering Information	
N and D Package (10 sec.)	300°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions		LF11331/2/3 LF11201/2			LF13331/2/3 LF13201/2			Units
				Min	Typ	Max	Min	Typ	Max	
R_{ON}	"ON" Resistance	$V_A=0$, $I_D=1$ mA	$T_A=25°C$		150	200		150	250	Ω
					200	300		200	350	Ω
R_{ON} Match	"ON" Resistance Matching		$T_A=25°C$		5	20		10	50	Ω
V_A	Analog Range			±10	±11		±10	±11		V
$I_{S(ON)}$ + $I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON," $V_S=V_D=\pm10V$	$T_A=25°C$		0.3	5		0.3	10	nA
					3	100		3	30	nA
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF," $V_S=+10V$, $V_D=-10V$	$T_A=25°C$		0.4	5		0.4	10	nA
					3	100		3	30	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF," $V_S=+10V$, $V_D=-10V$	$T_A=25°C$		0.1	5		0.1	10	nA
					3	100		3	30	nA
V_{INH}	Logical "1" Input Voltage			2.0			2.0			V
V_{INL}	Logical "0" Input Voltage					0.8			0.8	V
I_{INH}	Logical "1" Input Current	$V_{IN}=5V$	$T_A=25°C$		3.6	10		3.6	40	μA
						25			100	μA
I_{INL}	Logical "0" Input Current	$V_{IN}=0.8$	$T_A=25°C$			0.1			0.1	μA
						1			1	μA
t_{ON}	Delay Time "ON"	$V_S=\pm10V$, *(Figure 3)*	$T_A=25°C$		500			500		ns
t_{OFF}	Delay Time "OFF"	$V_S=\pm10V$, *(Figure 3)*	$T_A=25°C$		90			90		ns
$t_{ON}-t_{OFF}$	Break-Before-Make	$V_S=\pm10V$, *(Figure 3)*	$T_A=25°C$		80			80		ns
$C_{S(OFF)}$	Source Capacitance	Switch "OFF," $V_S=\pm10V$	$T_A=25°C$		4.0			4.0		pF
$C_{D(OFF)}$	Drain Capacitance	Switch "OFF," $V_D=\pm10V$	$T_A=25°C$		3.0			3.0		pF
$C_{S(ON)}$ + $C_{D(ON)}$	Active Source and Drain Capacitance	Switch "ON," $V_S=V_D=0V$	$T_A=25°C$		5.0			5.0		pF
$I_{SO(OFF)}$	"OFF" Isolation	*(Figure 4)*, (Note 4)	$T_A=25°C$		−50			−50		dB
CT	Crosstalk	*(Figure 4)*, (Note 4)	$T_A=25°C$		−65			−65		dB
SR	Analog Slew Rate	(Note 5)	$T_A=25°C$		50			50		V/μs
I_{DIS}	Disable Current	*(Figure 5)*, (Note 6)	$T_A=25°C$		0.4	1.0		0.6	1.5	mA
					0.6	1.5		0.9	2.3	mA
I_{EE}	Negative Supply Current	All Switches "OFF," $V_S=\pm10V$	$T_A=25°C$		3.0	5.0		4.3	7.0	mA
					4.2	7.5		6.0	10.5	mA
I_R	Reference Supply Current	All Switches "OFF," $V_S=\pm10V$	$T_A=25°C$		2.0	4.0		2.7	5.0	mA
					2.8	6.0		3.8	7.5	mA
I_{CC}	Positive Supply Current	All Switches "OFF," $V_S=\pm10V$	$T_A=25°C$		4.5	6.0		7.0	9.0	mA
					6.3	9.0		9.8	13.5	mA

Note 1: Refer to RETSF11201X, RETSF11331X, RETSF11332X and RETSF11333X for military specifications.

Note 2: For operating at high temperature the molded DIP products must be derated based on a +100°C maximum junction temperature and a thermal resistance of +150°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at ±100°C/W.

Note 3: Unless otherwise specified, $V_{CC}=+15V$, $V_{EE}=-15V$, $V_R=0V$, and limits apply for $-55°C \le T_A \le +125°C$ for the LF11331/2/3 and the LF11201/2, $-25°C \le T_A \le +85°C$ for the LF13331/2/3 and the LF13201/2.

Note 4: These parameters are limited by the pin to pin capacitance of the package.

Note 5: This is the analog signal slew rate above which the signal is distorted as a result of finite internal slew rates.

Note 6: All switches in the device are turned "OFF" by saturating a transistor at the disable node as shown in *Figure 5*. The delay time will be approximately equal to the t_{ON} or t_{OFF} plus the delay introduced by the external transistor.

Note 7: This graph indicates the analog current at which 1% of the analog current is lost when the drain is positive with respect to the source.

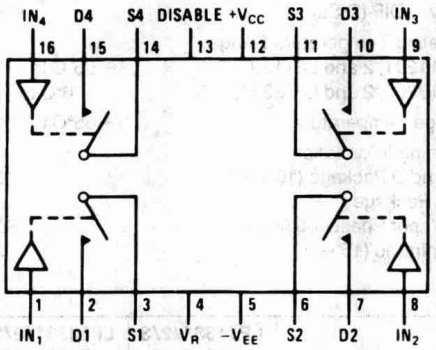
Note 8: θ_{JA} (Typical) Thermal Resistance

Molded DIP (N)	85°C/W
Cavity DIP (D)	100°C/W
Small Outline (M)	105°C/W

8

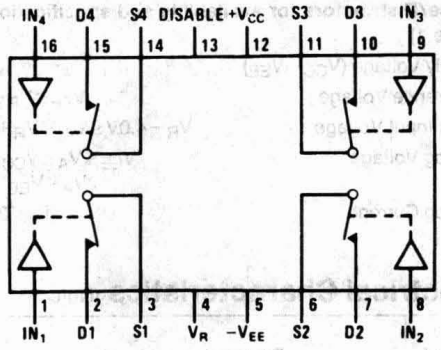
Connection Diagrams (Top View for SO and Dual-In-Line Packages) (All Switches Shown are For Logical "0")

LF11331/LF13331



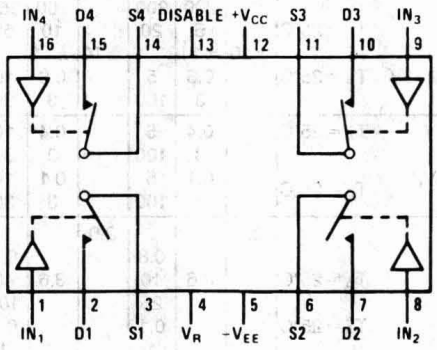
TL/H/5667–1

LF11332/LF13332



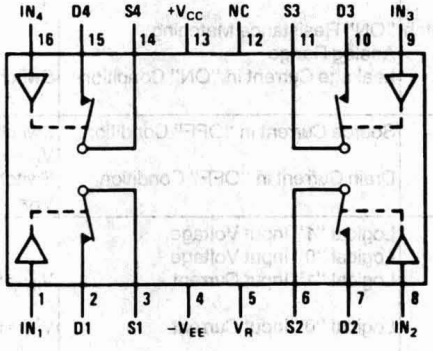
TL/H/5667–13

LF11333/LF13333



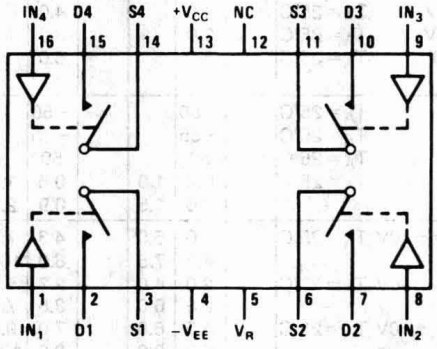
TL/H/5667–14

LF11201/LF13201



TL/H/5667–15

LF11202/LF13202



TL/H/5667–16

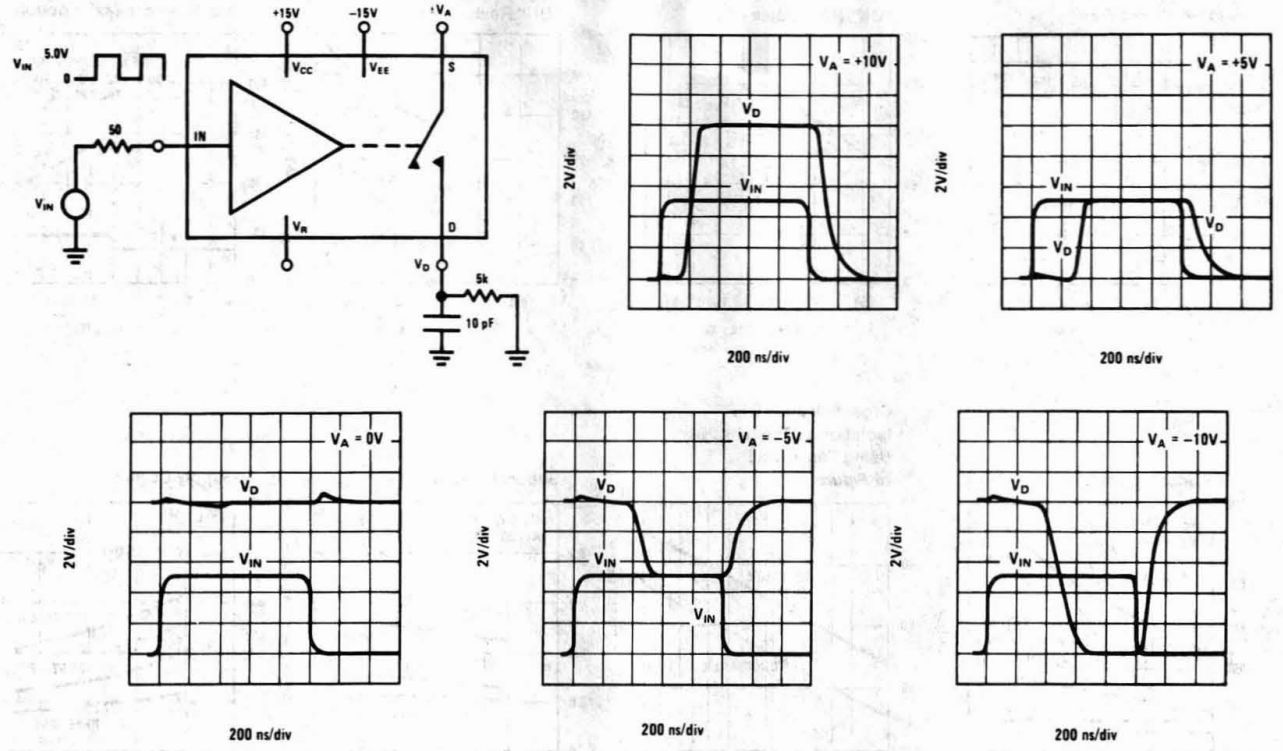
Order Number LF13201D, LF11201D, LF11201D/883, LF13202D, LF11202D, LF11202D/883, LF13331D, LF11331D, LF11331D/883, LF13332D, LF11332D, LF11332D/883, LF13333D, LF11333D or LH11333D/883
See NS Package Number D16C

Order Number LF13201M, LF13202M, LF13331M, LF13332M or LF13333M
See NS Package Number M16A

Order Number LF13201N, LF13202N, LF13331N, LF13332N or LF13333N
See NS Package Number N16A

Test Circuit and Typical Performance Curves

Delay Time, Rise Time, Settling Time, and Switching Transients



TL/H/5667–3

Additional Test Circuits

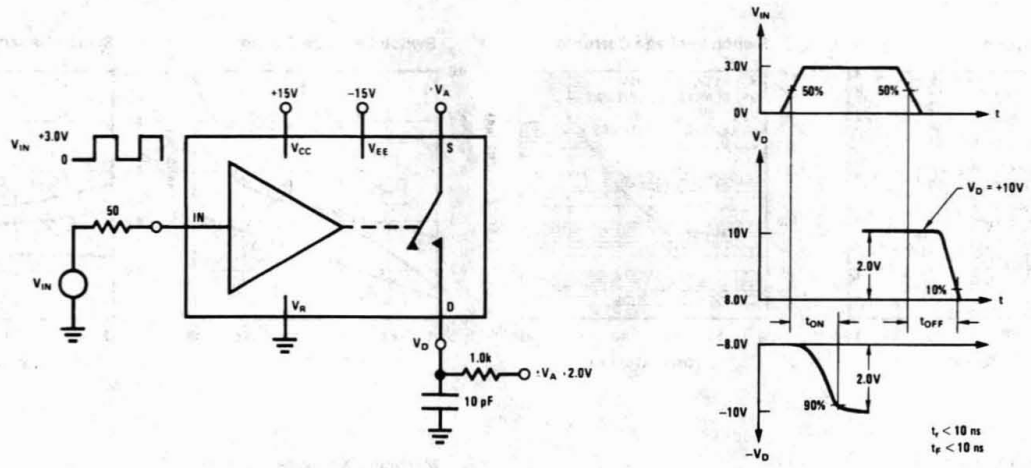
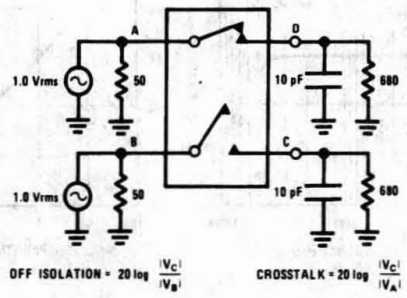


FIGURE 3. t_{ON}, t_{OFF} Test Circuit and Waveforms for a Normally Open Switch



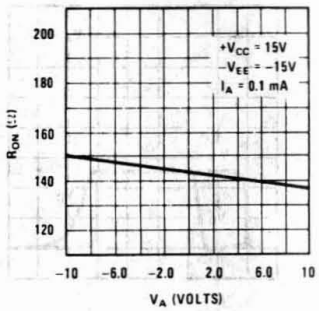
TL/H/5667–4

FIGURE 4. "OFF" Isolation, Crosstalk, Small Signal Response

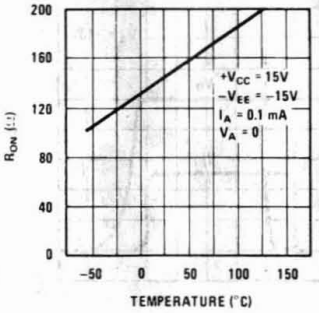
8

Typical Performance Characteristics

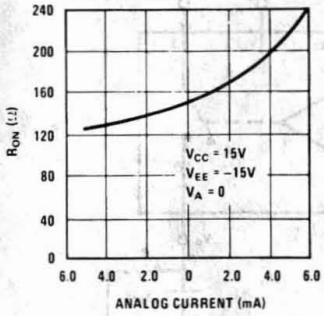
"ON" Resistance



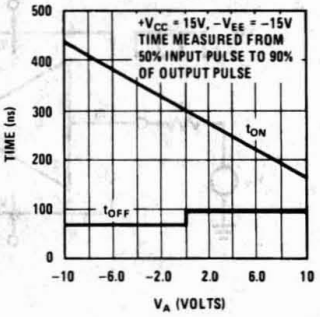
"ON" Resistance



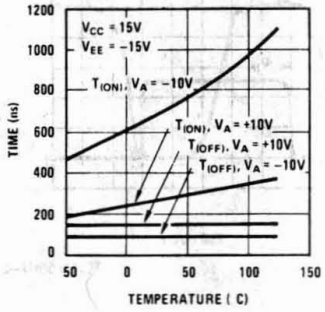
"ON" Resistance



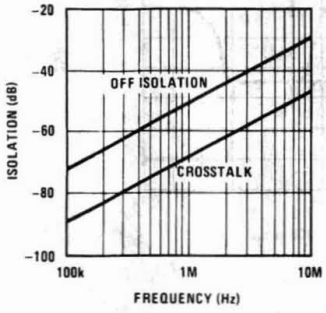
Break-Before-Make Action



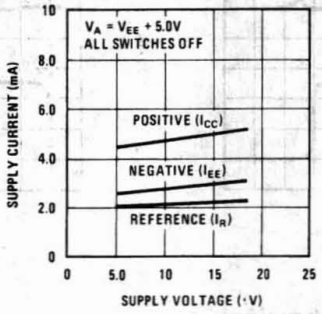
Switching Times



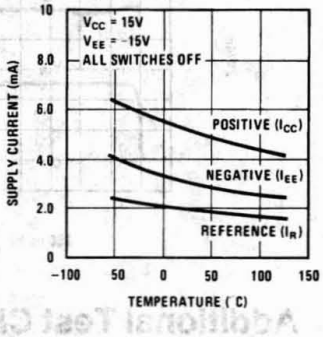
Crosstalk and "OFF" Isolation vs Frequency Using Test Circuit of *Figure 5*



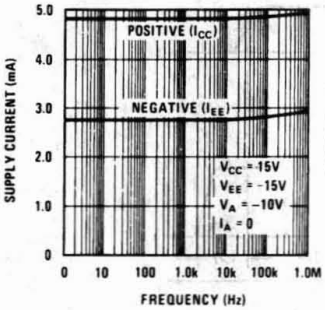
Supply Current



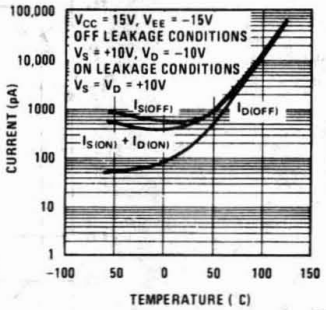
Supply Current



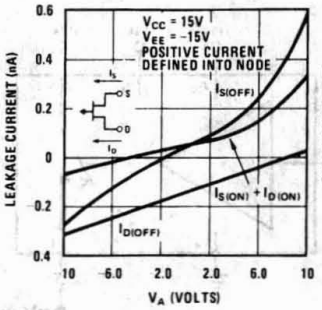
Supply Current



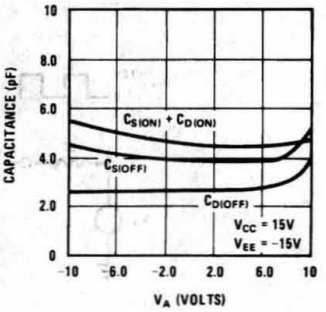
Switch Leakage Currents



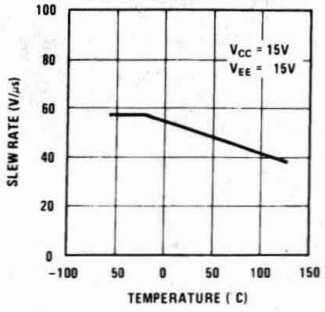
Switch Leakage Current



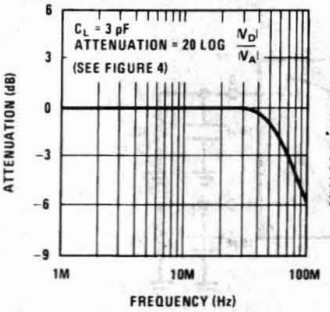
Switch Capacitances



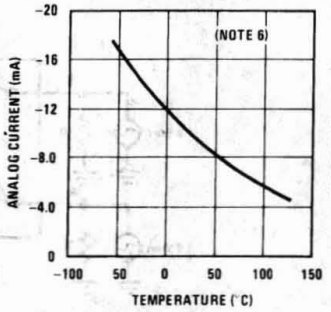
Slew Rate of Analog Voltage Above Which Signal Loading Occurs



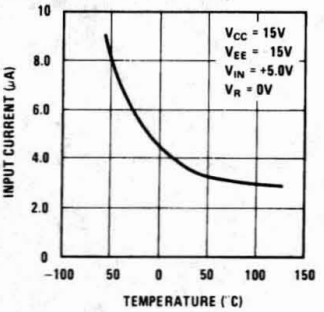
Small Signal Response



Maximum Accurate Analog Current vs Temperature



Logical "1" Input Bias Current



TL/H/5667–5

Application Hints

GENERAL INFORMATION

These devices are monolithic quad JFET analog switches with "ON" resistances which are essentially independent of analog voltage or analog current. The leakage currents are typically less than 1 nA at 25°C in both the "OFF"and "ON" switch states and introduce negligible errors in most applications. Each switch is controlled by minimum TTL logic levels at its input and is designed to turn "OFF" faster than it will turn "ON." This prevents two analog sources from being transiently connected together during switching. The switches were designed for applications which require break-before-make action, no analog current loss, medium speed switching times and moderate analog currents.

Because these analog switches are JFET rather than CMOS, they do not require special handling.

LOGIC INPUTS

The logic input (IN), of each switch, is referenced to two forward diode drops (1.4V at 25°C) from the reference supply (V_R) which makes it compatible with DTL, RTL, and TTL logic families. For normal operation, the logic "0" voltage can range from 0.8V to -4.0V with respect to V_R and the logic "1" voltage can range from 2.0V to 6.0V with respect to V_R, provided V_{IN} is not greater than ($V_{CC}-2.5$V). If the input voltage is greater than ($V_{CC}-2.5$V), the input current will increase. If the input voltage exceeds 6.0V or -4.0V with respect to V_R, a resistor in series with the input should be used to limit the input current to less than 100μA.

ANALOG VOLTAGE AND CURRENT

Analog Voltage

Each switch has a constant "ON" resistance (R_{ON}) for analog voltages from ($V_{EE}+5$V) to ($V_{CC}-5$V). For analog voltages greater than ($V_{CC}-5$V), the switch will remain ON independent of the logic input voltage. For analog voltages less than ($V_{EE}+5$V), the ON resistance of the switch will increase. Although the switch will not operate normally when the analog voltage is out of the previously mentioned range, the source voltage can go to either ($V_{EE}+36$V) or ($V_{CC}+6$V), whichever is more positive, and can go as negative as V_{EE} without destruction. The drain (D) voltage can also go to either ($V_{EE}+36$V) or ($V_{CC}+6$V), whichever is more positive, and can go as negative as ($V_{CC}-36$V) without destruction.

Analog Current

With the source (S) positive with respect to the drain (D), the R_{ON} is constant for low analog currents, but will increase at higher currents (>5 mA) when the FET enters the saturation region. However, if the drain is positive with respect to the source and a small analog current loss at high analog currents (Note 6) is tolerable, a low R_{ON} can be maintained for analog currents greater than 5 mA at 25°C.

LEAKAGE CURRENTS

The drain and source leakage currents, in both the ON and the OFF states of each switch, are typically less than 1 nA at 25°C and less than 100 nA at 125°C. As shown in the typical curves, these leakage currents are Dependent on power supply voltages, analog voltage, analog current and the source to drain voltage.

DELAY TIMES

The delay time OFF (t_{OFF}) is essentially independent of both the analog voltage and temperature. The delay time ON (t_{ON}) will decrease as either ($V_{CC}-V_A$) decreases or the temperature decreases.

POWER SUPPLIES

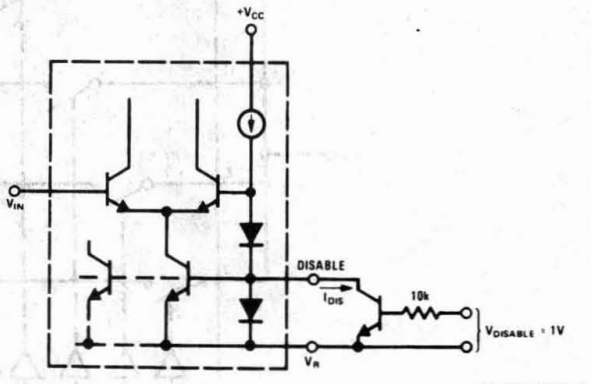
The voltage between the positive supply (V_{CC}) and either the negative supply (V_{EE}) or the reference supply (V_R) can be as much as 36V. To accommodate variations in input logic reference voltages, V_R can range from V_{EE} to ($V_{CC}-4.5$V). Care should be taken to ensure that the power supply leads for the device never become reversed in polarity or that the device is never inadvertantly installed backwards in a test socket. If one of these conditions occurs, the supplies would zener an internal diode to an unlimited current; and result in a destroyed device.

SWITCHING TRANSIENTS

When a switch is turned OFF or ON, transients will appear at the load due to the internal transient voltage at the gate of the switch JFET being coupled to the drain and source by the junction capacitances of the JFET. The magnitude of these transients is dependent on the load. A lower value R_L produces a lower transient voltage. A negative transient occurs during the delay time ON, while a positive transient occurs during the delay time OFF. These transients are relatively small when compared to faster switch families.

DISABLE NODE

This node can be used, as shown in *Figure 5*, to turn all the switches in the unit off independent of logic inputs. Normally, the node floats freely at an internal diode drop ($\approx$0.7V) above V_R. When the external transistor in *Figure 5* is saturated, the node is pulled very close to V_R and the unit is disabled. Typically, the current from the node will be less than 1 mA. This feature is not available on the LF11201 or LF11202 series.

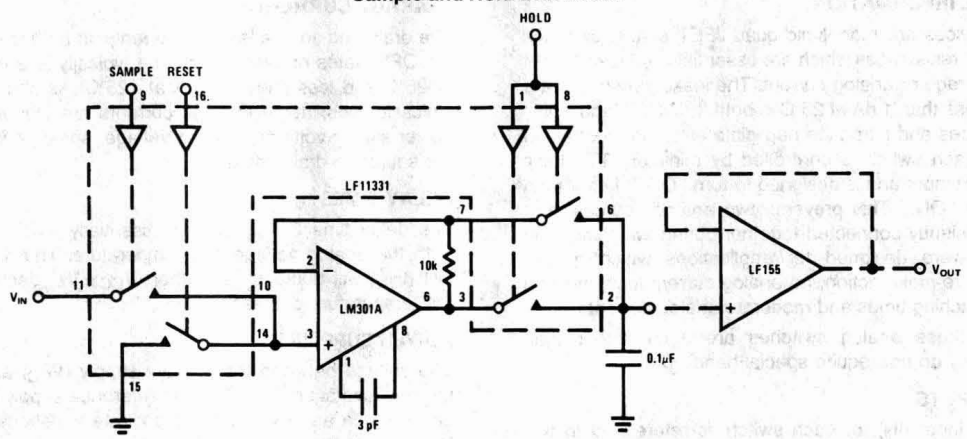


TL/H/5667–6

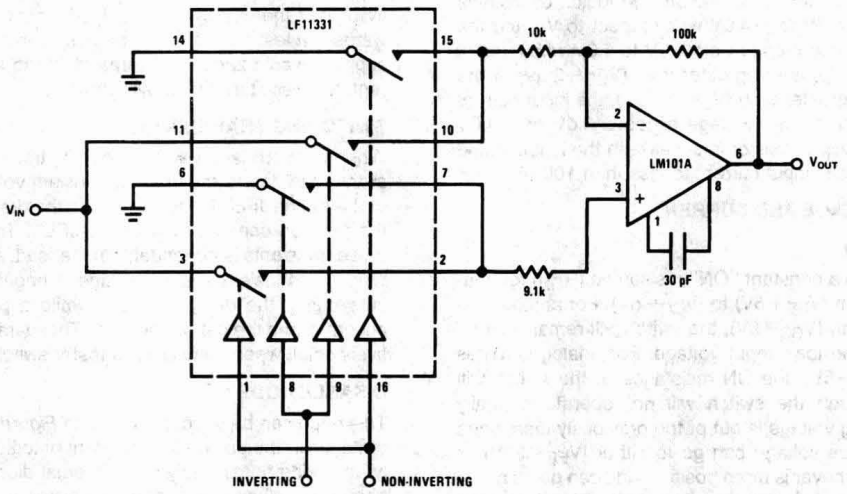
FIGURE 5. Disable Function

Typical Applications

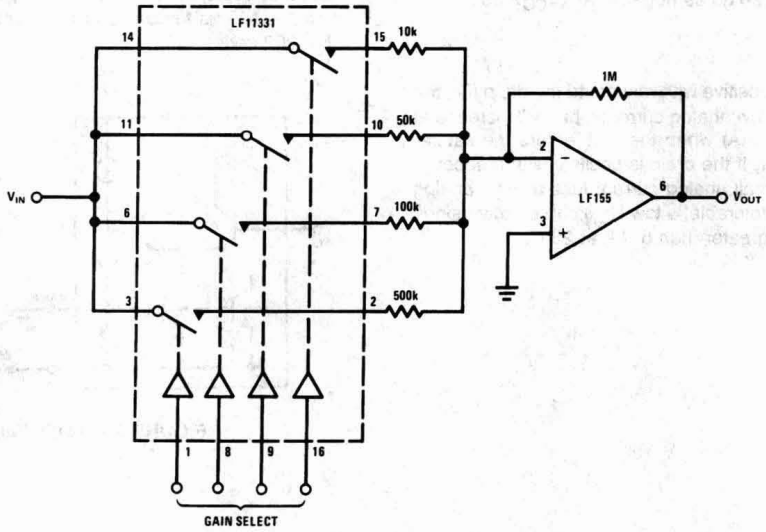
Sample and Hold with Reset



Programmable Inverting Non-Inverting Operational Amplifier



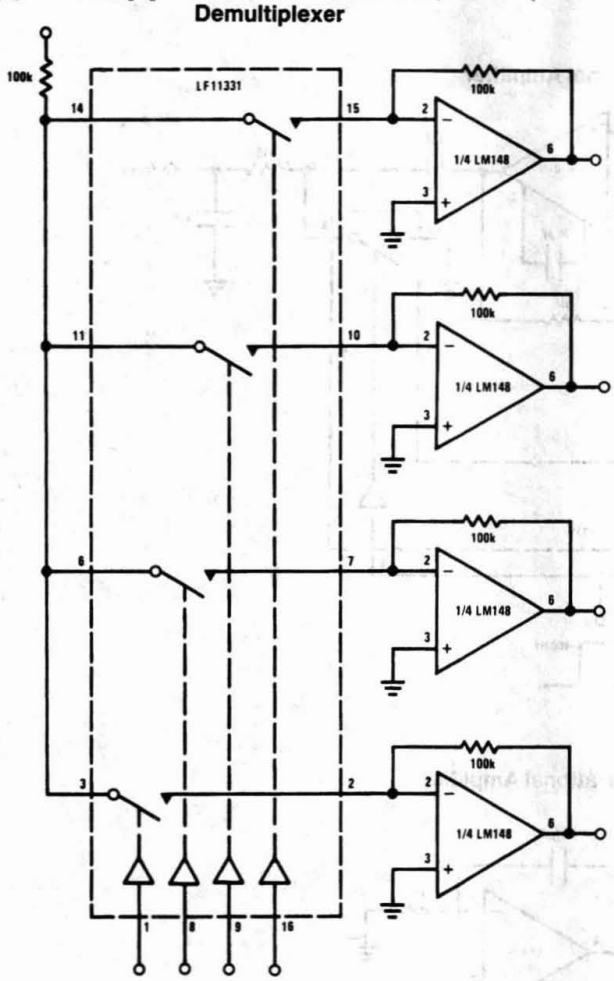
Programmable Gain Operational Amplifier



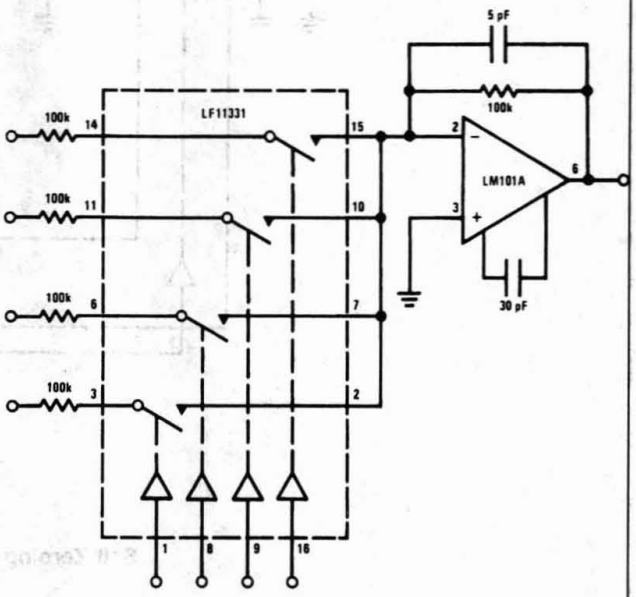
TL/H/5667–7

Typical Applications (Continued)

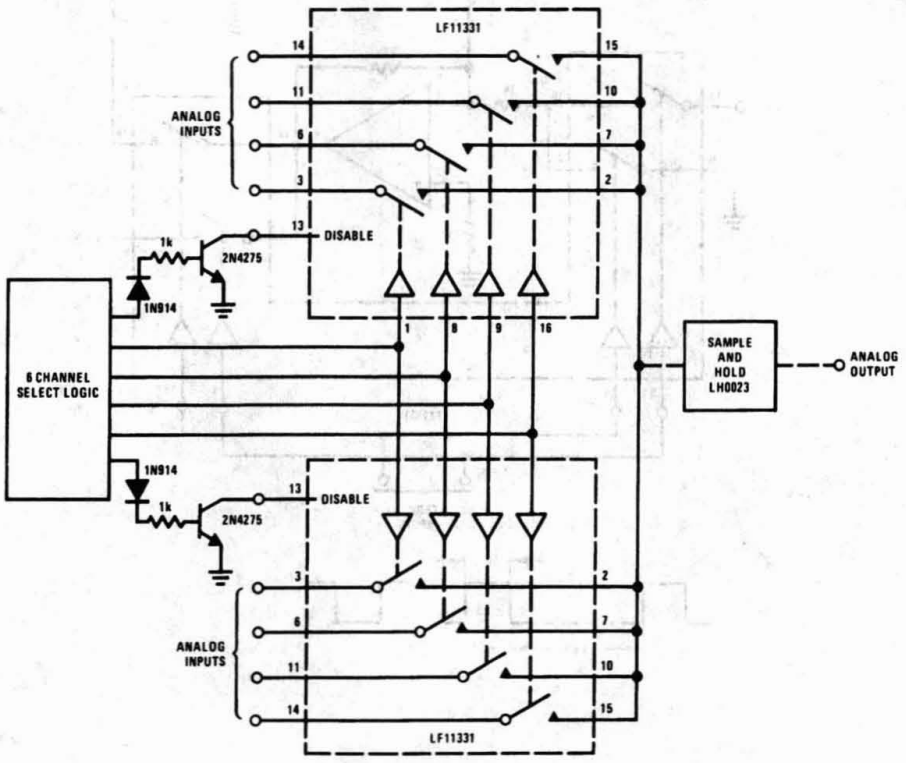
Demultiplexer



Multiplexer/Mixer



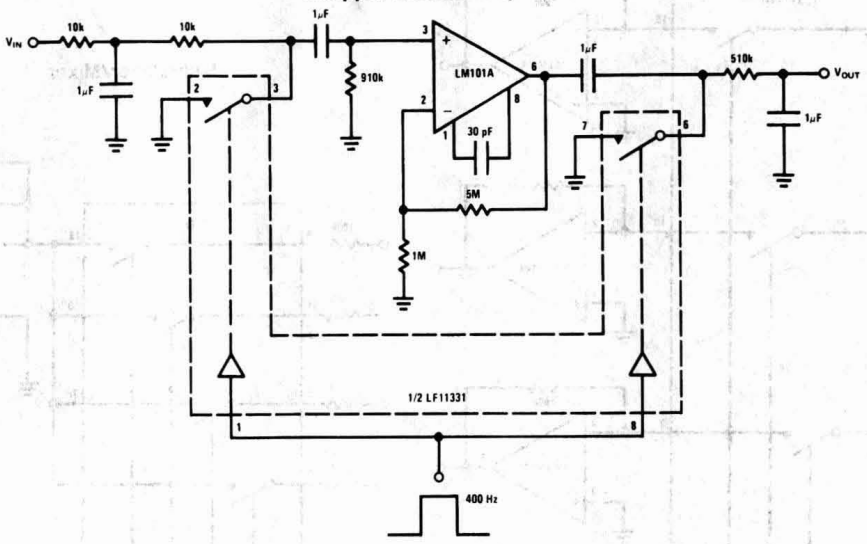
8-Channel Analog Commutator with 6-Channel Select Logic



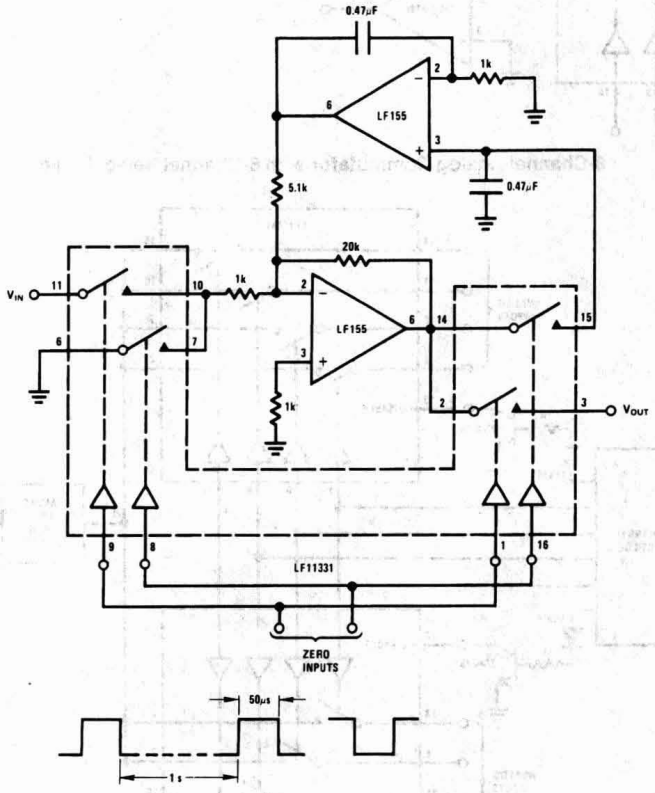
TL/H/5667–8

Typical Applications (Continued)

Chopper Channel Amplifier



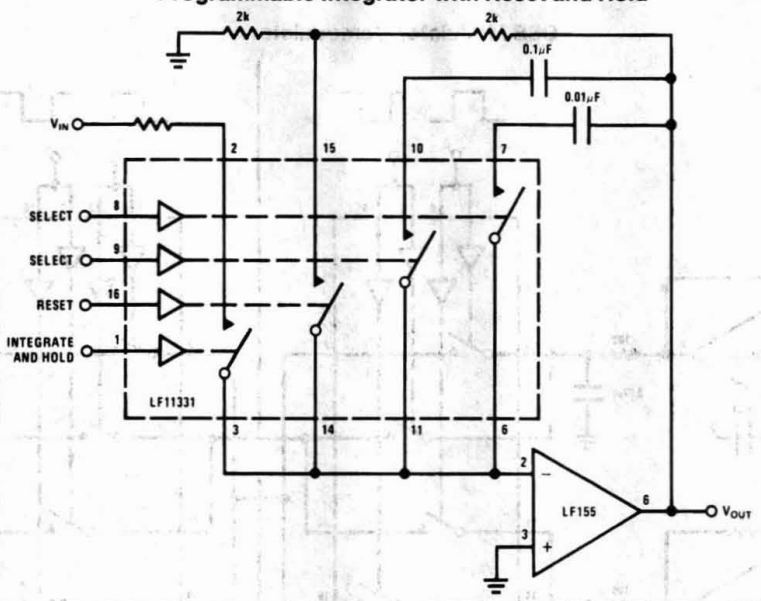
Self-Zeroing Operational Amplifier



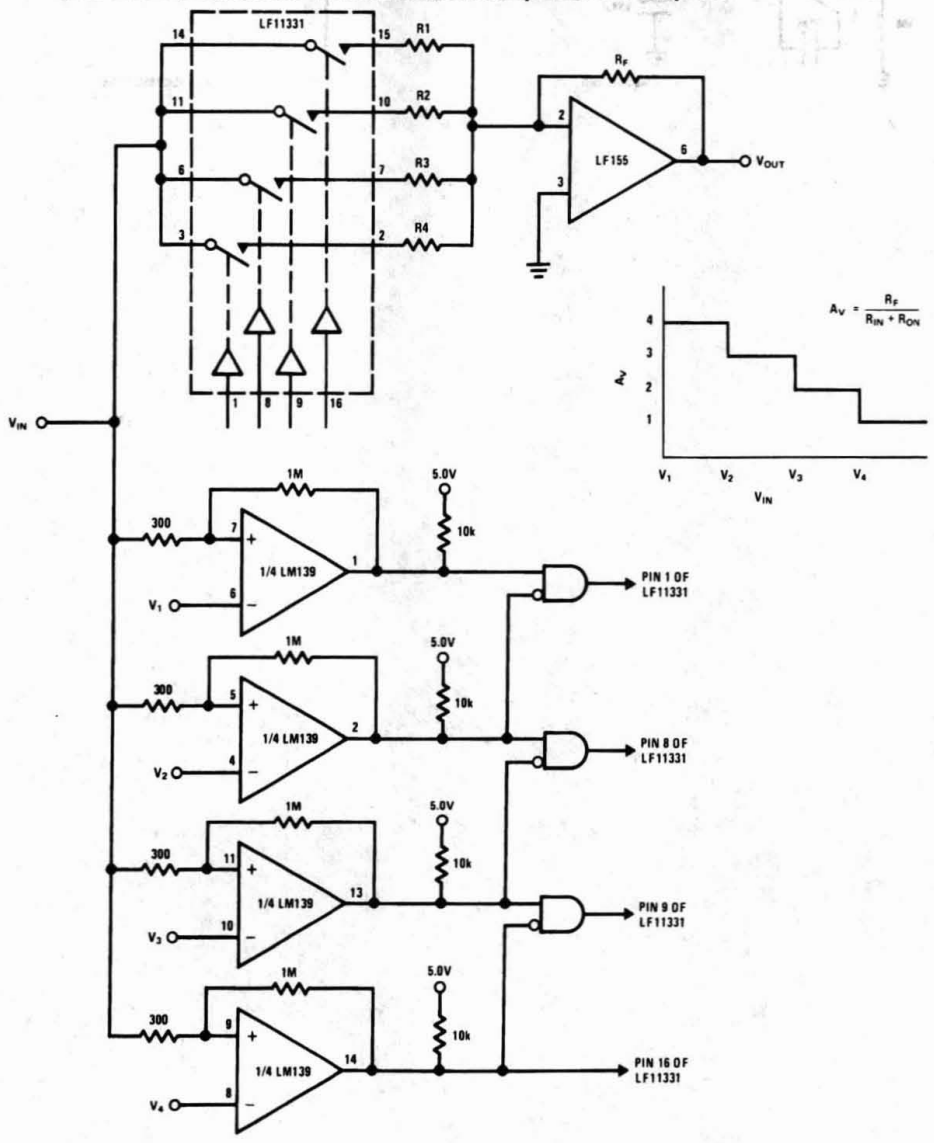
TL/H/5667–9

Typical Applications (Continued)

Programmable Integrator with Reset and Hold



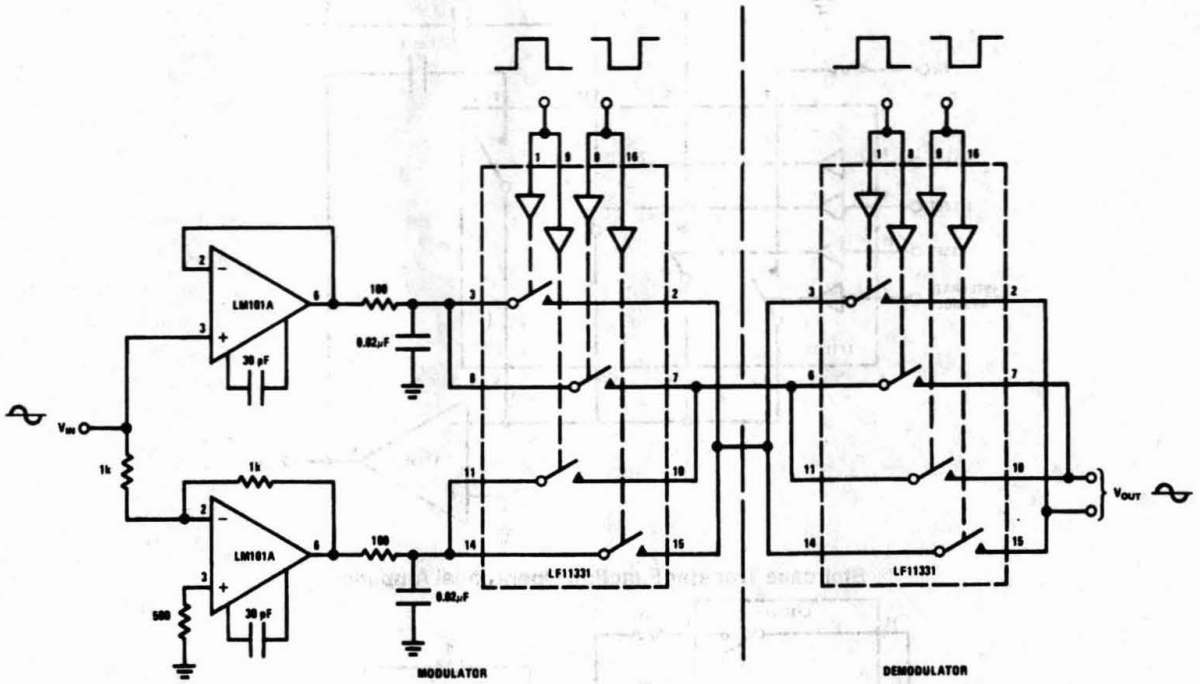
Staircase Transfer Function Operational Amplifier



TL/H/5667–10

Typical Applications (Continued)

DSB Modulator-Demodulator



TL/H/5667–11

National Semiconductor

LF13508 8-Channel Analog Multiplexer
LF13509 4-Channel Differential Analog Multiplexer

General Description

The LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

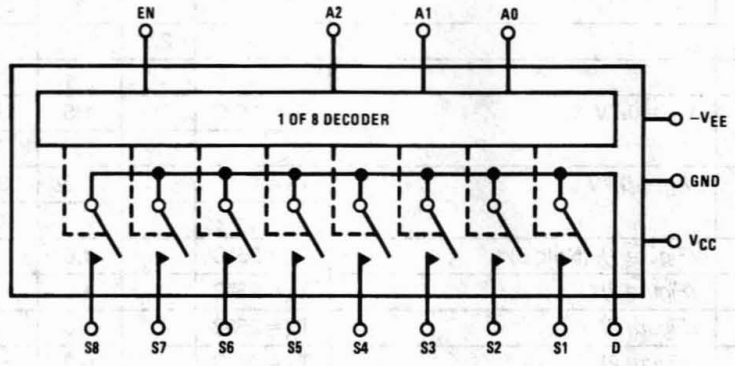
The LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF13508 series and should be used whenever differential analog inputs are required.

Features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: $t_{OFF} = 0.2\ \mu s$; $t_{ON} = 2\ \mu s$ typ
- Lower leakage devices available

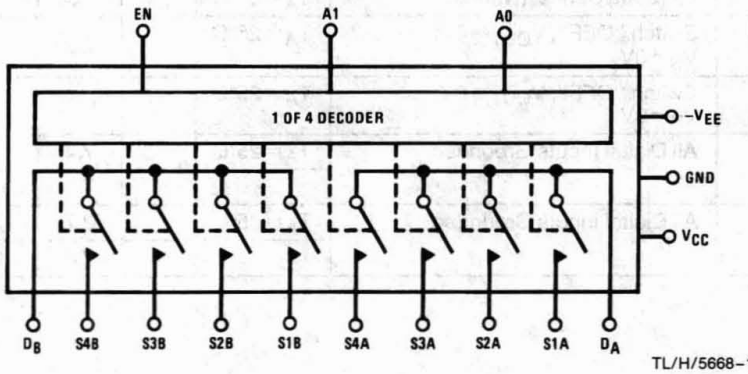
Functional Diagrams and Truth Tables

LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

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8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply − Negative Supply ($V_{CC}-V_{EE}$)	36V
Positive Analog Input Voltage (Note 1)	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}
Negative Digital Input Voltage	−5V
Analog Switch Current	$\|I_S\| < 10$ mA

Power Dissipation (P_D at 25°C) (Notes 2 & 7)		
Molded DIP (N)	P_D	500 mW
Cavity DIP (D)	P_D	900 mW
Small Outline (SO)	P_D	500 mW
Maximum Junction Temperature (T_{jMAX})		100°C
Operating Temperature Range		$0°C \le T_A \le +70°C$
Storage Temperature Range		−65°C to +150°C
Lead Temperature		
D Package (Soldering, 10 seconds)		300°C
N Package (Soldering, 10 seconds)		260°C
Surface Mount Package (SO)		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions		LF13508 LF13509			Units
				Min	Typ	Max	
R_{ON}	"ON" Resistance	$V_{OUT}=0V$, $I_S=100\ \mu A$	$T_A=25°C$		380	650	Ω
					500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \le V_{OUT} \le +10V$, $I_S=100\ \mu A$	$T_A=25°C$		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	$V_{OUT}=0V$, $I_S=100\ \mu A$	$T_A=25°C$		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", $V_S=11$, $V_D=-11$, (Note 4)	$T_A=25°C$			5	nA
					0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", $V_S=11$, $V_D=-11$, (Note 4)	$T_A=25°C$			20	nA
					0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" $V_D=11V$, (Note 4)	$T_A=25°C$			20	nA
					1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7	V
I_{INL}	Digital "0" Input Current	$V_{IN}=0.7V$	$T_A=25°C$		1.5	30	μA
						40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	$V_{EN}=0.7V$	$T_A=25°C$		1.2	30	μA
						40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	$T_A=25°C$		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	$T_A=25°C$		1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	$T_A=25°C$		1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	$T_A=25°C$		0.2		μs
$I_{SO(OFF)}$	"OFF" Isolation	(Note 6)	$T_A=25°C$		−66		dB
CT	Crosstalk	LF13509 Series, (Note 6)	$T_A=25°C$		−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", $V_{OUT}=0V$, $V_S=0V$	$T_A=25°C$		2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", $V_{OUT}=0V$, $V_S=0V$	$T_A=25°C$		11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	$T_A=25°C$		7.4	12	mA
					7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	$T_A=25°C$		2.7	5	mA
					2.8	6	mA

Electrical Characteristics (Continued)

Note 1: If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

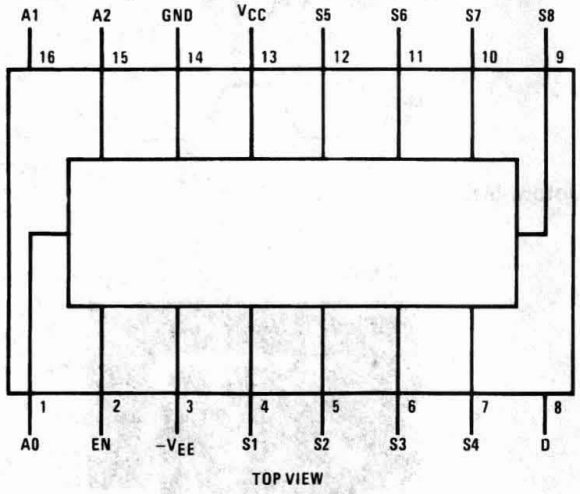
Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L = 200$, $C_L = 7$ pF, $V_S = 3$ Vrms, f = 500 kHz.

Note 7: Thermal Resistance θ_{jA} (Junction to Ambient)

Molded DIP (N)	150°C/W
Cavity DIP (D)	100°C/W

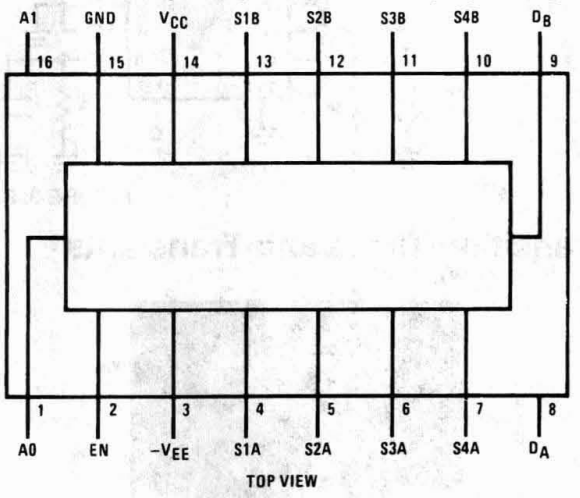
Connection Diagrams

LF13508
Dual-In-Line (N or D) or Small Outline (SO) Packages



Order Number LF13508D
See NS Package Number D16C
Order Number LF13508M
See NS Package Number M16A
Order Number LF13508N
See NS Package Number N16A

LF13509
Dual-In-Line (N or D) or Small Outline (SO) Packages



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Order Number LF13509D
See NS Package Number D16C
Order Number LF13509M
See NS Package Number M16A
Order Number LF13509N
See NS Package Number N16A

AC Test Circuits and Switching Time Waveforms

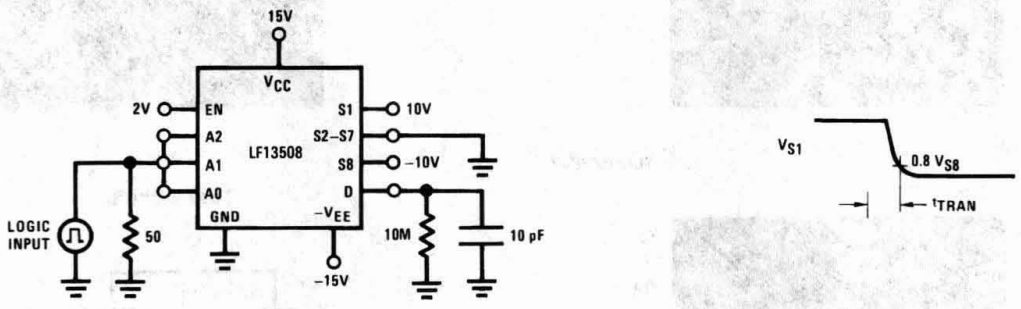

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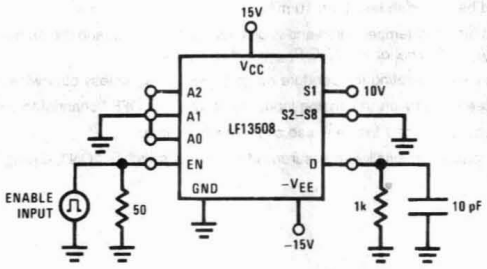
FIGURE 1. Transition Time

AC Test Circuit and Switching Time Waveforms (Continued)



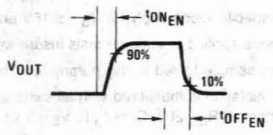
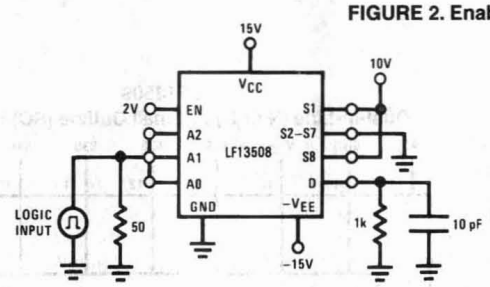


FIGURE 2. Enable Times



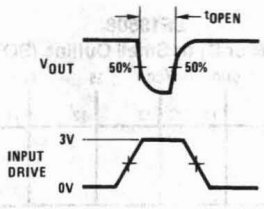


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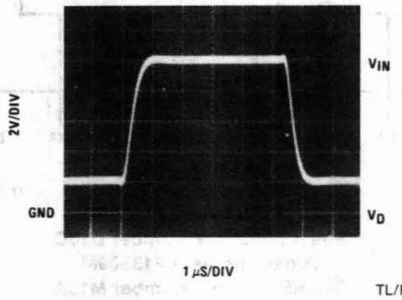
FIGURE 3. Break-Before-Make

Transition Times and Transients

V_A = 10V



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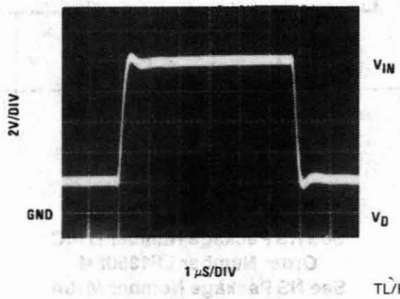
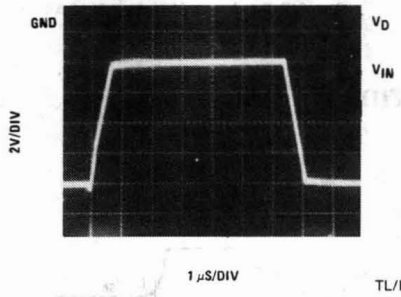
V_A = 5V



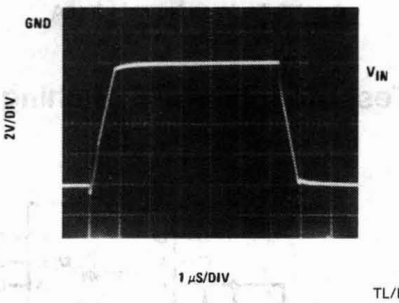
TL/H/5668–6

V_A = 0V



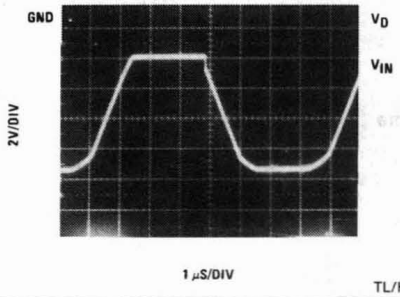
TL/H/5668–7

V_A = –5V



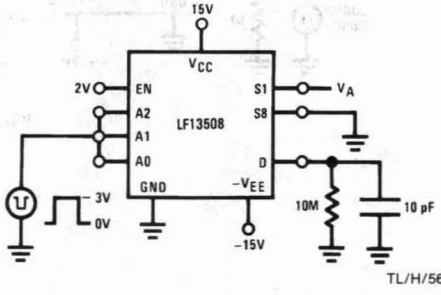
TL/H/5668–8

V_A = –10V



TL/H/5668–9

Test Circuit



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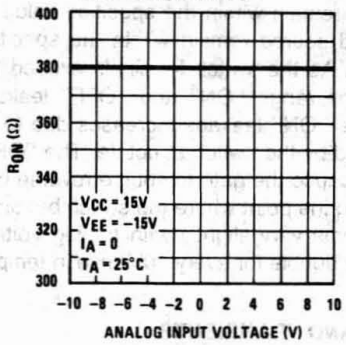
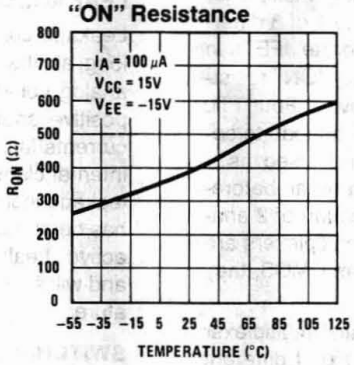
Typical Performance Characteristics

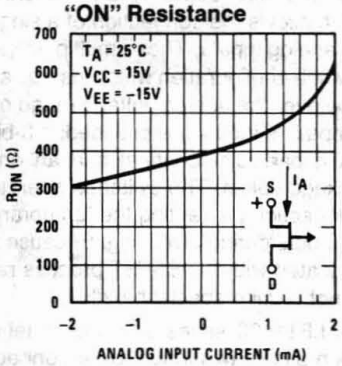
"ON" Resistance



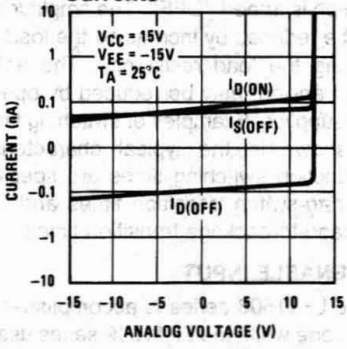
"ON" Resistance



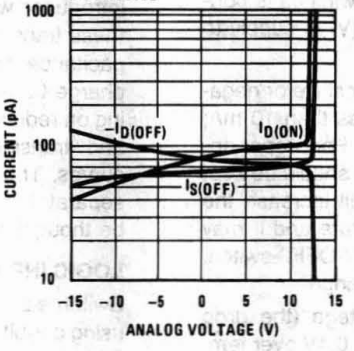
"ON" Resistance



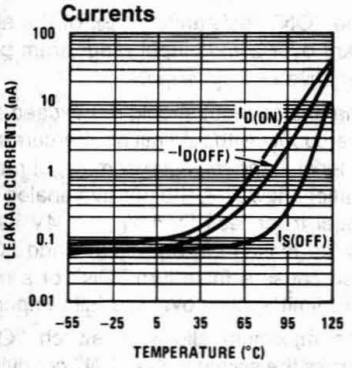
Switch Leakage Currents



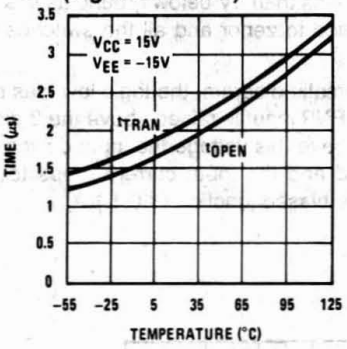
Switch Leakage Currents



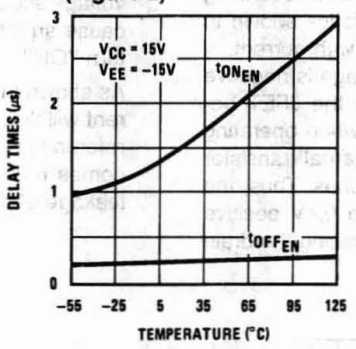
Switch Leakage Currents



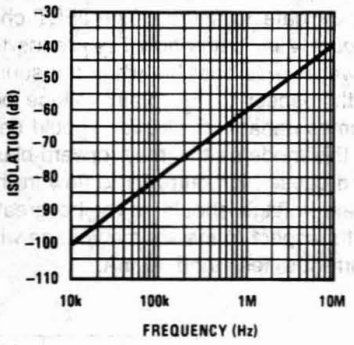
Switching Times (Figures 1 and 3)



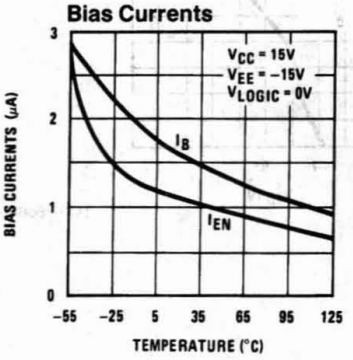
Enable Delay Times (Figure 2)



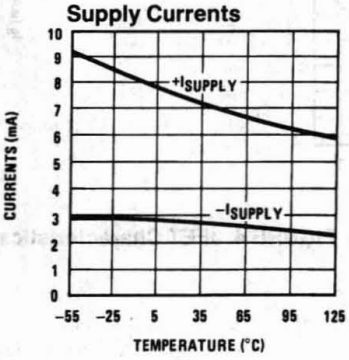
"OFF" Isolation and Crosstalk



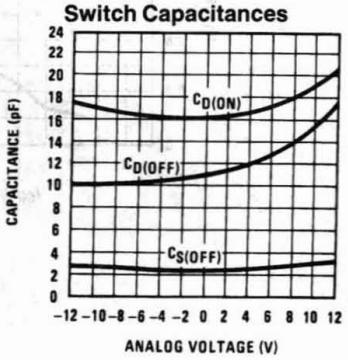
Bias Currents



Supply Currents



Switch Capacitances



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8

Application Hints

The LF11508 series is an 8-channel analog multiplexer which allows the connection of a single load to 1 of 8 different analog inputs. These multiplexers incorporate JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is $\pm 0.4V$ over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect to the source voltage without limiting the drain current to less than 10 mA.

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE}+36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference ($\approx 2.1V$). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction ($<0.1\ \mu A$).

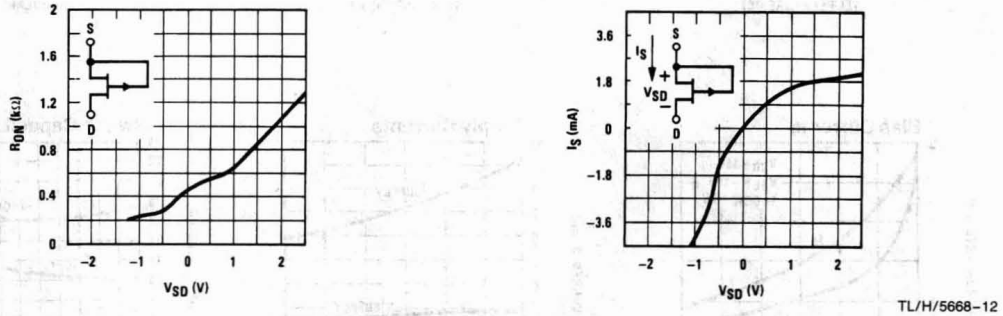

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FIGURE 4. JFET Characteristics

Typical Applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multi-channel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6).*

   a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

$$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})} \text{ where:}$$

   R_{IN} = following stage input impedance

   ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

   Example: Let R_{ON} = 450 Ω, ΔR_{ON} = 0, R_S = 0, T_A = 25°C and allowable E = 0.01% which is equivalent to 1/2 LSB in a 12-bit system:

$$R_{IN}\Big|_{min} = \frac{R_{ON}(100 - E)}{E} = 4.5\ M\Omega$$

   Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

   b. Multiplexer settling time (t_s):

   $t_{s(ON)}$: is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

   C_S *(Figure 6):* MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	t_s(ON) TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$$t = C_S (R_{ON} + R_S) \parallel R_{IN}$$

   $t_{s(OFF)}$: is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case of doubling of the $t_{s(ON)}$.

2. Sample and Hold Influence on System Accuracy

   The sample and hold, if used, also introduces errors into the system accuracy due to:
   - Offset voltage of sample and hold
   - Droop rate in the Hold mode
   - T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
   - Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
   - Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

   For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy

   The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

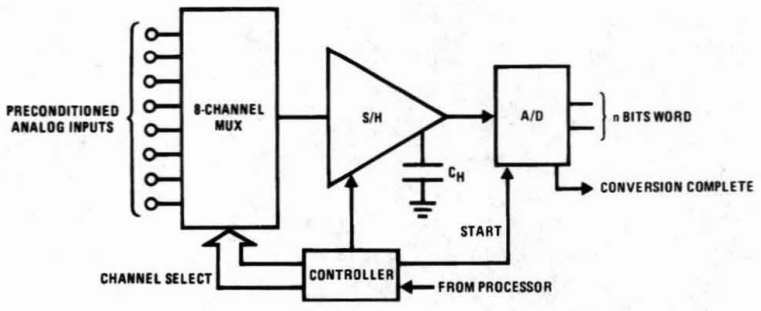

FIGURE 5. Random-Addressed, Multiplexed DAU

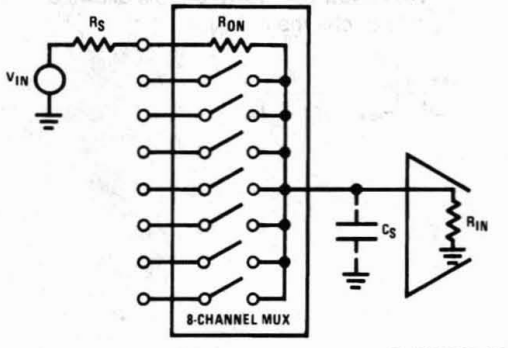

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FIGURE 6. 8-Channel MUX

8

Typical Applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ LSB}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let $T_C = 40\ \mu s$ (MM4357), $V_{FS} = 10V$ and n = 8.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$\text{Th. R}\Big|_{max} = \frac{1}{8(T_C + T_{MUX})} = 3k\ \text{samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})max}{\pi\ Vp\text{-}p}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

The system speed can be improved by using the S/H shown in *Figure 5.* This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: $T_C = 40\ \mu s$, $T_A = 0.5\ \mu s$, n = 8: $T_C/T_A = 80$

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$\text{Th. R}\Big|_{max} = \frac{1}{8(T_A + Taq + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

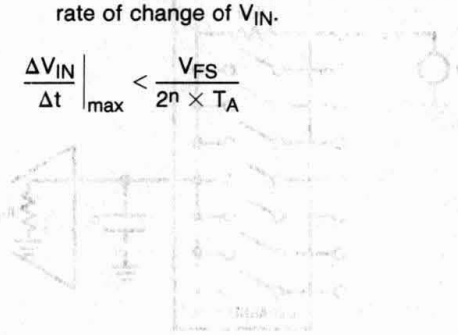
The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

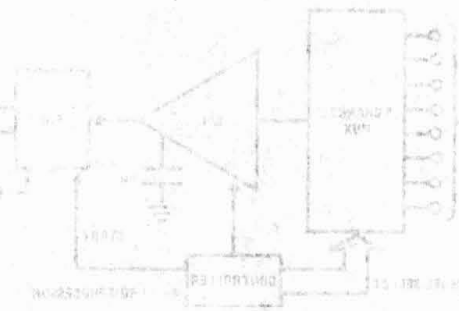
$$\frac{\Delta V_{IN}}{\Delta t} \le \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5mV/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$\text{Th. R}\Big|_{max} = \frac{1}{8(5 + 40)10^{-6}} = 2800\ \text{samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8.*





Typical Applications (Continued)

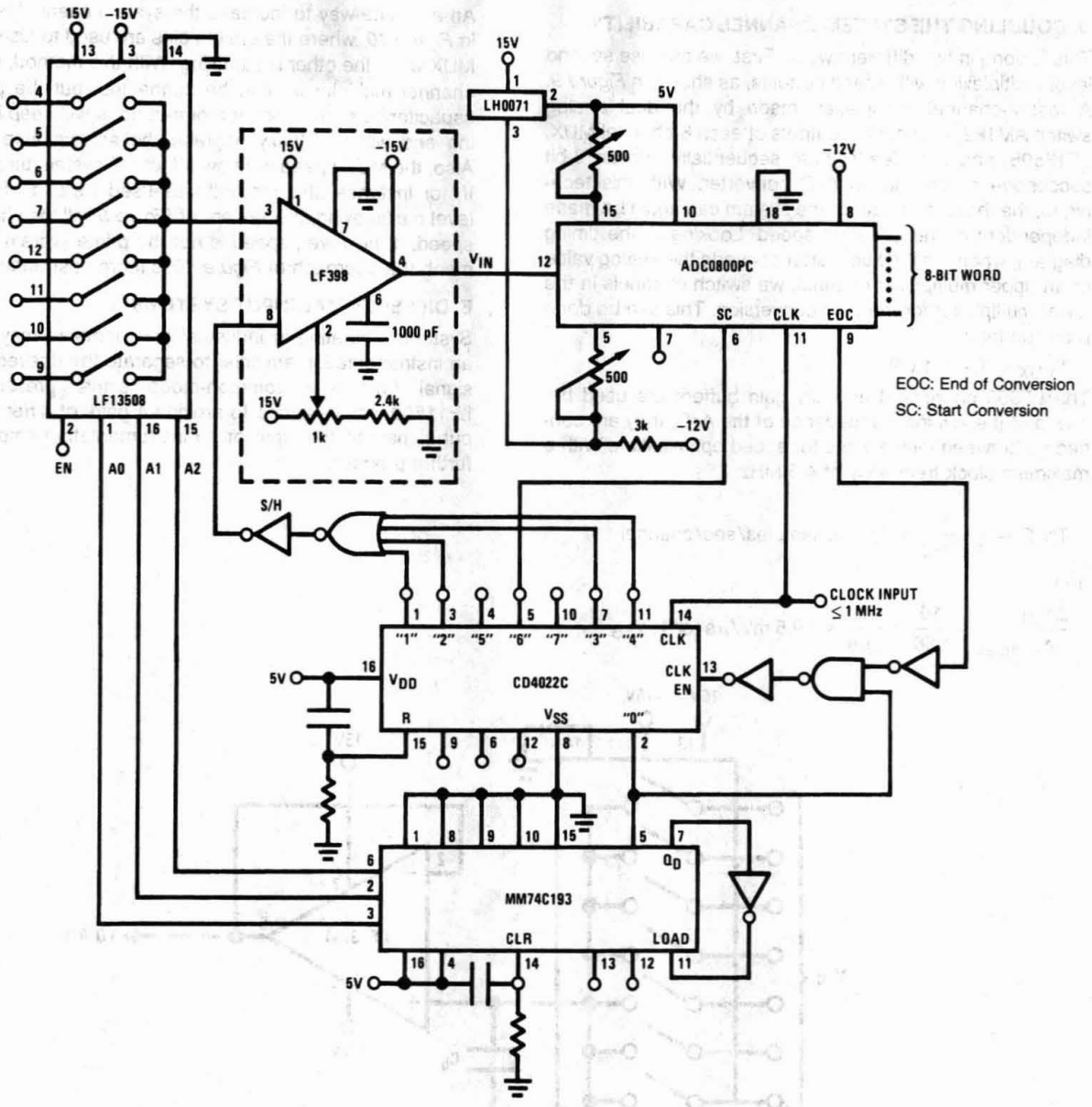
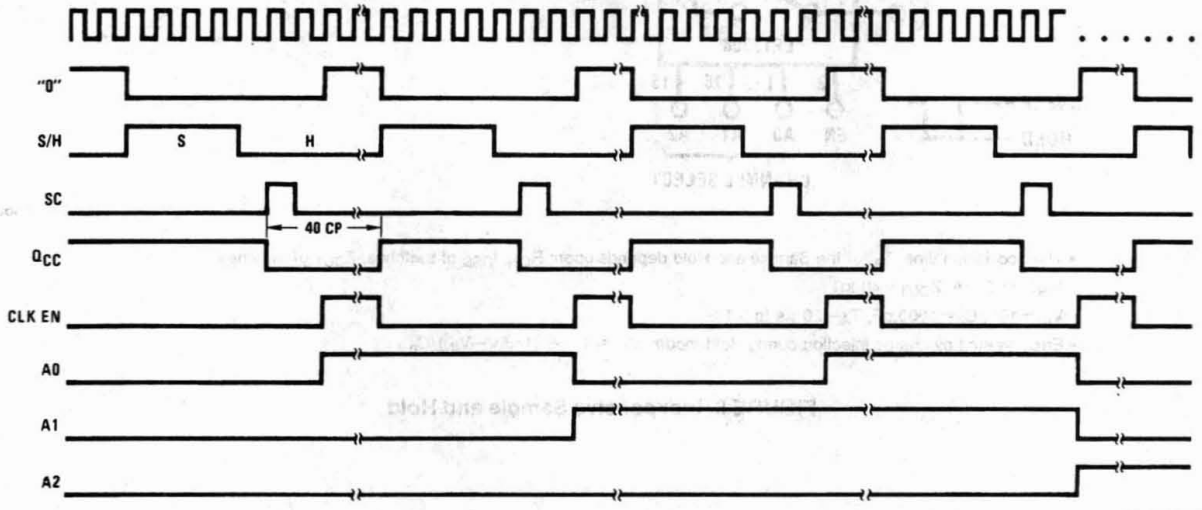


FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold



TL/H/5668–14

FIGURE 7b. Timing Diagram

Typical Applications (Continued)

D. DOUBLING THE SYSTEM CHANNEL CAPABILITY

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9.* A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\ CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. R} = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

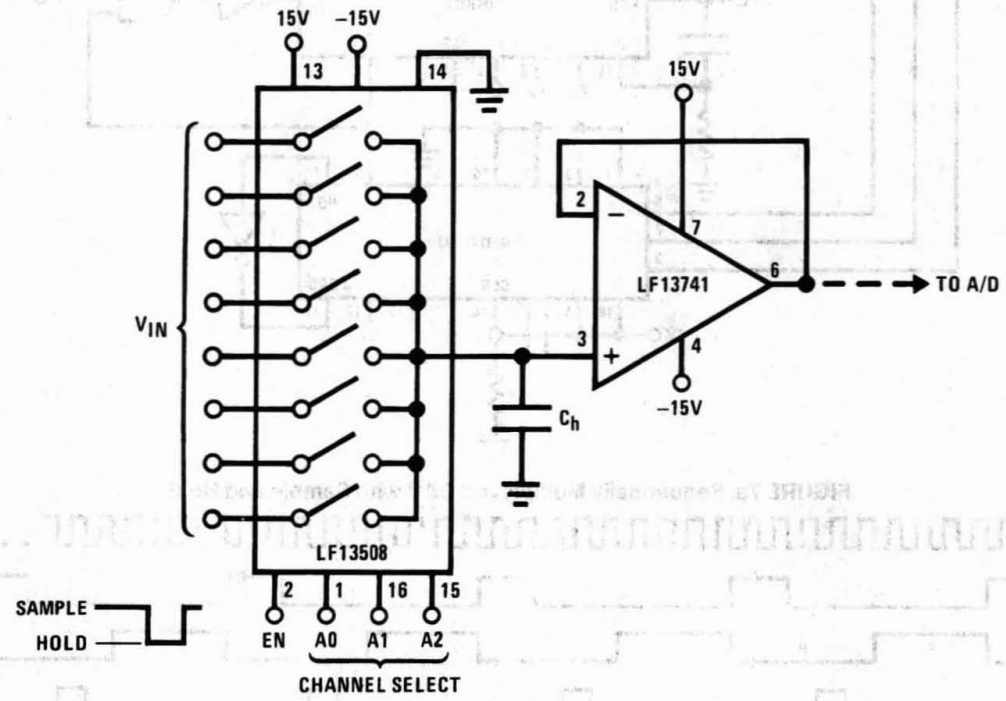
and

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\mu s} = 19.5\ mV/\mu s \text{ for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10,* where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_{s(ON)}$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process.



TL/H/5668–15

- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \cong 1.5$ mA, $Z_{OUT} = 40\ k\Omega$
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20\ \mu s$ to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \cong 10\ pF\ (14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

Typical Applications (Continued)

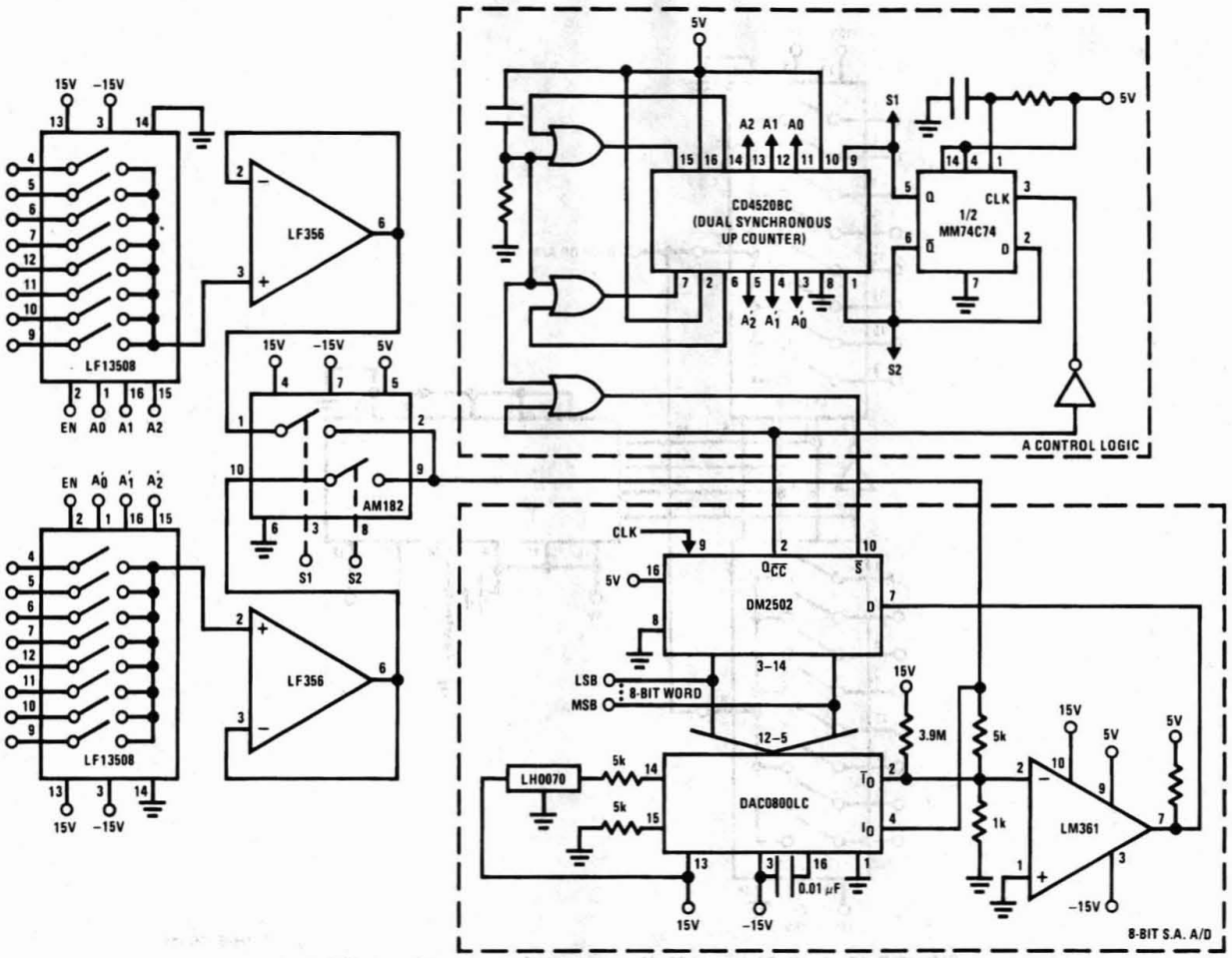


FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing

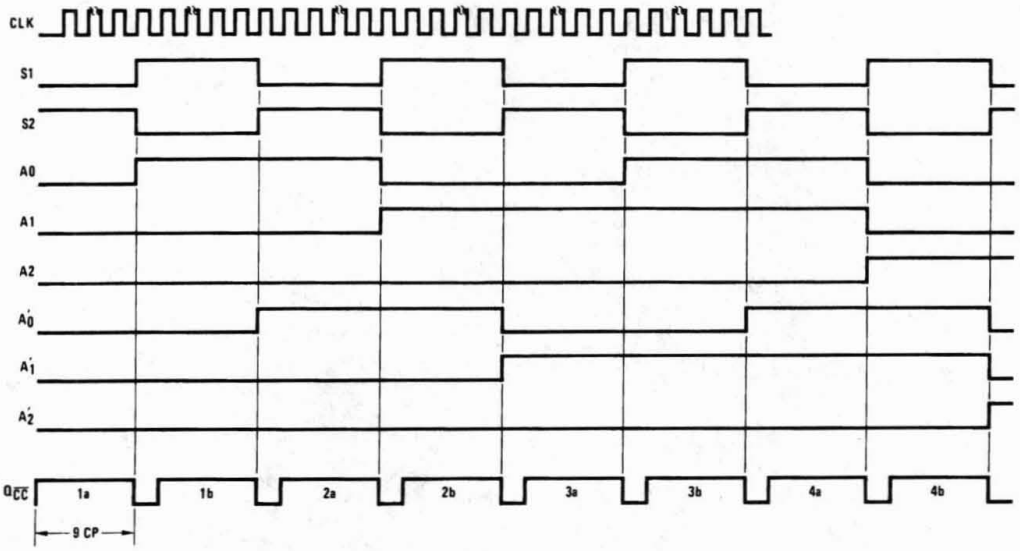


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FIGURE 9b. Timing Diagram

Typical Applications (Continued)

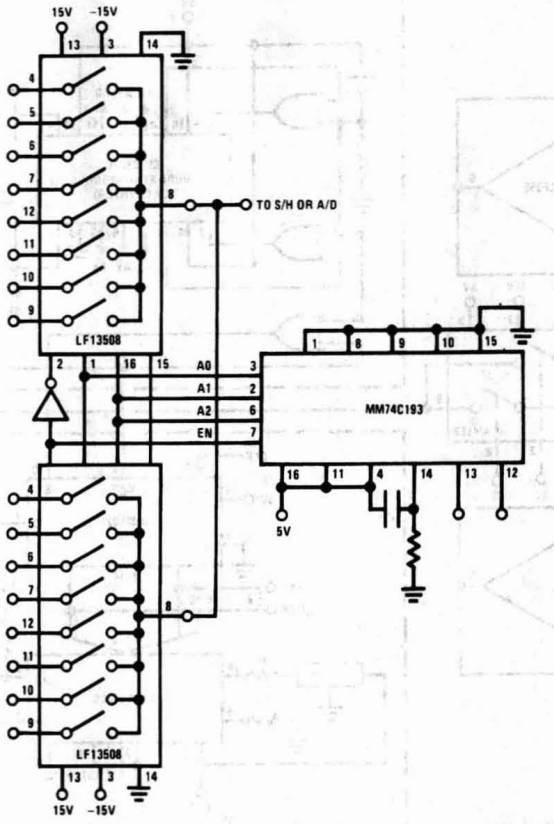

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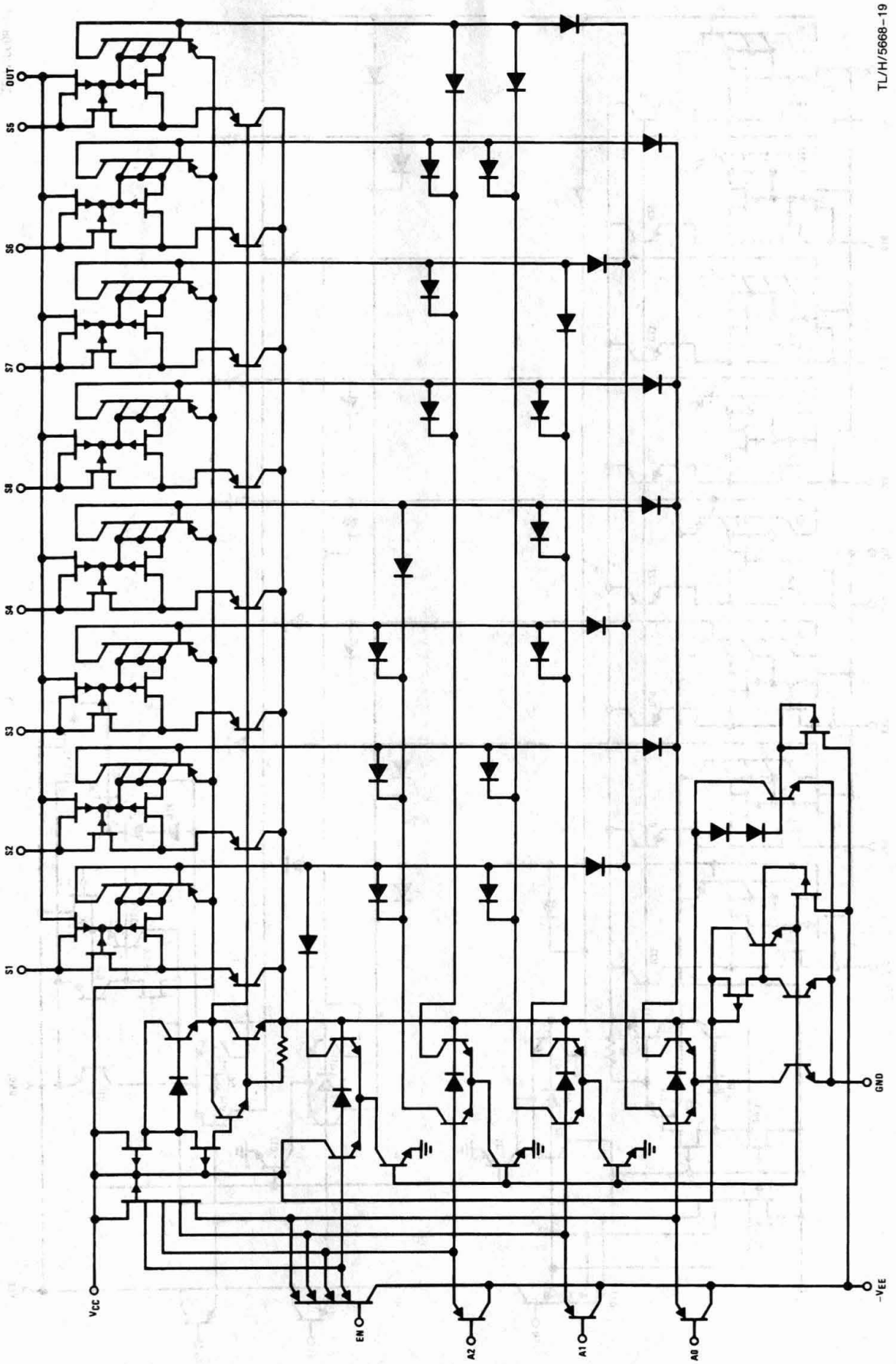
FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing

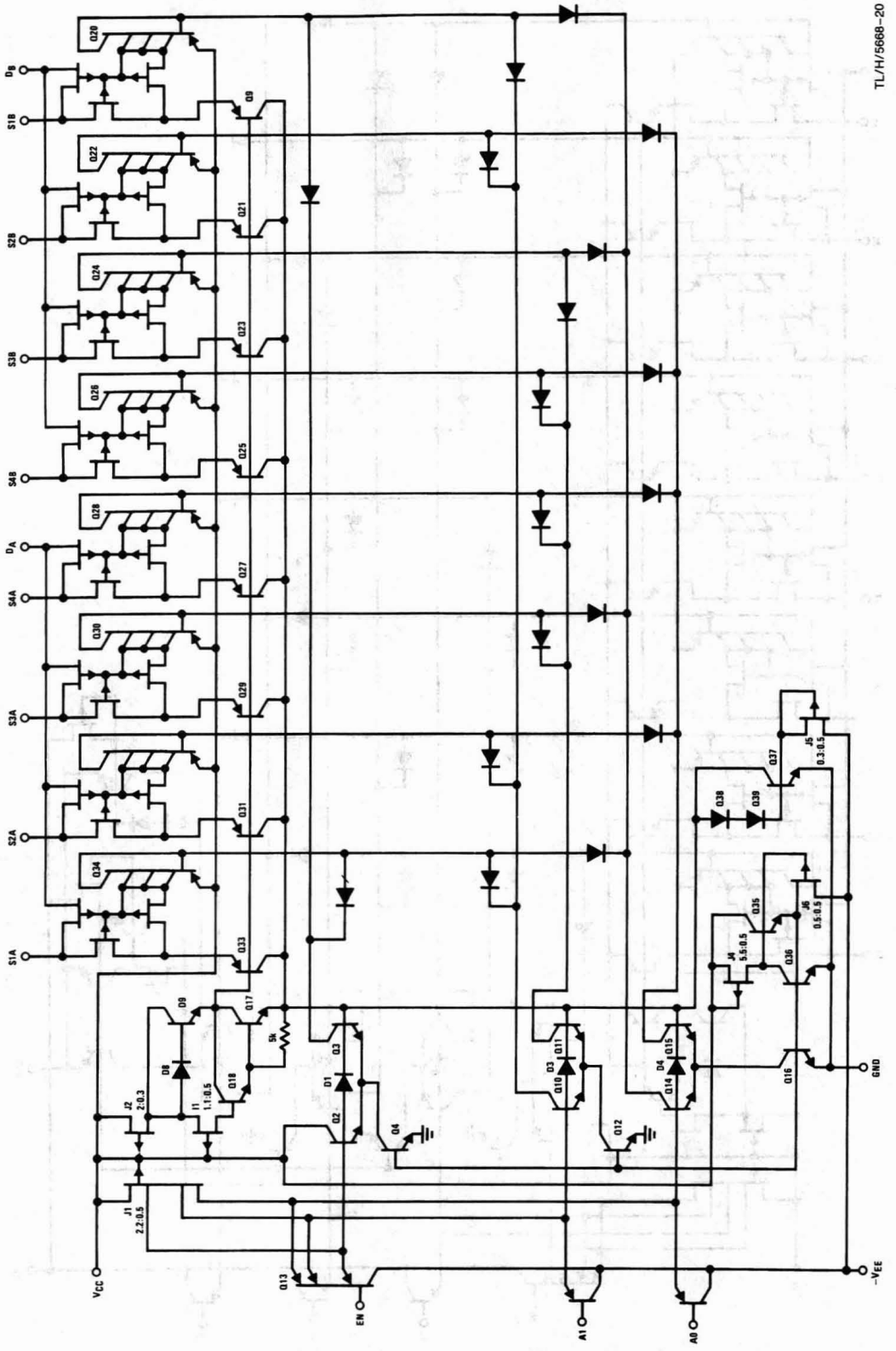
Schematic Diagrams

LF13508



Schematic Diagrams (Continued)

LF13509



Section 9

Surface Mount

Section 9 Contents

Packing Considerations (Methods, Materials and Recycling) 9-3
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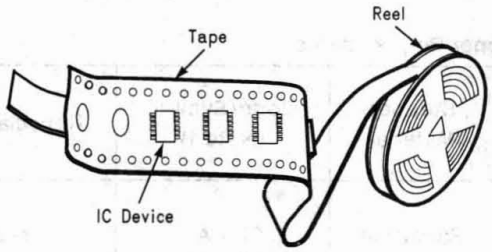
Recommended Soldering Profiles—Surface Mount 9-23
AN-450 Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability 9-24
Land Pattern Recommendations 9-35

Packing Considerations (Methods, Materials and Recycling)

Transport Media

All NSC devices are prepared, inspected and packed to insure proper physical support and to protect during transport and shipment. All assembled devices are packed in one or more of the following container forms—immediate containers, intermediate containers and outer/shipping containers. An example of each container form is illustrated below.

IMMEDIATE CONTAINER



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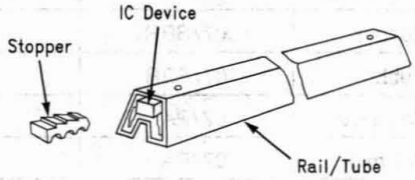

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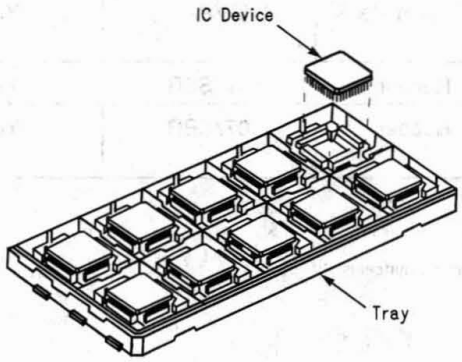

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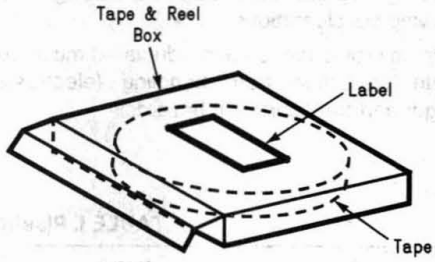
INTERMEDIATE CONTAINER



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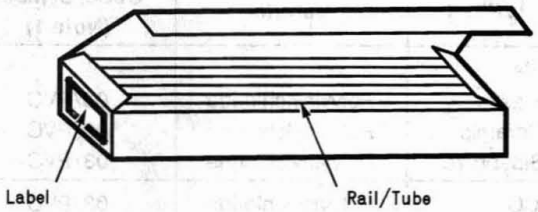

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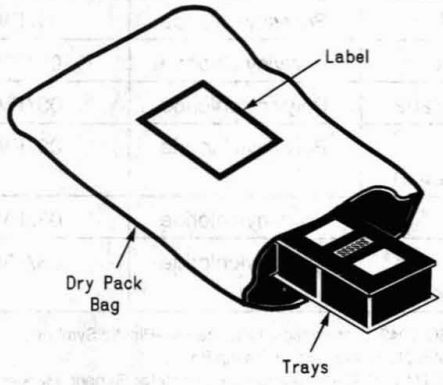

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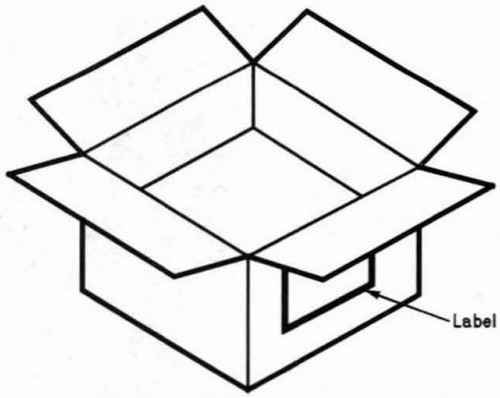
OUTER/SHIPPING CONTAINER



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Methods of immediate carrier packing include insertion of components into molded trays and rails/tubes, mounting of components onto tape and reel or placement in corrugated cartons. The immediate containers are then packed into intermediate containers (bags or boxes) which specify quantities of trays, rails/tubes or tape and reels. Outer/shipping containers are then filled or partially filled with intermediate containers to meet order quantity requirements and to further insure protection from transportation hazards. Additional dunnage filler material is required to fill voids within the intermediate and outer/shipping containers.

General Packing Requirements

NSC packing methods and materials are designed based on the following considerations:

— Optimum protection to the products—it must provide adequate protection from handling (electrostatic discharge) and transportation hazards;

— Ease of handling—it should be easy to assemble, load and unload products in and from it; and

— Impacts to the environment—it shall be reusable and recyclable.

Levels of Product Packing

IMMEDIATE CONTAINER

The first level of product packing is the immediate container. The immediate container type varies with the product or package being packed. In addition, the materials used in the immediate container depend on the fragility, size and profile of the product. The four types of immediate containers used by NSC are rails/tubes, trays, tape and reel, and corrugated and chipboard containers.

Rails/tubes are generally made of acrylic or polyvinyl chloride (PVC) plastics. The electrical characteristics of the material are altered by either intrinsically adding carbon fillers, and/or topically coating it with antistatic solution. Refer to Table I for rail/tube material and recyclabillty information.

TABLE I. Plastic Rail/Tube and Stopper Requirements

Package Type	Rail		Type	Stopper Material	Code/Symbol (Note 1)	Recyclability
	Material	Code/Symbol (Note 1)				
DIP's						
Plastic	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
Ceramic	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
Sidebraze	Polyvinylchloride	03/PVC	Pin	Polyamide	07/PA	Yes
PLCC	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
TapePak	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
Flatpack	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
Cerpack	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
TO-220/202	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
TO-5/8 (in Carrier)	Polyvinylchloride	03/PVC	Pin	Polymide	07/PA	Yes
SOP	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes
LCC 18L–44L	Polyvinylchloride	03/PVC	Plug	Rubber	07/SBR	Yes

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Molded injection and vacuum formed trays can be either conductive or static dissipative. Molded injection trays are classified as either low-temperature or high-temperature depending on the material type. Vacuum formed trays are only used in ambient room temperature conditions. Refer to Table II for tray material and recyclability information.

TABLE II. Tray Requirements

Package Type	Class	Material	Tray		Binding Type
			Recyclability (Note 1)	Code/Symbol (Note 1)	
PQFP (All)	High Temperature	Polyethersulfone	Yes	07/PES	Wire Tie or Nylon Strap
	Low Temperature	Acrylonitrilebutadiene Styrene	Yes	07/ABS	Wire Tie or Nylon Strap
PGA, LDCC CERQUADs and LCC (48 leads–125 leads)	Low Temperature Only	ABS/PVC	Yes	07/ABS-PVC	Wire Tie
PPGA	Low Temperature Only	Polyarylsulfone	Yes	07/PAS	Wire Tie

Tape and reel is a multi-part immediate container system. The reel is made of either polystyrene (PS) material coated with antistatic solution or chipboard. The embossed or cavity tape is made of either PVC or PS material. The cover tape is made of polyester (PET) and polyethylene (PE) materials. Refer to Table III for tape and reel material and recyclability Information.

TABLE III. Tape and Reel Requirements

Package Type	Reel		Cover Type		Carrier Tape		Recyclability (Note 1)
	Material	Code/ Symbol (Note 1)	Material	Code/ Symbol (Note 1)	Material	Code/ Symbol (Note 1)	
TO-92	Chipboard	Resy	N/A		Paper Tape		Yes
SOP-23	Polystyrene Chipboard	06/PS Resy	Polystyrene	06/PS	PVC	03/PVC	Yes
SOP, SSOP and PLCC	Polystyrene Polyethylene	06/PS	Polyester	07/PET-PE	PVC	03/PVC	Yes

Note 1: 150 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Corrugated containers are generally constructed with fibreboard facings and a fluted corrugated medium in between the facings. Chipboard containers are comprised of just one fibreboard facing. Facings and corrugated medium are kraft (brown) fibreboard, and generally single wall construction. Refer to Table IV for material and recyclability information.

TABLE IV. Fibreboard Container Requirements

Package Type	Pack Method		Container Type		Recyclability
	Material	Code/ Symbol (Note 1)	Immediate (IMM) Intermediate (INT) Outer or Shipping (SHP)		
TO-92/18, TO-46/5, TO-39, 220, TO-202/126, TO-237	Corrugated (E070 BOX)	Resy	IMM		Yes
All Products	Corrguated	Resy	INT and SHIP		Yes
All Products	3-Ply Paper (Padpak)	Resy	Dunnage		Yes
All Products PLCC	Plastic Bubble Sheet	04/PE	Dunnage		Yes

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D1972–91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

INTERMEDIATE CONTAINERS

The second level of product packing is the intermediate container. Three types on intermediate containers are used by NSC. They are plastic bags, moisture barrier bags and corrugated cartons/boxes.

Two types of plastic bags are used and usage of each type depends on the product or package being packed. Conductive bags are made of polyvinylchloride plastic material. The electrical characteristics of the bag are altered by adding carbon fillers which make the bag black (opaque) in color. Conductive bags are used on products or packages that are packed in static dissipative (SD) rails/tubes. Static shielding bags are made of two layers of SD polyethylene sheets with a metallized film separating the sheets. Refer to Table V for material and recyclability information.

Moisture barrier bags are used on rail/tube, tape and reel, and tray packs for moisture sensitive products. NSC uses National Metallizing's Stratoguard™ 4.6.

TABLE V. Conductive and Static Shielding Bag Requirements

Package Type	Container Type	Material Type	Mat'l and Symbol (Note 1)	Mat'l Recyclability
All Prod. in Rails	Conductive Bag	Polyethlene	04/PE	Yes
TO-92/81, TO-46/5, TO-39/220, TO-202/126, TO-3/237	Static Shielding Bag	Polyethlene Alum. Laminant	N/A	No

TABLE VI. Drypack Bag Requirements

Package Type	Container Type	Material Type	Mat'l and Symbol (Note 1)	Mat'l Recyclability
TapePak PLCC (52-84L) PQFP	Drypack Bag	Stratoguard™ 4.6	N/A	No

Note 1: ISO 1043-1 International Standards—Plastic Symbols.
SAE J1344 Marking of Plastic Parts.
ASTM D1972-91 Standard Practice for Generic Marking of Plastic Products.
DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials

Corrugated cartons/boxes are generally constructed with fibreboard facings and a fluted corrugated medium in between the facings. Facings and corrugated medium are kraft (brown) fibreboards, and are generally of single wall construction. Carton style varies with the product that it will contain. For example, packing of a rail/tube will require the use of a carton with a roll end from lock (REFL) design. Other products generally use the regular slotted container (RSC) box. Refer to Table IV for material and recyclability information.

OUTER/SHIPPING CONTAINERS

The third level of product packing is the outer/shipping container. The outer/shipping containers use by NSC are similar to the corrugated containers used for immediate and intermediate packaging, but are heavier in facing thickness. The style generally used is the regular slotted container (RSC) box and can be single, double or triple wall, depending on the total weight of products being transported or shipped. Refer to Table IV for material and recyclability information.

OTHER PACKING MATERIALS

Additional dunnage and void filler materials are required to fill voids within the intermediate and outer/shipping containers. Two types of dunnage/filler material are Padpack and bubble pack. Padpak is a machine processed, 3-ply kraft paper sheet dunnage system. Refer to Table IV for material and recyclability information.

Bubble pack is made of polyethylene plastic sheets with air pockets trapped in between the plastic layers and can be either static dissipative or conductive. Refer to Table IV for material and recyclability information.

Immediate Container Pack Methods

The following table identifies the primary immediate container pack method for all hermetic and plastic packages offered by National Semiconductor. A secondary immediate container pack method is identified where applicable.

Immediate Packing Method for Ceramic Packages

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Sidebrazed Dual-In-Line Package (SB)	D08C	Rail/Tube	35		
	D14D	Rail/Tube	25		
	D16C	Rail/Tube	20		
	D18A	Rail/Tube	20		
	D20A	Rail/Tube	18		
	D20B	Rail/Tube	18		
	D24C	Rail/Tube	15		
	D24H	Rail/Tube	15		
	D24K	Rail/Tube	15		
	D28D	Rail/Tube	13		
	D28G	Rail/Tube	13		
	D28H	Rail/Tube	13		
	D40C	Rail/Tube	9		
	D40J	Rail/Tube	9		
	D48A	Rail/Tube	7		
	D52A	Rail/Tube	7		
Ceramic Leadless Chip Carrier (LCC)	E20A	Rail/Tube	50		
	EA20B	Rail/Tube	50		
	E24B	Tray	25		
	E28A	Tray	28		
	EA028C	Tray	100		
	E32A	Rail/Tube	35		
	E32B	Rail/Tube	35		
	E32C	Rail/Tube	35		
	E40A	Rail/Tube	35		
	E44A	Rail/Tube	25		
	E48A	Tray	25		
	E68B	Tray	48		
	E68C	Tray	48		
	E84A	Tray	42		
	E84B	Tray	42		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Quad J-Bend (CQJB)	EL28A	Tray	96		
	EL44A	Tray	80		
	EL44B	Tray	80		
	EL44C	Tray	80		
	EL52A	Tray	50		
	EL68A	Tray	44		
	EL68B	Tray	44		
	EL68C	Tray	44		
	EL84A	Tray	42		
Ceramic Quad Flatpack (CQFP)	EL28B	Rail	15		
	EL64A	Box	36		
	EL100A	Tray	12		
	EL116A	Tray	12		
	EL132B	Tray	20		
	EL132C	Tray	20		
	EL132D	Tray	20		
	EL164A	Tray	12		
	EL172B	Tray	12		
	EL172C	Tray	12		
Ceramic Flatpack	F10B	Carrier/Rail	19	Carrier/Box	200
	F14C	Carrier/Rail	19	Carrier/Box	200
	F16B	Carrier/Rail	19	Carrier/Box	200

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Dual-In-Line Package (Cerdip)	J08A	Rail/Tube	40		
	J14A	Rail/Tube	25		
	J16A	Rail/Tube	25		
	J18A	Rail/Tube	20		
	J20A	Rail/Tube	20		
	J22A	Rail/Tube	17		
	J24A	Rail/Tube	15		
	J24AQ	Rail/Tube	15		
	J24B-Q	Rail/Tube	15		
	J24CQ	Rail/Tube	15		
	J24E	Rail/Tube	16		
	J24F	Rail/Tube	15		
	J28A	Rail/Tube	12		
	J28AQ	Rail/Tube	12		
	J28B	Rail/Tube	12		
	J28BQ	Rail/Tube	12		
	J28CQ	Rail/Tube	13		
	J32B	Rail/Tube	11		
	J32AQ	Rail/Tube	11		
	J40A	Rail/Tube	9		
	J40AQ	Rail/Tube	9		
	J40BQ	Rail/Tube	9		
Ceramic Small Outline Package, Wide	MC16A	Rail/Tube	45		
	MC20A	Rail/Tube	36		
	MC20B	Rail/Tube	36		
	MC24A	Rail/Tube	30		
	MC28A	Rail/Tube	26		
	MC28B	Rail/Tube	26		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Ceramic Pin Grid Array (CPGA)	U44A	Tray	80		
	U68B	Tray	42		
	U68C	Tray	42		
	U68D	Tray	42		
	U68E	Tray	42		
	U75A	Tray	35		
	U84A	Tray	42		
	U84B	Tray	42		
	U84C	Tray	42		
	U99A	Tray	25		
	U100A	Tray	30		
	U109A	Tray	25		
	U120A	Tray	30		
	U120C	Tray	30		
	U124A	Tray	30		
	U132A	Tray	30		
	U132B	Tray	30		
	U144A	Tray	20		
	U156A	Tray	20		
	U156B	Tray	20		
	U169A	Tray	20		
	U173A	Tray	20		
	U175A	Tray	20		
	U180A	Tray	20		
	U223A	Tray	20		
	U224A	Tray	20		
	U257A	Tray	12		
	U259A	Tray	12		
	U299A	Tray	12		
	U301A	Tray	12		
	U303A	Tray	12		
	U323A	Tray	12		

Immediate Packing Method for Ceramic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Cerpack	W10A	Carrier/Rail	19	Carrier/Box	200
	W14B	Carrier/Rail	19	Carrier/Box	200
	W14C	Carrier/Rail	19	Carrier/Box	200
	W16A	Carrier/Rail	19	Carrier/Box	200
	W20A	Carrier/Rail	19	Carrier/Box	200
	W24C	Carrier/Rail	15	Carrier/Box	80
	W28A	Carrier/Rail	15	Carrier/Box	80
	WA28D	Carrier/Rail	15	Carrier/Box	80
Cerquad	W24B	Rail/Tube	15		
	W56B	Tray	20		
	W64A	Tray	20		
	W68A	Tray	12		
	W84A	Tray	12		
Cerquad, EIAJ	WA80A	Tray	84		
	WA80AQ	Tray	84		
	W120A	Tray	12		
	W144A	Tray	12		
	W144B	Tray	12		
	W160A	Tray	12		
	W208A	Tray	12		

Immediate Packing Method for Metal Cans

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
TO-5	H06C	Tray	100	Carrier/Rail	18
	H08A	Tray	100	Carrier/Rail	18
	H08C	Tray	100	Carrier/Rail	18
	H10C	Tray	100	Cerrier/Rail	18
TO-18	H03C	Box	1800	Tray	100
TO-39	H03A	Tray	100	Carrier/Rail	18
	H03B	Tray	100	Carrier/Rail	18
	HA04E	Tray	100	Carrier/Rail	18
TO-46	H02A	Box	1800	Tray	100
	H03H	Box	1800	Tray	100
	H04A	Box	1800	Tray	100
	H04D	Box	1800	Tray	100
TO-52	H03J	Box	1800	Tray	100
TO-72	H04C	Box	1800	Tray	100

Immediate Packing Method for Plastic Packages

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Small Outline Transistor (SOT-23)	M03A	Tape and Reel	3000/ 10000	Bulk/Bag	500
	M03B	Tape and Reel	3000/ 10000	Bulk/Bag	500
Small Outline Package, JEDEC (SOP)	M08A	Rail/Tube	95	Tape and Reel	2500
	M14A	Rail/Tube	55	Tape and Reel	2500
	M14B	Rail/Tube	50	Tape and Reel	1000
	M16A	Rail/Tube	48	Tape and Reel	2500
	M16B	Rail/Tube	45	Tape and Reel	1000
	M20B	Rail/Tube	36	Tape and Reel	1000
	M24B	Rail/Tube	30	Tape and Reel	1000
	M28B	Rail/Tube	26	Tape and Reel	1000
Small Outline Package, EIAJ (SOP)	M14D	Rail/Tube	47	Tape and Reel	1000
	M16D	Rail/Tube	47	Tape and Reel	1000
	M20D	Rail/Tube	37	Tape and Reel	1000
Shrink Small Outline Package, JEDEC (SSOP)	MQA20	Rail/Tube	54	Tape and Reel	2500
	MQA24	Rail/Tube	54	Tape and Reel	2500
	MS48A	Rail/Tube	29	Tape and Reel	1000
	MS56A	Rail/Tube	25	Tape and Reel	1000
Shrink Small Outline Package, EIAJ (SSOP)	MSA20	Rail/Tube	65	Tape and Reel	1000
	MSA24	Rail/Tube	58	Tape and Reel	1000
	MS40A	Rail/Tube	34	Tape and Reel	1000
Very Small Outline Package (VSOP)	M40A	Rail/Tube	34	Tape and Reel	1000
Thin Small Outline Package, EIAJ (TSOP)	MBH32A	Tray	156		
Thin Shrink Small Outline Package, EIAJ (TSSOP)	MTA20	Tape and Reel	2500		

Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Molded Dual-In-Line Package (MDIP)	N08E	Rail/Tube	40		
	N14A	Rail/Tube	25		
	N16A	Rail/Tube	20		
	N16E	Rail/Tube	25		
	N16G	Rail/Tube	20		
	N18A	Rail/Tube	20		
	N20A	Rail/Tube	18		
	N22A	Rail/Tube	15		
	N22B	Rail/Tube	15		
	N24A	Rail/Tube	15		
	N24C	Rail/Tube	15		
	N24D	Rail/Tube	15		
	N24E	Rail/Tube	15		
	N28B	Rail/Tube	13		
	N40A	Rail/Tube	9		
	N48A	Rail/Tube	7		
TO-202	P03A	Rail/Tube	45	Box	300
	P03B	Rail/Tube	45	Box	300
	P03C	Rail/Tube	45	Box	300
	P03D	Rail/Tube	45	Box	300
	P03E	Rail/Tube	45	Box	300
	P03F	Rail/Tube	45	Box	300
	P03G	Rail/Tube	45	Box	300
	P03H	Rail/Tube	45	Box	300
	P03J	Rail/Tube	45	Box	300
	P04A	Rail/Tube	45	Box	300
	P11A	Rail/Tube	15		
TO-237	R03A	Box	1500	Tape and Reel	2000
	R03B	Box	1500	Tape and Reel	2000
	R03C	Box	1500	Tape and Reel	2000
	R03D	Box	1500	Tape and Reel	2000
TO-226	RC03A	Box	1500	Tape and Reel	2000
	RC03B	Box	1500	Tape and Reel	2000
	RC03C	Box	1500	Tape and Reel	2000
	RC03D	Box	1500	Tape and Reel	2000

Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
TO-220	TA02A	Rail/Tube	45	Box	300
	T02D	Rail/Tube	45	Box	300
	TA03A	Rail/Tube	45	Box	300
	TA03B	Rail/Tube	45	Box	300
	TA03D	Rail/Tube	45	Box	300
	T03A	Rail/Tube	45	Box	300
	T03B	Rail/Tube	45	Box	300
	T03D	Rail/Tube	45	Box	300
	T03F	Rail/Tube	45	Box	300
	T05A	Rail/Tube	45	Box	300
	T05B	Rail/Tube	45	Box	300
	T05C	Rail/Tube	45	Box	300
	T05D	Rail/Tube	45	Box	300
	T05E	Rail/Tube	45	Box	300
	T05F	Rail/Tube	45	Box	300
	TA05A	Rail/Tube	45	Box	300
	TA05B	Rail/Tube	45	Box	300
	TA11A	Rail/Tube	20	Box	300
	TA11B	Rail/Tube	20	Box	300
	TA11C	Rail/Tube	20	Box	300
	TA11D	Rail/Tube	20	Box	300
	TA11E	Rail/Tube	20	Box	300
	TA12A	Rail/Tube	20	Box	300
	TA15A	Rail/Tube	20	Box	300
	TA23A	Rail/Tube	15	Box	300
TapePak®	TP40A	Coinstack Tube	100	Flat Rail	25
Plastic Pin Grid Array (PPGA)	UP124A	Tray	30		
	UP159A	Tray	20		
	UP175A	Tray	20		
Plastic Leaded Chip Carrier (PLCC)	V20A	Rail/Tube	40	Tape and Reel	1000
	V28A	Rail/Tube	35	Tape and Reel	750
	V32A	Rail/Tube	30		
	V44A	Rail/Tube	25	Tape and Reel	500
	V52A	Rail/Tube	22	Tape and Reel	500
	V68A	Rail/Tube	18	Tape and Reel	250
	V84A	Rail/Tube	15	Tape and Reel	250

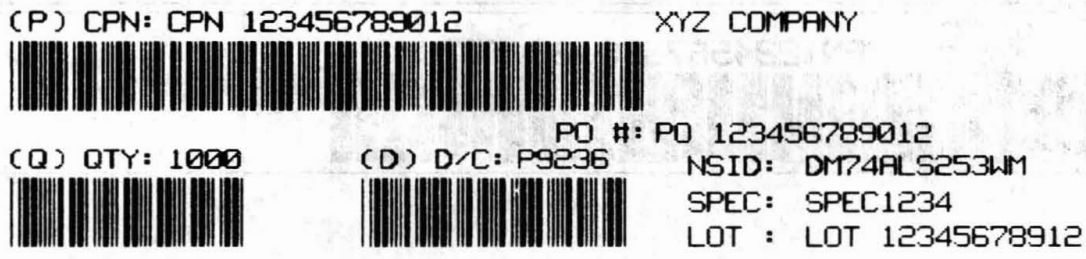
Immediate Packing Method for Plastic Packages (Continued)

Package Type (Code)	Package Marketing Drawing	Primary Immediate Container		Secondary Immediate Container	
		Method	Quantity	Method	Quantity
Plastic Quad Flatpack (PQFP)	VEF44A	Tray	96		
	VBG48A	Tray	60		
	VHG80A	Tray	60		
	VJE80A	Tray	84		
	VCC80A	Tray	50/66		
	VCE100A	Tray	84		
	VLJ100A	Tray	50		
	VJG100A	Tray	60		
	VNG144A	Tray	60		
	VUL160A	Tray	24		
	VQL160A	Tray	24		
	VUW208A	Tray	24		
	VF132A	Tray	36		
	VF196A	Tray	21		
TO-92	Z03A	Box	1800	Tape and Reel	2000
	Z03B	Box	1800	Tape and Reel	2000
	Z03C	Box	1800	Tape and Reel	2000
	Z03D	Box	1800	Tape and Reel	2000
	Z03E	Box	1800	Tape and Reel	2000
	Z03G	Box	1800	Tape and Reel	2000
	Z03H	Box	1800	Tape and Reel	2000
	Z03J	Box	1800	Tape and Reel	2000

Labeling

National Semiconductor offers 3 standard bar code labels; reel and intermediate container labels for Tape and Reel; intermediate container label other than for Tape and Reel; and outer/shipping container labels. The tape and reel, and intermediate container labels are National's own format while the outer/shipping container label is based on the EIA-556-A label standard.

NSC Standard Tape and Reel Label



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This label is placed on the reel (immediate container) as well as on the intermediate box.

NSC Standard Intermediate Container Label

XYZ COMPANY

(P) CPN CPN 1234567890

(Q) QTY 1000

(D)D.C. P9236

(A) P.O. PO 123456789012

NSID : DM74ALS253WM
FIN OPT : SPEC1234
LOT : LOT 123456789

P.L. : PL1234
REQA : RV1234
BOX 01 OF 03

NATIONAL SEMICONDUCTOR

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NSC Standard Outer/Shipping Container Label

(3S) PKG ID: EIA14+EP123456

FROM: N S C
SANTA CLARA, CA 95051

TO: XYZ COMPANY
SHIP TO ADDRESS 1
SHIP TO ADDRESS 2
SHIP TO ADDRESS 3
SHIP TO ADDRESS 4
SHIP TO ADDRESS 5

(Z) SPECIAL:

(Q) QUANTITY
10000 EA

PACKAGE COUNT
02 OF 05

(K) TRANS. ID: PO12345678901234567890

PACKAGE WEIGHT
1000 KG 2540 LB

(P) CUSTOMER PROD ID: CPN12345678901234567890

TL/P/11809–10

Board Mount of Surface Mount Components

Abstract

In facing the challenges of "Surface Mount Technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this process. However, as the availability of all products as surface mount components is still limited, many have had to mix lead-inserted components with surface mount devices (SMD's). Furthermore, to take advantage of using both sides of the board, some surface mounted components are adhered to the bottom side of the board while the top side is reserved for the conventional lead-insert packages and fine pitch surface mount packages.

There are three surface mount processes in hi-volume use today:

1. **WAVE SOLDER;** the surface mounted components are adhered to the bottom side of the board while the top side is reserved for the lead-inserted packages. The surface mount components are subjected to severe thermal stress when they are immersed into the molten solder.
2. **INFRA-RED** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, the solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment.
3. **VAPOR PHASE** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, tbe solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment, more severe than Infra-red but much less than wavesolder.

A discussion of the effect of these processes on the reliability of plastic semiconductor packages follows.

Role of Wave Soldering in Application of SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave soldering machine. The reasons being:

Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.

Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.

Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW Board Assembly Procedures

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.

b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or a combination of two or more methods.

The various processes that may be employed are:

A) WAVE SOLDER BEFORE VAPOR/IR REFLOW SOLDER

1. Components on the same side of PW Board. Lead insert standard DIPS onto PW Board Wave solder (conventional). Wash and lead trim. Dispense solder paste on SEM pads. Pick and place SMDs onto PW Board. Bake Vapor phase/IR reflow. Clean.
2. Components on opposite side of PW Board. Lead insert standard DIPs onto PW Board Wave Solder (conventional). Clean and lead trim. Invert PW Board. Dispense drop of adhesive on SMD sites (optional for smaller components). Pick and place SMDs onto board. Bake/Cure. Invert board to rest on raised fixture. Vapor/IR reflow soldering. Clean.

B) VAPOR/IR REFLOW SOLDER THEN WAVE SOLDER

1. Components on the same side of PW Board. Solder paste screened on SMD side of Printed Wire Board. Pick and place SMDs. Bake Vapor/IR reflow. Lead insert on same side as SMD's. Wave solder. Clean and trim underside of PCB.

C) VAPOR/IR REFLOW ONLY

1. Components on the same side of PW Board Trim and form standard DIPs in "gull wing" configuration. Solder paste screened on PW Board. Pick and place SMDs and DIPs. Bake Vapor/IR reflow. Clean.
2. Components on opposite sides of PW Board. Solder paste screened on SMD-side of Printed Wire Board. Adhesive dispensed at central location of each component. Pick and place SMDs. Bake. Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads. Lead insert DIPs. Vapor/IR reflow. Clean and lead trim.

PW Board Assembly Procedures

(Continued)

D) WAVE SOLDERING ONLY

1. Components on opposite sides of PW board. Adhesive dispense on SMD side of PW Board. Pick and place SMDs. Cure adhesive. Lead insert top side with DIPs. Wave solder with SMDs down and into solder bath. Clean and lead trim.

All of the above assembly procedures can be divided into three categories for IC. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a "pallet" where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Thermal Characteristics of Molded Integrated Circuits

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1.* Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on leadframes, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of leadframe material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal leadframe in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the epoxy-metal interface. However, If the package is subjected to temperature above its glass-transition temperature, the epoxy will expand much faster than the metal and the probability of separation is greatly increased.

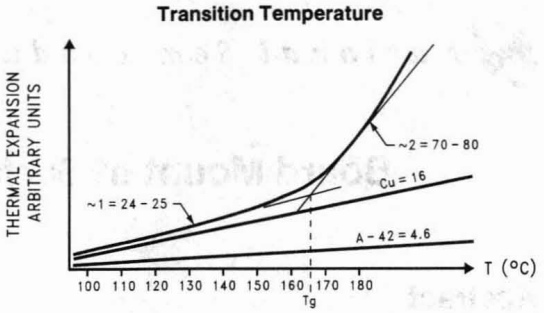

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FIGURE 1. Thermal Expansion and Glass

Conventional Wave Soldering

Most wave soldering operations occur at temperatures between 240°C–260°C. Conventional epoxies for encapsulation have glass-transition temperatures between 140°C–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1. The PW board has a certain amount of heat-sink effort and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120°C–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

Effect on Package Performance by Epoxy-Metal Separation

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metalization over time and premature failure of the device in the field.

Vapor Phase/IR Reflow Soldering

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Maximum operating temperatures are 219°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-leadframe interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

Bias Moisture Test

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a steam chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and 85% relative humidity. One cycle of approximately 100 hours has been shown to be equivalent to 2,000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2,000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

Test Results

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 217°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H.
85°C for 2,000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4,000 hours 85/85 test. Results were compared for packages by themselves against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 4 Sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 Sec @ 260°C	—	0/83
Solder Dip 6 Sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 Sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the packages being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6,000 hours in an 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturing Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Environment)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0/30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	12/30*	14/30*	2/30*	
Manuf E	1/30**	0/30	0/30	0/30	
Manuf F	0/30	0/30	0/30	0/30	
NSC	0/30	0/30	0/30	0/30	

*Corrosion failures

**No Visual Defects-Non-corrosion failues

Test Accelerated Bias Moisture Test: 85% R.H./85°C. 6,000 equivalent hours

Summary

Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low T_g compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of the package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

Recommended Soldering Profiles—Surface Mount

		Wave Solder	IR Profile	Vapor Phase
Ramp Up °C/sec	Maximum	6°C/sec	4°C/sec	24°C/sec
	Recommended	**4°C/sec***	**2°C/sec***	**2°C/sec**
	Minimum	**	**	**
ΔT	Maximum	135°C	N/A	N/A
	Recommended	**120°C**	**N/A**	**N/A**
	Minimum	110°C	N/A	N/A
Dwell Time ≥ 183°C	Maximum	N/A	85 seconds	85 seconds
	Recommended	**N/A**	**75 seconds***	**75 seconds***
	Minimum	N/A	30 seconds**	**
Solder Temperature	Maximum	260°C	240°C***	219°C
	Recommended	**240°C**	**215°C***	**215°C***
	Minimum	**	**	**
Dwell Time @ Max.	Maximum	4 seconds	10 seconds	75
	Recommended	**3 seconds**	**5 seconds**	**70 seconds**
	Minimum	**	1 second	**
Ramp Down °C/sec	Maximum	No Information	4°C/sec	4°C/sec
	Recommended	**4°C/sec**	**2°C/sec**	**2°C/sec**
	Minimum	No Information	**	**

Note: Temperature in degrees celcius. N/A = Not Applicable.

ΔT = The temperature differential between the final preheat stage and the soldering stage. Temperature measured at the component lead area.

*Will vary depending on board density, geometry, and package type.

**Will vary depending on package types, and board density.

***For plastic packages; ceramic packages maximum may be 250°C.

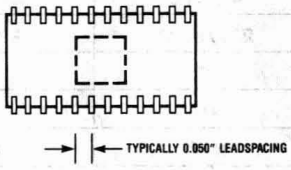
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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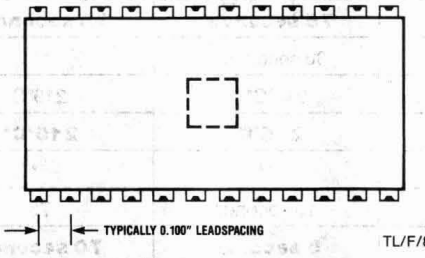
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

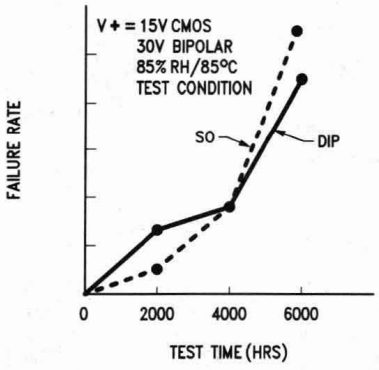

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

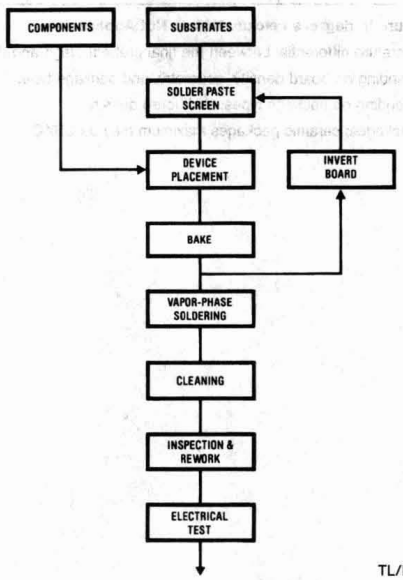
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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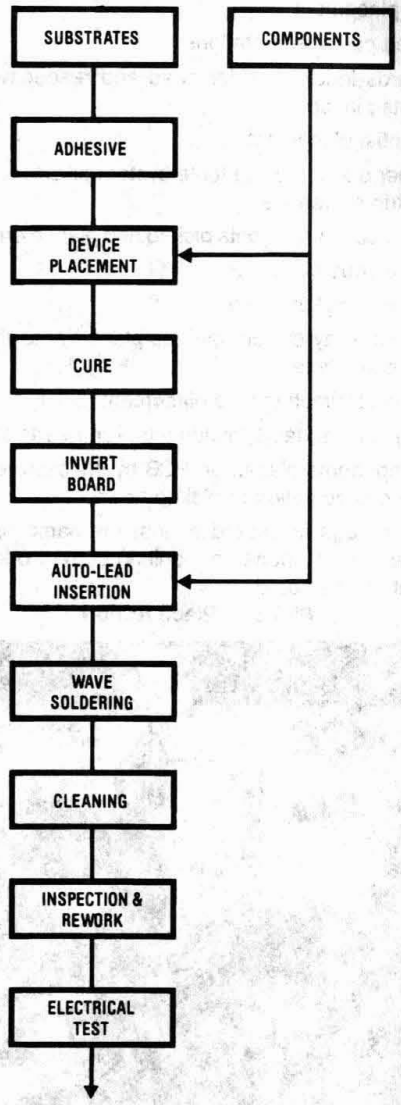
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

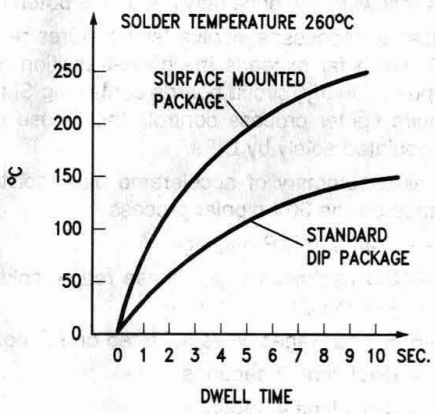

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

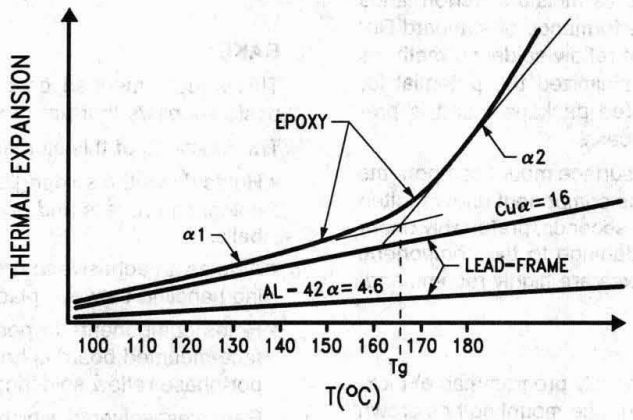

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

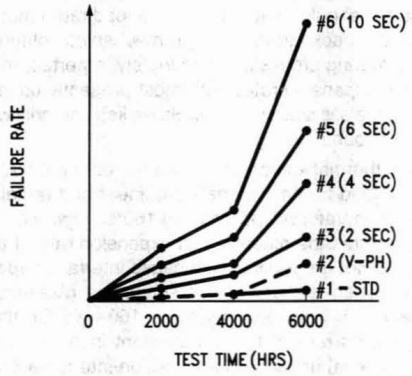

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

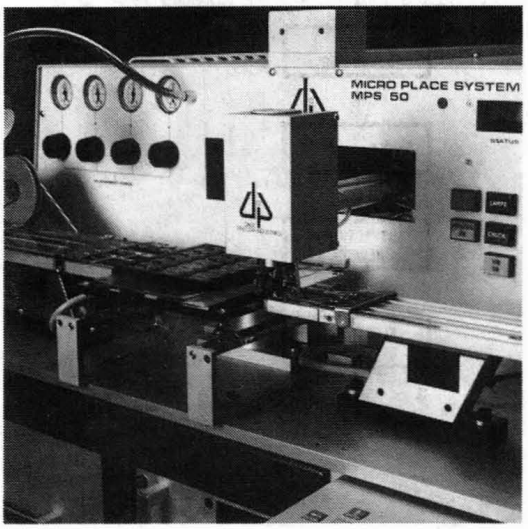
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

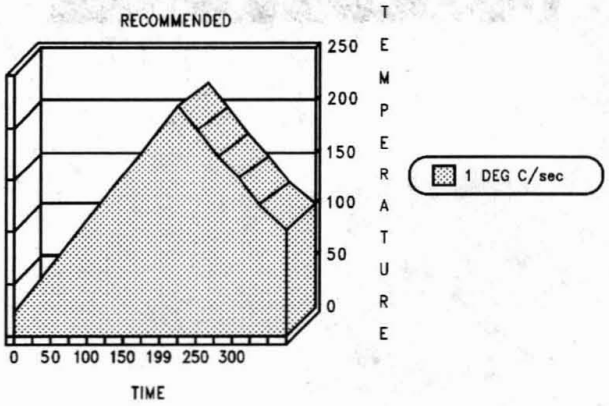
A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

INFRARED REFLOW SOLDERING

Use of an infrared furnace is currently the most popular method to automate mass reflow, the heating is promoted by use of IR lamps or panels. Early objections to this method were that certain materials may heat up at different rates under IR radiation and could result in damage to those components (usually sockets and connectors). This has been minimized by using far-infrared (non-focused) systems and convected air.

Infrared Profile



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VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

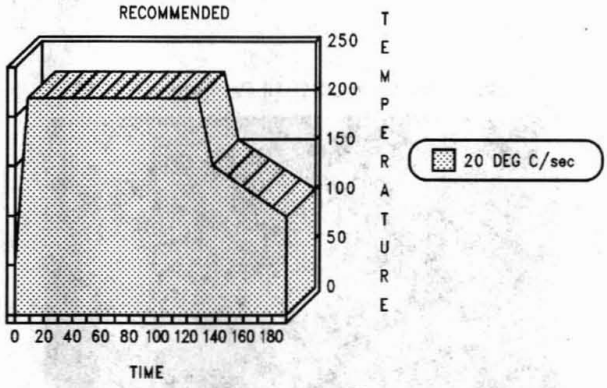
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

Vapor-Phase Profile



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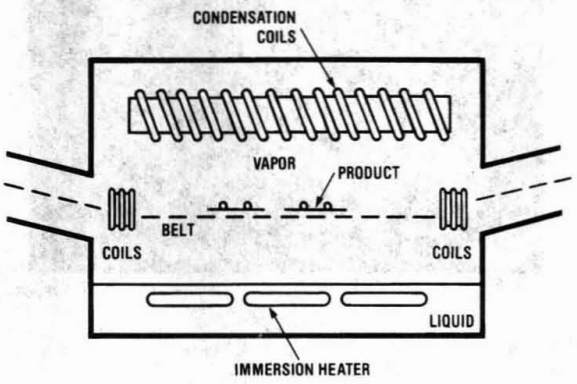
In-Line Conveyorized Vapor-Phase Soldering



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The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

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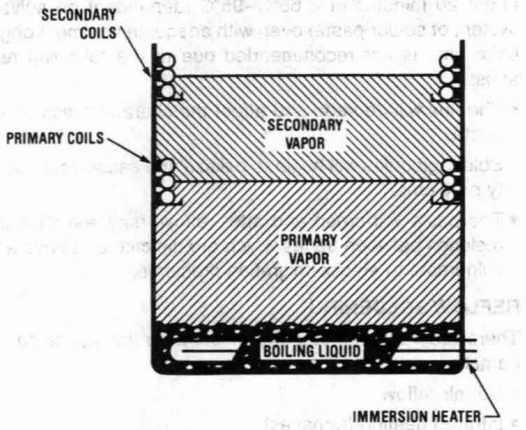
Batch-Fed Production Vapor-Phase Soldering Unit



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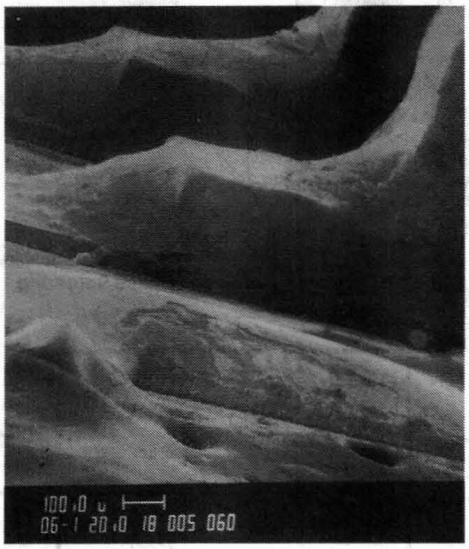
Solder Joints on a SO-14 Package on PCB



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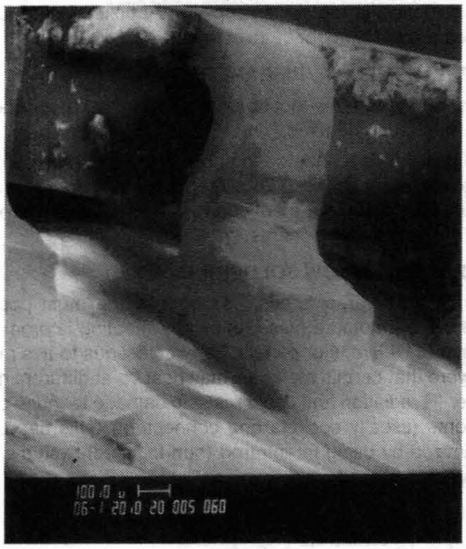
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed 1/8″, to avoid damage to screens and minimize distortion.

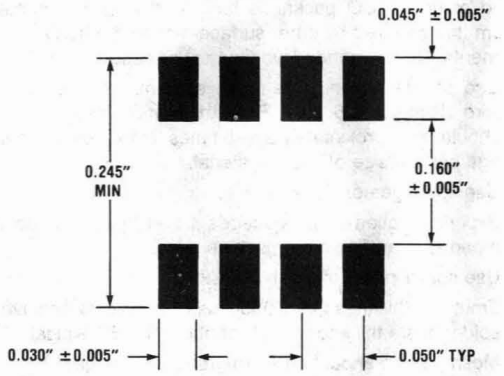
SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see following photographs). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.
- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



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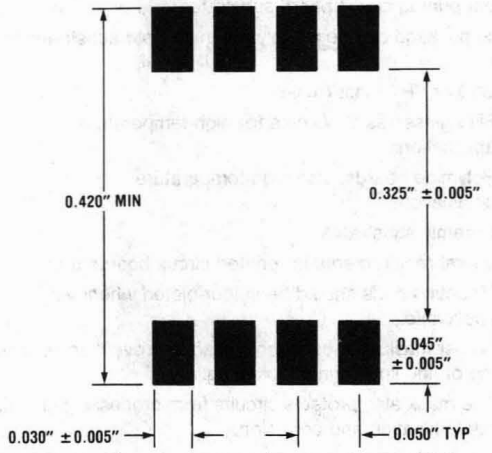
SO-16L, SO-20



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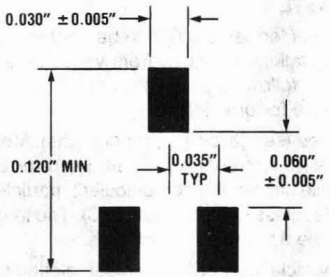
SOT-23



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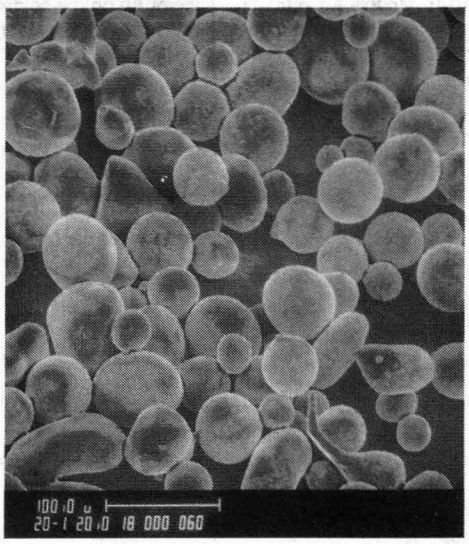
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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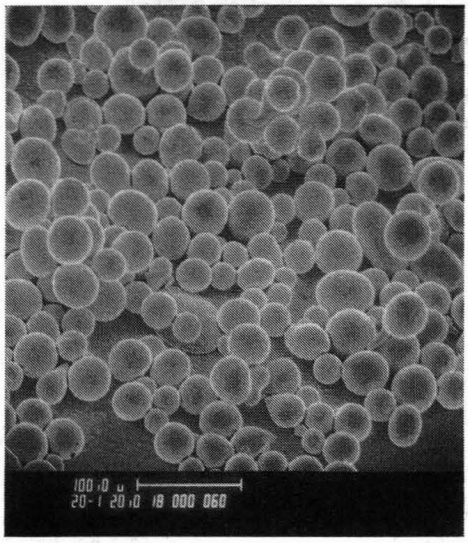
200 × Kester (63/37)



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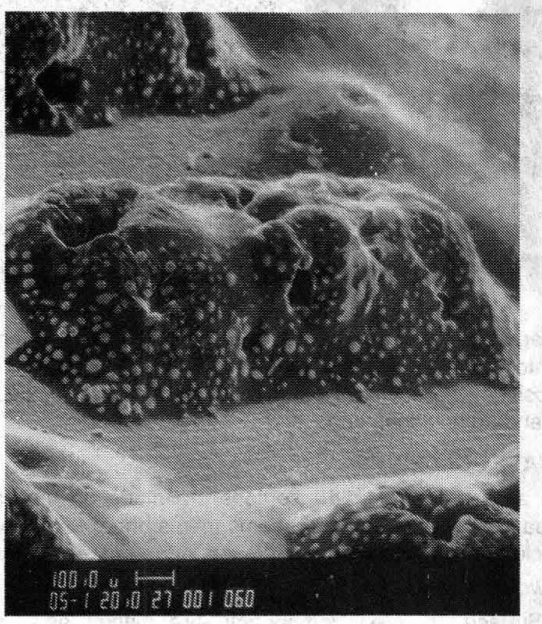
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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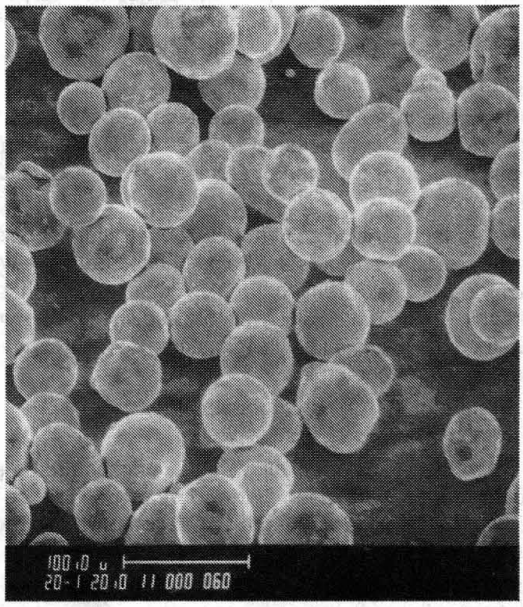
200 × Fry Metal (63/37)



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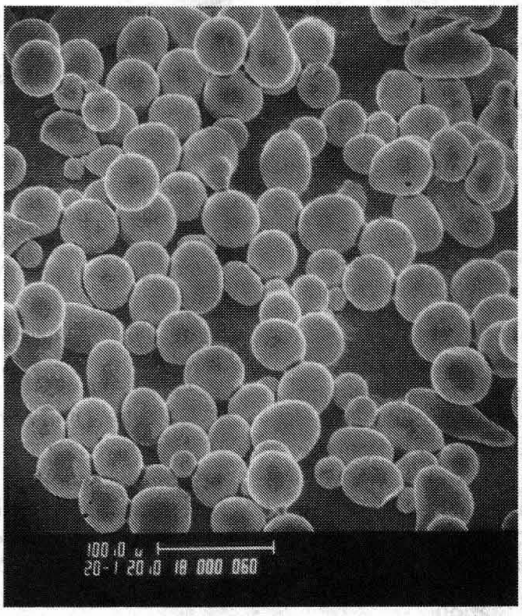
200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. CFC solvents are being phased out as they are hazardous to the environment. Other approaches to cleaning are commercially available and should be investigated on an individual basis considering local and government environmental rules.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

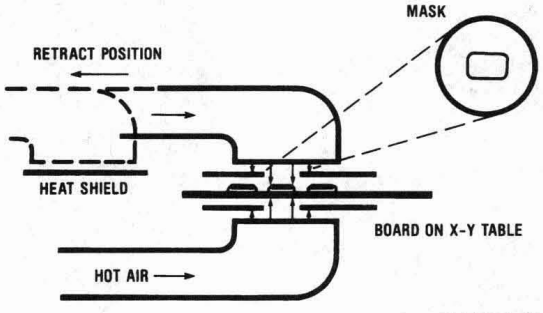
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

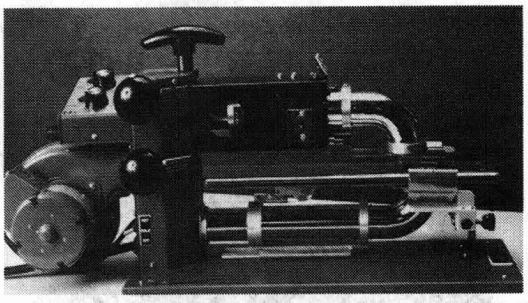
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/F/8766–22

Hot-Air Rework Machine



TL/F/8766–23

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

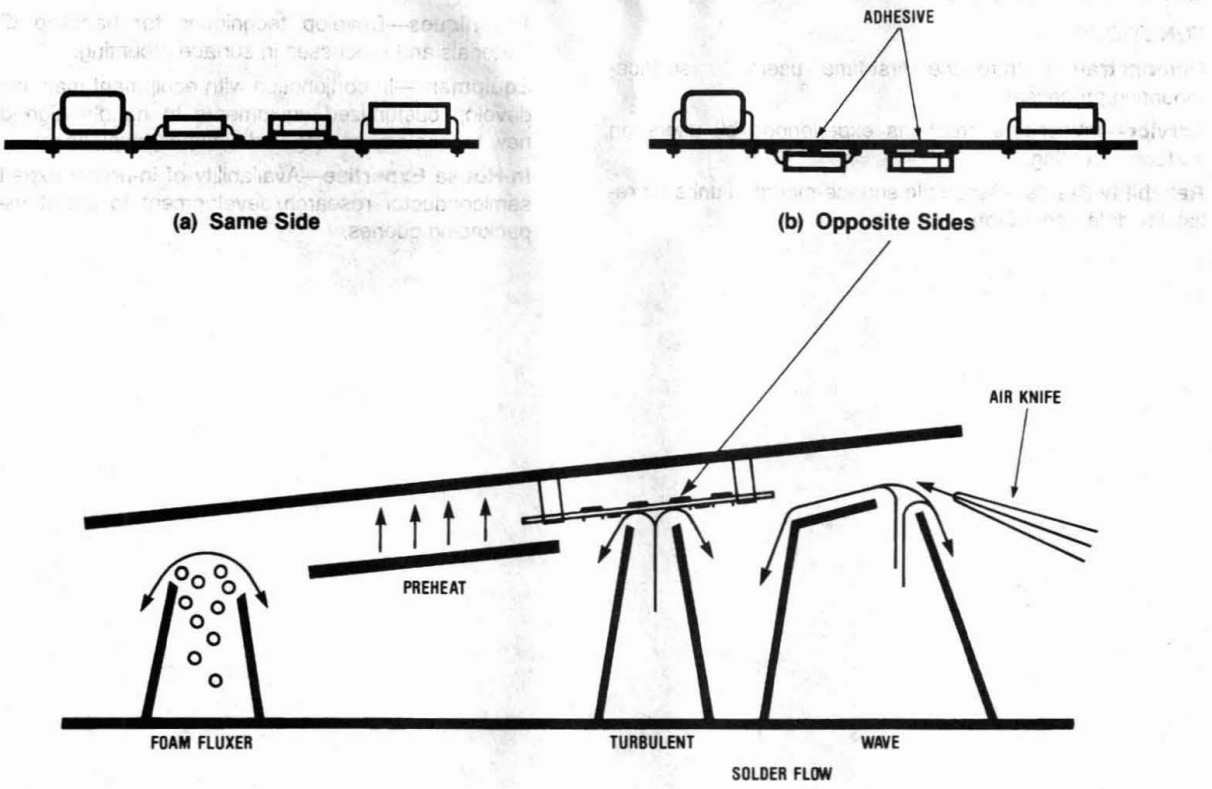
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



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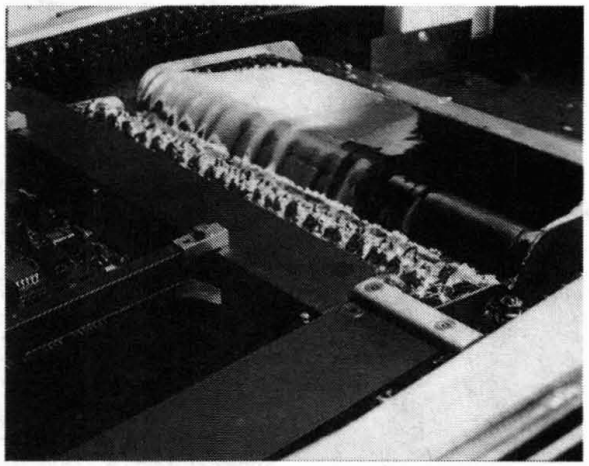
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

Dual Wave



TL/F/8766–25

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

National Semiconductor

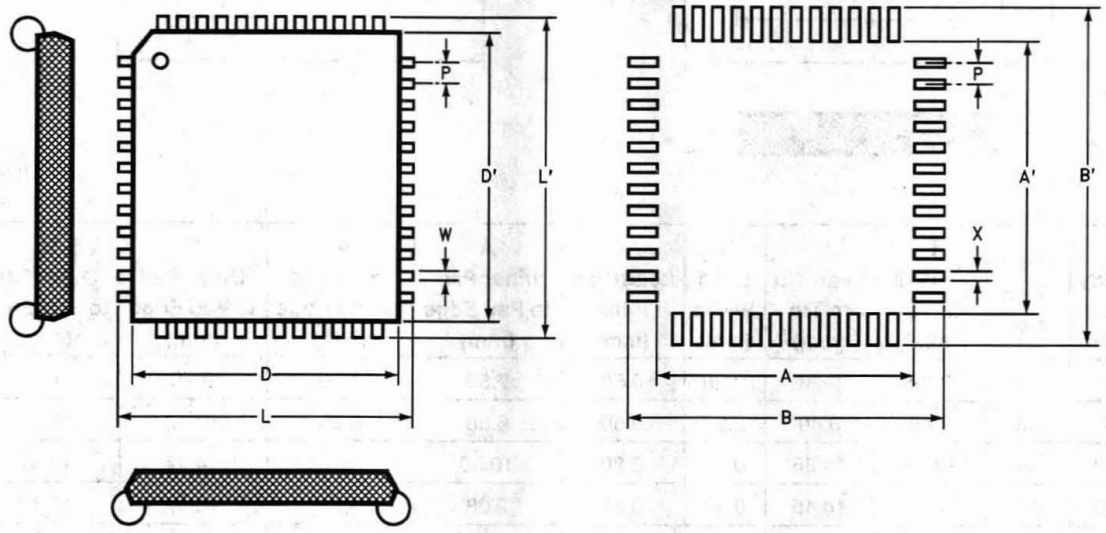
Land Pattern Recommendations

The following land pattern recommendations are provided as guidelines for board layout and assembly purposes.

These recommendations cover the following National Semiconductor packages: PLCC, PQFP, SOP, SSOP and TSOP.

For SOT-23 (5-Lead) and TO-263 (3- or 5-Lead) packages, refer to land patterns shown in the Physical Dimensions for MA05A and TS3B or TS5B packages, respectively.

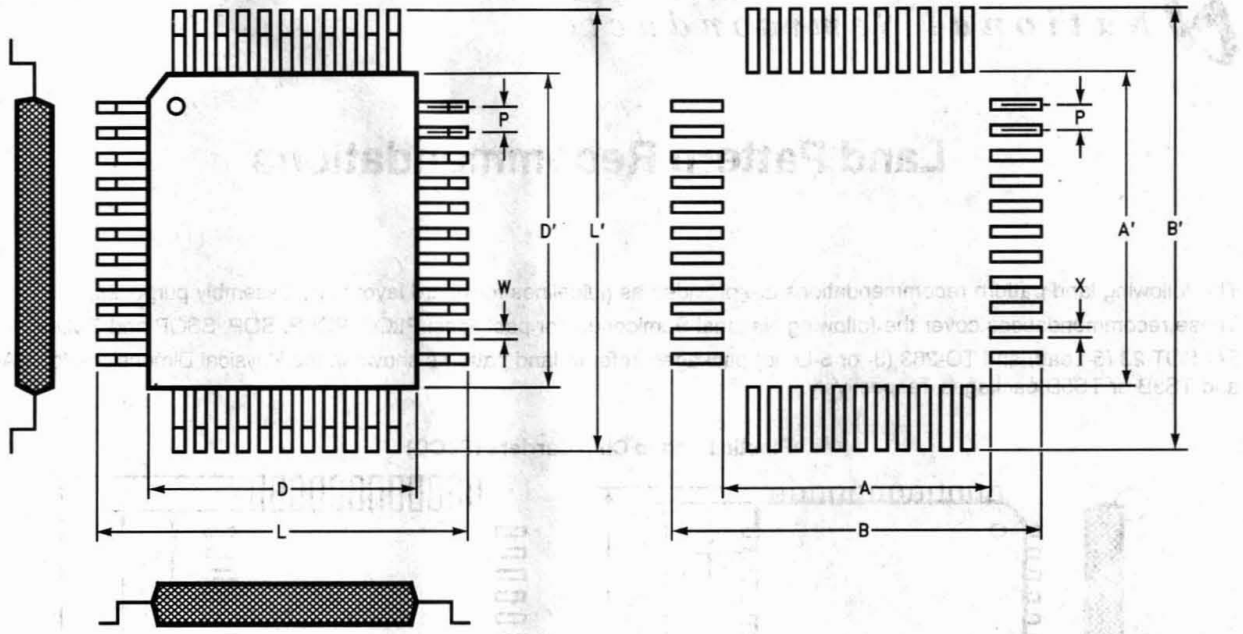
Plastic Leaded Chip Carriers (PLCC)



TL/P/11811–1

D Body Size (mm)	D' Body Size (mm)	Lead Count No.	L Lead Tip to Tip (mm)	L' Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	A' Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	B' Outer Pad to Pad Edge (mm)	X Land Width (mm)
8.89	8.89	20	10.03	10.03	0.53	1.27	6.73	6.73	10.80	10.80	0.63
11.43	11.43	28	12.57	12.57	0.53	1.27	9.27	9.27	13.34	13.34	0.63
11.43	14.05	32	12.57	15.11	0.53	1.27	9.27	12.00	13.34	16.00	0.63
16.51	16.51	44	17.65	17.65	0.53	1.27	14.35	14.35	18.42	18.42	0.63
19.05	19.05	52	20.19	20.19	0.53	1.27	16.89	16.89	20.96	20.96	0.63
24.13	24.13	68	25.27	25.27	0.53	1.27	21.97	21.97	26.04	26.04	0.63
29.21	29.21	84	30.35	30.35	0.53	1.27	27.05	27.05	31.12	31.12	0.63

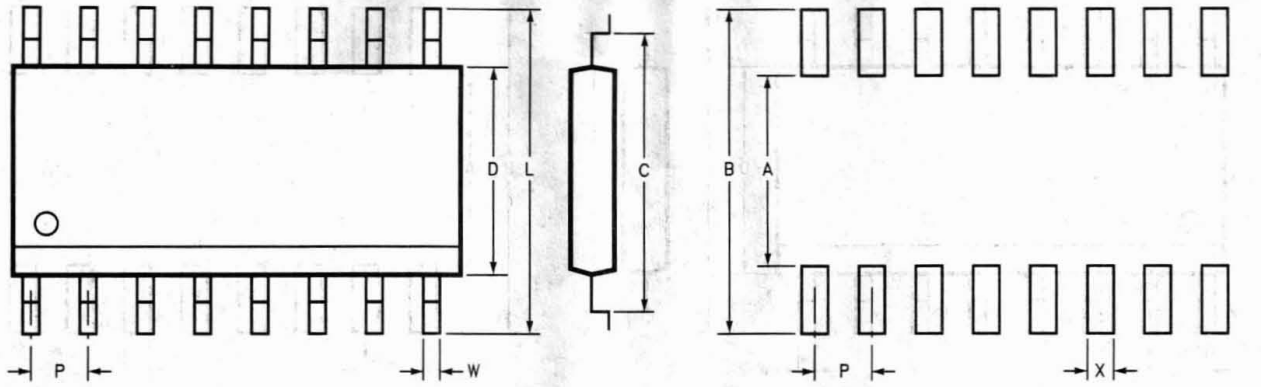
Plastic Quad Flat Packages (PQFP)



TL/P/11811–2

D Body Size (mm)	D' Body Size (mm)	Lead Count No.	L Lead Tip to Tip (mm)	L' Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	A' Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	B' Outer Pad to Pad Edge (mm)	X Land Width (mm)
7	7	40	9.29	9.29	0.26	0.50	7.50	7.50	9.78	9.78	0.30
7	7	48	9.40	9.40	0.27	0.50	6.88	6.90	10.42	10.40	0.32
10	10	44	13.35	13.35	0.45	0.80	10.53	10.53	14.47	14.47	0.55
10	10	52	14.15	14.15	0.38	0.65	9.08	9.08	15.17	15.17	0.43
12	12	64	14.00	14.00	0.38	0.65	11.48	11.48	15.02	15.02	0.43
14	14	80	18.15	18.15	0.38	0.65	13.08	13.08	19.17	19.17	0.43
14	20	80	17.80	23.80	0.35	0.80	13.50	19.50	18.50	24.50	0.40
14	14	100	17.45	17.45	0.30	0.50	13.08	13.08	18.47	18.47	0.35
14	20	100	17.80	23.80	0.30	0.65	13.50	19.50	18.50	24.50	0.35
20	20	100	24.30	18.30	0.40	0.65	21.28	15.28	25.32	19.32	0.45
24	24	132	24.21	24.21	0.30	0.64	21.67	21.67	25.23	25.23	0.40
28	28	120	32.15	32.15	0.45	0.80	27.88	27.88	33.17	33.17	0.55
28	28	128	31.45	31.45	0.45	0.80	28.03	28.03	32.47	32.47	0.55
28	28	144	32.15	32.15	0.38	0.65	28.03	28.03	33.17	33.17	0.43
28	28	160	32.40	32.40	0.38	0.65	29.48	29.48	33.42	33.42	0.43
28	28	208	30.60	30.60	0.30	0.50	28.08	28.08	31.62	31.62	0.35

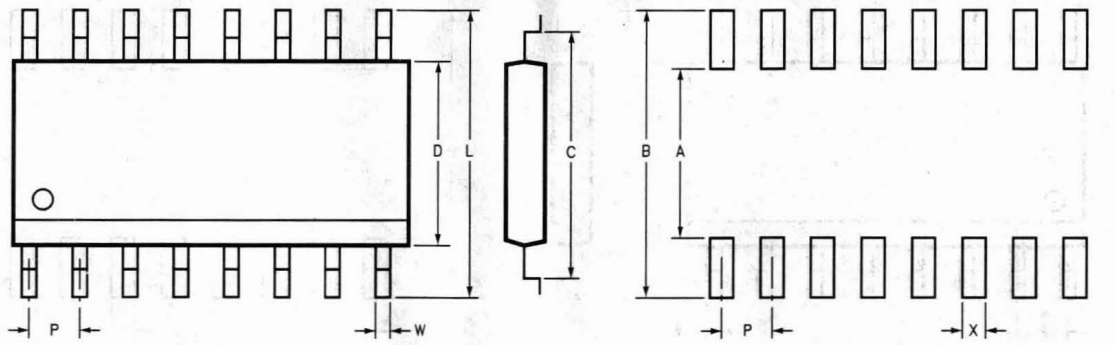
JEDEC Small Outline and Shrink Small Outline Packages (SOP and SSOP)



TL/P/11811–3

D Body Size (in)	Lead Count No.	C Shoulder to Shoulder (in)	L Lead Tip to Tip (in)	W Lead Width (in)	P Lead/Pad Pitch (in)	A Inner Pad to Pad Edge (in)	B Outer Pad to Pad Edge (in)	X Pad Width (in)
SOP								
0.150	8	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.150	14	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.150	16	0.144	0.244	0.020	0.050	0.094	0.294	0.028
0.300	14	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	16	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	20	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	24	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
0.300	28	0.3300	0.4100	0.0190	0.0500	0.2800	0.4600	0.0270
SSOP								
0.150	20	0.185	0.241	0.010	0.025	0.145	0.281	0.014
0.150	24	0.185	0.241	0.010	0.025	0.145	0.281	0.014
0.300	48	0.340	0.420	0.012	0.025	0.300	0.460	0.016
0.300	56	0.340	0.420	0.012	0.025	0.300	0.460	0.016

EIAJ Small Outline, Shrink Small Outline, and Thin Small Outline Packages (SOP, SSOP and TSOP)



TL/P/11811–4

D Body Size (mm)	Lead Count No.	C Shoulder to Shoulder (mm)	L Lead Tip to Tip (mm)	W Lead Width (mm)	P Lead/Pad Pitch (mm)	A Inner Pad to Pad Edge (mm)	B Outer Pad to Pad Edge (mm)	X Pad Width (mm)
SOP TYPE II								
5.300	14	6.280	8.000	0.400	1.270	5.010	9.270	0.600
5.300	16	6.280	8.000	0.400	1.270	5.010	9.270	0.600
5.300	20	6.280	8.000	0.400	1.270	5.010	9.270	0.600
SSOP TYPE II								
5.300	20	6.600	8.100	0.400	0.650	5.584	9.116	0.451
5.300	24	6.600	8.100	0.400	0.650	5.584	9.116	0.451
SSOP TYPE III								
7.500	40	8.900	10.500	0.350	0.650	7.884	11.516	0.452
TSOP TYPE I								
18.500	32	19.000	20.200	0.250	0.500	17.984	21.216	0.301

Section 10

Appendices/ Physical Dimensions

Section 10 Contents

Appendix A General Product Marking and Code Explanation 10-3
Appendix B Device/Application Literature Cross-Reference 10-4
Appendix D Military Aerospace Programs from National Semiconductor 10-10
Appendix E Understanding Integrated Circuit Package Power Capabilities 10-20
Appendix F How to Get the Right Information from a Datasheet 10-25
Physical Dimensions 10-29
Bookshelf
Distributors

National Semiconductor

Appendix A
General Product Marking & Code Explanation

LF 356 N /A+

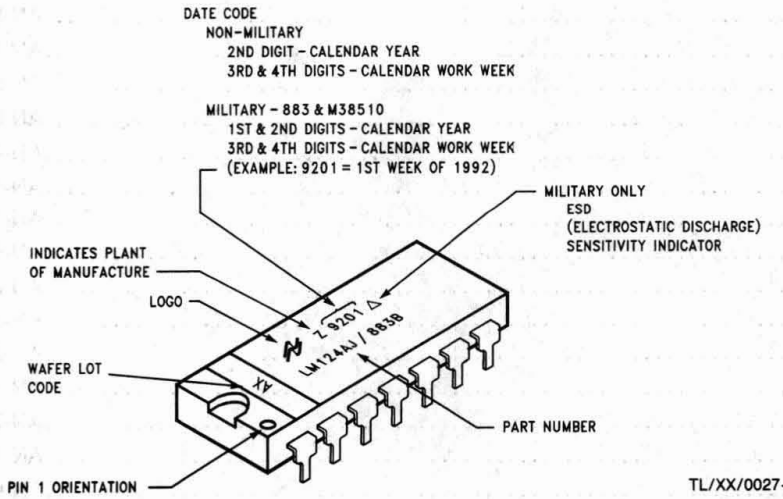
- /A+ — Reliability Program (Optional) (Refer to Appendix C)
- N — Package Type (See Right)
- 356 — Device Number (Generic Type) and Suffix Letter (Optional)
  - A or B: Improved Electrical Specification
  - C, I, E or M: Temperature Range
- LF — Device Family (See Below)

Device Family

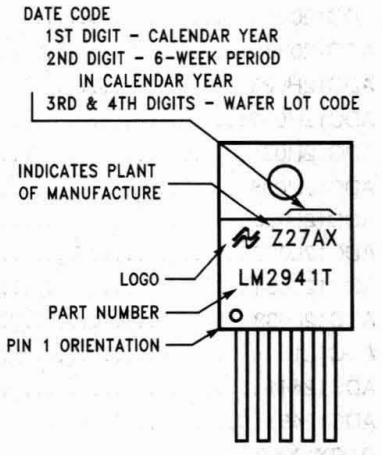
ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (BI-FET™)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LP	Linear (Low Power)
LPC	Linear CMOS (Low Power)
MF	Linear (Monolithic Filter)
LMF	Linear Monolithic Filter

Package Type

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (¼" x ¼")
G	12 Lead TO-8 Metal Can (M/C)
H	Multi-Lead Metal Can (M/C)
H-05	4 Lead M/C (TO-5) } Shipped with
H-46	4 Lead M/C (TO-46) } Thermal Shield
J	Lo-Temp Ceramic DIP
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
M3	3-Lead Small Outline Package
M5	5-Lead Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 Power Pkg
Q	Cerdip with UV Window
S	3,5,11, & 15 Lead TO-263 Surf. Mt. Power Pkg
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package



TL/XX/0027-2



TL/XX/0027-3

10

National Semiconductor

Appendix B
Device/Application Literature Cross-Reference

Device Number	Application Literature
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN-274, AN-280, AN-281, LB-53
ADC08031	AN-460
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC10461	AN-769
ADC10462	AN-769
ADC10464	AN-769
ADC10662	AN-769
ADC10664	AN-769
ADC12030	AN-929
ADC12032	AN-929
ADC12034	AN-929
ADC12038	AN-929
ADC12H030	AN-929
ADC12H032	AN-929
ADC12H034	AN-929
ADC12H038	AN-929
ADC12L030	AN-929
ADC12L032	AN-929
ADC12L034	AN-929
ADC12L038	AN-929
ADC1210	AN-245
ADC12441	AN-769
ADC12451	AN-769
DACXXXX	AN-156
DAC0800	AN-693
DAC0830	AN-284

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-2293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1219	AN-693
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-262, AN-263, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693
LF357	AN-263, AN-447, LB-42
LF398	AN-247, AN-258, AN-266, AN-294, AN-298, LB-45
LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LH0002	AN-13, AN-227, AN-263, AN-272, AN-301
LH0024	AN-253
LH0032	AN-242, AN-253
LH0033	AN-48, AN-227, AN-253
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0094	AN-301
LH0101	AN-261

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LH1605	AN-343
LH2424	AN-867
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693
LM11	AN-241, AN-242, AN-260, AN-266, AN-271
LM12	AN-446, AN-693, AN-706
LM101	AN-4, AN-13, AN-20, AN-24, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241 AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM105	AN-23, AN-110, LB-3
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82
LM129	AN-173, AN-178, AN-262, AN-266
LM131	AN-210, AN-460, Appendix D
LM131A	AN-210
LM134	LB-41, AN-460
LM135	AN-225, AN-262, AN-292, AN-298, AN-460
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260
LM199A	AN-161
LM211	LB-39

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM231	AN-210
LM231A	AN-210
LM235	AN-225
LM239	AN-74
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM34	AN-460
LM35	AN-460
LM301A	AN-178, AN-181, AN-222
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-299, LB-21
LM319	AN-828, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D
LM331A	AN-210, Appendix C
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM385	AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777
LM386	LB-54
LM391	AN-272
LM392	AN-274, AN-286

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM393	AN-271, AN-274, AN-293, AN-694
LM394	AN-262, AN-263, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28
LM399	AN-184
LM555	AN-694, AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM604	AN-460
LM628	AN-693, AN-706
LM629	AN-693, AN-694, AN-706
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-79, LB-19, LB-22
LM833	AN-346
LM1036	AN-390
LM1202	AN-867
LM1203	AN-861
LM1204	AN-934
LM1458	AN-116
LM1524	AN-272, AN-288, AN-292, AN-293
LM1558	AN-116
LM1578A	AB-30
LM1823	AN-391
LM1830	AB-10
LM1865	AN-390
LM1886	AN-402
LM1889	AN-402
LM1894	AN-384, AN-386, AN-390
LM2419	AN-861
LM2577	AN-776, AN-777
LM2876	AN-898
LM2889	AN-391, AN-402
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3525A	AN-694
LM3578A	AB-30
LM3875	AN-898
LM3876	AN-898
LM3886	AN-898
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3914	AN-460, LB-48, AB-25
LM3915	AN-386
LM3999	AN-161

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM4250	AN-88, LB-34
LM6181	AN-813, AN-840
LM7800	AN-178
LM12454	AN-906, AN-947, AN-949
LM12458	AN-906, AN-947, AN-949
LM12H454	AN-906, AN-947, AN-949
LM12H458	AN-906, AN-947, AN-949
LM12L458	AN-906, AN-947, AN-949
LM18293	AN-706
LM78L12	AN-146
LM78S40	AN-711
LMC555	AN-460, AN-828
LMC660	AN-856
LMC835	AN-435
LMC6044	AN-856
LMC6062	AN-856
LMC6082	AN-856
LMC6484	AN-856
LMD18200	AN-694, AN-828
LMF40	AN-779
LMF60	AN-779
LMF90	AN-779
LMF100	AN-779
LMF380	AN-779
LMF390	AN-779
LP324	AN-284
LP395	AN-460
LPC660	AN-856
MF4	AN-779
MF5	AN-779
MF6	AN-779
MF8	AN-779
MF10	AN-307, AN-779
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74HC86	AN-861, AN-867
MM74LS138	LB-54
MM53200	AN-290
2N4339	AN-32

National Semiconductor

Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. The process flows and catagories shown below are for general reference only. For further information and availability, please contact the Customer Response Center at 1-800-272-9959, Military/Aerospace Marketing group or your local sales office.

National Semiconductor's Military/Aerospace Program is founded on dedication to excellence. National offers complete support across the broadest range of products with the widest selection of qualification levels and screening flows. These flows include:

Process Flows (Integrated Circuits)	Description
JAN S	QML products processed to MIL-I-38535 Level S or V for Space level applications.
JAN B	QML products processed to MIL-I-38535 Level B or Q for Military applications.
SMD	QML products processed to a Standard Microcircuit Drawing with Table I Electricals controlled by DESC.
883	QML products processed to MIL-STD-883 Level B for Military applications.
MLP	Products processed on the Monitored Line (Program) developed by the Air Force for Space level applications.
-MIL	Similar to MIL-STD-883 with exceptions noted on the Certificate of Conformance.
MSP	Military Screening Products for initial release of advanced products.
MCP	Commercial products processed in a military assembly. Electrical testing performed at 25°C, plus minimum and maximum operating temperature to commercial limits.
MCR	Commercial products processed in a military assembly. Electrical testing performed at 25°C to commercial limits
MRP	Military Ruggedized Plastic products processed to avionics requirements.
MRR	Commercial Ruggedized plastic product processed in a commercial assembly with electrical testing at 25°C.
MPC	Commercial plastic products processed in a commercial assembly with electrical testing at 25°C.

- **QML:** The purpose of the QML program, which is administered by the Defense Electronics Supply Center (DESC), is to provide the military community with standardized products that have been manufactured and screened to the highest quality and reliability standards in facilities that have been certified by the government. To achieve QML status, manufacturers must submit their facilities, quality procedures and design philosophies to a thorough audit aimed at confirming their ability to produce product to the highest design and quality standards. They must be listed on DESC's Qualified Manufacturer List (QML) before devices can be marked and shipped as QML product.

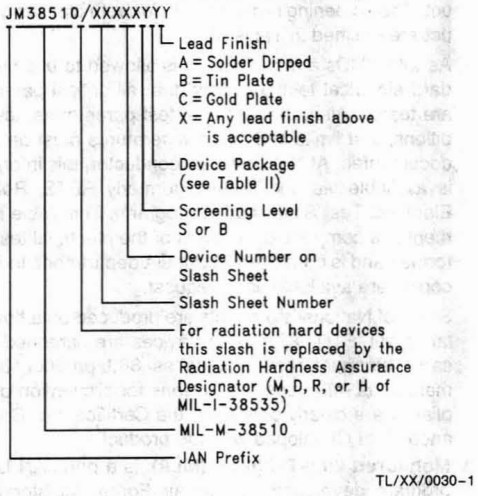
  Two processing levels are specified within MIL-I-38535, the QML standard: Class S (typically specified for space and strategic applications) and Class B (used for tactical missile, airborne, naval and ground systems). The requirements for both classes are defined within MIL-STD-883. National is one of the industry's leading suppliers of both classes.
- **Standard Microcircuit Drawings (SMD).** SMDs are issued to provide standardized versions of devices offered under QML. MIL-STD-883 screening is coupled with tightly controlled electrical test specifications that allow a manufacturer to use his standard electrical tests. Table I explains the marking of JAN devices, and Table II outlines current marking requirements for QML/SMD devices. Copies of MIL-I-38535 and the QML can be obtained from the Naval Publications and Forms Center (5801 Tabor Avenue, Philadelphia, PA 19120, 212/697-2179. A current listing of National's SMD offerings can be obtained from our authorized distributors, our sales offices, our Customer Response Center (Arlington, Texas, 817/468-6300), or from DESC.
- **MIL-STD-883.** Originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-SMD military product. MIL-STD-883 defines the minimum requirements for a device to be marked and advertised as 883-compliant. Design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures are outlined in paragraph 1.1.2 of MIL-STD-883.

  National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

  As with SMDs a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits and test temperatures must be clearly documented. At National Semiconductor, this information is available via our Table I (formerly RETS, Reliability Electrical Test Specification Program). The Table I document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

  Some of National's products are produced on a flow similar to MIL-STD-883. These devices are screened to the same stringent requirements as 883 product, but are marked as **-MIL**; specific reasons for prevention of compliancy are clearly defined in the Certificate of Conformance (C of C) shipped with the product.
- **Monitored Line Program (MLP):** is a non JAN Level S program developed by the Air Force. Monitored Line product usually provides the shortest cycle time, and is acceptable for application in several space level programs. Lockheed Missiles and Space Company in Sunnyvale, California, under an Air Force contract, provides "on-site" monitoring of product processing, and as appropriate, program management. Monitored Line orders generally do not allow "customizing", and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company.
- **Military Screening Program (MSP):** National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly. Through this program, screened product is made available for prototypes and breadboards prior to or during the QML activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. JAN S or B Part Marking


JM38510/XXXXXYYY
Lead Finish
A = Solder Dipped
B = Tin Plate
C = Gold Plate
X = Any lead finish above is acceptable
Device Package (see Table II)
Screening Level S or B
Device Number on Slash Sheet
Slash Sheet Number
For radiation hard devices this slash is replaced by the Radiation Hardness Assurance Designator (M, D, R, or H of MIL-I-38535)
MIL-M-38510
JAN Prefix

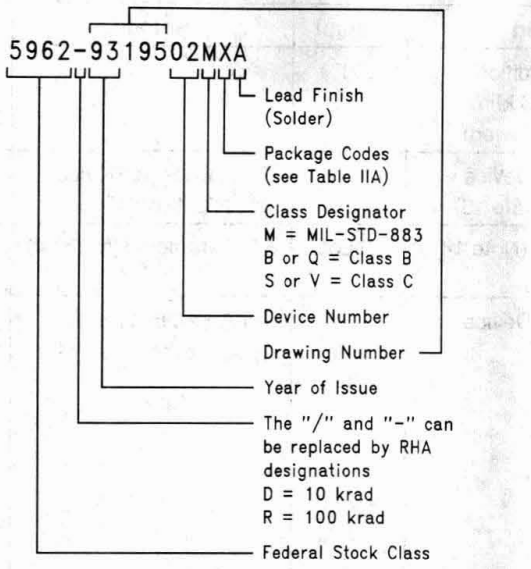
TL/XX/0030–1

TABLE I-A. JAN Package Codes

JAN Package Designation	Microcircuit Industry Description
A	14-pin 1/4" x 1/4" (Metal) Flatpak
B	14-pin 3/16" x 1/4" (Metal) Flatpak
C	14-pin 1/4" x 3/4" Dual-In-Line
D	14-pin 1/4" x 3/8" (Ceramic) Flatpak
E	16-pin 1/4" x 7/8" Dual-In-Line
F	16-pin 1/4" x 3/8" (Metal or Ceramic) Flatpak
G	8-pin TO-99 Can or Header
H	10-pin 1/4" x 1/4" (Metal) Flatpak
I	10-pin TO-100 Can or Header
J	24-pin 1/2" x 1 1/4" Dual-In-Line
K	24-pin 3/8" x 5/8" Flatpak
L	24-pin 1/4" x 1 1/4" Dual-In-Line
M	12-pin TO-101 Can or Header
N	(Note 1)
P	8-pin 1/4" x 3/8" Dual-In-Line
Q	40-pin 3/16" x 2 1/16" Dual-In-Line
R	20-pin 1/4" x 1 1/16" Dual-In-Line
S	20-pin 1/4" x 1/2" Flatpak
T	(Note 1)
U	(Note 1)
V	18-pin 3/8" x 15/16" Dual-In-Line
W	22-pin 3/8" x 1 1/8" Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350" x 0.350" Chip Carrier
3	28-terminal 0.450" x 0.450" Chip Carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE II. Standard Military Drawing (SMD) Marking



TL/XX/0030–2

TABLE II-A. SMD Package Codes

SMD Package Designation	Microcircuit Industry Description
C	14-pin Flatpak
D	14-pin C DIP
E	16-pin C DIP
F	16-pin Flatpak
G	8-pin TO-99 Can
H	10-pin (Metal) Flatpak
I	10-pin TO-100 Can
X	(Note 2)
Y	(Note 2)
P	8-pin C DIP
2	20-pin LCC
R	20-Pin DIP

Note 2: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
1.	Wafer Lot Acceptance	5007	All Lots		
2.	Nondestructive Bond Pull (Note 14)	2023	100%		
3.	Internal Visual (Note 1)	2020, Condition A	100%	2010, Condition B	100%
4.	Stabilization Bake (Note 16)	1008, Condition C, Min 24 Hrs. Min	100%	1008, Condition C, Min 24 Hrs. Min	100%
5.	Temperature Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E Min Y_1 Orientation Only	100%	2001, Condition E Min Y_1 Orientation Only	100%
7.	Visual Inspection (Note 3)		100%		100%
8.	Particle Impact Noise Detection (PIND)	2010, Condition A (Note 4)	100%		
9.	Serialization	(Note 5)	100%		
10.	Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	
11.	Burn-In Test	1015 240 Hrs. @ 125°C Min (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min	100%
12.	Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 3)	100%		

TABLE III. 100% Screening Requirements (Continued)

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
13.	Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min (Cond. F Not Allowed)	100%		
14.	Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15.	PDA Calculation	5% Parametric (Note 14), 3% Functional	All Lots	5% Parametric (Note 14)	All Lots
16.	Final Electrical Test (Note 15) a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005) b) Dynamic Tests or Functional Tests 1) 25°C (Subgroup 4 or 7) 2) Max and Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005) c) Switching Tests 25°C (Subgroup 9, Table I, 5005)	Per Applicable Device Specification	 100% 100% 100% 100% 100%	Per Applicable Device Specification	 100% 100% 100% 100% 100%
17.	Seal Fine, Gross	1014	100% (Note 8)	1014	100% (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock Method 1011, Test Condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-I-38585 paragraph 40.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpaks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

Military Analog Products Available from National Semiconductor

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
HIGH PERFORMANCE AMPLIFIERS AND BUFFERS				
LF147	D, J	Wide BW Quad JFET Op Amp	SMD/JAN	/11906
LF155A	H	JFET Input Op Amp	883	—
LF156	H	JFET Input Op Amp	883	—
LF156A	H	JFET Input Op Amp	883	—
LF157	H	JFET Input Op Amp	883	—
LF157A	H	JFET Input Op Amp	883	—
LF411M	H	Low Offset, Low Drift JFET Input	883/JAN	/11904
LF412M	H, J	Low Offset, Low Drift JFET Input-Dual	883/JAN	/11905
LF441M	H	Low Power JFET Input	883	—
LF442M	H	Low Power JFET Input-Dual	883	—
LF444M	D	Low Power JFET Input-Quad	883	—
LH0002	H	Buffer Amp	"-MIL"	—
LH0021	K	1.0 Amp Power Op Amp	"-MIL"	—
LH0024	H	High Slew Rate Op Amp	"-MIL"	—
LH0032	G	Ultra Fast FET-Input Op Amp	"-MIL"	—
LH0041	G	0.2 Amp Power Op Amp	"-MIL"	—
LH0101	K	Power Op Amp	"-MIL"	—
LM10	H	Super-Block™ Micropower Op Amp/Ref	883/SMD	5962-87604
LM101A	J, H, W	General Purpose Op Amp	883/JAN	/10103
LM108A	J, H, W	Precision Op Amp	883/JAN	/10104
LM118	J, H	Fast Op Amp	883/JAN	/10107
LM124	J, E, W	Low Power Quad Op Amp	883/JAN	/11005
LM124A	J, E, W	Low Power Quad	883/JAN	/11006
LM146	J	Quad Programmable Op Amp	883	—
LM148	J, E	Quad 741 Op amp	883/JAN	/11001
LM158A	J, H	Low Power Dual Op Amp	883/SMD	5962-8771002
LM158	J, H	Low Power Dual Op Amp	883/SMD	5962-8771001
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	—
LM613AM	J, E	Super-Block Dual Op Amp/Dual Comp/Ref	883/SMD	—
LM614AM	J	Super-Block Quad Op Amp/Ref	883/SMD	—
LM709A	H, J, W	General Purpose Op Amp	883/SMD	7800701
LM741	J, H, W	General Purpose Op Amp	883/JAN	/10101
LM747	J, H	General Purpose Dual Op Amp	883/JAN	/10102
LM6118	J, E	VIP Dual Op Amp	883/SMD	5962-91565
LM6121	H, J	VIP Buffer	883/SMD	5962-90812
LM6125	H	VIP Buffer with Error Flag	883/SMD	5962-90815
LM6161	J, E, W	VIP Op Amp (Unity Gain)	883/SMD	5962-89621
LM6162	J, E, W	VIP Op Amp ($A_V > 2, -1$)	883/SMD	5962-92165
LM6164	J, E, W	VIP Op Amp ($A_V > 5$)	883/SMD	5962-89624
LM6165	J, E, W	VIP Op Amp ($A_V > 25$)	883/SMD	5962-89625
LM6181AM	J	VIP Current Feedback Op Amp	883/SMD	5962-9081802
LM6182AM	J	VIP Current Feedback Dual Op Amp	883/SMD	5962-9460301
LMC660AM	J	Low Power CMOS Quad Op Amp	883/SMD	5962-9209301
LMC662AM	J	Low Power CMOS Dual Op Amp	883/SMD	5962-9209401
LPC660AM	J	Micropower CMOS Quad Op Amp	883/SMD	5962-9209302
LPC662AM	J	Micropower CMOS Dual Op Amp	883/SMD	5962-9209402
LMC6482AM	J	Rail to Rail CMOS Dual Op Amp	883/SMD	5962-9453401
LMC6484AM	J	Rail to Rail CMOS Quad Op Amp	883/SMD	5962-9453402
OP07	H	Precision Op Amp	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
COMPARATORS				
LF111	H	Voltage Comparator	"-MIL"	—
LH2111	J, W	Dual Voltage Comparator	883/JAN	/10305
LM106	H, W	Voltage Comparator	883/SMD	8003701
LM111	J, H, E, W	Voltage Comparator	883/JAN	/10304
LM119	J, H, E, W	High Speed Dual Comparator	883/JAN	/10306
LM139	J, E, W	Quad Comparator	883/JAN	/11201
LM139A	J, E, W	Precision Quad Comparator	883/SMD	5962-87739
LM160	J, H	High Speed Differential Comparator	883/SMD	8767401
LM161	J, H, W	High Speed Differential Comparator	883/SMD	5962-87572
LM193	J, H	Dual Comparator	883	—
LM193A	J, H	Dual Comparator	883/JAN	/11202
LM612AM	J	Dual-Channel Comparator/Reference	883/SMD	5962-93002
LM613AM	J, E	Super-Block Dual Comparator/ Dual Op Amp/Adj Reference	883/SMD	5962-93003
LM615AM	J	Quad Comparator/Adjustable Reference	883	—
LM710A*	J, H, W	Voltage Comparator	883/JAN	/10301
LM711A*	J, H, W	Dual LM710	883/JAN	/10302
LM760	J, H	High Speed Differential Comparator	883/SMD	5962-87545

*Formerly manufactured by Fairchild Semiconductor as part numbers μA710 and μA711.

LINEAR REGULATORS				
Positive Voltage Regulators				
LM105	H	Adjustable Voltage Regulator	883/SMD	5962-89588
LM109	H	5V Regulator, I_O = 20 mA	883/JAN	/10701BXA
LM109	K	5V Regulator, I_O = 1A	883/JAN	/10701BYA
LM117	H, E, K	Adjustable Regulator	883/JAN	/11703, /11704
LM117HV	H	Adjustable Regulator, I_O = 0.5A	883/SMD	7703402XA
LM117HV	K	Adjustable Regulator, I_O = 1.5A	883/SMD	7703402YA
LM123	K	3A Voltage Regulator	883	—
LM138	K	5A Adjustable Regulator	"-MIL"	—
LM140-5.0	H	0.5A Fixed 5V Regulator	883/JAN	/10702
LM140-6.0	H	0.5A Fixed 6V Regulator	883	—
LM140-8.0	H	0.5A Fixed 8V Regulator	883	—
LM140-12	H	0.5A Fixed 12V Regulator	883/JAN	/10703
LM140-15	H	0.5A Fixed 15V Regulator	883/JAN	/10704
LM140-24	H	0.5A Fixed 24V Regulator	883	—
LM140A-5.0	K	1.0A Fixed 5V Regulator	883	—
LM140A-12	K	1.0A Fixed 12V Regulator	883	—
LM140A-15	K	1.0A Fixed 15V Regulator	883	—
LM140K-5.0	K	1.0A Fixed 5V Regulator	883/JAN	/10706
LM140K-12	K	1.0A Fixed 12V Regulator	883/JAN	/10707
LM140K-15	K	1.0A Fixed 15V Regulator	883/JAN	/10708
LM140LAH-5.0	H	100 mA Fixed 5V Regulator	883	—
LM140LAH-12	H	100 mA Fixed 12V Regulator	883	—
LM140LAH-15	H	100 mA Fixed 15V Regulator	883	—
LM150	K	3A Adjustable Power Regulator	883	—
LM2940-5.0	K	5V Low Dropout Regulator	883/SMD	5962-89587
LM2940-8.0	K	8V Low Dropout Regulator	883/SMD	5962-90883
LM2940-12	K	12V Low Dropout Regulator	883/SMD	5962-90884
LM2940-15	K	15V Low Dropout Regulator	883/SMD	5962-90885
LM2941	K	Adjustable Low Dropout Regulator	883/SMD	TBD
LM431	H, K	Adjustable Shunt Regulator	883	—
LM723	H, J, E	Precision Adjustable Regulator	883/JAN	/10201
LP2951	H, E, J	Adjustable Micropower LDO	883/SMD	5962-38705
LP2953AM	J	250 mA Adj. Micropower LDO	883/SMD	5962-9233601

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
LINEAR REGULATORS (Continued)				
Negative Voltage Regulators				
LM120-5.0	H	Fixed 0.5A Regulator, $V_{OUT} = -5V$	883/JAN	/11501
LM120-8.0	H	Fixed 0.5A Regulator, $V_{OUT} = -8V$	883	—
LM120-12	H	Fixed 0.5A Regulator, $V_{OUT} = -12V$	883/JAN	/11502
LM120-15	H	Fixed 0.5A Regulator, $V_{OUT} = -15V$	883/JAN	/11503
LM120-5.0	K	Fixed 1.0A Regulator, $V_{OUT} = -5V$	883/JAN	/11505
LM120-12	K	Fixed 1.0A Regulator, $V_{OUT} = -12V$	883/JAN	/11506
LM120-15	K	Fixed 1.0A Regulator, $V_{OUT} = -15V$	883/JAN	/11507
LM137A	H	Precision Adjustable Regulator	883/SMD	7703406XA
LM137A	K	Precision Adjustable Regulator	883/SMD	7703406YA
LM137	H, K	Adjustable Regulator	883/JAN	/11803, /11804
LM137HV	H	Adjustable (High Voltage) Regulator	883/SMD	7703404XA
LM137HV	K	Adjustable (High Voltage) Regulator	883/SMD	7703404YA
LM145-5.0	K	Negative 3 Amp Regulator	883/SMD	5962-90645
LM145-5.2	K	Negative 3 Amp Regulator	883	—
SWITCHING REGULATORS				
LM1575-5	J, K	Simple Switcher™ Step-Down, $V_{OUT} = 5V$	883/SMD	5962-9167201
LM1575-12	J, K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	5962-9167301
LM1575-15	J, K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	5962-9167401
LM1575-ADJ	J, K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	5962-9167101
LM1575HV-5	K	Simple Switcher Step-Down, $V_{OUT} = 5V$	883	—
LM1575HV-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883	—
LM1575HV-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883	—
LM1575HV-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883	—
LM1577-12	K	Simple Switcher Step-Up, $V_{OUT} = 12V$	883/SMD	5962-9216701
LM1577-15	K	Simple Switcher Step-Up, $V_{OUT} = 15V$	883/SMD	5962-9216801
LM1577-ADJ	K	Simple Switcher Step-Up, Adj V_{OUT}	883/SMD	5962-9216601
LM1578	H	750 mA Switching Regulator	883/SMD	5962-89586
LM78S40*	J	Universal Switching Regulator Subsystem	883/SMD	5962-88761
VOLTAGE REFERENCES				
LM103-3.0	H	Reference Diode, BV = 3.0V	883/SMD	7702806
LM103-3.3	H	Reference Diode, BV = 3.3V	883/SMD	7702807
LM103-3.6	H	Reference Diode, BV = 3.6V	883/SMD	7702808
LM103-3.9	H	Reference Diode, BV = 3.9V	883/SMD	7702809
LM113	H	Reference Diode with 5% Tolerance	883/SMD	5962-8671101
LM113-1	H	Reference Diode with 1% Tolerance	883/SMD	5962-8671102
LM113-2	H	Reference Diode with 2% Tolerance	883/SMD	5962-8671103
LM129A	H	Precision Reference, 10 ppm/°C Drift	883/SMD	5962-8992101XA
LM129B	H	Precision Reference, 20 ppm/°C Drift	883/SMD	5962-8992102XA
LM136A-2.5	H	2.5V Reference Diode, 1% V_{OUT} Tolerance	883	—
LM136A-5.0	H	5V Reference Diode, 1% V_{OUT} Tolerance	883/SMD	8418001
LM136-2.5	H	2.5V Reference Diode, 2% V_{OUT} Tolerance	883	—
LM136-5.0	H	5V Reference Diode, 2% V_{OUT} Tolerance	883	—

*Formerly manufactured by Fairchild Semiconductor as the μA78S40DMQB.

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
VOLTAGE REFERENCES (Continued)				
LM169	H	10V Precision Reference, Low Tempco 0.05% Tolerance	883	—
LM185B	H, E	Adjustable Micropower Voltage Reference	883/SMD	5962-9041401
LM185BX2.5	H	2.5V Micropower Reference Diode, Ultralow Drift	883/SMD	5962-8759404
LM185BY	H	Adjustable Micropower Voltage Reference	883	—
LM185BY1.2	H	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759405
LM185BY2.5	H	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759406
LM185-1.2	H, E	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759401
LM185-2.5	H, E	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759402
LM199	H	Precision Reference, Low Tempco	883/SMD	5962-8856102
LM199A	H	Precision Reference, Ultralow Tempco	883/SMD	5962-8856101
LM199A-20	H	Precision Reference, Ultralow Tempco	883	—
LM611AM	J	Super-Block Op Amp/Reference	883	—
LM612AM	J	Super-Block Dual-Channel Comparator/Reference	883/SMD	5962-9300201
LM613AM	J, E	Super-Block Dual Op Amp/DualComp/Dual Ref	883/SMD	5962-9300301
LM614AM	J	Super-Block Quad Op Amp/Reference	883/SMD	5962-9300401
LM615AM	J	Super-Block Quad Comparator/Reference	883/SMD	TBD
LH0070-0	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-1	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-2	H	Precision BCD Buffered Reference	"-MIL"	—
DATA ACQUISITION				
ADC08020L	J	8-Bit μP-Compatible	883/SMD	5962-90966
ADC0851	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC0858	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC08061CM	J	8-Bit Multistep ADC	883/SMD	TBD
ADC10061CM	J	10-Bit Multistep ADC	883/SMD	TBD
ADC10062CM	J	10-Bit Multistep ADC w/Dual Input Mutiplexer	883/SMD	TBD
ADC10064CM	J	10-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC1241CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	5962-9157801
ADC12441CM	J	Dynamically-Tested ADC1241	883/SMD	5962-9157802
ADC1251CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	5962-9157801
ADC12451CM	J	Dynamically-Tested ADC1251	883/SMD	TBD
DAC0854CM	J	Quad 8-Bit D/A Converter with Read Back	883/SMD	TBD
DAC1054CM	J	Quad 10-Bit D/A Converter with Read Back	883/SMD	TBD
LM12458M	EL, W	12-Bit Data Acquisition System	883/SMD	5962-9319501
LM12H458M	EL, W	12-Bit Data Acquisition System	883/SMD	5962-9319502

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
DATA ACQUISITION SUPPORT				
Switched Capacitor Filters				
LMF60CMJ50	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF60CMJ100	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF90CM	J	4th Order Elliptic Notch	883/SMD	5962-90968
LMF100A	J, E	Dual 2nd Order General Purpose	883/SMD	5962-9153301
Sample and Hold				
LF198	H	Monolithic Sample and Hold	SMD/JA	5962-87608 /12501
Motion Control				
LMD18200-2	D	Dual 3A, 55V H-Bridge	883/JAN	5962-9232501

Note 1: D: Side-Brazed DIP
E: Leadless Ceramic Chip Carrier
G: Metal Can (TO-8)
H: Metal Can (TO-39, TO-5, TO-99, TO-100)
J: Ceramic DIP
K: Metal Can (TO-3)
W: Flatpak

Note 2: Process Flows
JAN = JM38510, Level B
SMD = Standard Military Drawing
883 = MIL-STD-883 Rev C
-MIL = Exceptions to 883C noted on Certificate of Conformance

Note 3: Please call your local sales office to determine price and availability of space-level products. All "LM" prefix products in this guide are availble with space-level processing.

National Semiconductor

Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

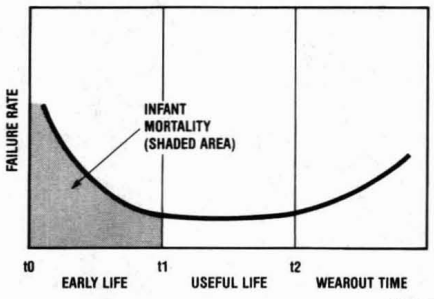


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

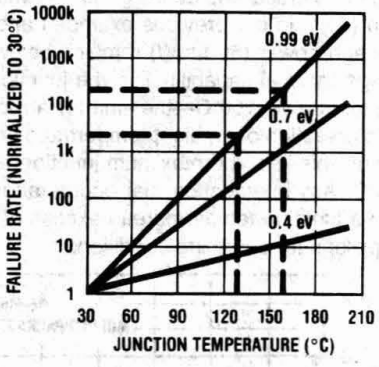

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

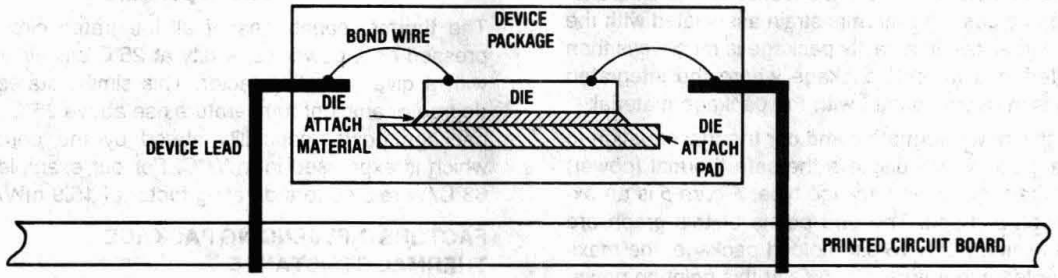

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

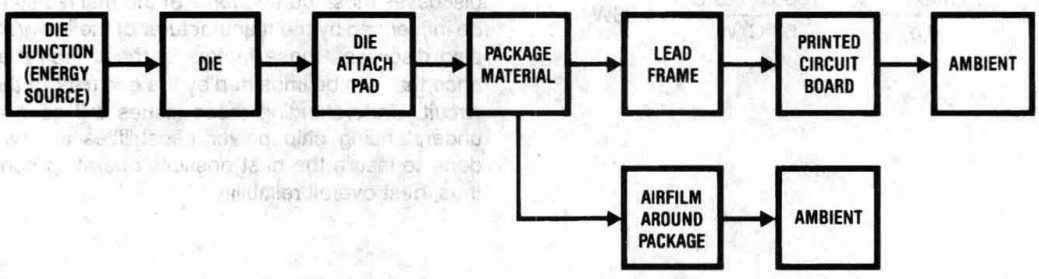

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

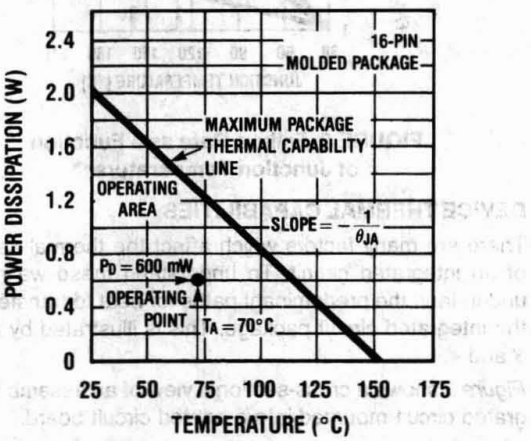

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

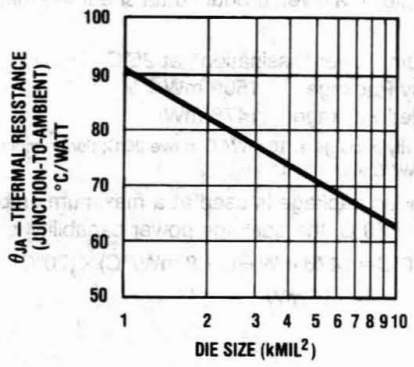

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

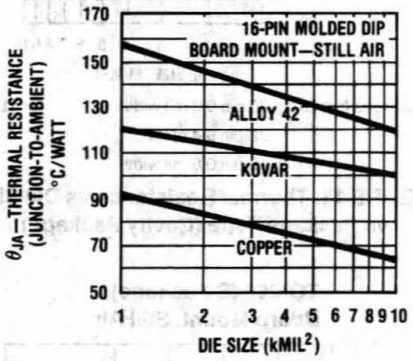

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

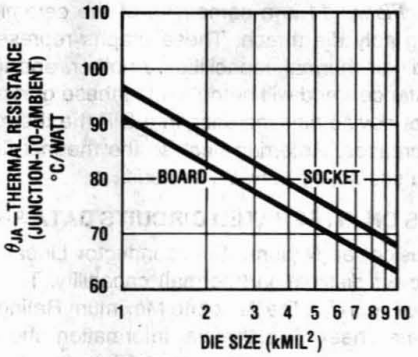

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

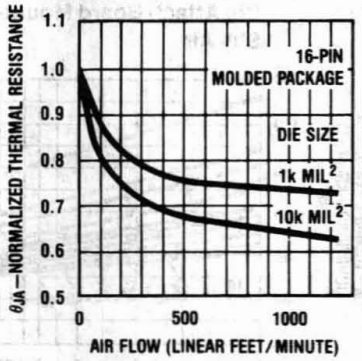

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

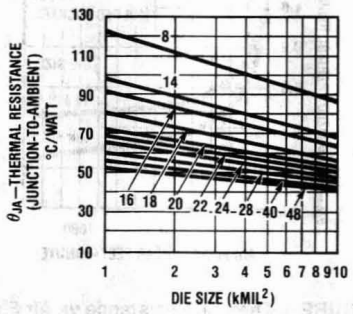
Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded

package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTEGRATED CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

Molded (N Package) DIP*
Copper Leadframe—HTP Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Surface Mount (M, MW Packages), Board Mount, Still Air

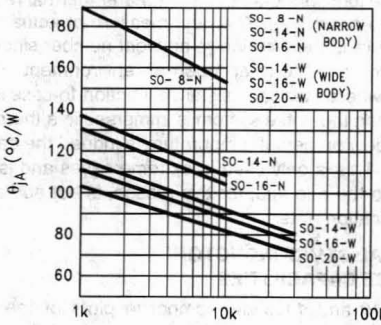

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FIGURE 12. Thermal Resistance for "SO" Packages (Board Mount)

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

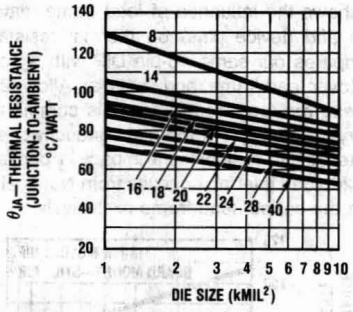
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70°C = 1476\ mW - (11.8\ mW/°C) \times (70°C - 25°C)$$
$$\doteq 945\ mW$$

Cavity (J Package) DIP*
Poly Die Attach Board Mount—Still Air

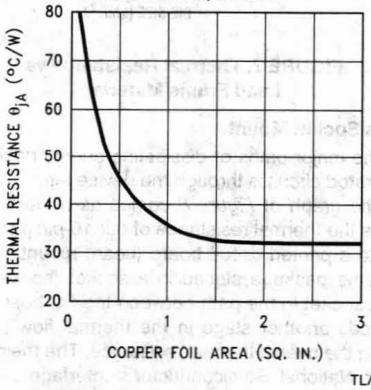


*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/H/9312–11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

TO-263 (S Package)
Board Mount, Still Air



TL/H/9312–13

*For products with high current ratings (>3A), thermal resistance may be lower. Consult product datasheet for more information.

FIGURE 13. Thermal Resistance (typ.*) for 3-, 5-, and 7-L TO-263 packages mounted on 1 oz. (0.036mm) PC board foil

National Semiconductor

APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, **Note 6**)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	5V ≤ V_S ≤ 30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	4V ≤ V_S ≤ 30V, +77°F	+0.5	2.0		0.5	2.0		µA
	5V ≤ V_S ≤ 30V	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: −50°F ≤ T_j ≤ + 300°F for the LM34 and LM34A; −40°F ≤ T_j ≤ +230°F for the LM34C and LM34CA; and +32°F ≤ T_j ≤ + 212°F for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2*; +6 Vdc for LM34 and LM34A for 230°F ≤ T_j ≤ 300°F. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1*.

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

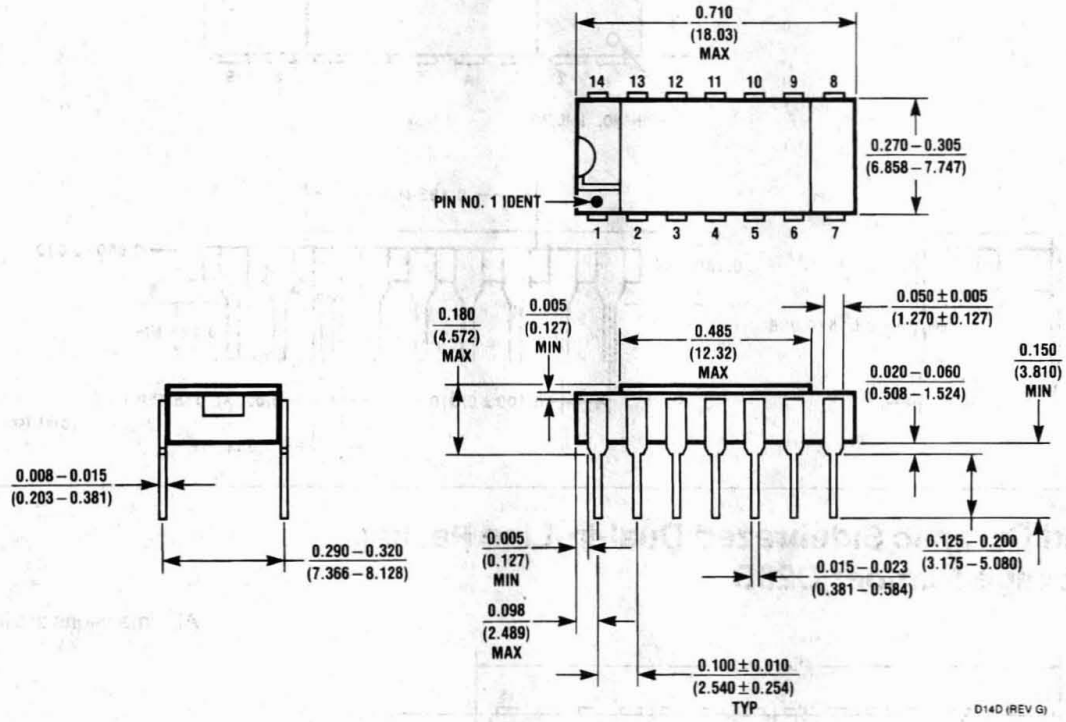
The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

National Semiconductor

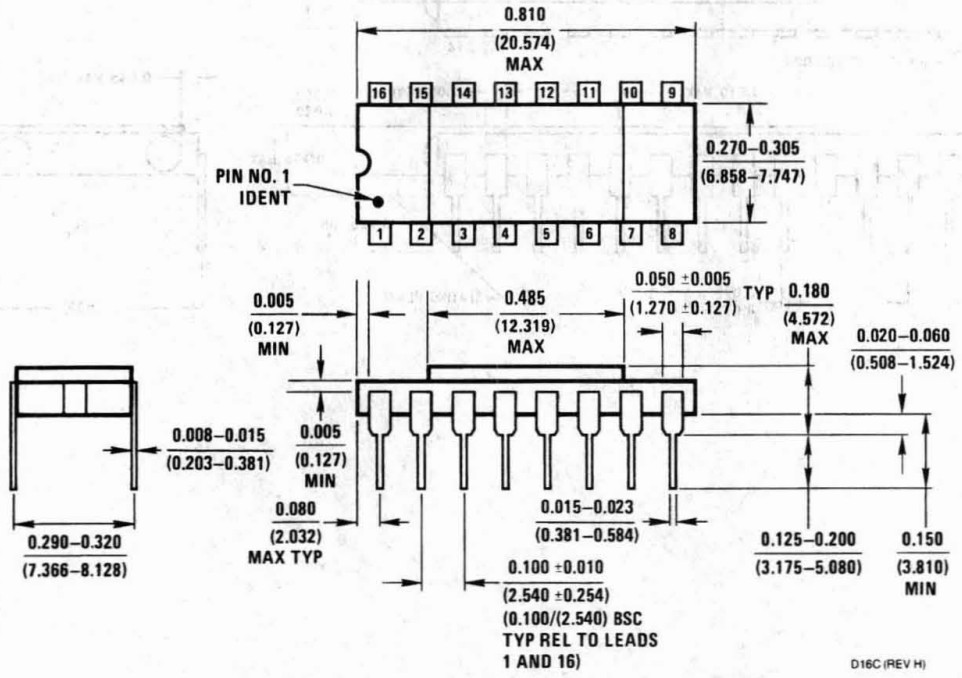
14 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D14D

All dimensions are in inches (millimeters)



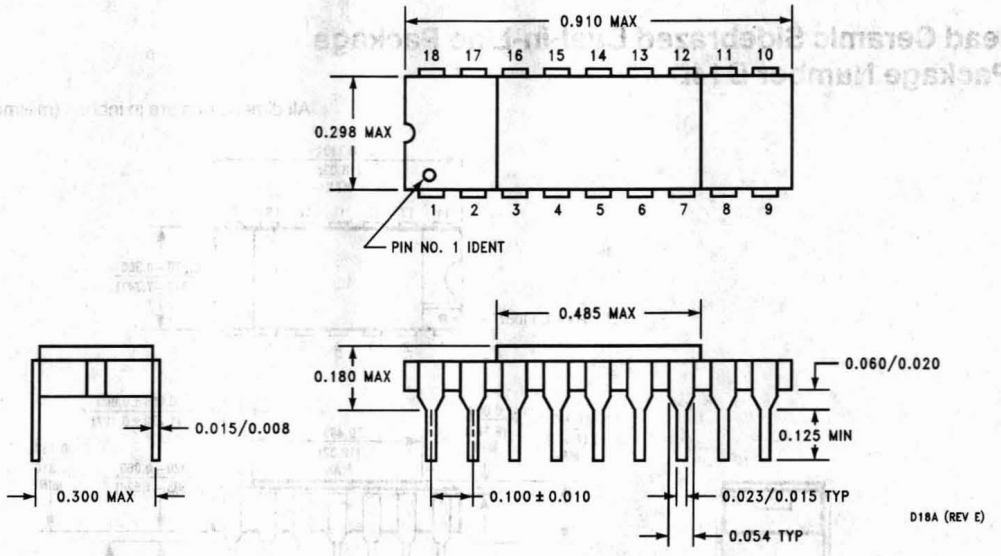
16 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D16C

All dimensions are in inches (millimeters)



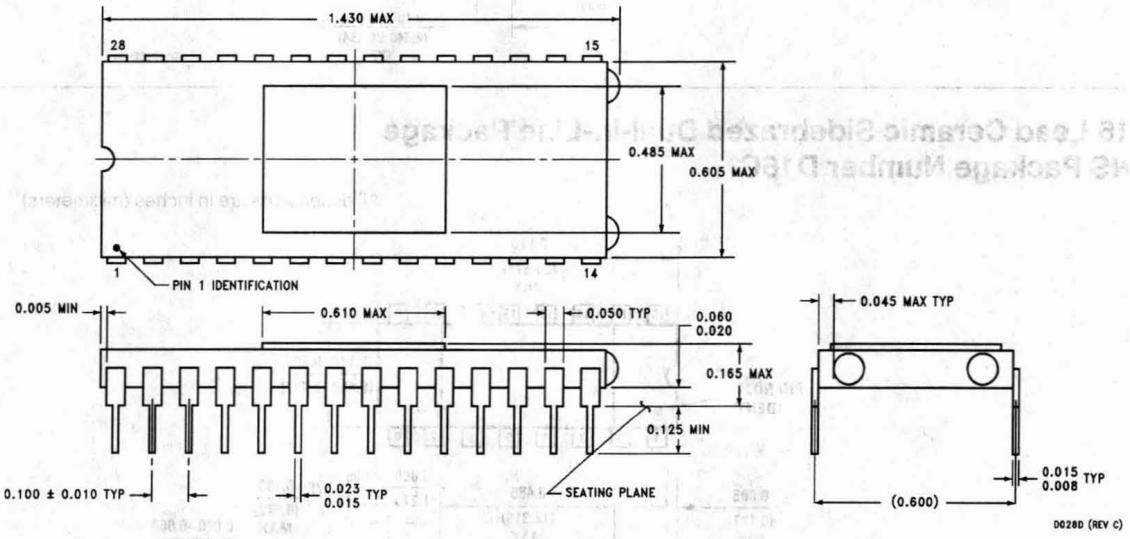
18 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D18A

All dimensions are in inches



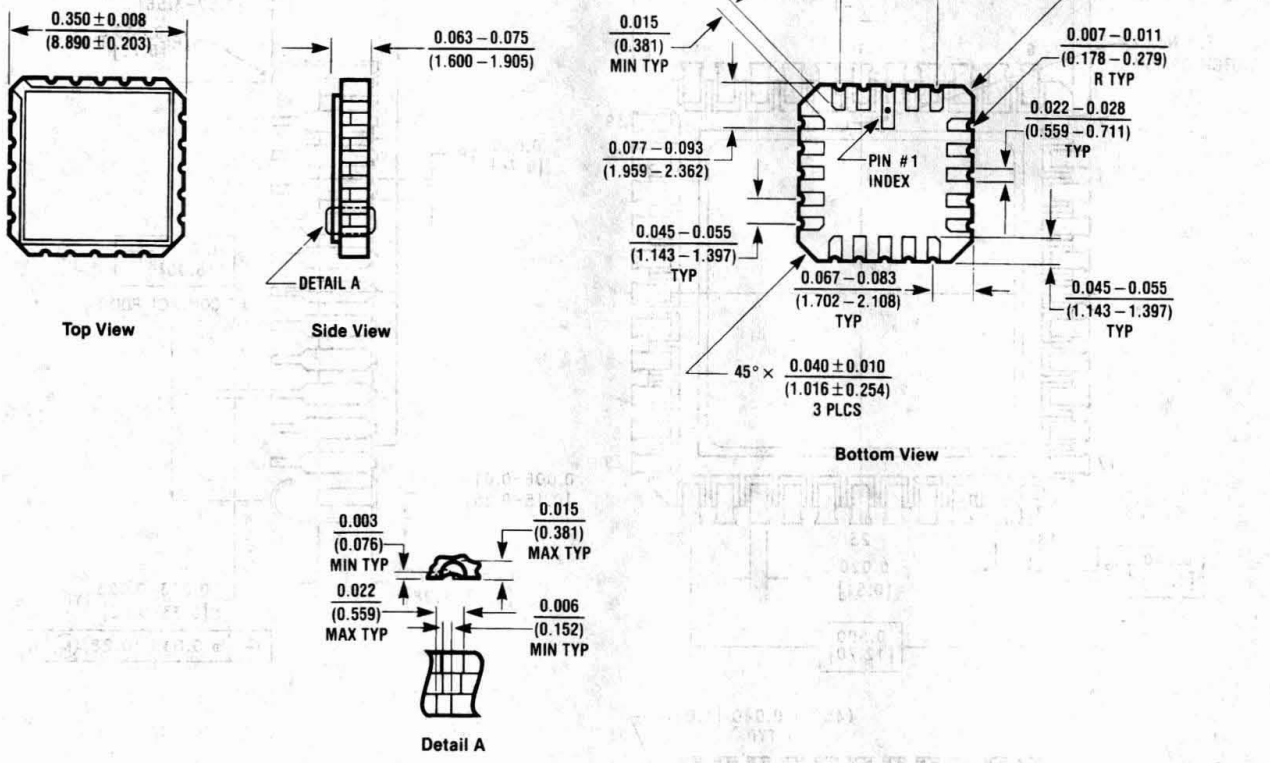
28 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D28D

All dimensions are in inches



20 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E20A

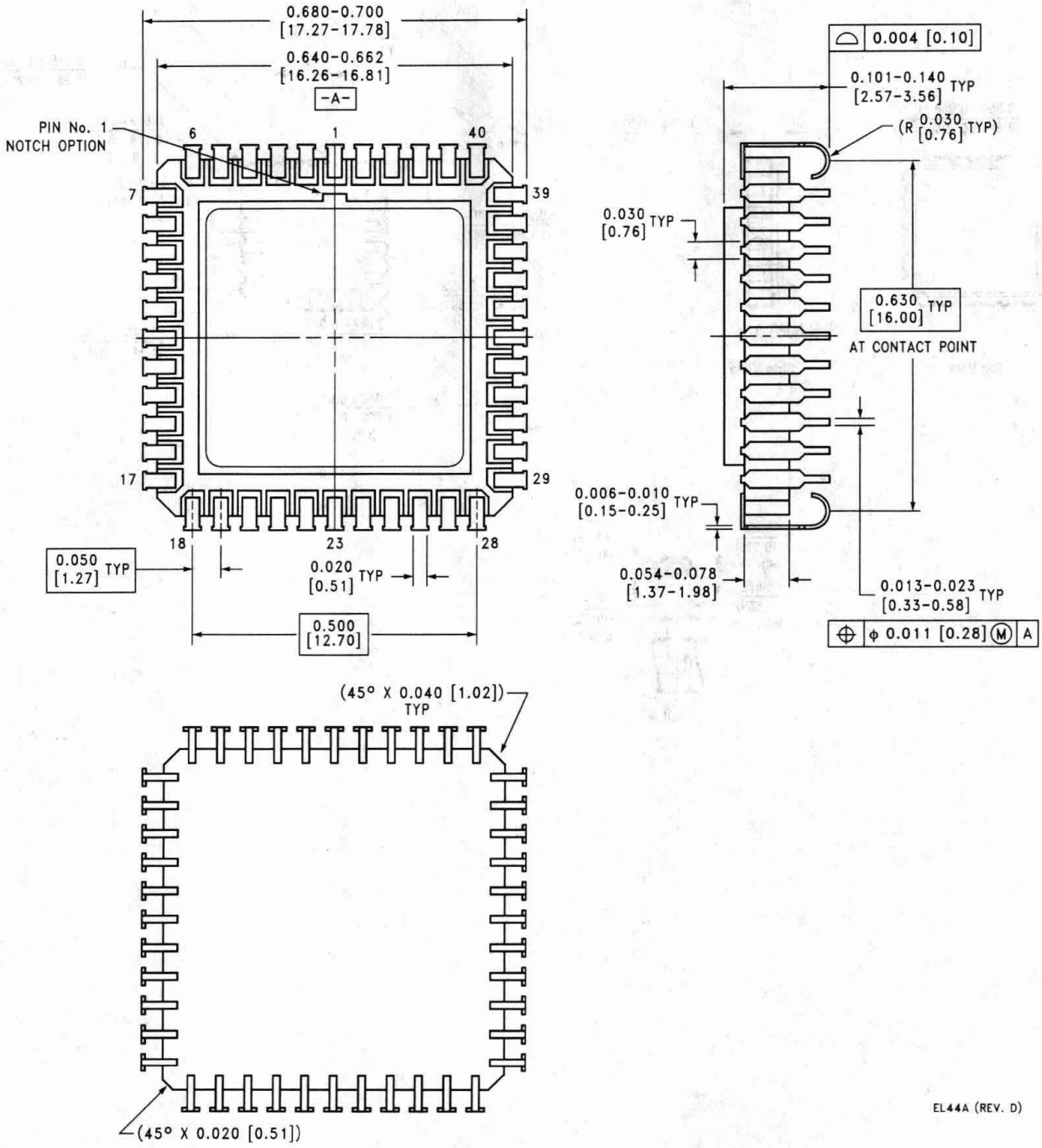
All dimensions are in inches (millimeters)



E20A (REV D)

44 Lead Ceramic Quad J-Bend
NS Package Number EL44A

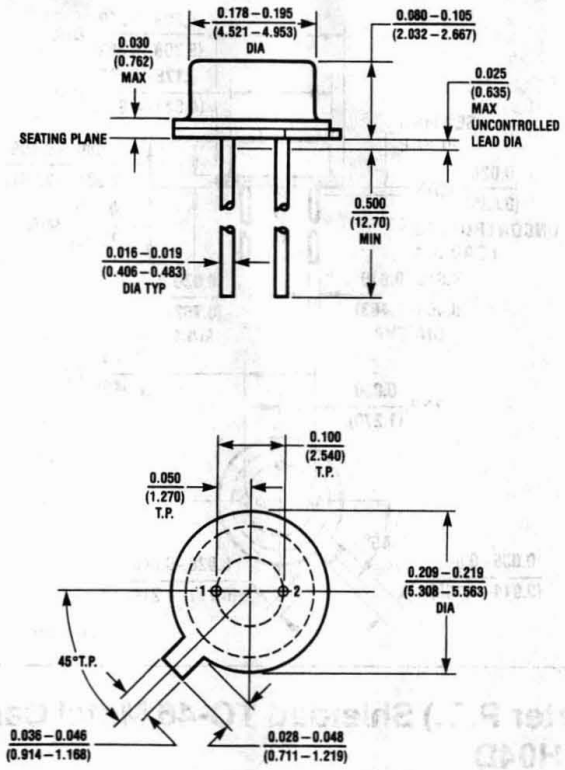
All dimensions are in inches [millimeters]



EL44A (REV. D)

2 Lead (0.100″ Diameter P.C.) TO-46 Metal Can Package
NS Package Number H02A

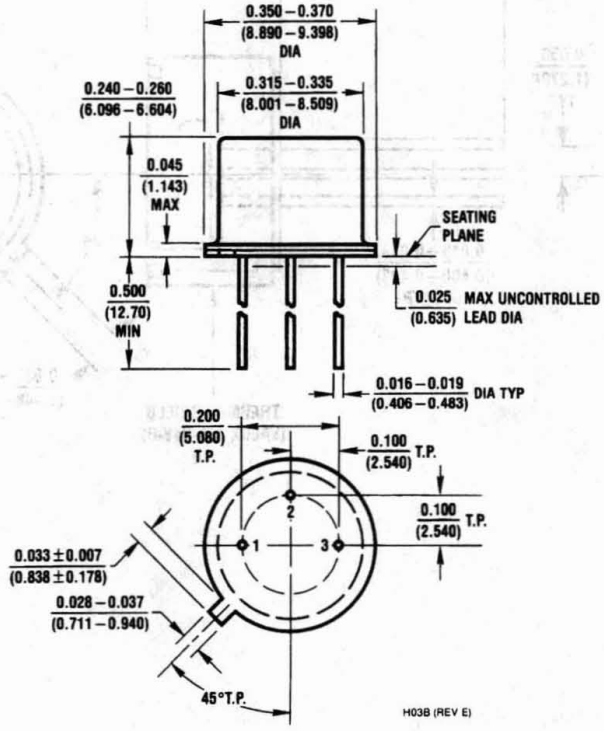
All dimensions are in inches (millimeters)



H02A (REV C)

3 Lead (0.200″ Diameter P.C.) TO-39 Metal Can Package, High Profile
NS Package Number H03B

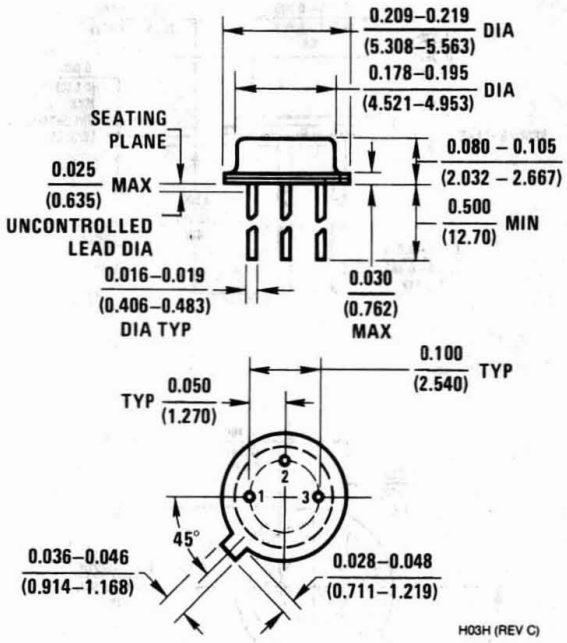
All dimensions are in inches (millimeters)



H03B (REV E)

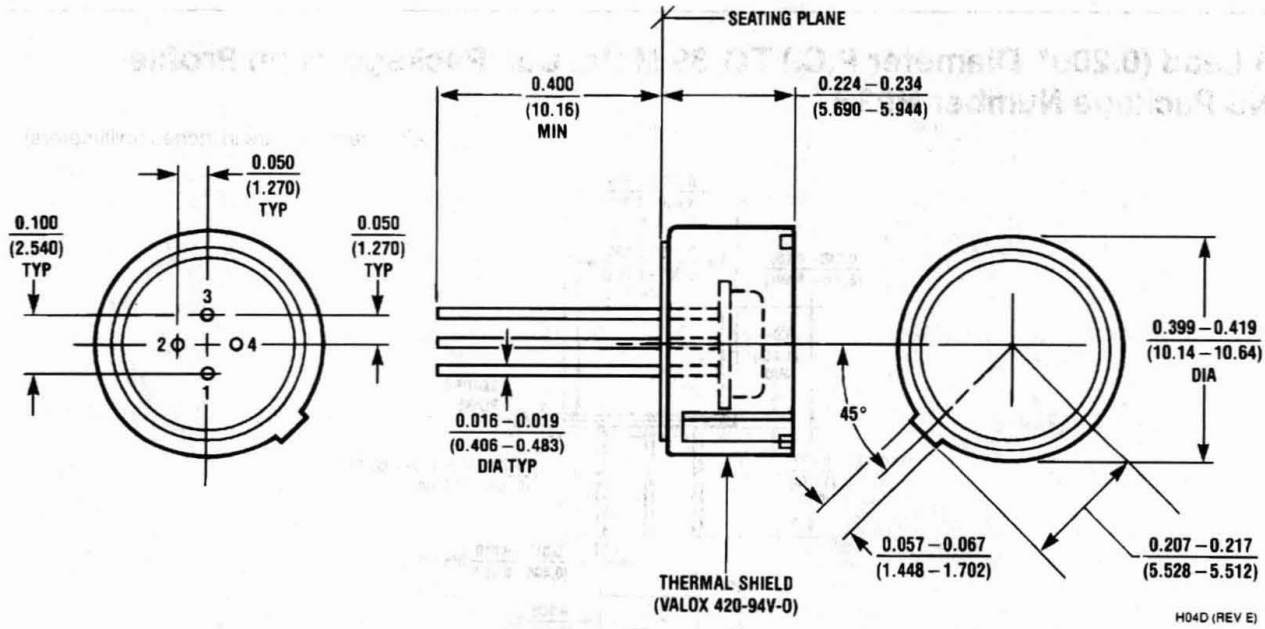
3 Lead (0.100″ Diameter P.C.) TO-46 Metal Can Package
NS Package Number H03H

All dimensions are in inches (millimeters)



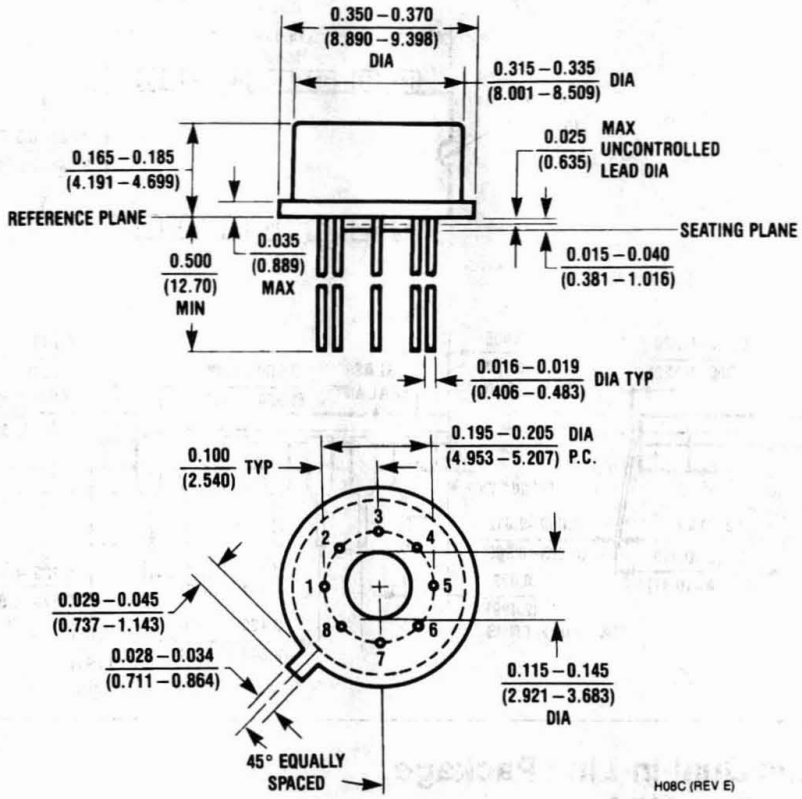
4 Lead (0.100″ Diameter P.C.) Shielded TO-46 Metal Can Package
NS Package Number H04D

All dimensions are in inches (millimeters)



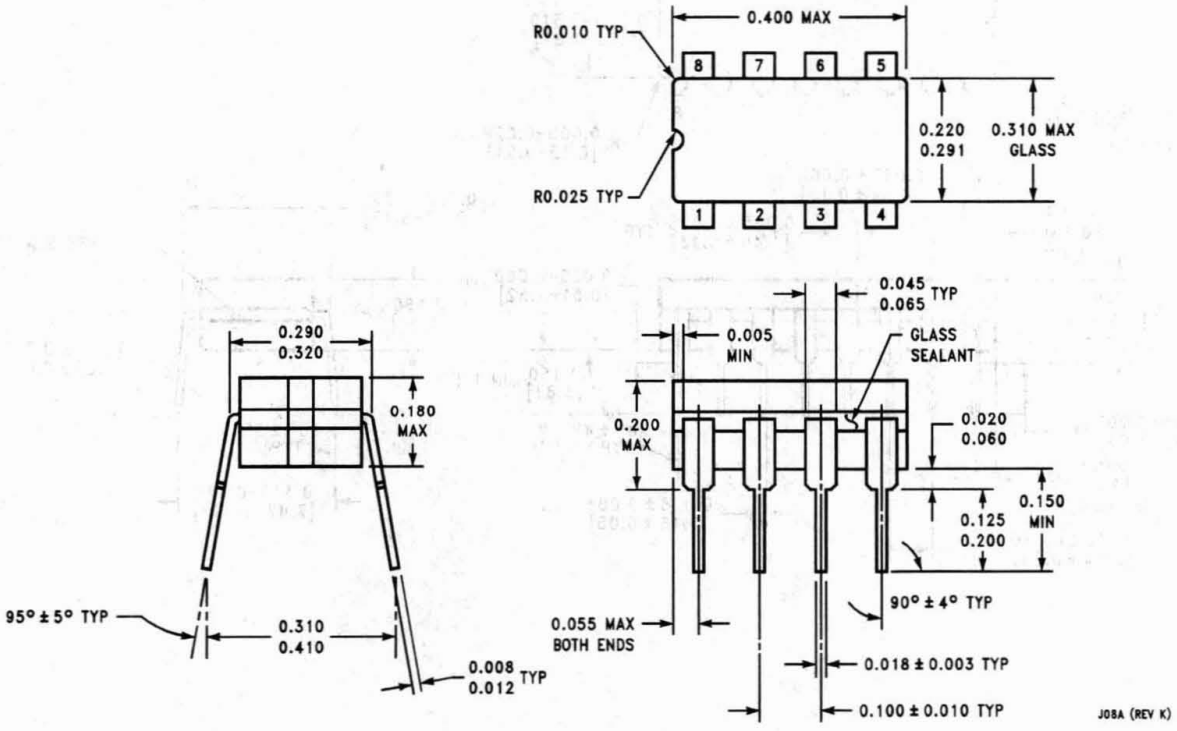
8 Lead (0.200" Diameter P.C.) TO-5 Metal Can Package
NS Package Number H08C

All dimensions are in inches (millimeters)



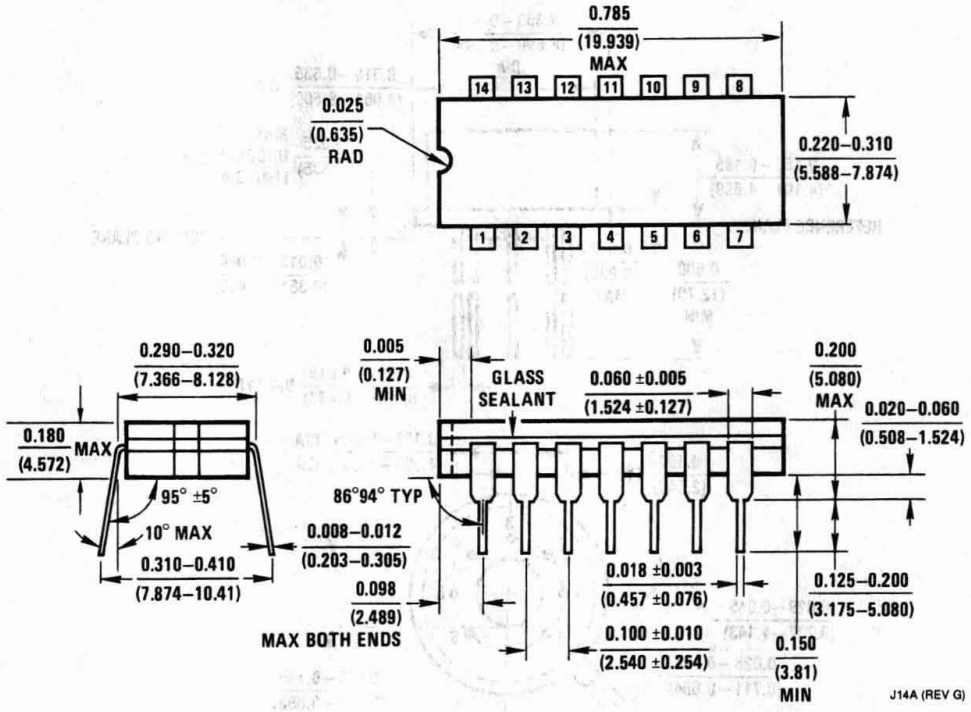
8 Lead Ceramic Dual-in-Line Package
NS Package Number J08A

All dimensions are in inches



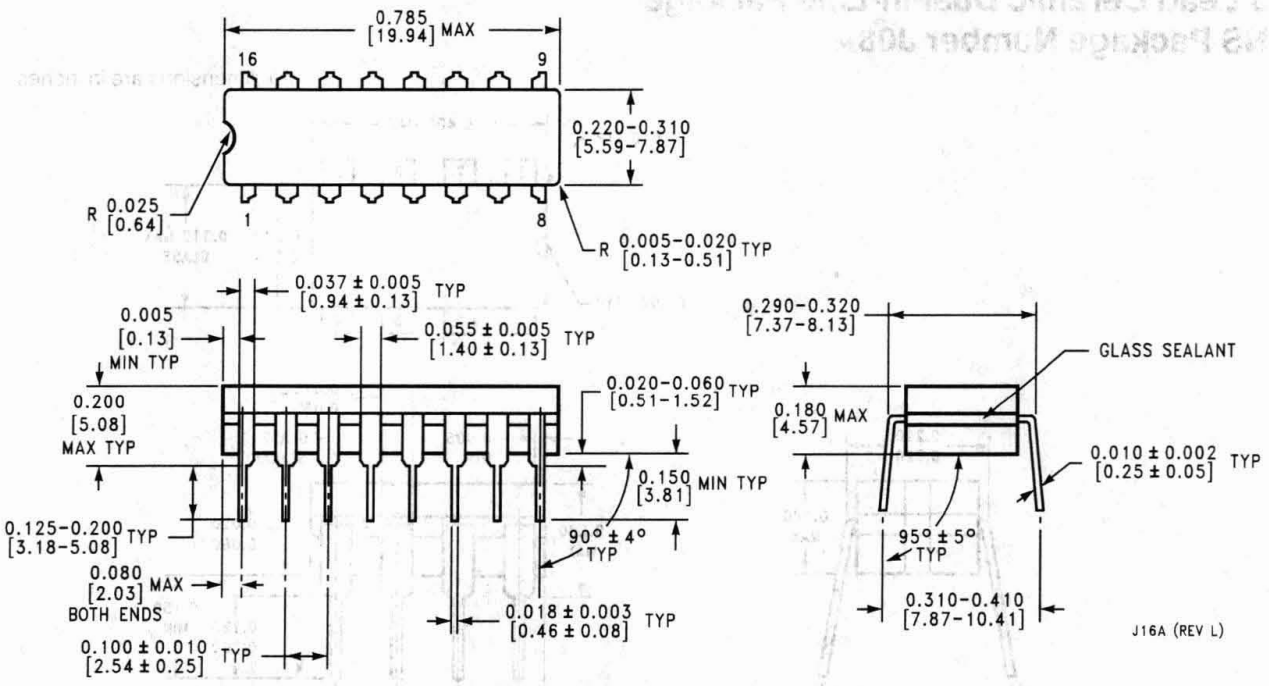
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A

All dimensions are in inches (millimeters)



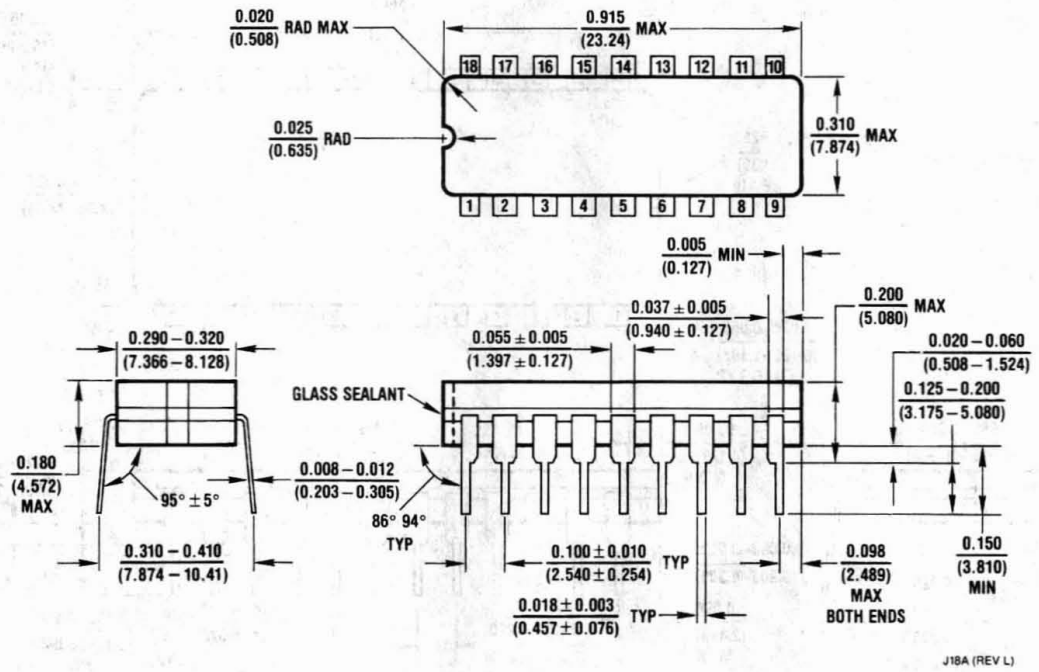
16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A

All dimensions are in inches [millimeters]



18 Lead Ceramic Dual-in-Line Package
NS Package Number J18A

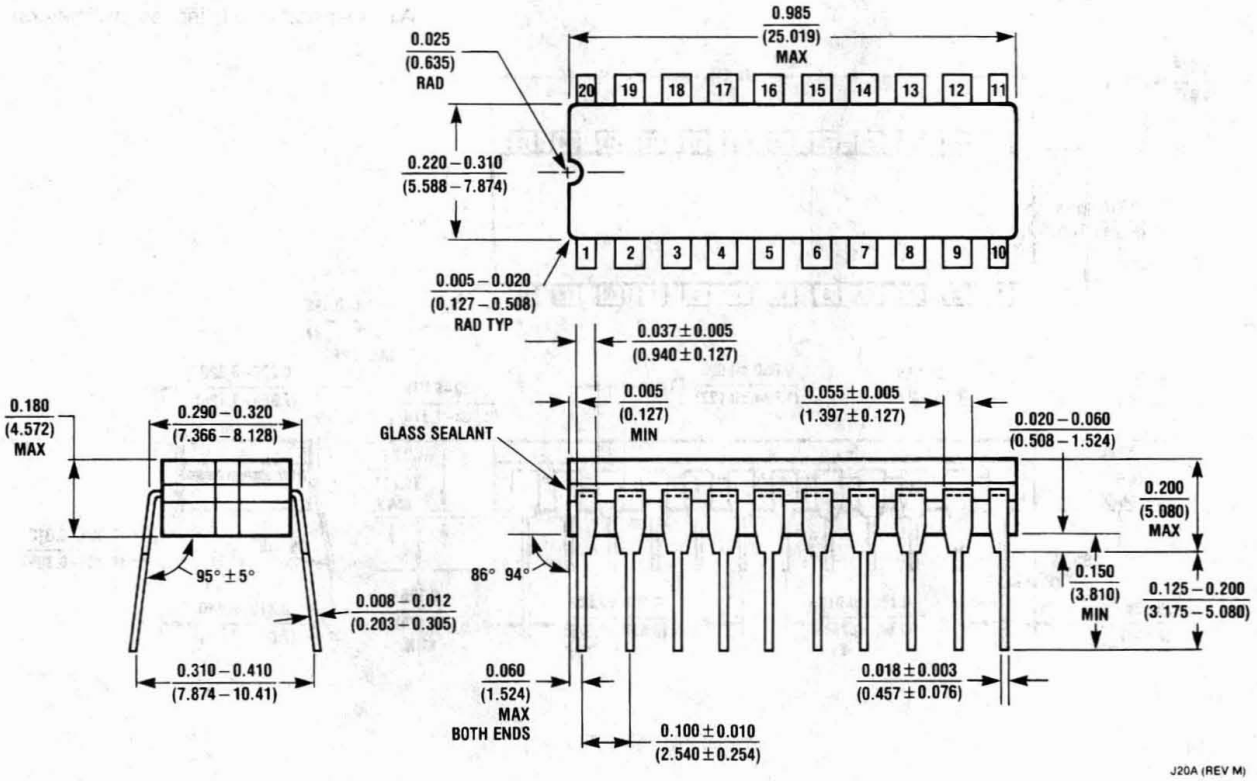
All dimensions are in inches (millimeters)



J18A (REV L)

20 Lead Ceramic Dual-in-Line Package
NS Package Number J20A

All dimensions are in inches (millimeters)

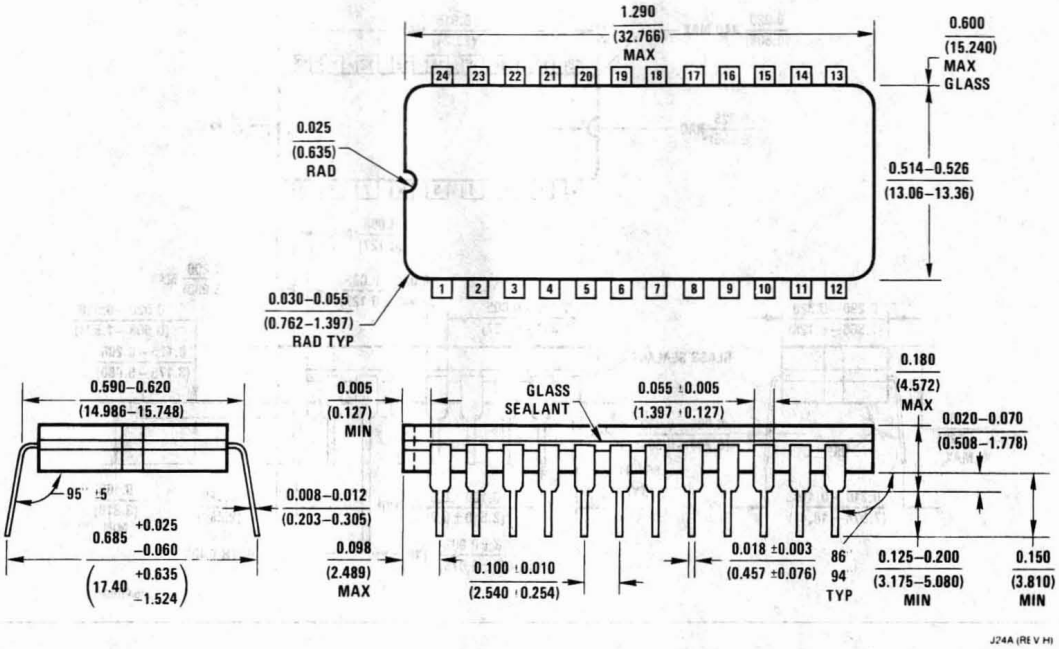


J20A (REV M)

10

24 Lead Ceramic Dual-in-Line Package
NS Package Number J24A

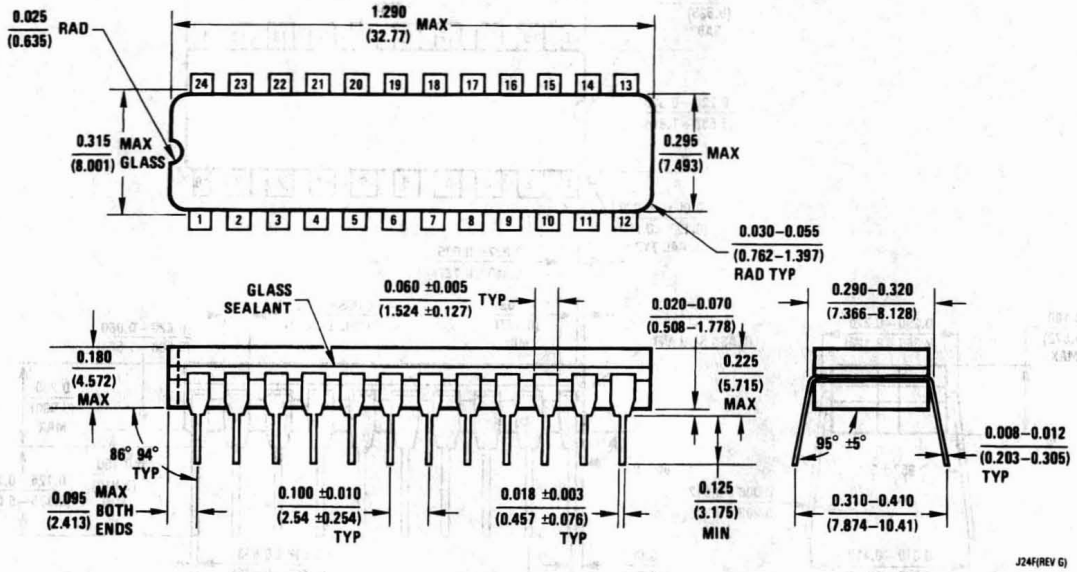
All dimensions are in inches (millimeters)



J24A (REV H)

24 Lead (0.300″ Wide) Ceramic Dual-in-Line Package
NS Package Number J24F

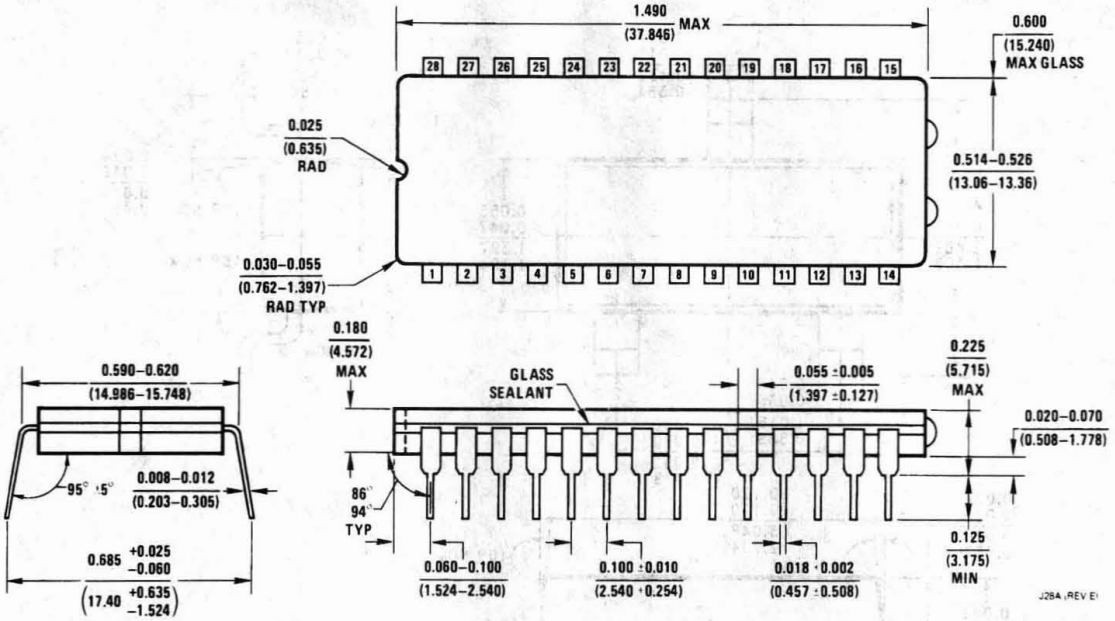
All dimensions are in inches (millimeters)



J24F(REV G)

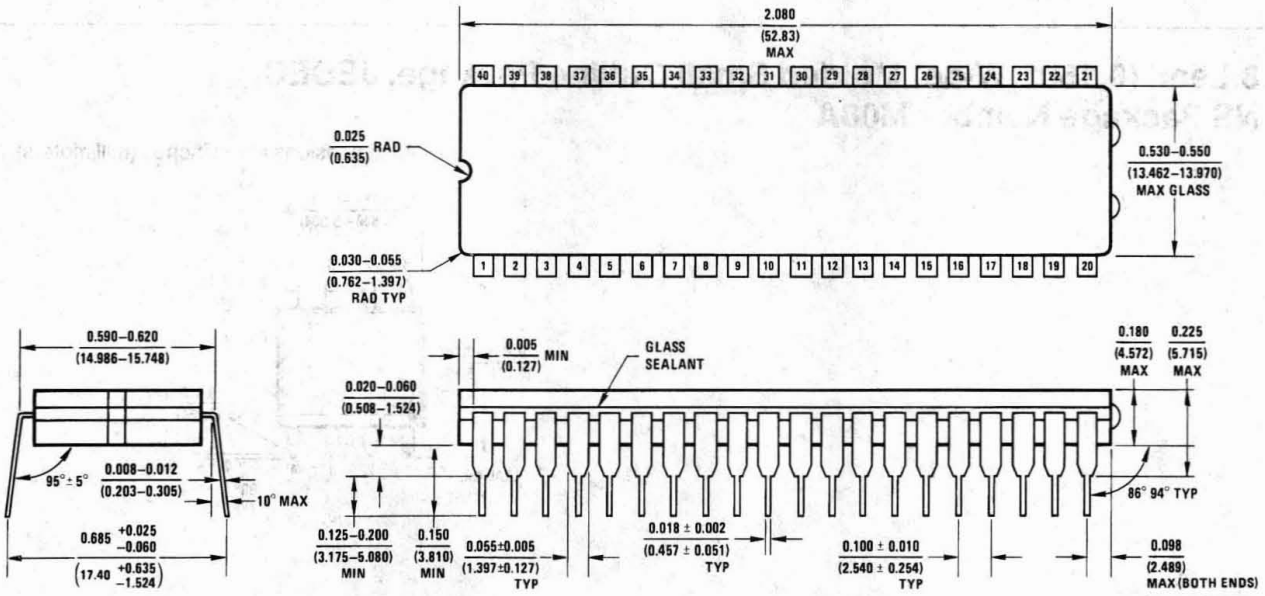
28 Lead Ceramic Dual-in-Line Package
NS Package Number J28A

All dimensions are in inches (millimeters)



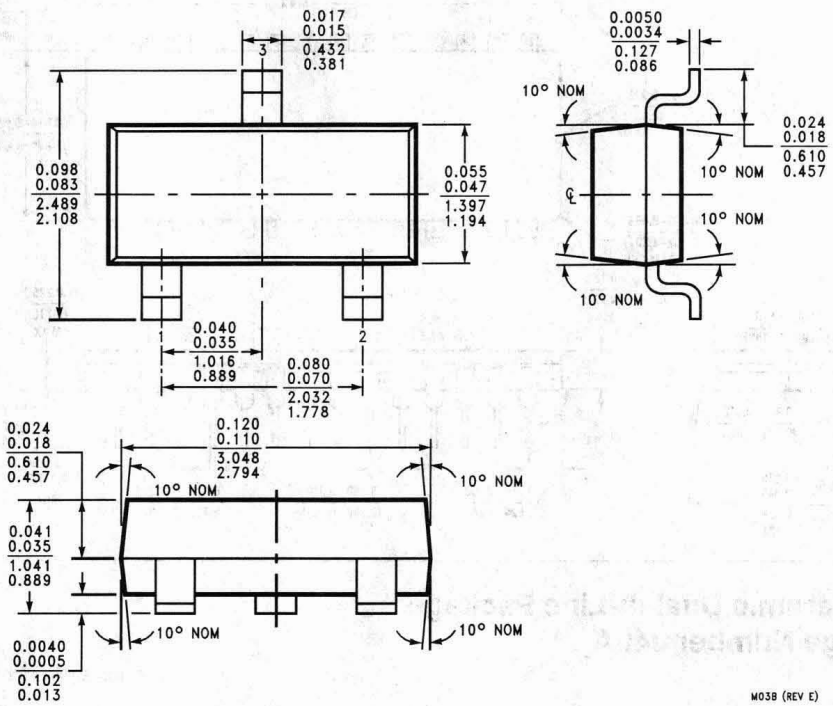
40 Lead Ceramic Dual-in-Line Package
NS Package Number J40A

All dimensions are in inches (millimeters)



3 Lead Molded SOT-23, Low Profile
NS Package Number M03B

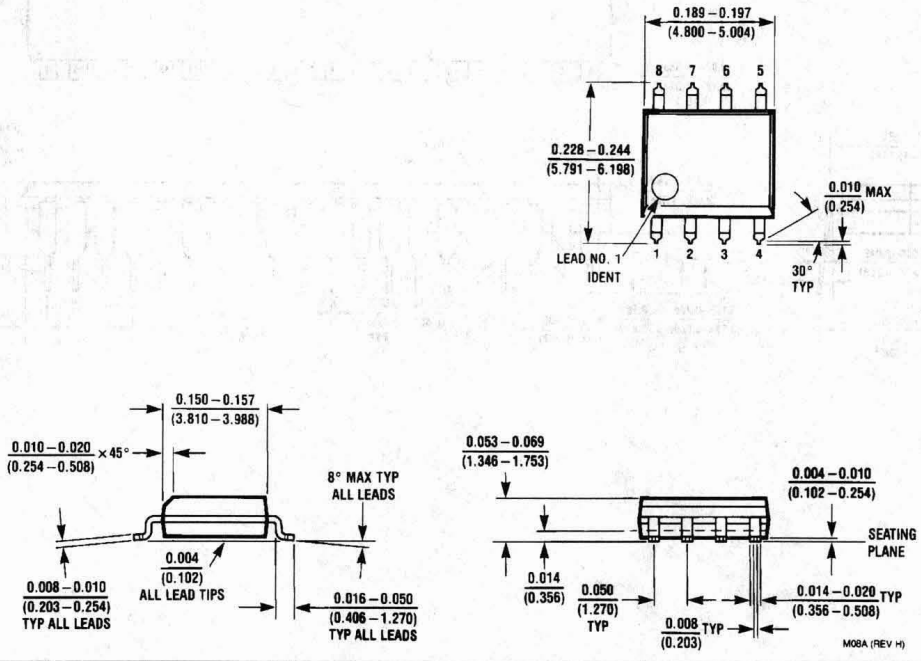
All dimensions are in inches / millimeters



M03B (REV E)

8 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

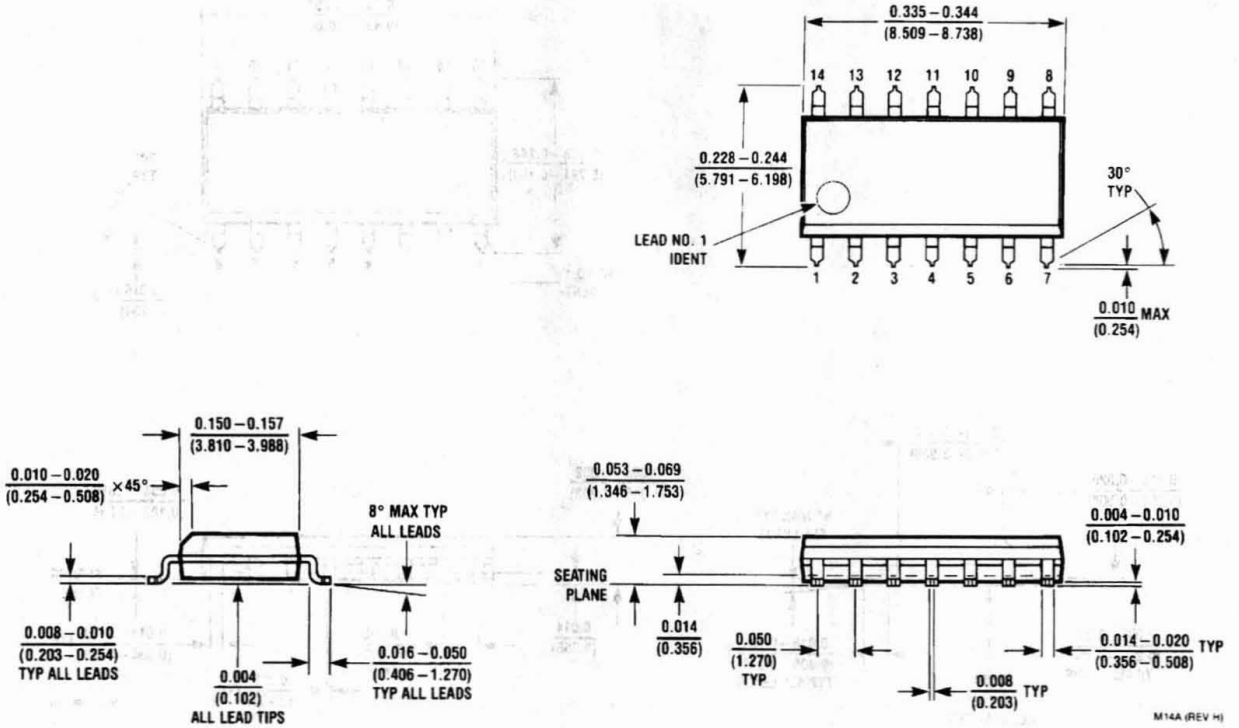
All dimensions are in inches (millimeters)



M08A (REV H)

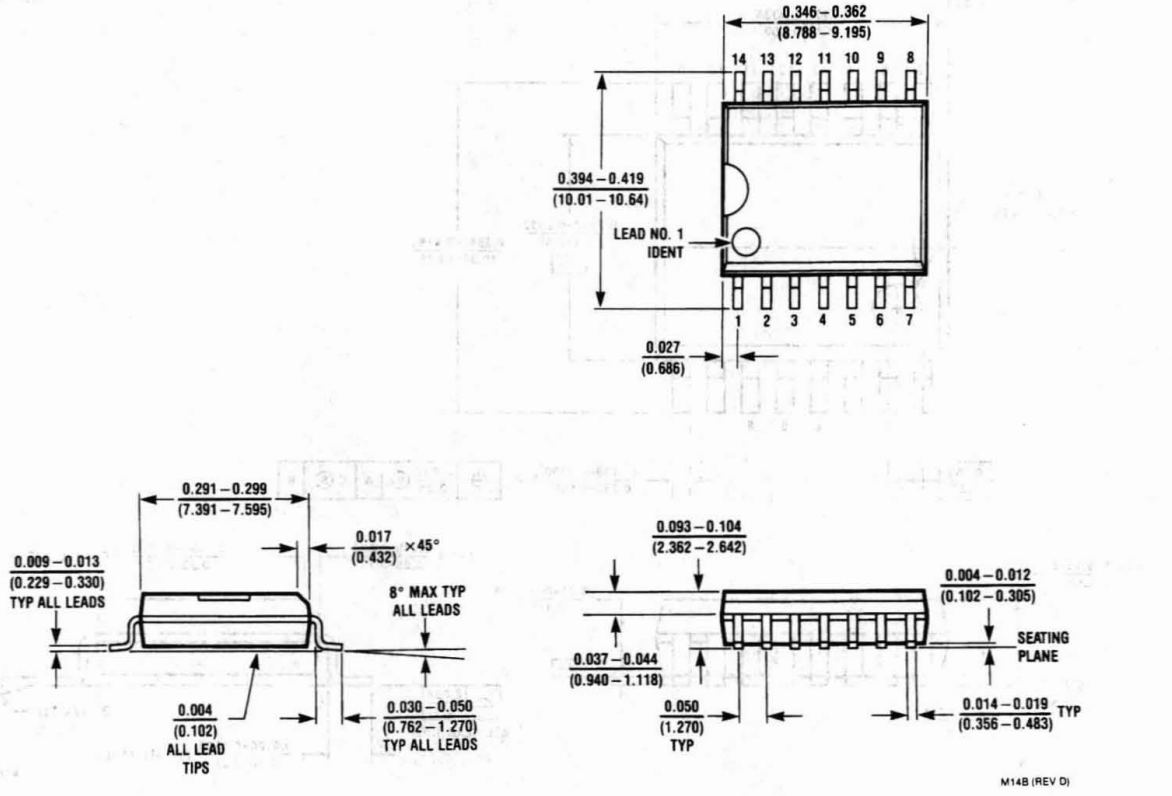
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A

All dimensions are in inches (millimeters)



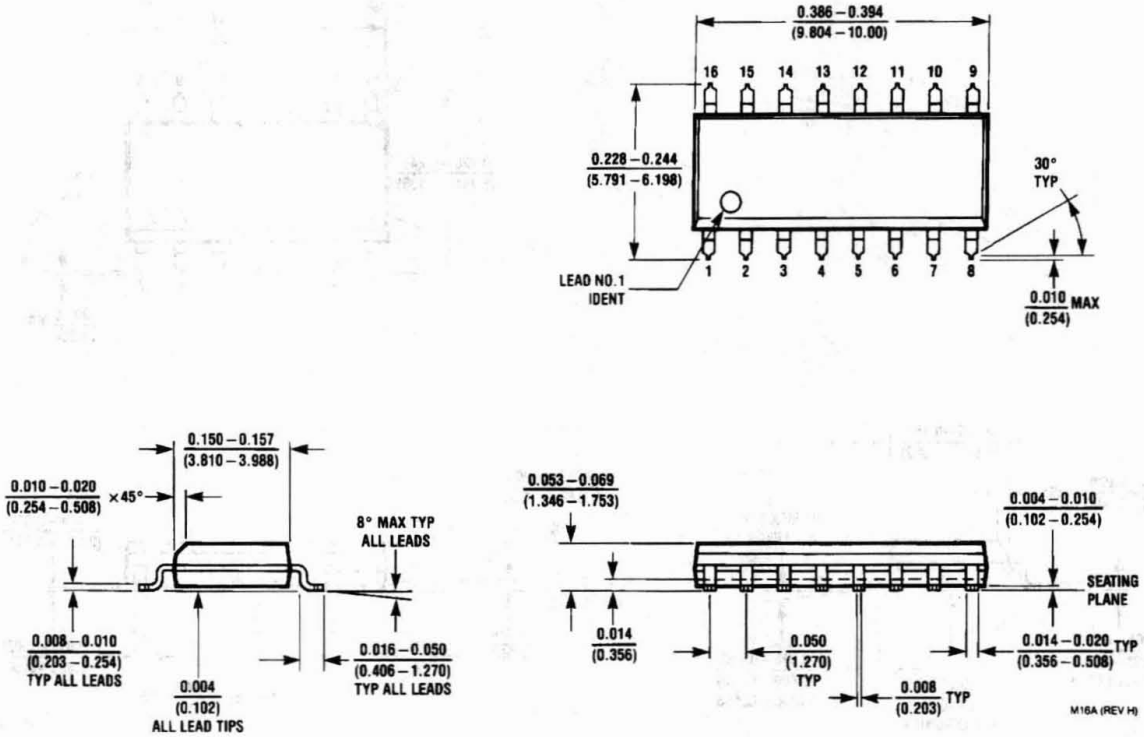
14 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14B

All dimensions are in inches (millimeters)



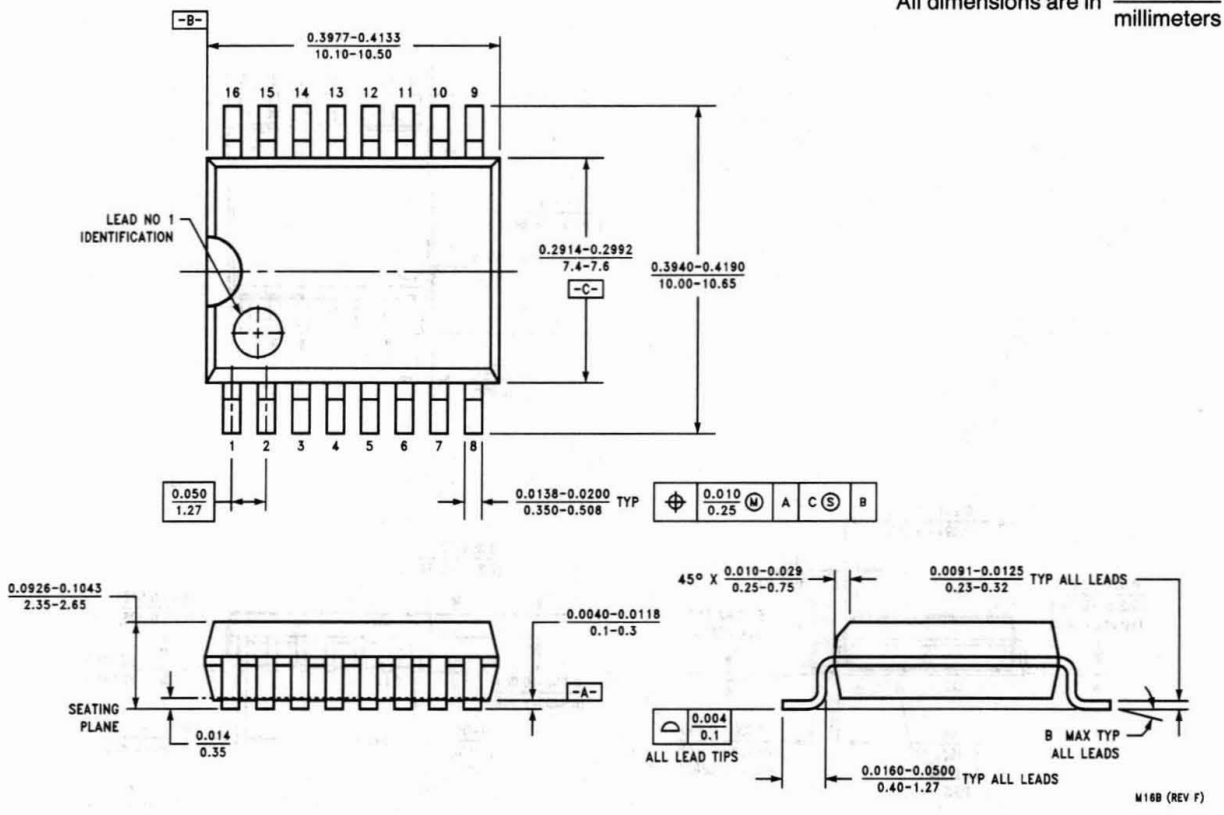
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

All dimensions are in inches (millimeters)



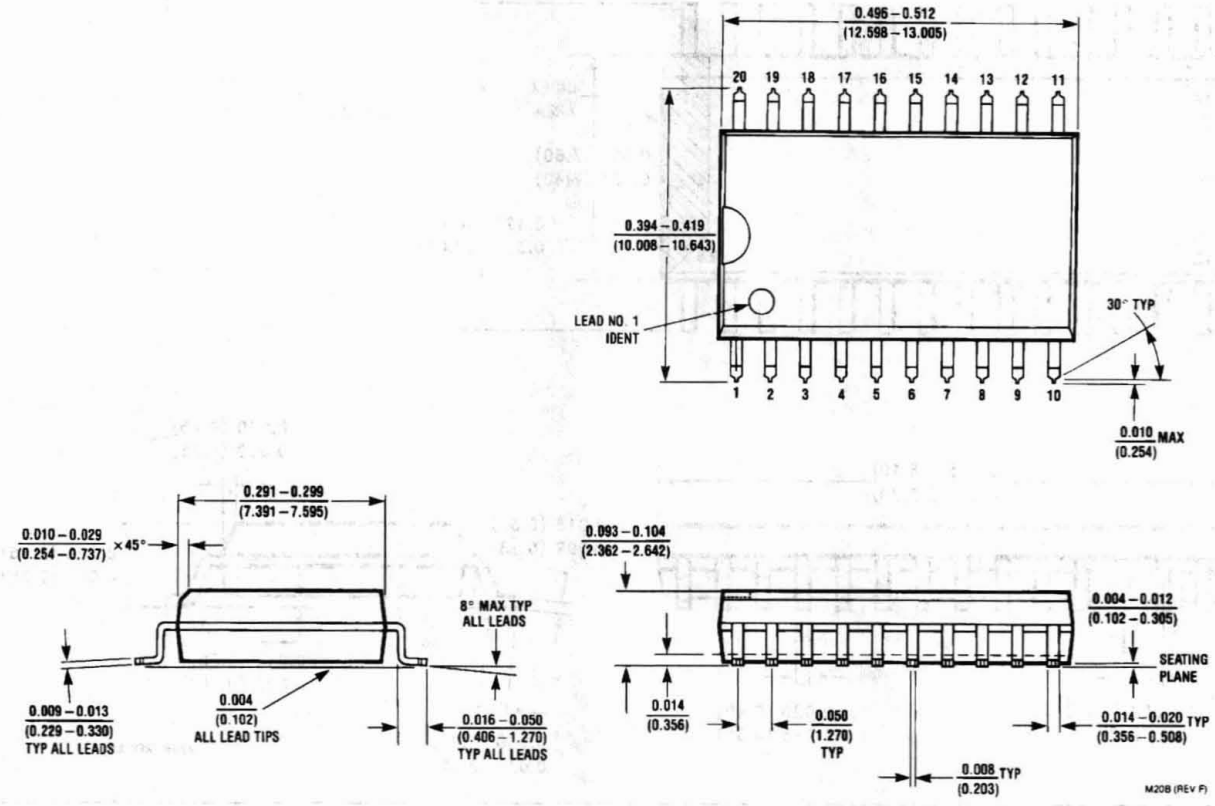
16 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



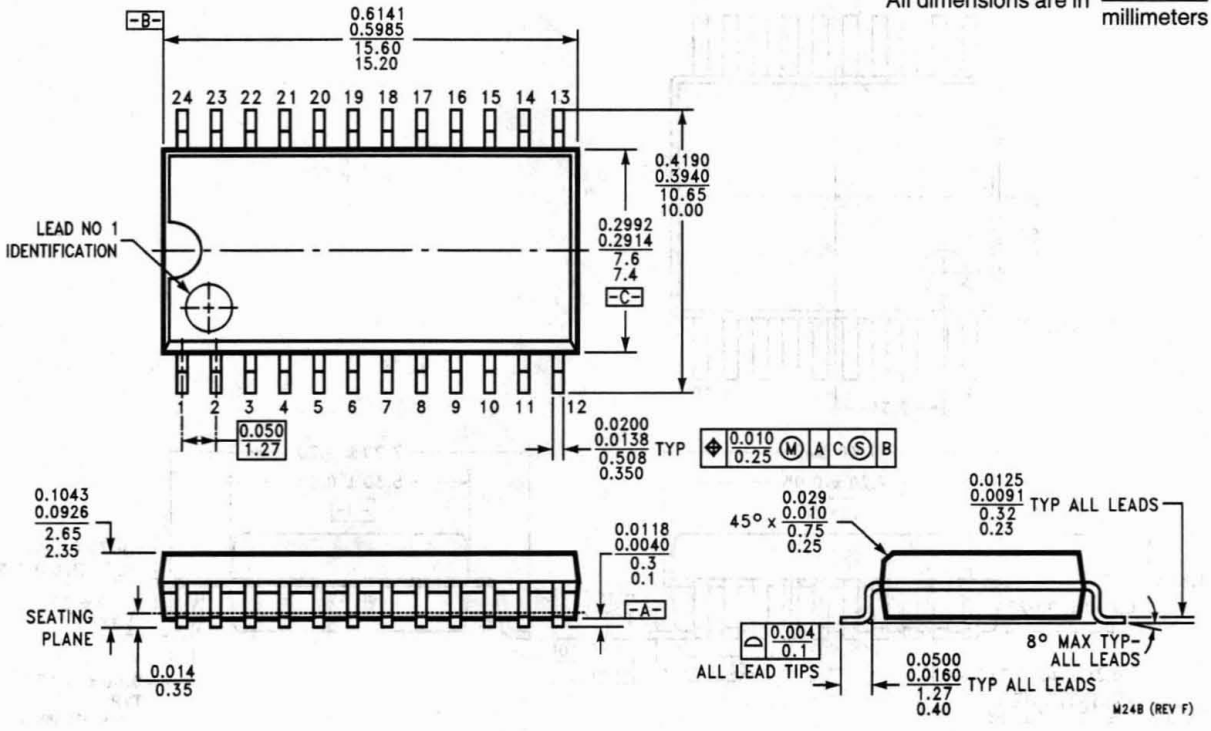
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B

All dimensions are in inches (millimeters)



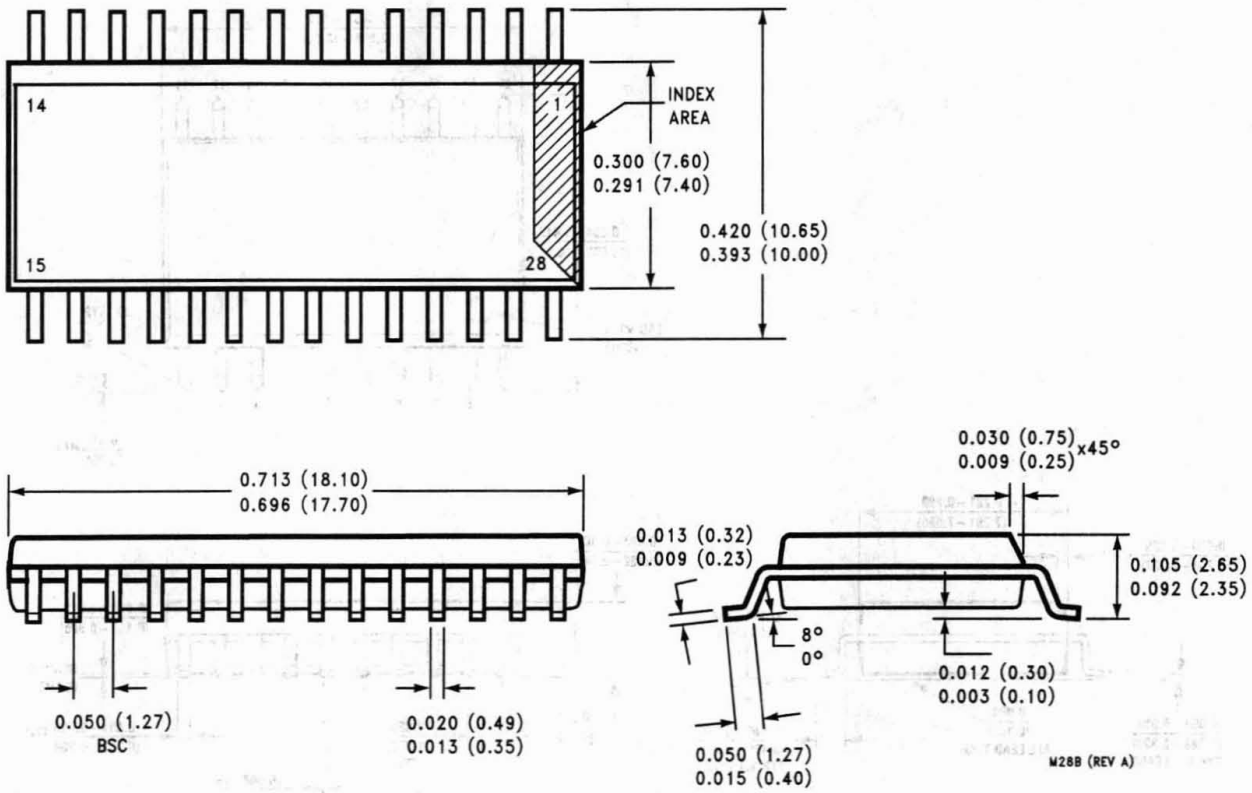
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



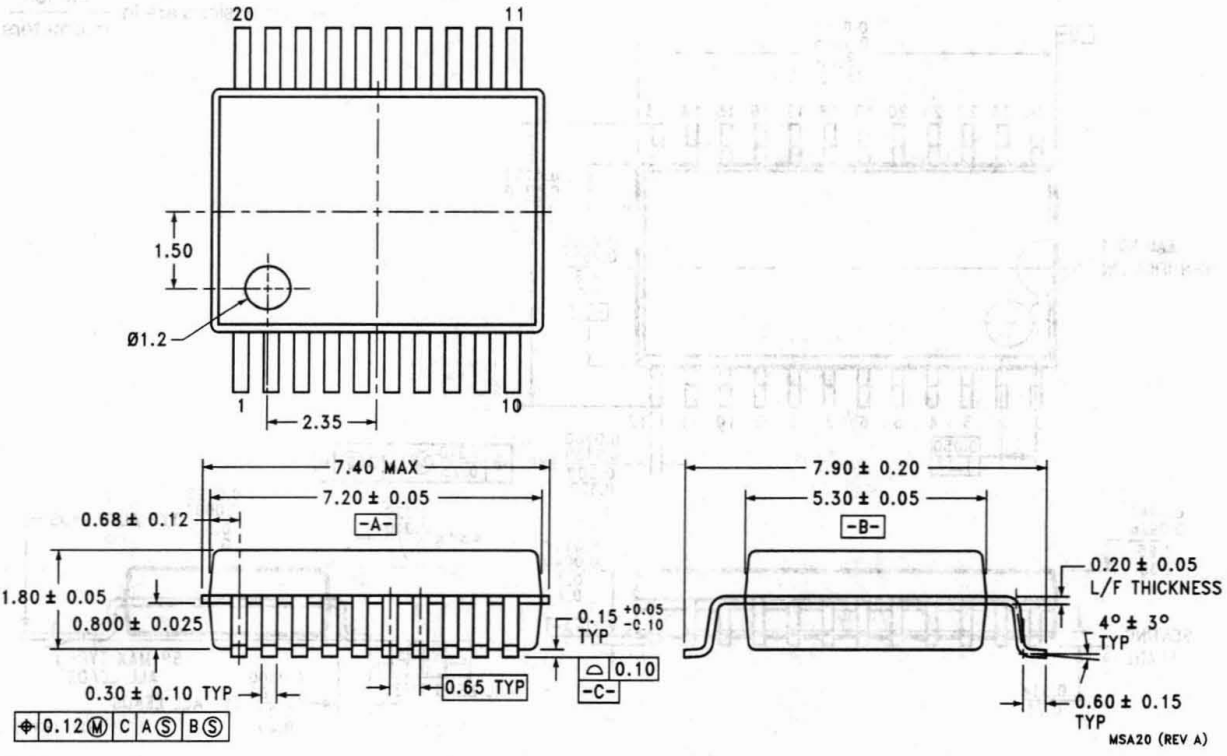
28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M28B

All dimensions are in inches (millimeters)



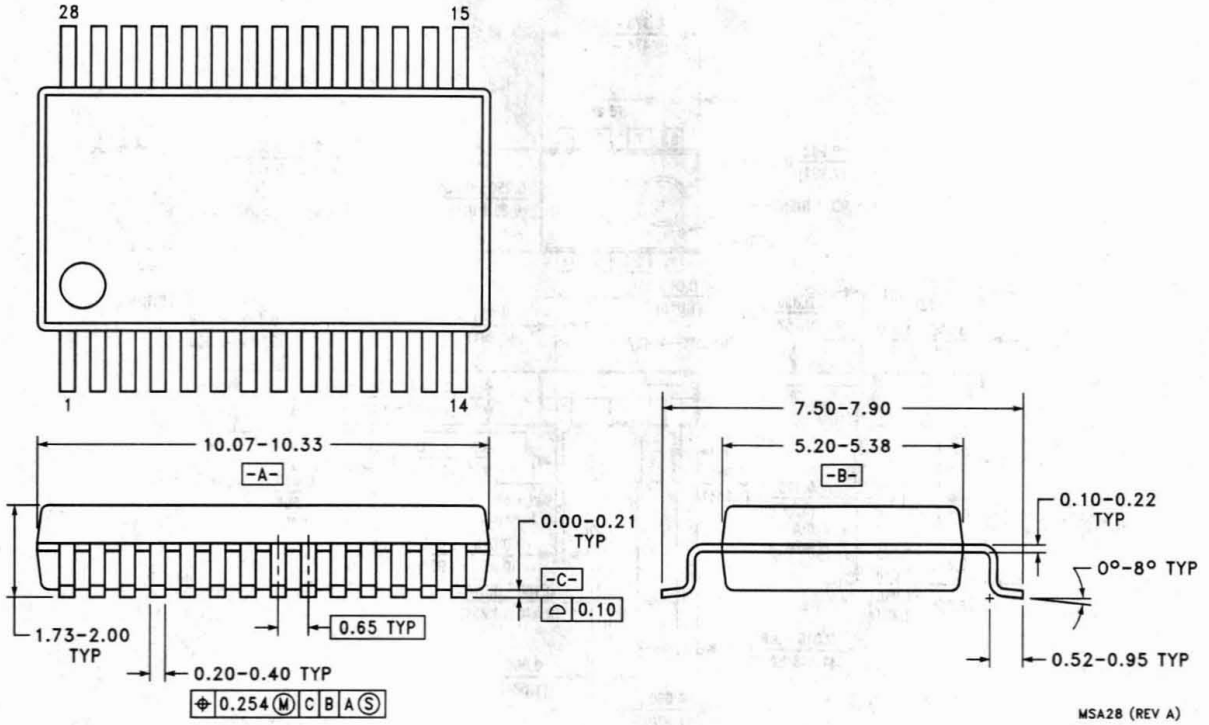
20 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA20

All dimensions are in millimeters



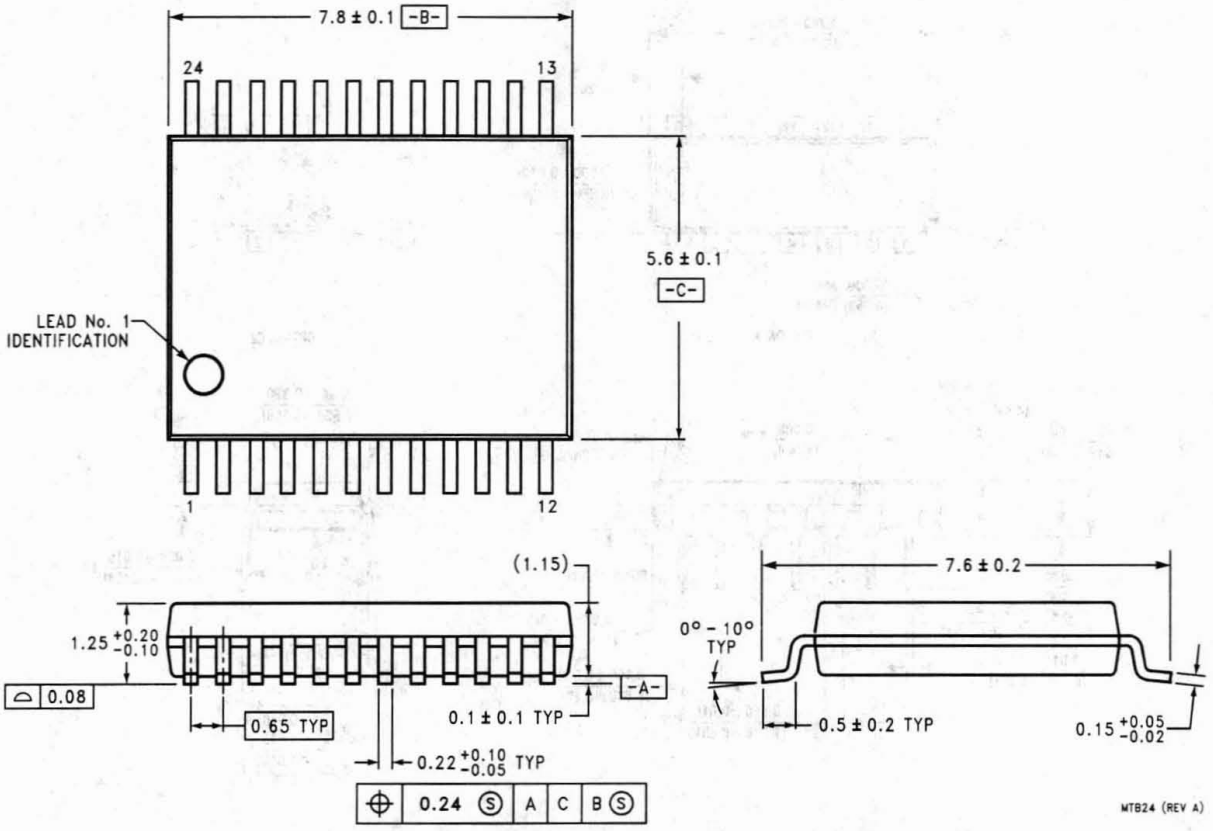
28 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA28

All dimensions are in millimeters



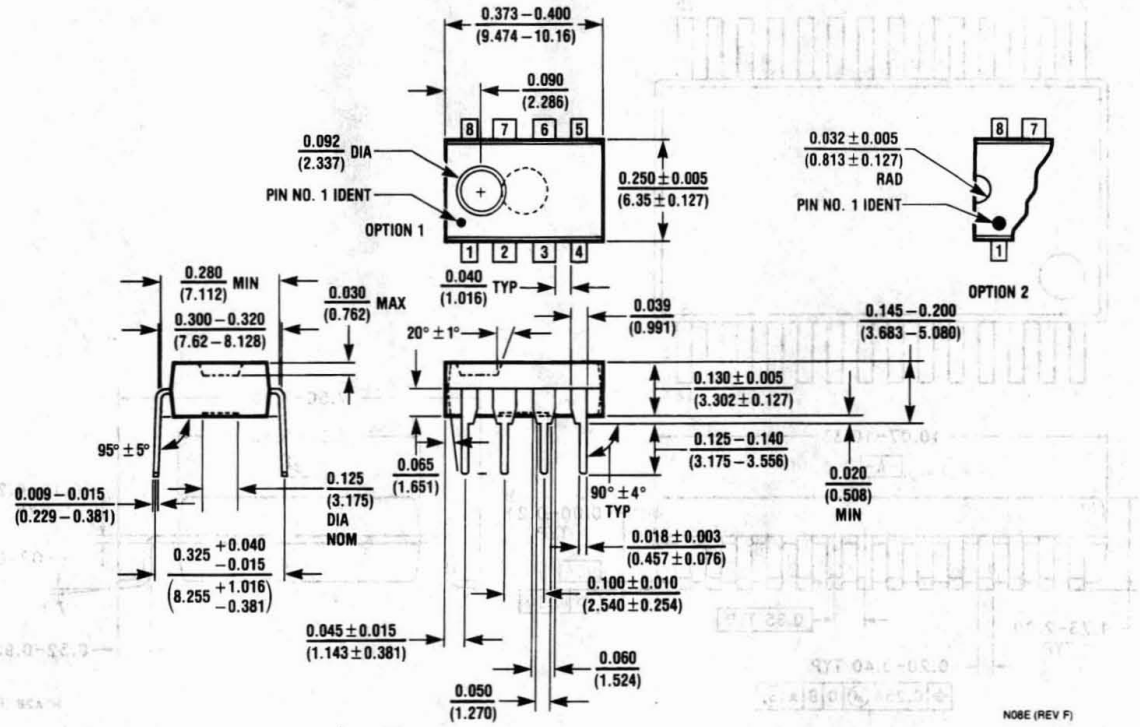
24 Lead Molded Thin Shrink Small Outline Package
NS Package Number MTB24

All dimensions are in millimeters



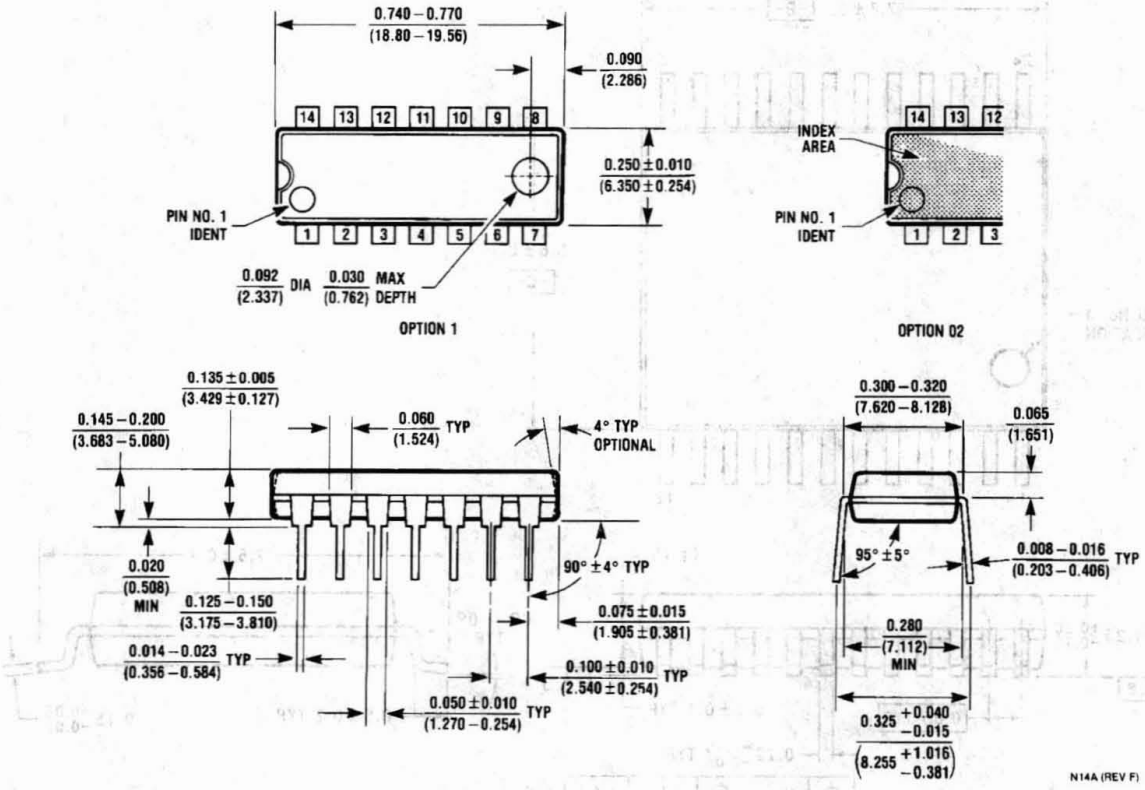
8 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N08E

All dimensions are in inches (millimeters)



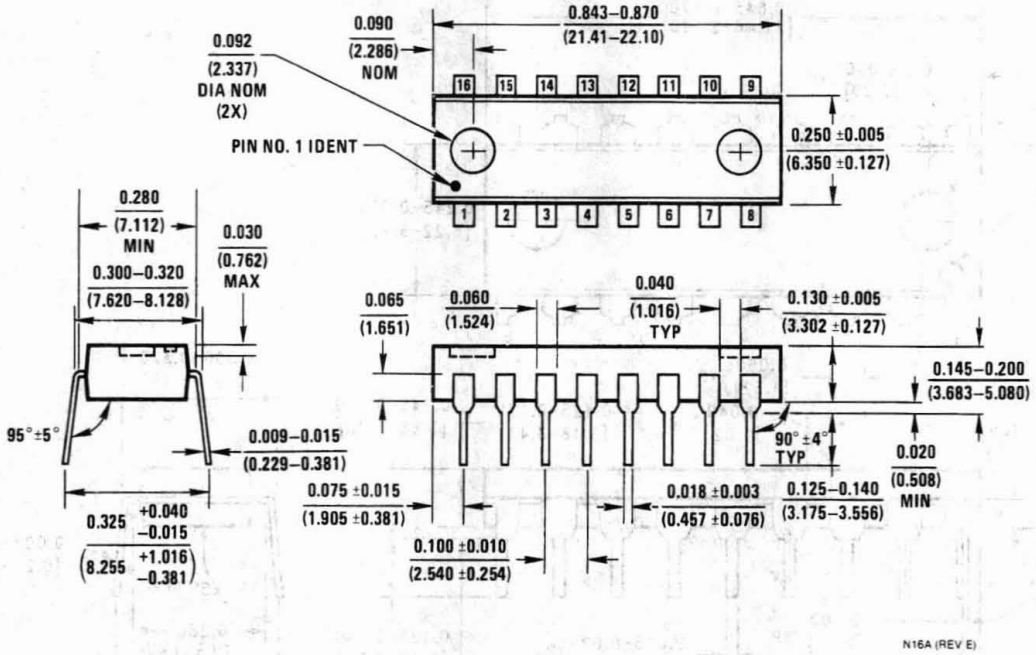
14 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N14A

All dimensions are in inches (millimeters)



16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16A

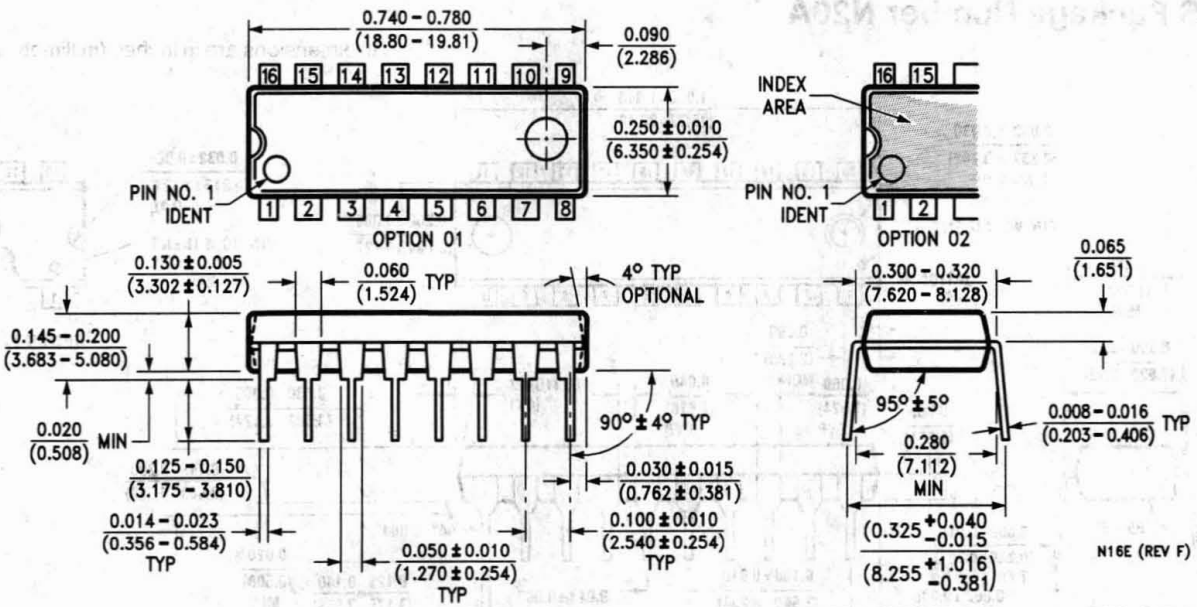
All dimensions are in inches (millimeters)



N16A (REV E)

16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16E

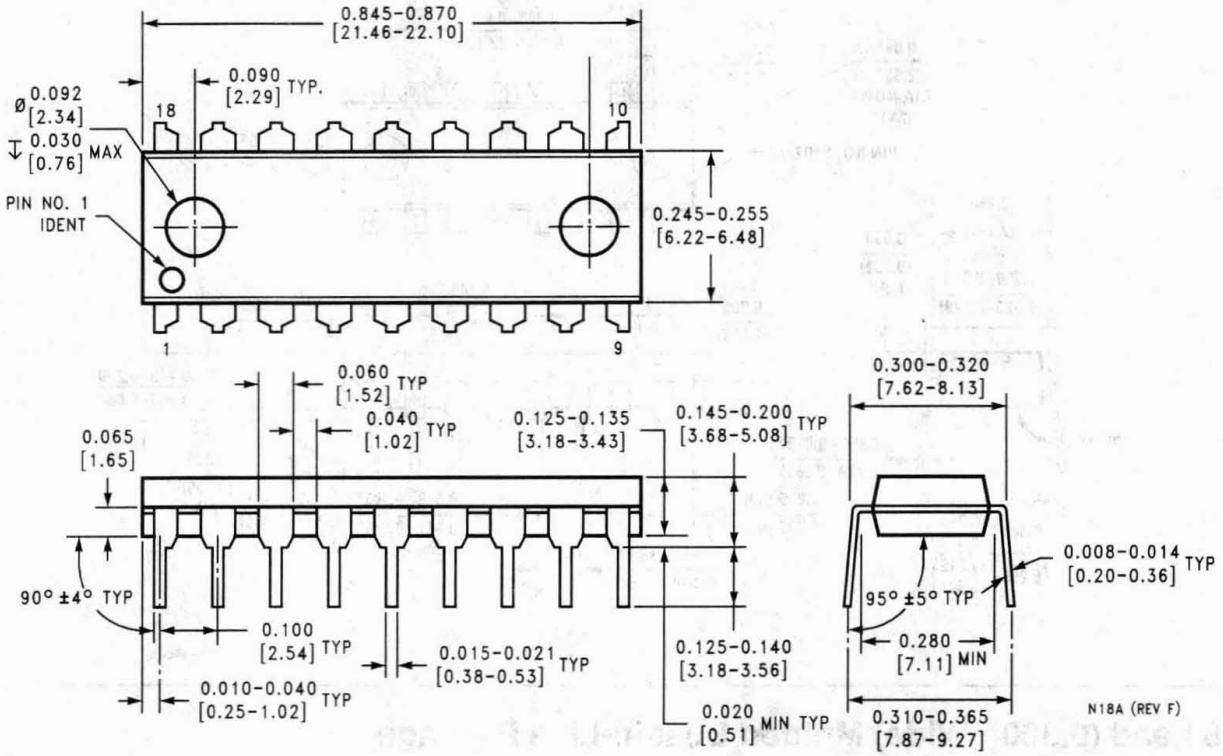
All dimensions are in inches (millimeters)



N16E (REV F)

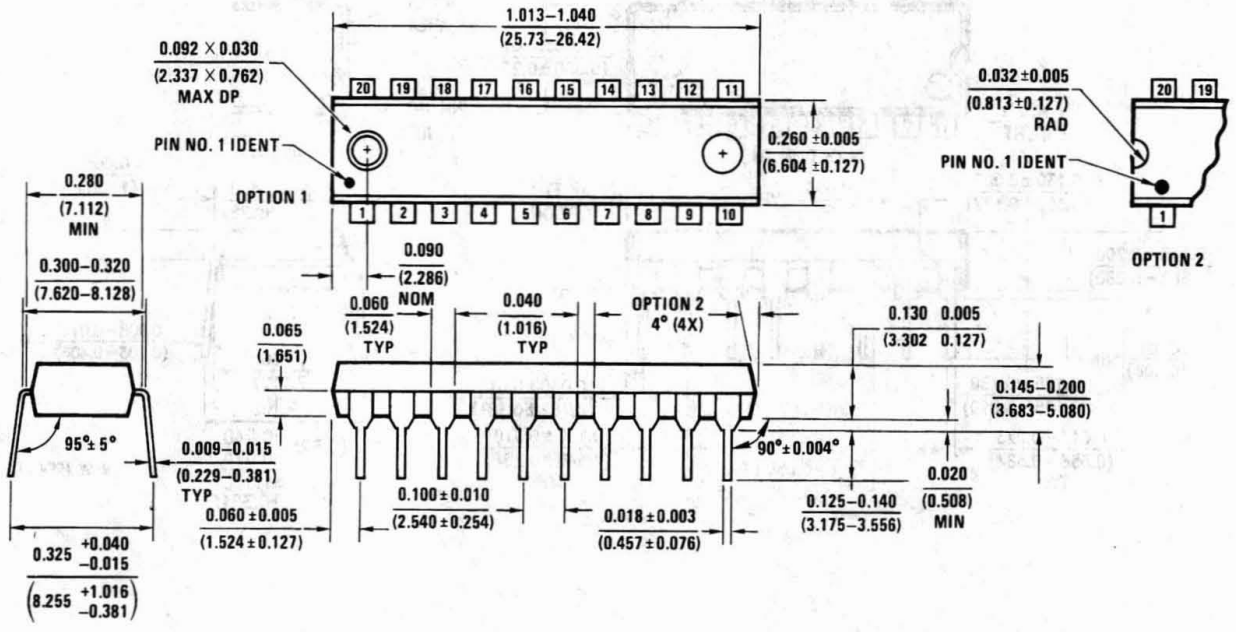
18 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N18A

All dimensions are in inches [millimeters]



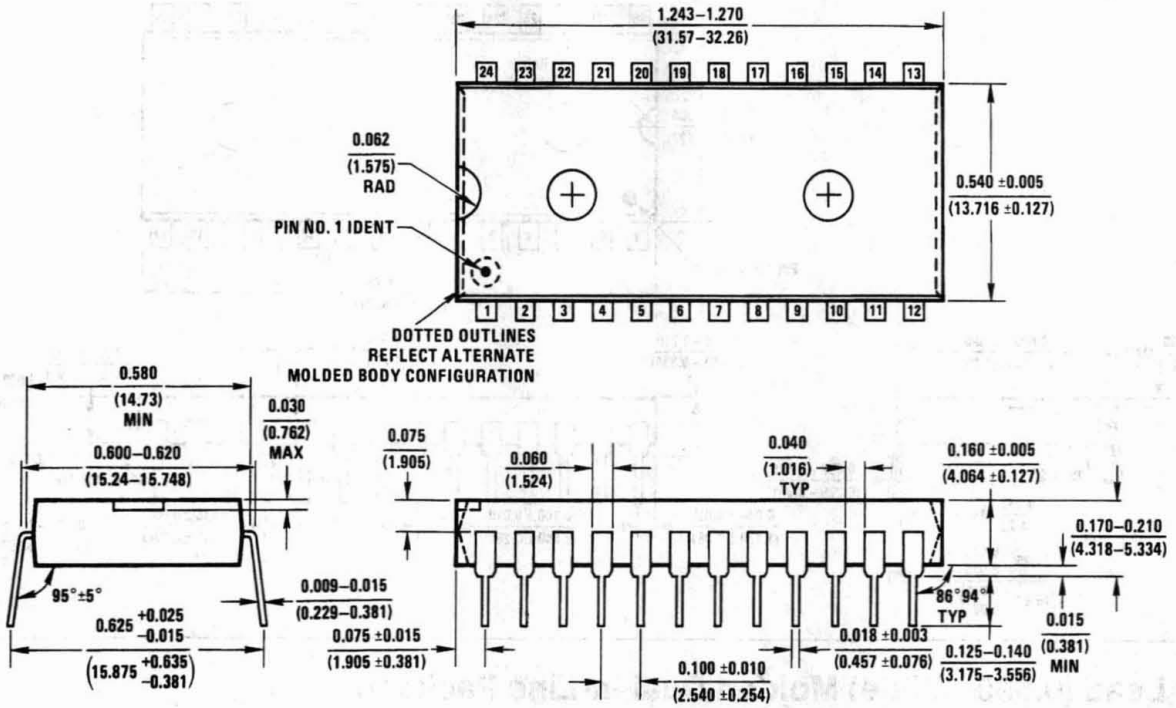
20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20A

All dimensions are in inches (millimeters)



24 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N24A

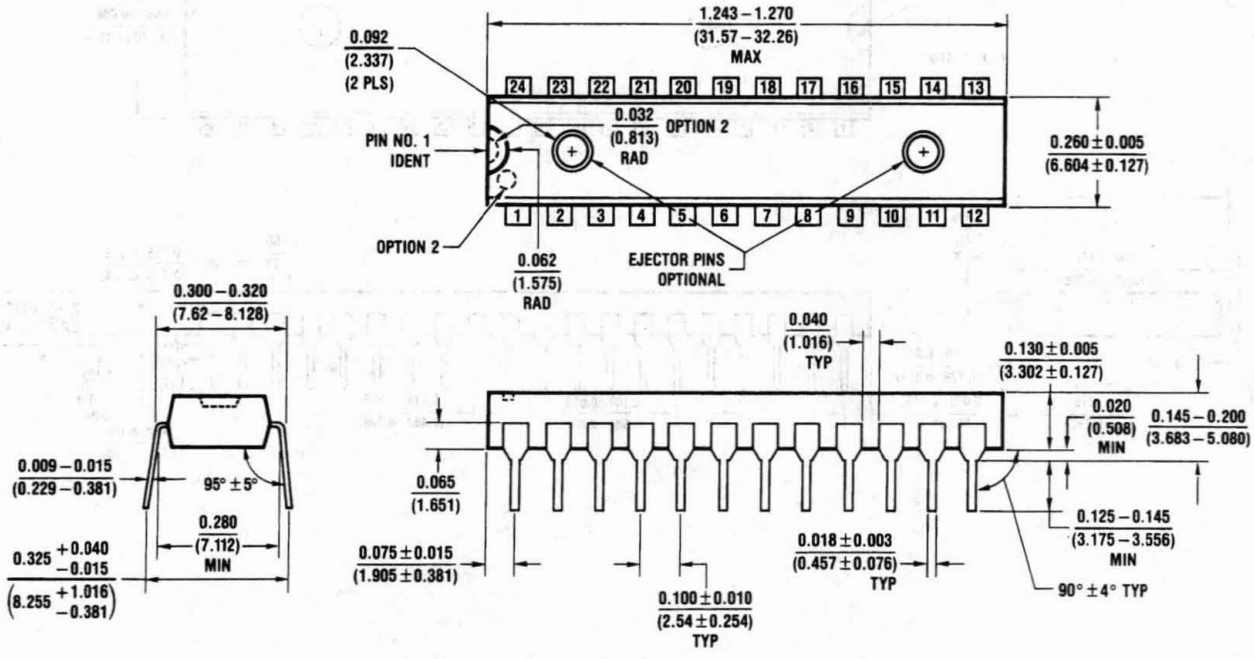
All dimensions are in inches (millimeters)



N24A (REV E)

24 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N24C

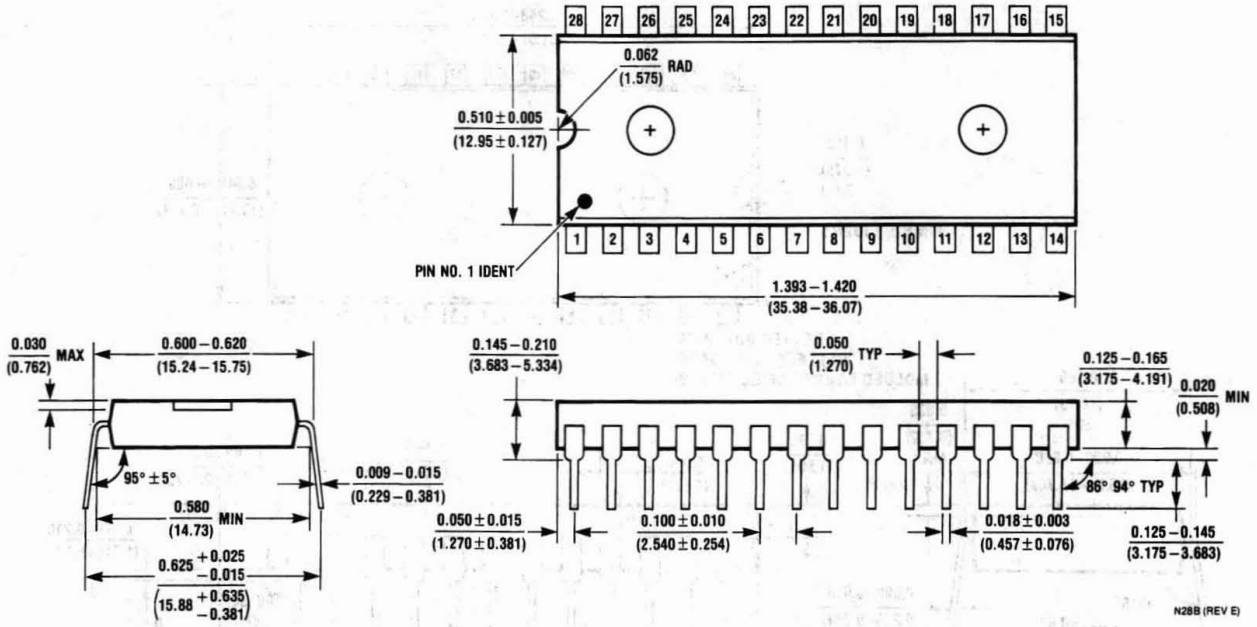
All dimensions are in inches (millimeters)



N24C (REV F)

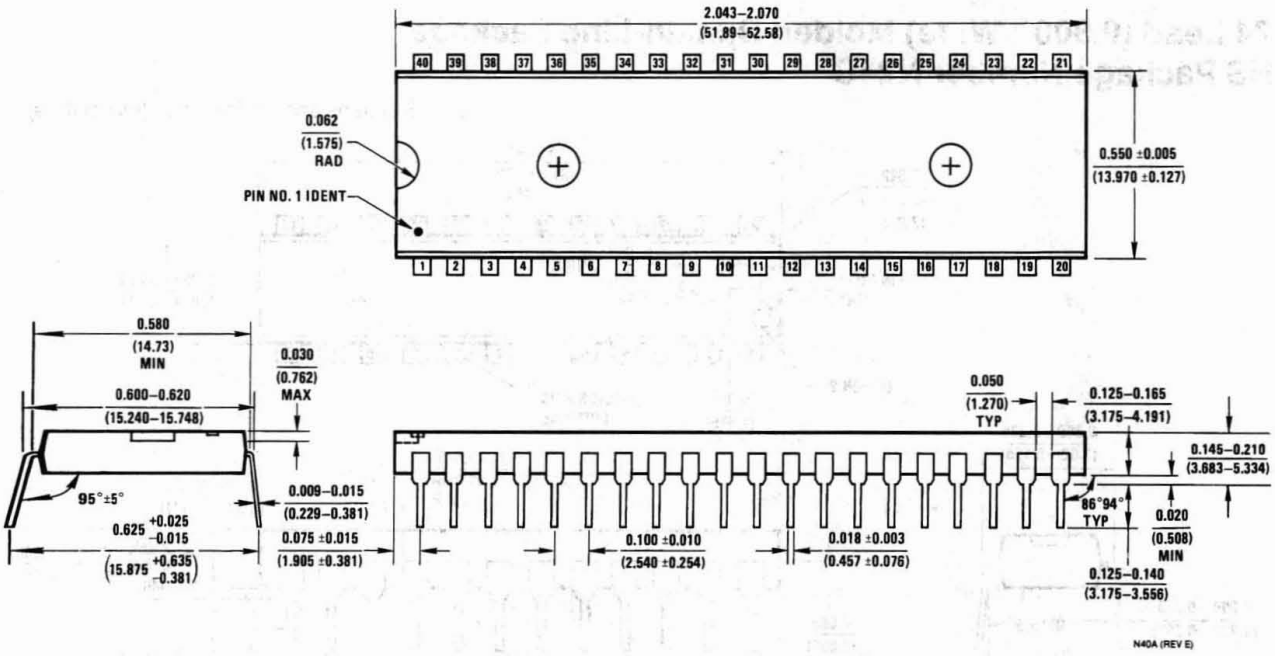
28 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N28B

All dimensions are in inches (millimeters)



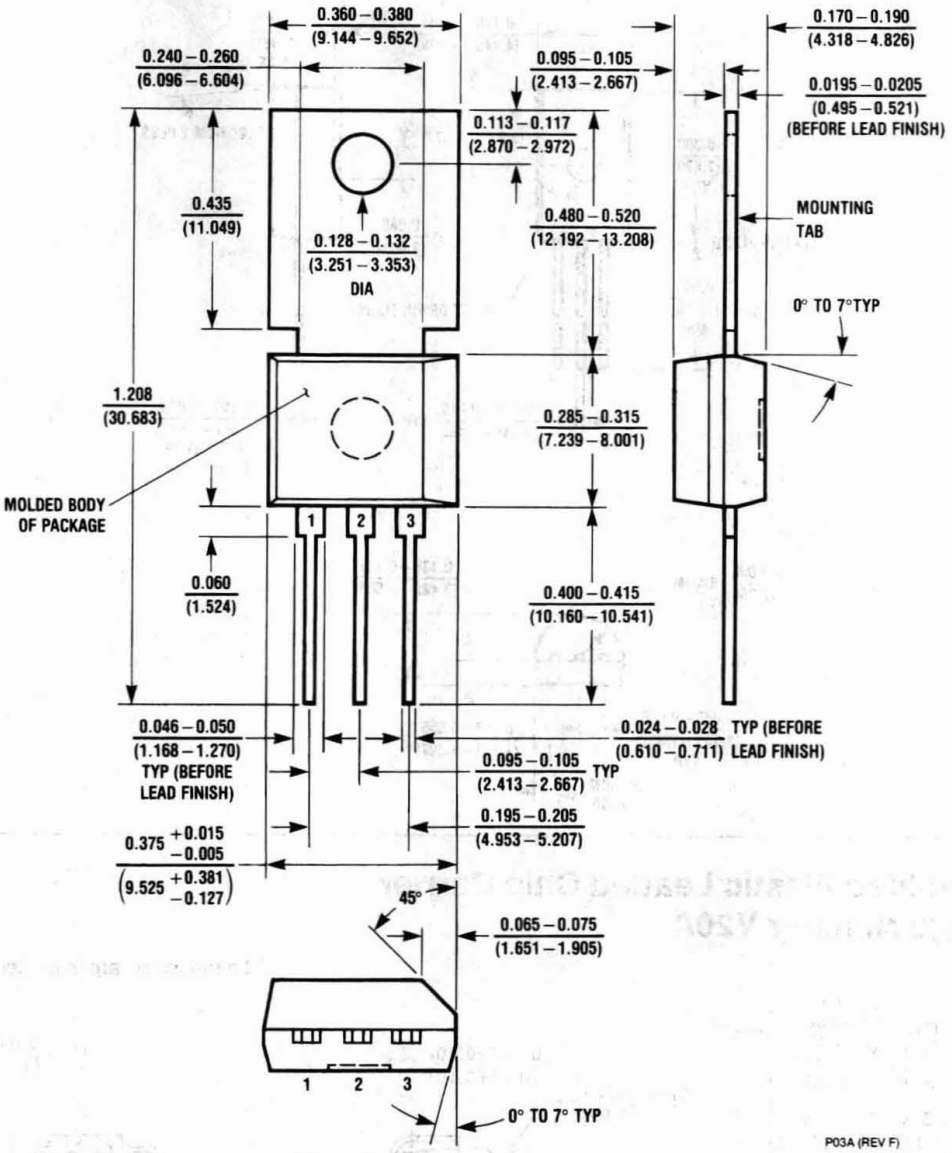
40 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N40A

All dimensions are in inches (millimeters)



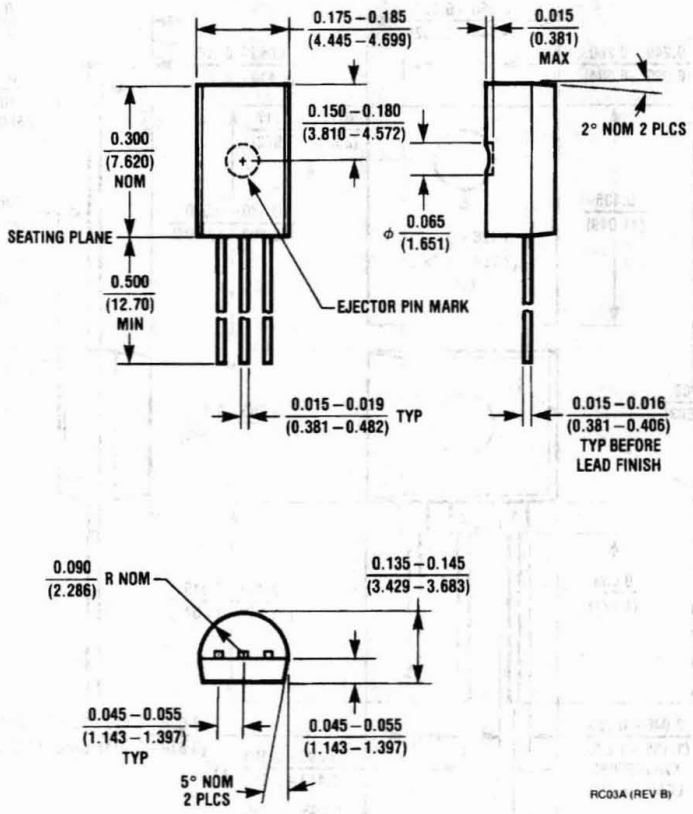
3 Lead Molded TO-202
NS Package Number P03A

All dimensions are in inches (millimeters)



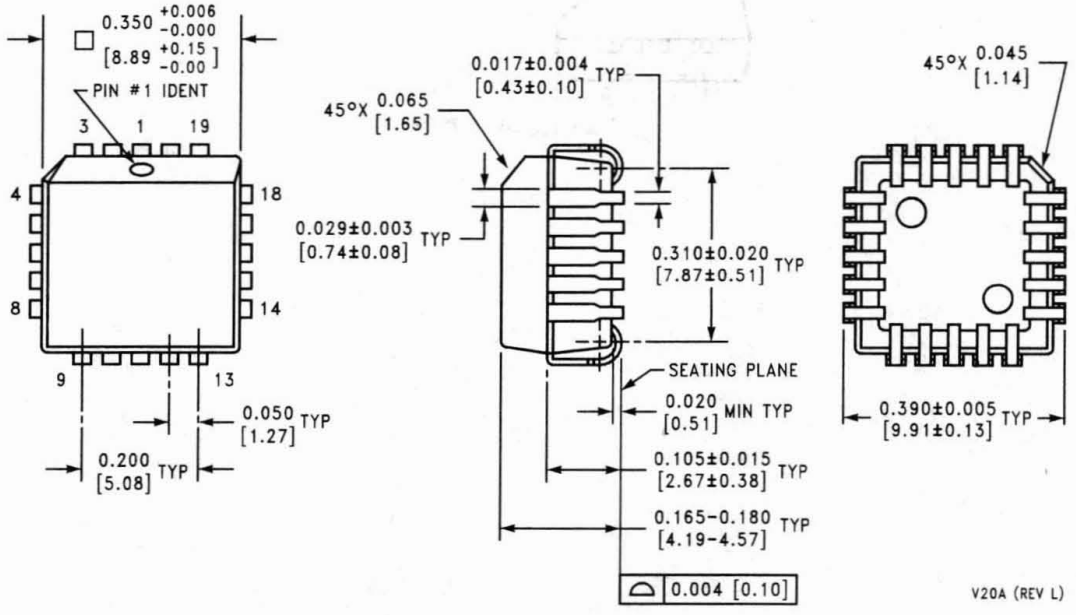
3 Lead Molded TO-226
NS Package Number RC03A

All dimensions are in inches (millimeters)



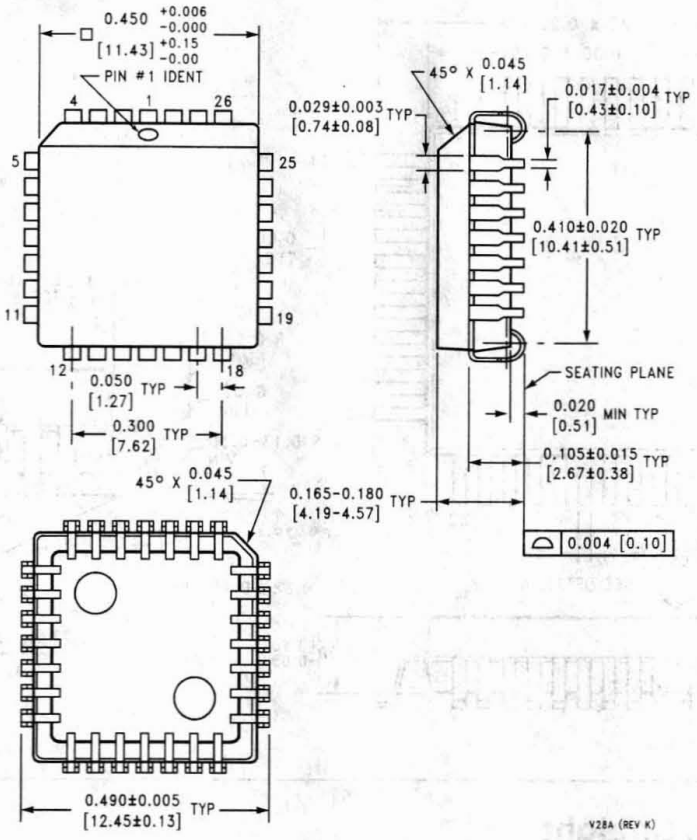
20 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V20A

All dimensions are in inches [millimeters]



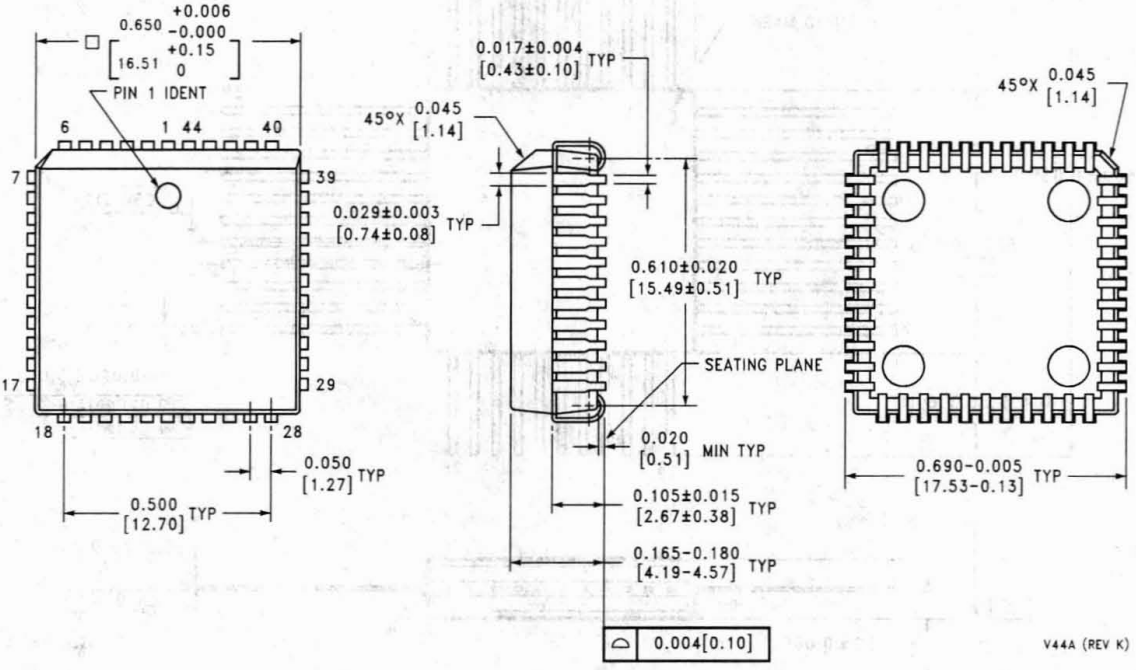
28 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A

All dimensions are in inches [millimeters]



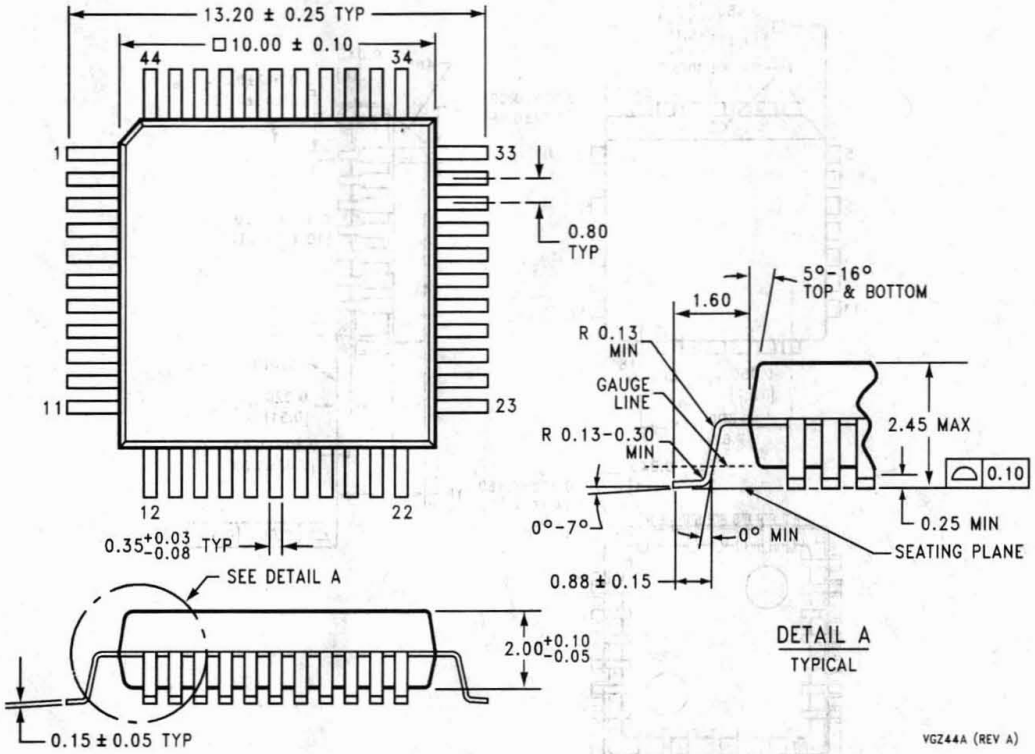
44 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V44A

All dimensions are in inches [millimeters]



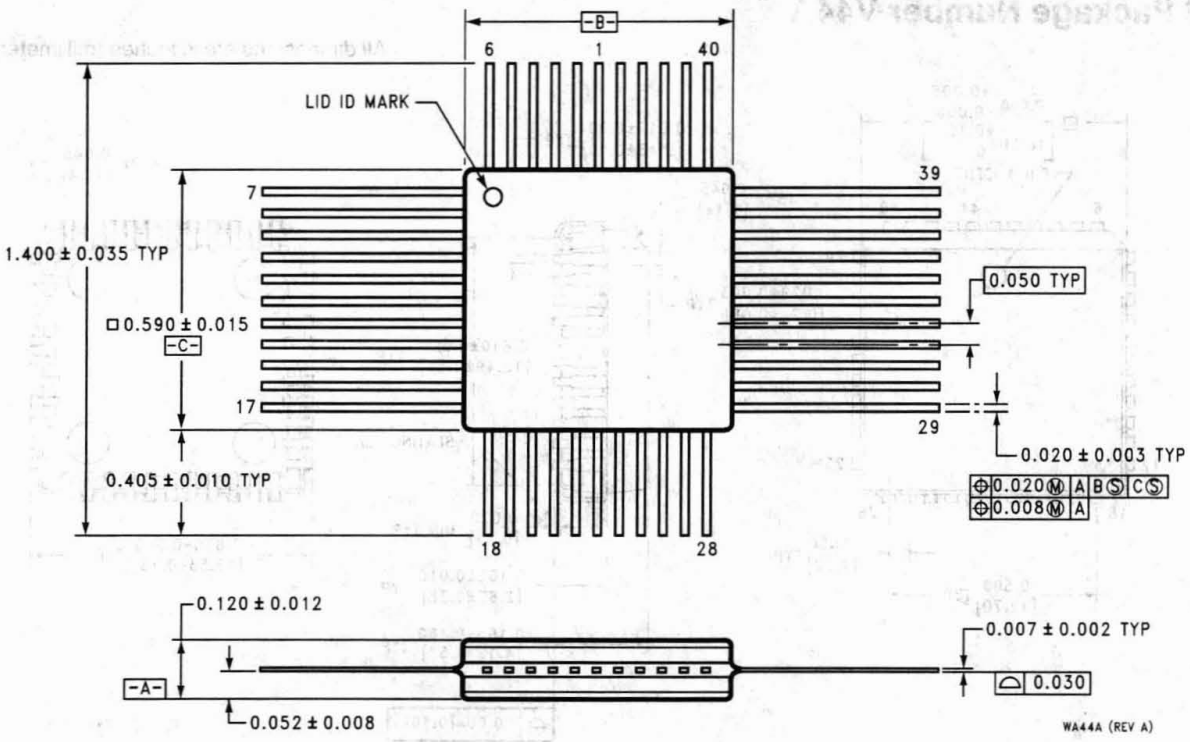
44 Lead (10mm x 10mm) Molded Plastic Quad Flat Package
NS Package Number VGZ44A

All dimensions are in millimeters



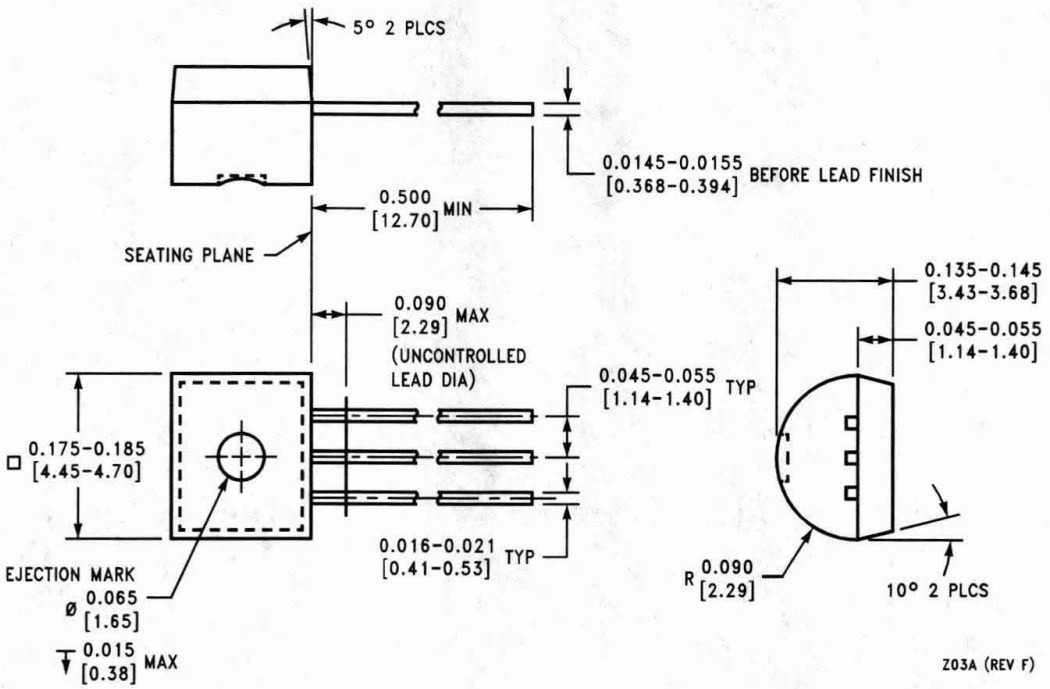
44 Lead Cerquad, Straight
NS Package Number WA44A

All dimensions are in inches



3 Lead Molded TO-92
NS Package Number Z03A

All dimensions are in inches [millimeters]



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ADVANCED BiCMOS LOGIC (ABTC, IBF, BiCMOS SCAN, LOW VOLTAGE BiCMOS, EXTENDED TTL TECHNOLOGY) DATABOOK—1994

ABTC/BCT Description and Family Characteristics • ABTC/BCT Ratings, Specifications and Waveforms
ABTC Applications and Design Considerations • Quality and Reliability • Integrated Bus Function (IBF) Introduction
54/74ABT3283 Synchronous Datapath Multiplexer • 74FR900/25900 9-Bit 3-Port Latchable Datapath Multiplexer
54/74ACTQ3283 32-Bit Latchable Transceiver with Parity Generator/Checker and Byte Multiplexing
SCAN18xxxA BiCMOS 5V Logic with Boundary Scan • 74LVT Low Voltage BiCMOS Logic
VME Extended TTL Technology for Backplanes

ALS/AS LOGIC DATABOOK—1990

Introduction to Advanced Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

APPLICATION SPECIFIC ANALOG PRODUCTS DATABOOK—1995

Audio Circuits • Video Circuits • Automotive • Special Functions • Surface Mount

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK—1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC
MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

CLOCK GENERATION AND SUPPORT (CGS) DESIGN DATABOOK—1994

Low Skew Clock Buffers/Drivers • Video Clock Generators • Low Skew PLL Clock Generators
Crystal Clock Generators

COP8™ DATABOOK—1994

COP8 Family • COP8 Applications • MICROWIRE/PLUS Peripherals • COP8 Development Support

CROSSVOLT™ LOW VOLTAGE LOGIC SERIES DATABOOK—1994

LCX Family • LVX Translator Family • LVX Bus Switch Family • LVX Family • LVQ Family • LVT Family

DATA ACQUISITION DATABOOK—1995

Data Acquisition Systems • Analog-to-Digital Converters • Digital-to-Analog Converters • Voltage References
Temperature Sensors • Active Filters • Analog Switches/Multiplexers • Surface Mount

DATA ACQUISITION DATABOOK SUPPLEMENT—1992

New devices released since the printing of the 1989 Data Acquisition Linear Devices Databook.

DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK—1989

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors
Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

DRAM MANAGEMENT HANDBOOK—1993

Dynamic Memory Control • CPU Specific System Solutions • Error Detection and Correction
Microprocessor Applications

EMBEDDED CONTROLLERS DATABOOK—1992

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

FDDI DATABOOK—1994

Datasheets • Application Notes

F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1992

Family Overview • 300 Series (Low-Power) Datasheets • 100 Series Datasheets • 11C Datasheets
Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations
Power Distribution and Thermal Considerations • Testing Techniques • 300 Series Package Qualification
Quality Assurance and Reliability • Application Notes

FACT™ ADVANCED CMOS LOGIC DATABOOK—1993

Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1990

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—1990

Reprint of 1987 Fairchild FAST Applications Handbook
Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics

HIGH-PERFORMANCE BUS INTERFACE DATABOOK—1994

QuickRing • Futurebus+ /BTL Devices • BTL Transceiver Application Notes • Futurebus+ Application Notes
High Performance TTL Bus Drivers • PI-Bus • Futurebus+ /BTL Reference

IBM DATA COMMUNICATIONS HANDBOOK—1992

IBM Data Communications • Application Notes

INTERFACE: DATA TRANSMISSION DATABOOK—1994

TIA/EIA-232 (RS-232) • TIA/EIA-422/423 • TIA/EIA-485 • Line Drivers • Receivers • Repeaters
Transceivers • Low Voltage Differential Signaling • Special Interface • Application Notes

LINEAR APPLICATIONS HANDBOOK—1994

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LOCAL AREA NETWORKS DATABOOK—1993 SECOND EDITION

Integrated Ethernet Network Interface Controller Products • Ethernet Physical Layer Transceivers
Ethernet Repeater Interface Controller Products • Token-Ring Interface Controller (TROPIC)
Hardware and Software Support Products • FDDI Products • Glossary and Acronyms

LOW VOLTAGE DATABOOK—1992

This databook contains information on National's expanding portfolio of low and extended voltage products. Product datasheets included for: Low Voltage Logic (LVQ), Linear, EPROM, EEPROM, SRAM, Interface, ASIC, Embedded Controllers, Real Time Clocks, and Clock Generation and Support (CGS).

MASS STORAGE HANDBOOK—1989

Rigid Disk Pulse Detectors • Rigid Disk Data Separators/Synchronizers and ENDECs
Rigid Disk Data Controller • SCSI Bus Interface Circuits • Floppy Disk Controllers • Disk Drive Interface Circuits
Rigid Disk Preamplifiers and Servo Control Circuits • Rigid Disk Microcontroller Circuits • Disk Interface Design Guide

MEMORY DATABOOK—1994

FLASH • CMOS EPROMs • CMOS EEPROMs • PROMs • Application Notes

MEMORY APPLICATIONS HANDBOOK—1994

FLASH • EEPROMs • EPROMs • Application Notes

OPERATIONAL AMPLIFIERS DATABOOK—1995

Operational Amplifiers • Buffers • Voltage Comparators • Active Matrix/LCD Display Drivers
Special Functions • Surface Mount

PACKAGING DATABOOK—1993

Introduction to Packaging • Hermetic Packages • Plastic Packages • Advanced Packaging Technology
Package Reliability Considerations • Packing Considerations • Surface Mount Considerations

POWER IC's DATABOOK—1995

Linear Voltage Regulators • Low Dropout Voltage Regulators • Switching Voltage Regulators
Motion Control • Surface Mount

PROGRAMMABLE LOGIC DEVICE DATABOOK AND DESIGN GUIDE—1993

Product Line Overview • Datasheets • Design Guide: Designing with PLDs • PLD Design Methodology
PLD Design Development Tools • Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1993

3-Volt Low Voltage Real Time Clocks • Real Time Clocks and Timer Clock Peripherals • Application Notes

RELIABILITY HANDBOOK—1987

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
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